DESIGN AND ANALYSIS OF A SINGLE PHASE SINGLE SWITCH ĈUK AND SEPIC AC-DC CONVERTER WITH IMPROVED PERFORMANCE

By

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APPROVAL

This thesis titled **"DESIGN AND ANALYSIS OF A SINGLE PHASE SINGLE SWITCH ĈUK AND SEPIC AC-DC CONVERTER WITH IMPROVED PERFORMANCE"** submitted by Md. Shamsul Arifin, Roll No. 0413062120, Session: April 2013 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of Masters of Science in Electrical and Electronic Engineering on January 30, 2016.

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Signature of the candidate

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DEDICATED

TO

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LIST OF ACRONYMS

AC: Alternating Current

CCM: Continuous Conduction Mode

DCM: Discontinuous Conduction Mode

DC: Direct Current

DM: Differential Mode

IEC: International Electro technical Committee

IEEE: Institute of Electrical and Electronics Engineers

IGBT: Insulated Gate Bipolar Transistor

LN: Line-to-neutral

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

PFC: Power Factor Correction

PWM: Pulse Width Modulation

RMS: Root Mean Square

SEPIC: Single-Ended Primary-Inductor Converter

THD: Total Harmonic Distortion

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ABSTRACT

Single phase full wave bridge rectifiers are nonlinear in nature and draws non sinusoidal current from a sinusoidal voltage source. This causes low input power factor and high input current THD and causes a lot of problems in sensitive electronic equipment and high power equipment in power system. There are several methods including passive and active filtering to solve the problem. Passive filtering uses bulky sized inductors and capacitors, while active filtering uses switching mode regulators to improve the input current and power factor. The inductors and capacitors required in active filtering are smaller sized than that of passive filters. Generally, switching is performed in output side of the rectifier, which makes input current high frequency switched. Then a passive filter is used to get low THD and high input power factor. In this thesis, two new topologies of single phase single switch AC-DC converter using Ĉuk and SEPIC conversion is proposed. These converters' input current is chopped at high frequency during positive and negative cycle by a single semiconductor switch to get step up/step down AC to DC conversion, instead of using a single phase rectifier followed by a DC-DC converter or using a bridge rectifier with two diodes and two switches. Comparison is made between proposed and conventional circuit under same Load and operating conditions. The proposed circuit shows better performance i.e. higher power factor and lower THD than conventional one. The efficiency of these converters is also high. No additional control scheme is required to achieve these advantages. The feedback controller circuits are also introduced to the proposed converters to achieve regulated output voltage. The results after connecting the feedback controller are also presented in the thesis.

CHAPTER 1

INTRODUCTION

1.1 Introduction

Telecommunications and computer industries have become essential part of modern society. Currently electric vehicles are occupying the place of conventional vehicles due to their environment friendly technology. DC power supply is necessary to run these devices, which consist of battery storage and charging system. Moreover renewable energy specially the solar energy is becoming a dominating power source in almost every country. DC power conditioning and processing is a major challenge in these sectors. The DC power supply is also required in operating sensitive electronic devices, separating magnets, particle acceleration, fusion, electrolyte cells, electro refining, chemical process, industrial cranes, protective and measuring instrument like relay and in DC motors. In most of the cases this DC power supply has come from AC supply. That's why input power factor, input current THD and efficiency are the major issues to be considered while using AC-DC conversion.

1.2 Background

Single phase full wave bridge rectifier draws non sinusoidal currents from sinusoidal voltage source due to its non-linear characteristics. Several power quality problems arise at source side due to this non-linear characteristic. These problems include low input power factor, high input current THD, failure of transformer due to overheating, interference at communication channel, harmonic pollution at power system [1,2] etc. Due to harmonic pollution at power system power supply is interrupted, which cause malfunction or damage of sensitive electric device. Restrictions on current and voltage harmonics are maintained through IEEE 519-1992 and IEC 61000-3-2/IEC 61000-3-4[3] standard in most of the countries.

There are several methods to solve the problem of harmonic pollution in power system and new methods are still being investigated. One of these methods is to use a passive filter in input side. This filter consists of an inductor and a capacitor, which are bulky in size. This filter can improve THD but input power factor remains low. Moreover using bulky inductor and capacitor imposes a restriction on using it for high power application. To overcome these problems switch mode regulator has been introduced. This method employs a single phase

rectifier followed by a DC-DC converter. This method is also known as active filtering [4-10]. In this case the input filter required is relatively smaller than passive filter. Moreover improved input power factor is achieved in this method.

The Boost DC-DC converter is commonly used after rectifier for power factor correction. Buck, Buck-Boost etc. are also used to get different input/output voltage gain relationship [10-18]. The DC-DC converters chop the input current at high frequency which can be filtered with a low pass filter to get near sinusoidal input current with high input power factor and low THD.

The DC-DC converter use unidirectional switch for switching purpose, which may be a BJT, MOSFET or IGBT. The boost rectifier must be operated in critical mode [19-22] in boost regulated AC-DC conversion. In this case the switch should be ON at the instant of zero current in the boost diode. This needs variable switching frequency operation of the DC-DC converter with the change of load or source voltage. Another approach for boost regulated rectifier involves controlling to a constant level of the average current of the boost diode [18-22]. To do this the duty cycle must be modulated.

In this thesis, two new single phase single switch AC-DC converters on Ĉuk and SEPIC topologies of high performance are reported. Very few remarkable works are done with Ĉuk and SEPIC topology based AC-DC converter. Ĉuk topology has several advantages over Buck-Boost topology like continuous input and output current. Moreover Ĉuk converter supplies energy to load both when switch is open and close. Ĉuk circuit has also reduced circuit parameters than SEPIC converter, hence reduces cost [3, 23-26]. Similarly SEPIC topology has advantage of less active components than conventional Boost+Buck or Buck+Boost converter. It also has other advantages like low noise operation, simple control scheme etc. Moreover SEPIC is more stable and produces less power ripples than Ĉuk converter. Ĉuk topology is frequently used in renewable energy sector [25-26].

The proposed converters chop input current by a single switch. These converters are different from conventional DC-DC converter regulated rectifiers because input current switching ensures input AC current to be almost in phase with input voltage without any control scheme. This would result almost sinusoidal input current with using of small filter and also ensure good input power factor. The proposed converters provide step up/step down output DC voltage with the duty cycle control of switch. The efficiency is also high for both converters.

1.3 Goal of the thesis

The objectives of the proposed work are

1. To develop and design of schemes for high input power factor, high efficiency single switch AC-DC converter.

2. To select the circuit parameters to achieve low THD, high input power factor and efficiency.

3. To analyze the performance of proposed circuits by simulation.

4. To compare the performance of proposed schemes with conventional switch mode AC-DC SEPIC and Ĉuk converter (rectifier followed by DC-DC converter).

1.4 Thesis Organization

This thesis consists of seven chapters.

Chapter-1 is the introduction of the thesis work and provides a brief discussion about back ground and objective of this research.

Chapter-2 illustrates the types of Diode Rectifier, their construction, operation principle, wave shapes and performance of these rectifiers.

Chapter-3 describes the operation of linear regulator circuit and a simple chopper circuit. Then it illustrates types of dc-dc converter, their construction, operation principle wave shapes etc.

Chapter-4 discusses the idea of power factor and power factor correction, necessity of power factor correction, methods of power factor correction and selection of appropriate method of power factor correction in details.

Chapter-5 presents the proposed converter based on Ĉuk topology. It describes the circuit configurations, analyzes their operation and presents their performance under different frequencies and different load conditions.

Chapter-6 presents the proposed converter based on SEPIC topology. It describes the circuit configurations, analyzes their operation and presents their performance under different frequencies and different load conditions.

Chapter-7 concludes the thesis with a summary on the research and suggests for future works.

CHAPTER 2

RECTIFIERS

2.1 Introduction

A rectifier is a circuit that converts an AC supply to a unidirectional output. Diodes are extensively used in rectifier circuits.

Diode rectifiers are of two types:

1. Single phase Diode rectifier.

2. Three phase Diode rectifier.

There are two types of single-phase diode rectifier:

1. Full wave Rectifier.

2. Half wave Rectifier.

There are also two types of three-phase diode rectifier:

1. Full wave Rectifier.

2. Half wave Rectifier.

In the following subsections, the operations of these rectifier circuits are investigated. To avoid complexity the diodes are considered to be ideal, that is, they have zero forward voltage drop and reverse recovery time. Furthermore, it is assumed that the load is purely resistive such that load voltage and load current have similar waveforms.

2.2 Single-Phase Half-Wave Rectifiers

The single-phase diode rectifier is the simplest rectifier. A single-phase half-wave rectifier with resistive load is shown in Fig. 2.1. The circuit consists of one diode that is normally connected to a transformer secondary as shown. During the positive half-cycle of the transformer secondary voltage, diode D conducts. During the negative half-cycle, diode D does not conduct. Providing perfect sinusoidal voltage on its secondary winding, the voltage and current waveforms of resistive load R and the voltage waveform of diode D are shown in Fig. 2.2.

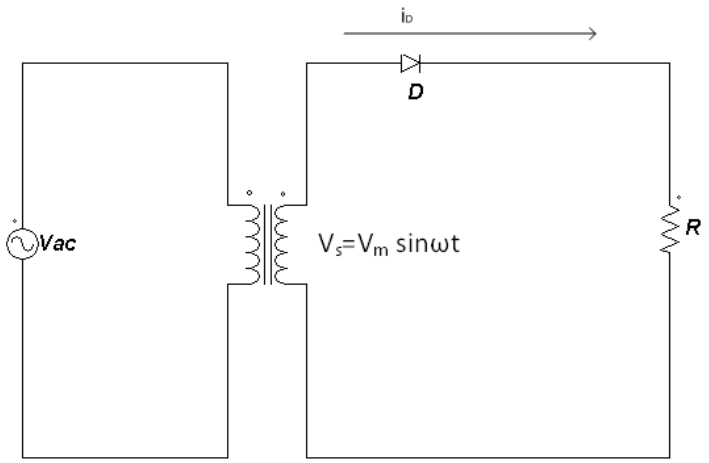


Fig. 2.1 A single-phase half-wave rectifier with resistive load.

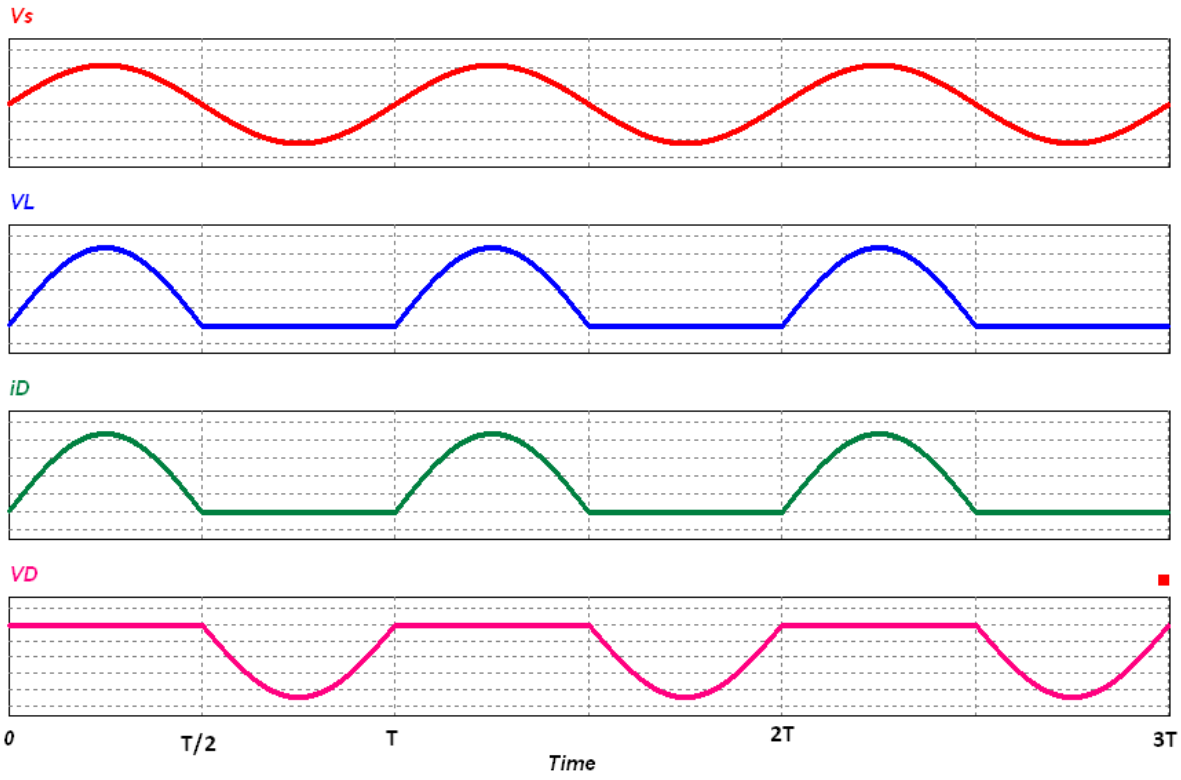


Fig. 2.2 Voltage and current waveforms of the half-wave rectifier with resistive load.

2.3 Single-Phase Full-Wave Rectifiers

There are two types of single-phase full-wave rectifier,

1. Full-wave rectifiers with center-tapped transformer

2. Bridge rectifiers.

2.3.1. Full-Wave Rectifiers with Center-Tapped Transformer

A full-wave rectifier with a center-tapped transformer is shown in Fig. 2.3. In this full wave rectifier each diode is associated with the half of the transformer and acts as a half-wave rectifier. The outputs of the two half-wave rectifiers are combined to produce full-wave rectification in the load.

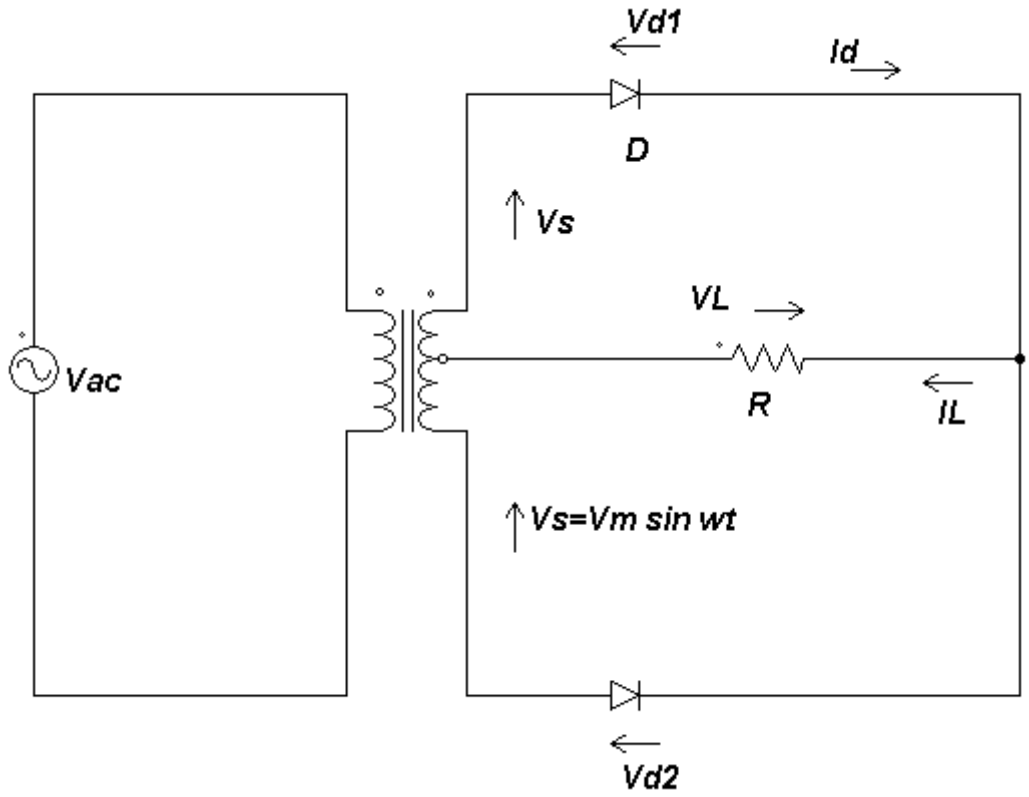


Fig. 2.3 Full-wave rectifier with center-tapped transformer.

As the transformer is concerned, the DC currents of the two half-wave rectifiers are equal and opposite, such that there is no DC current for creating a transformer core saturation problem. The voltage and current waveforms of the full-wave rectifier are shown in Fig. 2.4.

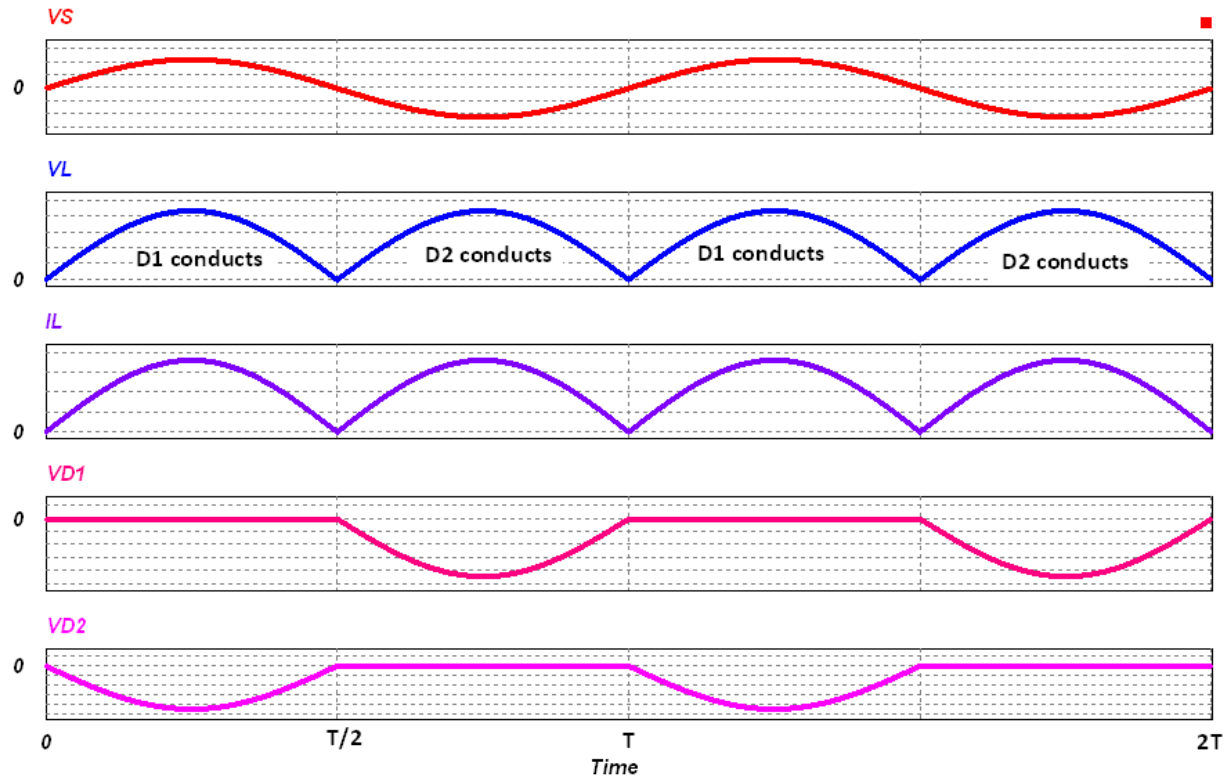


Fig. 2.4 Voltage and current waveforms of the full-wave rectifier with center-tapped transformer.

2.3.2 Bridge Rectifiers

Using four diodes instead of two, a bridge rectifier as shown in Fig. 2.5 can provide full-wave rectification without using a center-tapped transformer. During the positive half-cycle of the transformer secondary voltage, the current flows to the load through diodes D1 and D2. During the negative half cycle, D3 and D4 conduct. The voltage and current waveforms of the rectifier is shown in Fig. 2.6.

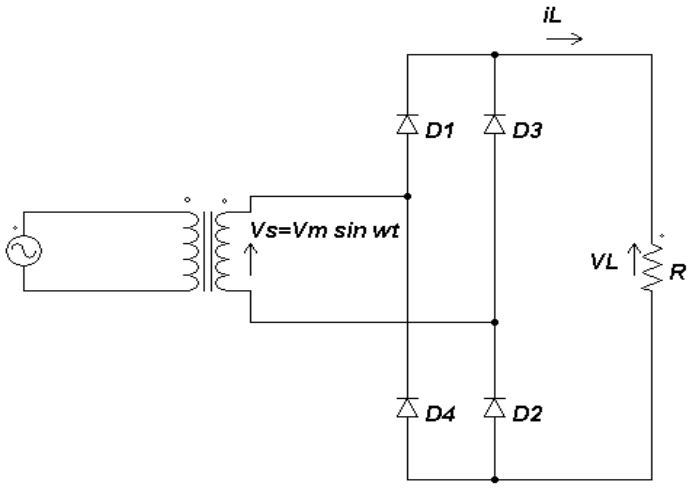


Fig. 2.5 Bridge rectifier.

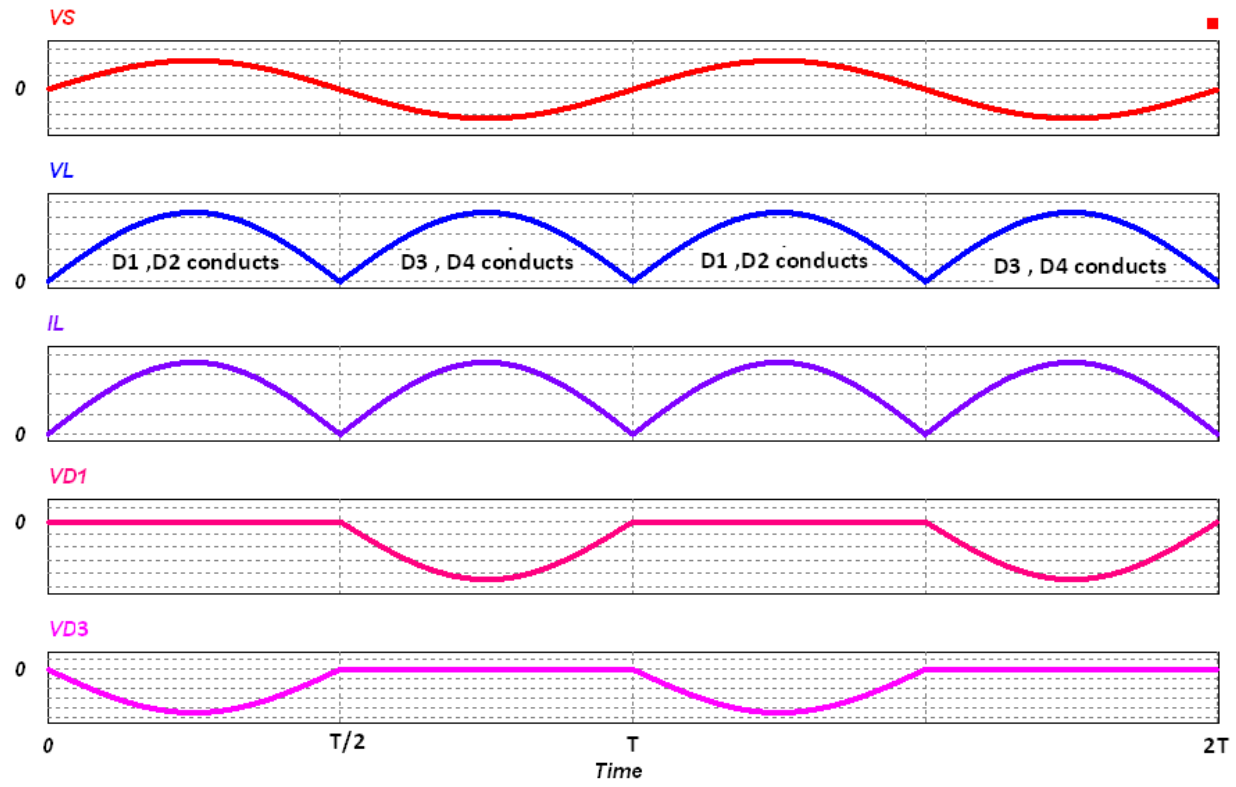


Fig. 2.6 Voltage and current waveforms of the bridge rectifier.

2.3.3 Performance Parameters

In this section the performance of the rectifiers mentioned in the preceding will be evaluated in terms of the following parameters.

The average value of the load voltage v_L is V_{dc} and it is defined as

$$V_{dc} = \frac{1}{T}\int_0^T VL(t)dt \quad \text{.....(2.1)}$$

Therefore, for half wave rectifier

$$V_{dc} = 0.318\ V_m \quad \text{.....(2.2)}$$

In the case of a full-wave rectifier, v_L (t)=Vm sin ωt for both the positive and negative half-cycles. Hence,

$$V_{dc} = \frac{1}{\pi}\int_0^\pi Vm \sin \omega t\ d(\omega t) \quad \text{.....(2.3)}$$

Therefore, for half wave rectifier

$$V_{dc} = 0.636\ V_m \quad \text{.....(2.4)}$$

The root-mean-square (rms) value of load voltage v is V_{rms}, which is defined as

$$V_{rms} = \sqrt{\frac{1}{T} * \int_0^T V^2(t)\ dt} \quad \text{.....(2.5)}$$

or,

Therefore, for half wave rectifier

$$V_{rms} = 0.5\ V_m \quad \text{.....(2.6)}$$

In the case of a full-wave rectifier, v (t) =V_m sin ωt for both the positive and negative half-cycles. Hence, for half wave rectifier

$$V_{rms} = \sqrt{\frac{1}{\pi} * \int_0^{\pi} (Vm \sin \omega t)^2\ (t)\ d(\omega t)} \quad \text{.....(2.7)}$$

$$= 0.707\ V_m$$

The result is as expected because the rms value of a full-wave rectified voltage should be equal to that of the original AC voltage.

The rectification ratio, which is a figure of merit for comparing the effectiveness of rectification, is defined as

$$\sigma = \frac{Pdc}{PL} \quad \text{.....(2.8)}$$

In the case of a half-wave diode rectifier, the rectification ratio σ is 40.5%, and for a full-wave rectifier, the rectification ratio σ is 81%

2.4 Three-Phase Diode Rectifiers

Single-Phase diode rectifiers are suitable only for low to medium power applications. For power output higher than 15 kW, three-phase or poly-phase diode rectifiers are used. There are two types of three-phase diode rectifier that convert a three-phase AC supply into a DC voltage, star rectifiers and bridge rectifiers. In the following subsection, the operations of these rectifiers are investigated and their performances are analyzed. For the sake of simplicity, the diodes and transformers are considered to be ideal, that is, the diodes have zero forward voltage drop and reverse current, and the transformers do not have either resistance or leakage inductance. Furthermore, it is assumed that the load is purely resistive, such that the load voltage and the load current have similar waveforms.

2.4.1 Three-Phase Star Rectifiers

A half bridge three-phase star rectifier circuit is shown in Fig. 2.7. This circuit can be considered as three single-phase half-wave rectifiers combined together. For this reason, it is sometimes referred to as a three-phase half-wave rectifier. The diode in a particular phase conducts during the period when the voltage on that phase is higher than that on the other two phases. The voltage waveforms of each phase and the load are shown in Fig. 2.8. This circuit is used where the required DC output voltage is relatively low and the required output current is too large for a practical single-phase system.

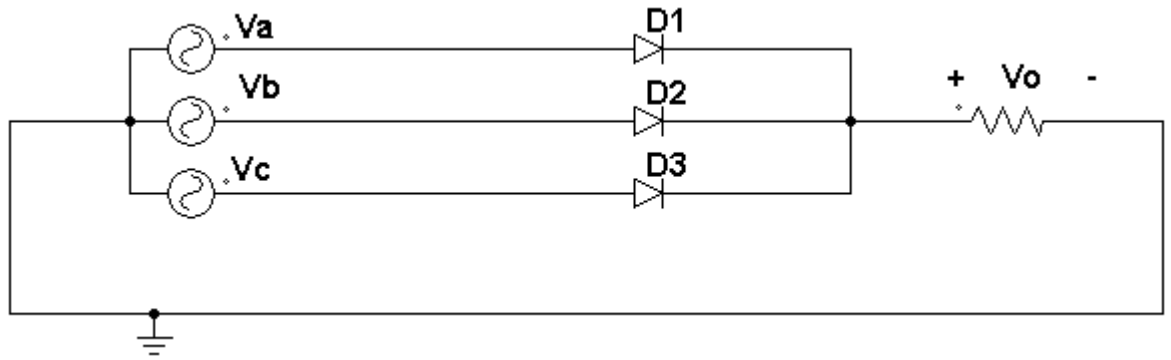


Fig. 2.7 Three-phase star rectifier.

The average value of the output is

$$V_{dc} = \frac{3}{2\pi}\int_{\pi/6}^{5\pi/6} Vm \sin\theta \, d\theta \qquad \text{.....(2.9)}$$

or,

$$V_{dc} = \frac{3\sqrt{3}}{2\pi} V_m$$

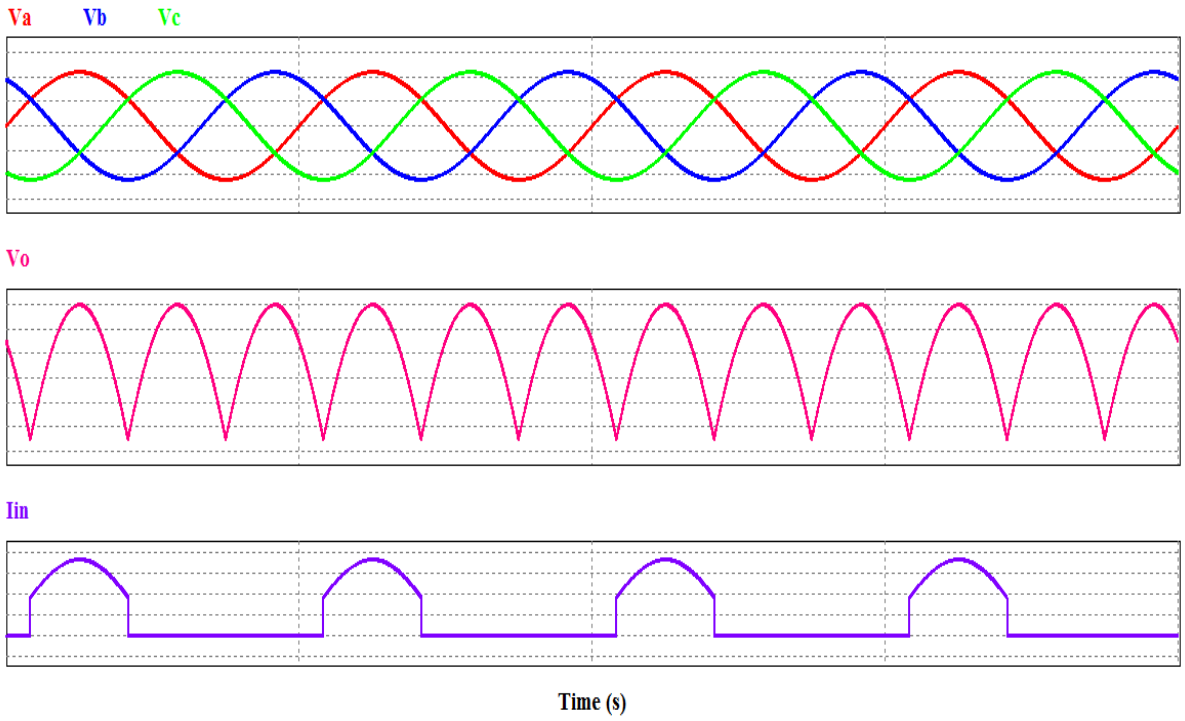


Fig. 2.8 Waveforms of voltage and current of the three-phase star rectifier

2.4.2 Three-Phase Bridge Rectifirs

The commonly used rectifiers for high-power applications are three-phase bridge rectifiers because of their highest possible transformer utilization factor for a three-phase system. The circuit of a three-phase bridge rectifier is shown in Fig. 2.9. The diodes are numbered in the order of conduction sequences and the conduction angle of each diode is $2\pi = 3$.The conduction sequence for diodes is 12, 23, 34, 45, 56 and 61. The voltage and current waveforms of the three-phase bridge rectifier are shown in Fig. 2.10. The line voltage is $\sqrt{3}$ times the phase voltage of a three-phase star-connected source. There is no problem to use any combination of star- or delta- connected primary and secondary windings because the currents associated with the secondary windings are symmetrical.

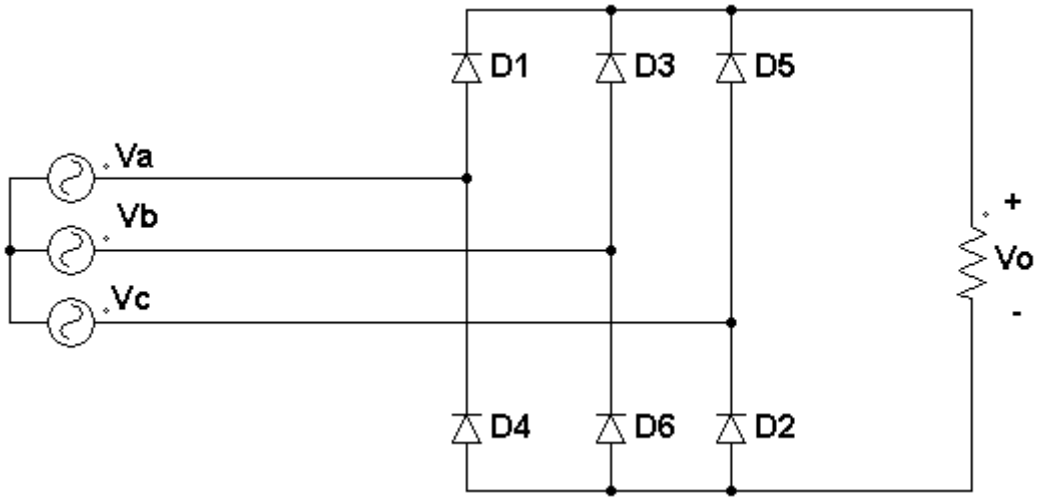


Fig. 2.9 Three-phase bridge rectifier.

The average value of the output can be found as,

$$V_{dc} = \frac{6}{2\pi} \int_{\pi/3}^{2\pi/3} \sqrt{3}\, Vm \sin \theta \, d\theta \qquad \text{.....(2.10)}$$

or,

$$V_{dc} = \frac{3\sqrt{3}}{\pi} V_m$$

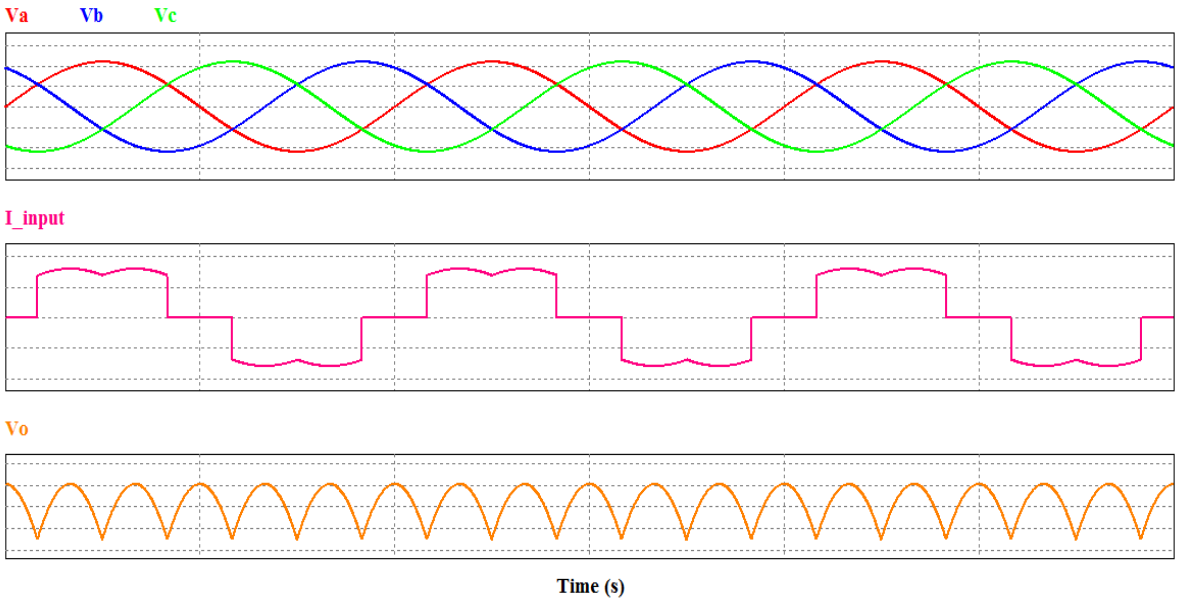


Fig. 2.10 Voltage and current waveforms of the three-phase bridge rectifier.

CHAPTER 3
DC-DC CONVERTERS

3.1 Introduction

The conversion of variable DC voltage from a fixed DC voltage source is required frequently in many industrial applications. A converter that converts DC directly from DC is known DC-DC converter. DC converters are widely used in motor controlling, trolley cars, marine hoists, forklift trucks and mine haulers. Moreover DC converters can be used as a DC voltage regulators as well as the conjunction with an inductor, which can be used as a current source.

Linear power regulators operate based on the principle of voltage divider or current divider, which are inefficient. This is because their output voltages are always smaller than the input voltage. Linear regulators can, however, provide a very high-quality output voltage. These regulators can be used in low power levels. But at low and medium power levels switching regulators are used. Power electronic semiconductor switches (like BJT, MOSFET, IGBT etc.) are used in switching regulators because of their small power loss in both states (low voltage across a switch in the on state, zero current through a switch in the off state). Moreover, switching regulators are efficient for power conversion. Modern power electronic switches can operate at high frequencies. By applying higher switching frequency, we can reduce the size of inductors and capacitors. In addition, the dynamic characteristics of converters improve with increasing operating frequencies.

High operating frequencies allow achieving faster dynamic responses to rapid changes in the load current and the input voltage. The functions of DC-DC converters are:

I. to convert a DC input voltage V_S into a DC output voltage V_O;
II. to regulate the DC output voltage against load and line variations;
III. to reduce the AC voltage ripple on the DC output voltage below the required level;
IV. to protect the supplied system and the input source from electromagnetic interference (EMI);
V. to satisfy various international and national safety standards;
VI. to provide isolation between the input source and the load (isolation is not always required).

The DC-DC converters can be divided into two main types:

I. hard-switching pulse width modulated (PWM) converters

II. resonant and soft-switching converters.

This chapter deals with PWM DC-DC converters, which are widely used at all power levels. Advantages of PWM converters include low component consumption, high conversion efficiency, constant frequency operation, relatively simple control scheme and commercial availability of integrated circuit controllers and ability to achieve high conversion ratios for both step-down and step-up application. A disadvantage of PWM DC-DC converters is that PWM rectangular voltage and current waveforms cause turn-on and turn-off losses in semiconductor devices, which limit practical operating frequencies to hundreds of kilohertz. Rectangular waveforms also inherently generate EMI.

This chapter begins with a discussion on DC choppers that are used primarily in DC motor drives. The output voltage of DC choppers is controlled by adjusting the on time of a switch, which in turn adjusts the width of an output voltage pulse. That's why it is called pulse width modulation (PWM) control. The DC choppers with additional filtering components form PWM DC-DC converters.

3.2 Linear Regulator

A basic linear regulator with a resistive load is shown in Fig. 3.1. It consists of a series connection of a DC input voltage source V_S, a variable resistance, and load resistance R. To keep the output voltage fixed with the variation of input voltage or load, this regulator adjusts the variable resistance.

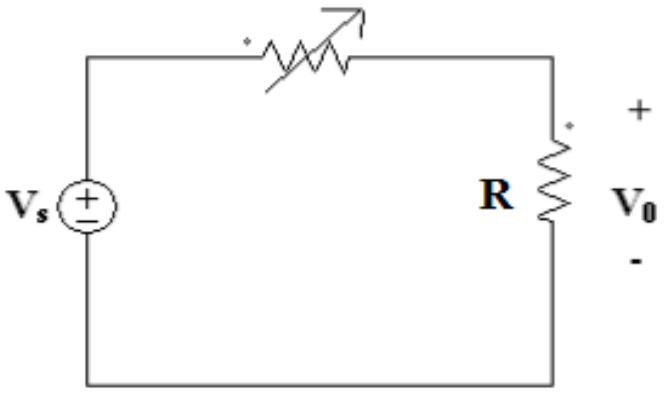


Fig. 3.1 Linear regulator circuit.

3.3 DC Choppers

A step-down DC chopper with a resistive load is shown in Fig. 3.2. It consists of a series connection of a DC input voltage source V_S, controllable switch S, and load resistance R. In most cases, switch S is unidirectional. Power electronic switches are usually implemented with power MOSFETs, IGBTs, MCTs, power BJTs, or GTOs. Fig. 3.3 shows waveforms of a step-down chopper. The switch is operated with a duty ratio, D defined as a ratio of the on time to the sum of the on and off times of the switch.

$$D = \frac{Ton}{Ton+Toff} = \frac{Ton}{T} \quad \text{.....(3.1)}$$

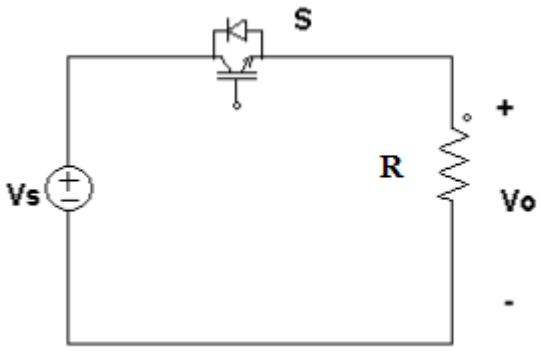


Fig. 3.2 DC chopper circuit.

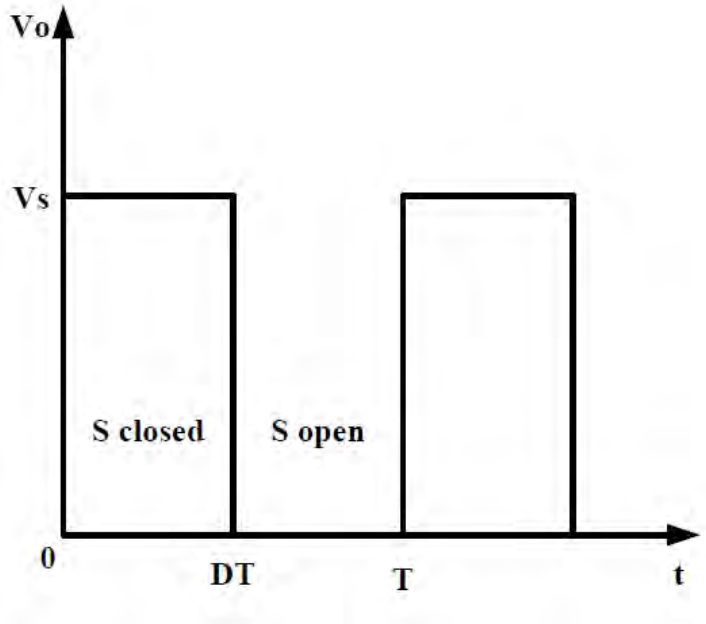


Fig. 3.3 Output voltage waveform of a DC chopper with resistive load.

The average value of the output voltage is

$$Vo = DVs \quad \text{.....(3.2)}$$

Vo can be regulated by adjusting the duty ratio D. The average output voltage is always smaller than the input voltage.

3.4 Buck (Step-Down) Converter

The step-down DC-DC converter, commonly known as a buck converter, is shown in Fig. 3.4. It consists of DC input voltage source V_S, controlled switch S, diode D, filter inductor L, filter capacitor C, and load resistance R. The operation of this converter is shown in Fig. 3.5.Typical waveforms of the converter are shown in Fig. 3.6. The state of the converter in which the inductor current never reaches to zero for any period of time is called the continuous conduction mode (CCM). It can be seen from the circuit that when the switch S is in on state, the diode D is reverse-biased. When the switch S is off, the diode conducts to support an uninterrupted current in the inductor.

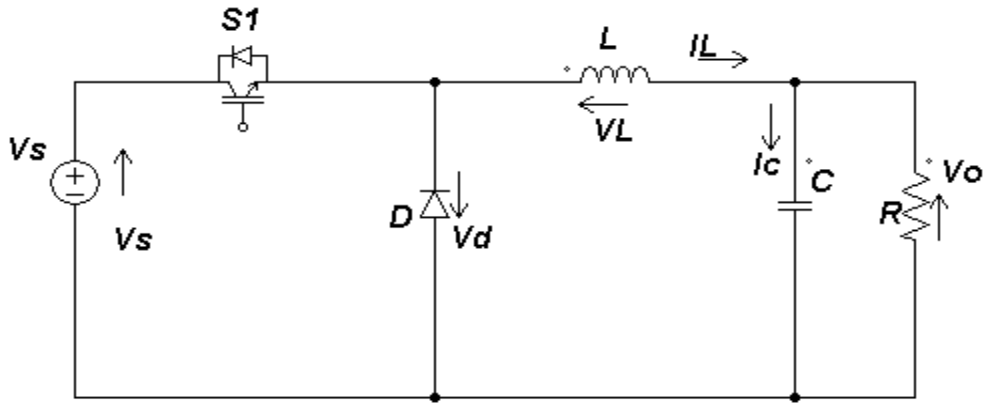
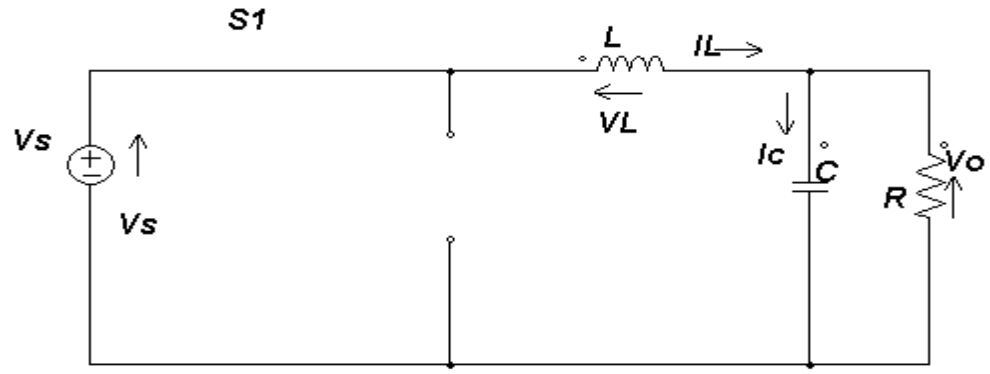
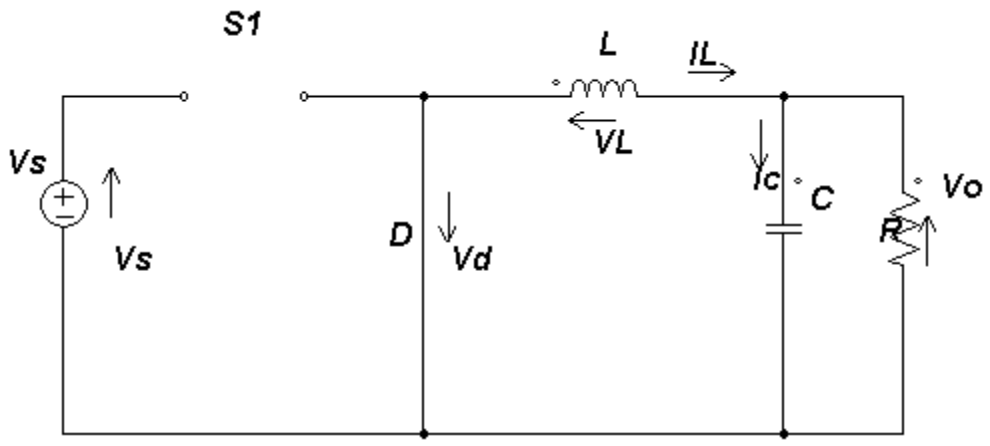


Fig. 3.4 Buck DC-DC converter.



(a)



(b)

Fig. 3.5 Equivalent circuit of Buck DC-DC converter when (a) switch closed (b) switch open

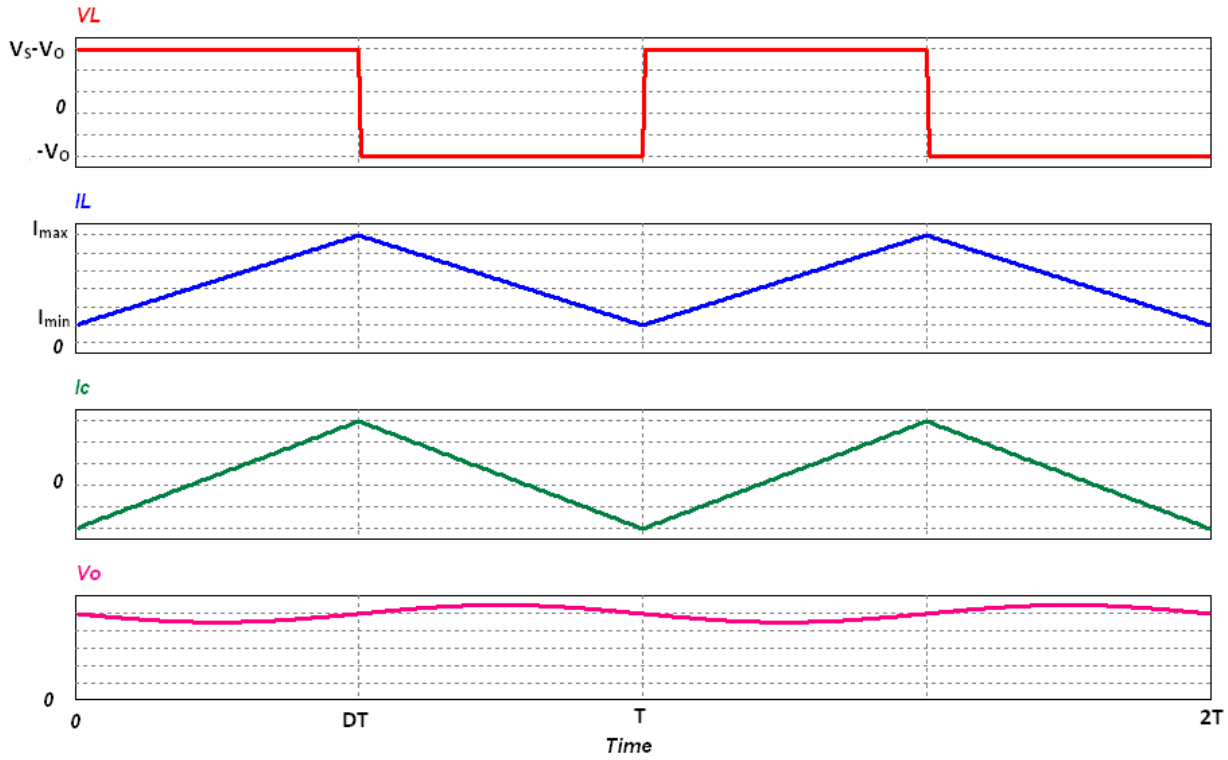


Fig. 3.6 Waveforms of Buck converter

The relationship among the input voltage, output voltage, and the switch duty ratio D can be derived, for instance, from the inductor voltage V_L waveform. For the buck converter,

$$(Vs - Vo)\, DT = - Vo(1 - D)T$$

Hence, the DC voltage transfer function, defined as the ratio of the output voltage to the input voltage, is

$$D = \frac{Vo}{Vs} \quad \text{.....(3.3)}$$

It can be seen from Eq. 3.4 that the output voltage is always smaller than the input voltage. The DC-DC converters can operate in two modes with respect to the inductor current I_L. Figure 3.6 shows the CCM in which the inductor current is always greater than zero. When the average value of the output current is low (high R) or the switching frequency f is low, the converter may enter the discontinuous conduction mode (DCM).

For the buck converter, the value of the filter inductance that determines the boundary between CCM and DCM is given by

$$L_b = \frac{(1-D)R}{2f} \quad \text{.....(3.4)}$$

To limit the peak-to-peak value of the ripple voltage below a certain value Vr , the filter capacitance C must be greater than

$$C_{min} = \frac{(1-D)Vo}{8Vr\ L\ f^2} \quad \text{.....(3.5)}$$

Equations (3.4) and (3.5) are the key design equations for the buck converter. The input and output DC voltages (hence, the duty ratio D), and the range of load resistances R are usually considered as initial specifications. The designer needs to determine values of passive components L and C, and of the switching frequency f.

3.5 Boost (Step-Up) Converter

Fig. 3.7 shows a step-up or a PWM boost converter. It consists of DC input voltage source V_S, boost inductor L, controlled switch S, diode D, filter capacitor C, and load resistance R. The converter operation is shown in Fig. 3.8.The waveforms in the CCM are presented in Fig. 3.9. When the switch S is in the on state, the current in the boost inductor increases linearly and the diode D is off at that time. When the switch S is turned off, the energy stored in the inductor is released through the diode to the output RC circuit.

For the boost inductor,

$$Vs\ DT = (Vo-Vs)\ (1 - D)\ T$$

From which the DC voltage transfer function turns out to be

$$\frac{V0}{Vs} = \frac{1}{1-D} \quad \text{.....(3.6)}$$

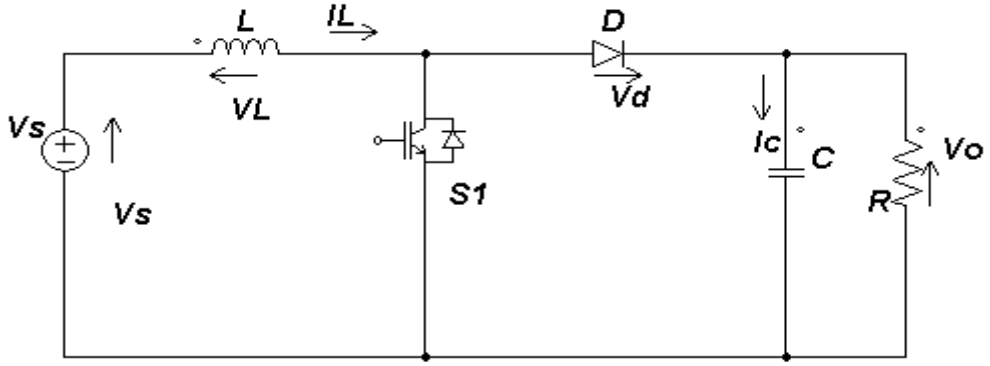
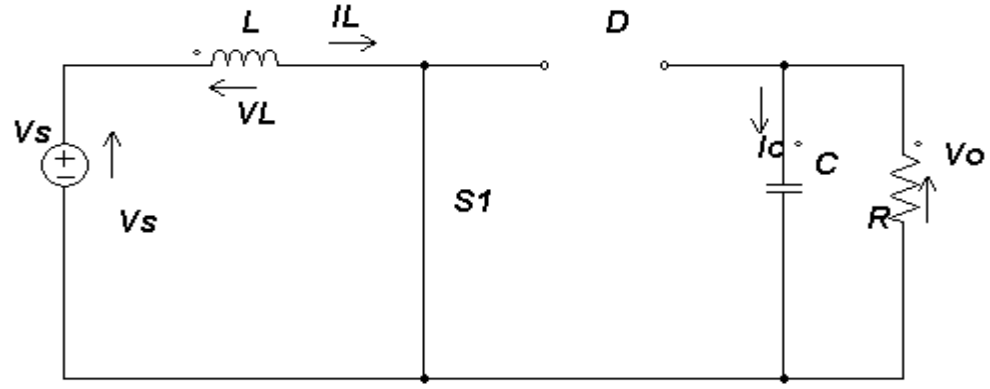
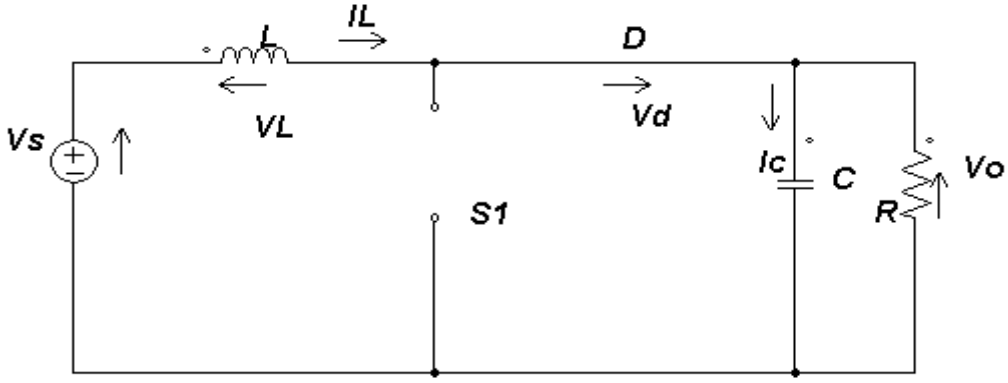


Fig. 3.7 Boost DC-DC converter.



(a)



(b)

Fig. 3.8 Equivalent circuit of Boost DC-DC converter when (a) switch closed (b) switch open

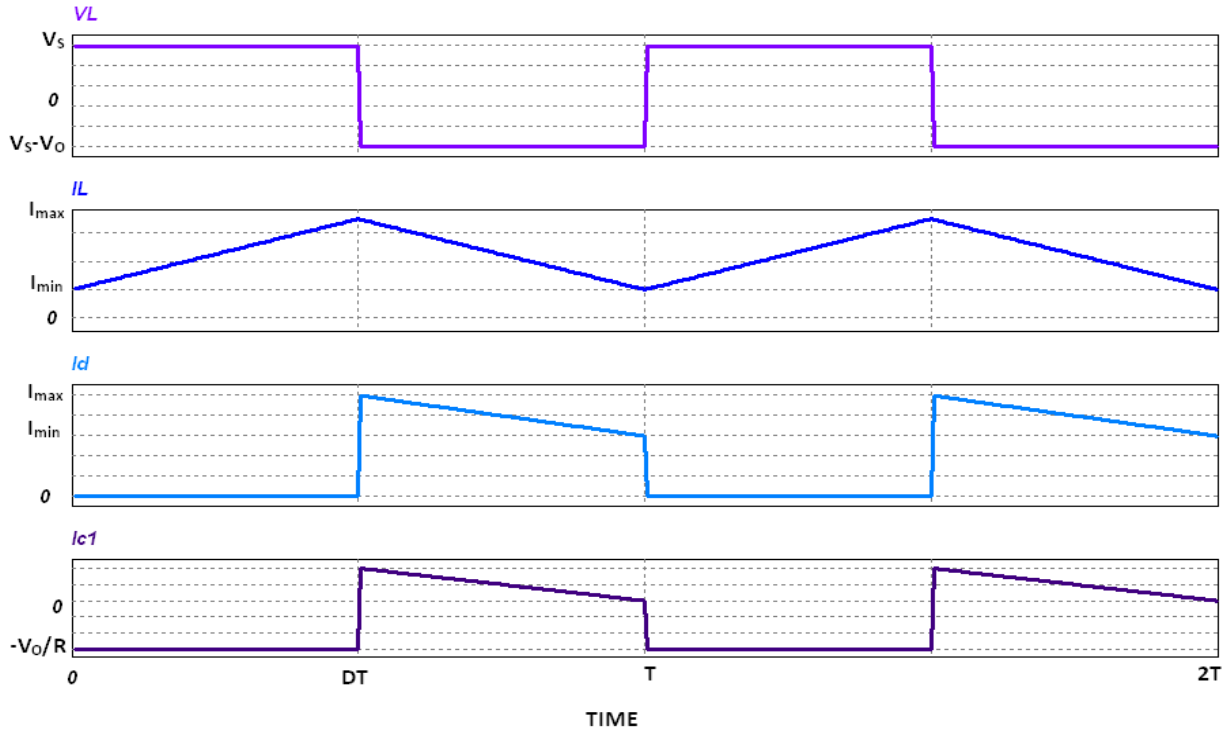


Fig. 3.9 Waveforms of Boost converter

As the name of the converter suggests, the output voltage is always greater than the input voltage.

The boost converter operates in the CCM for $L > L_b$ where

$$L_b = \frac{(1-D)^2\ DR}{2f} \quad \text{.....(3.7)}$$

The filter capacitor must provide the output DC current to the load when the diode is off. The minimum value of the filter capacitance that results in the voltage ripple Vr is given by

$$C_{min} = \frac{D\ Vo}{Vr\ Rf} \quad \text{.....(3.8)}$$

3.6 Buck-Boost Converter

A buck-boost converter is shown in Fig.. 3.10. The converter consists of DC input voltage source V_S, controlled switch S, inductor L, diode D, filter capacitor C, and load resistance R. With the switch on, the inductor current increases while the diode is maintained off. When the switch is turned off, the diode provides a path for the inductor current. Note the polarity of the diode that results in its current being drawn from the output. The buck-boost converter operation is depicted in Fig. 3.11. Fig. 3.12 shows the waveforms for CCM of buck-boost converter.

The condition of a zero volt-second product for the inductor in steady state yields

$$Vs\ DT = -\ Vo\ (1 - D)\ T$$

Hence, the DC voltage transfer function of the buck-boost converter is

$$\frac{V0}{Vs} = -\frac{D}{1-D} \quad \text{.....(3.9)}$$

The output voltage V_O is negative with respect to the ground. Its magnitude can be either greater or smaller (equal at D= 0.5) than the input voltage as the name of the converter implies.

The value of the inductor that determines the boundary between the CCM and DCM is

$$L_b = \frac{(1-D)^2 R}{2f} \quad \text{.....(3.10)}$$

The minimum value of the filter capacitance that results in the voltage ripple Vr is given by

$$C_{min} = \frac{D\ Vo}{Vr\ Rf} \quad \text{.....(3.11)}$$

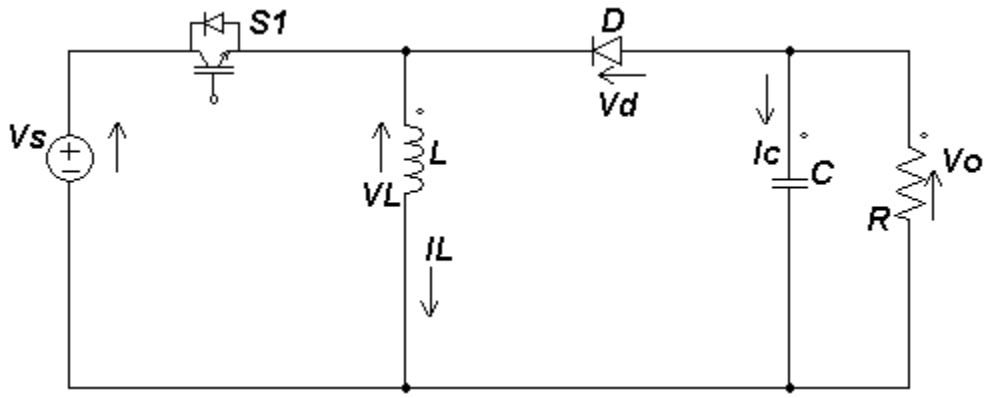
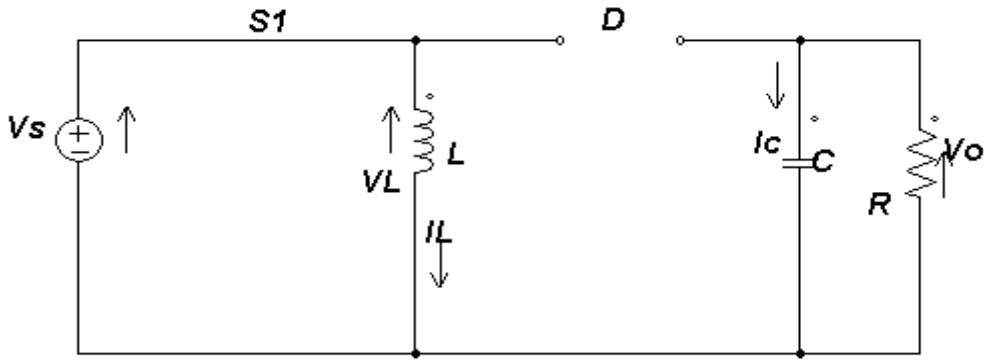
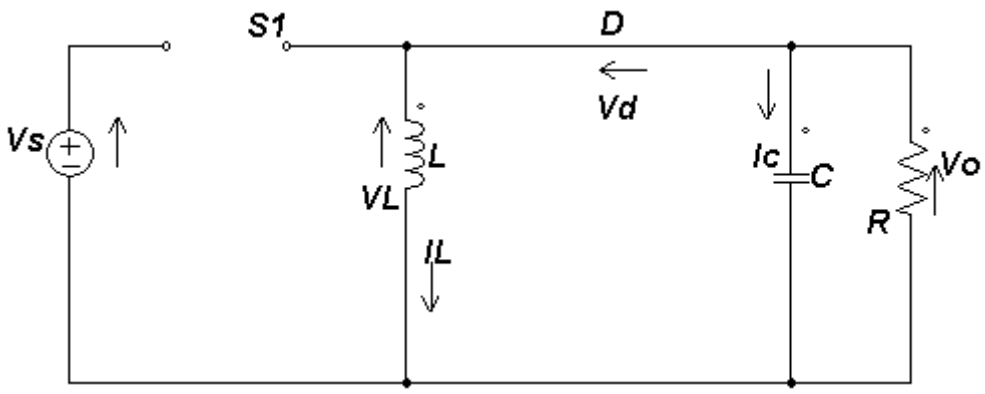


Fig. 3.10 Buck-Boost DC-DC converter.



(a)



(b)

Fig. 3.11 Equivalent circuit of Buck-Boost DC-DC converter when (a) switch closed (b) switch open

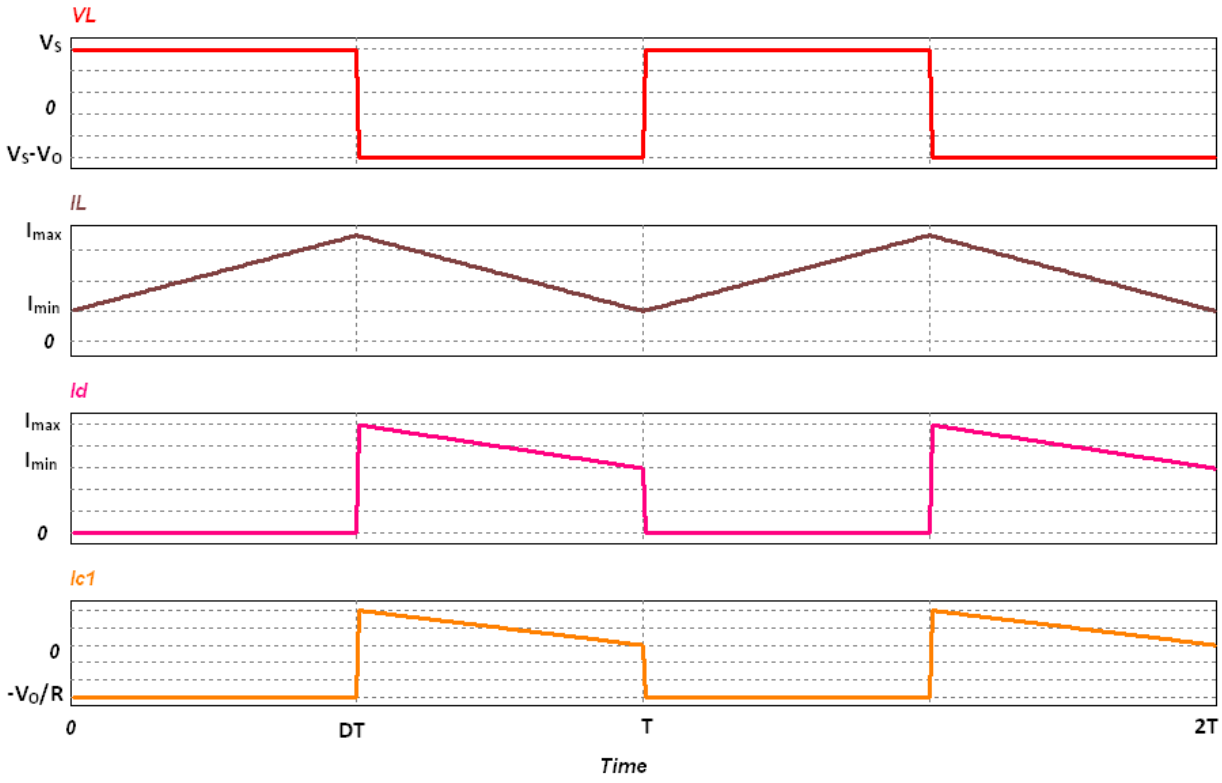


Fig. 3.12 Waveforms of Buck-Boost converter.

3.7 Ĉuk Converter

The circuit of the Ĉuk converter is shown in Fig. 3.13. It consists of DC input voltage source V_S, input inductor L_1, controllable switch S, energy transfer capacitor C_1, diode D, filter inductor L_2, filter capacitor C_2, and load resistance R. An important advantage of this topology is a continuous current at both the input and the output of the converter. Disadvantages of the Ĉuk converter are a high number of reactive components and high

current stresses on the switch, the diode, and the capacitor C_1. The operation of the converter is presented in Fig. 3.14. When the switch is on, the diode is off and the capacitor C_1 is discharged by the inductor L_2 current. With the switch in the off state, the diode conducts currents of the inductors L1 and L2, whereas capacitor C1 is charged by the inductor L1 current. The waveforms of the converter are shown in Fig. 3.15

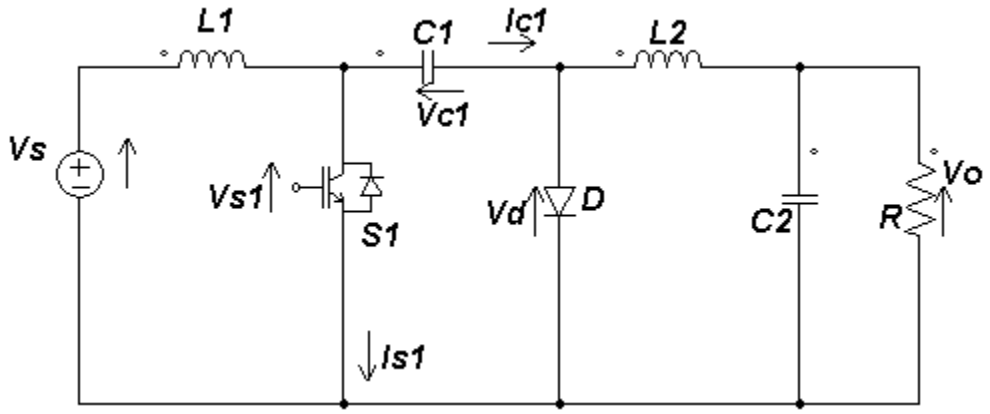
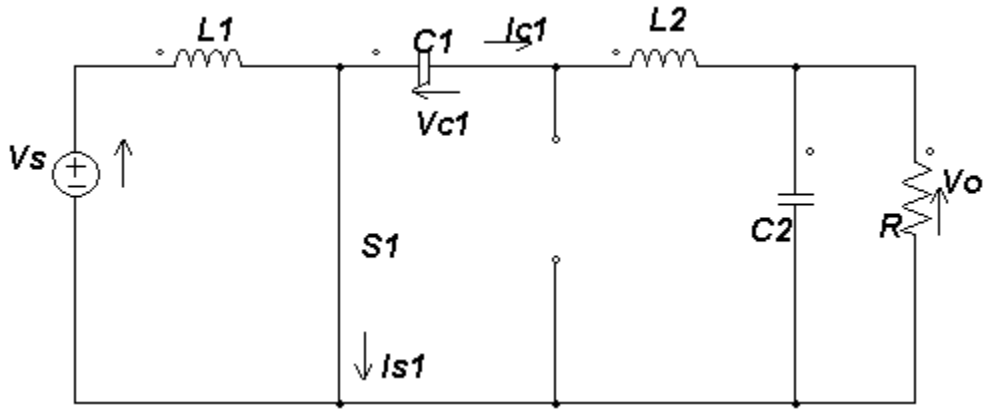
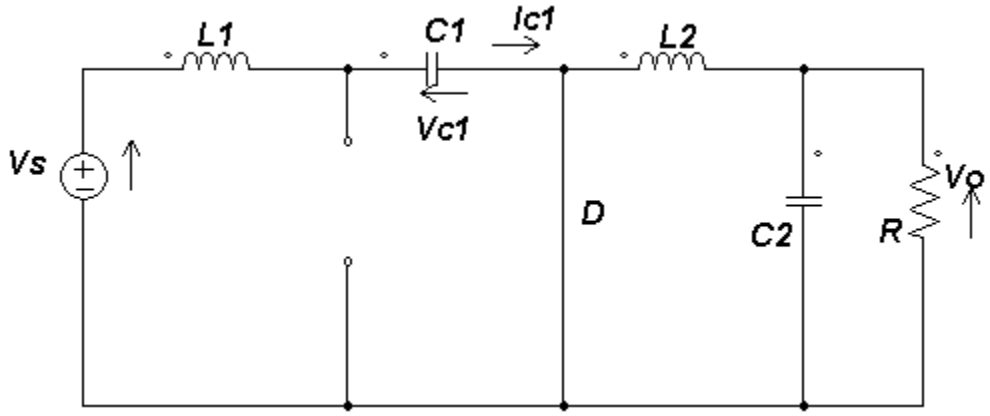


Fig. 3.13 Ĉuk DC-DC converter



(a)



(b)

Fig. 3.14 Equivalent circuit of Ĉuk DC-DC converter when (a) switch closed (b) switch open.

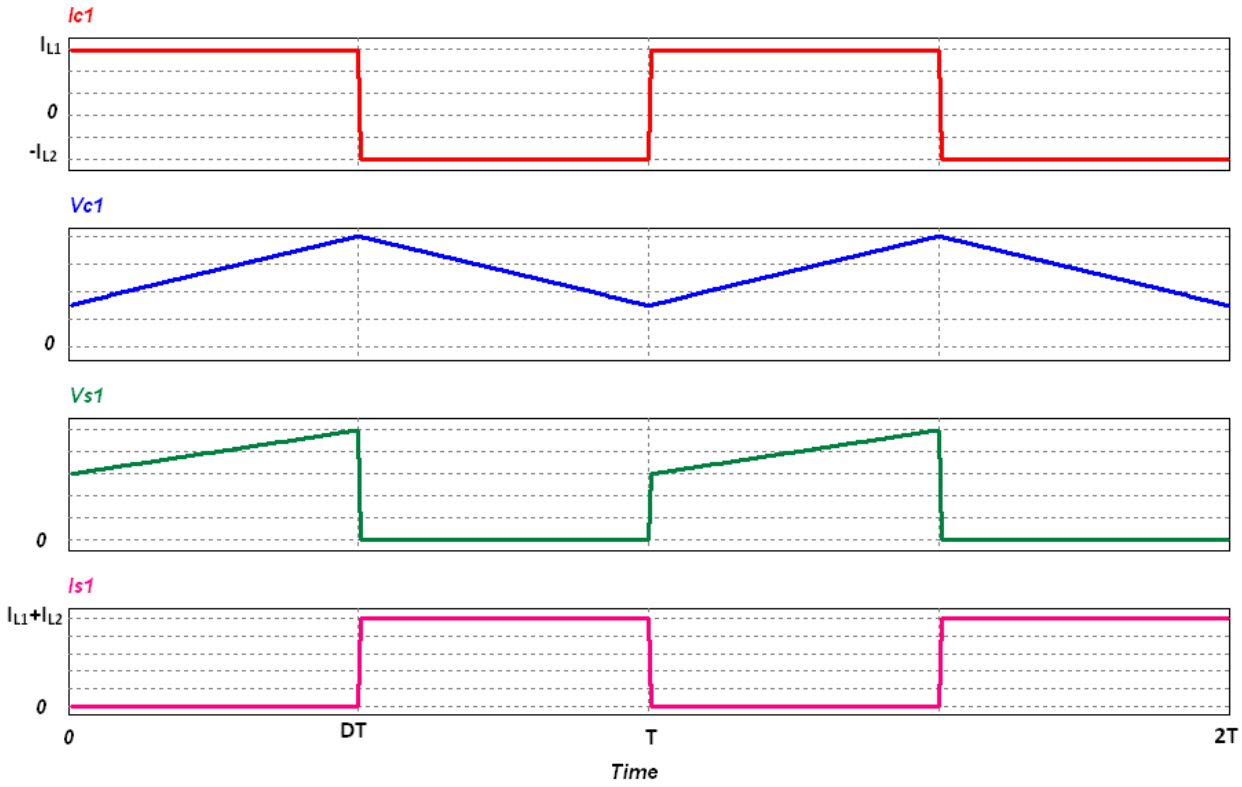


Fig. 3.15 Waveforms of Ĉuk converter

For Ĉuk converter,

$$I_{L2}\,DT = I_{L1}(1-D)T$$

For a lossless conversion

$$Ps = Vs\,I_{L1} = -\,Vo\,I_{L2} = Po$$

Combining these two equations, the DC voltage transfer function of the Ĉuk converter is

$$\frac{V0}{Vs} = -\frac{D}{1-D} \qquad \text{.....(3.12)}$$

This voltage transfer function is the same as that for the buck-boost converter.

The boundaries between the CCM and DCM are

For L_1

$$L_{b1} = \frac{(1-D)R}{2Df} \qquad \text{.....(3.13)}$$

For L_2.

$$L_{b2} = \frac{(1-D)R}{2f} \qquad \text{.....(3.14)}$$

The output part of the Ĉuk converter is similar to that of the buck converter. Hence, the expression for the filter capacitor C is

$$C_{min} = \frac{(1-D)Vo}{8Vr\ L2\ f^2} \quad \text{.....(3.15)}$$

3.8 SEPIC Converter

Single-ended primary-inductor converter (SEPIC) is a type of DC-DC converter allowing the electrical potential (voltage) at its output to be greater than, less than, or equal to that at its input. A SEPIC is similar to a traditional buck-boost converter, but has advantages of having non-inverted output.

The circuit of the SEPIC converter is shown in Fig. 3.16. It consists of DC input voltage source V_S, inductors L_1, L_2 and L_3,controllable switch S_1, capacitors C_1, C_2, C_3, diode D_1, and load resistance R. Capacitor C_3 is used for filtering .

Figure 3.17 shows the circuit operation when the switch is on and off respectively.

For SEPIC converter

$$\frac{Vo}{Vs} = \frac{D}{1-D} \quad \text{.....(3.16)}$$

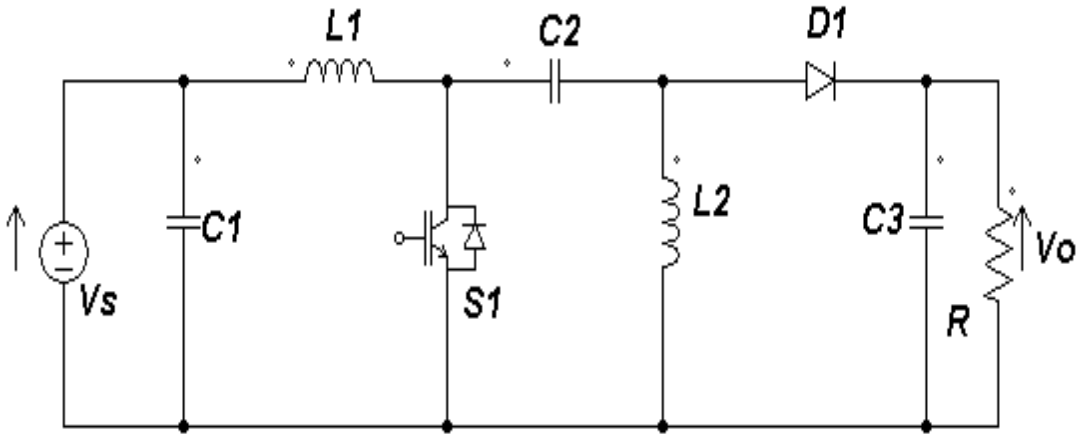
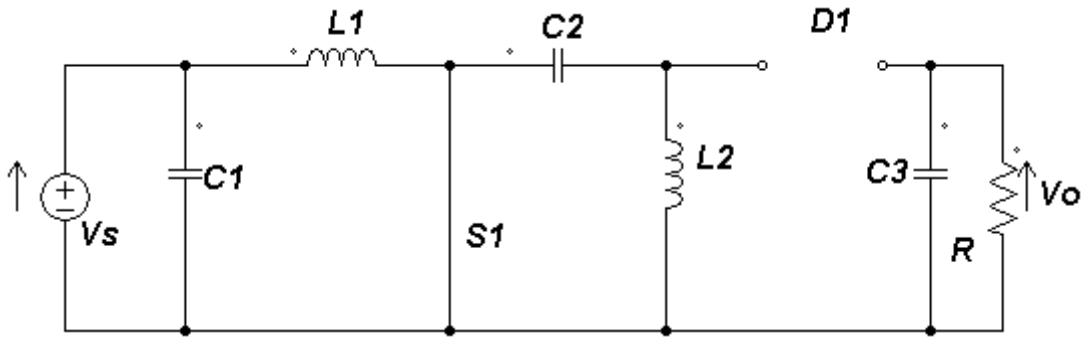
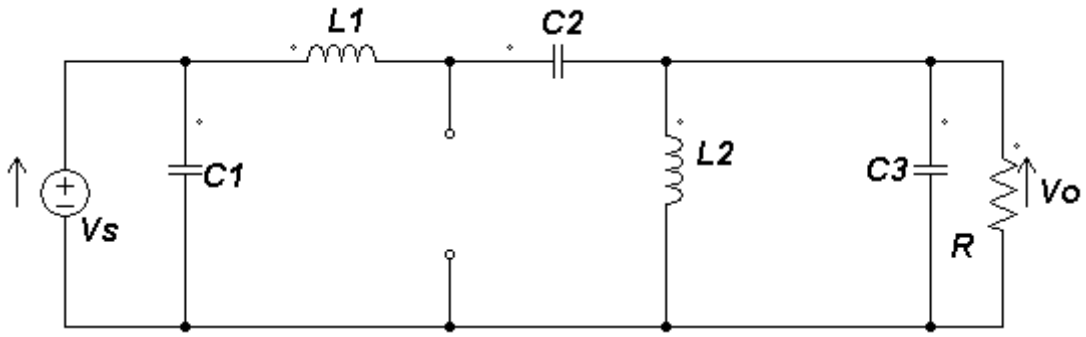


Fig. 3.16 SEPIC DC-DC converter



(a)



(b)

Fig. 3.17 Equivalent circuit of SEPIC DC-DC converter when (a) switch closed (b) switch open.

3.9 Inverse SEPIC Converter

The circuit of the inverse SEPIC converter is shown in Fig. 3.18. It consists of DC input voltage source V_S, inductors L_1, L_2, L_3,controllable switch S_1, capacitors C_1, C_2, C_3, diode D_1, and load resistance R. Capacitor C_3 is used for filtering .

Figure 3.19a and Fig. 3.19b show the circuit operation when the switch is on and off respectively.

For inverse SEPIC converter

$$\frac{V0}{Vs} = \frac{D}{1-D} \quad \text{.....(3.17)}$$

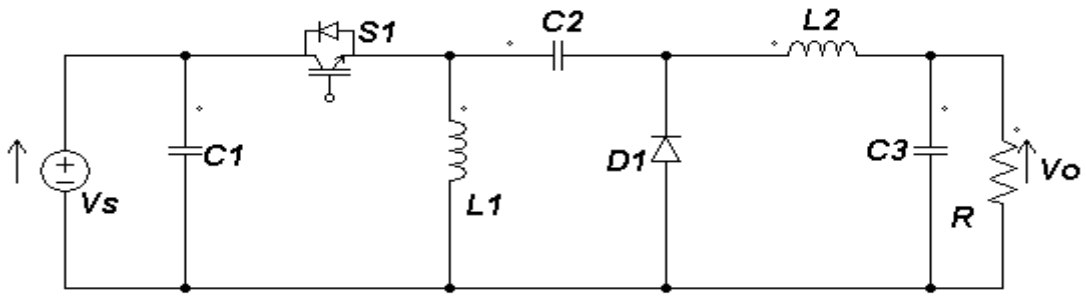
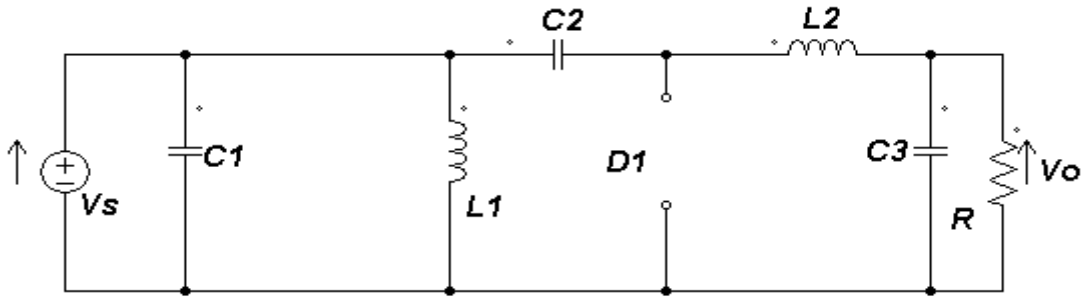
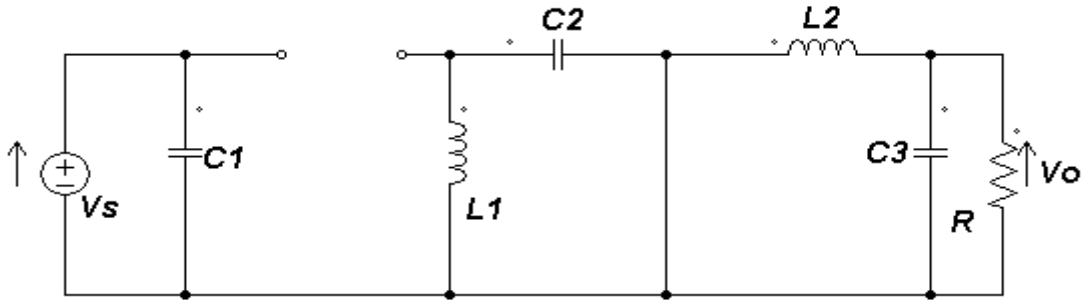


Fig. 3.18 Inverse SEPIC DC-DC converter



(a)



(b)

Fig. 3.19 Equivalent circuit of Inverse SEPIC DC-DC converter when (a) switch closed (b) switch open.

CHAPTER 4

POWER FACTOR CORRECTION

4.1 Definitions

Power factor is defined as the ratio of the average power to the apparent power drawn by a load from an AC source. If the input voltage source is sinusoidal, then power factor can be expressed as the product of the distortion power factor and displacement power factor.

The ratio of the fundamental root-mean-square (RMS) current ($I_{rms(1)}$) to the total RMS current (I_{rms}) is called distortion power factor K_d. The distortion power factor K_d is given by the following equation.

$$K_d = I_{rms(1)} / I_{rms}$$

The cosine of the displacement angle between the fundamental input current and the input voltage is called displacement power factor K_θ. The displacement power factor K_θ is given by the following equation.

$$K_\theta = \cos\theta$$

So from the definition of power factor (PF) we can write-

$$PF = K_d * K_\theta$$

$$= (I_{rms(1)} / I_{rms}) * \cos\theta$$

Less than unity power factor of a converter means that absorbs apparent power, which is higher than the active power that it consumes. Therefore, the higher VA rating is required for a power source than the load needs. The power quality of the source deteriorates for the current harmonics generated by the converter [27].

4.2 Power Factor Correction and Harmonic Reduction

There is no direct relation between power factor and THD [27]. But it is not easy to get High power factor and low harmonics at the same time. The following equations can give some relations between total harmonic distortion (THD) and power factor.

$$THD\ (\%) = 100 \times \sqrt{\left(\frac{1}{Kd}\right)^2 - 1} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.1)$$

The distortion power factor K_d can be written as-

$$K_d = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}}$$

The displacement power factor K_θ can be made unity with a capacitor or inductor but making the distortion power factor K_d unity is more difficult. When the fundamental component of the input current is in phase with the input voltage, displacement power factor, $K_\theta = 1$. So,

$$PF = K_d * K_\theta = K_d$$

$$\text{or, } PF = \frac{1}{\sqrt{1+\left(\frac{THD(\%)}{100}\right)^2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (4.2)$$

From equation (4.2) we can determine at a 10% THD corresponds to a Power Factor of approximately 0.995 and at a 20% THD corresponds to a Power Factor of approximately 0.98.

4.3 Need for Power Factor Correction

The Off-Line Rectifier

The input stage of any AC-DC converter consists of a bridge rectifier and a large filter capacitor. The bridge rectifier is followed by the large filter capacitor [27-29]. The input current of such rectifier has high input current harmonic distortion. Diode rectifiers conduct only for a short period which causes high distortion of input current. This period corresponds to the time when the input instantaneous voltage is greater than the capacitor voltage. Since the instantaneous voltage is greater than the capacitor voltage only for very short periods of time, when the capacitor is fully charged; large current pulses are drawn from the line during this short period of time. The typical power factor for this kind of rectification is about 0.6 and input current harmonic distortion is usually in the range of 55% to 65%.

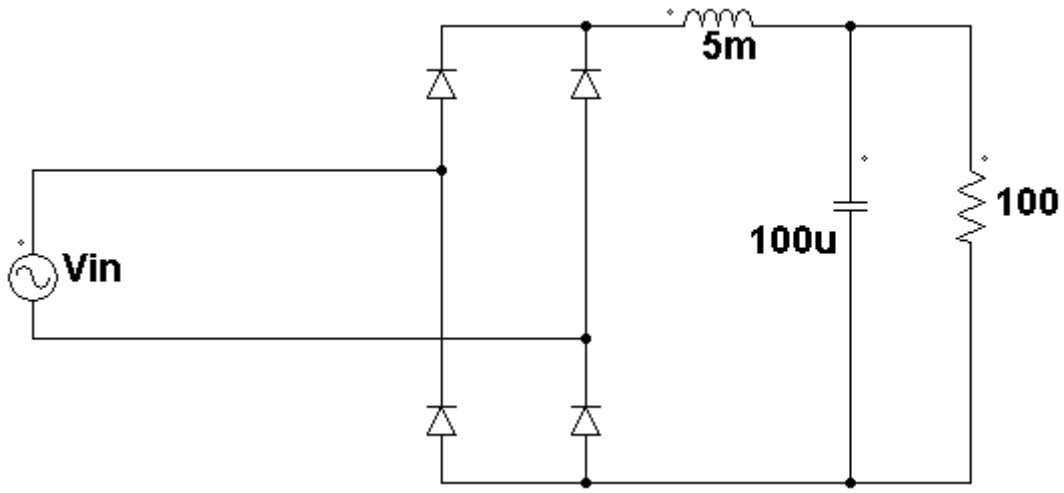


Fig. 4.1 Single phase bridge rectifier.

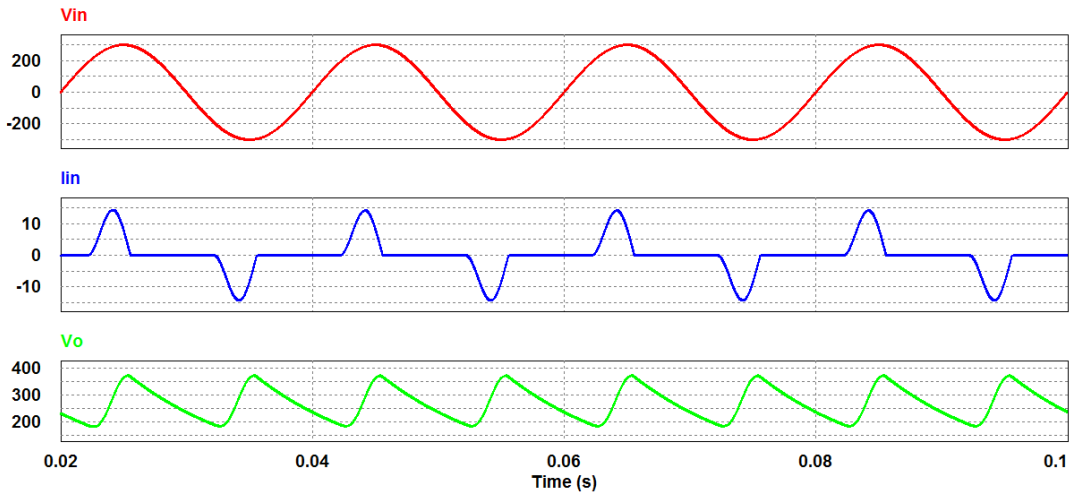


Fig. 4.2 Typical simulated line voltage and current waveforms.

Fig. 4.1 shows the diagram of a typical single-phase diode rectifier filter circuit while Fig. 4.2 shows the typical simulated line voltage and current waveforms.

It has the following main disadvantages:

1. It creates harmonics and electromagnetic interference (EMI).
2. Its power factor is poor.
3. It is inefficient as it produces high losses.
4. It requires over-dimensioning of parts.
5. It reduces maximum power capability from the line.

4.4 Types of Power Factor Correctors

PFC circuits are of two types, passive and active PFC circuits. In passive PFC, the output voltage is not regulated and changes with line variations. Only passive elements are used in addition to the diode bridge rectifier, for shaping of the line current. In active PFC, the output voltage is normally regulated for line variations. Active elements i.e. semiconductor switches are used in conjunction with inductors. Based on the switching frequency active PFC solutions can be divided into two classes, the high-frequency and the low–frequency active PFC. In high-frequency active PFC circuits, the switching frequency is much higher than the line frequency. On the other hand in low-frequency active PFC circuits, the switching is synchronized to the line voltage.

4.5 Passive Power Factor Correction Methods

Power factor depends not only on displacement factor but also on harmonic content. That's why Low harmonic content does not guarantee high power factor. High power factor can be

achieved even with substantial harmonic contents. If the amplitude of harmonics is low then the power factor is not significantly degraded by harmonics.

Harmonic contents can be controlled in the simplest way by using a filter that passes current only at line frequency (50 or 60 Hz). Harmonic contents are suppressed and the non-linear device looks like a linear load. Power factor can be improved by using capacitors and inductors i.e. passive devices. Such filters with passive devices are called passive filters.
But they require large value high current inductors which are expensive and bulky. A passive PFC circuit requires only a few components to increase efficiency, but they are large due to operating at the line power frequency.

4.5.1 Improving Harmonics with the Filter Capacitance of Rectifier Filter Circuits

Fig. 4.3 and Fig. 4.5 show the circuit of a typical single-phase diode rectifier. The simplest way to improve the shape of the line current is using a lower filter capacitance. This increases the output DC voltage ripple, power factor and reduces the harmonic content. For a 100 Ω constant power load simulated input current, output ripple waveforms for output capacitor values of 68 μF and 470 μF are shown in Fig. 4.4 and Fig. 4.6. This scheme has some limitations that it does not substantially reduce the harmonic currents and output voltage ripple is high. So it is not suitable for most applications.

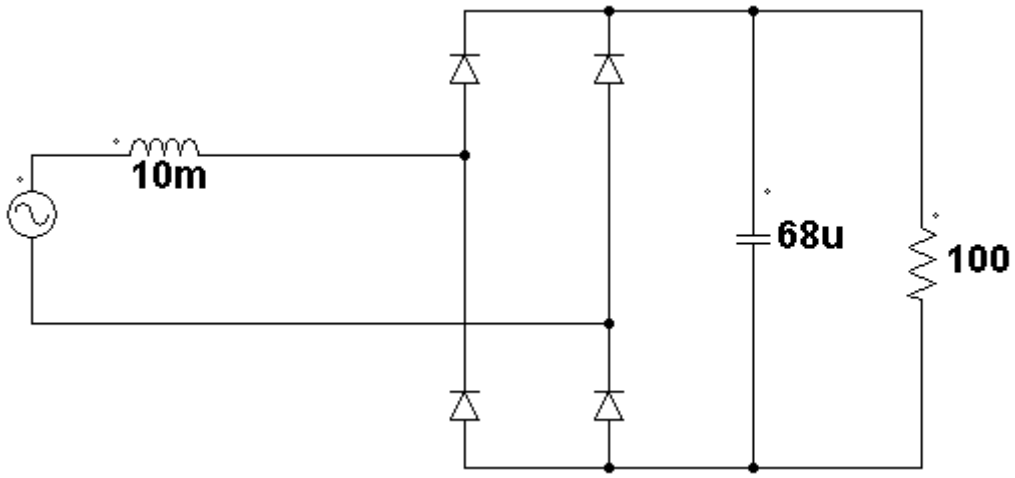


Fig. 4.3 Typical single-phase diode rectifier.

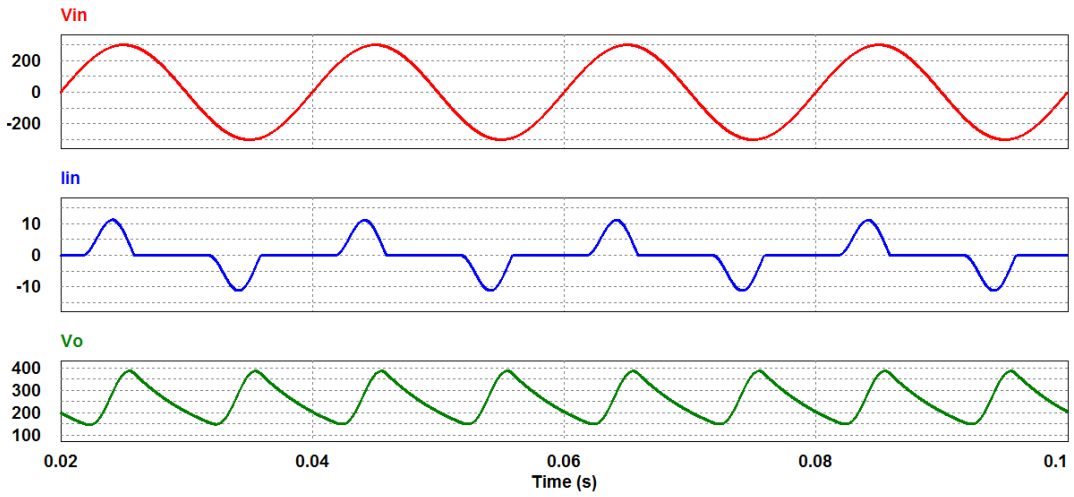


Fig. 4.4 Simulated input current, output ripple waveforms for output capacitor values of 68μF.

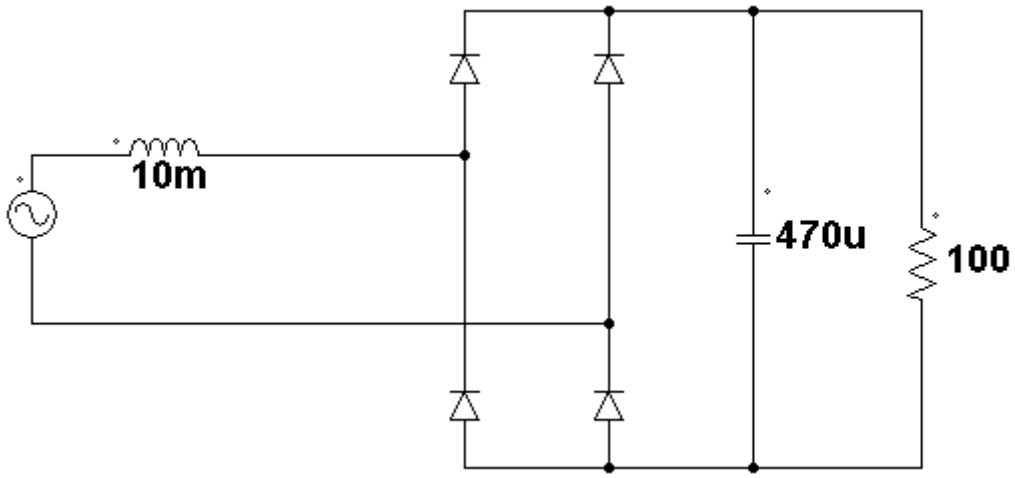


Fig. 4.5 Typical single-phase diode rectifier.

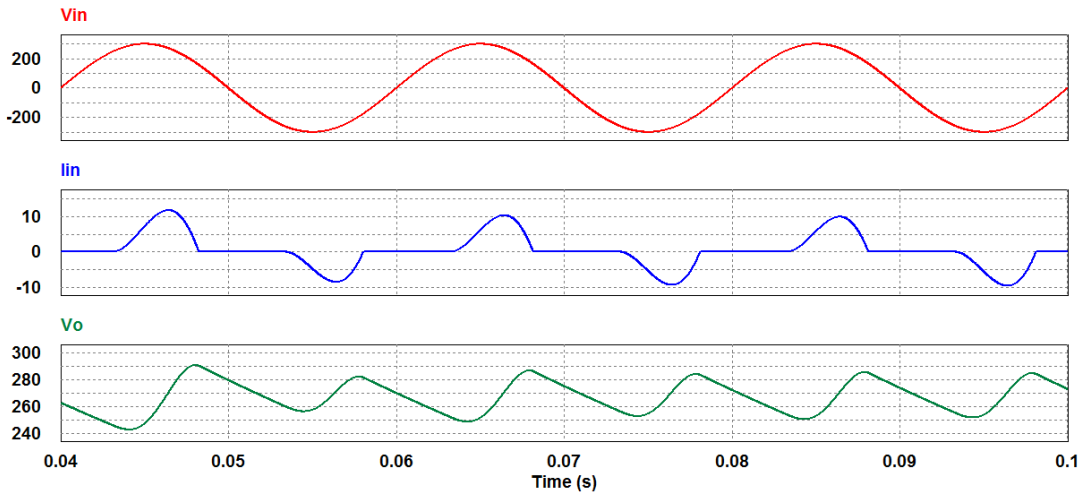


Fig. 4.6 Simulated input current, output ripple waveforms for output capacitor values of 470µF.

4.5.2 Passive PFC

As stated earlier the additional passive components in conjunction with the diode bridge rectifier is called Passive PFC circuits. So many possible schemes can be created using various combinations of these passive components in different circuit locations. Some commonly used schemes are discussed below:

4.5.2.1 Passive PFC with Inductor on the AC Side

Adding an inductor on the AC side of the diode bridge in series with the line voltage is one of the simplest methods to achieve PFC. Although this technique improves the power factor and reduce the input current harmonics, the output voltage is not regulated and increases with load. Popularly this is known as the passive PFC. PFC circuit and simulated input current waveforms for a 100 Ω load and inductor values of 5 mH and 25 mH are shown in Figures. 4.7 and 4.8 respectively

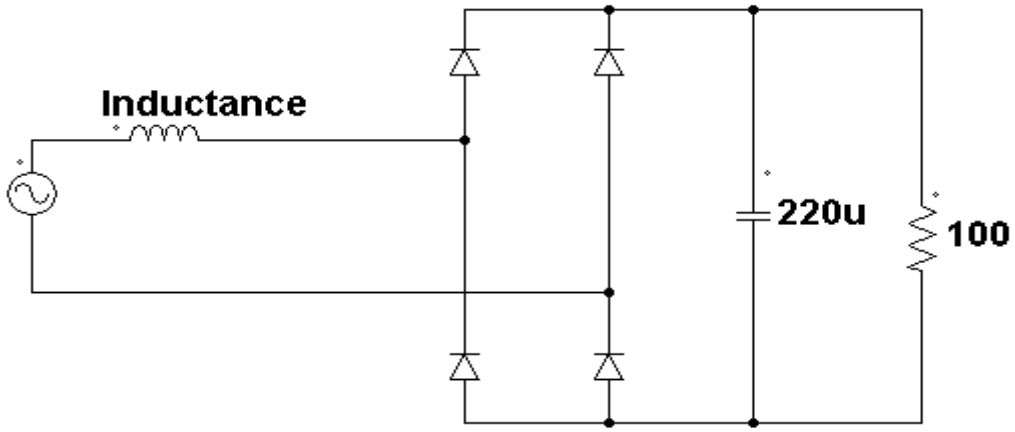


Fig. 4.7 Inductor on the AC side of the diode bridge rectifier.

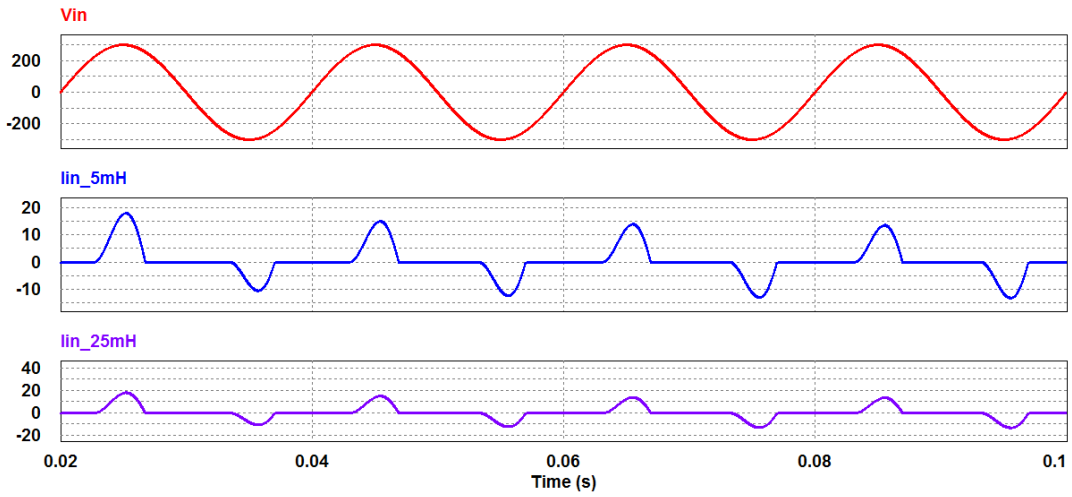


Fig. 4.8 Simulated input voltage and current waveforms

4.5.2.2 Passive PFC with Inductor on the DC Side

For this scheme an inductor is added in the DC side. If the inductor current is continuous for a given load current, the power factor can be high. This requires a relatively large inductance. When the inductor current becomes discontinuous due to reduction in load or when a lower inductance value is used, the input current wave shape becomes similar to that Passive PFC with inductor on the AC Side discussed before and the power factor also deteriorate.

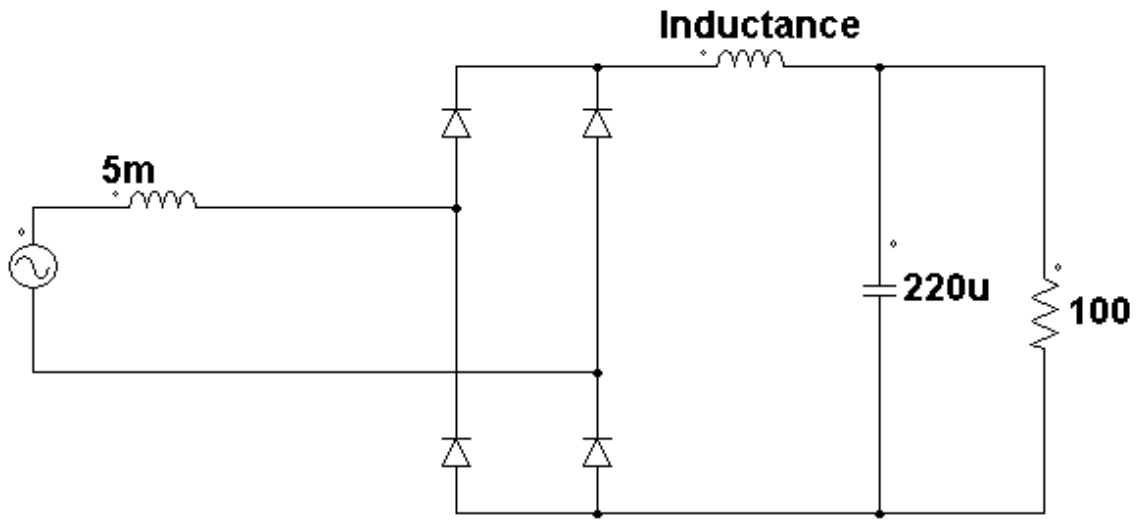


Fig. 4.9 Inductor on the DC side of the diode bridge rectifier.

PFC circuit and simulated input current waveforms for a 100 Ω constant power load are shown in Fig. 4.9 and Fig. 4.10 for inductance values of 40 mH and 180 mH.

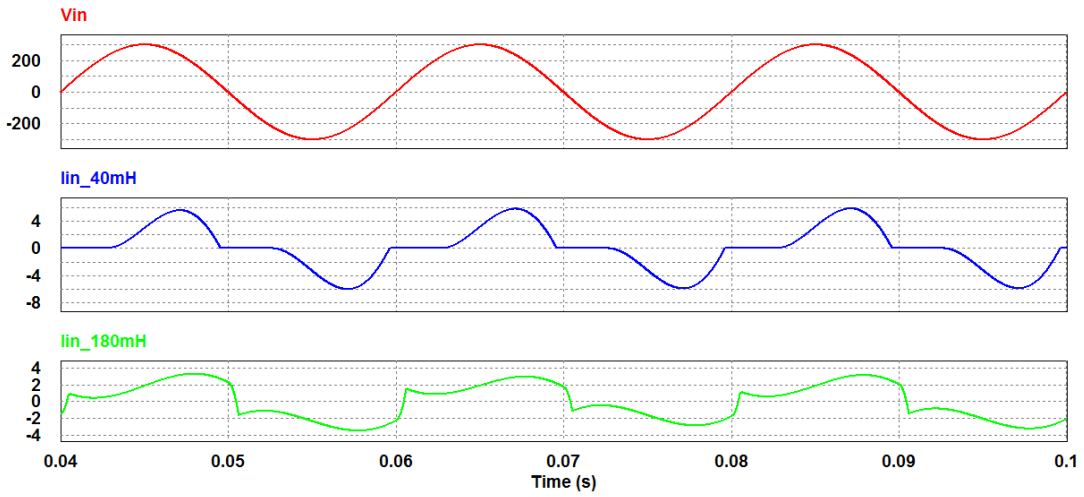


Fig. 4.10 Simulated input voltage and current waveforms

4.6 Active Power Factor Correction Methods

Active PFC methods are the most effective ways to correct power factor of electronic supplies. Active PFC circuits have better characteristics and do not have many of the above drawbacks as passive PFC circuits.

Active PFC functions:

1. Active wave shaping of the input current
2. Filtering of the high frequency switching
3. Feedback sensing of the source current for waveform control
4. Feedback control to regulate output voltage

4.6.1. High Frequency Active PFC

The active PFC's employ six basic converter topologies

1) Buck Corrector
2) Boost Corrector
3) Buck-Boost Corrector
4) Ĉuk Corrector
5) SEPIC Corrector
6) Zeta Corrector

The high frequency active PFC circuit consists of a buck, a boost or a buck-boost or other converter in between the filter capacitor and the bridge rectifier of a conventional rectifier filter circuit. The switching frequency is much higher than the AC source frequency for all converter topologies, the output DC is regulated most of the case. The PFC output voltage

can be higher or lower than the maximum amplitude of the input voltage based on the type of converter. The output voltage can be lower in buck converter, higher in boost converter, higher or lower in buck-boost converter than the input voltage.

4.6.1.1 Buck Converter Based Active PFC

Buck converter can operate only when the instantaneous input voltage V_{in} is higher than the output voltage V_{out}. Inspite of the inductor current being continuous, the input switching current of the converter is discontinuous as the high frequency switch interrupts the input current during every switching cycle. Thus, the input current has significant high-frequency components that increase EMI and filtering requirements.

This converter based PFC circuit and its associated waveforms are shown in Fig. 4.11 and Fig. 4.12.

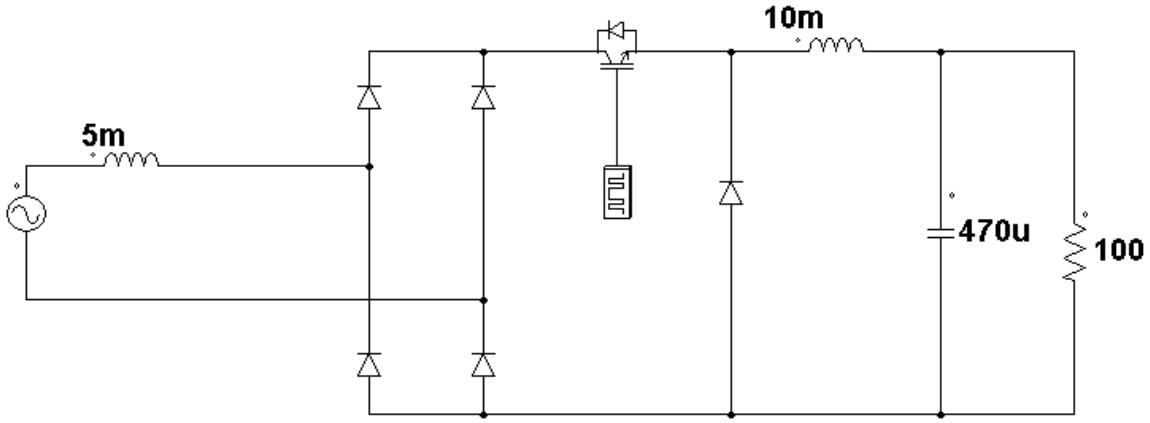


Fig. 4.11 Buck converter based active PFC circuit.

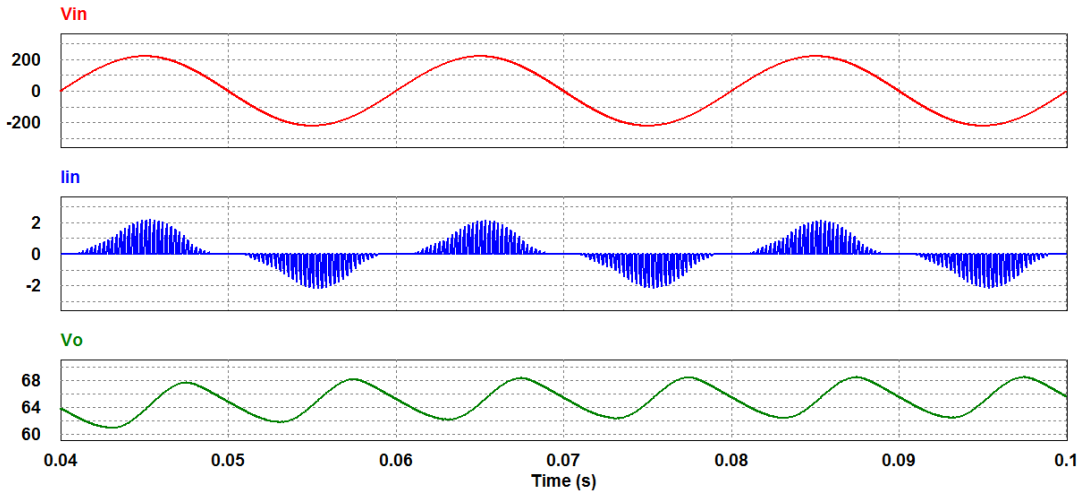


Fig. 4.12 Simulated voltage and current waveforms

4.6.1.2Boost Converter Based Active PFC

Boost converter can operate only when the instantaneous input voltage V_{in} is lower than the output voltage V_{out}. This converter based PFC circuit and its corresponding waveforms are shown in Fig. 4.13 and Fig. 4.14. The input switching current of the converter is continuous as the boost inductor is placed in series with the input and the high frequency switch does not interrupt the input current. So the input current has lesser high-frequency components resulting in lower EMI and reduced filtering requirements. The output capacitor limits the switch's turn-off voltage to almost the output voltage through diode and thus protects the switch.

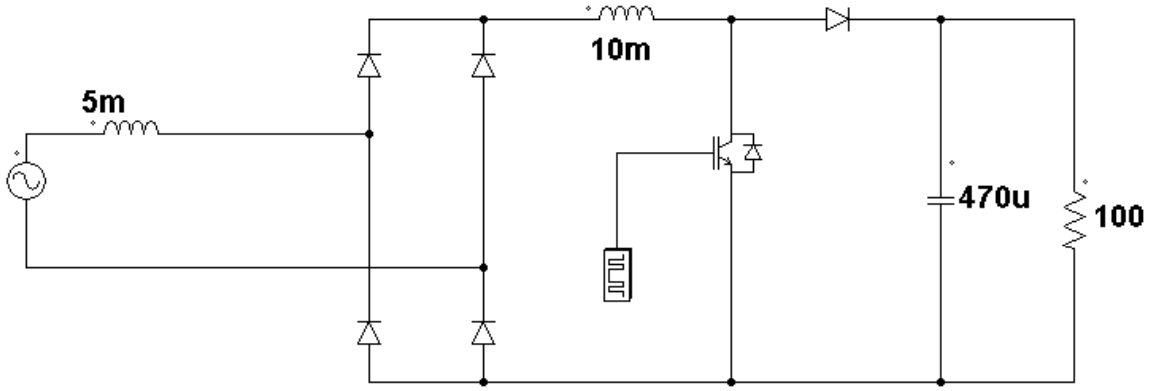


Fig. 4.13 Boost converter based active PFC circuit.

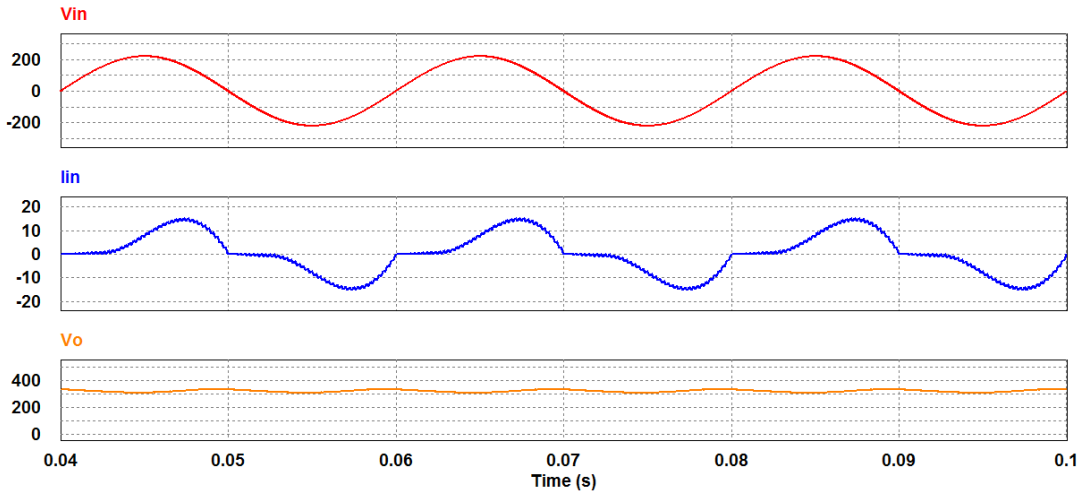


Fig. 4.14 Simulated voltage and current waveforms.

4.6.1.3 Buck-Boost Converter Based Active PFC

Buck-Boost converter can step up or step down the input voltage. This converter based PFC circuit and its associated waveforms are shown in Fig. 4.15 and Fig. 4.16. This output voltage

is inverted. The input current does not have crossover distortions due to its operation throughout the line-cycle. This gives the line current envelope no distortion near the input voltage zero crossing. Although even if the inductor current is continuous, the input switching current of the converter is discontinuous because the high frequency switch interrupts the input current. Thus, the input current has significant high-frequency components that increase EMI and filtering requirements.

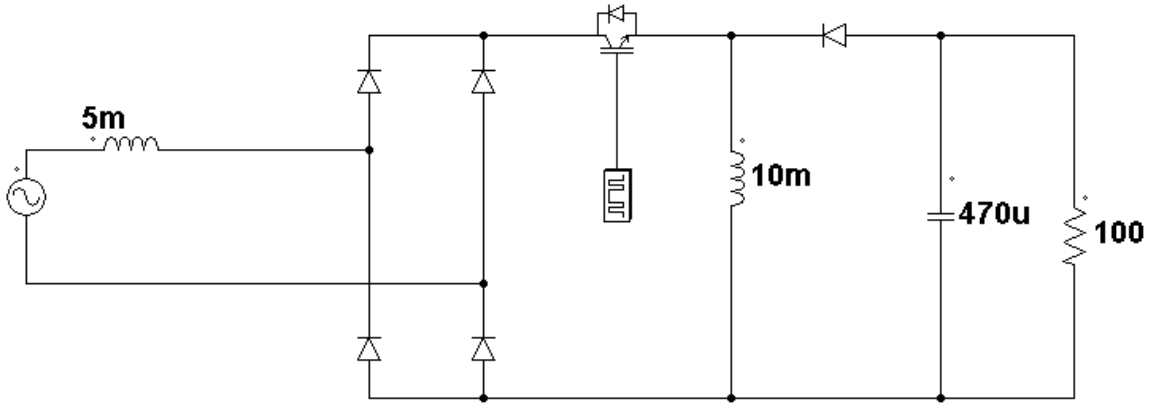


Fig.4.15 Buck-Boost converter based active PFC circuit.

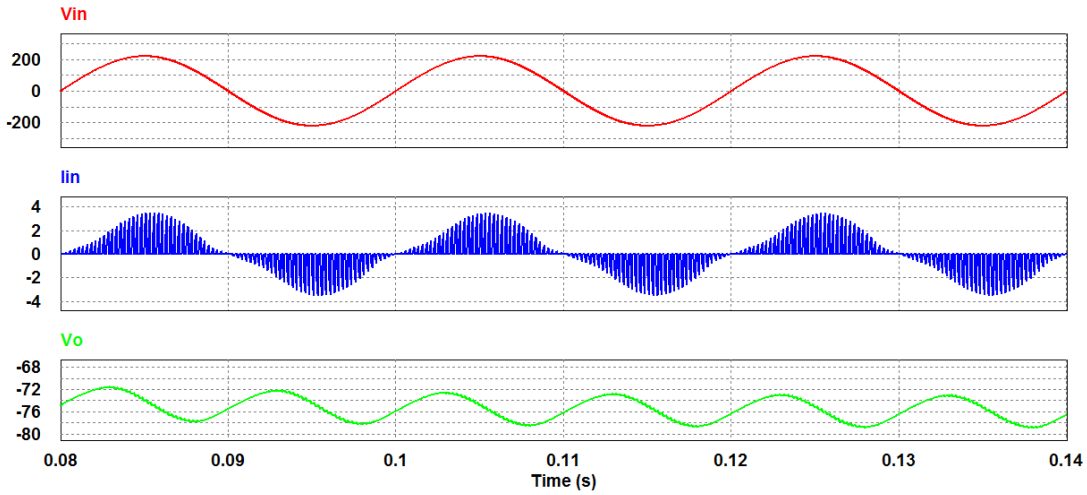
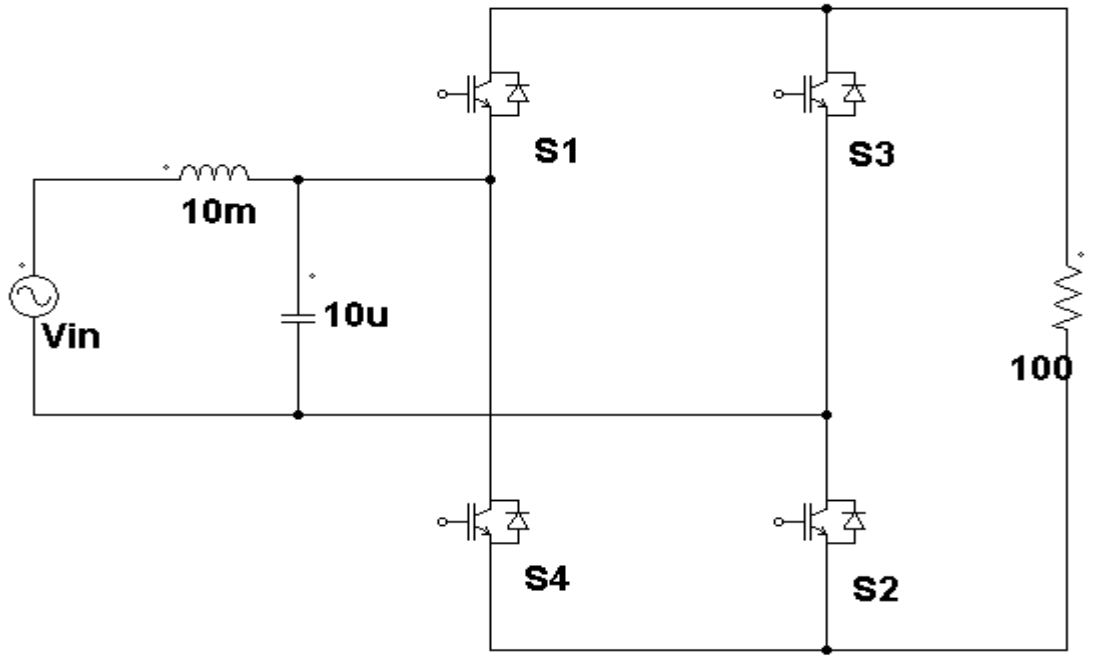


Fig. 4.16 Simulated voltage and current waveforms.

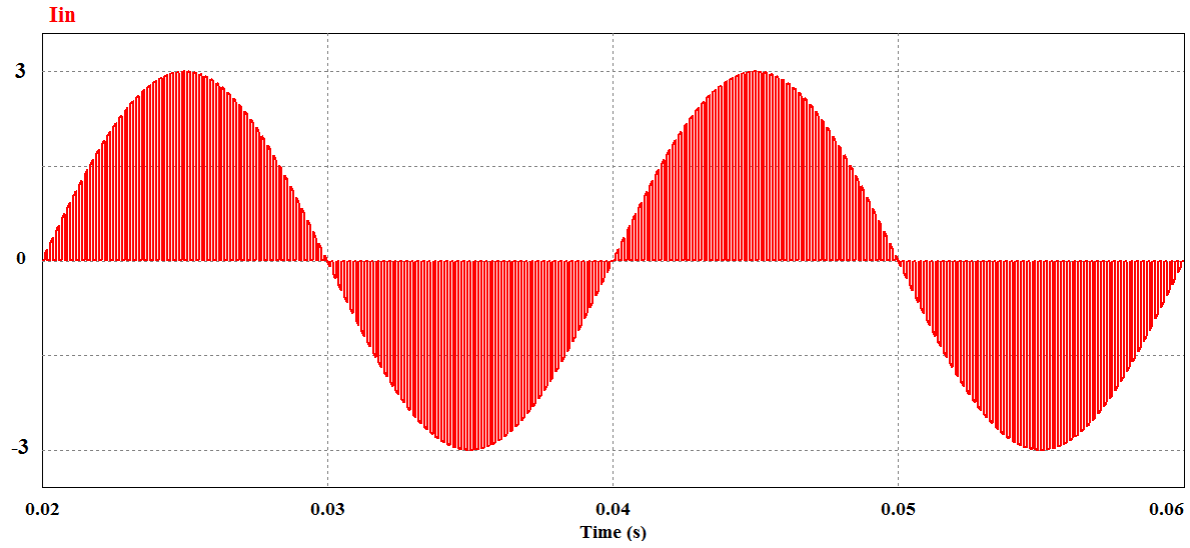
4.7. Four Switches based bidirectional rectifier

Fig. 4.17 shows the circuit diagram of four controlled switches based bidirectional rectifier. The switches are controlled such that at positive half cycle switches S1 and S2 conduct.

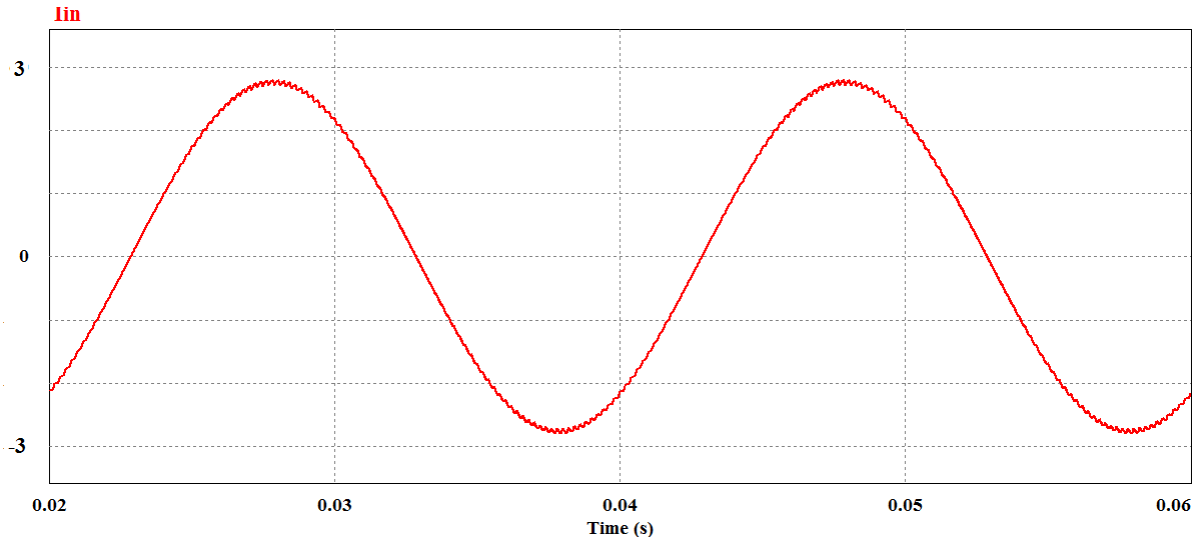
Similarly at negative half cycle S3 and S4 conduct. Figs. 4.18 to 4.19 show the simulated waveform of input current before and after filtering respectively.



4.17. Four Switches based bidirectional rectifier



4.18. Wave shape of the bidirectional rectifier before filtering.



4.19. Wave shape of the bidirectional rectifier after filtering

4.8. The Future of Power Factor Correction

PFC methods are frequently used today in off-line power converter designs. Active PFC circuits are used more than passive PFC circuits. Additional circuitry is required for active PFC method which has some adverse impacts on the system:

a. Efficiency is slightly lower due to additional conversion stage.

b. Additional cost and complexity for the power converter.

c. Reliability is lower due to additional components.

Although PFC has several limitations it is often a very good design trade-off for the power system. Undistorted current waveforms, universal input operation and additional useful power capability of converters is provided by using PFC. For all AC-DC converter designs active power factor correction is very useful. So, optimizing cost, increasing efficiency and reliability of PFC circuits is the common challenge of the day.

CHAPTER 5

PROPOSED ĈUK AC-DC CONVERTER

A single phase single switched Ĉuk AC-DC converter is proposed in this chapter. For simulation purpose PSIM professional version 9.0.3.400, has been used. The working principle of proposed Ĉuk converter is described here. The wave shapes of input voltage, input current, output voltage and input current spectrum at different frequencies and duty cycles are also shown. Data table of the input current THD (%), input power factor, efficiency (%) and output power at different frequencies and duty cycles of the proposed converter are presented in this chapter. The proposed converters are compared to corresponding conventional converters with switching at DC side. Comparisons are made in terms of input current THD (%), input power factor and efficiency (%) at different duty cycles and loads.

5.1 Proposed Single phase Ĉuk AC-DC Converter

Fig. 5.1 shows the circuit diagram of proposed single phase single switch Ĉuk AC-DC converter. The circuit consists of inductors (L1, L2), capacitors (C1, C2), diodes and a switch (M1). As the given supply voltage is AC, the conversion on both positive and negative cycle of the input voltage is required. L1and C1 are used for positive half cycle and L2 and C2 are for negative half cycle. The inductors L1_pos, L1_Neg, L2_pos, L2_Neg and capacitors C_pos and C_Neg form the input filter. C_Load and R_Load are the output capacitor and load respectively.

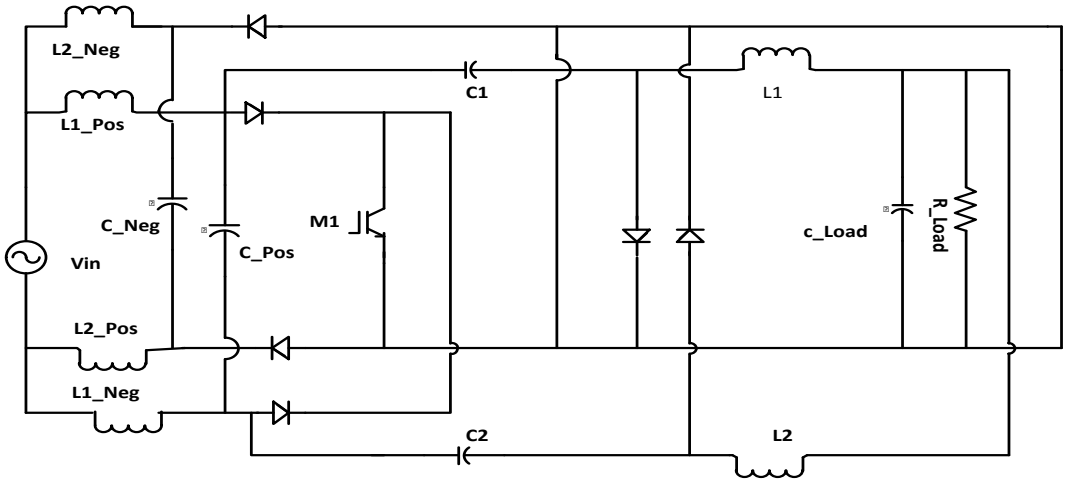


Fig. 5.1Proposed AC-DC Ĉuk Converter

5.2 Principle of Operation

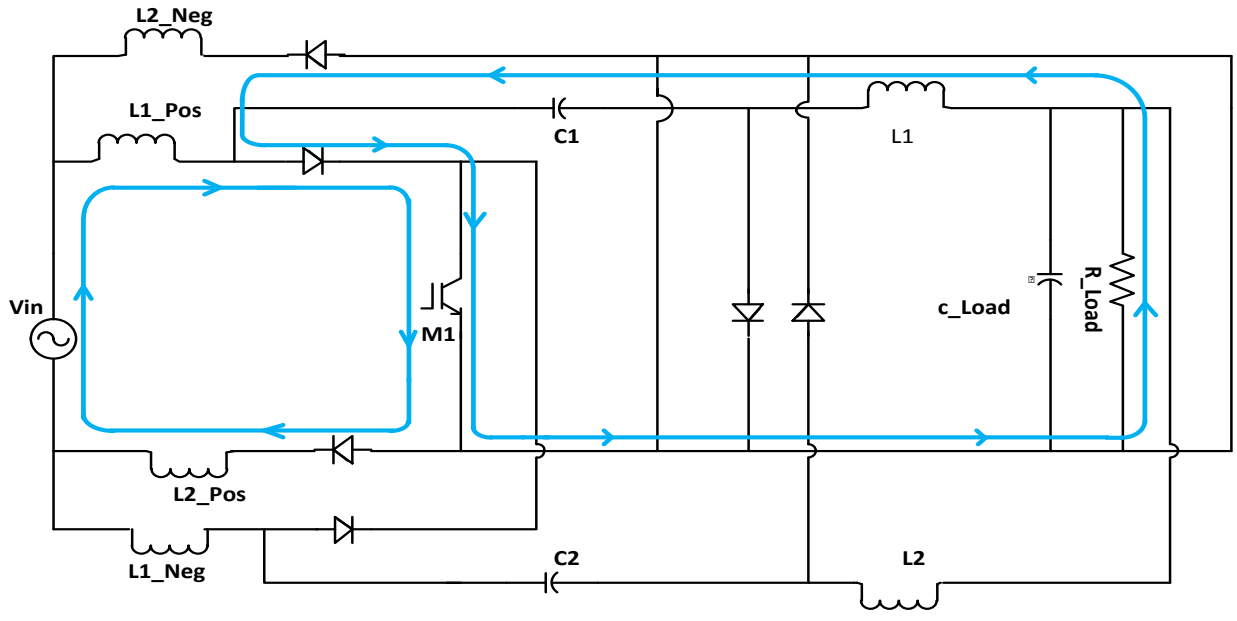
Input AC current chopping at high frequency, provides switched AC current that requires small filter to make it nearly sinusoidal. As a result, the input current THD reduces and the input power factor improves. The proposed Ĉuk AC to DC converter has four operating states – positive and negative half cycles each with switch ON and OFF condition, as shown in Fig.5.2. The operating states are described below.

State 1 is for positive half cycle of the input signal when the switch S is turned ON. This state is presented in Fig. 5.2 (a).The blue line indicates the direction of current flow. Energy transfer is associated with inductors and capacitors L1 and C1 for this state.

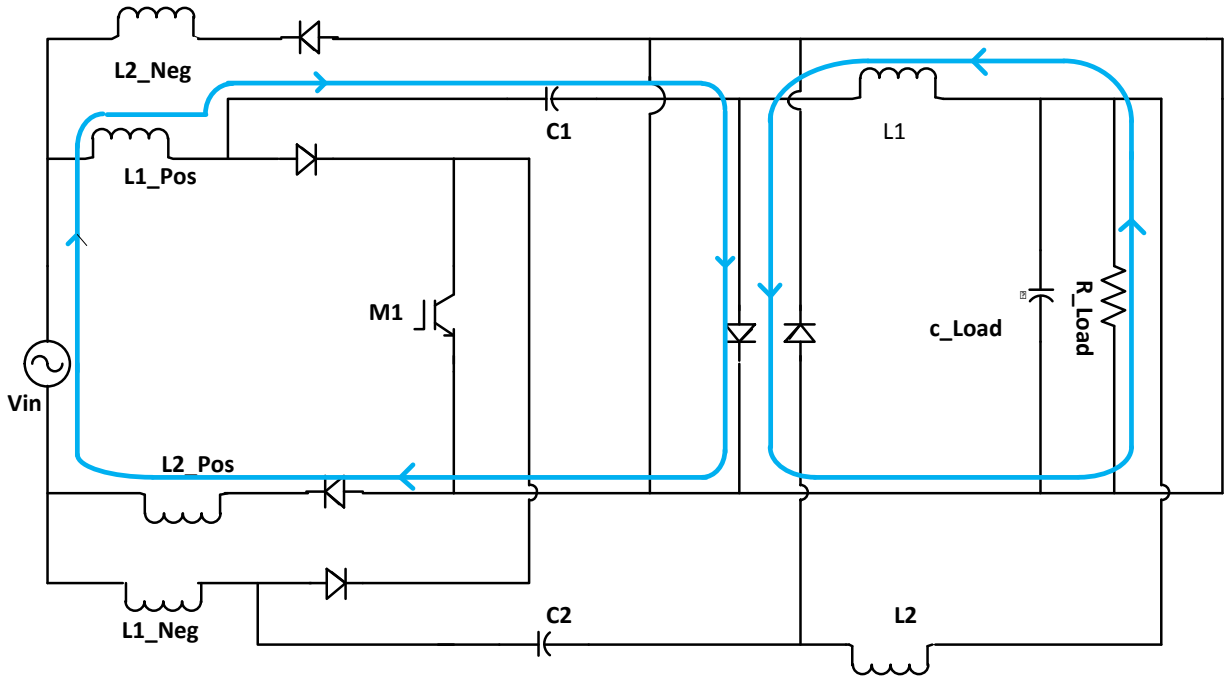
State 2 is for the positive half cycle of the input signal when the switch S is OFF. This state is presented in Fig. 5.2 (b).The blue line indicates the direction of current flow. Energy transfer is associated with inductors and capacitors L1 and C1 for this state.

State 3 is for the negative half cycle of the input signal when the switch S is turned ON. This state is shown in Fig. 5.2 (c).The violet line indicates the direction of current flow. Energy transfer is associated with inductors and capacitors L2 and C2 for this state.

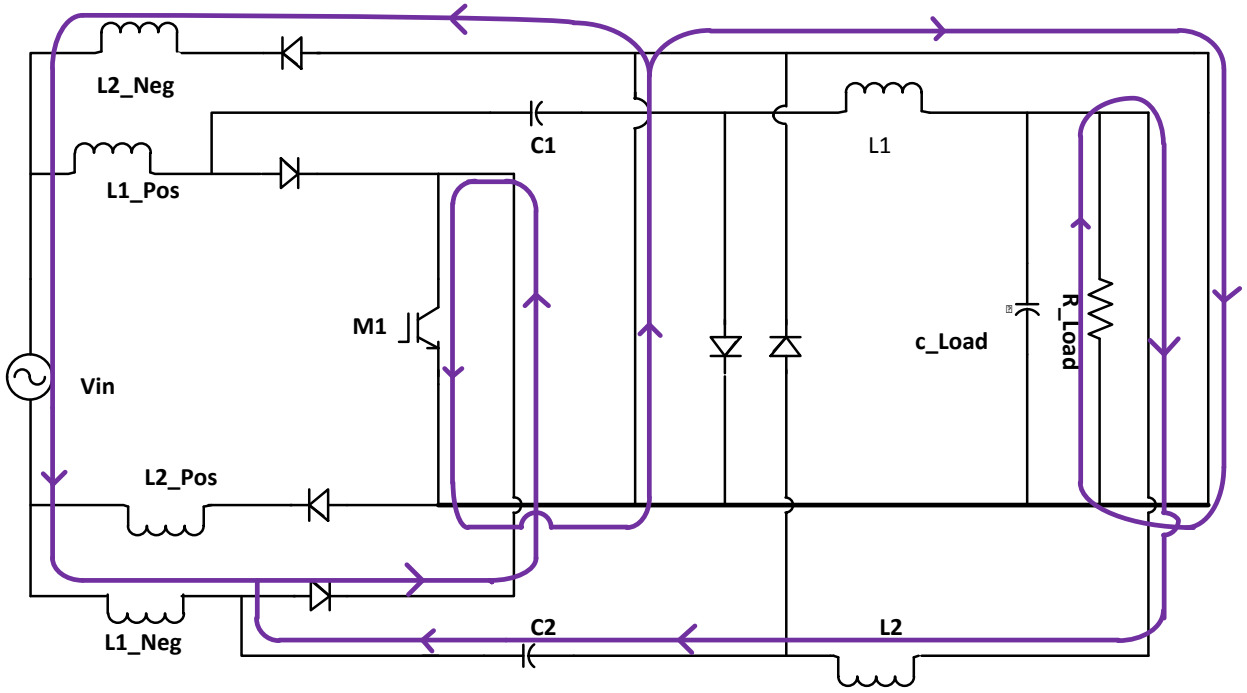
State 4 is for the negative half cycle of the input signal when the switch S is turned OFF. This state is shown in Fig. 5.2 (d).The violet line indicates the direction of current flow. Energy transfer is associated with inductors and capacitors L2 and C2 for this state.



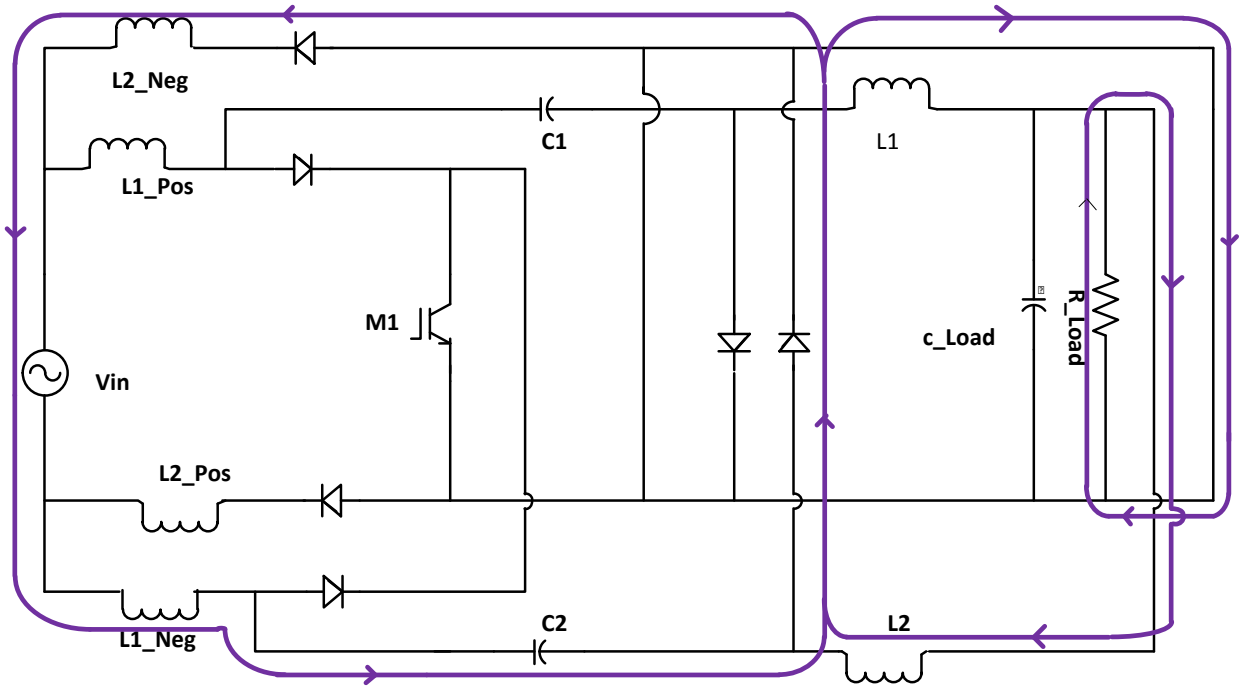
(a)


L2_Neg
C1
L1
L1_Pos
M1
c_Load
R_Load
Vin
L2_Pos
L1_Neg
C2
L2

(b)


L2_Neg
C1
L1
L1_Pos
M1
c_Load
R_Load
Vin
L2_Pos
L1_Neg
C2
L2

(c)



(d)

Fig. 5.2. Four states of operation of proposed AC-DC converter (A) State 1, circuit when switch is ON during positive half cycle of the AC supply, (B) State 2, circuit when switch is OFF during positive half cycle of the AC supply, (C) State 3, circuit when switch is ON during negative half cycle of the AC supply,(D) State 4, circuit when switch is OFF during negative half cycle of the AC supply

5.3 Simulation Results

5.3.1 Circuit Parameters

For simulation of Ĉuk configuration, an input ac source of 300V amplitude with frequency of 50 Hz. is used. An IGBT is used for switching purpose. For Ĉuk scheme, the inductors L1and L2 have the values of 1.5mH each. The filter inductors L1_pos, L1_Neg, L2_pos, L2_Neg have the values of 4 mH and capacitors C1and C2 have the values of 0.5µF each. The filter capacitors C_pos and C_neg have the values of 1µF each. The output capacitor C_Load has the value of 100 µF and a resistor R_Load of 100 Ω is used as load in the proposed circuit. The proposed single-phase converter has been compared with the conventional single-phase diode bridge rectifier followed by a DC-DC Ĉuk converter shown in Fig. 5.3.The conventional circuits also have same parameters and conditions like the proposed one for simulation.

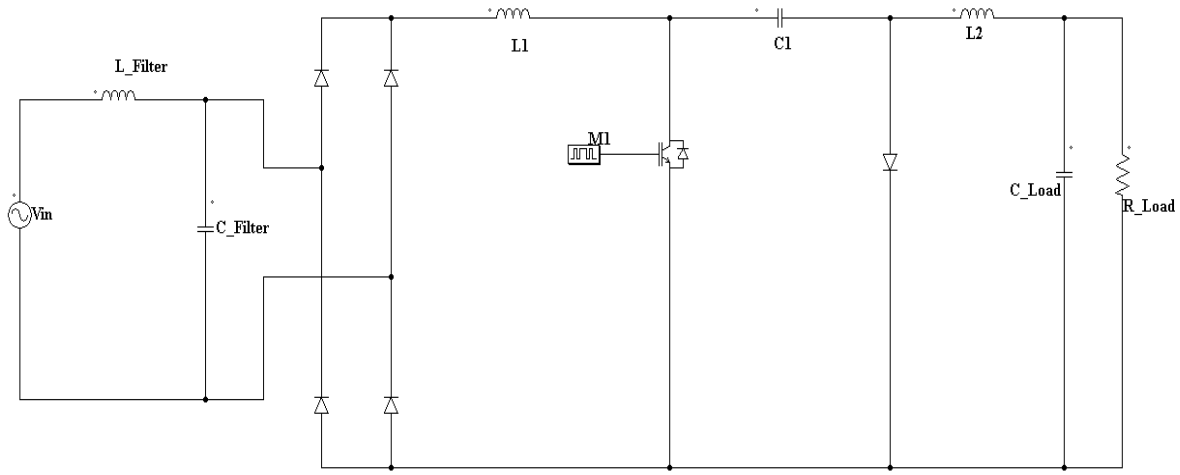


Fig. 5.3 Conventional Ĉuk AC-DC Converter

5.3.2 Results from Simulation

Typical input voltage, input current and output voltage waveforms of the proposed single-phase AC-DC Ĉuk converter circuit at different switching frequencies (f_s) of different duty cycles (D) and load resistance (R_Load) of 100 Ω are presented here. Fig. 5.4 shows the typical input voltage of the proposed converter. Input current at different frequencies and duty cycles and their corresponding spectrums are presented in Figs. 5.5 to 5.16. From these figures it is observed that, the input current is nearly sinusoidal. Figs. 5.17 to 5.28 shows the input current and corresponding input current spectrums of the conventional circuit consisting of a rectifier followed by a Ĉuk DC-DC converter under same operating condition to observe the typical improvement. Figs. 5.29 to 5.36 show the Output voltage waveform of proposed Ĉuk converter at switching frequency of 4000 Hz. and different duty cycles.

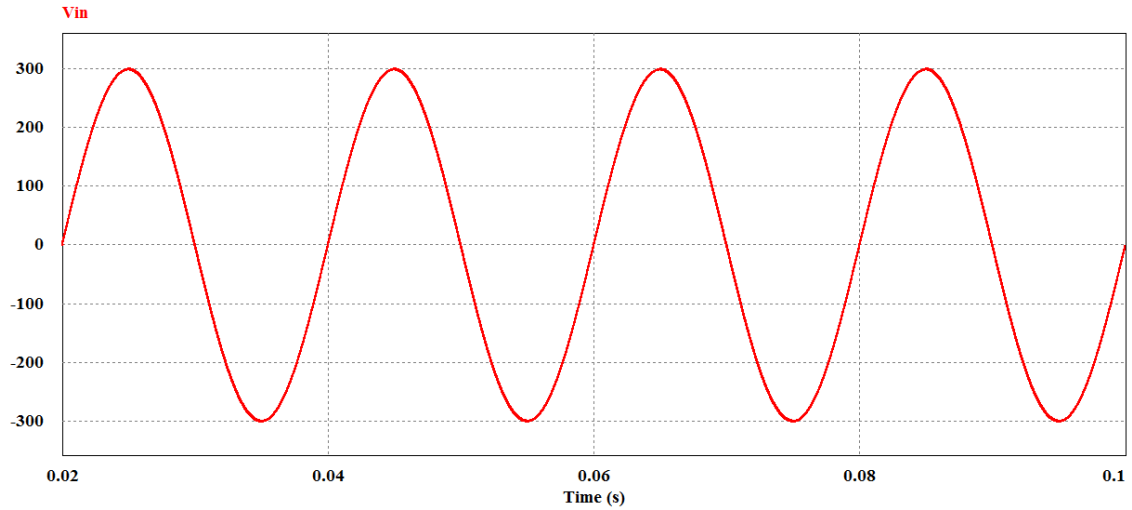


Fig. 5.4 Wave shape of input voltage of Proposed AC-DC Ĉuk Converter

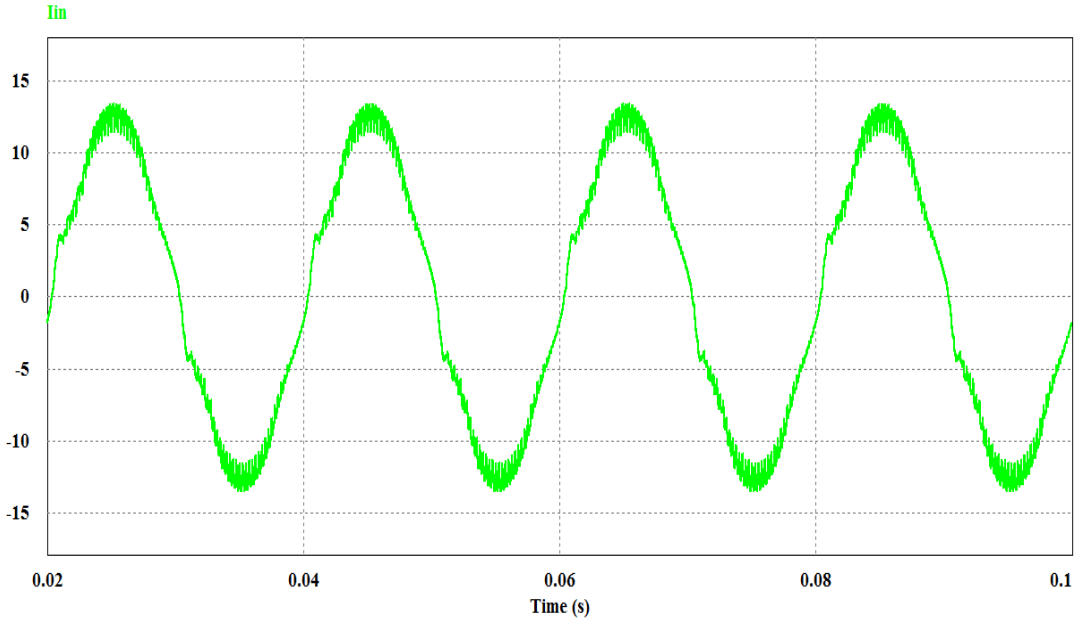


Fig.5.5 Input current of proposed Ĉuk converter at f_s= 4000Hz. and D = 0.6

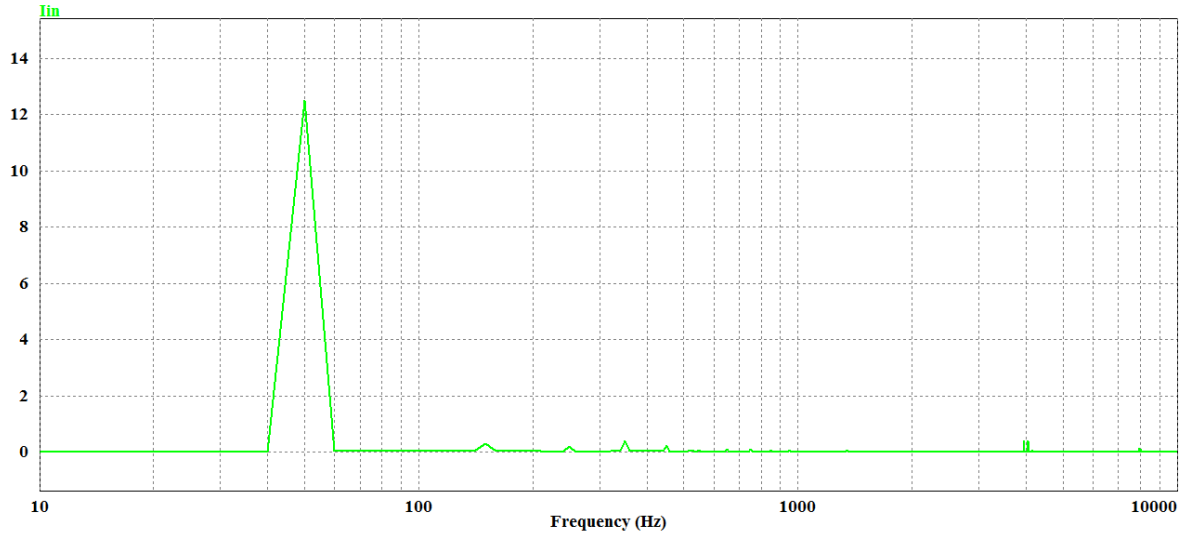


Fig.5.6 Input current spectrum of proposed Ĉuk converter at f_s = 4000Hz. and D = 0.6.

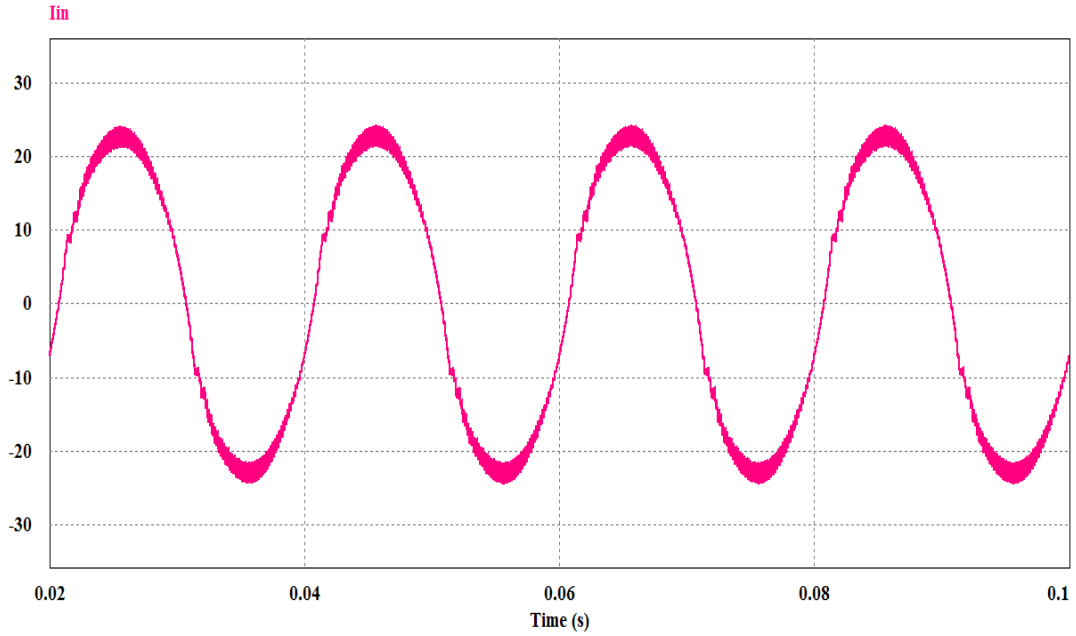


Fig.5.7 Input current of proposed Ĉuk converter at f_s= 6000Hz. and D = 0.6

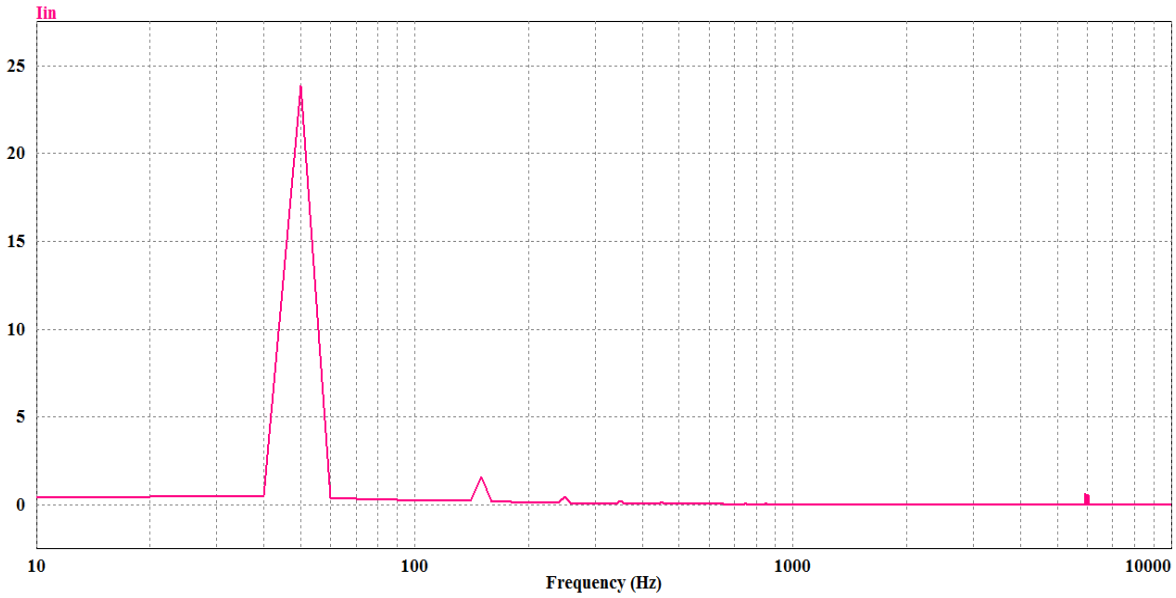


Fig.5.8 Input current spectrum of proposed Ĉuk converter at f_s = 6000Hz. and D = 0.6

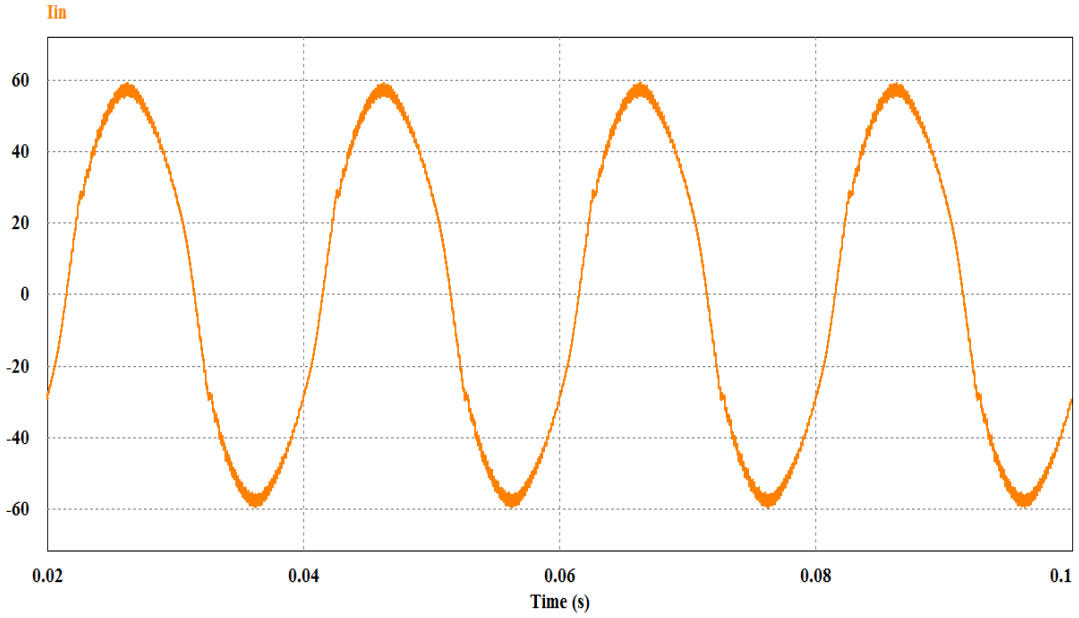


Fig.5.9 Input current of proposed Ĉuk converter at f_s = 6000Hz. and D = 0.8

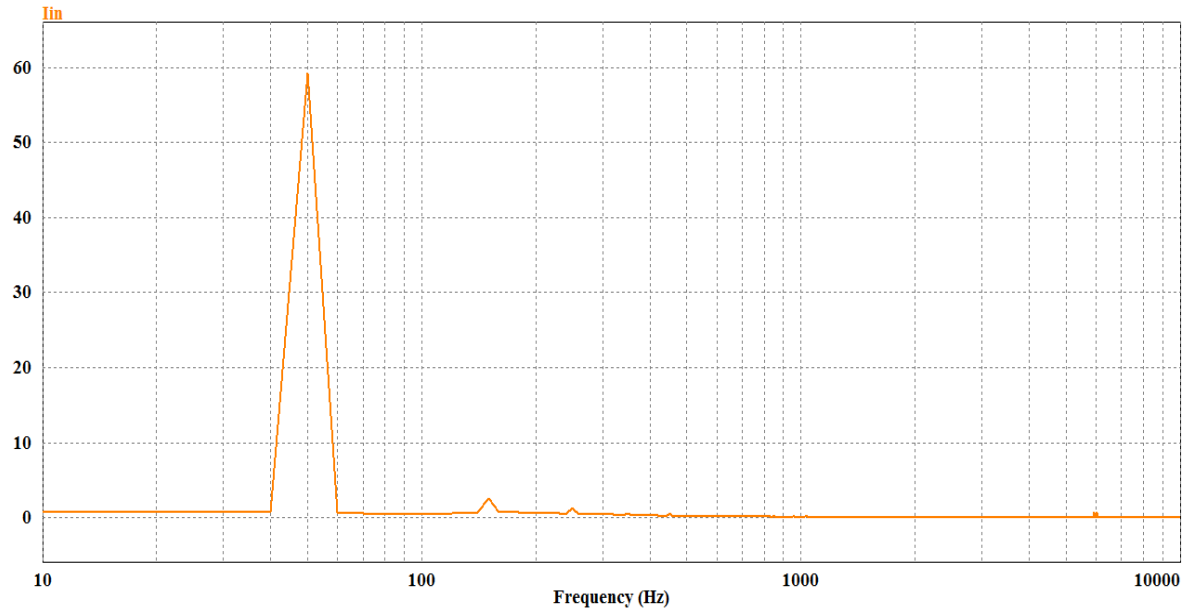


Fig.5.10 Input current spectrum of proposed Ĉuk converter at f_s = 6000Hz. and D = 0.6

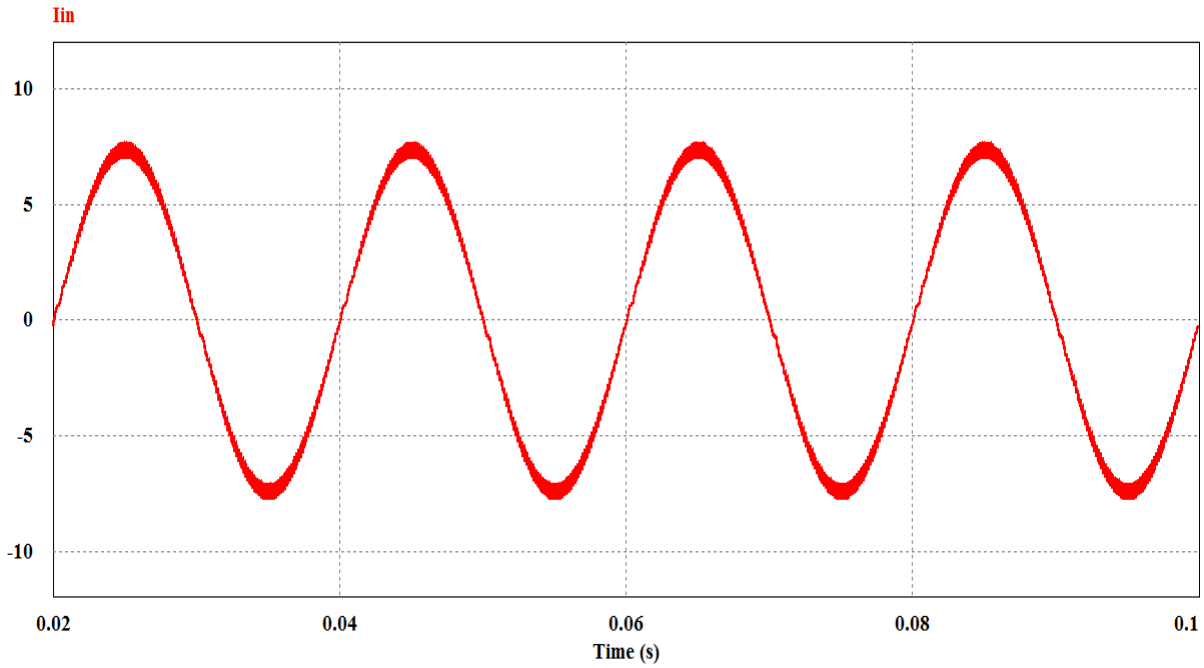


Fig.5.11 Input current of proposed Ĉuk converter at f_s = 8000Hz. and D = 0.4

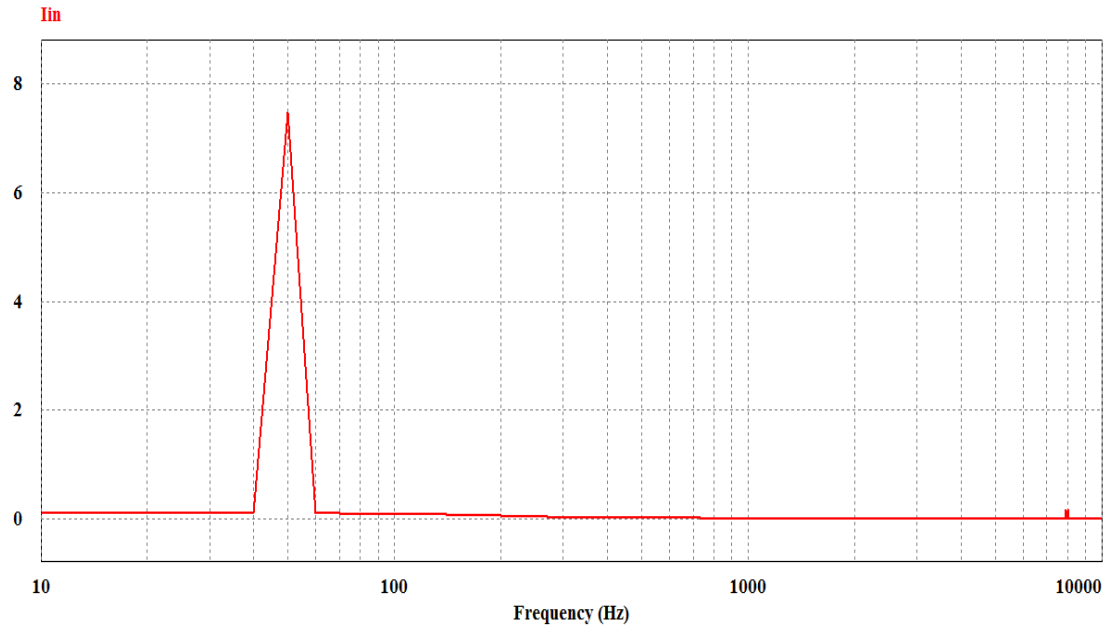


Fig.5.12 Input current spectrum of proposed Ĉuk converter at f_s = 8000Hz. and D = 0.4

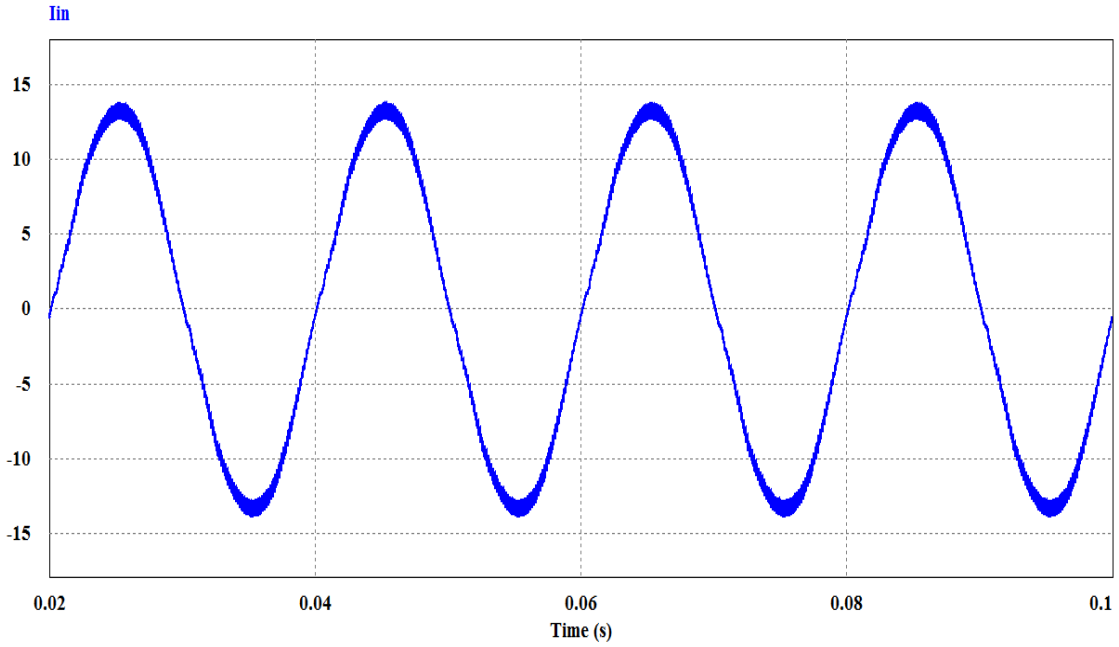


Fig.5.13 Input current of proposed Ĉuk converter at f_s = 8000Hz. and D = 0.5

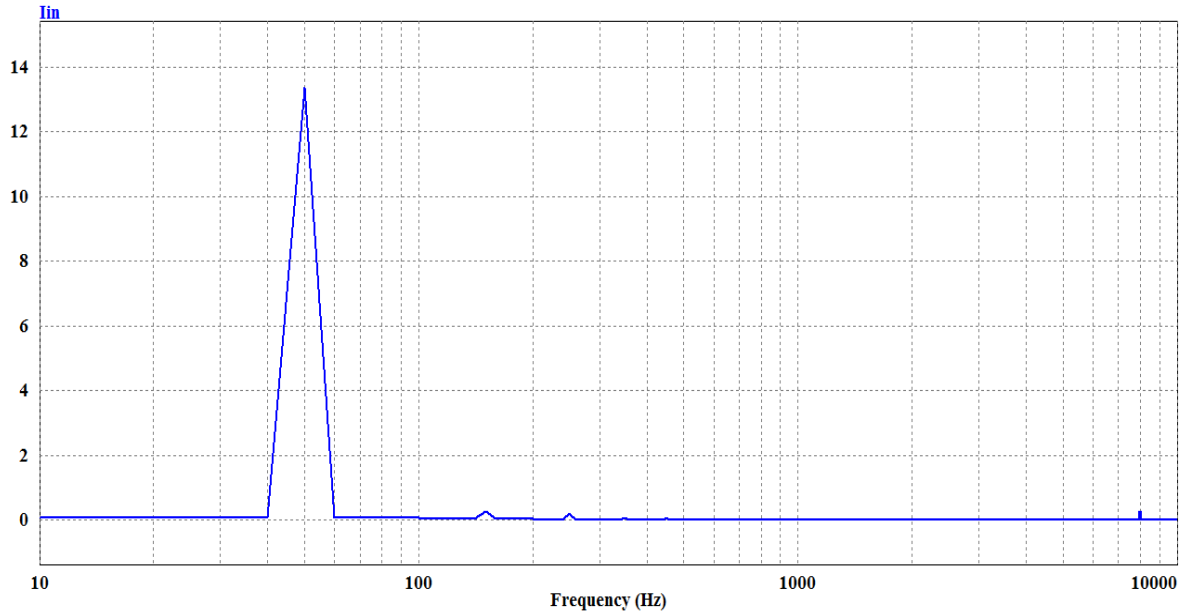


Fig.5.14 Input current spectrum of proposed Ĉuk converter at f_s = 8000Hz. and D = 0.5

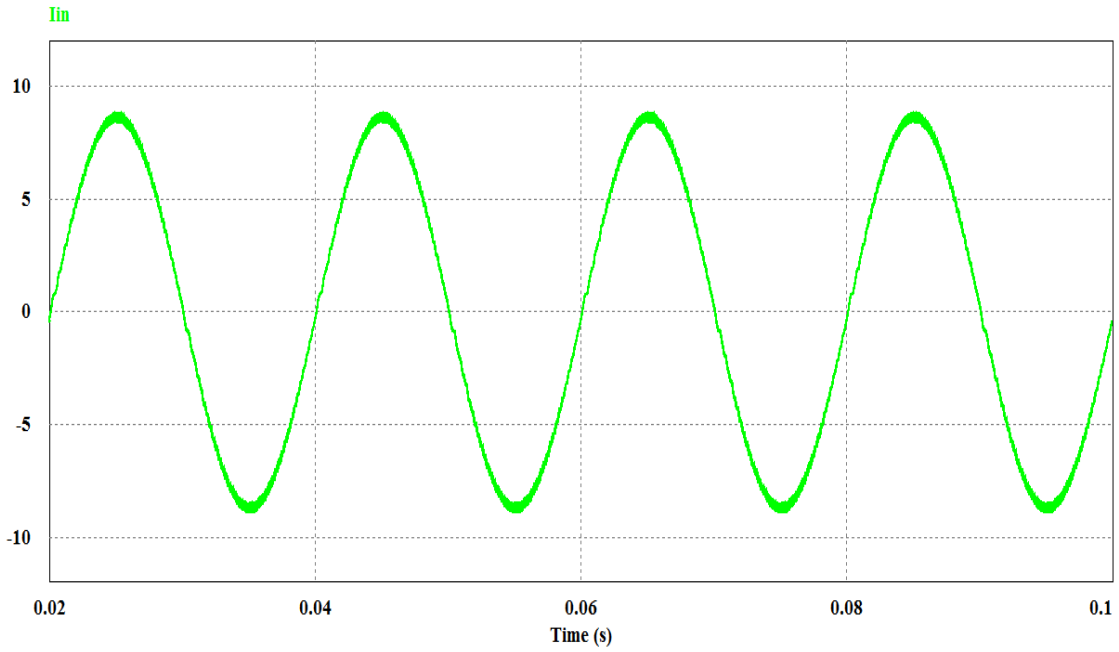


Fig.5.15 Input current of proposed Ĉuk converter at f_s = 10000Hz. and D = 0.5

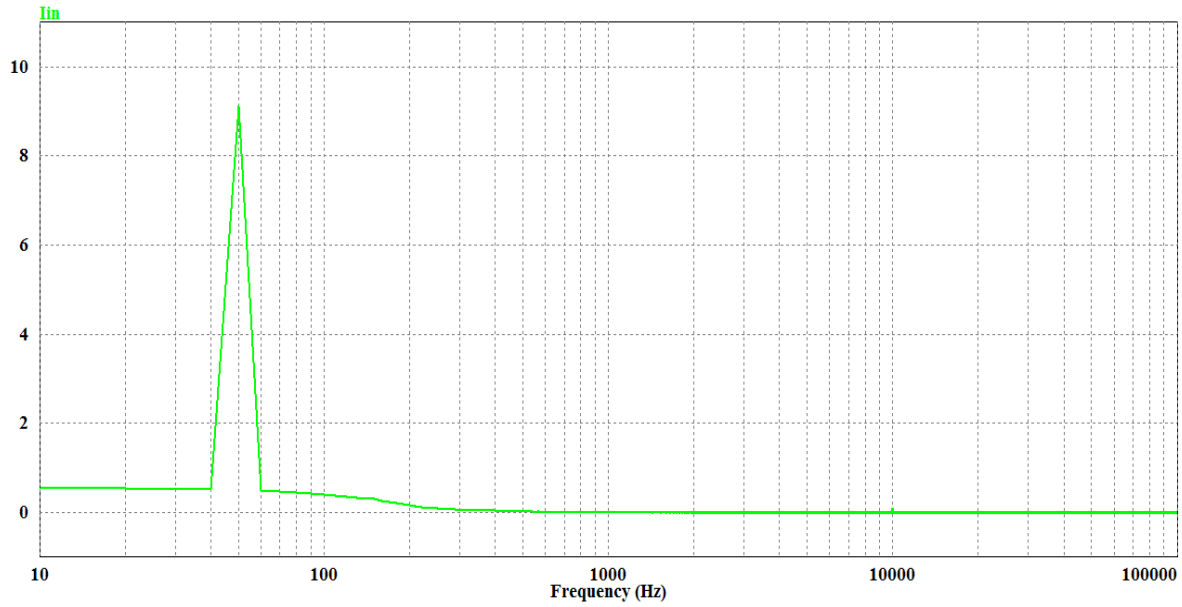


Fig.5.16 Input current spectrum of proposed Ĉuk converter at f_s = 10000Hz. and D = 0.5

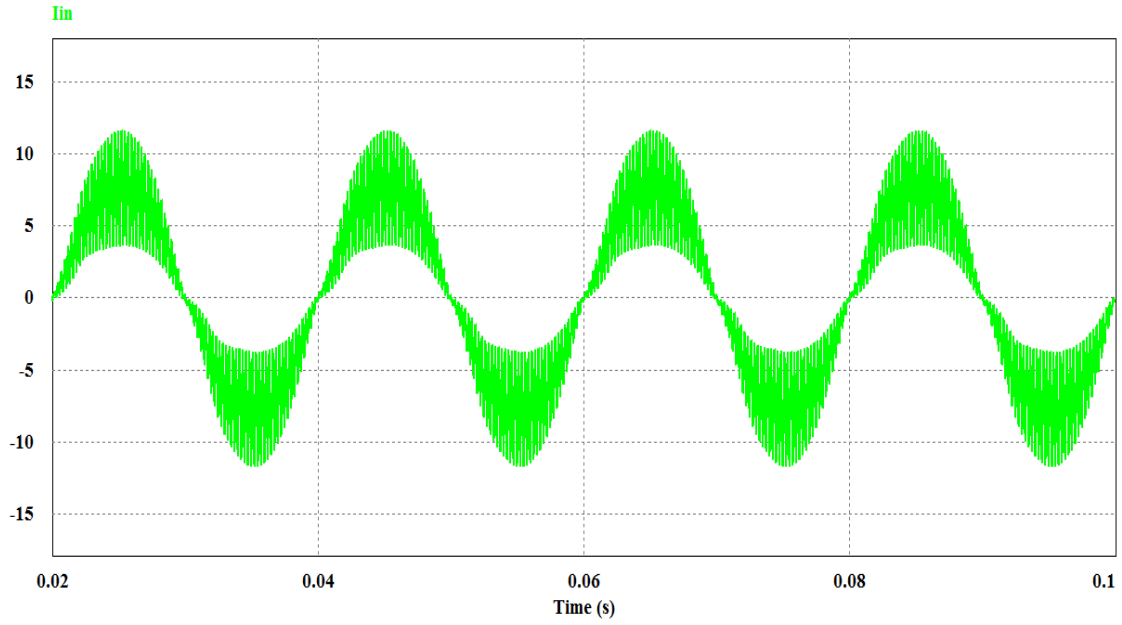


Fig.5.17 Input current of conventional Ĉuk converter at f_s = 4000Hz. and D = 0.6

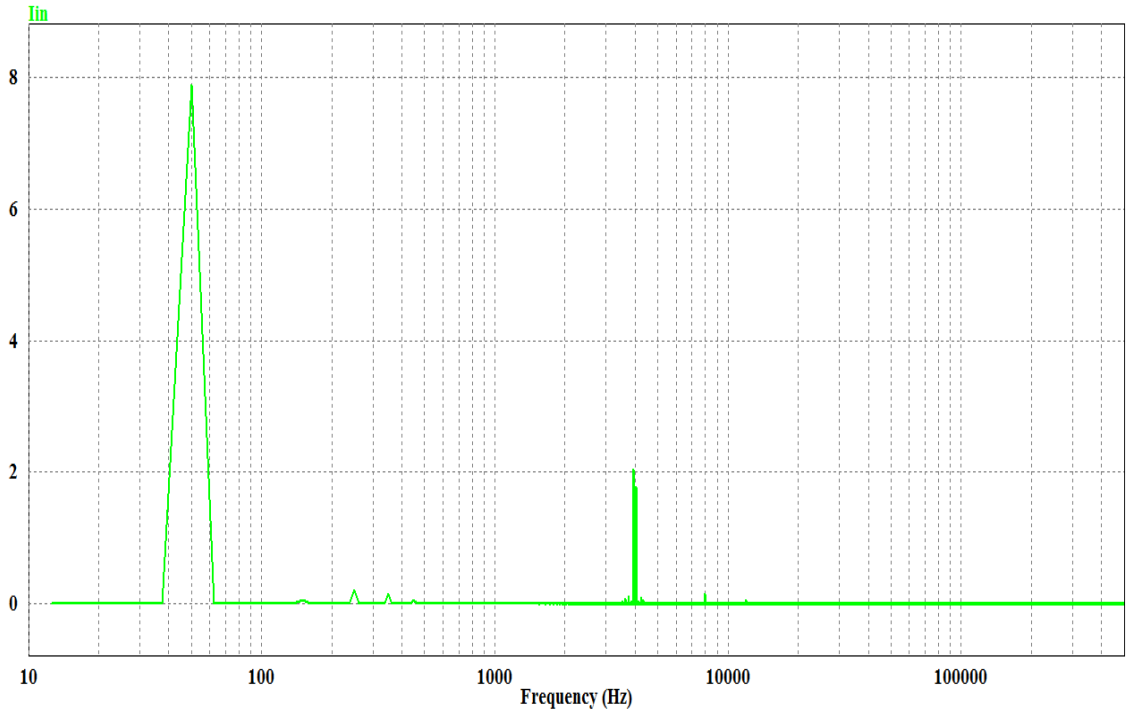


Fig.5.18 Input current spectrum of conventional Ĉuk converter at f_s = 4000 Hz. and D = 0.6

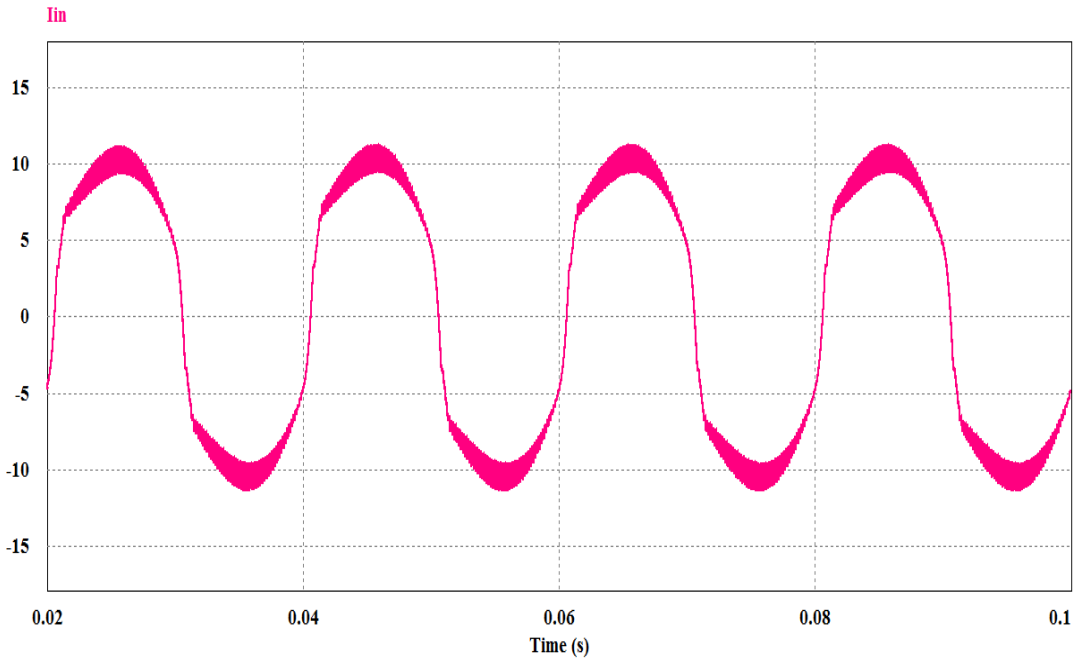


Fig.5.19 Input current of conventional Ĉuk converter at f_s = 6000 Hz. and D = 0.6

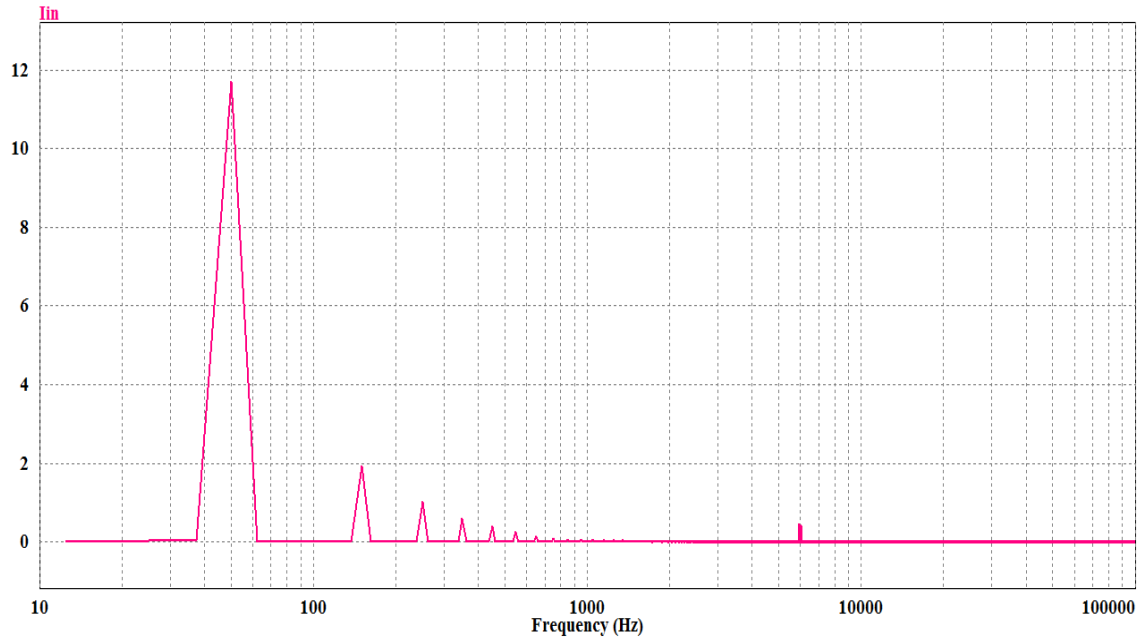


Fig.5.20 Input current spectrum of conventional Ĉuk converter at f_s = 6000 Hz. and D = 0.6

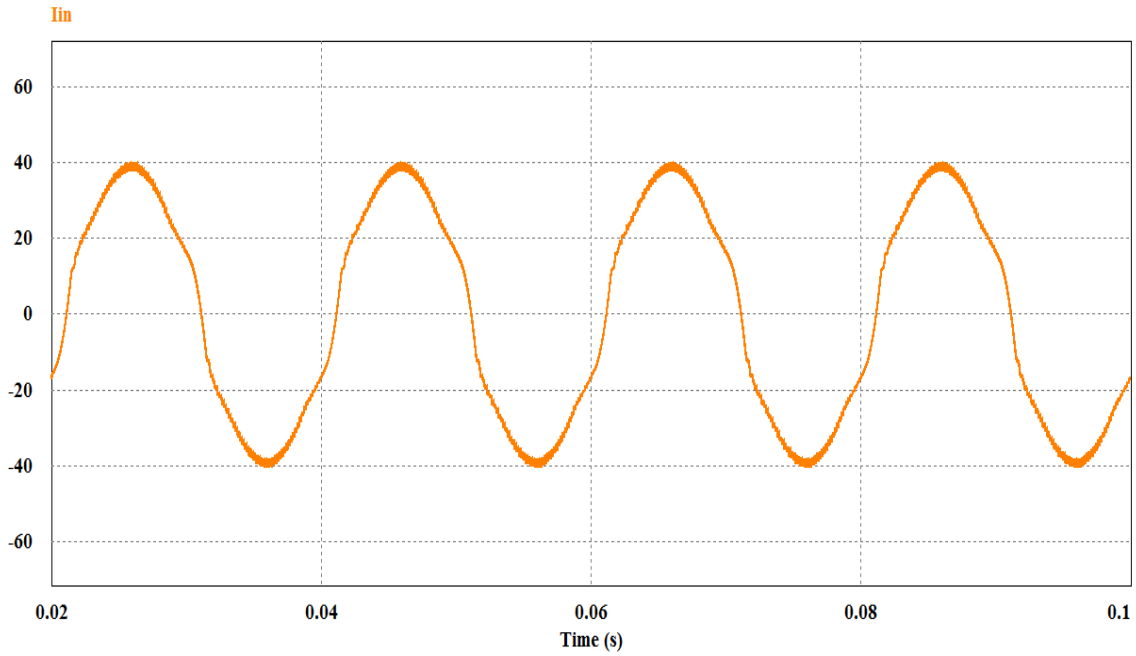


Fig.5.21 Input current of conventional Ĉuk converter at f_s = 6000 Hz. and D = 0.8

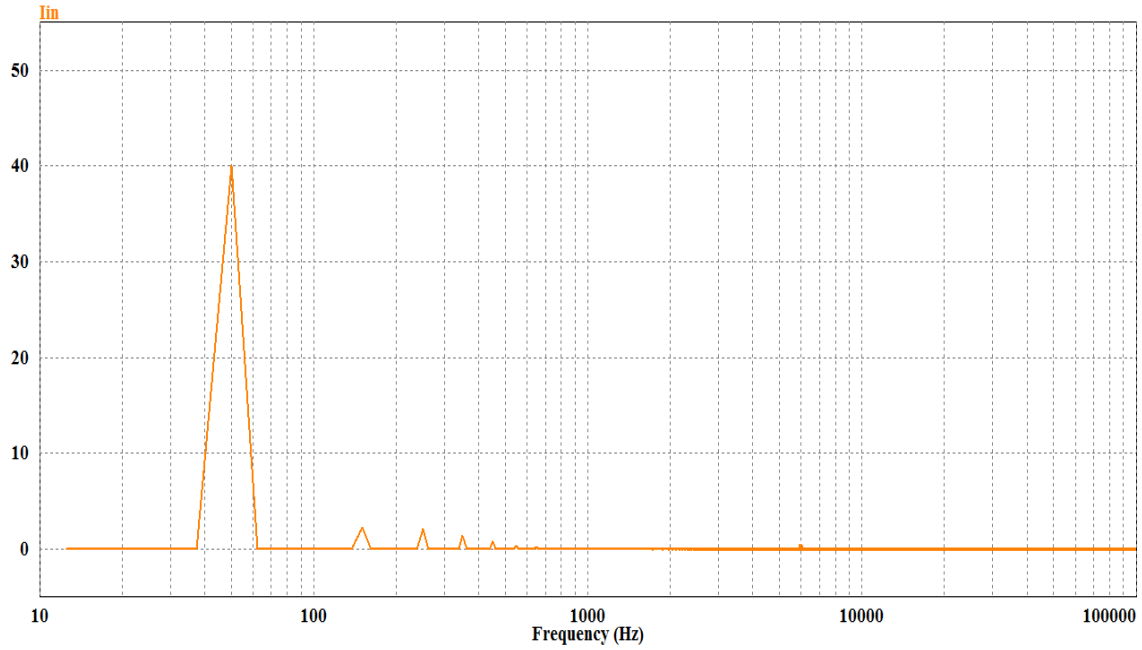


Fig.5.22 Input current spectrum of conventional Ĉuk converter at f_s = 6000 Hz. and D = 0.8

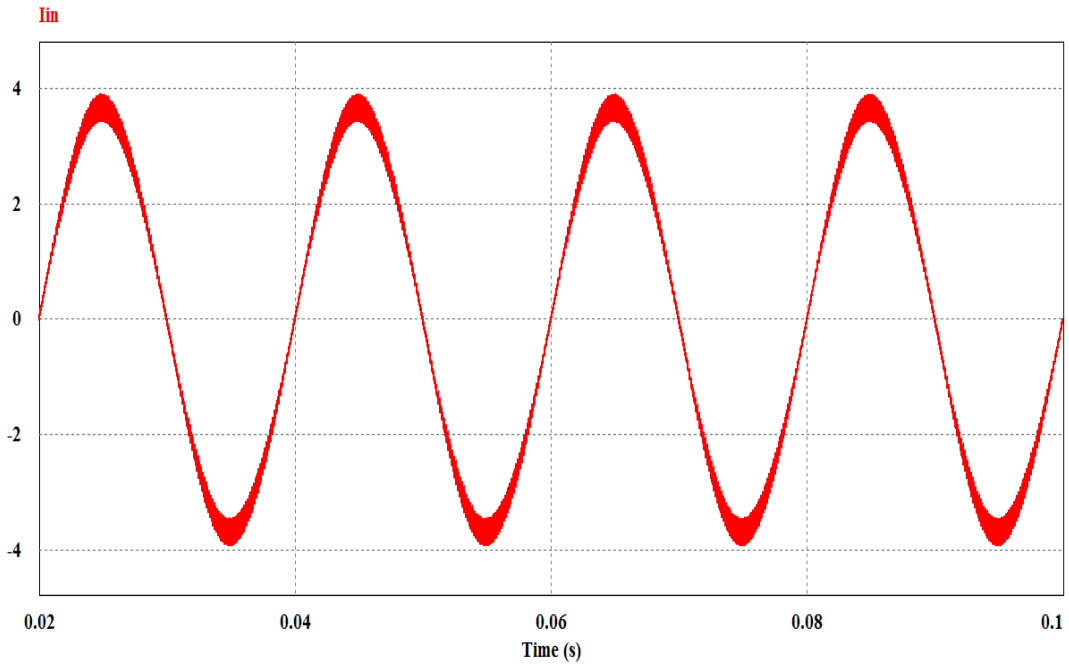


Fig.5.23 Input current of conventional Ĉuk converter at f_s = 8000 Hz. and D = 0.4

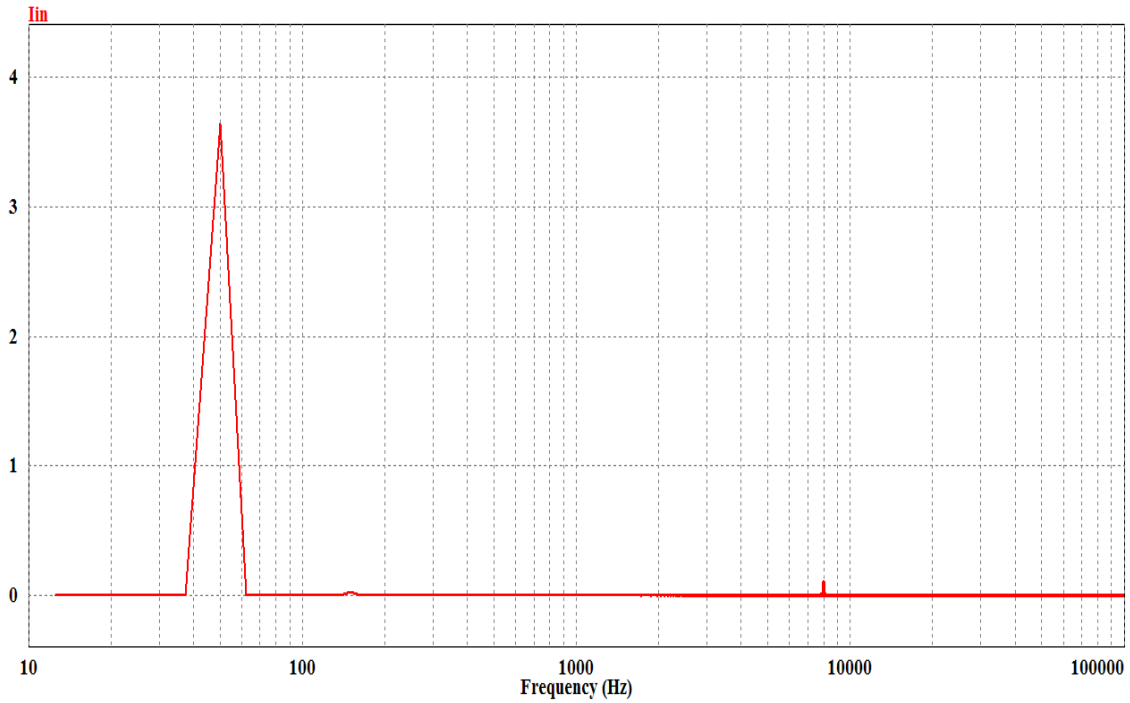


Fig.5.24 Input current spectrum of conventional Ĉuk converter at f_s = 8000 Hz. and D = 0.4

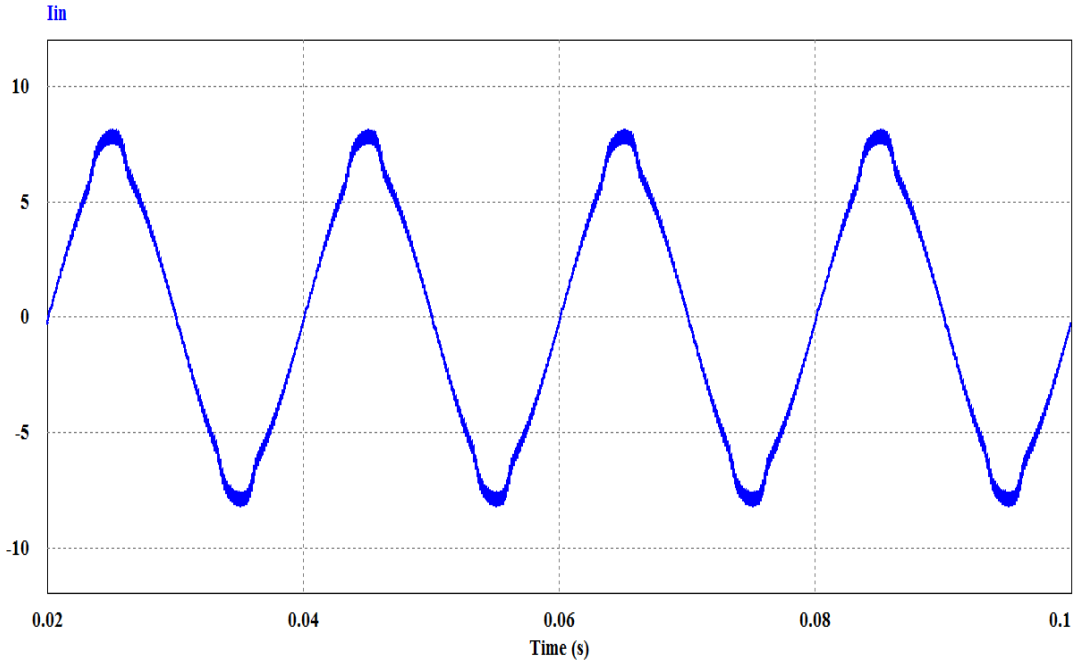


Fig.5.25 Input current of conventional Ĉuk converter at f_s = 8000Hz. and D = 0.5

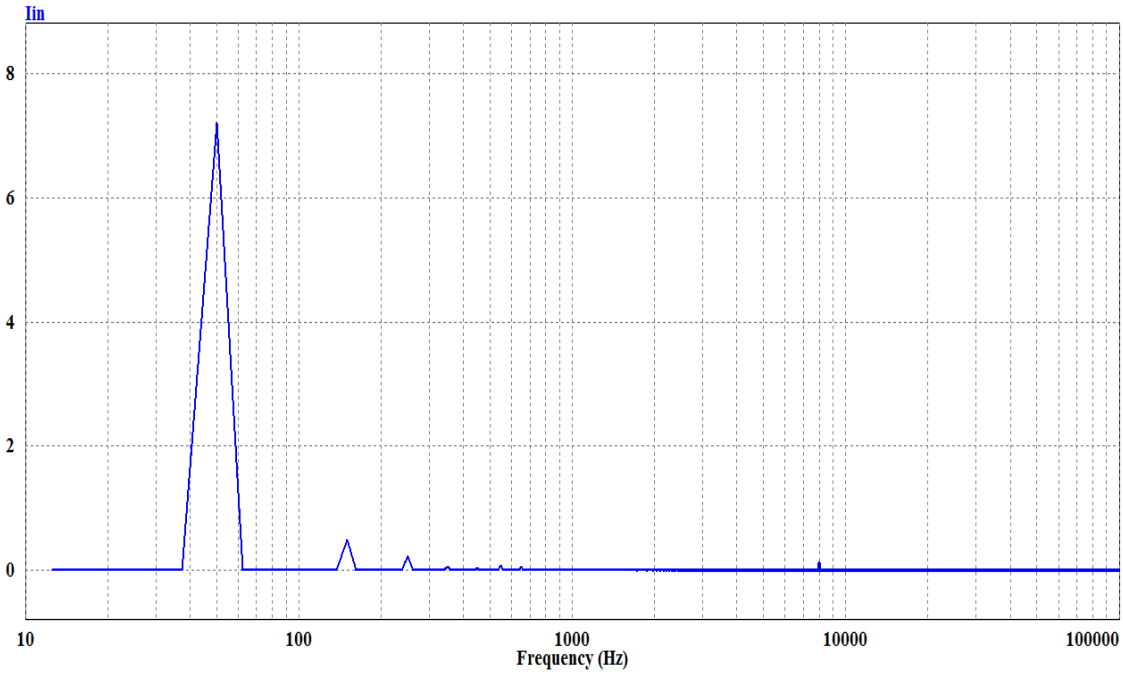


Fig.5.26 Input current spectrum of conventional Ĉuk converter at f_s = 8000Hz. and D = 0.5

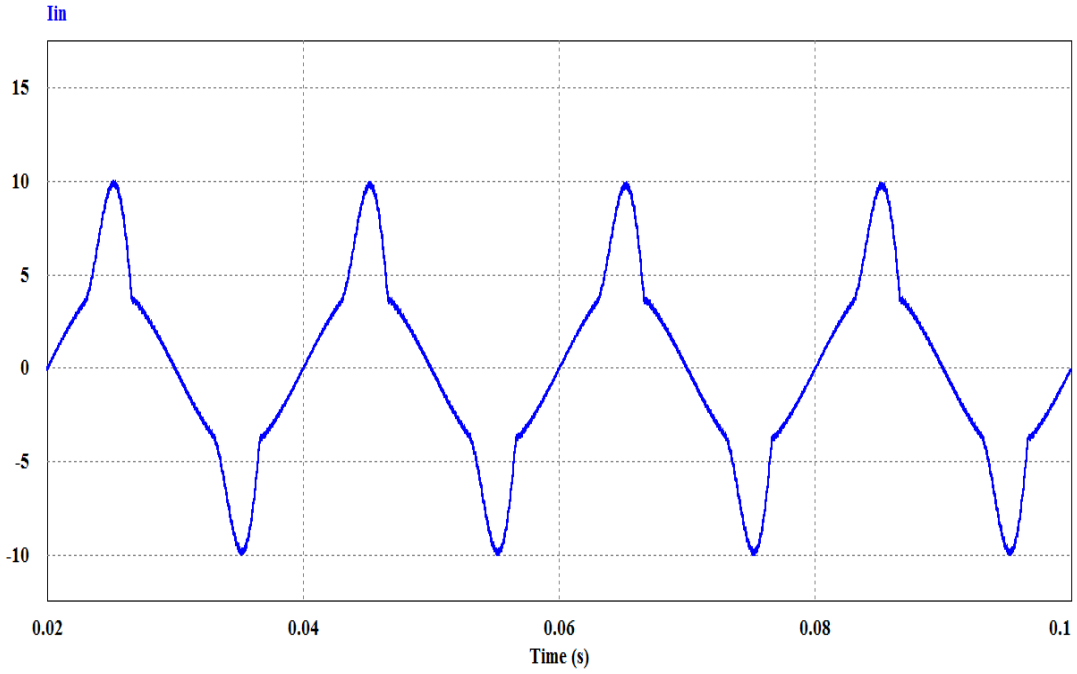


Fig.5.27 Input current of conventional Ĉuk converter at f_s = 10000 Hz. and D = 0.5

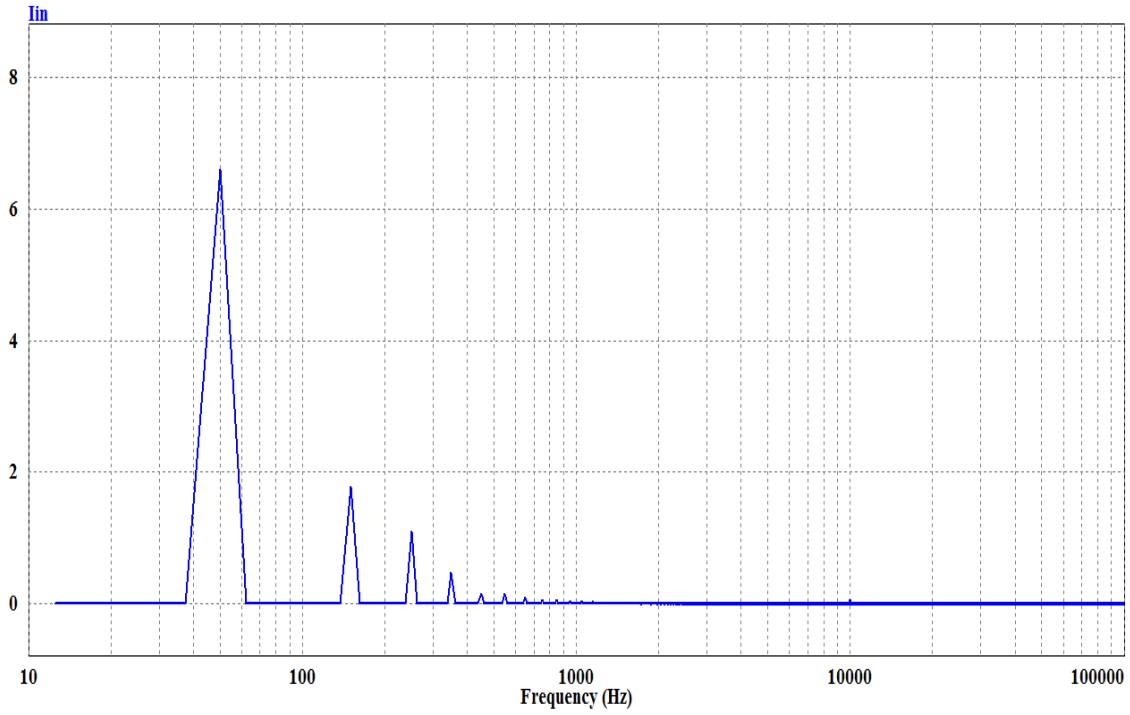


Fig.5.28 Input current spectrum of conventional Ĉuk converter at f_s = 10000 Hz. and D = 0.5

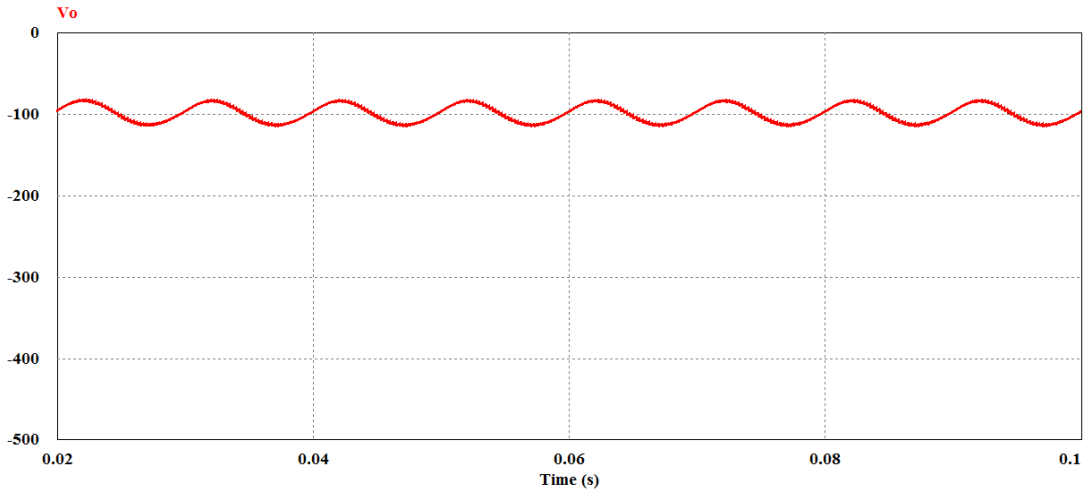


Fig.5.29 Output voltage waveform of proposed Ĉuk converter at f_s = 4000Hz. and D = 0.1

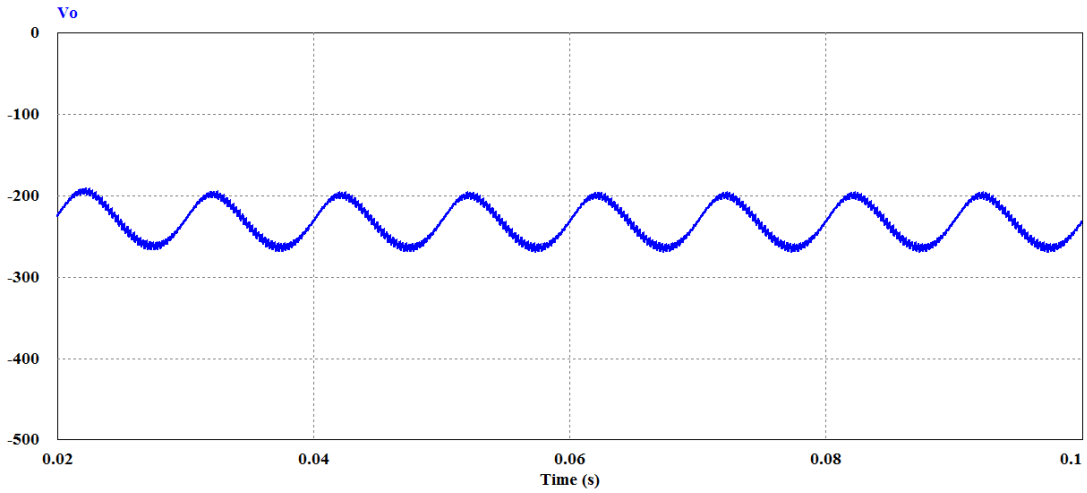


Fig.5.30 Output voltage waveform of proposed Ĉuk converter at f_s = 4000Hz. and D = 0.2

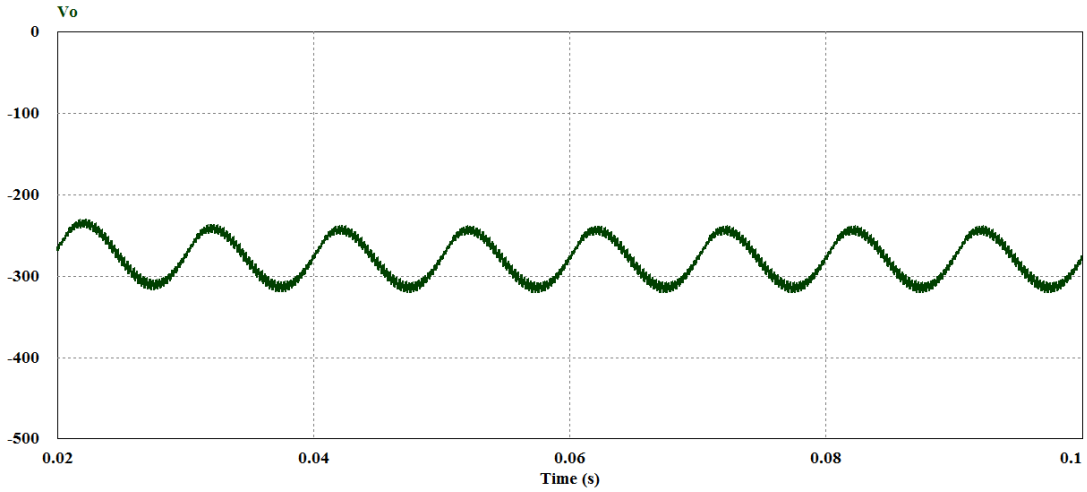


Fig.5.31 Output voltage waveform of proposed Ĉuk converter at f_s = 4000Hz. and D = 0.3

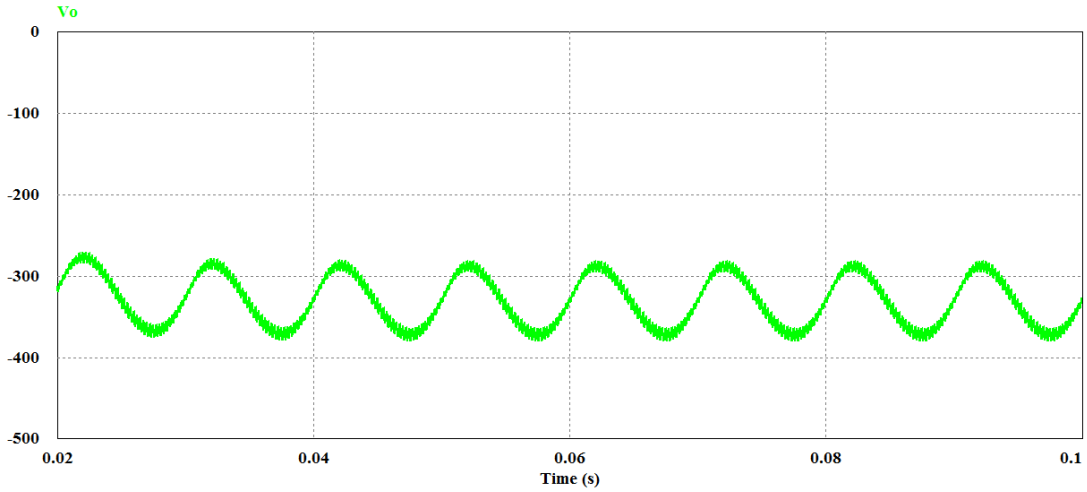


Fig.5.32 Output voltage waveform of proposed Ĉuk converter at f_s = 4000Hz. and D = 0.4

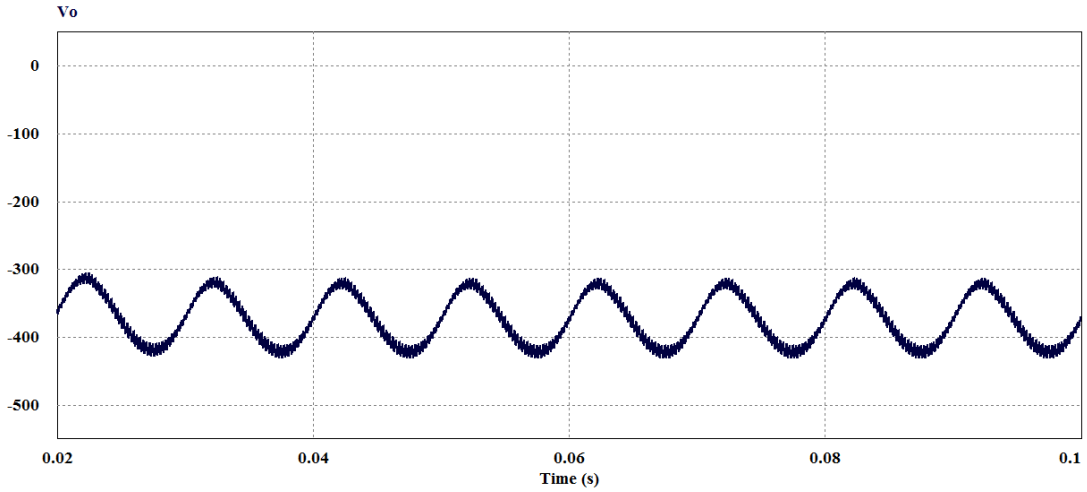


Fig.5.33 Output voltage waveform of proposed Ĉuk converter at f_s = 4000Hz. and D = 0.5

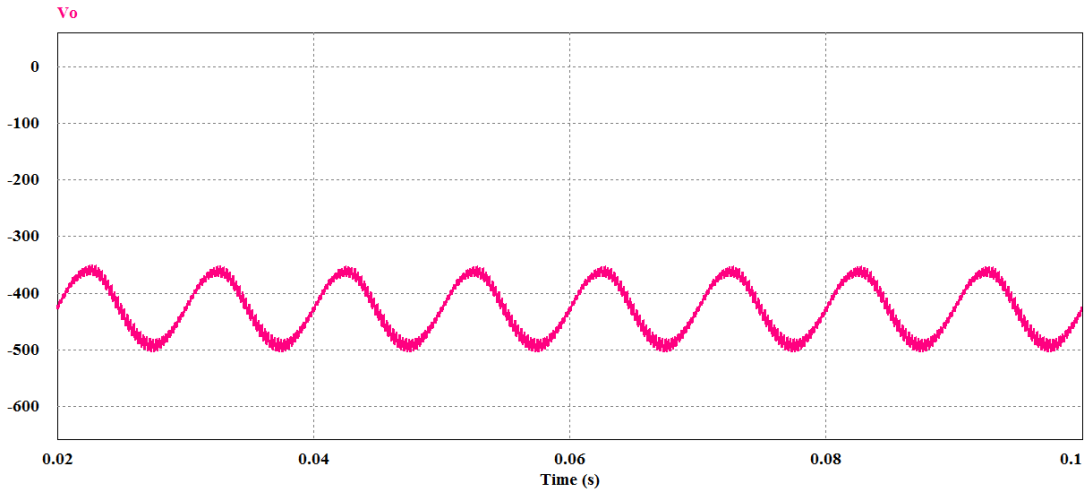


Fig.5.34 Output voltage waveform of proposed Ĉuk converter at f_s = 4000Hz. and D = 0.6

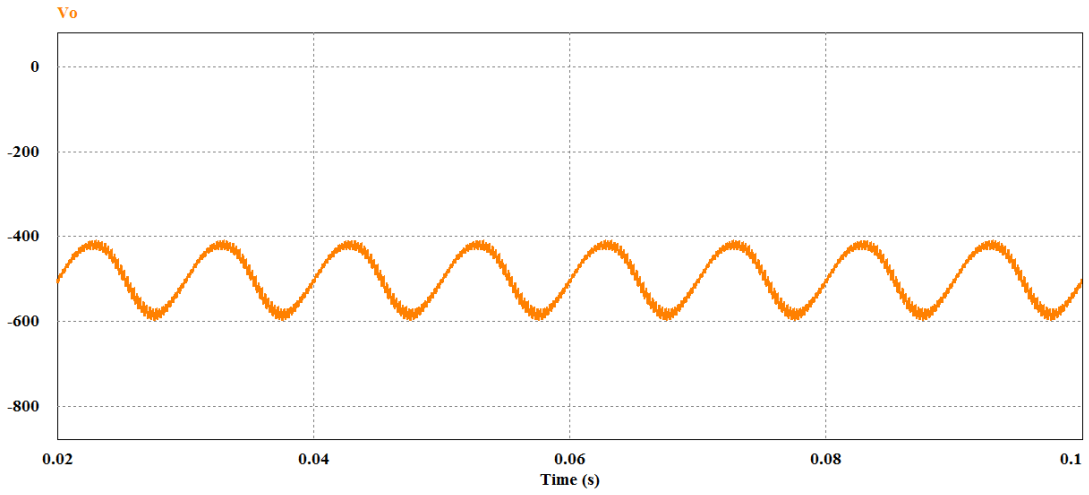


Fig.5.35 Output voltage waveform of proposed Ĉuk converter at f_s = 4000Hz. and D = 0.7

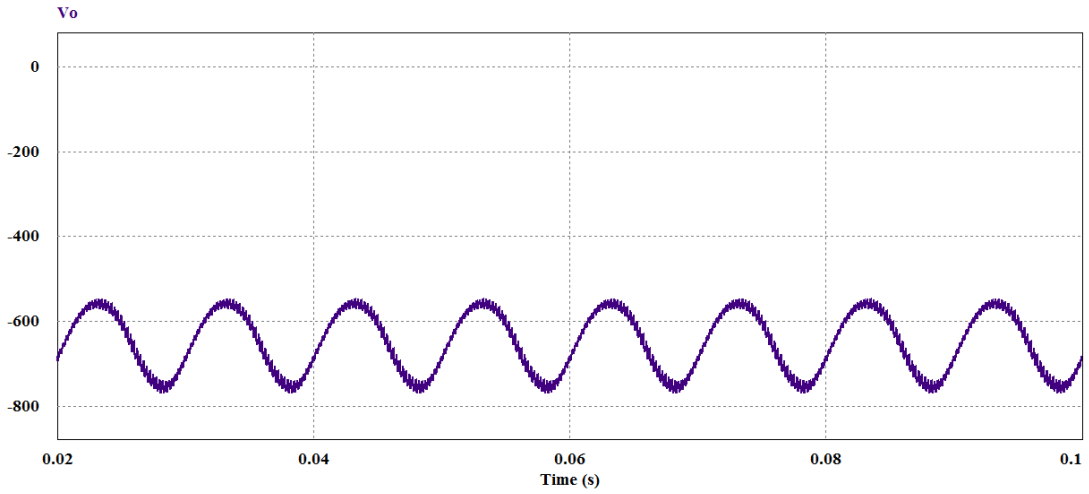


Fig.5.36 Output voltage waveform of proposed Ĉuk converter at f_s = 4000Hz. and D = 0.8

5.3.3 Quantitative Comparison

The performances of the proposed single phase Ĉuk AC-DC converter scheme is compared with conventional one having a Ĉuk DC-DC converter at the output as shown in Fig 5.3. For comparison, results are evaluated in terms of THD (%) of input current, input power factor and efficiency (%). The results of comparisons are presented in Figs. 5.37 to 5.51.

The bar chart shown in Figs. 5.37 to 5.41 indicates that the THD (%) of input current of the proposed converter is better than the conventional one for almost all duty cycles at different frequencies. The proposed converter also exhibits high input power factor at all duty cycles compared to conventional one which is presented in Figs 5.42 to 5.46. In terms of efficiency, the proposed Ĉuk converter has almost same efficiency as the conventional one which is presented in Figs. 5.47 to 5.51.

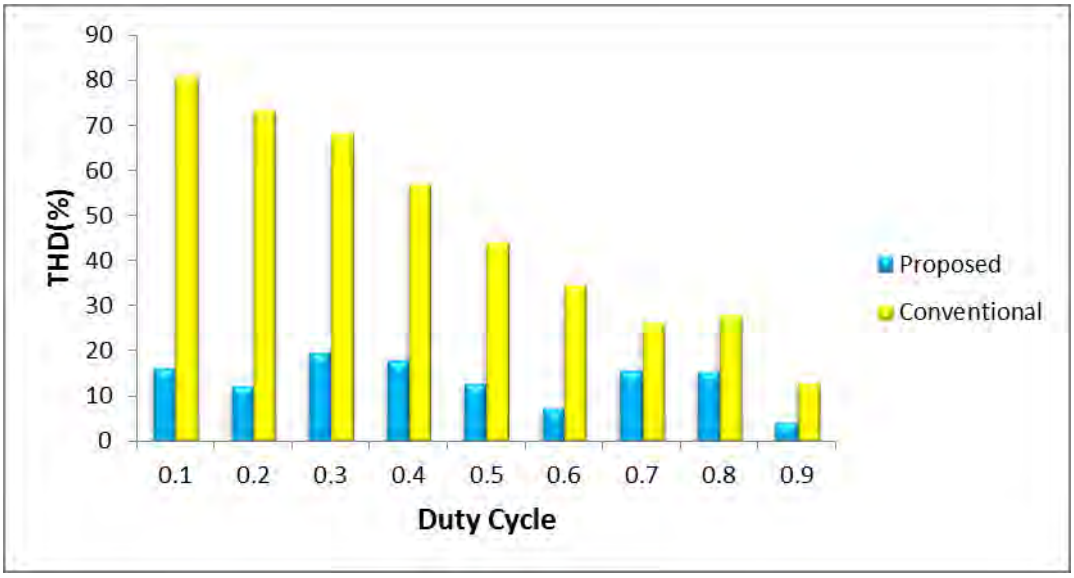


Fig. 5.37 Comparison of input current THD (%) between conventional and proposed scheme at f_s = 4000Hz. and R_Load = 100Ω.

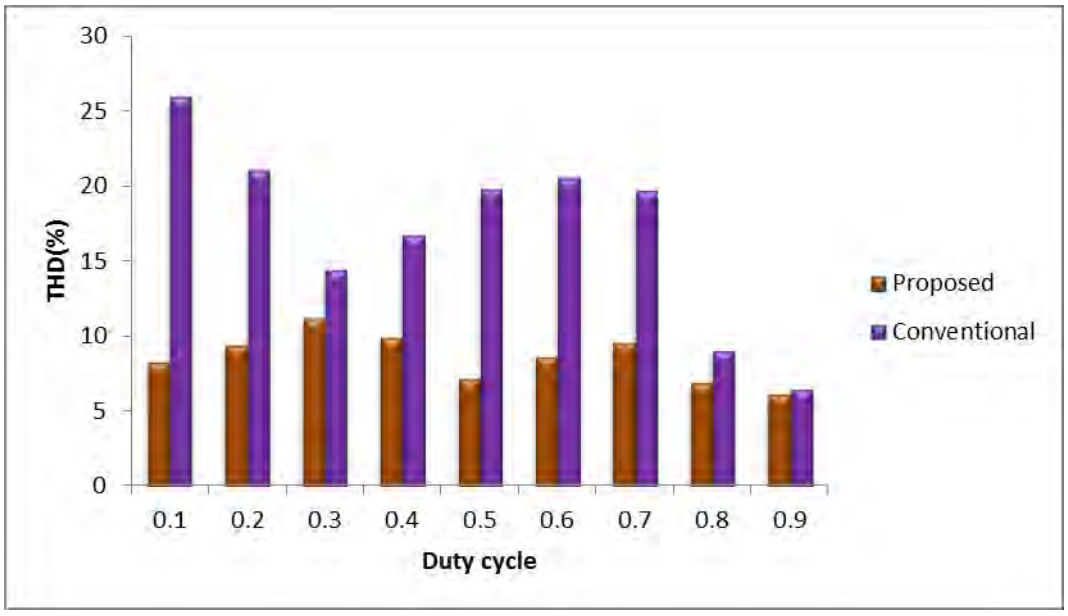


Fig.5.38. Comparison of input current THD (%) between conventional and proposed scheme at f_s = 6000Hz. and R_Load = 100Ω.

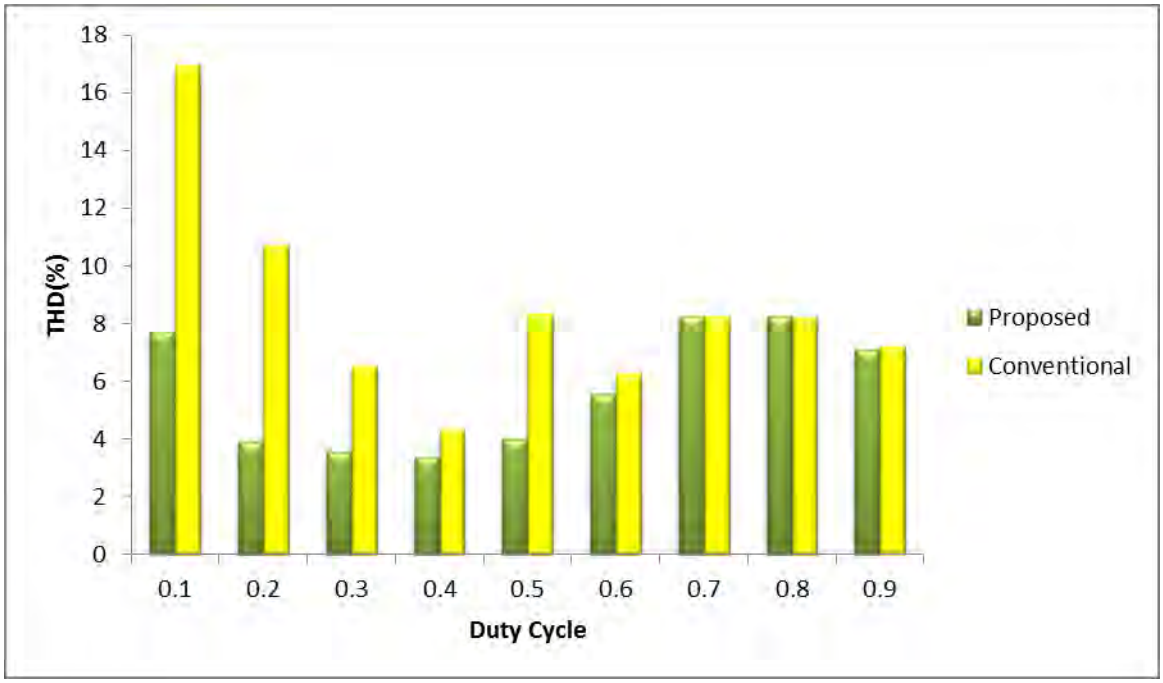


Fig. 5.39 Comparison of input current THD (%) between conventional and proposed scheme at f_s = 8000Hz. and R_Load = 100Ω.

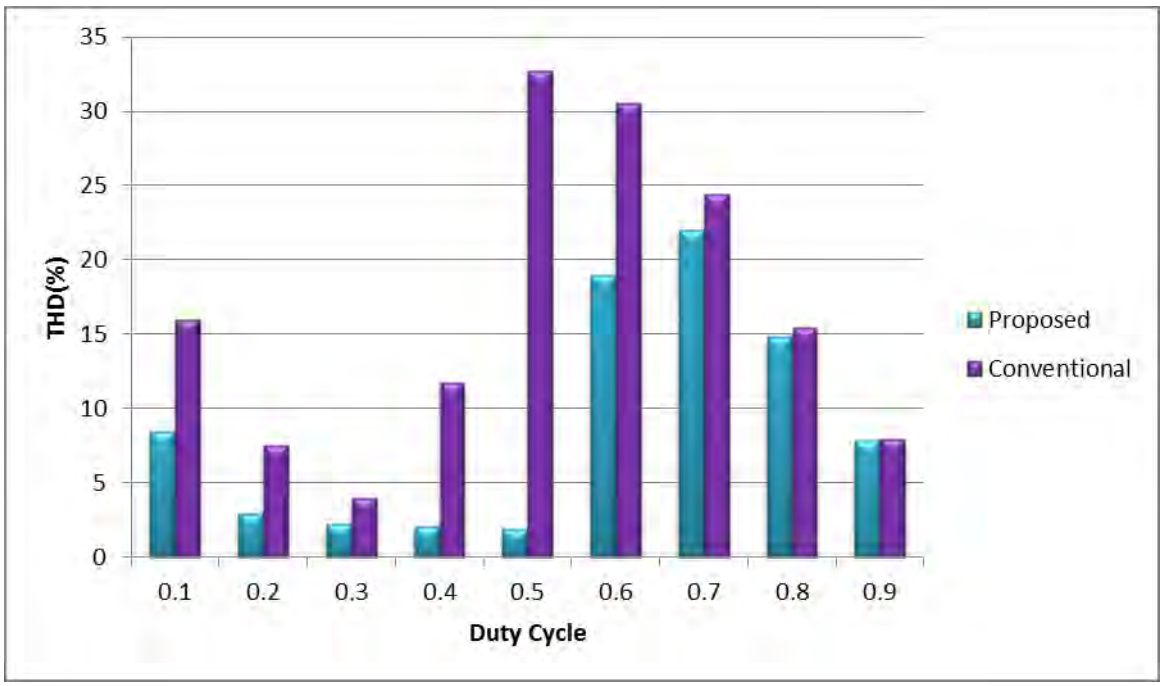


Fig. 5.40 Comparison of input current THD (%) between conventional and proposed scheme at f_s = 10000Hz. and R_Load = 100Ω.

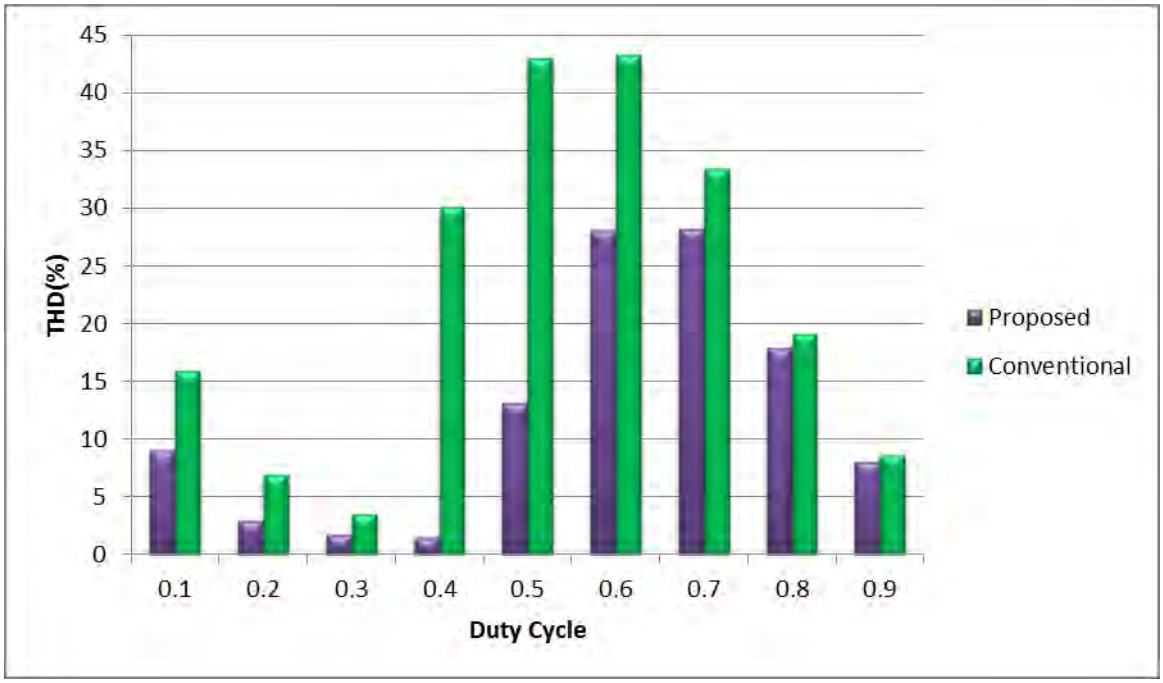


Fig. 5.41 Comparison of input current THD (%) between conventional and proposed scheme at f_s = 12000Hz. and R_Load = 100Ω.

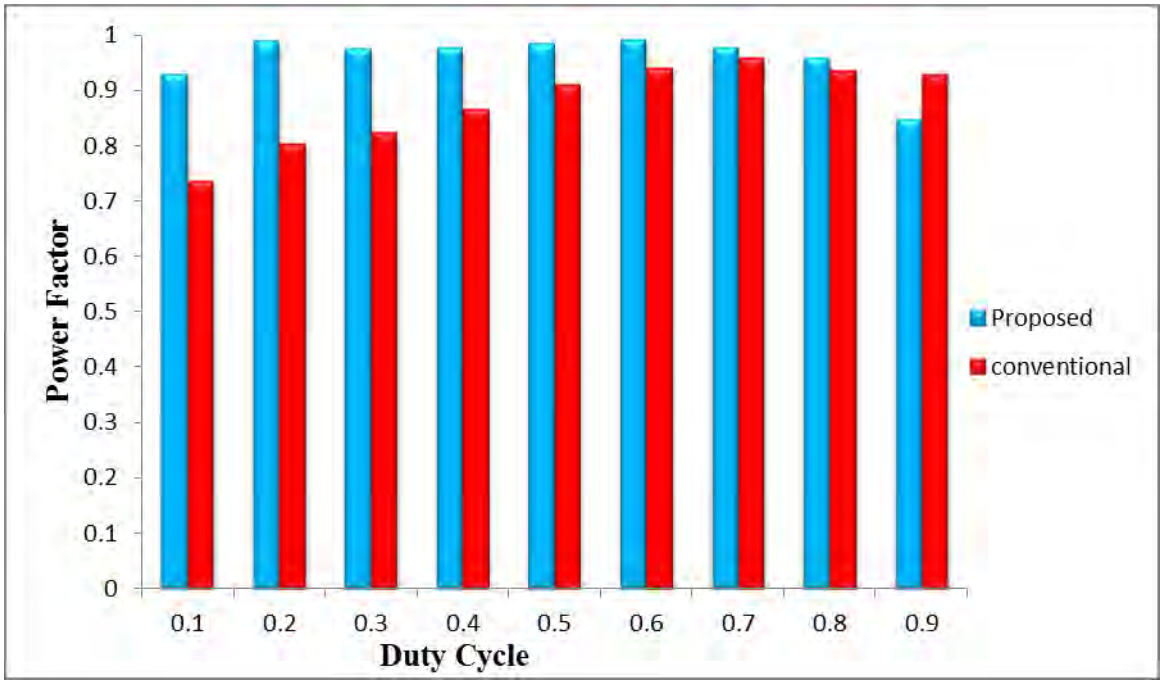


Fig. 5.42 Comparison of input power factor between conventional and proposed scheme at f_s = 4000Hz. and R_Load = 100 Ω.

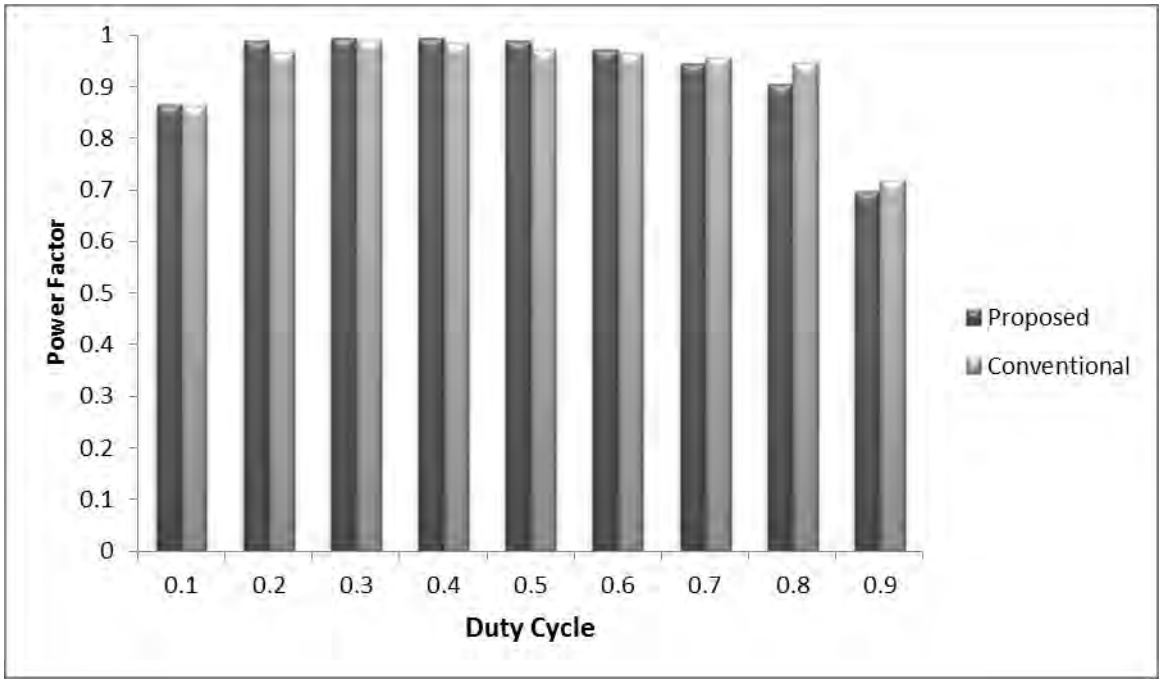


Fig. 5.43 Comparison of input power factor between conventional and proposed scheme at f_s = 6000Hz. and R_Load = 100 Ω.

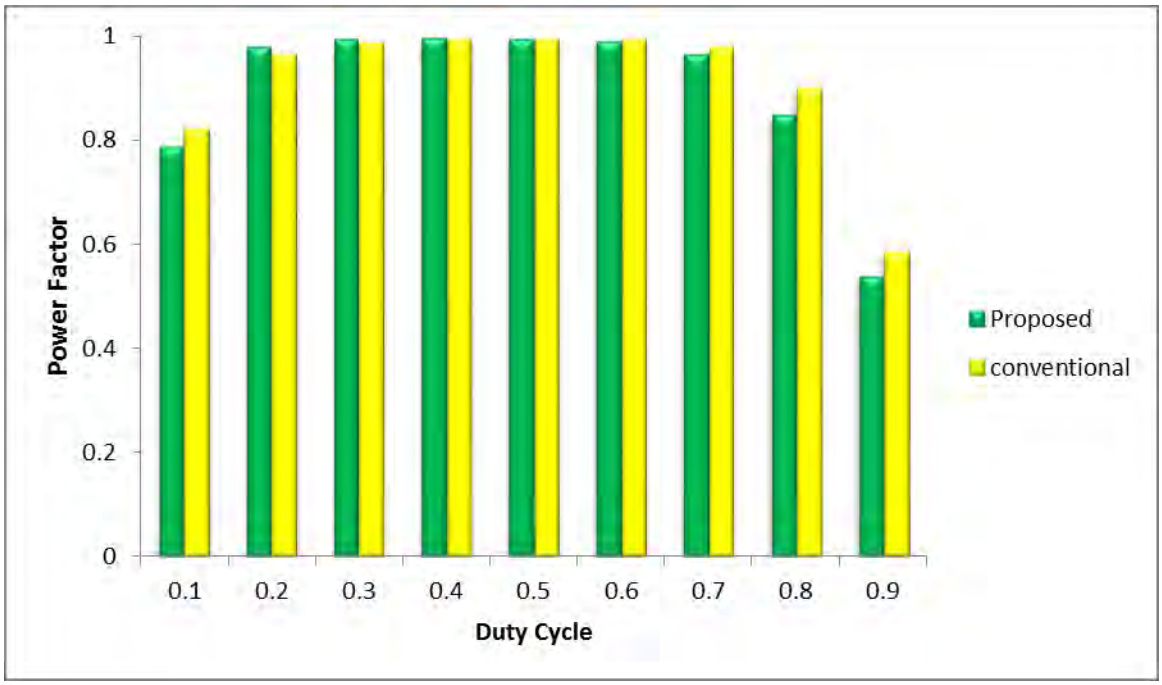


Fig. 5.44 Comparison of input power factor between conventional and proposed scheme at f_s = 8000Hz. and R_Load = 100 Ω.

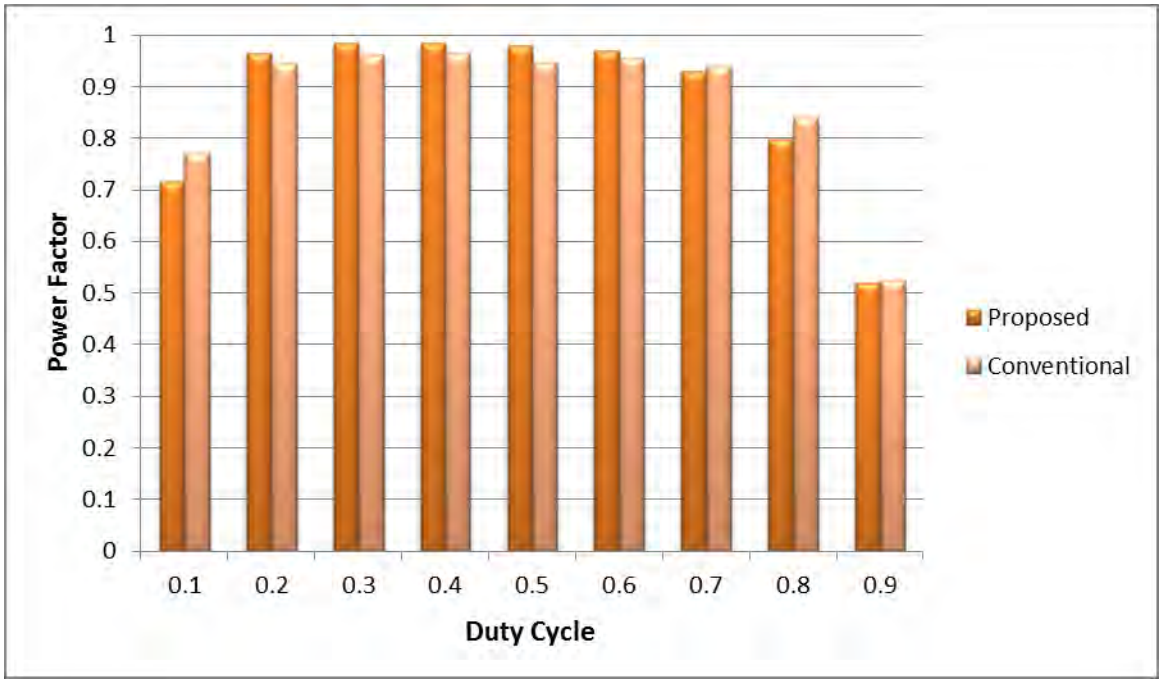


Fig. 5.45 Comparison of input power factor between conventional and proposed scheme at f_s = 10000Hz. and R_Load = 100 Ω.

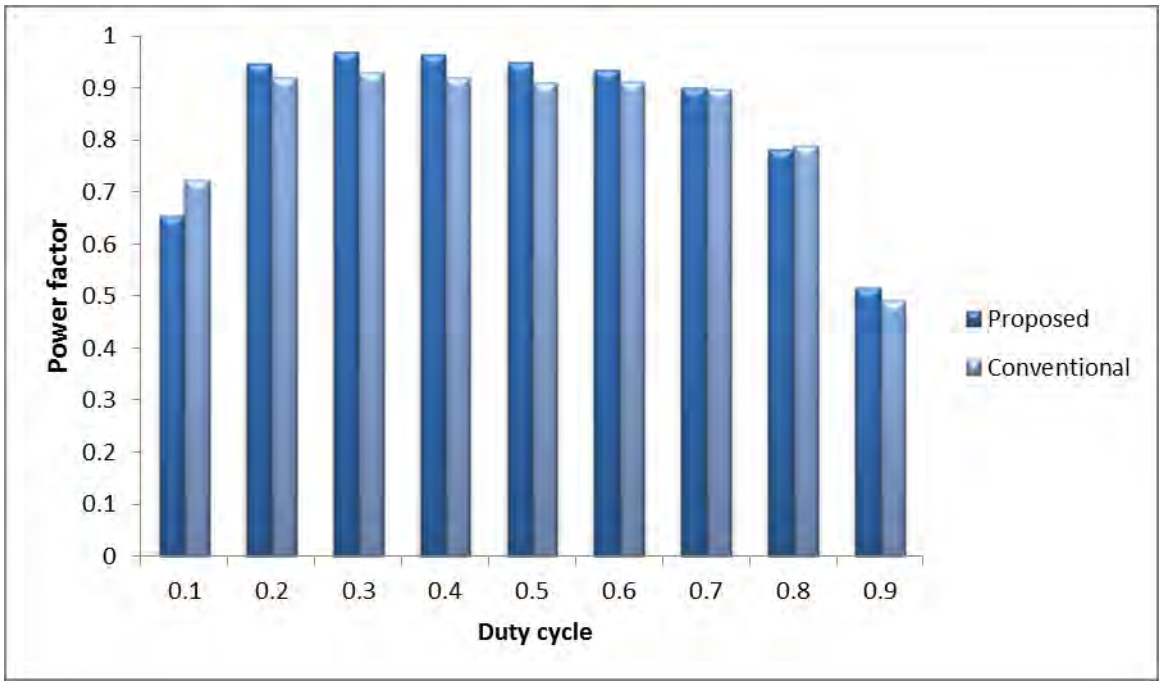


Fig. 5.46 Comparison of input power factor between conventional and proposed scheme at f_s = 12000Hz. and R_Load = 100 Ω.

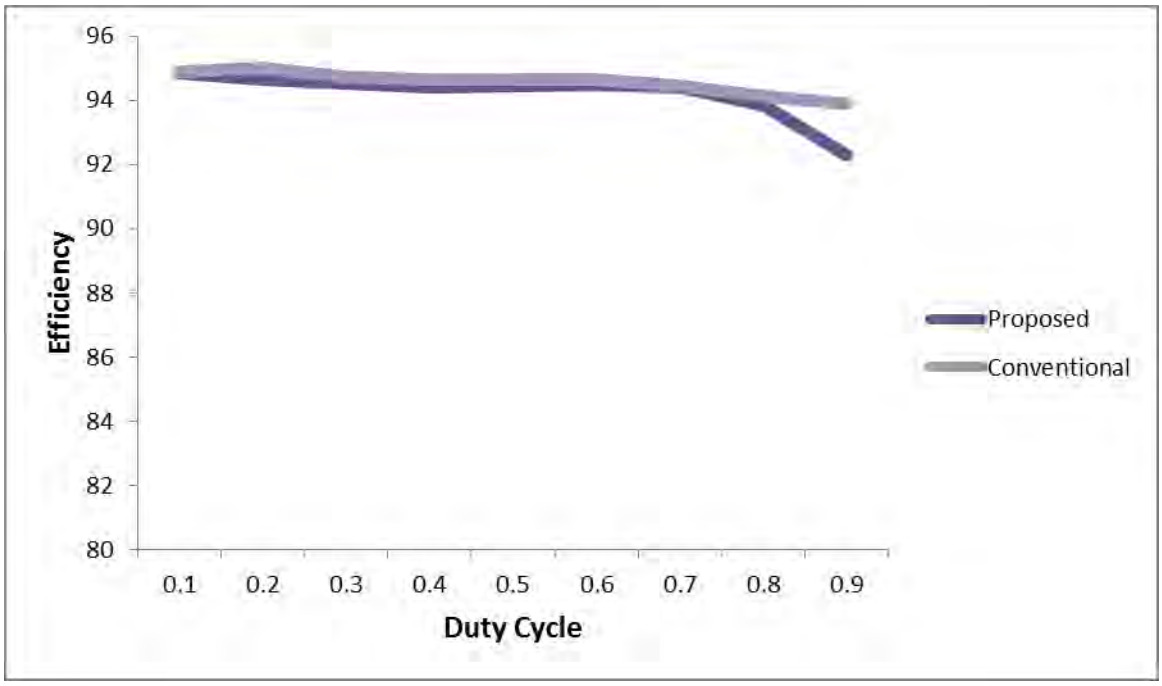


Fig. 5.47 Comparison of efficiency (%) between conventional and proposed scheme at f_s = 4000Hz. and R_Load = 100 Ω.

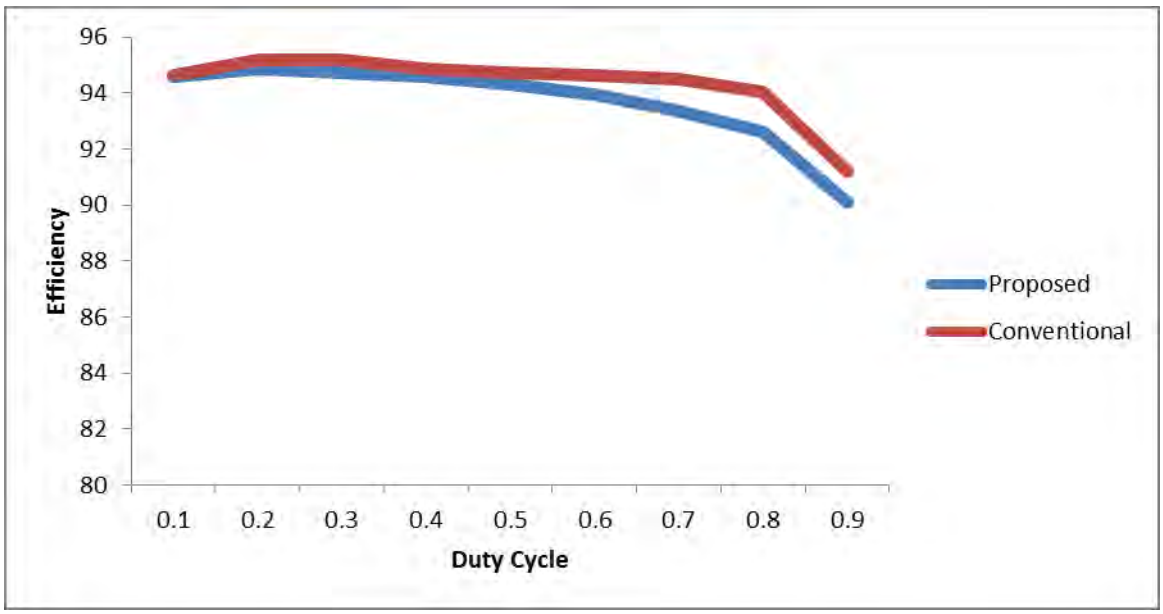


Fig. 5.48 Comparison of efficiency (%) between conventional and proposed scheme at f_s = 6000Hz. and R_Load = 100 Ω.

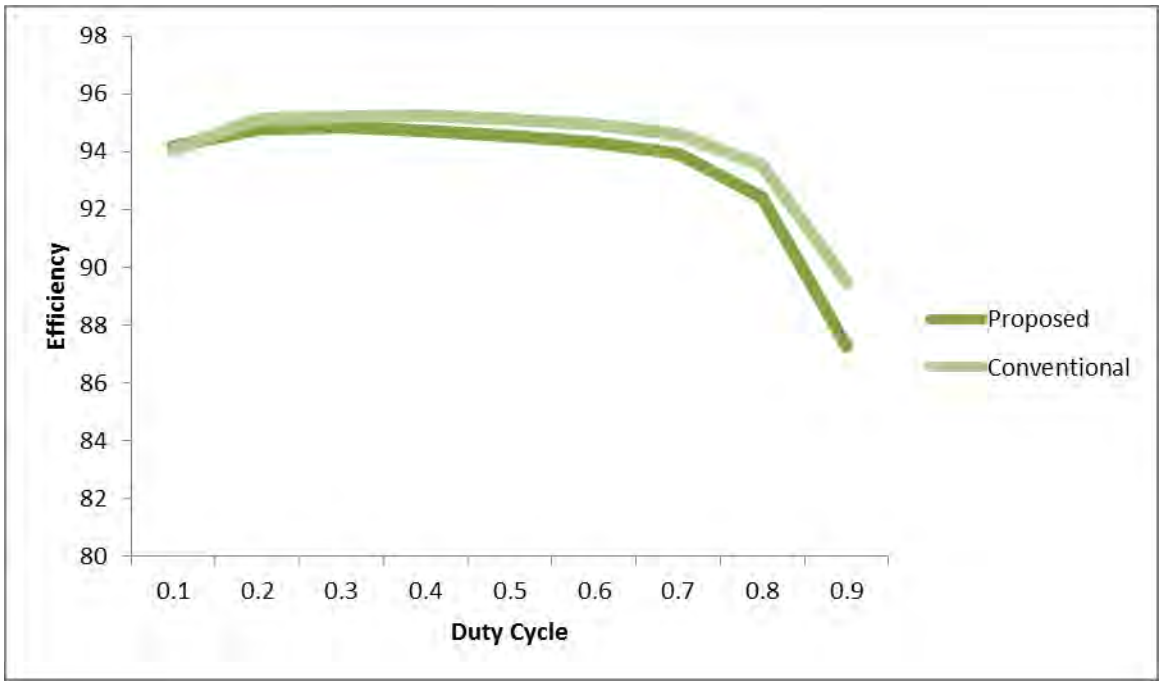


Fig. 5.49 Comparison of efficiency (%) between conventional and proposed scheme at f_s = 8000Hz. and R_Load = 100 Ω.

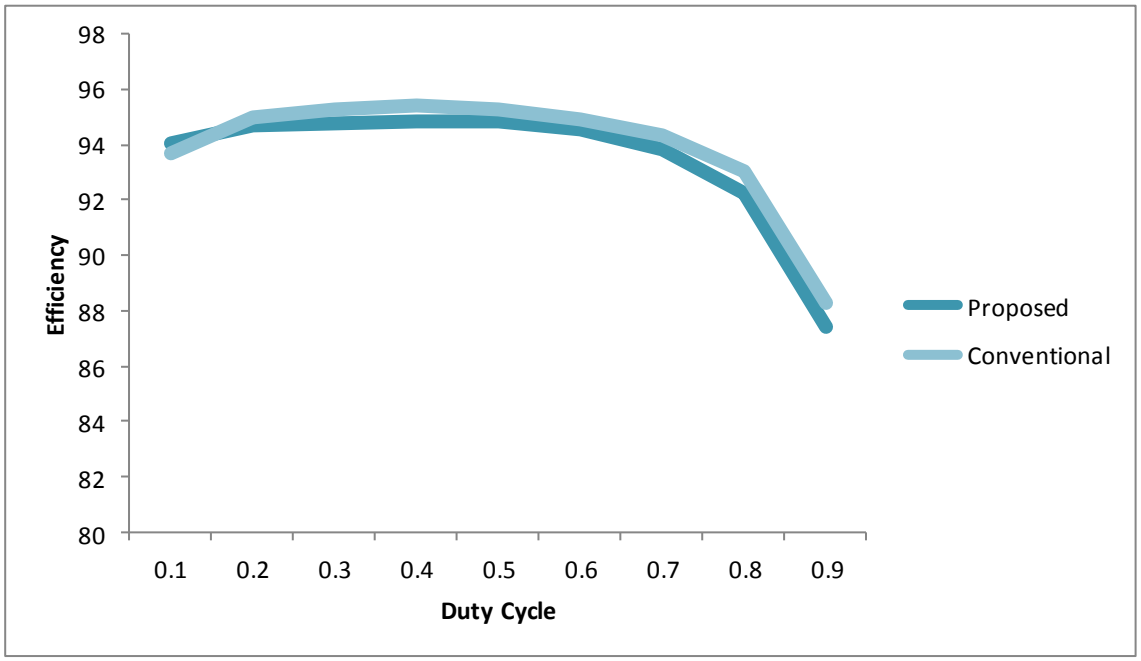


Fig. 5.50 Comparison of efficiency (%) between conventional and proposed scheme at f_s = 10000Hz. and R_Load = 100 Ω.

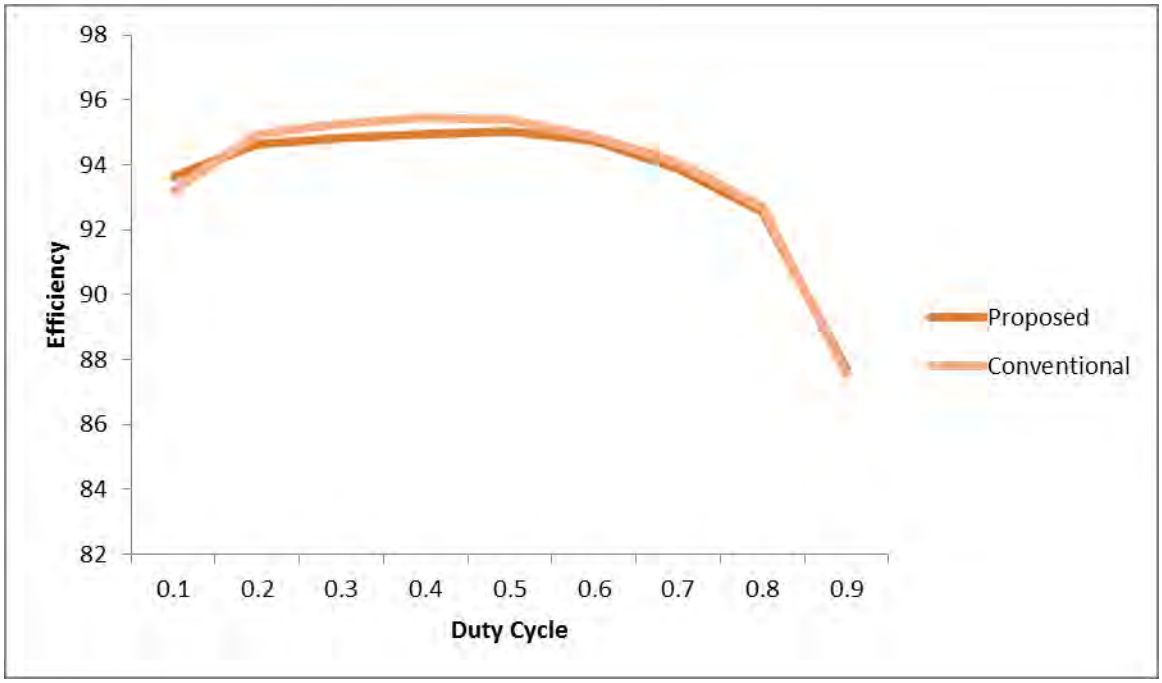


Fig. 5.51 Comparison of efficiency (%) between conventional and proposed scheme at f_s = 12000Hz. and R_Load = 100 Ω.

Numerical values of simulation data for input current THD (%), input current power factor, efficiency (%) and output power at frequency 4 to 12 KHz. for 0.1-0.9 duty cycles are given in Table 5.1.From this table it is observed that input current THD (%), input current power factor, efficiency (%) are in desirable limit.

Table 5.1 Numerical values of simulation data for proposed AC-DC Ĉuk converter

Frequency	Duty Cycle	Power Factor	Efficiency (%)	THD (%)	Average output Voltage	Output Power
4000 Hz.	**0.1**	0.931	94.86	16.3	95	92.88
	0.2	0.991	94.64	12.37	221	509.56
	0.3	0.977	94.53	19.7	265	727.05
	0.4	0.978	94.42	18.01	312	1018
	0.5	0.986	94.45	12.93	355	1315
	0.6	0.993	94.5	7.35	412	1766
	0.7	0.979	94.4	15.72	484	2438
	0.8	0.96	93.85	15.34	631	4150
	0.9	0.849	92.27	4.38	926	9015
5000 Hz.	**0.1**	0.896	94.62	11	82	69.35
	0.2	0.992	94.7	9.87	175	317.808
	0.3	0.987	94.56	13.4	289	867.138

	0.4	0.977	94.43	17.1	354	1306.6
	0.5	0.977	94.38	15.75	423	1859
	0.6	0.976	94.65	11.63	517	2785
	0.7	0.963	93.73	8.71	631	4152
	0.8	0.939	93.39	7.89	741	5727
	0.9	0.816	92.06	9.69	922	8929
6000 Hz.	**0.1**	0.864	94.6	8.26	75	58.33
	0.2	0.988	94.87	9.42	159	262.786
	0.3	0.993	94.74	11.2	249	644.416
	0.4	0.993	94.6	9.91	354	1305
	0.5	0.988	94.32	7.16	457	2179
	0.6	0.972	93.96	8.6	561	3286
	0.7	0.945	93.37	9.58	688	4936
	0.8	0.904	92.6	6.88	845	7465
	0.9	0.697	90.1	6.17	998	10461.3
7000 Hz.	**0.1**	0.527	94.54	7.82	69	49.853
	0.2	0.986	94.88	5.34	146	221.288
	0.3	0.997	94.88	6.19	241	603.679
	0.4	0.996	94.66	7.52	342	1211
	0.5	0.991	94.46	7.4	453	2134
	0.6	0.979	94.12	4.76	561	3272
	0.7	0.961	93.79	4.98	679	4796
	0.8	0.886	92.68	3.29	879	8074
	0.9	0.601	88.15	6.34	1015	10825
8000 Hz.	**0.1**	0.789	94.2	7.75	65	43.431
	0.2	0.981	94.75	3.93	135	188.164
	0.3	0.995	94.84	3.55	218	496.362
	0.4	0.998	94.73	3.38	320	1061
	0.5	0.996	94.53	4.01	427	1892
	0.6	0.989	94.34	5.57	543	3076
	0.7	0.965	93.91	8.28	695	5047
	0.8	0.849	92.41	8.27	885	8186
	0.9	0.54	87.25	7.1	981	10104
9000 Hz.	**0.1**	0.752	94.29	8.12	61	38.549
	0.2	0.974	94.82	3.31	126	164.084
	0.3	0.991	94.9	2.77	200	413.827
	0.4	0.993	94.88	2.54	288	856.43
	0.5	0.993	94.79	2.43	390	1574
	0.6	0.985	94.5	11.9	527	2892
	0.7	0.947	93.88	16.74	699	5094

	0.8	0.814	92.27	12.35	875	8003
	0.9	0.521	87.15	7.71	965	9772
10000 Hz.	**0.1**	0.716	94.05	8.43	58	34.65
	0.2	0.965	94.7	2.96	119	145.55
	0.3	0.985	94.79	2.26	187	359.13
	0.4	0.9853	94.84	2.05	265	722.95
	0.5	0.98	94.855	1.87	354	1290
	0.6	0.969	94.53	19.01	503	2620
	0.7	0.929	93.83	22	683	4870
	0.8	0.798	92.27	14.85	863	7770
	0.9	0.52	87.44	7.87	959	9670
11000 Hz.	**0.1**	0.683	93.96	8.61	55	31.5
	0.2	0.957	94.74	2.85	113	131.1
	0.3	0.978	94.87	1.91	176	318.74
	0.4	0.975	94.95	1.74	247	630.24
	0.5	0.966	95.02	6.26	334	1150
	0.6	0.953	94.69	23.95	481	2410
	0.7	0.915	93.88	25.44	663	4590
	0.8	0.791	92.45	16.52	848	7510
	0.9	0.518	87.61	7.95	953	9560
12000 Hz.	**0.1**	0.653	93.63	9.04	53	28.88
	0.2	0.948	94.65	2.88	108	119.27
	0.3	0.97	94.83	1.69	167	286.95
	0.4	0.964	94.95	1.5	233	560.58
	0.5	0.949	95.04	13.12	321	1070
	0.6	0.936	94.74	28.14	466	2270
	0.7	0.901	93.88	28.15	647	4390
	0.8	0.782	92.53	17.86	835	7310
	0.9	0.516	87.74	8.02	948	9470

5.3.4. Performances under Load Variation

The proposed and conventional both circuits are subjected to load variation at frequency 8 KHz. and 40 % duty cycle. The load resistance was varied from 50Ω to 500Ω and the performance was monitored in terms of input power factor and input current THD (%).

The comparisons of input current THD (%) ,input power factor and efficiency between the proposed and the conventional converter are presented in Figs. 5.52 to Fig. 5.54. The proposed converter gives low input current THD (%) with respect to the conventional circuit.

The proposed circuit also has higher power factor than the conventional single-phase rectifier for all load resistance. The efficiency of the proposed converter is also high in almost all duty cycles. Fig. 5.55 presents Output Voltage of the proposed converter at 8000Hz. D = 0.4 for different load resistance. The output voltage reduces with increasing of load.

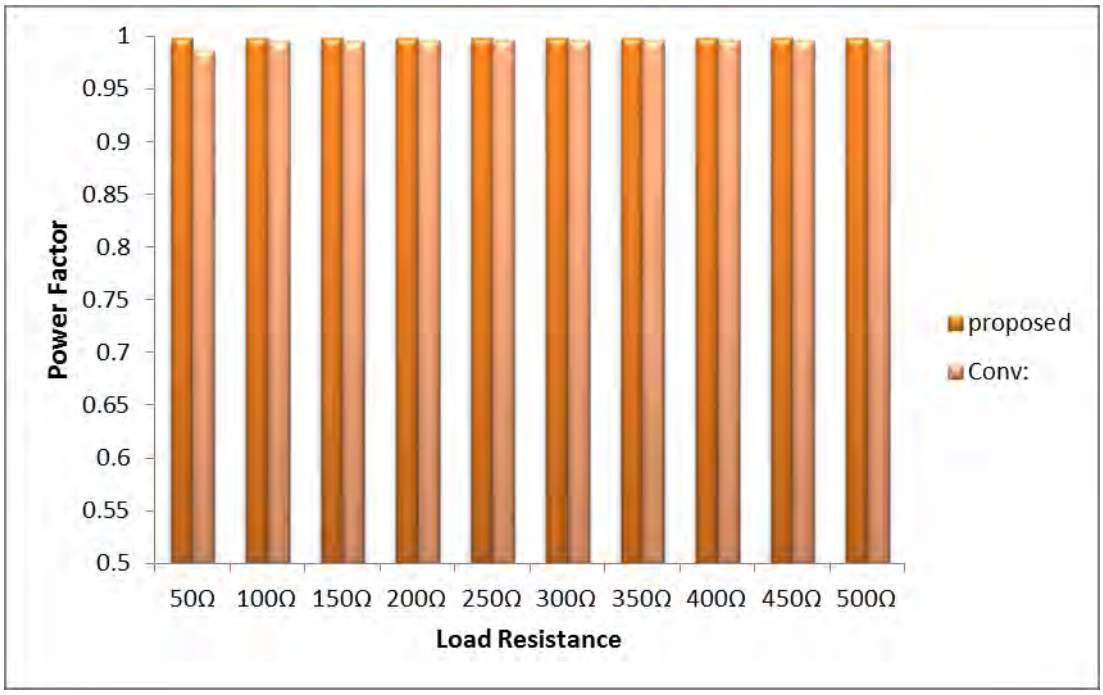


Fig. 5.52 Comparison of input power factor between conventional and proposed scheme with load variation at f_s = 8000Hz. and D = 0.4.

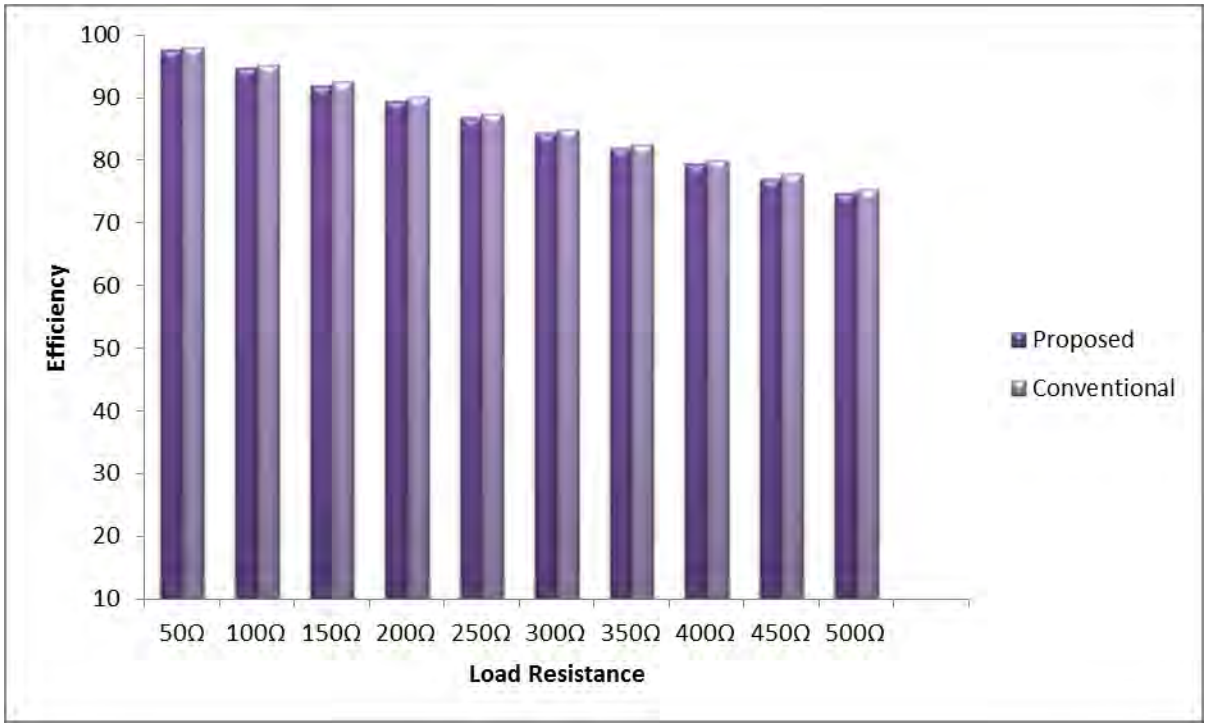


Fig. 5.53 Comparison of efficiency between conventional and proposed scheme with load variation at f_s = 8000Hz. and D = 0.4

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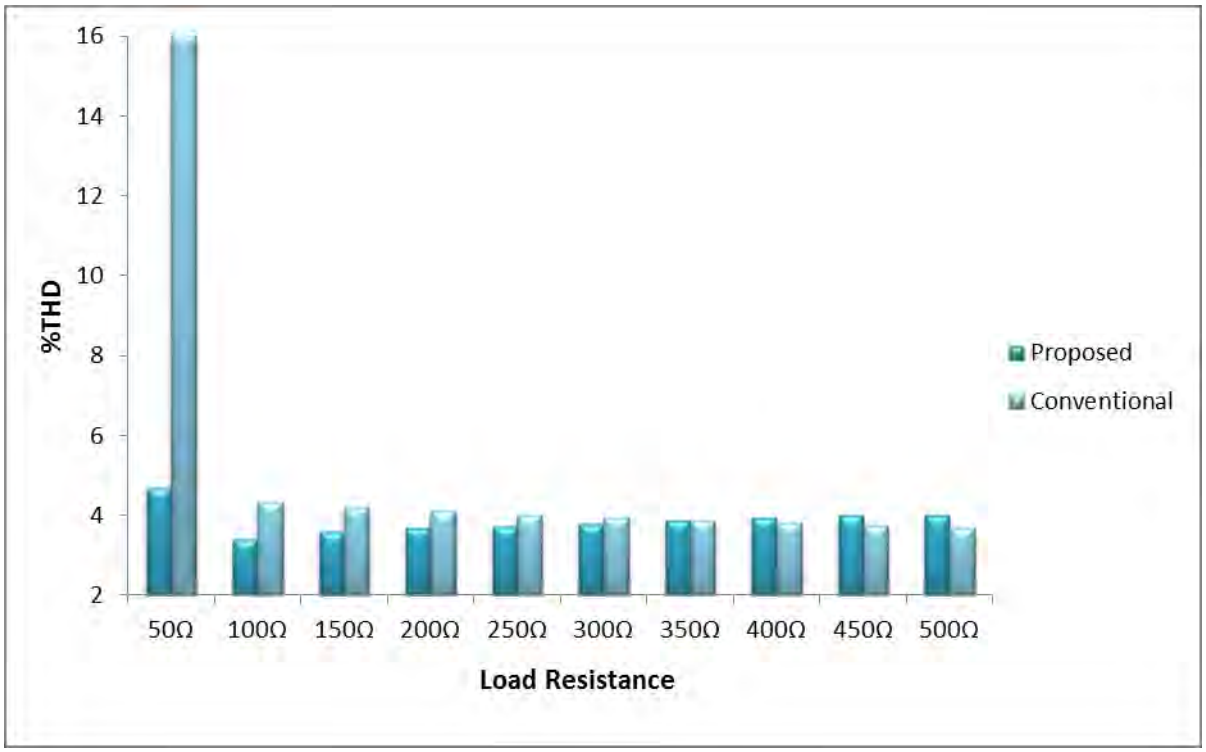


Fig. 5.54 Comparison of input current THD (%) between conventional and proposed scheme with load variation at f_s = 8000Hz. and D = 0.4

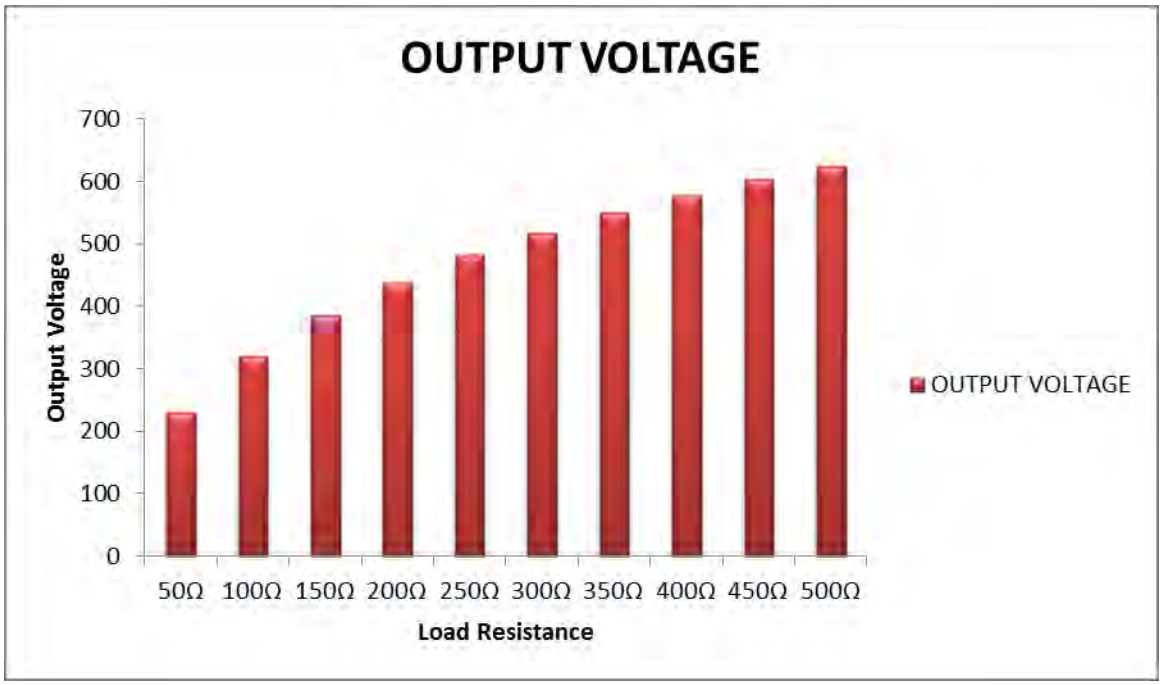


Fig. 5.55 Output Voltage of the proposed converter at f_s = 8000Hz. and D = 0.4

5.4 The Proposed Ĉuk Converter with Feedback Controller Circuit

It is observed in Fig. 5.55 that, the output voltage of the proposed Ĉuk converter is changed with changing load values. For light load the output voltage is higher and for heavy loads the output voltage decreases. This is not a desirable characteristic for high power application.

High power applications need regulated voltage under the variation of other parameters like load value. That's why feedback controller circuit is introduced to regulate the output voltage and to maintain good power factor and THD under the condition of load variation. Fig. 5.56 represents the block diagram of the total system which consists of the proposed converter with voltage and current controller at feedback path.

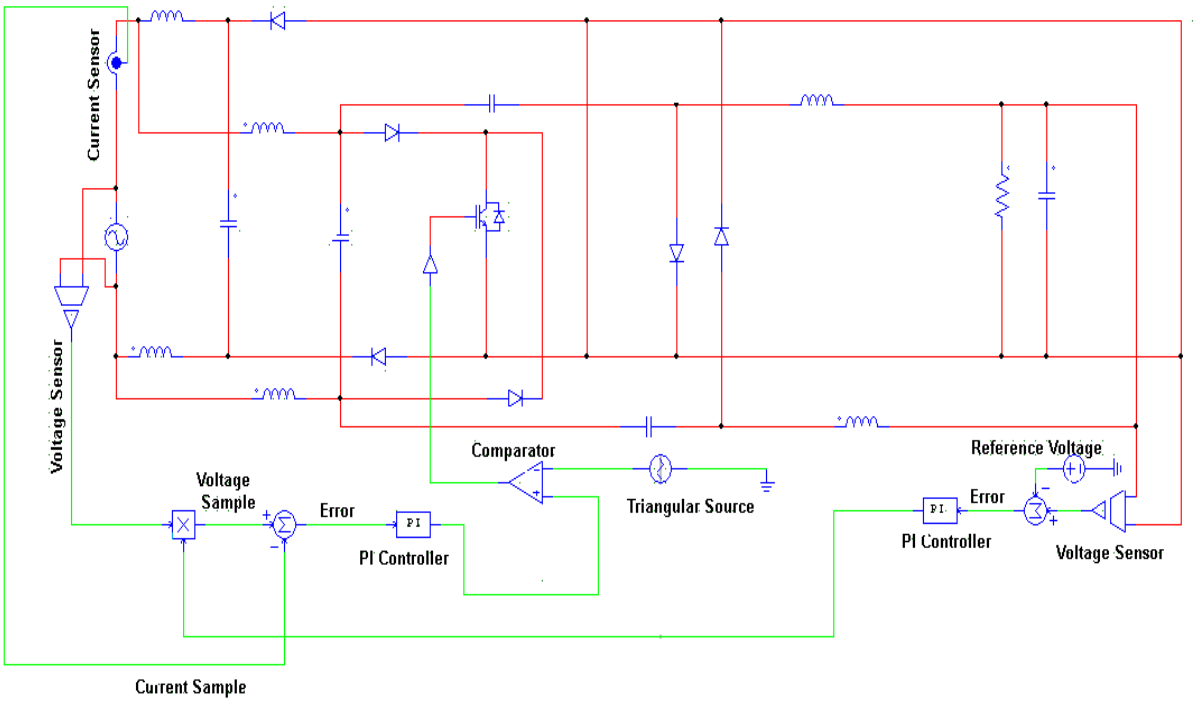


Fig. 5.56 The Proposed Ĉuk Converter with Feedback Controller Circuit.

Figs. 5.57 to 5.66 represent the waveform of input current and regulated output voltage for different load values. From the figures it is observed that the input current is nearly sinusoidal and the output voltage is also constant although load is changed.

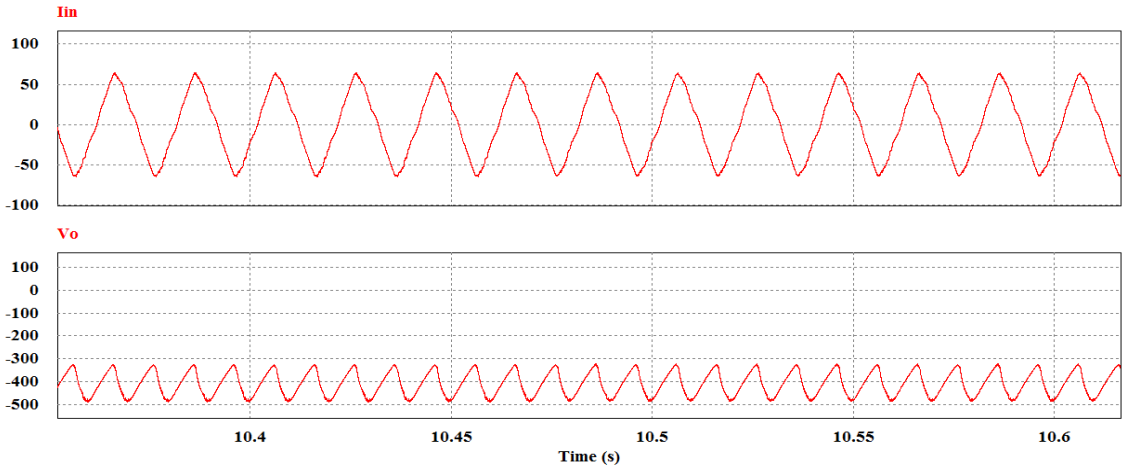


Fig.5.57 Input current and output voltage of proposed ĉuk converter with feedback controller for load resistance of 30 Ω

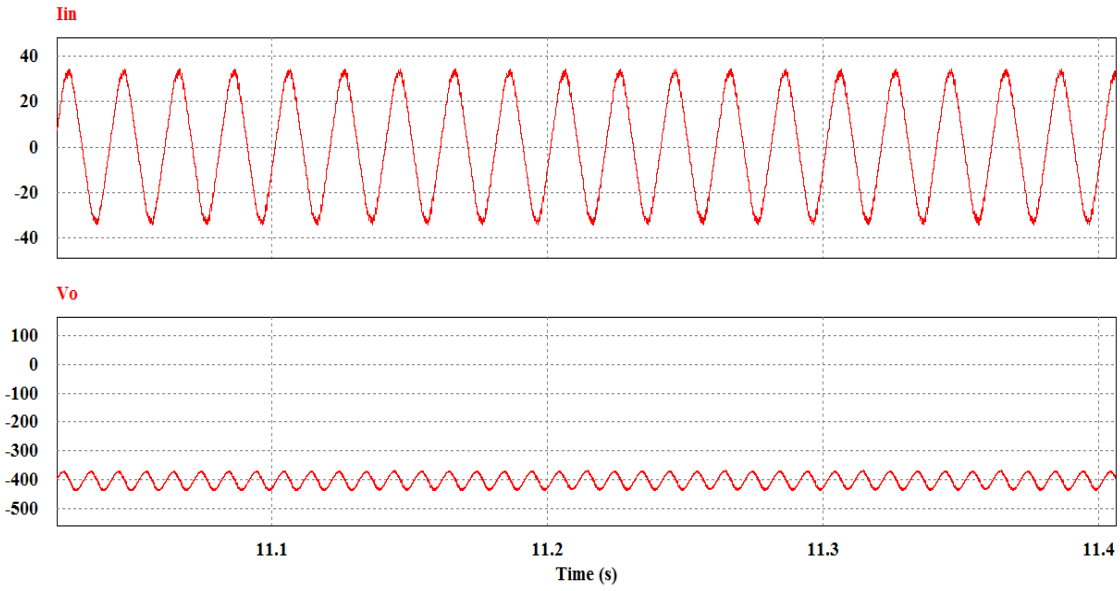


Fig.5.58 Input current and output voltage of proposed ĉuk converter with feedback controller for load resistance of 50 Ω

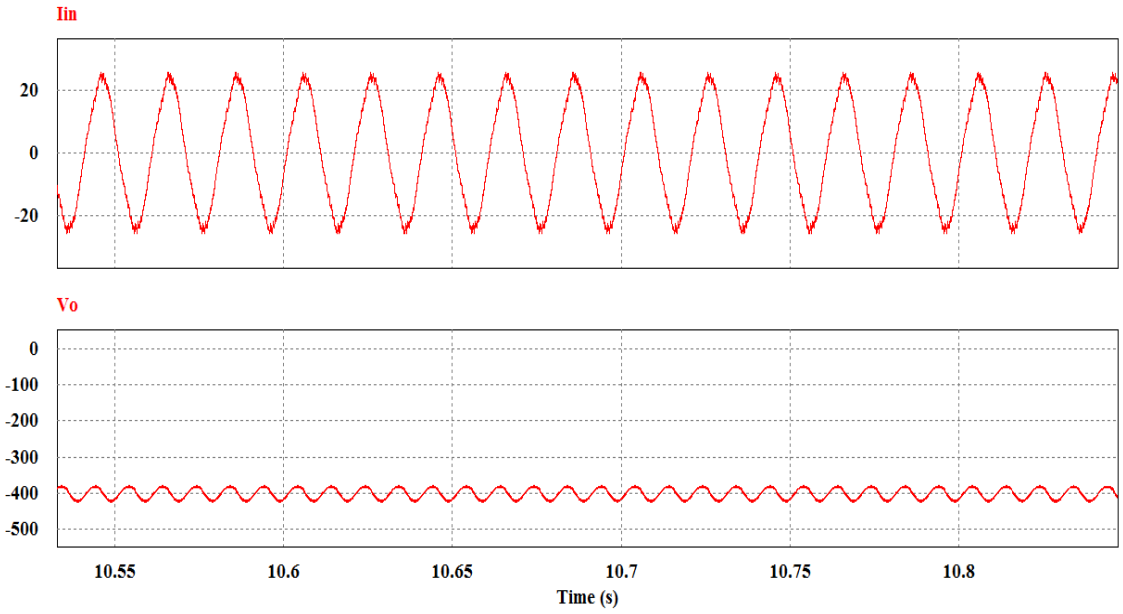


Fig.5.59 Input current and output voltage of proposed ĉuk converter with feedback controller for load resistance of 70 Ω

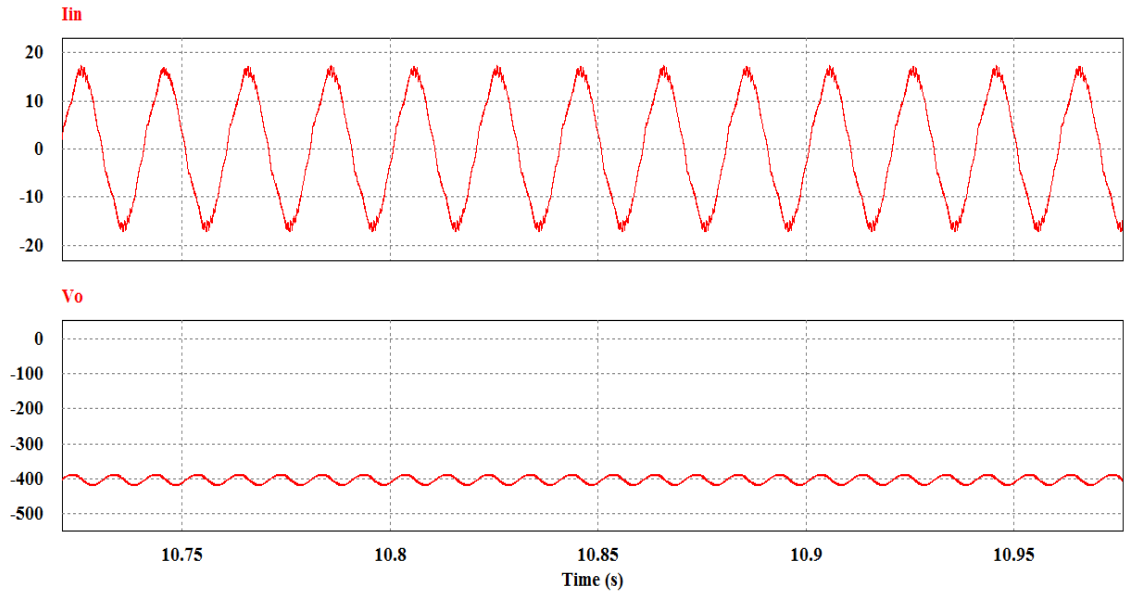


Fig.5.60 Input current and output voltage of proposed ĉuk converter with feedback controller for load resistance of 100 Ω

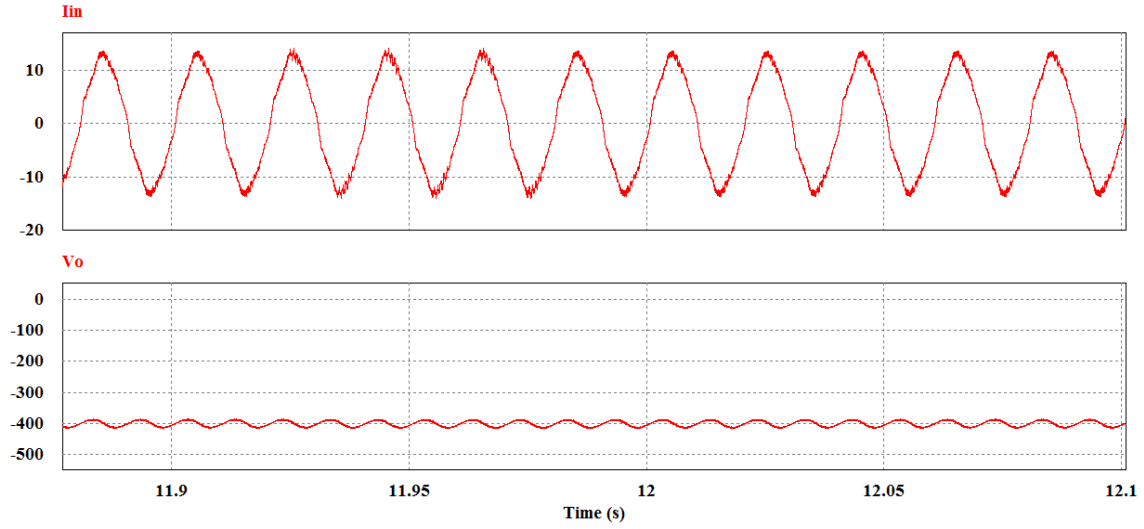


Fig.5.61 Input current and output voltage of proposed ĉuk converter with feedback controller for load resistance of 120 Ω

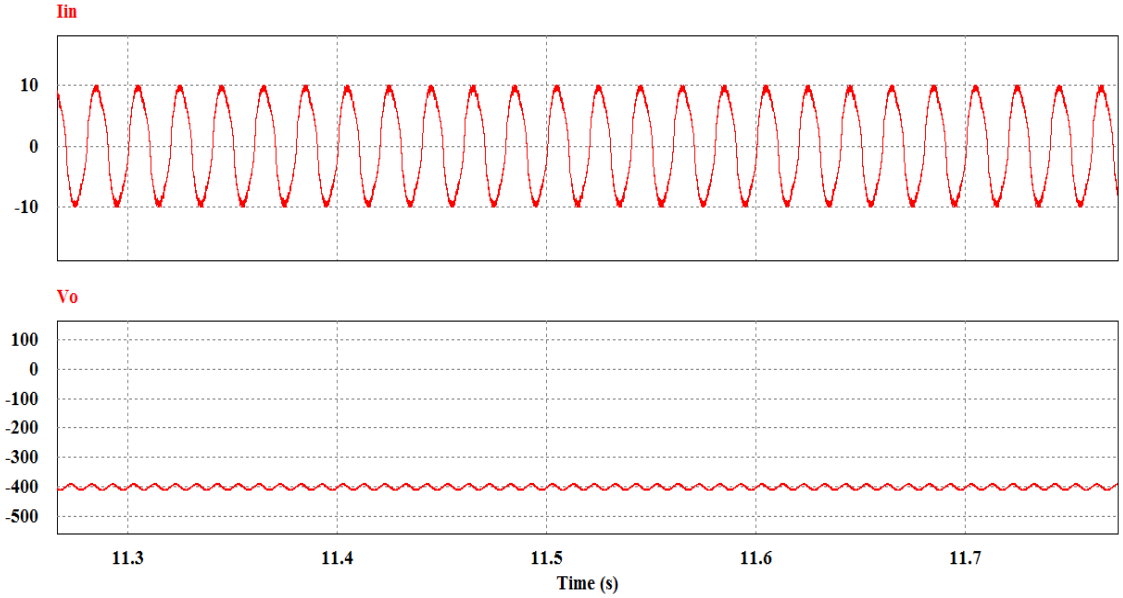


Fig.5.62 Input current and output voltage of proposed ĉuk converter with feedback controller for load resistance of 150 Ω

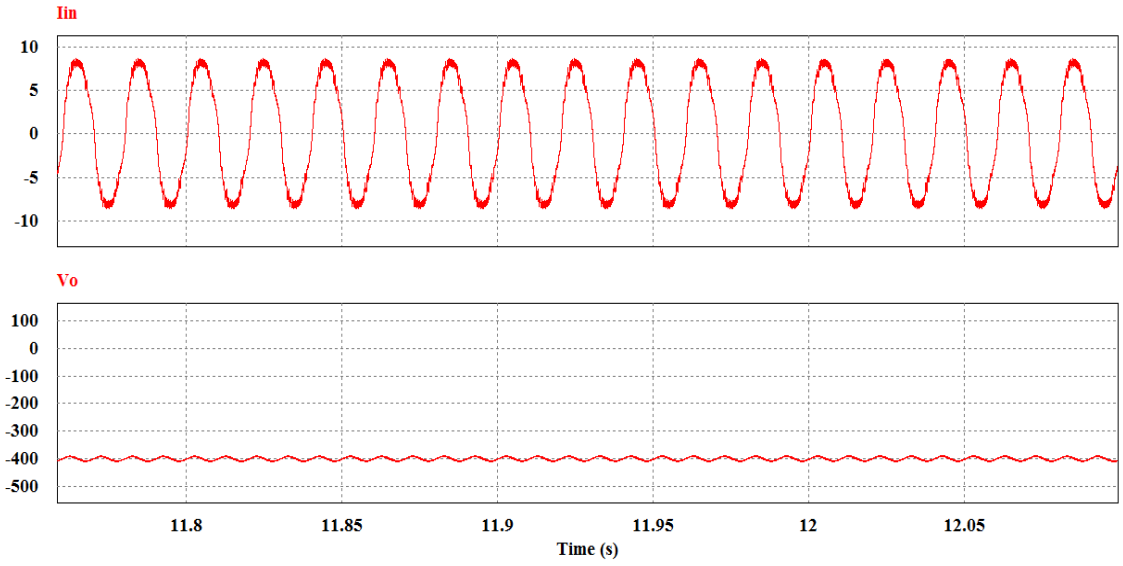


Fig.5.63 Input current and output voltage of proposed ĉuk converter with feedback controller for load resistance of 170 Ω

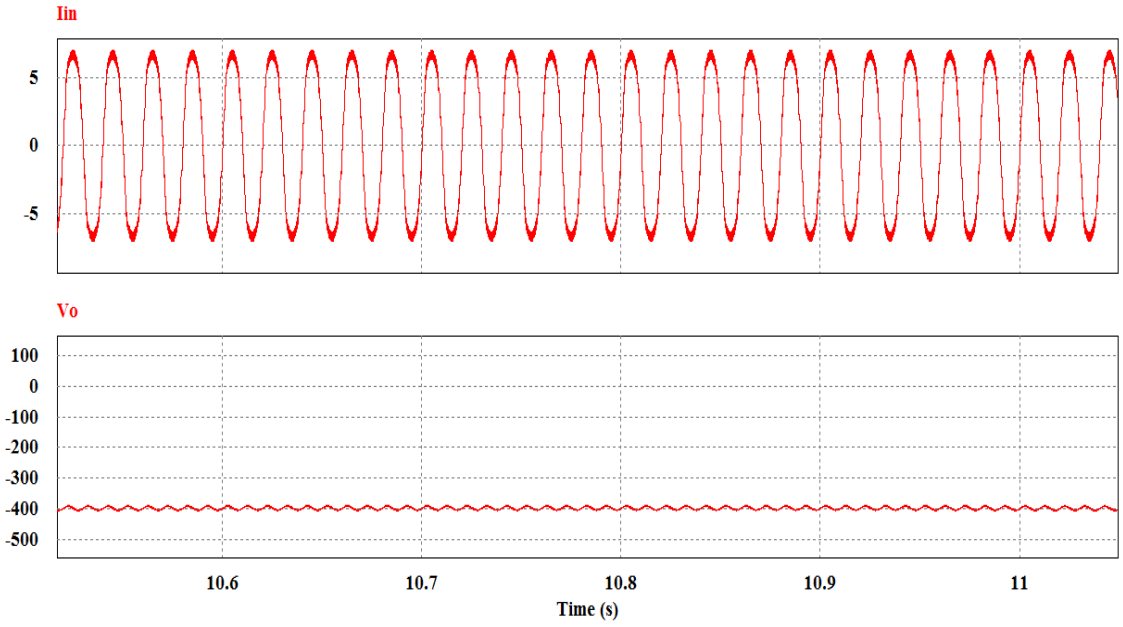


Fig.5.64 Input current and output voltage of proposed ĉuk converter with feedback controller for load resistance of 200 Ω

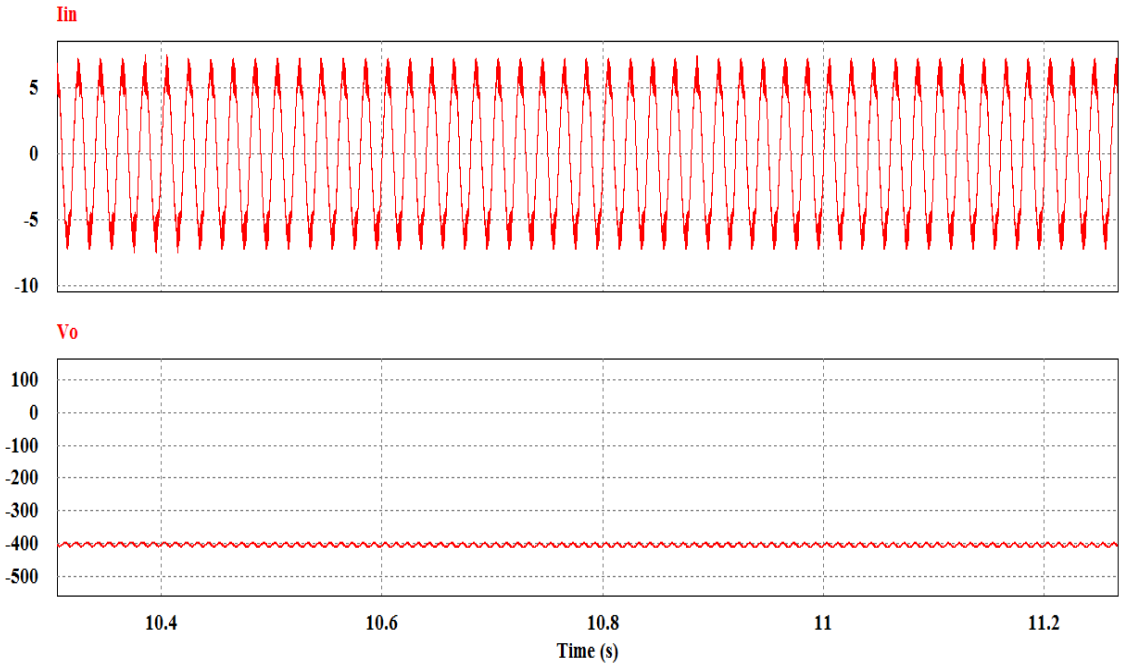


Fig.5.65 Input current and output voltage of proposed ĉuk converter with feedback controller for load resistance of 230 Ω

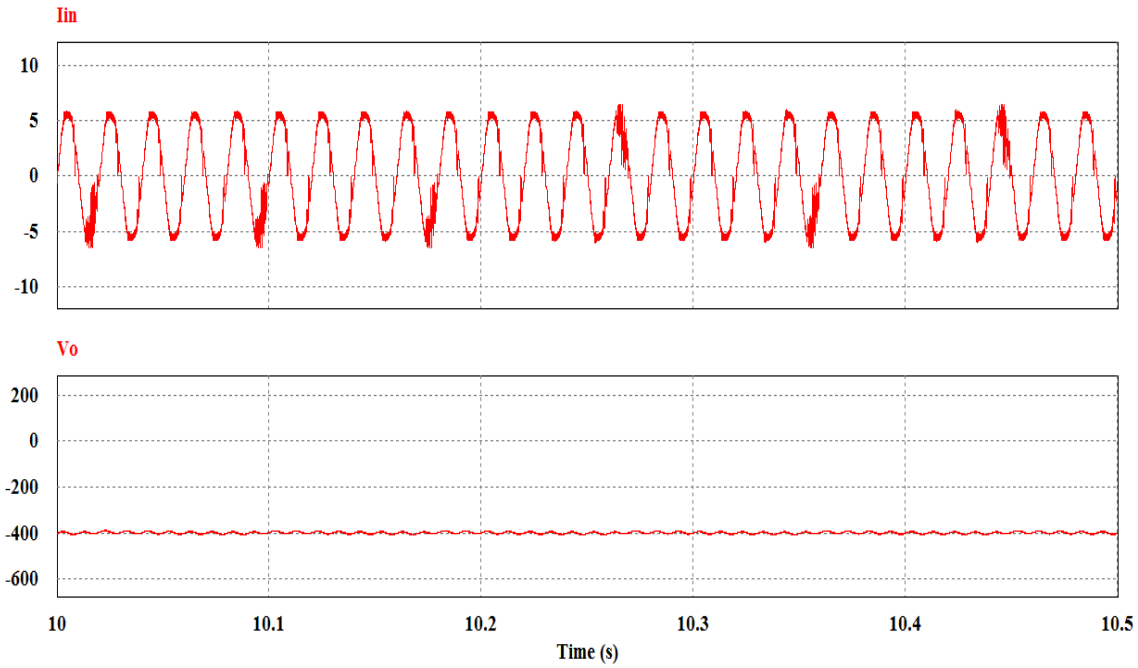


Fig.5.66 Input current and output voltage of proposed ĉuk converter with feedback controller for load resistance of 250 Ω

CHAPTER 6

PROPOSED SEPIC AC-DC CONVERTER

A single phase single switch SEIPC AC-DC converter is proposed in this chapter. For simulation purpose PSIM professional version 9.0.3.400, has been used. The working principle of proposed SEPIC converter is described here. The wave shapes of input voltage, input current, output voltage and input current spectrum at different frequencies and duty cycles are also shown. Data tables of the input current THD (%), input power factor, efficiency (%) and output power at different frequencies and duty cycles of the proposed converter are presented in this chapter. The proposed converters are compared to corresponding conventional converters with switching at DC side. Comparisons are made in terms of input current THD (%), input power factor and efficiency (%) at different duty cycles and loads.

6.1 Proposed Single phase SEPIC AC-DC Converter

The circuit diagram of proposed single phase single switch SEPIC AC-DC converter is shown in Fig. 6.1. The circuit consists of inductors (L1, L2, L3 and L4), capacitors (C1, C2), diodes and a switch (M1). As the given supply voltage is AC, the conversion on both positive and negative cycle of the input voltage is required. L1, L2 and C1 are used for positive half cycle and L3, L4 and C2 are for negative half cycle. The inductors L_pos, L_Neg and capacitors C_pos and C_Neg form the input filter. C_Load and R_Load are the output capacitor and load respectively.

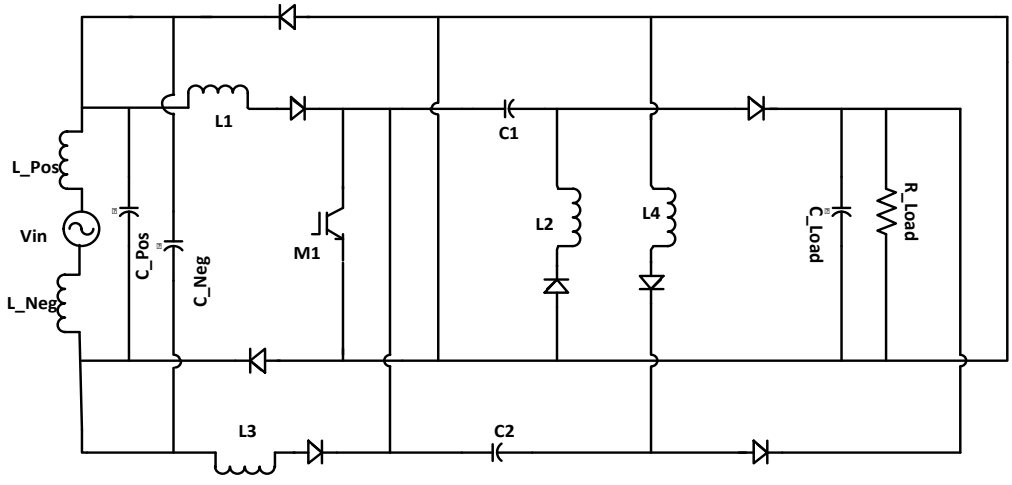


Fig. 6.1 Proposed AC-DC SEPIC Converter

6.2 Principle of Operation

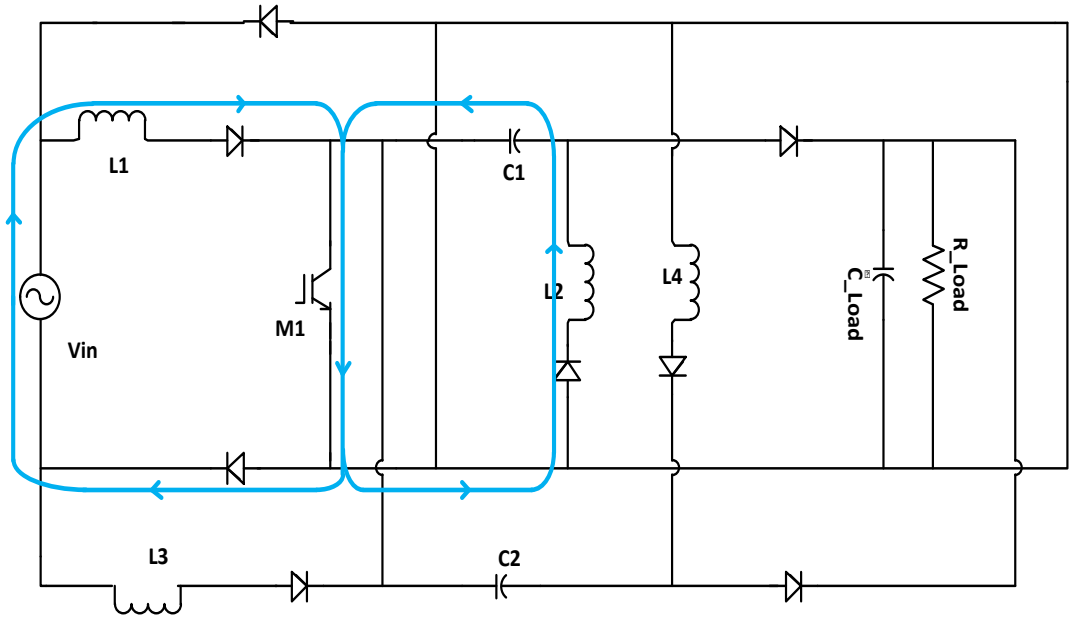
Input AC current chopping at high frequency, provides switched AC current that requires small filter to make it nearly sinusoidal. As a result, the input current THD reduces and the input power factor improves. The proposed SEPIC AC to DC converter has four operating states – positive and negative half cycles each with switch ON and OFF condition, as shown in Fig. 6.2. The operating states are described below.

State 1 is for positive half cycle of the input signal when the switch S is turned ON. This state is presented in Fig. 6.2 (a).The blue line indicates the direction of current flow. Energy transfer is associated with inductors and capacitors L1, L2 and C1 for this state.

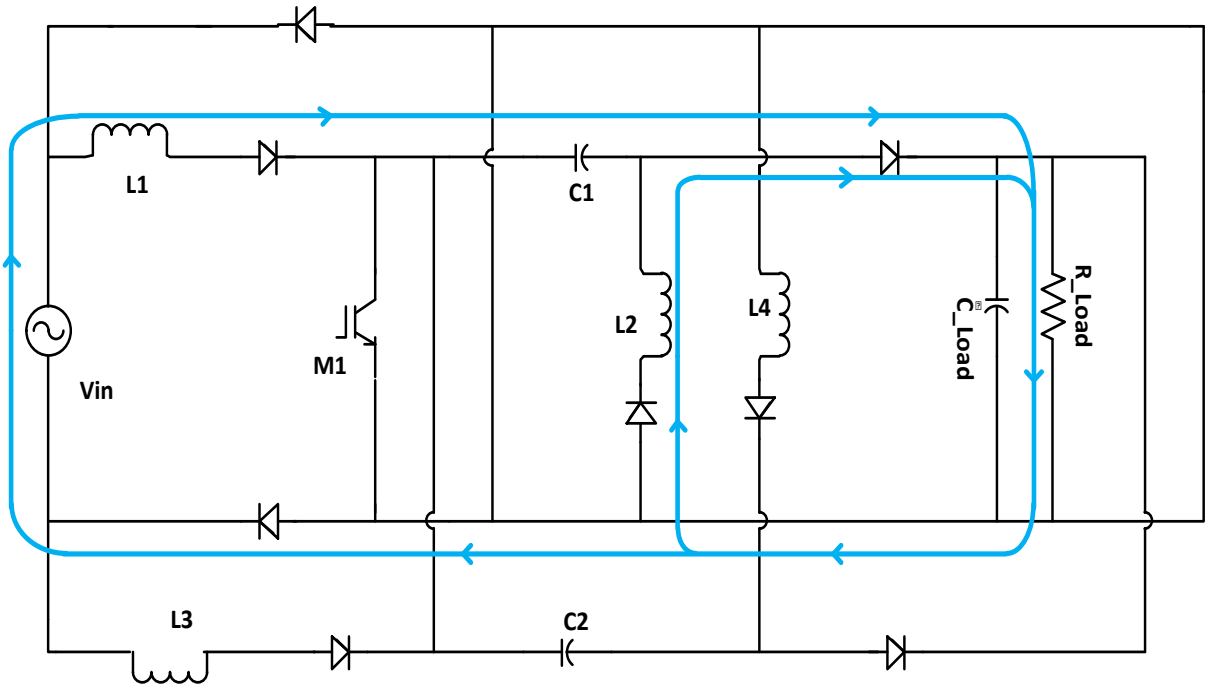
State 2 is for the positive half cycle of the input signal when the switch S is OFF. This state is presented in Fig. 6.2 (b).The blue line indicates the direction of current flow. Energy transfer is associated with inductors and capacitors L1, L2 and C1 for this state.

State 3 is for the negative half cycle of the input signal when the switch S is turned ON. This state is shown in Fig. 6.2 (c).The violet line indicates the direction of current flow. Energy transfer is associated with inductors and capacitors L3, L4 and C2 for this state.

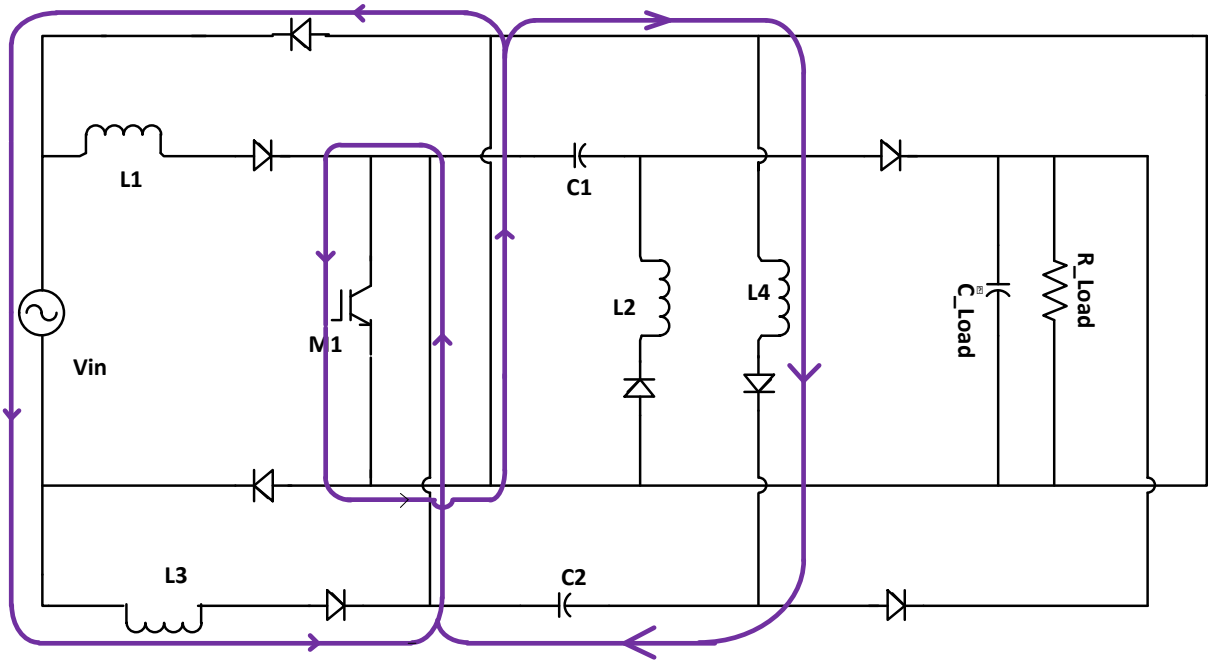
State 4 is for the negative half cycle of the input signal when the switch S is turned OFF. This state is shown in Fig. 6.2 (d).The violet line indicates the direction of current flow. Energy transfer is associated with inductors and capacitors L3, L4 and C2 for this state.



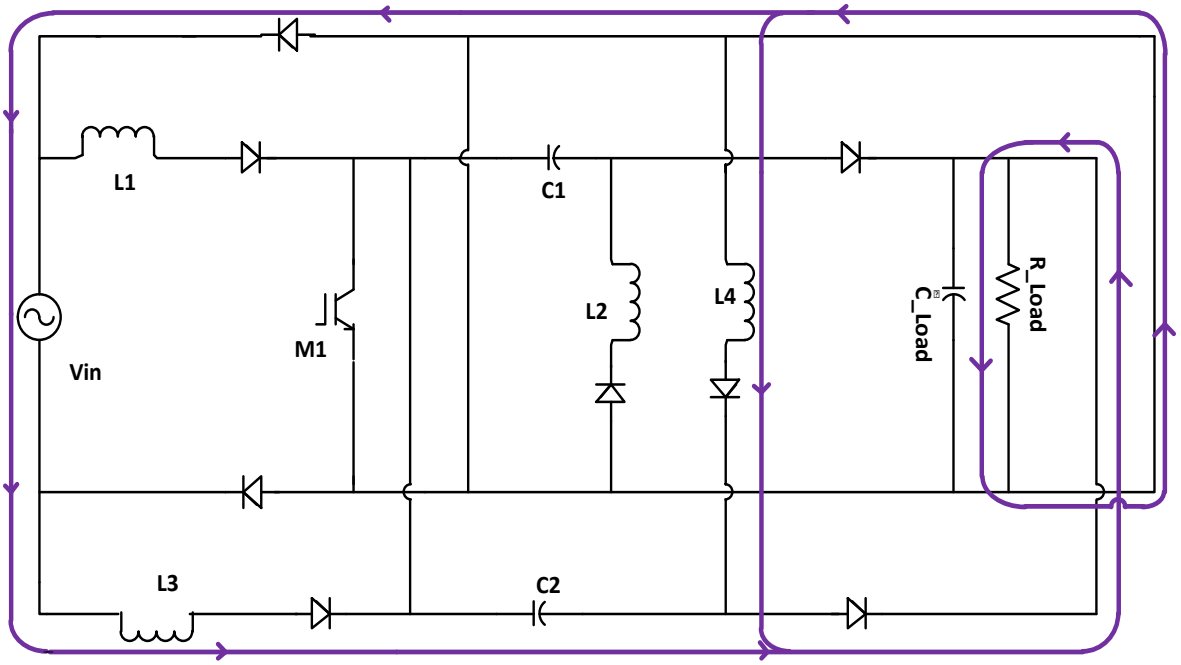
(a)


L1
C1
Vin
M1
L2
L4
C_Load
R_Load
L3
C2

(b)


L1
C1
Vin
M1
L2
L4
C_Load
R_Load
L3
C2

(c)



(d)

Fig. 6.2. Four states of operation of proposed AC-DC SEPIC converter (A) State 1, circuit when switch is ON during positive half cycle of the AC supply, (B) State 2, circuit when switch is OFF during positive half cycle of the AC supply,(C) State 3, circuit when switch is ON during negative half cycle of the AC supply,(D) State 4, circuit when switch is OFF during negative half cycle of the AC supply.

6.3 Simulation Results

6.3.1 Circuit Parameters

For simulation of SEPIC configuration, an input ac source of 300V amplitude with frequency of 50 Hz. is used. An IGBT is used for switching purpose. For SEPIC scheme, the inductors L1, L2, L3 and L4 have the values of 2 mH each. The filter inductors L_pos and L_Neg have the values of 2.5 mH and capacitors C1and C2 have the values of 1 µF each. The filter capacitors C_pos and C_neg have the values of 2 µF each. The output capacitor C_Load has the value of 20 µF and a resistor R_Load of 100 Ω is used as load in the proposed circuit. The proposed single-phase converter has been compared with the conventional single-phase diode bridge rectifier followed by a DC-DC SEPIC converter shown in Fig. 6.3.The conventional circuits also have same parameters and conditions like the proposed one for simulation.

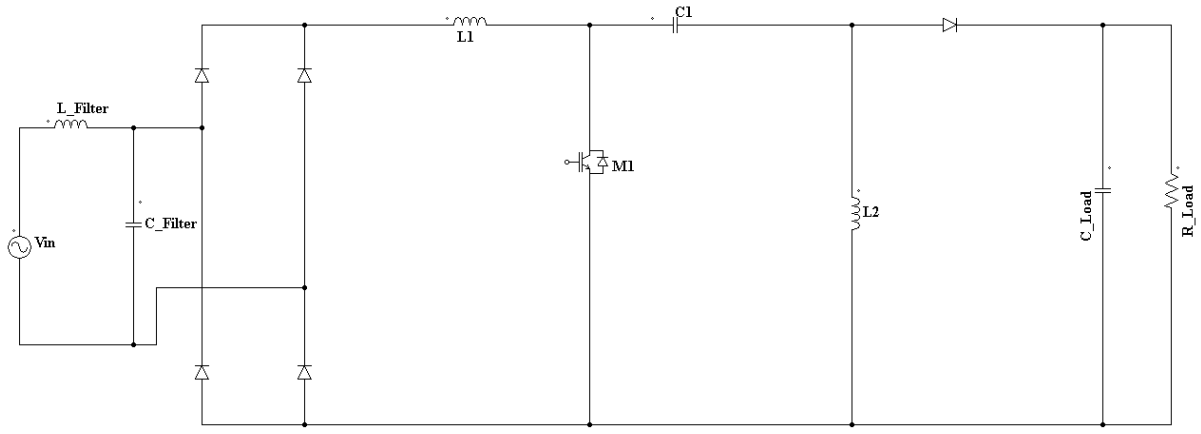


Fig. 6.3 Conventional SEPIC AC-DC Converter

6.3.2 Results from Simulation

Typical input voltage, input current and output voltage waveforms of the proposed single-phase AC-DC SEPIC converter circuit at different switching frequencies (f_s) of different duty cycles (D) and load resistance (R_Load) of 100 Ω are presented here. Fig. 6.4 shows the typical input voltage of the proposed converter. Input current at different frequencies and duty cycles and their corresponding spectrums are presented in Figs. 6.5 to 6.22. From these figures it is observed that, the input current is nearly sinusoidal. Figs. 6.23 to 6.40 shows the input current and corresponding current spectrums of the conventional circuit consisting of a rectifier followed by a SEPIC DC-DC converter under same operating condition to observe the typical improvement. Figs. 6.41 to 6.48 show the output voltage waveform of proposed SEPIC converter at switching frequency of 8 KHz. and different duty cycles. From these figures it is observed that the output voltage is DC contains few ripples.

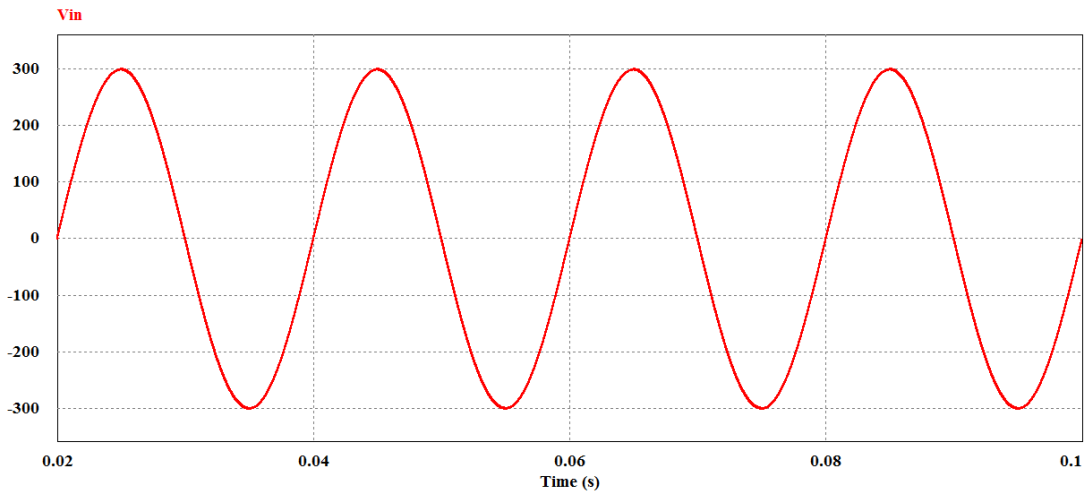


Fig. 6.4 Wave shape of input voltage of Proposed AC-DC SEPIC Converter

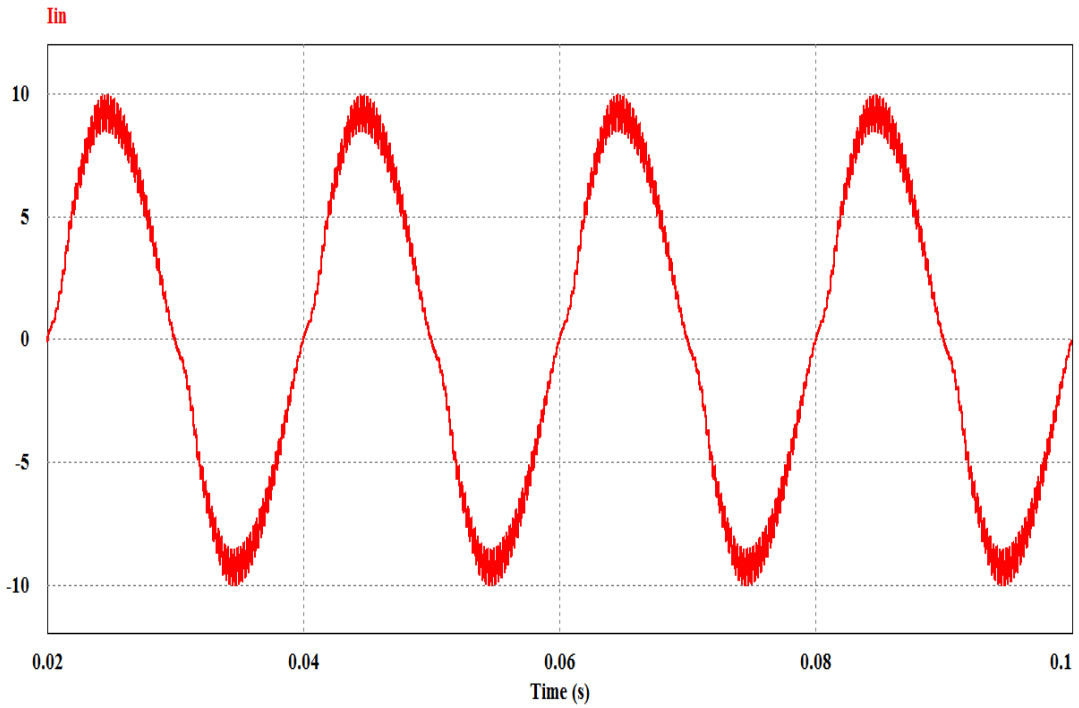


Fig.6.5 Input current of proposed SEPIC converter at f_s = 4KHz. and D = 0.5

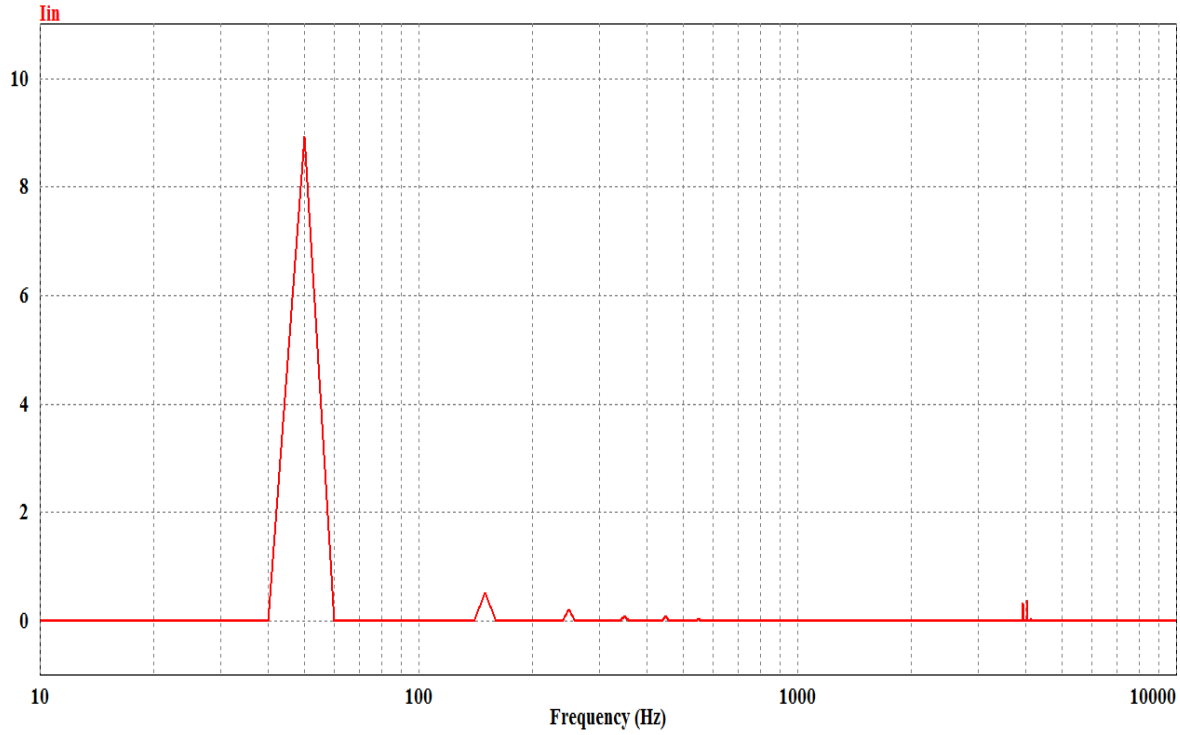


Fig.6.6 Input current spectrum of proposed SEPIC converter at f_s = 4 KHz. and D = 0.5

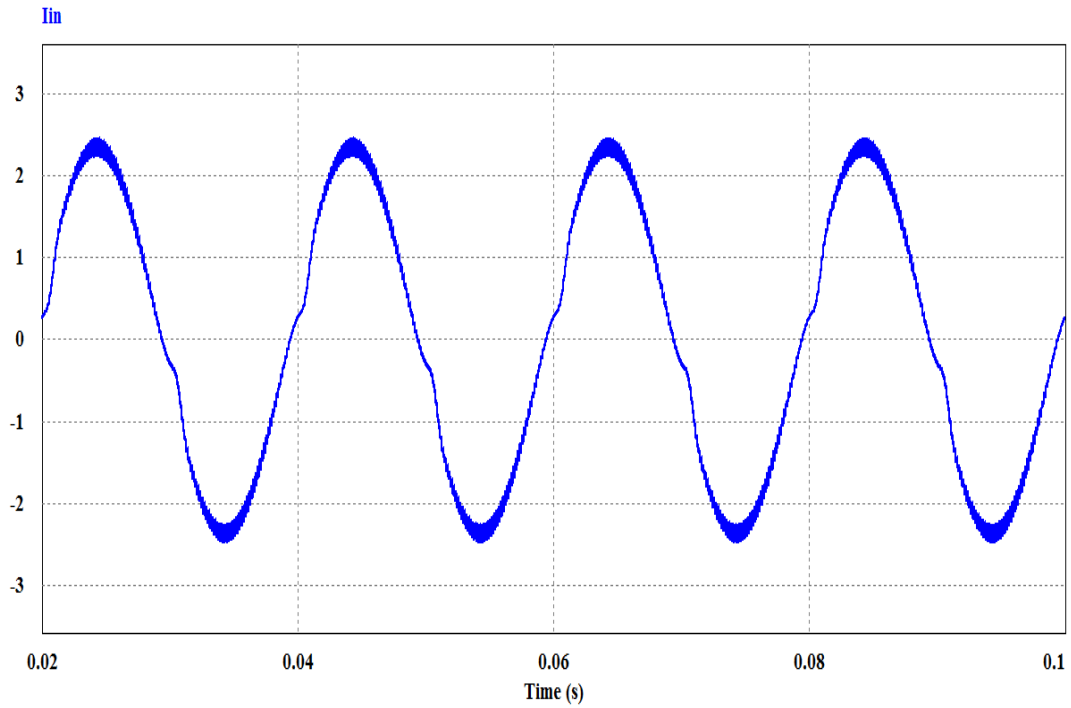


Fig.6.7 Input current of proposed SEPIC converter at f_s = 6 KHz. D = 0.3

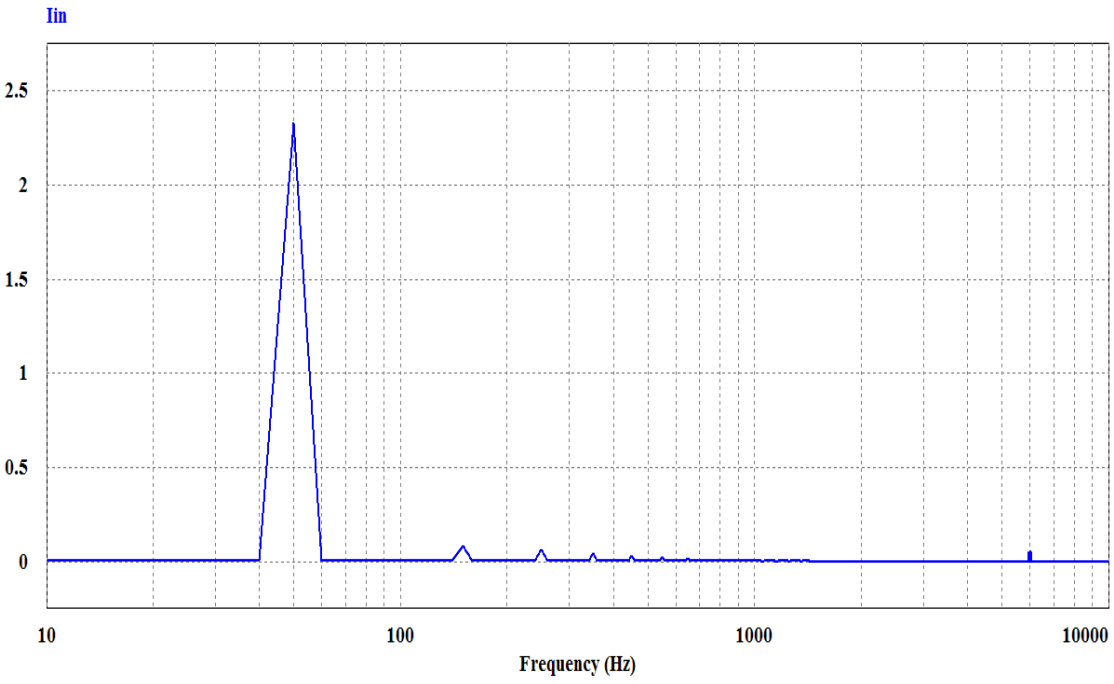


Fig.6.8 Input current spectrum of proposed SEPIC converter at f_s = 6 KHz. D = 0.3

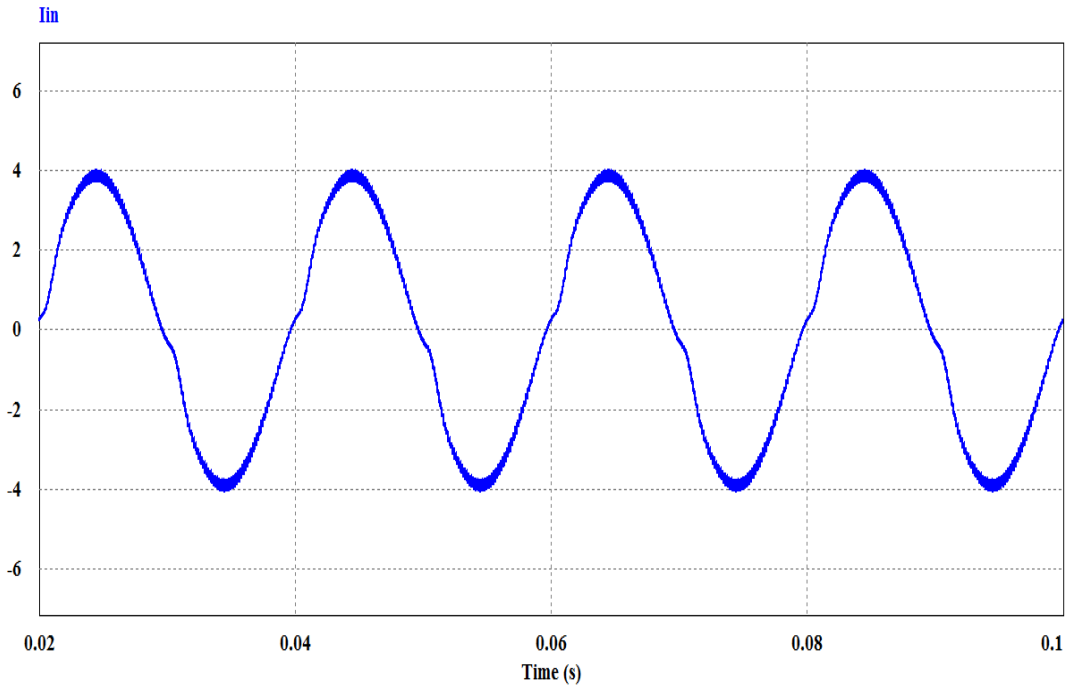


Fig.6.9 Input current of proposed SEPIC converter at f_s = 6 KHz. D = 0.4

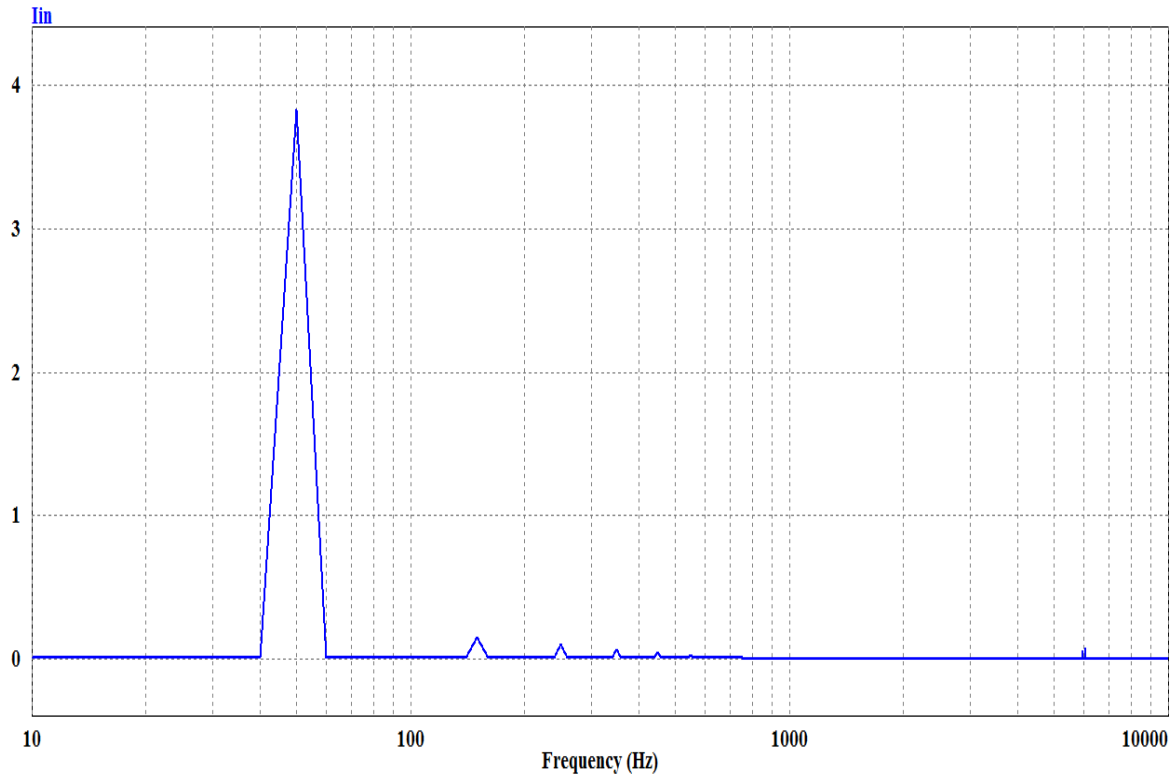


Fig.6.10 Input current spectrum of proposed SEPIC converter at f_s = 6 KHz. D = 0.4

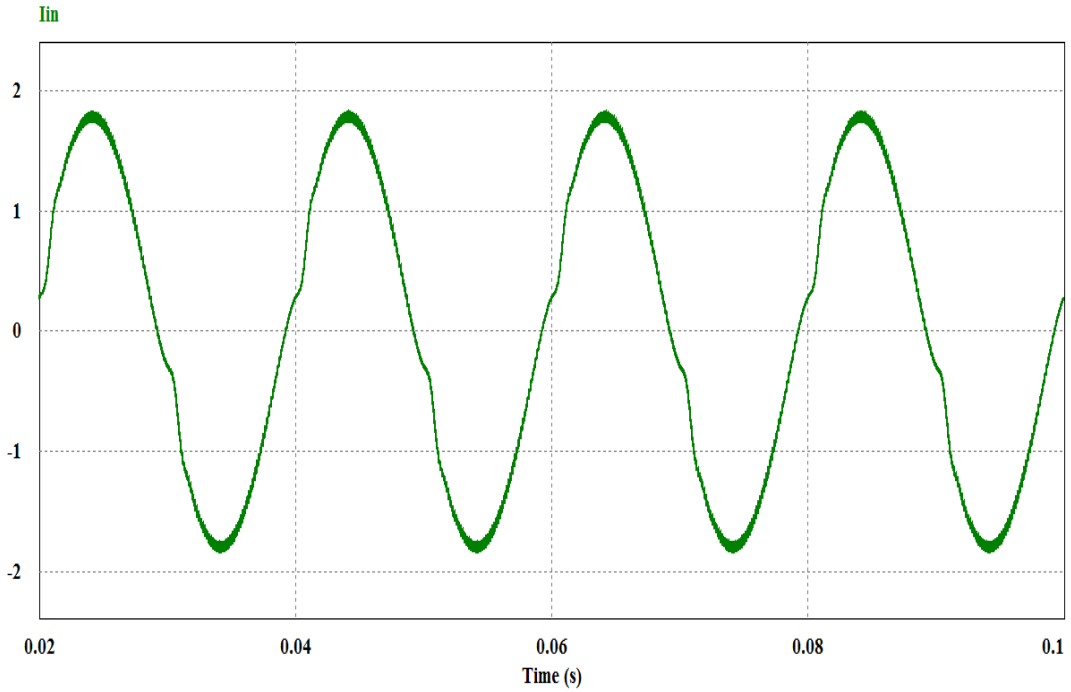


Fig.6.11 Input current of proposed SEPIC converter at f_s = 8 KHz. D = 0.3

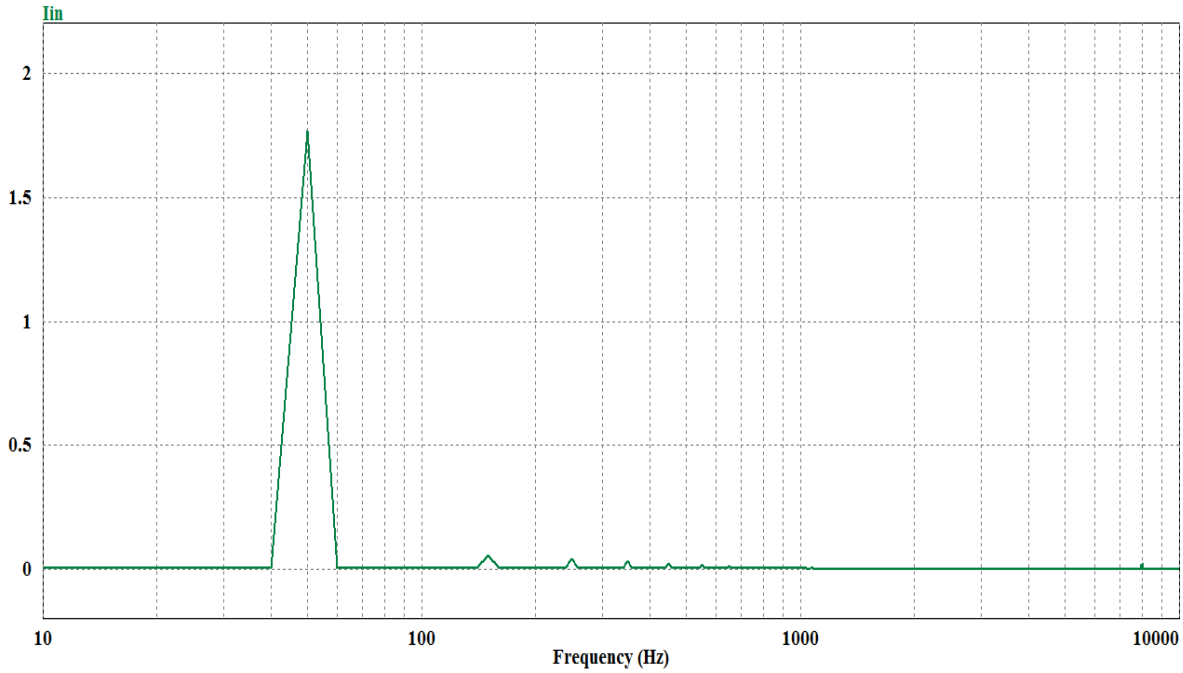


Fig.6.12 Input current spectrum of proposed SEPIC converter at f_s = 8 KHz. D = 0.3

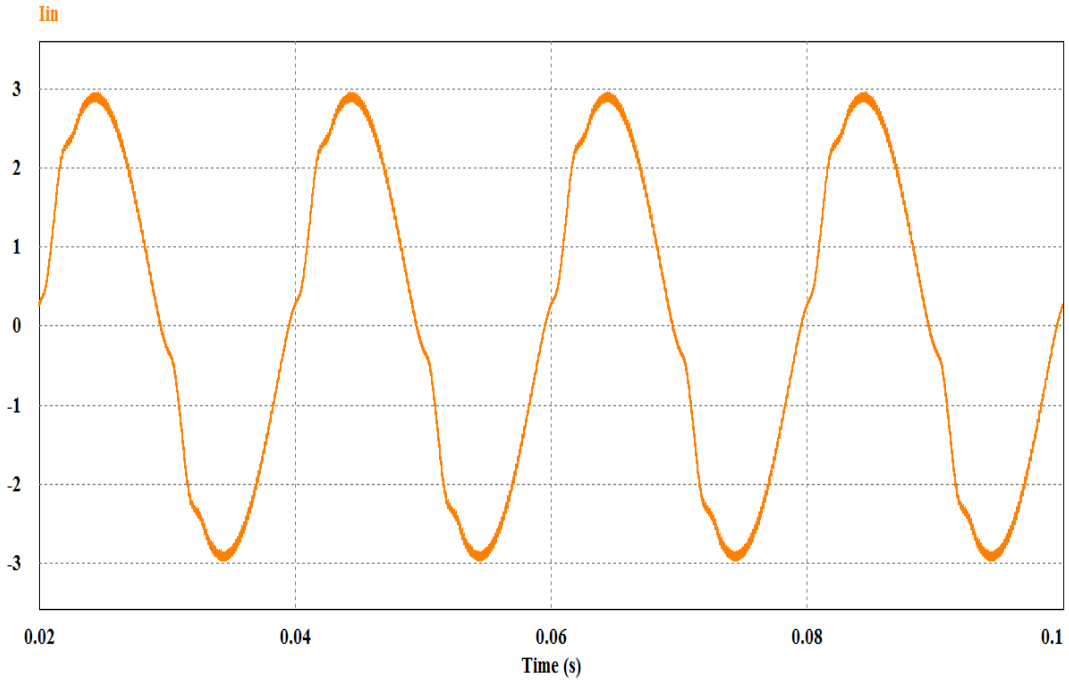


Fig.6.13 Input current of proposed SEPIC converter at f_s = 8 KHz. D = 0.4

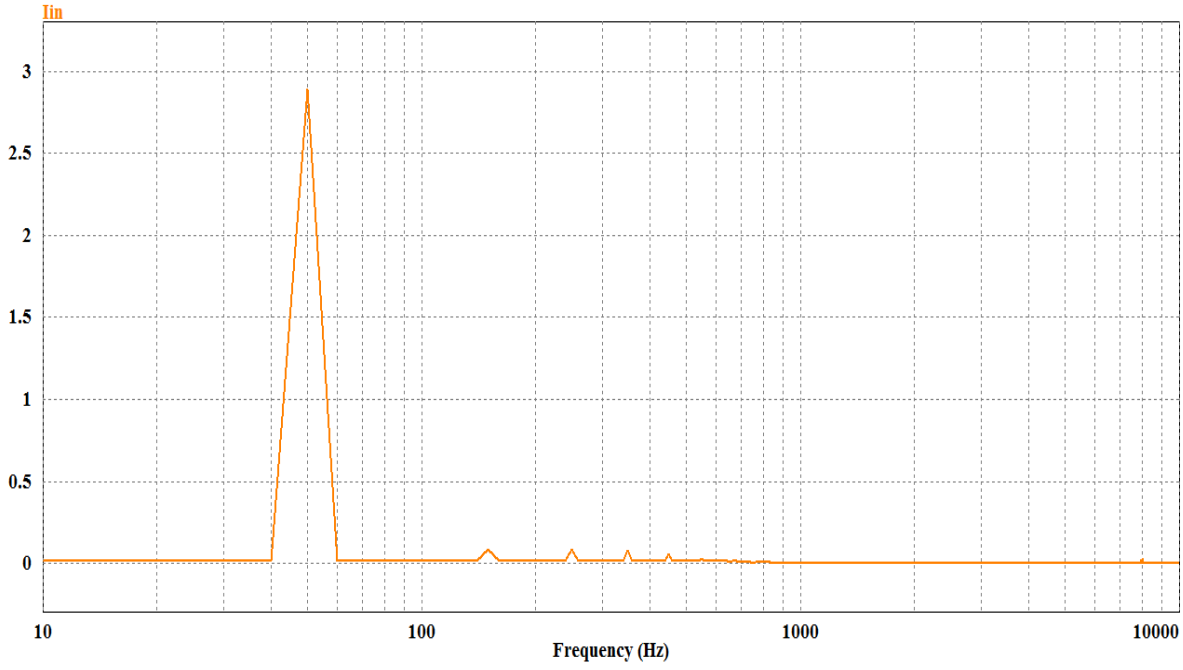


Fig.6.14 Input current spectrum of proposed SEPIC converter at f_s = 8 KHz. D = 0.4

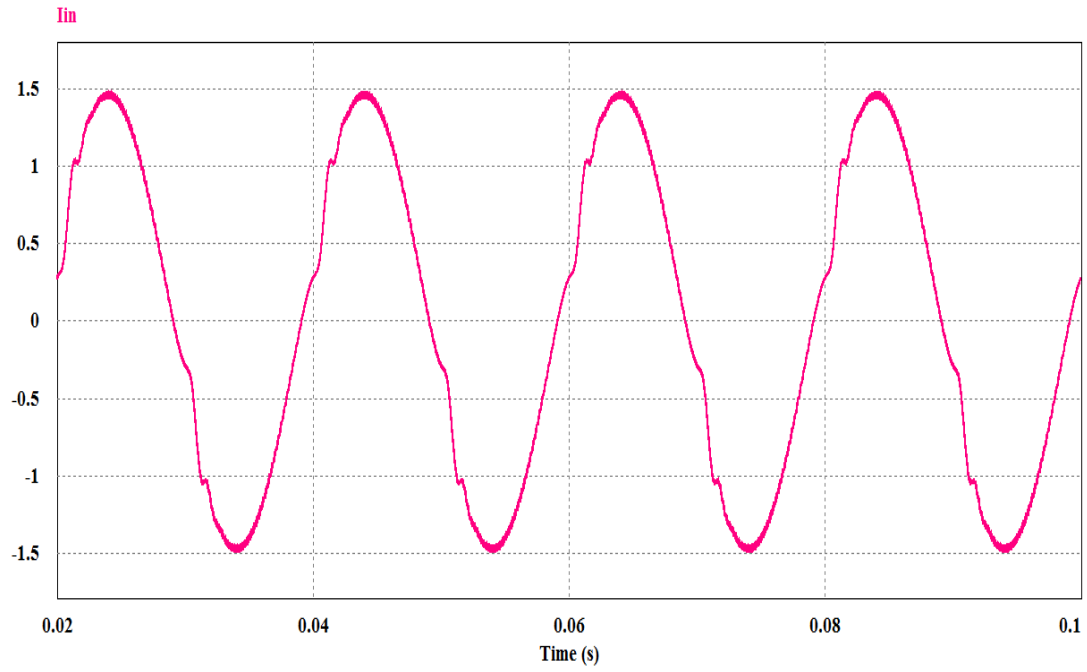


Fig.6.15 Input current of proposed SEPIC converter at f_s = 10 KHz. D = 0.3

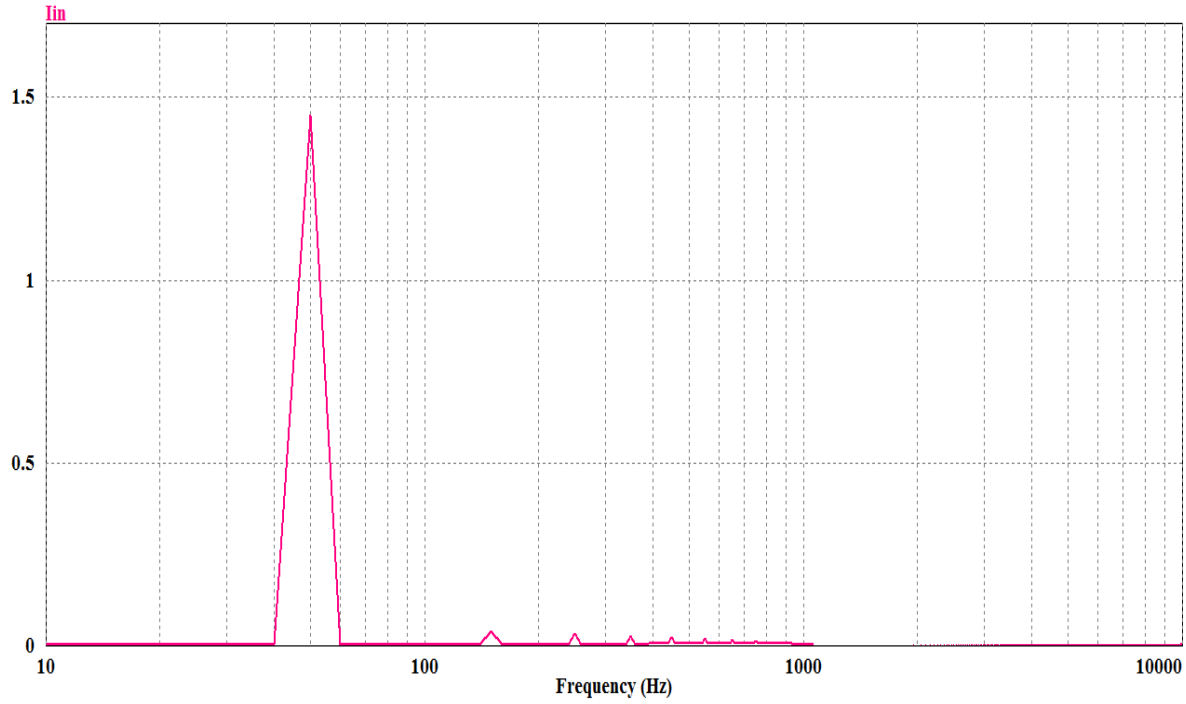


Fig.6.16 Input current spectrum of proposed SEPIC converter at f_s = 10 KHz. D = 0.3

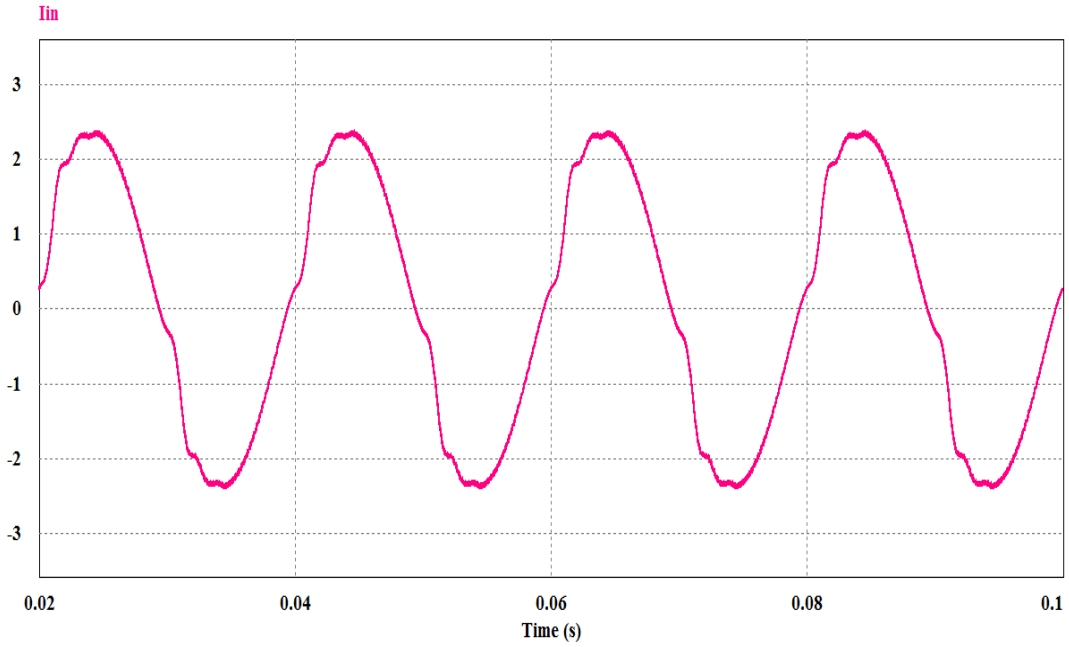


Fig.6.17 Input current of proposed SEPIC converter at f_s = 10 KHz. D = 0.4

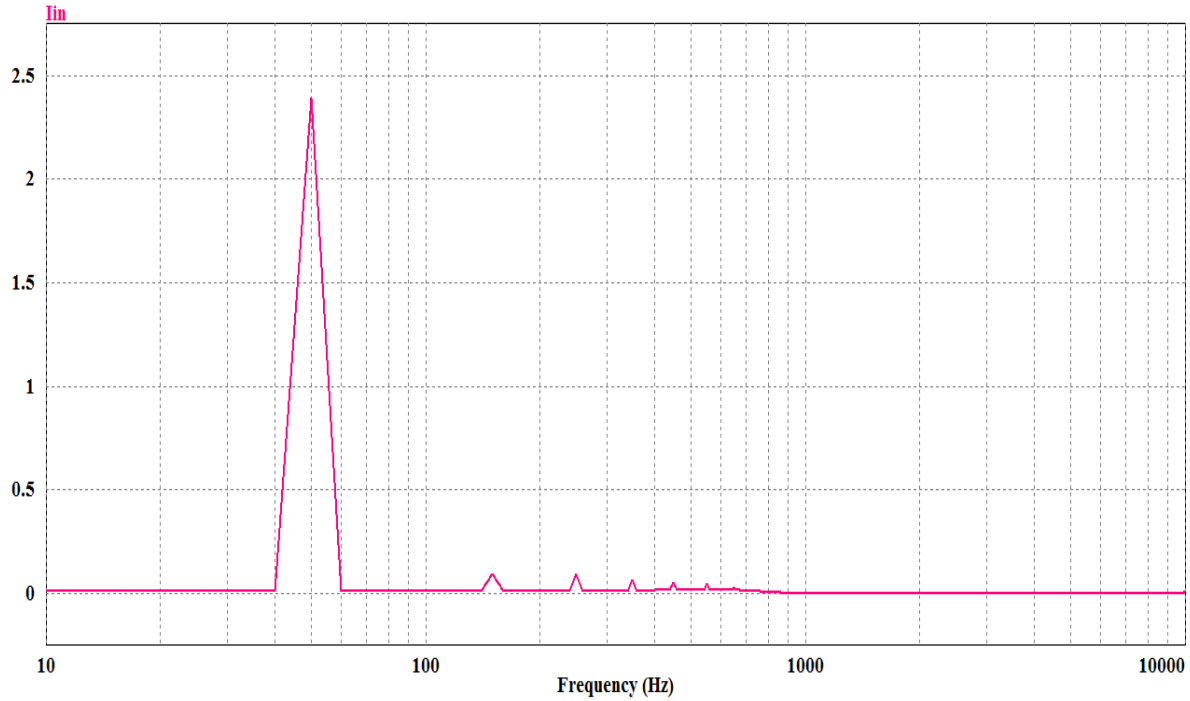


Fig.6.18 Input current spectrum of proposed SEPIC converter at f_s = 10 KHz. D = 0.4

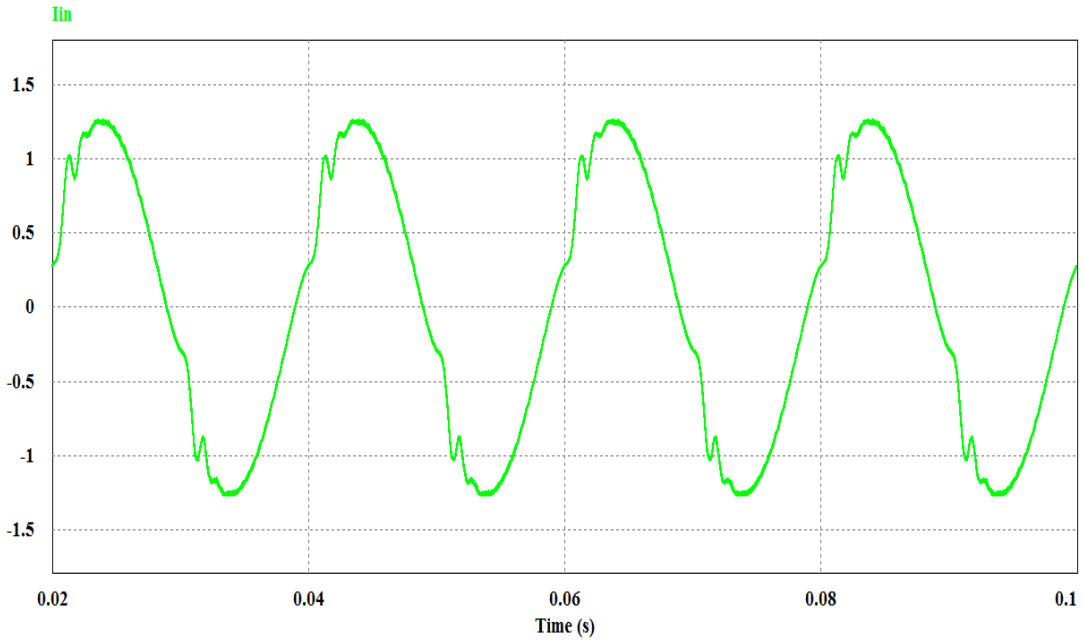


Fig.6.19 Input current of proposed SEPIC converter at f_s = 12 KHz. D = 0.3

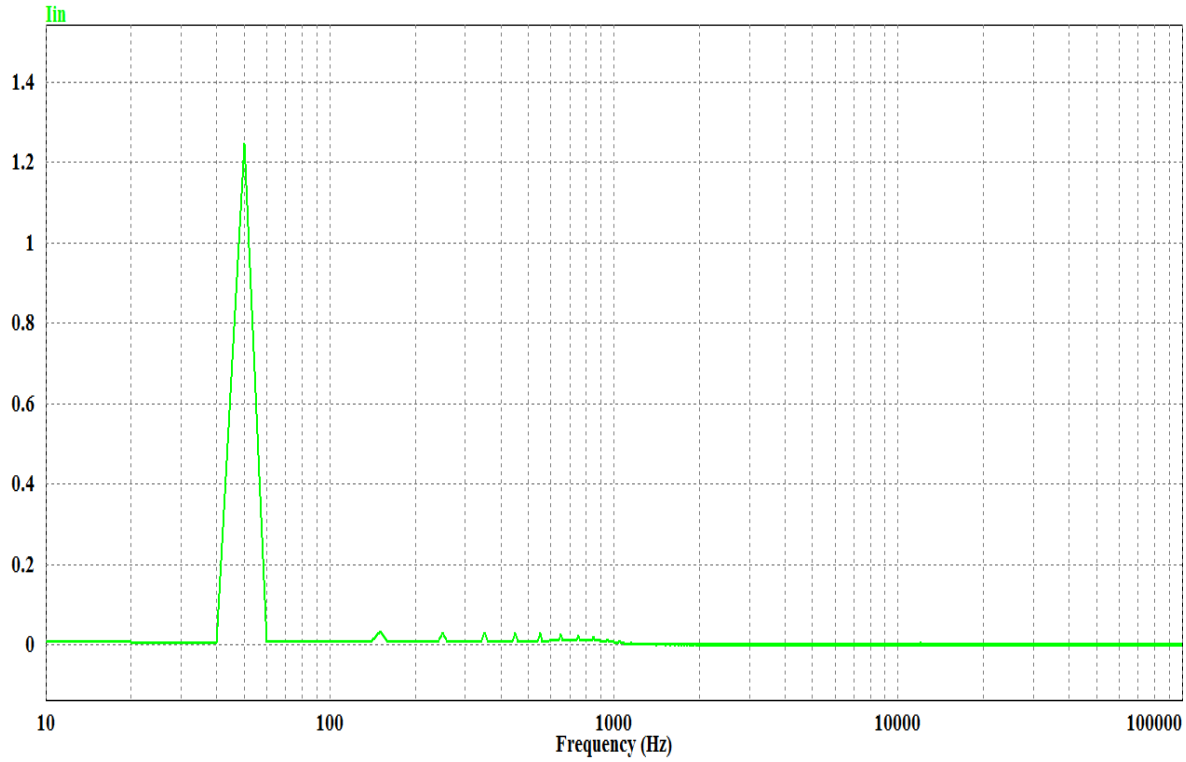


Fig.6.20 Input current spectrum of proposed SEPIC converter at f_s = 12 KHz. D = 0.3

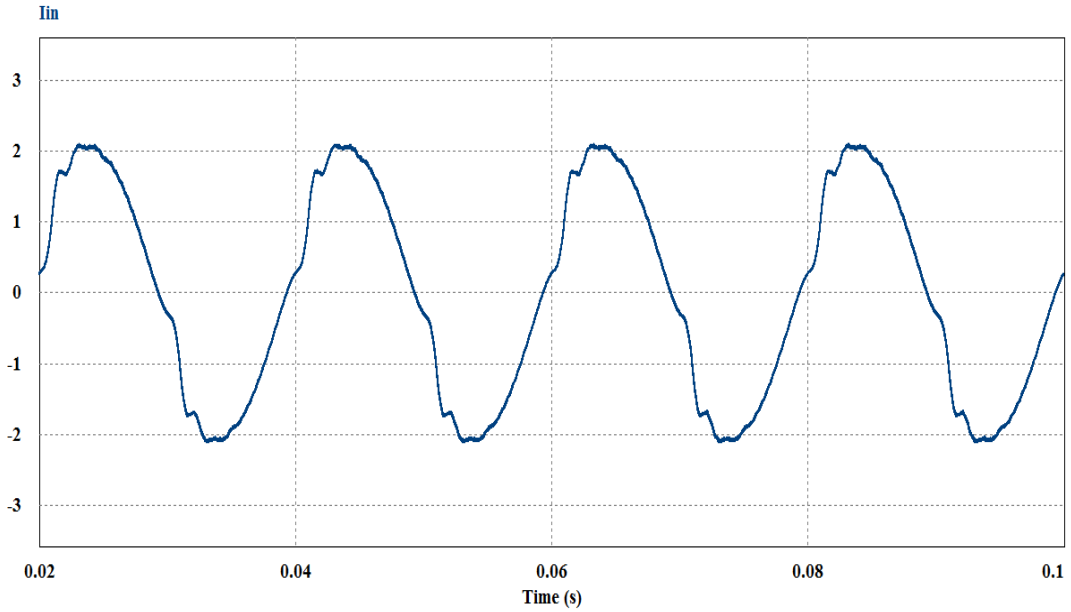


Fig.6.21 Input current of proposed SEPIC converter at f_s = 12 KHz. D = 0.4

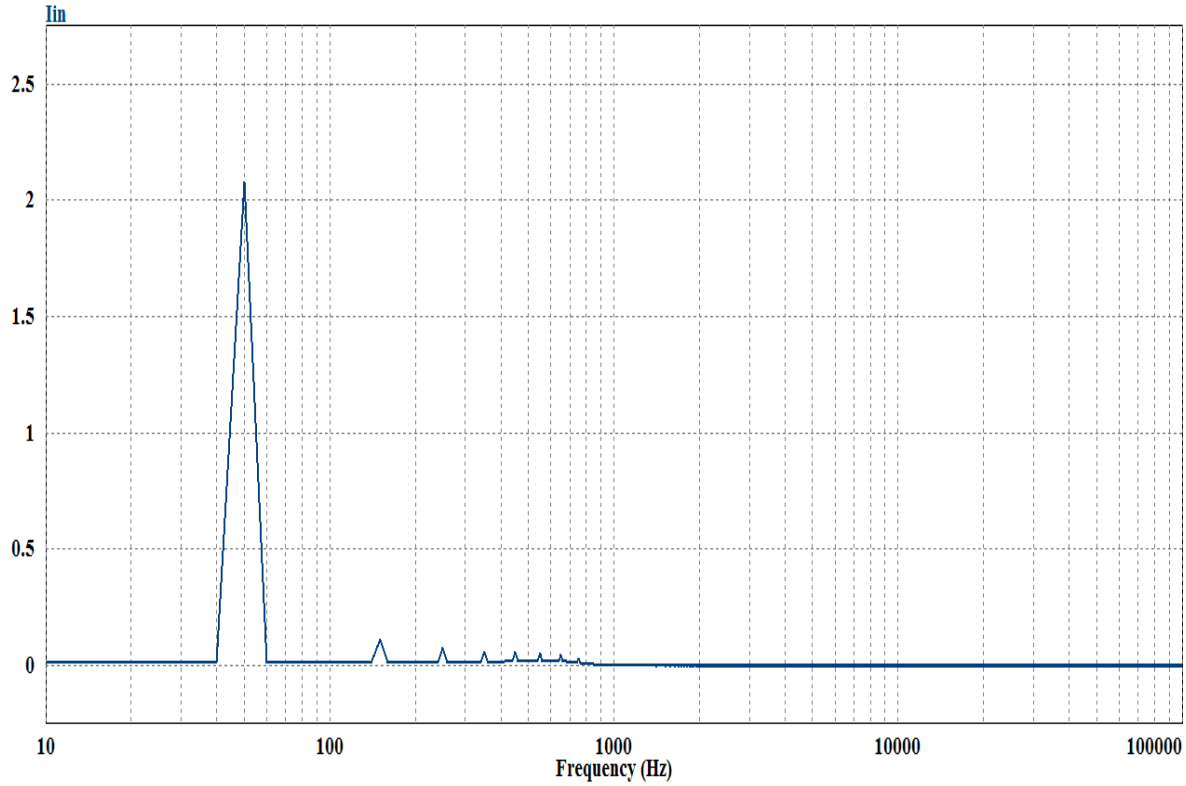


Fig.6.22 Input current spectrum of proposed SEPIC converter at f_s = 12 KHz. D = 0.4

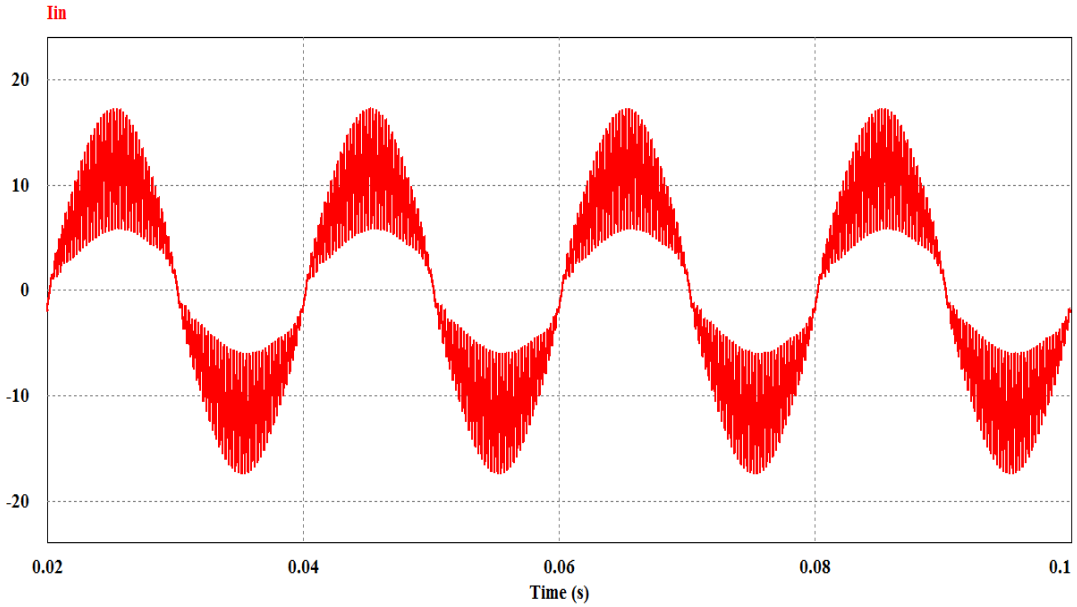


Fig.6.23 Input current of conventional SEPIC converter at f_s = 4 KHz. D = 0.5

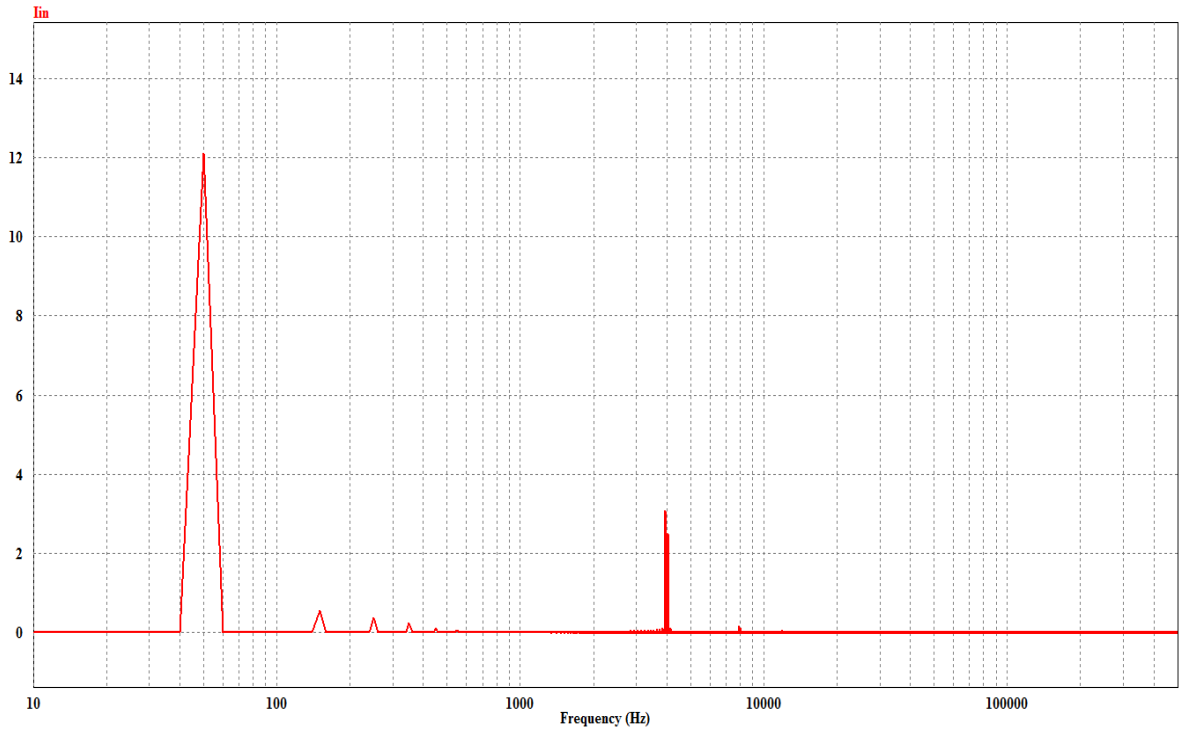


Fig.6.24 Input current spectrum of conventional SEPIC converter at f_s = 4 KHz. D = 0.5

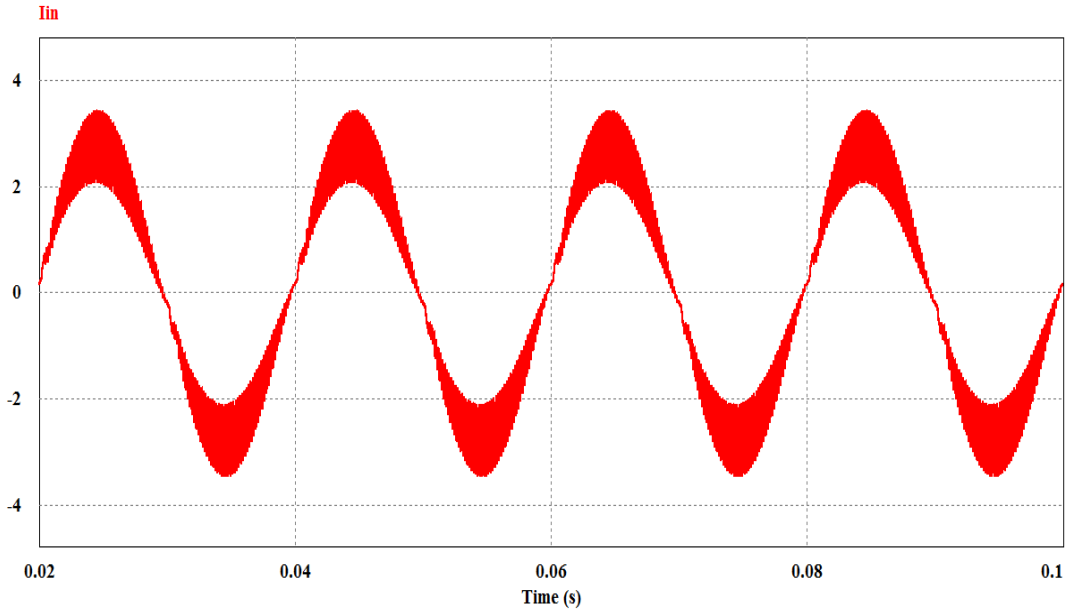


Fig.6.25 Input current of conventional SEPIC converter at f_s = 6 KHz. D = 0.3

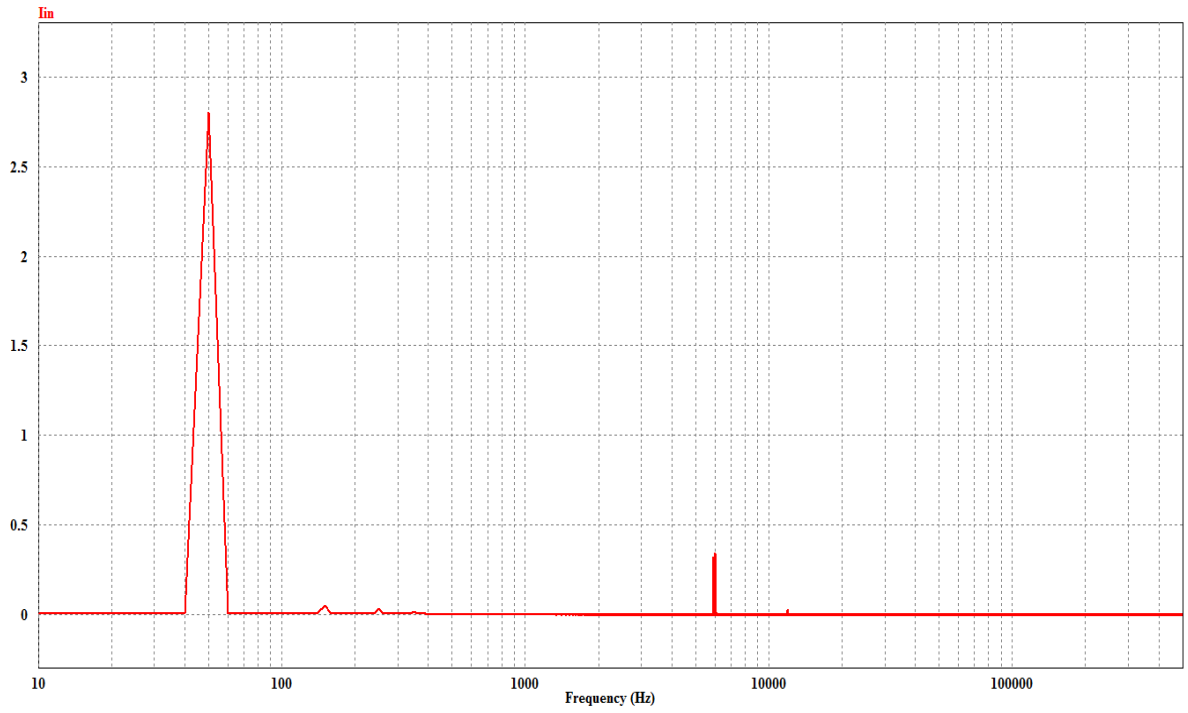


Fig.6.26 Input current spectrum of conventional SEPIC converter at f_s = 6 KHz. D = 0.3

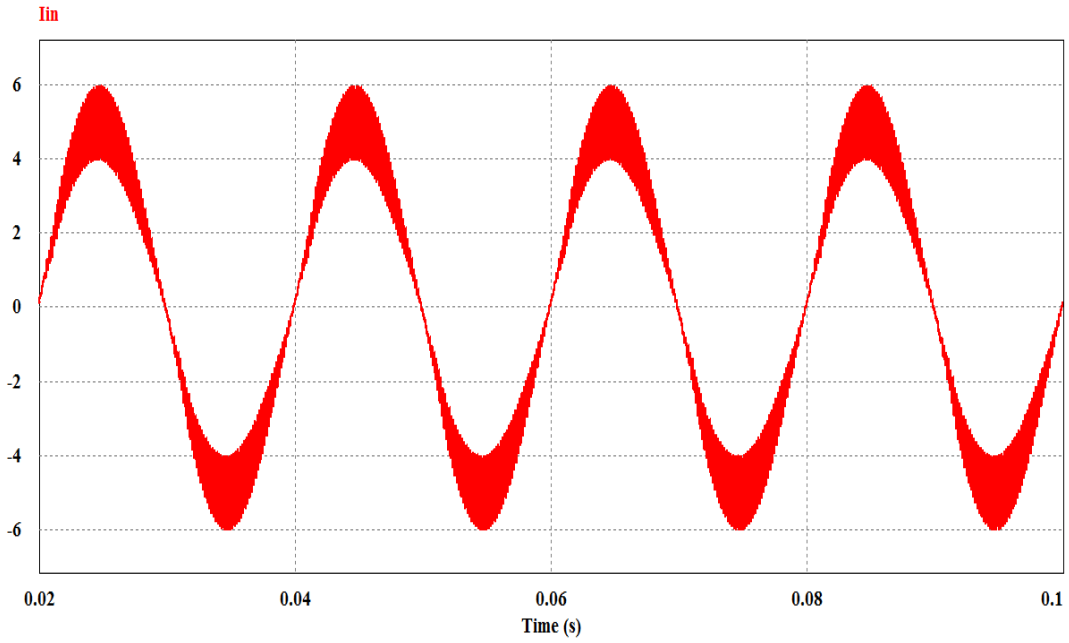


Fig.6.27 Input current of conventional SEPIC converter at f_s = 6 KHz. D = 0.4

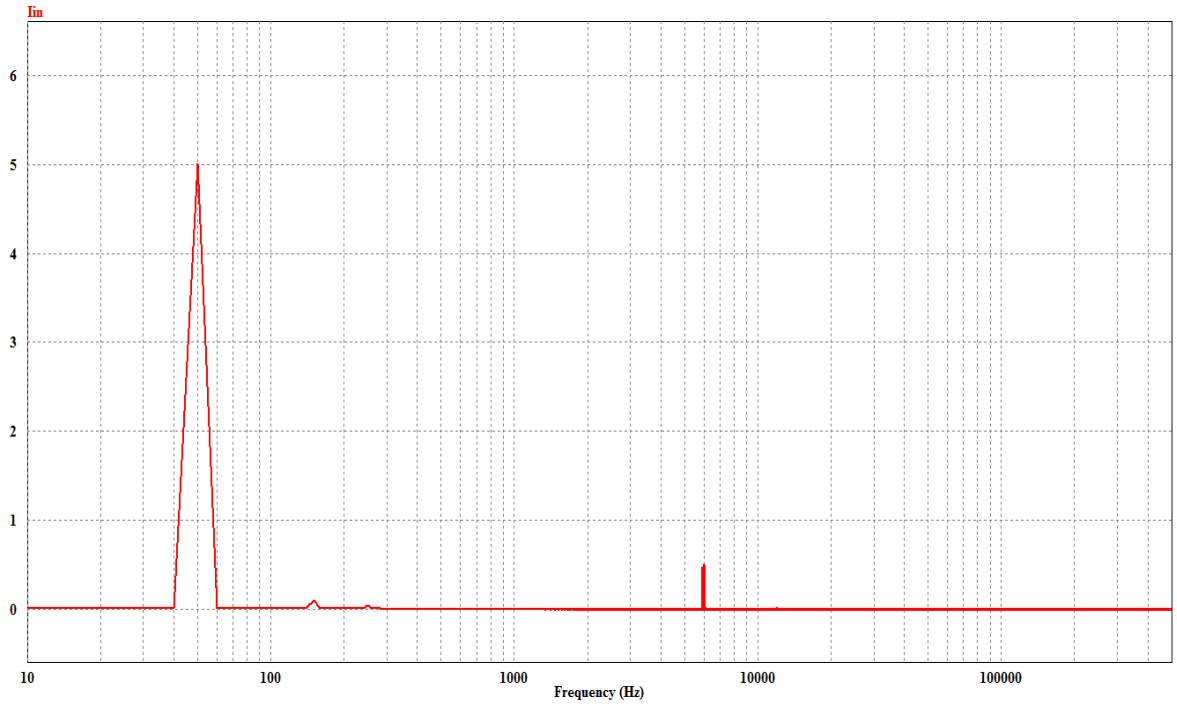


Fig.6.28 Input current spectrum of conventional SEPIC converter at f_s = 6 KHz. D = 0.4

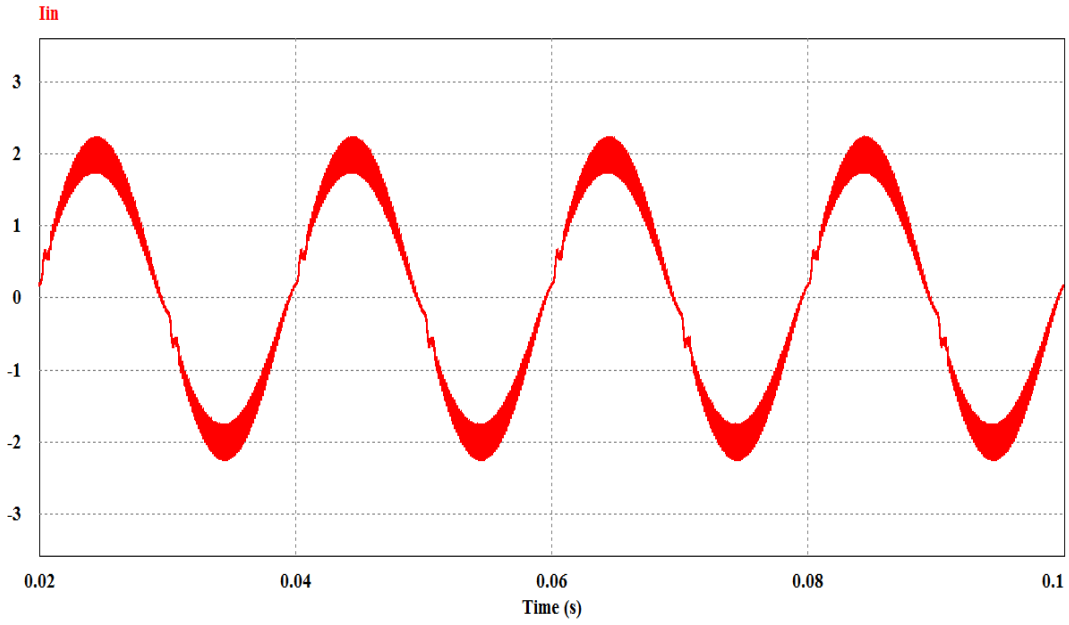


Fig.6.29 Input current of conventional SEPIC converter at f_s = 8 KHz. D = 0.3

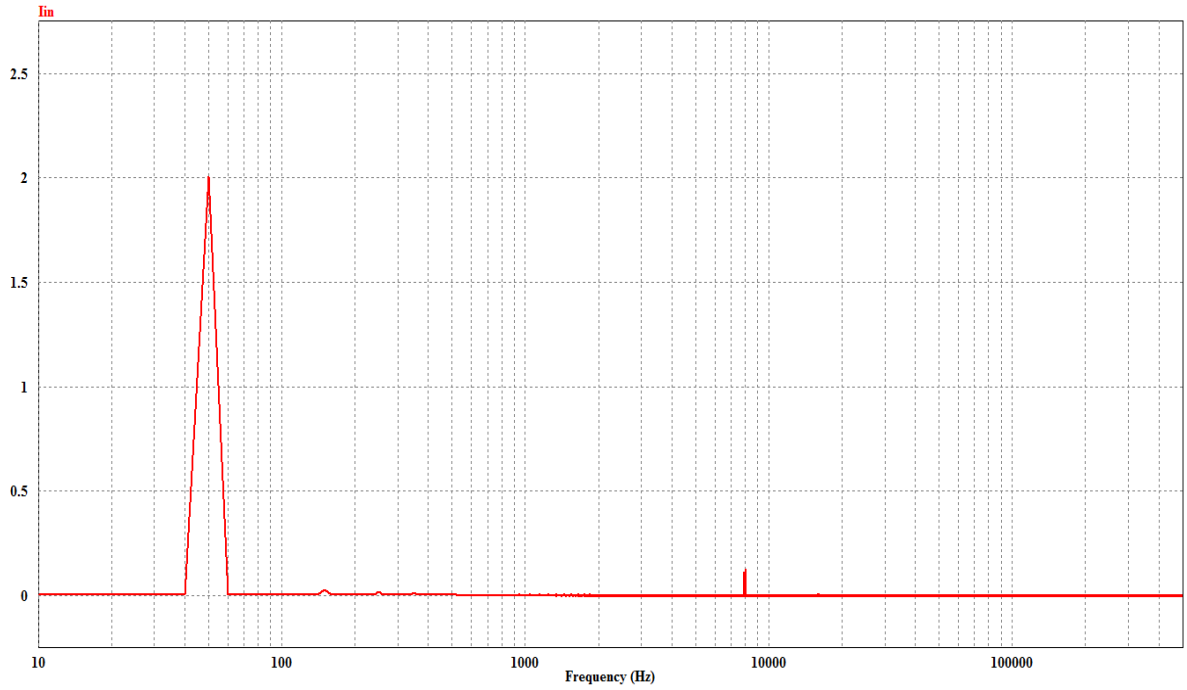


Fig.6.30 Input current spectrum of conventional SEPIC converter at f_s = 8 KHz. D = 0.3

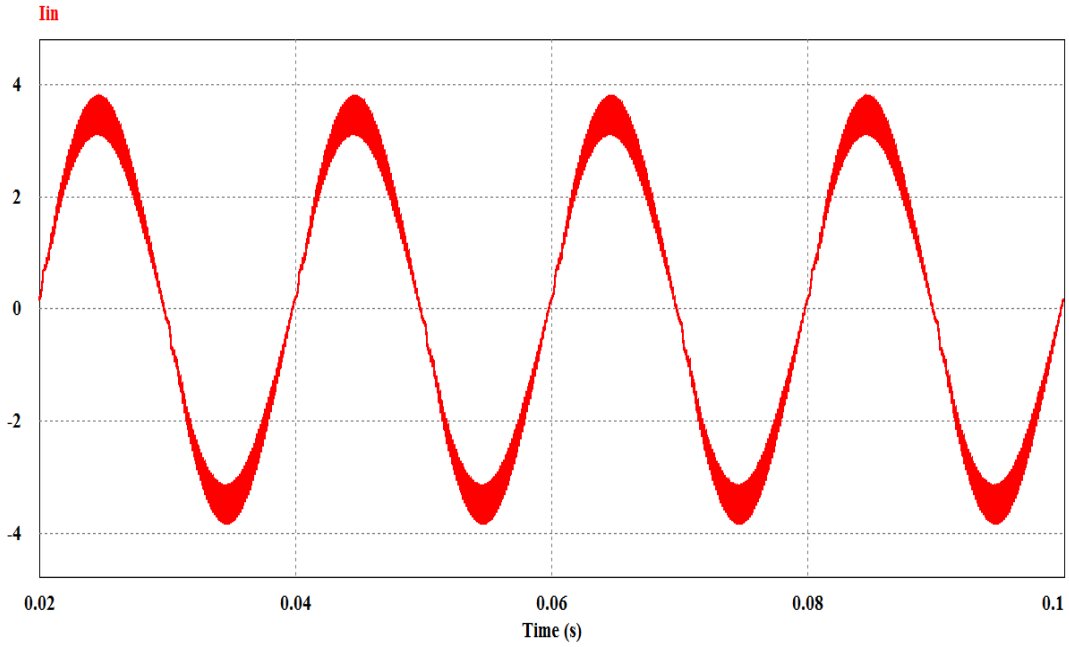


Fig.6.31 Input current of conventional SEPIC converter at f_s = 8 KHz. D = 0.4

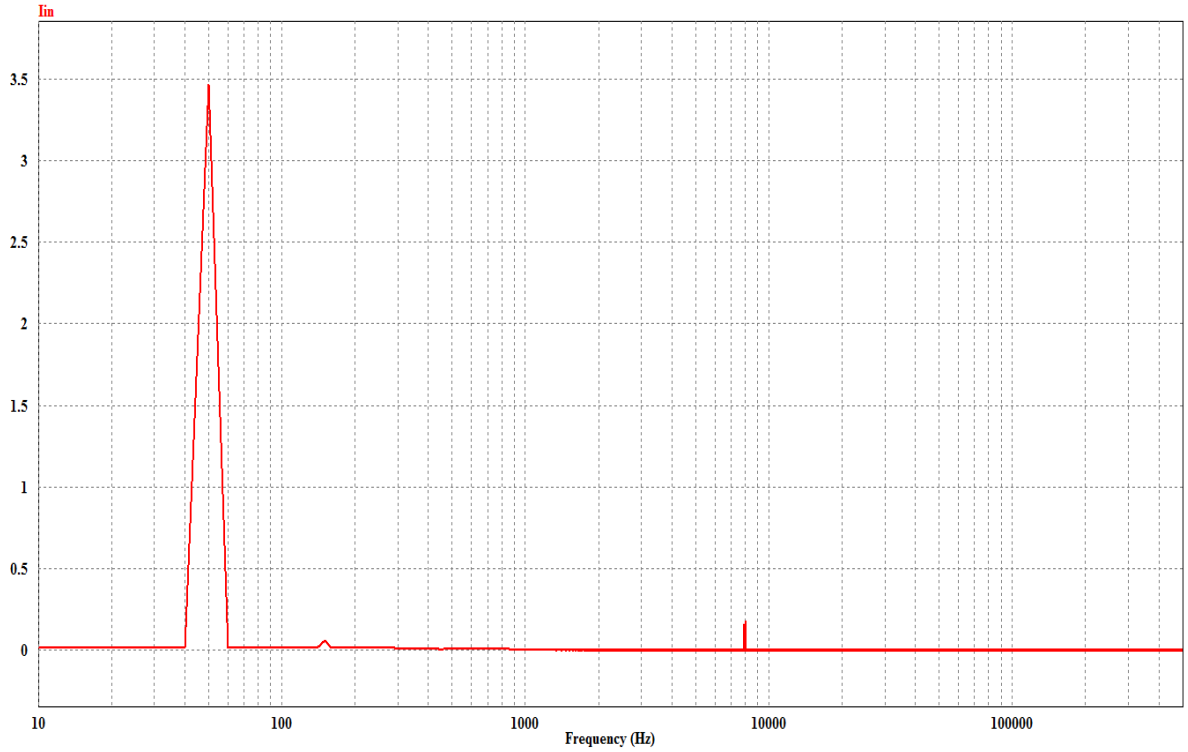


Fig.6.32 Input current spectrum of conventional SEPIC converter at f_s = 8 KHz. D = 0.4

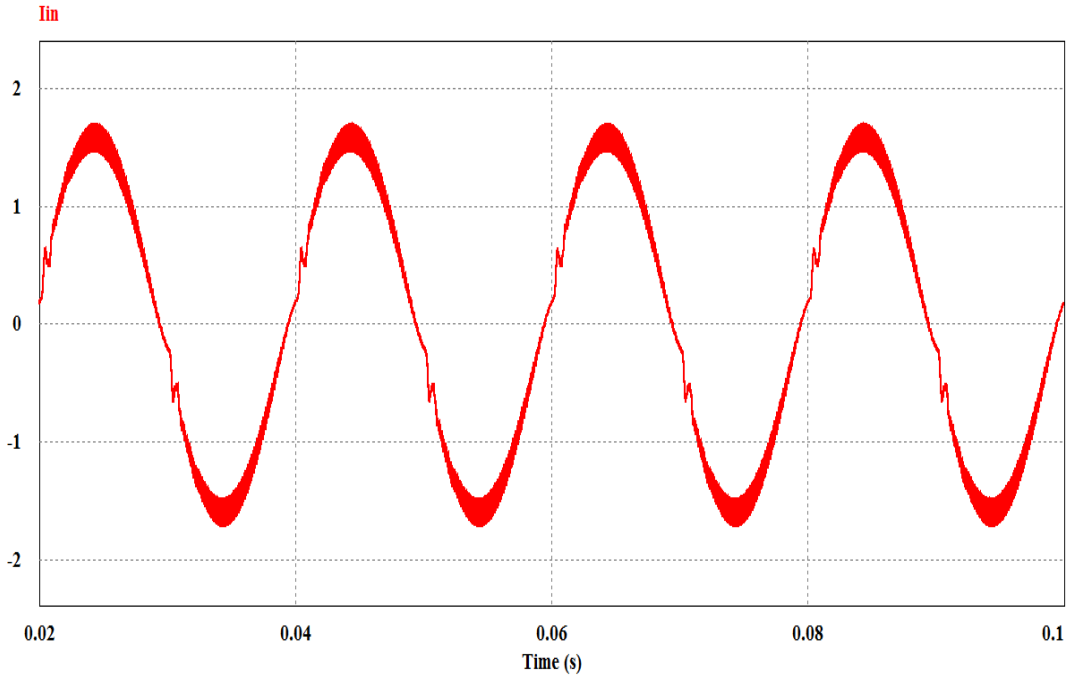


Fig.6.33 Input current of conventional SEPIC converter at f_s = 10 KHz. D = 0.3

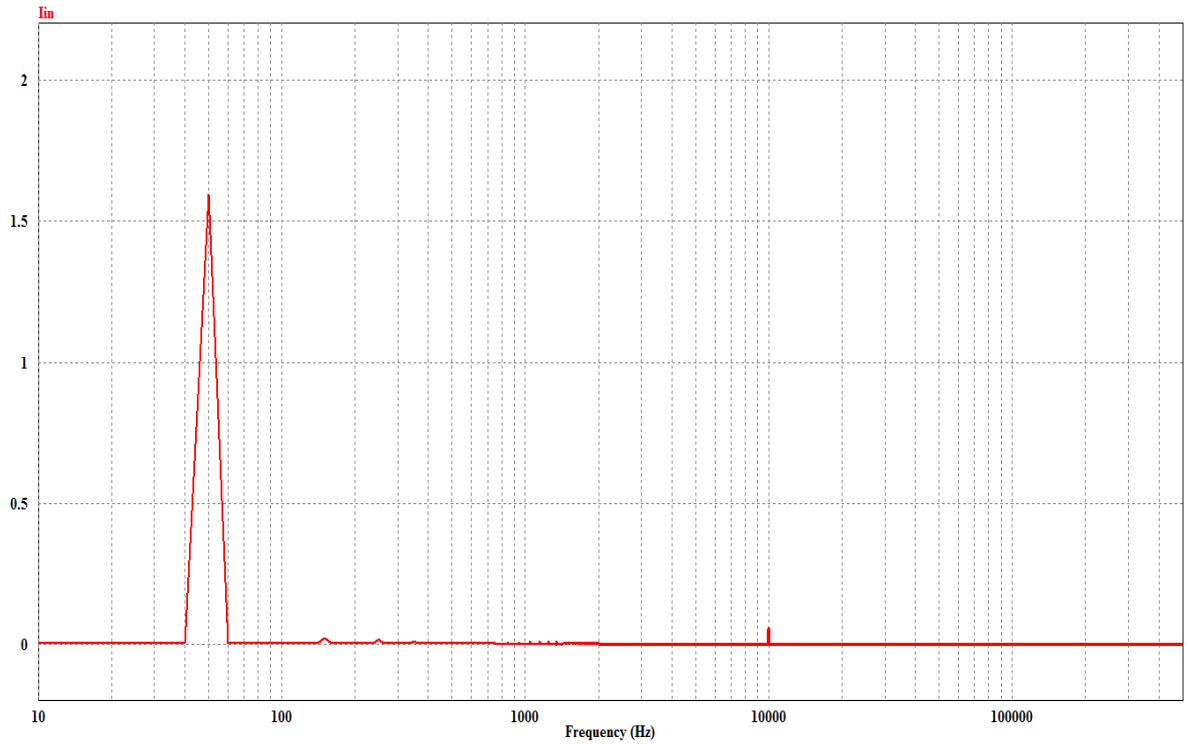


Fig.6.34 Input current spectrum of conventional SEPIC converter at f_s = 10 KHz. D = 0.3

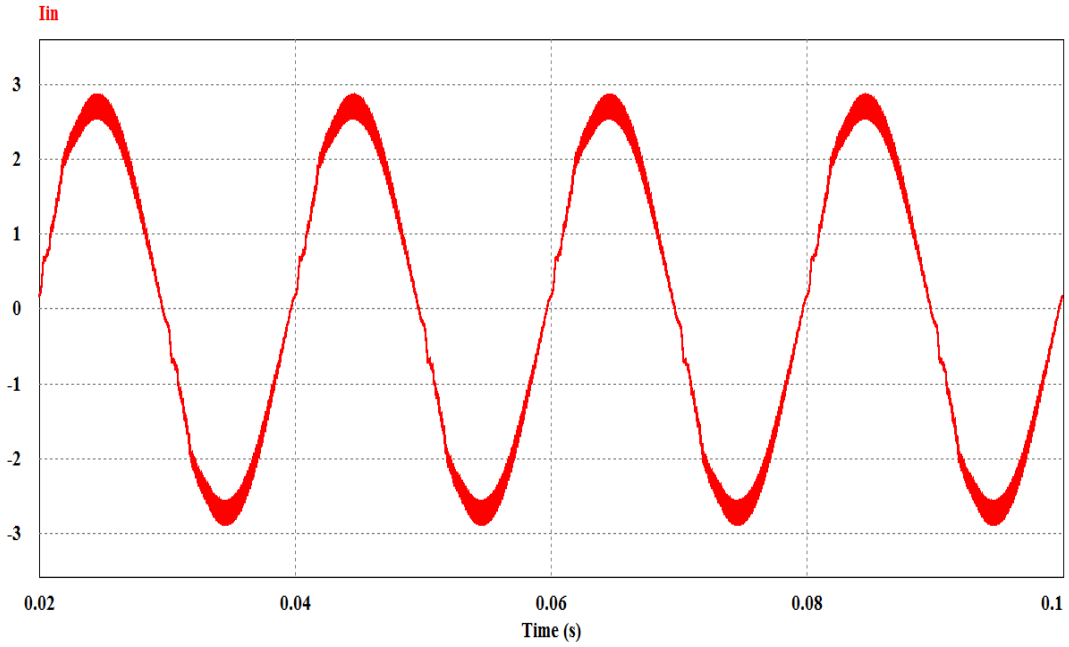


Fig.6.35 Input current of conventional SEPIC converter at f_s = 10 KHz. D = 0.4

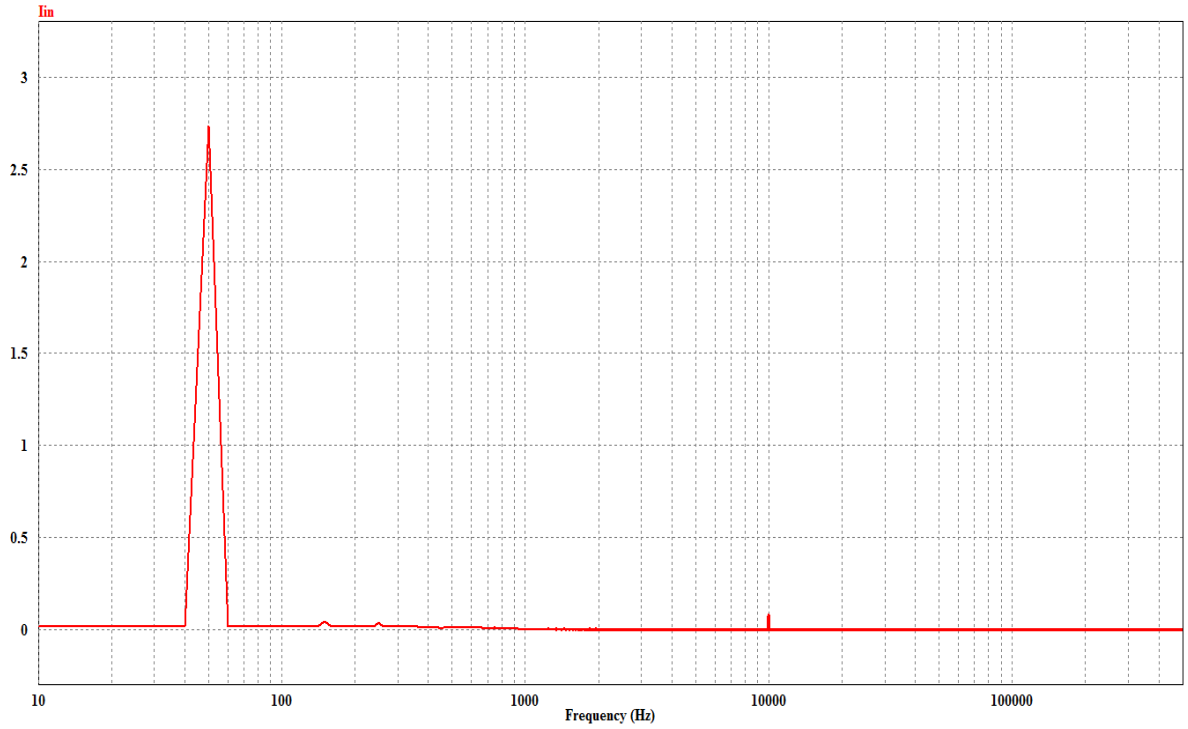


Fig.6.36 Input current spectrum of conventional SEPIC converter at f_s = 10 KHz. D = 0.4

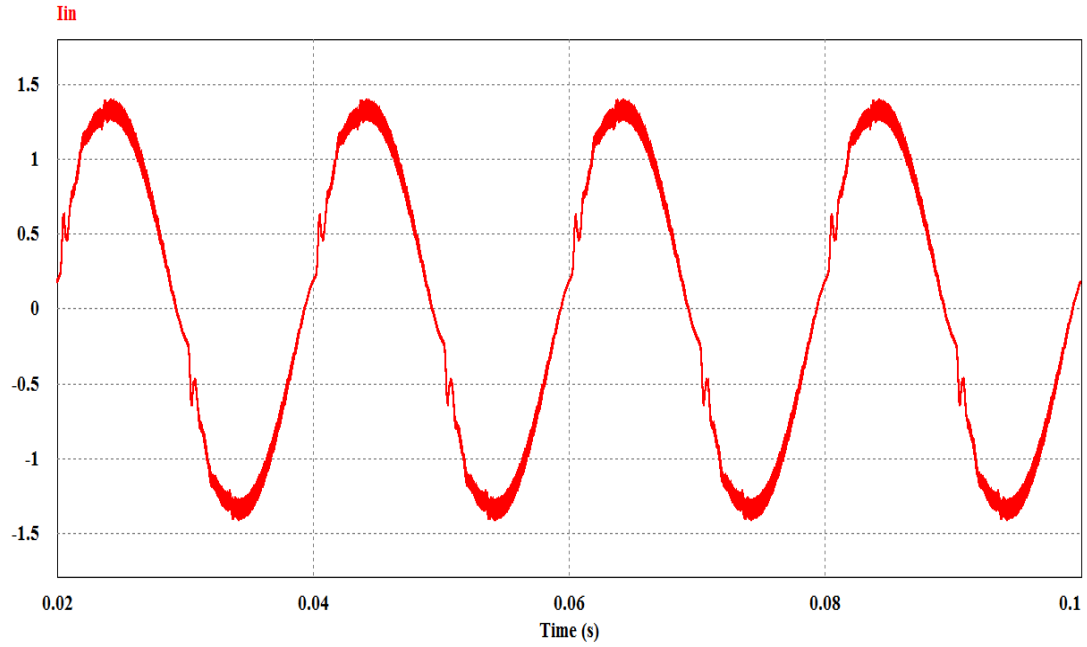


Fig.6.37 Input current of conventional SEPIC converter at f_s = 12 KHz. D = 0.3

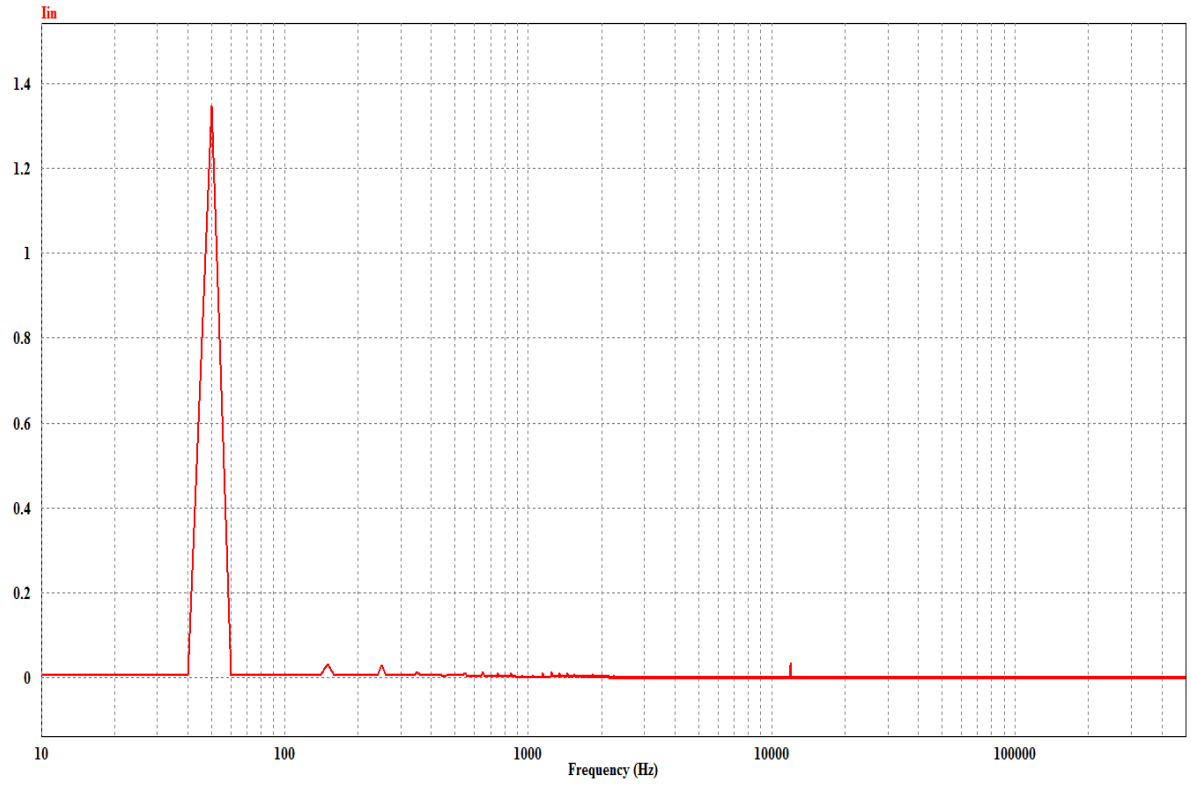


Fig.6.38 Input current spectrum of conventional SEPIC converter at f_s = 12 KHz. D = 0.3

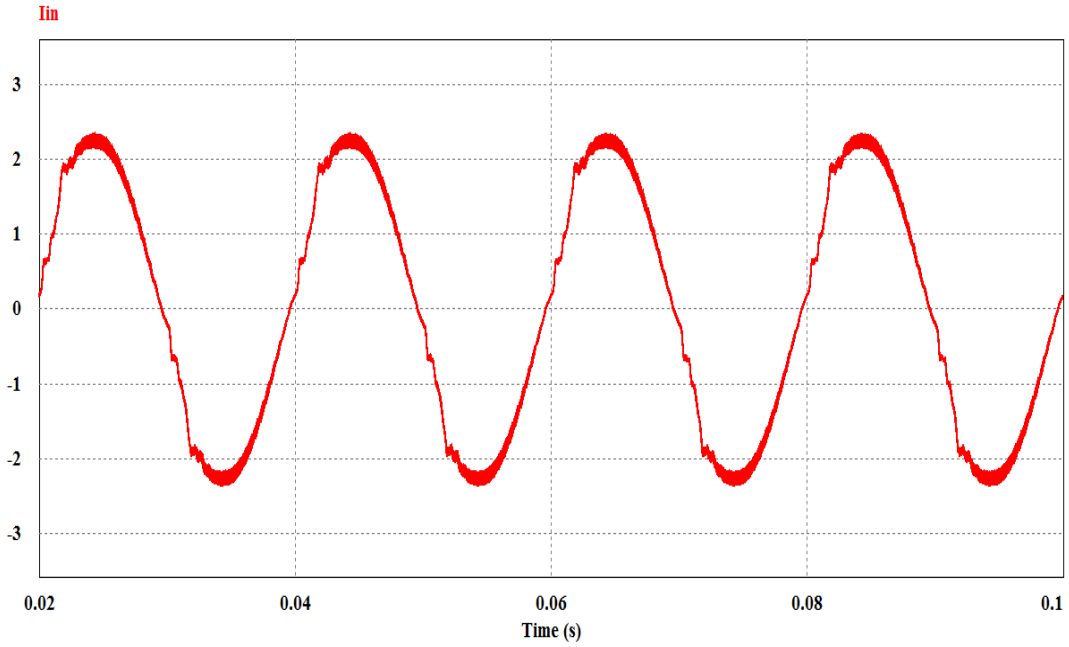


Fig.6.39 Input current of conventional SEPIC converter at f_s = 12 KHz. D = 0.4

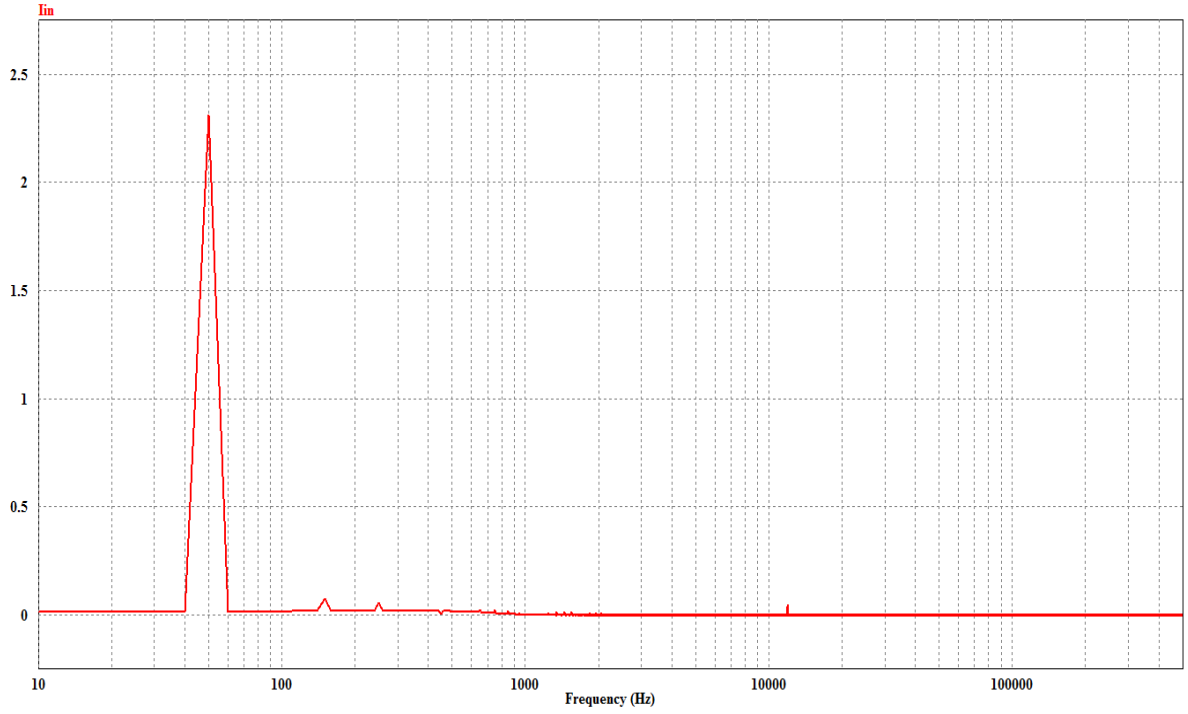


Fig.6.40 Input current spectrum of conventional SEPIC converter at f_s = 12 KHz. D = 0.4

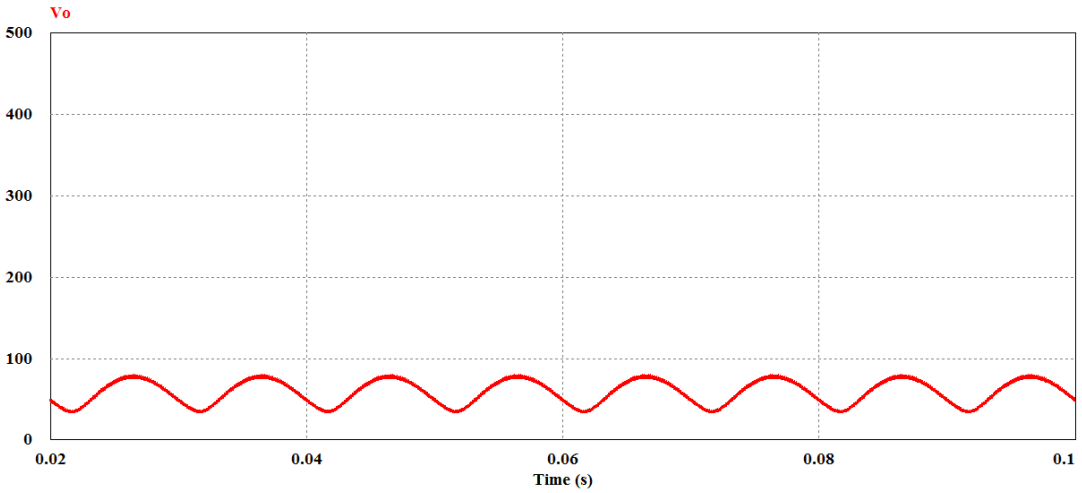


Fig.6.41 Output voltage waveform of proposed SEPIC converter at f_s = 8 KHz. D = 0.1

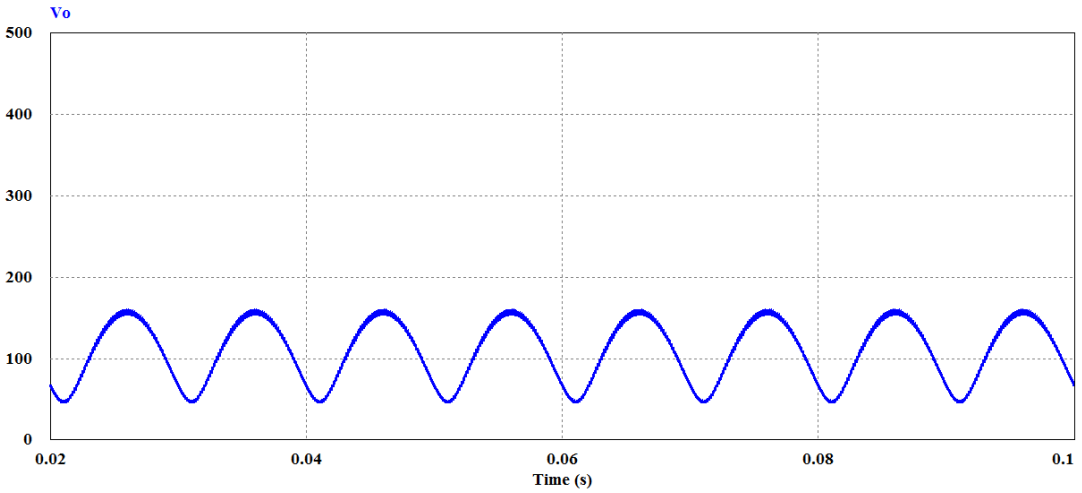


Fig.6.42 Output voltage waveform of proposed SEPIC converter at f_s = 8 KHz. D = 0.2

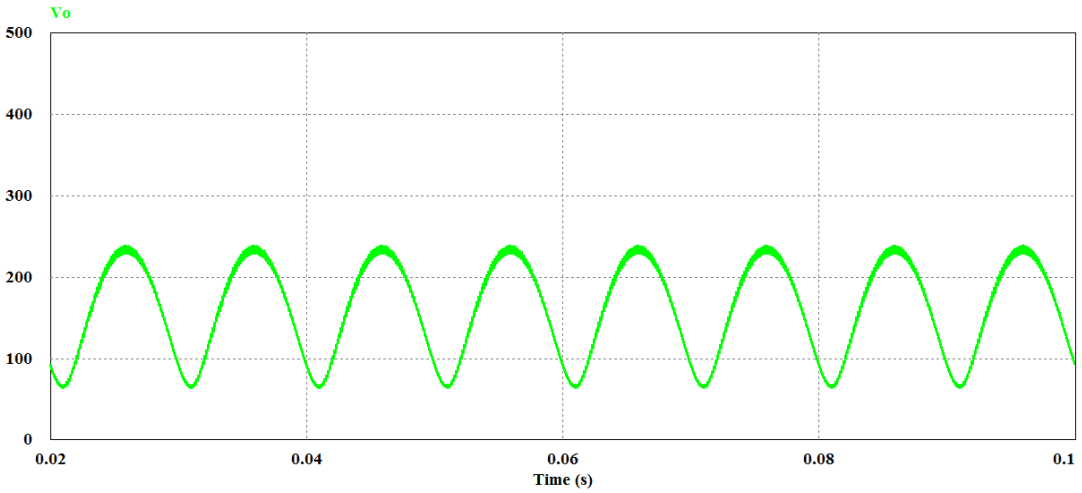


Fig.6.43 Output voltage waveform of proposed SEPIC converter at f_s = 8 KHz. D = 0.3

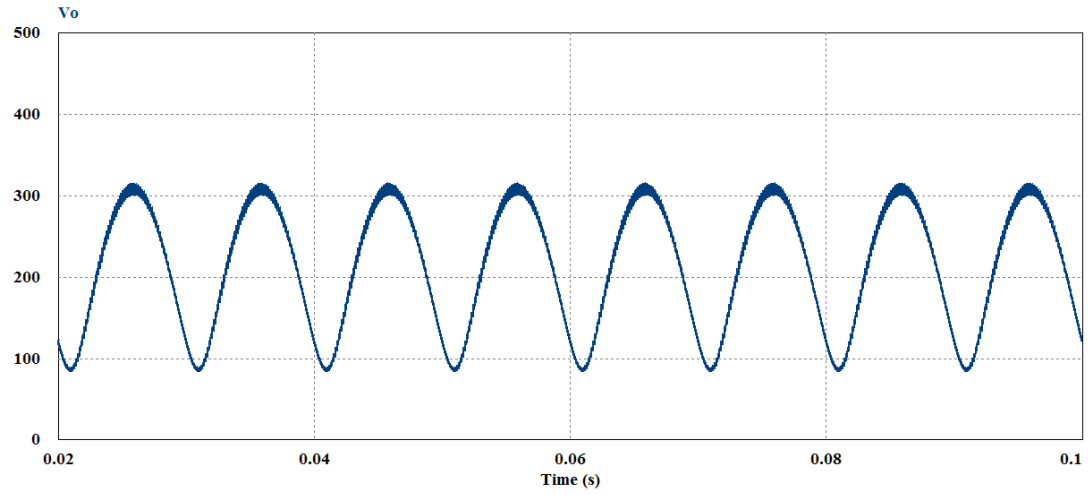


Fig.6.44 Output voltage waveform of proposed SEPIC converter at f_s = 8 KHz. D = 0.4

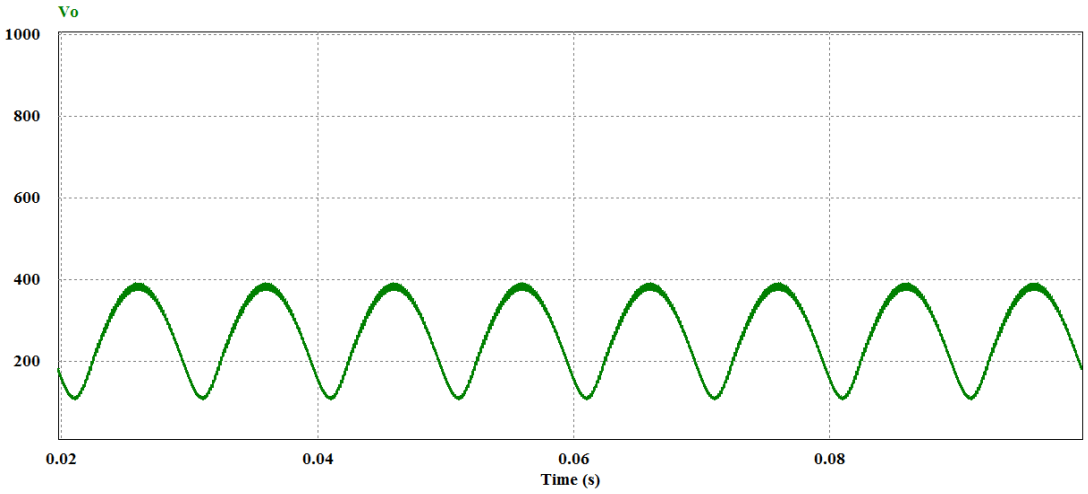


Fig.6.45 Output voltage waveform of proposed SEPIC converter at f_s = 8 KHz. D = 0.5

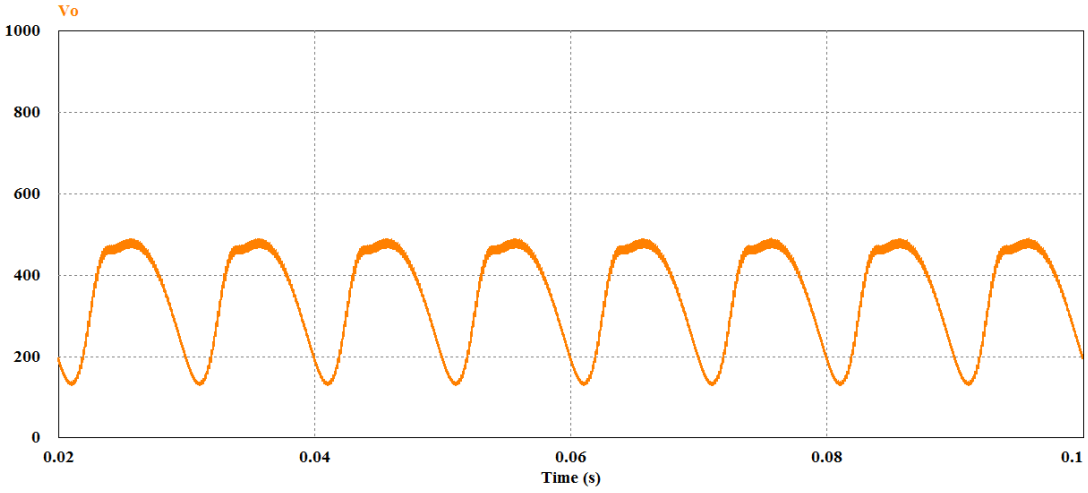


Fig.6.46 Output voltage waveform of proposed SEPIC converter at f_s = 8 KHz. D = 0.6

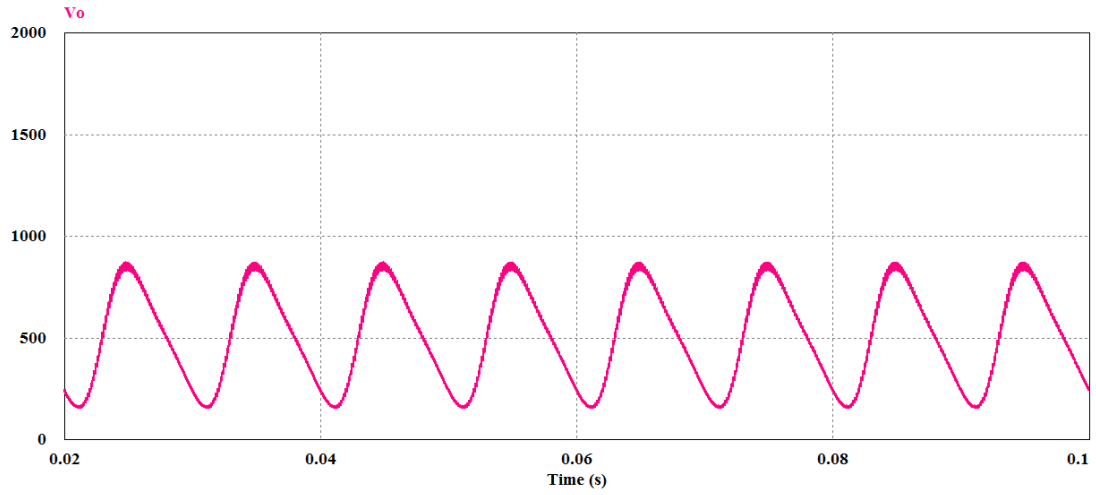


Fig.6.47 Output voltage waveform of proposed SEPIC converter at f_s = 8 KHz. D = 0.7

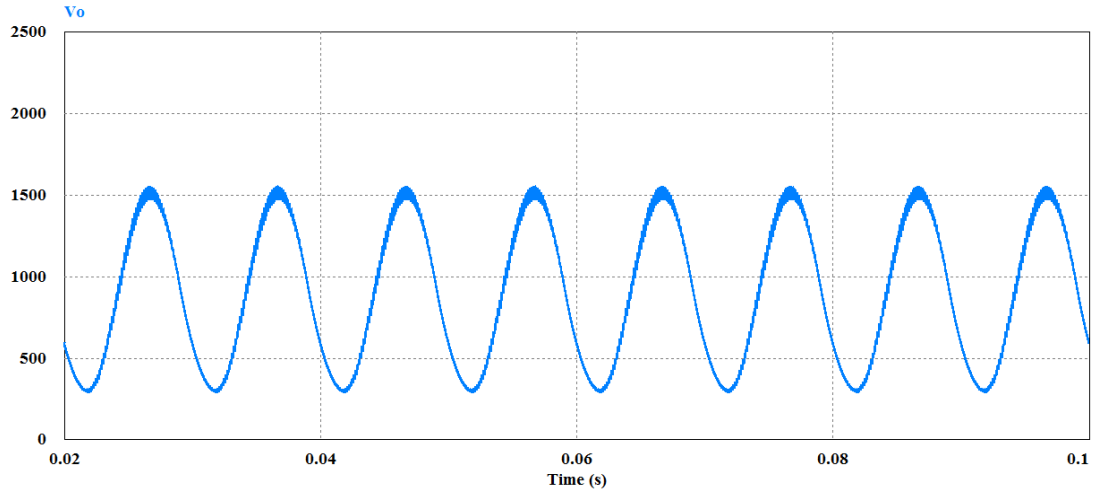


Fig.6.48 Output voltage waveform of proposed SEPIC converter at f_s = 8 KHz. D = 0.8

6.3.3 Quantitative Comparison

The performances of the proposed single phase SEPIC AC-DC converter scheme is compared with conventional one having DC-DC converter at the output. For comparison, results are evaluated in terms of THD (%) of input current, input power factor and efficiency (%). The results of comparisons are presented in Figs.6.49 to 6.63.

The bar chart shown in Figs. 6.49 to 6.53 indicates that the THD (%) of input current of the proposed converter is better than the conventional one for almost all duty cycles at different frequencies. The proposed converter also exhibits high input power factor at all duty cycles compared to conventional one which is presented in Figs. 6.54 to 6.58. In terms of efficiency,

the proposed SEPIC converter has almost same efficiency as the conventional one which is presented in Figs. 6.59 to 6.63.

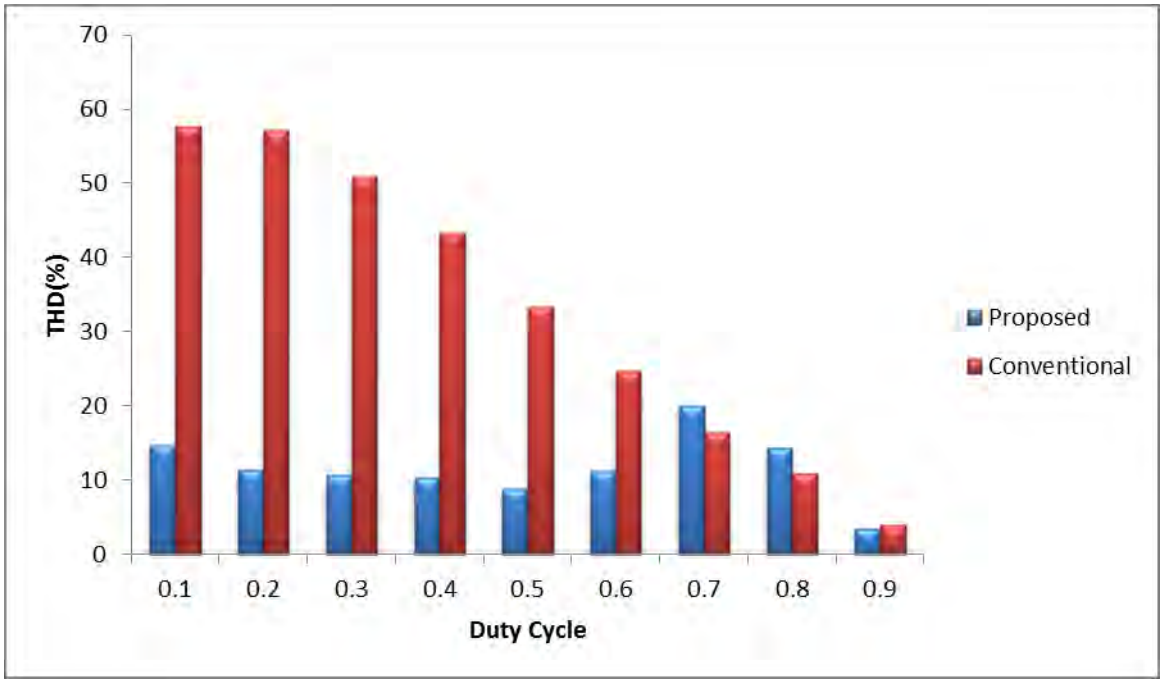


Fig. 6.49. Comparison of input current THD (%) between conventional and proposed scheme at f_s = 4 kHz. and R_Load = 100Ω.

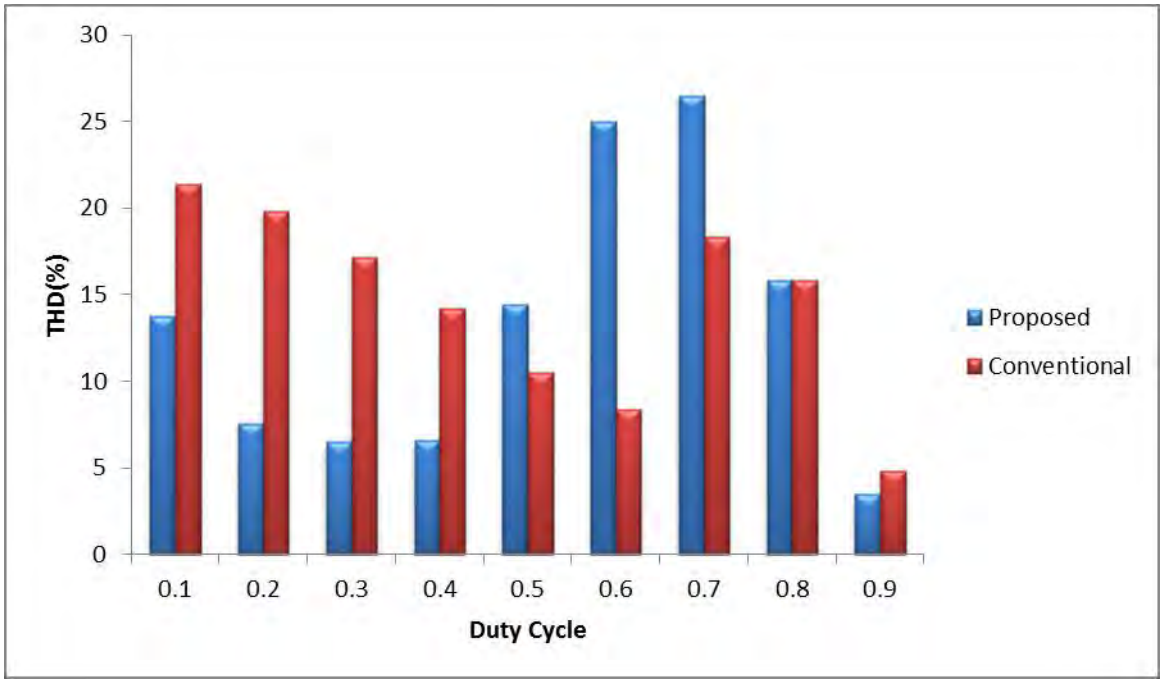


Fig. 6.50. Comparison of input current THD (%) between conventional and proposed scheme at f_s = 6 kHz. and R_Load = 100Ω.

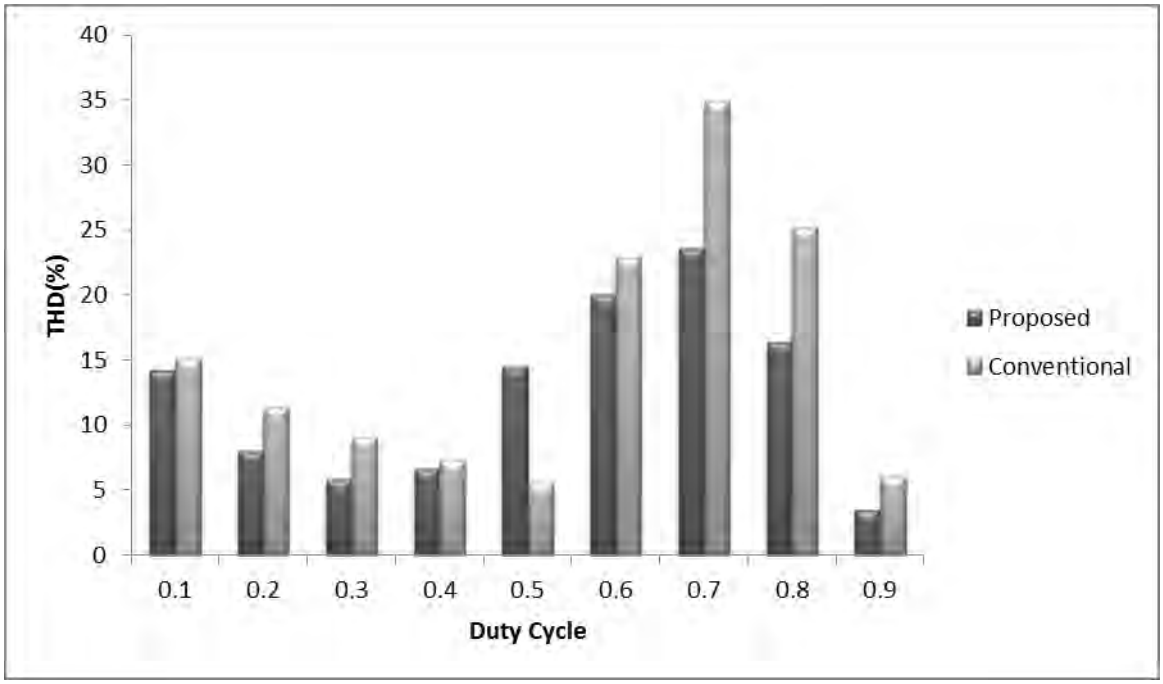


Fig. 6.51. Comparison of input current THD (%) between conventional and proposed scheme at f_s = 8 kHz. and R_Load = 100Ω.

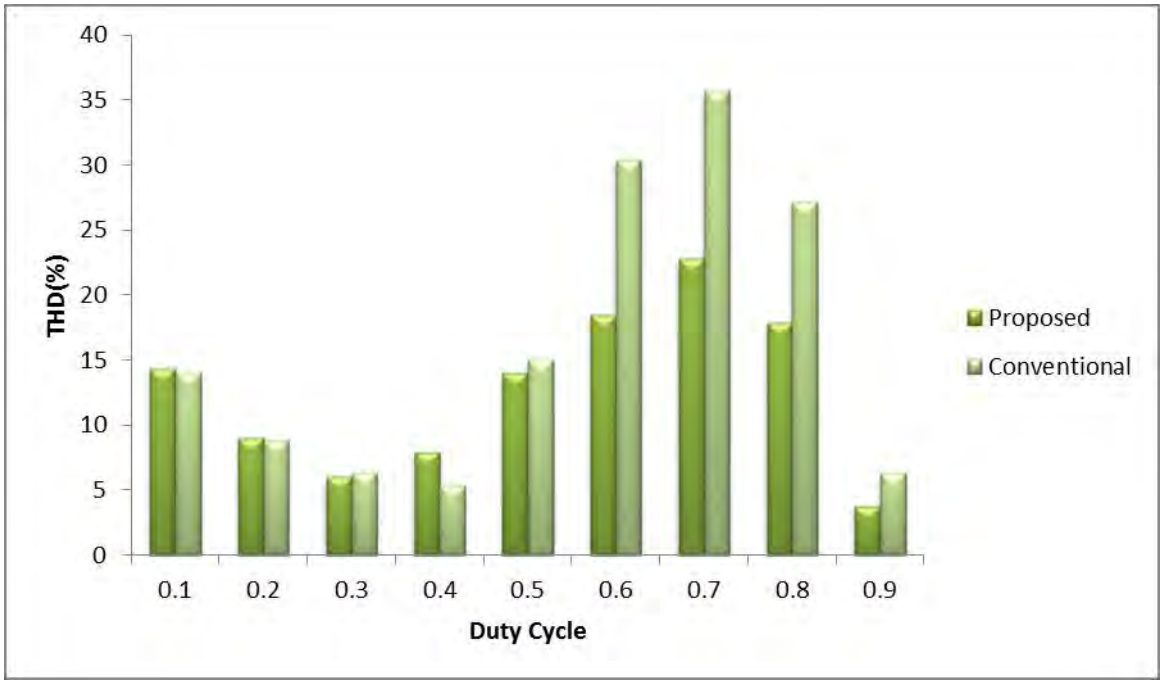


Fig. 6.52. Comparison of input current THD (%) between conventional and proposed scheme at f_s = 10 kHz. and R_Load = 100Ω.

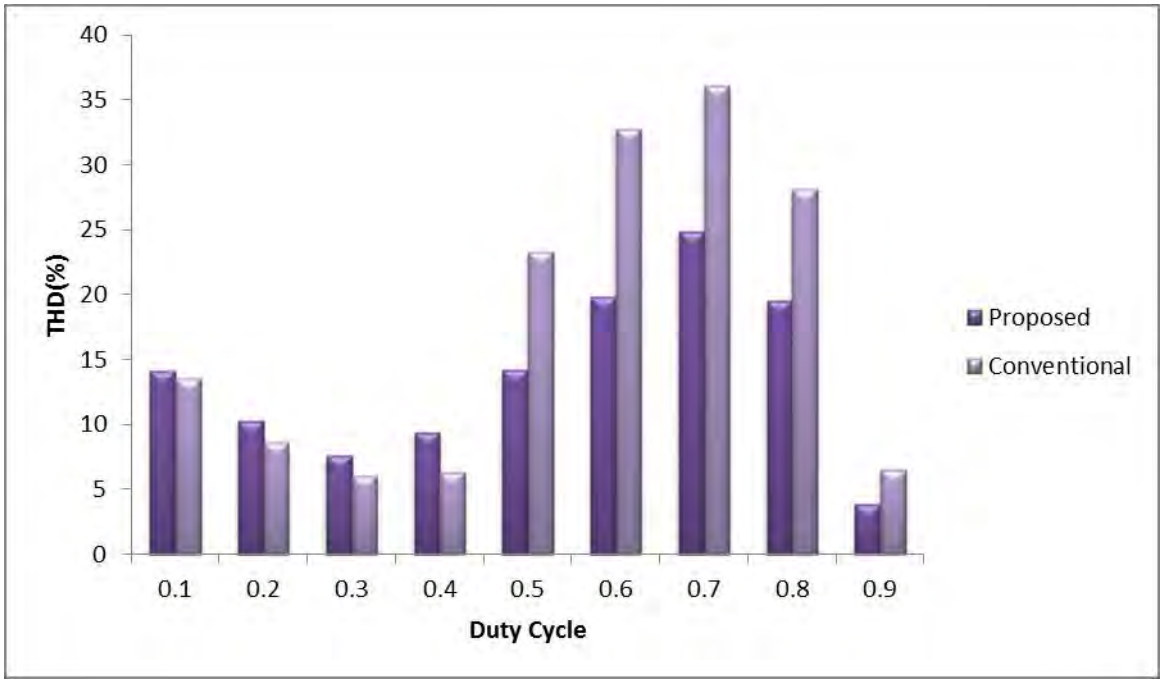


Fig. 6.53. Comparison of input current THD (%) between conventional and proposed scheme at f_s = 12 kHz. and R_Load = 100Ω.

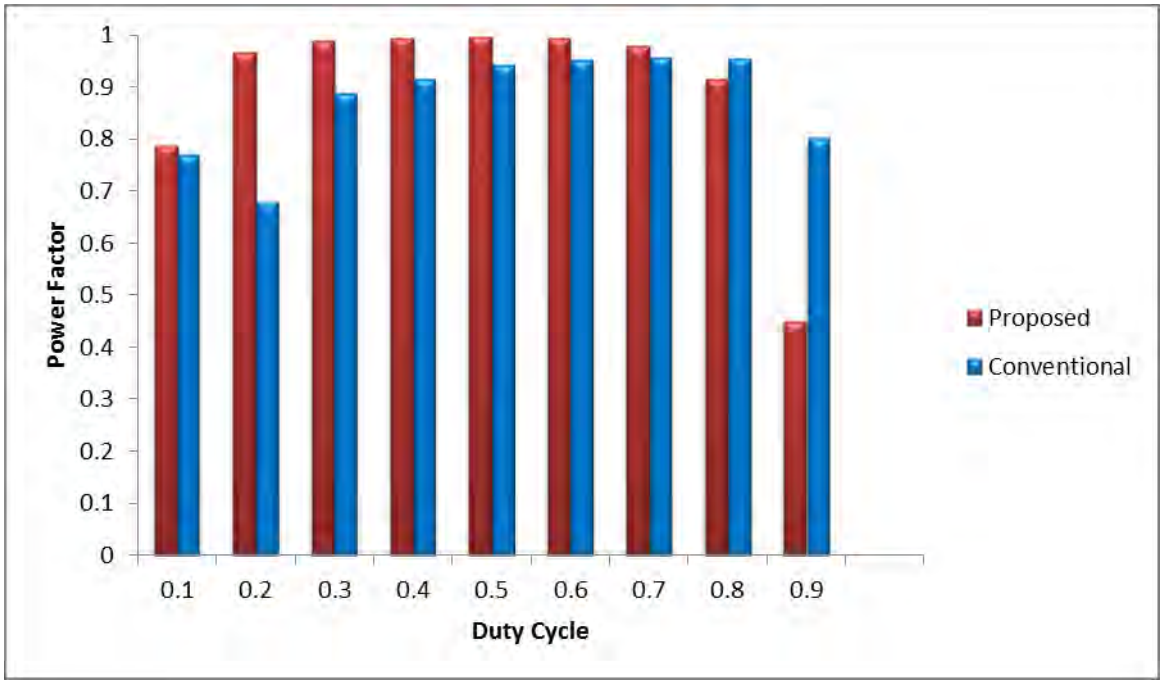


Fig. 6.54. Comparison of input power factor between conventional and proposed scheme at f_s = 4 kHz. and R_Load = 100 Ω.

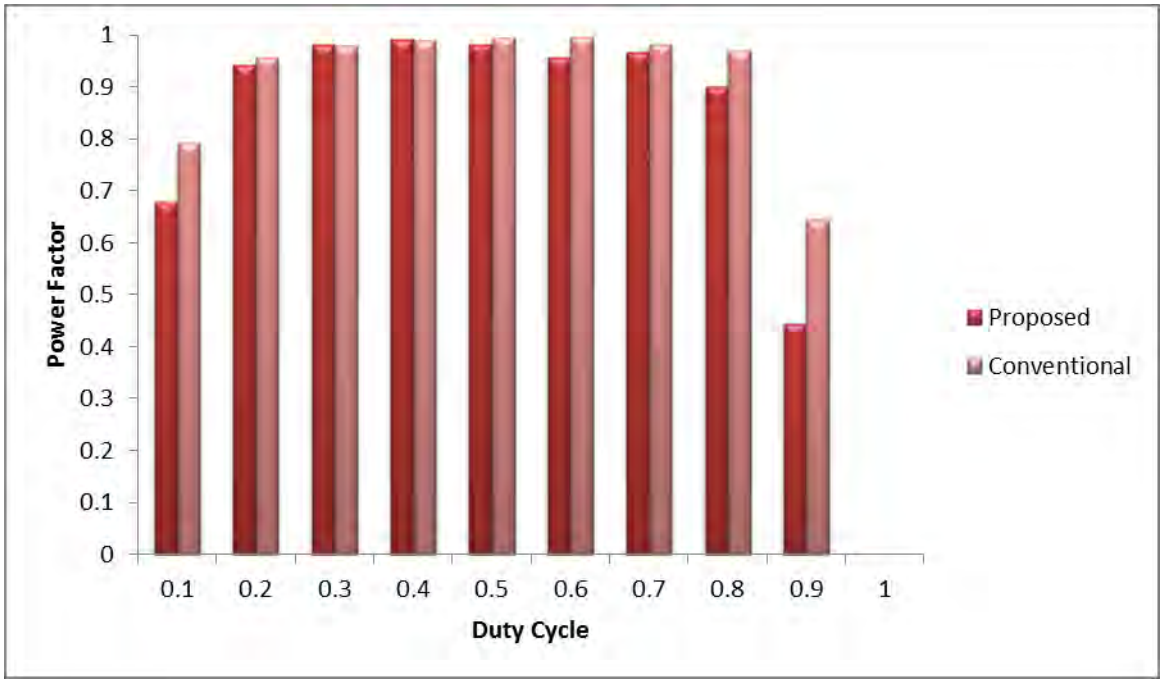


Fig. 6.55. Comparison of input power factor between conventional and proposed scheme at f_s = 6 kHz. and R_Load = 100 Ω.

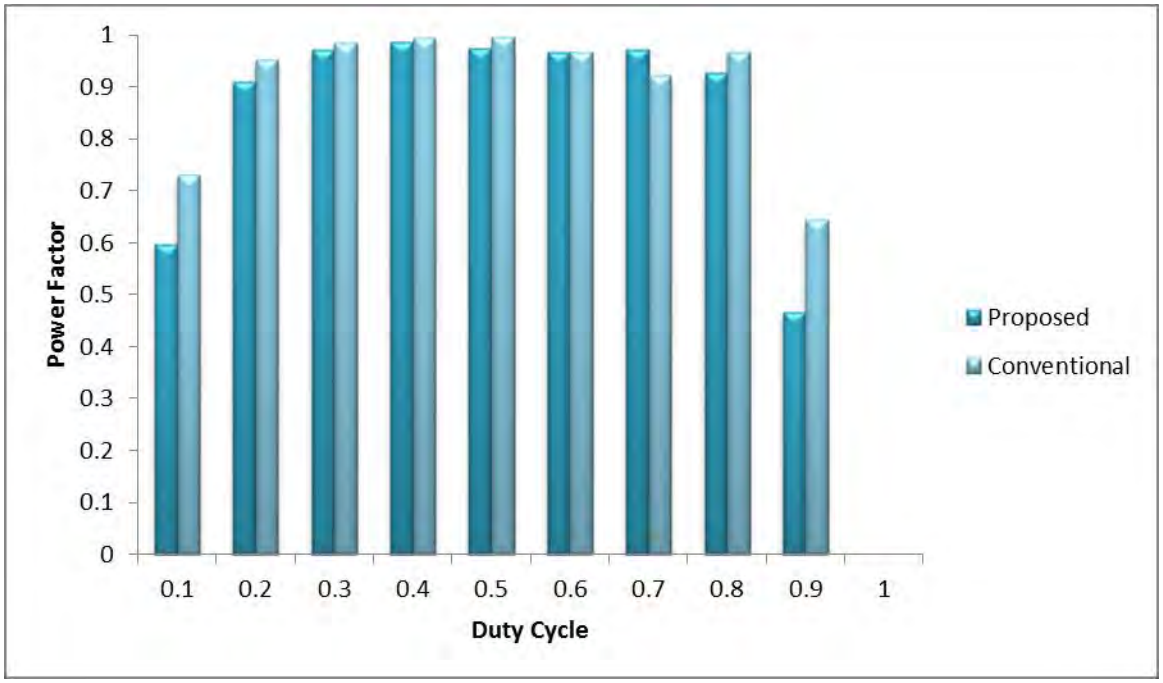


Fig. 6.56. Comparison of input power factor between conventional and proposed scheme at f_s = 8 kHz. and R_Load = 100 Ω.

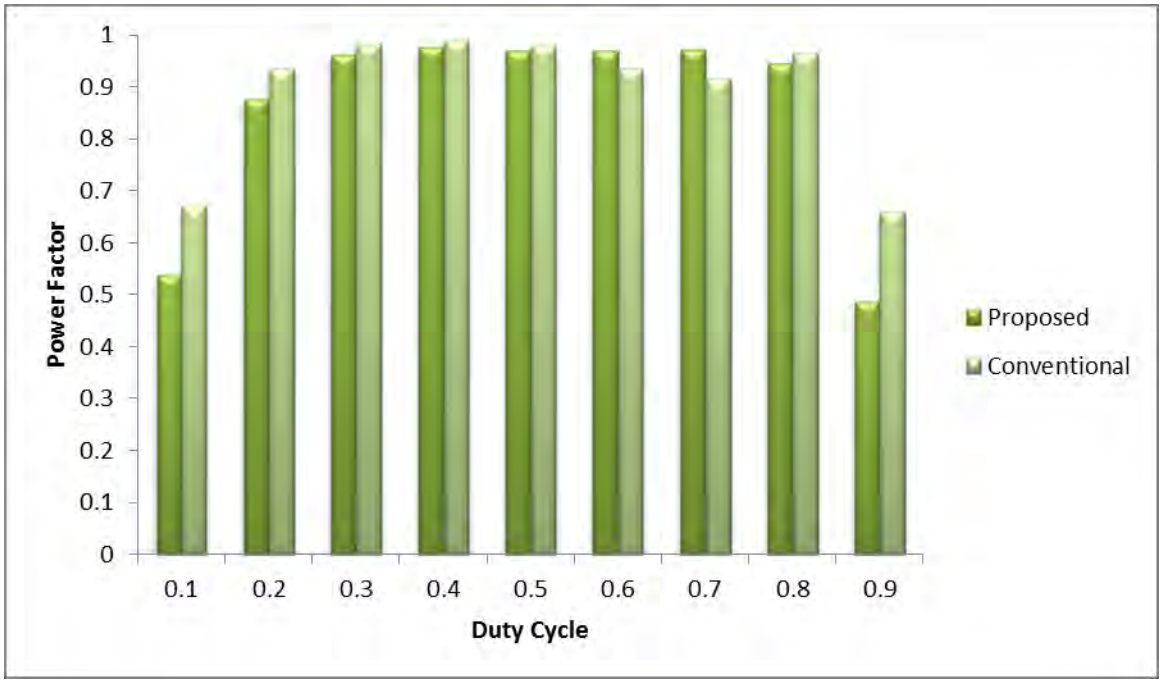


Fig. 6.57. Comparison of input power factor between conventional and proposed scheme at f_s = 10 kHz. and R_Load = 100 Ω.

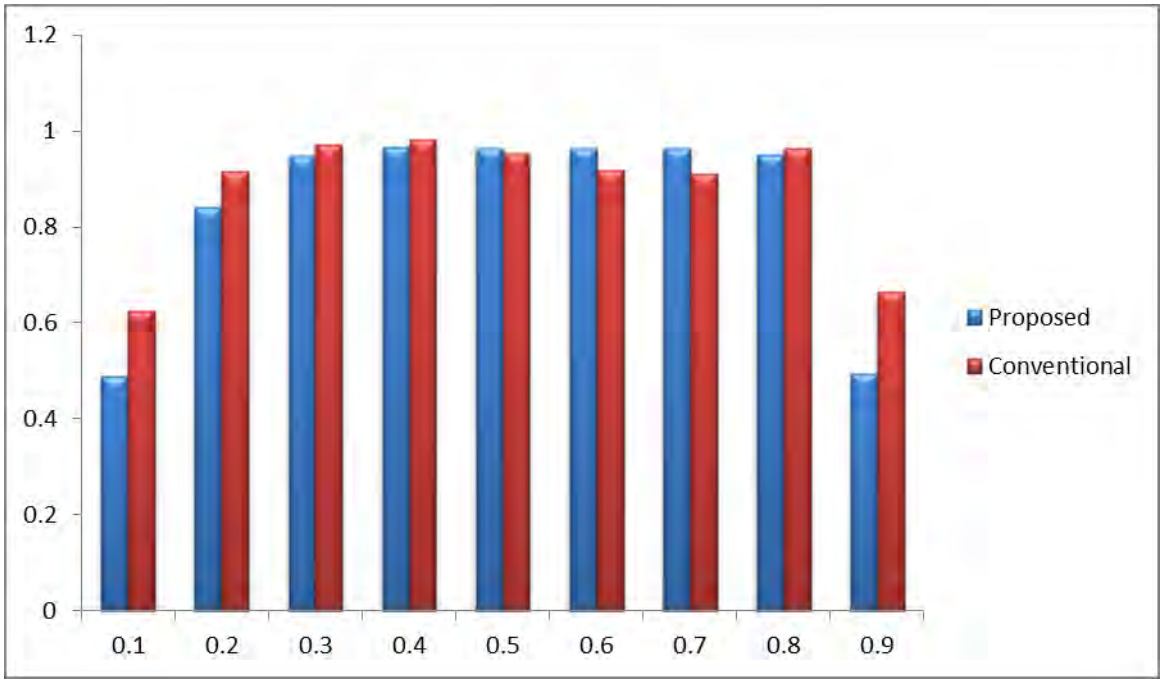


Fig. 6.58. Comparison of input power factor between conventional and proposed scheme at f_s = 12 kHz. and R_Load = 100 Ω.

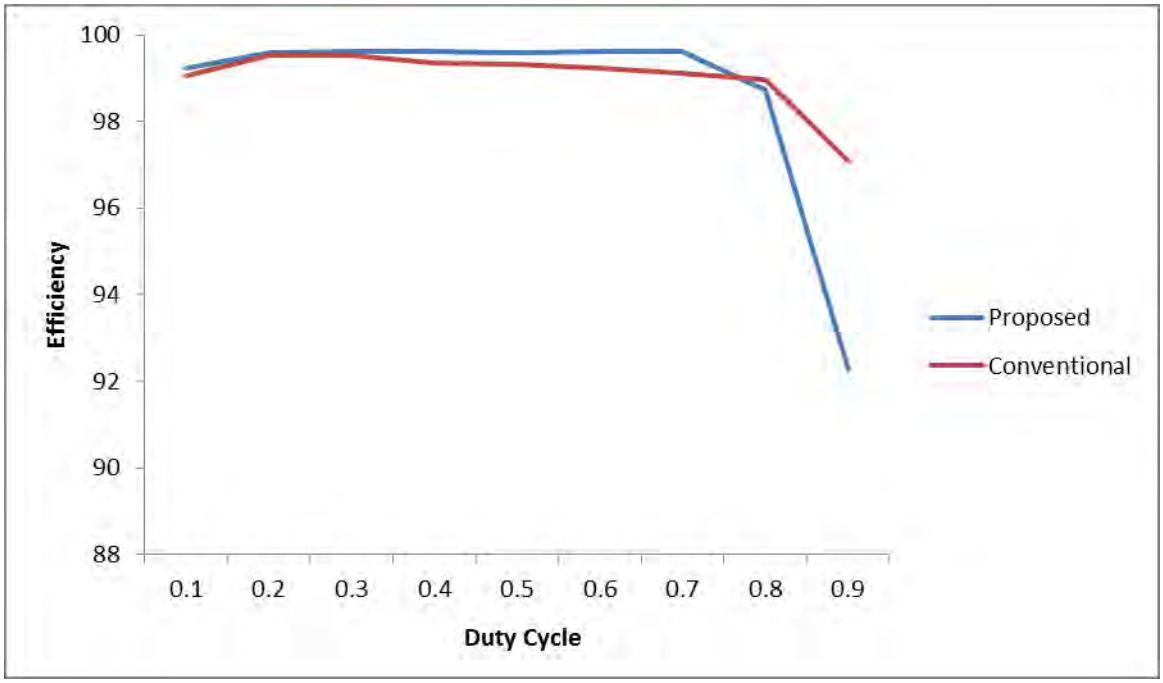


Fig. 6.59. Comparison of efficiency (%) between conventional and proposed scheme at f_s = 4 kHz. and R_Load = 100 Ω.

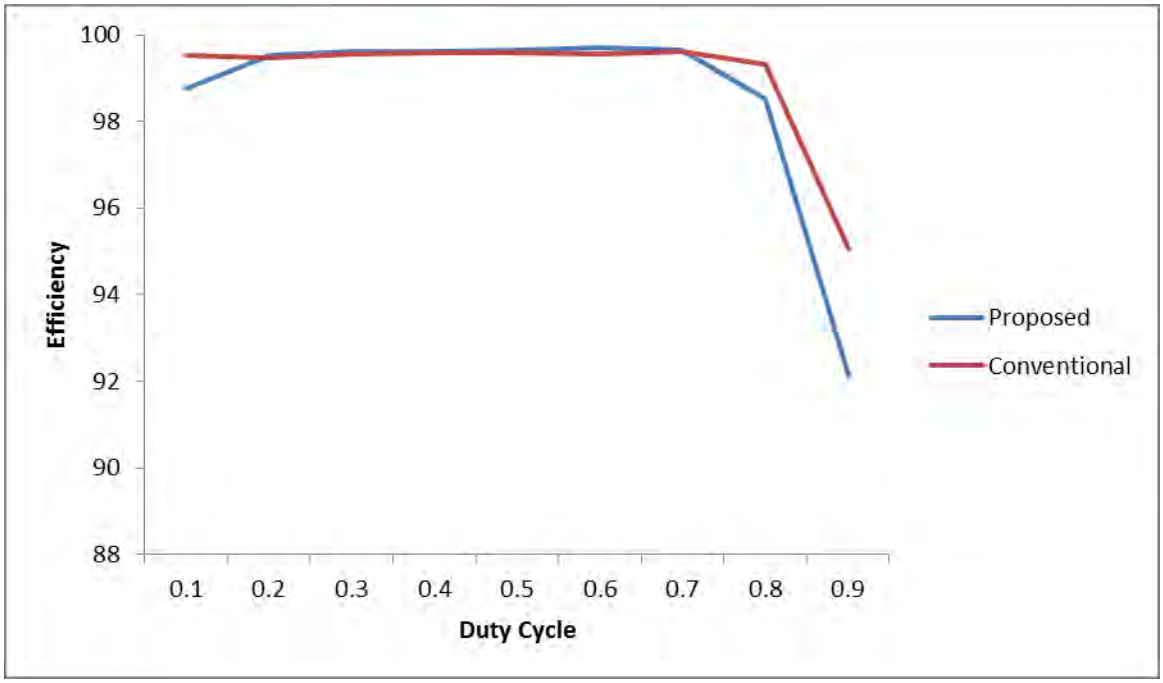


Fig. 6.60. Comparison of efficiency (%) between conventional and proposed scheme at f_s = 6 kHz. and R_Load = 100 Ω.

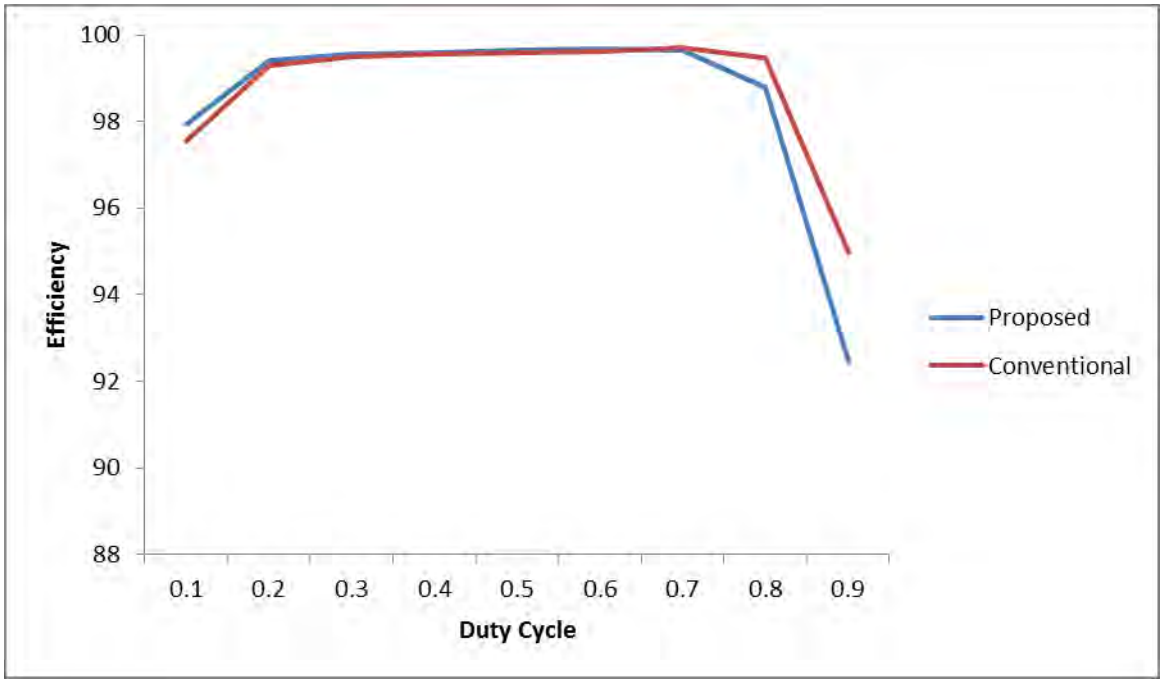


Fig. 6.61. Comparison of efficiency (%) between conventional and proposed scheme at f_s = 8 kHz. and R_Load = 100 Ω.

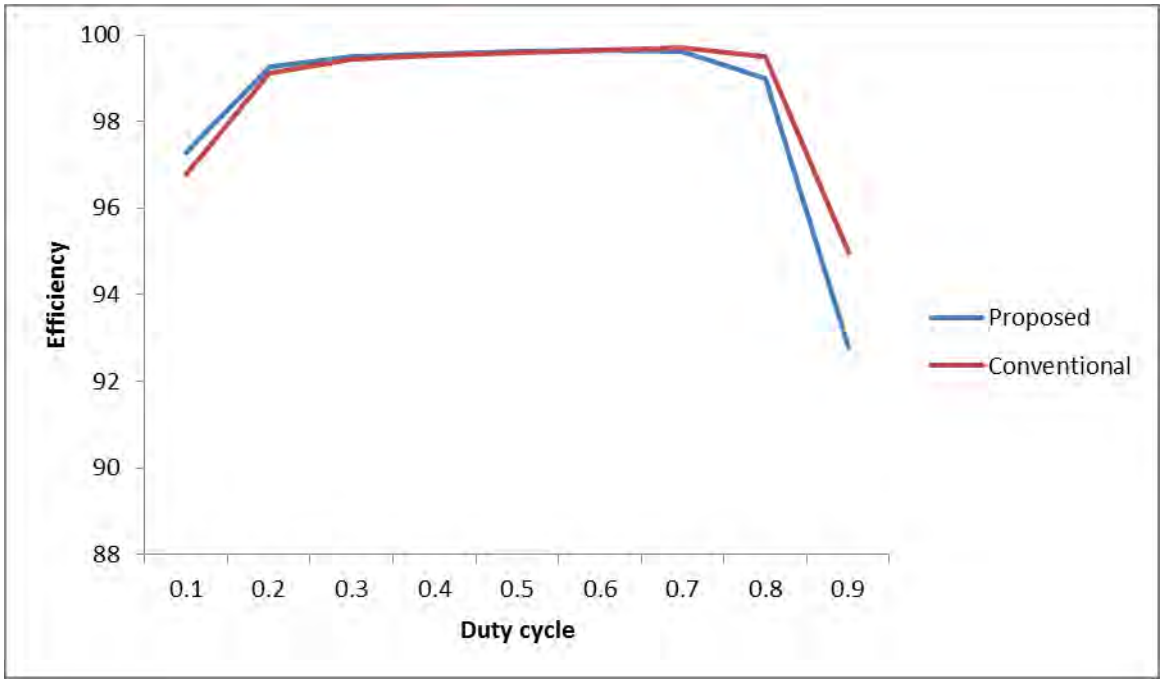


Fig. 6.62. Comparison of efficiency (%) between conventional and proposed scheme at f_s = 10 kHz. and R_Load= 100 Ω.

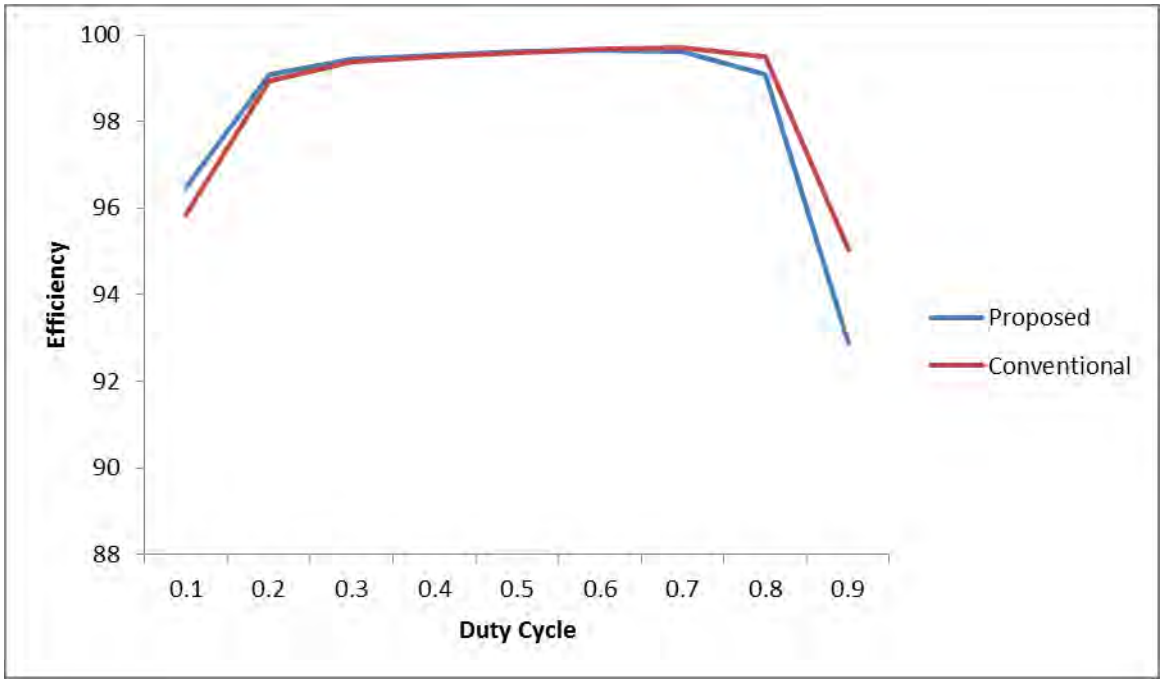


Fig. 6.63. Comparison of efficiency (%) between conventional and proposed scheme at f_s =12 kHz. and R_Load= 100 Ω.

Numerical values of simulation data for input current THD (%), input current power factor, efficiency (%) and output power at frequency 4 to 12 KHz. for 0.1-0.9 duty cycles are given in Table 6.1.From this table it is observed that input current THD (%), input current power factor, efficiency (%) are in desirable limit.

Table 6.1 Numerical values of simulation data for proposed AC-DC SEPIC converter

Frequency (Hz.)	Duty Cycle	Power Factor	Effeciency (%)	THD (%)	Average Output Voltage	Output Power
4000	**0.1**	0.786	99.23	14.78	68	51.101
	0.2	0.968	99.59	11.33	127	184.715
	0.3	0.988	99.63	10.71	187	401.217
	0.4	0.993	99.62	10.35	244	687.476
	0.5	0.996	99.59	8.88	291	979.204
	0.6	0.994	99.61	11.17	335	1301.8
	0.7	0.98	99.62	19.97	452	2473
	0.8	0.915	98.72	14.42	671	5273
	0.9	0.45	92.26	3.46	642	4671.9
5000	**0.1**	0.729	99	13.71	61	41.5669
	0.2	0.957	99.56	8.4	113	145.3359
	0.3	0.986	99.62	7.76	164	306.175
	0.4	0.993	99.63	7.7	212	513.245
	0.5	0.989	99.63	11.97	259	767.908

	0.6	0.959	99.67	26.13	335	1356.6
	0.7	0.969	99.65	25.6	479	2849.1
	0.8	0.904	98.62	15.71	687	5582.1
	0.9	0.445	92.18	3.45	639	4651.9
6000	**0.1**	0.679	98.75	13.77	57	35.326
	0.2	0.943	99.53	7.59	103	121.06
	0.3	0.983	99.61	6.54	148	251.539
	0.4	0.992	99.63	6.59	191	417.472
	0.5	0.982	99.64	14.45	238	649.359
	0.6	0.958	99.7	25	321	1238.5
	0.7	0.967	99.64	26.52	471	2776.8
	0.8	0.901	98.53	15.87	690	5631.3
	0.9	0.443	92.13	3.48	638	4642.1
7000	**0.1**	0.636	98.5	13.98	53	30.876
	0.2	0.928	99.5	7.626	96	104.331
	0.3	0.978	99.6	6.01	137	215.221
	0.4	0.99	99.63	6.19	177	355.876
	0.5	0.977	99.66	14.69	225	580.866
	0.6	0.965	99.7	22	307	1129.1
	0.7	0.97	99.64	25.18	450	2513.6
	0.8	0.913	98.66	16.15	677	5450
	0.9	0.447	92.01	3.4	640	4681.4
8000	**0.1**	0.598	97.92	14.18	51	27.487
	0.2	0.911	99.4	7.98	90	91.97
	0.3	0.973	99.55	5.82	129	188.982
	0.4	0.986	99.59	6.58	166	312.924
	0.5	0.974	99.66	14.5	214	527.955
	0.6	0.968	99.68	20.02	295	1033
	0.7	0.973	99.64	23.6	430	2278
	0.8	0.927	98.79	16.37	659	5180
	0.9	0.466	92.45	3.44	652	4854.6
9000	**0.1**	0.566	97.81	14.25	48	24.878
	0.2	0.894	99.38	8.46	86	82.484
	0.3	0.968	99.56	5.79	122	169.015
	0.4	0.982	99.61	7.2	157	281.309
	0.5	0.972	99.66	14.266	207	492.422
	0.6	0.969	99.68	18.911	285	964.969
	0.7	0.974	99.63	22.68	415	2115
	0.8	0.937	98.93	16.8	645	4980
	0.9	0.478	92.69	3.57	659	4970

10000	**0.1**	0.537	97.27	14.3	46	22.7139
	0.2	0.877	99.25	8.97	82	74.878
	0.3	0.961	99.49	6.066	116	153.189
	0.4	0.977	99.57	7.94	150	256.7216
	0.5	0.97	99.63	14.03	199	456.2866
	0.6	0.969	99.66	18.45	276	899.2597
	0.7	0.973	99.61	22.8	403	1984.2
	0.8	0.944	99.01	17.88	635	4858.9
	0.9	0.486	92.77	3.72	664	5042.9
11000	**0.1**	0.511	97.04	14.22	45	20.9761
	0.2	0.86	99.21	9.57	78	68.695
	0.3	0.954	99.5	6.76	111	140.4413
	0.4	0.971	99.58	8.65	145	237.481
	0.5	0.968	99.64	13.82	194	433.477
	0.6	0.967	99.66	18.83	270	857.7859
	0.7	0.97	99.63	23.63	394	1902.2
	0.8	0.948	99.08	18.76	629	4791.5
	0.9	0.491	92.87	3.79	667	5084.4
12000	**0.1**	0.488	96.47	14.15	43	19.459
	0.2	0.842	99.08	10.32	75	63.515
	0.3	0.947	99.44	7.62	107	129.763
	0.4	0.966	99.54	9.34	140	221.592
	0.5	0.965	99.62	14.17	189	409.716
	0.6	0.963	99.64	19.88	264	817.532
	0.7	0.965	99.61	24.91	387	1835.1
	0.8	0.95	99.1	19.54	625	4738.4
	0.9	0.494	92.87	3.865	668	5109.8

6.3.4. Performances under Load Variation

The proposed and conventional both circuits are subjected to load variation at frequency 8 KHz. and 30 % duty cycle. The load resistance was varied from 50Ω to 500Ω and the performance was monitored in terms of input power factor and input current THD (%).

The comparisons of input current THD (%), input power factor and efficiency between the proposed and the conventional converter are presented in Figs. 6.64 to Fig. 6.66. The proposed converter gives low input current THD (%) with respect to the conventional circuit. The proposed circuit also has higher power factor than the conventional single-phase rectifier

for all load resistance. The efficiency of the proposed converter is also high in almost all duty cycles. Fig. 6.67 presents Output Voltage of the proposed converter at 8000Hz. D = 0.3 for different load resistance.

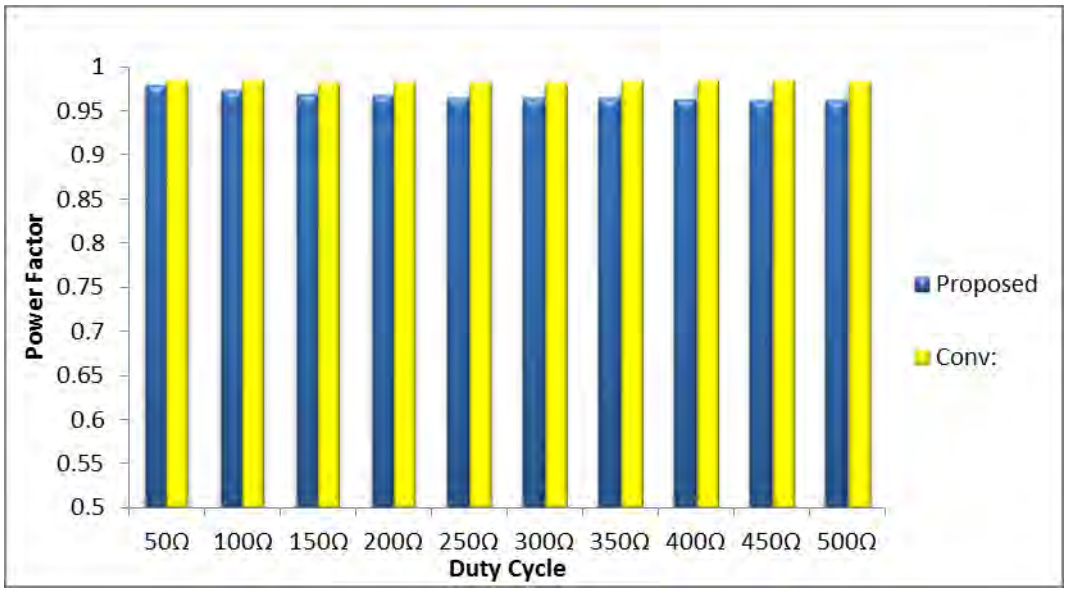


Fig. 6.64. Comparison of input power factor between conventional and proposed scheme with load variation at f_s = 8 kHz. and D = 0.3.

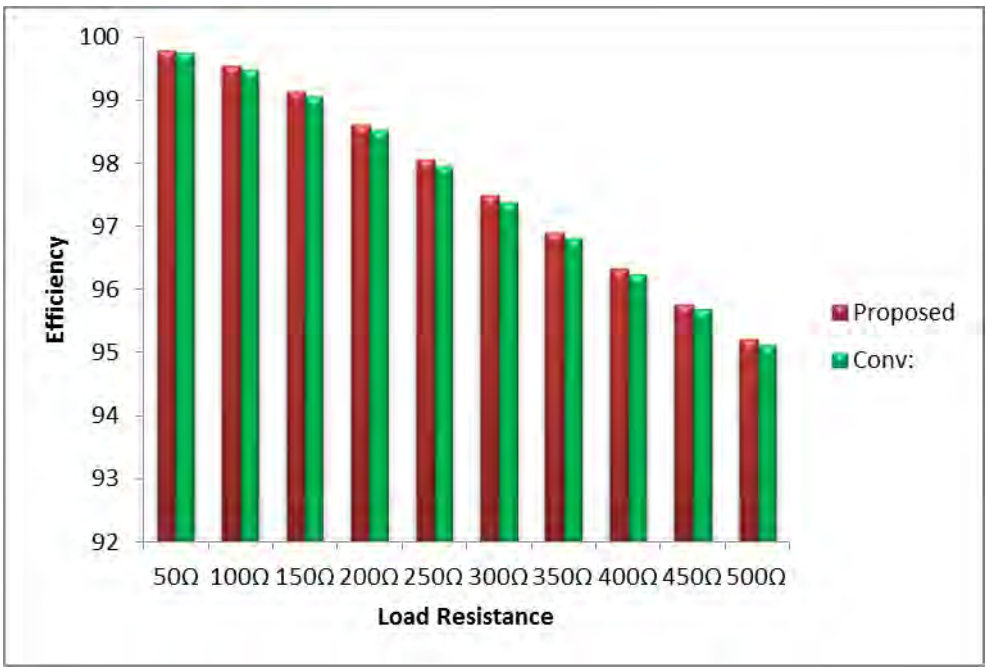


Fig. 6.65. Comparison of efficiency between conventional and proposed scheme with load variation at f_s = 8 kHz. and D = 0.3.

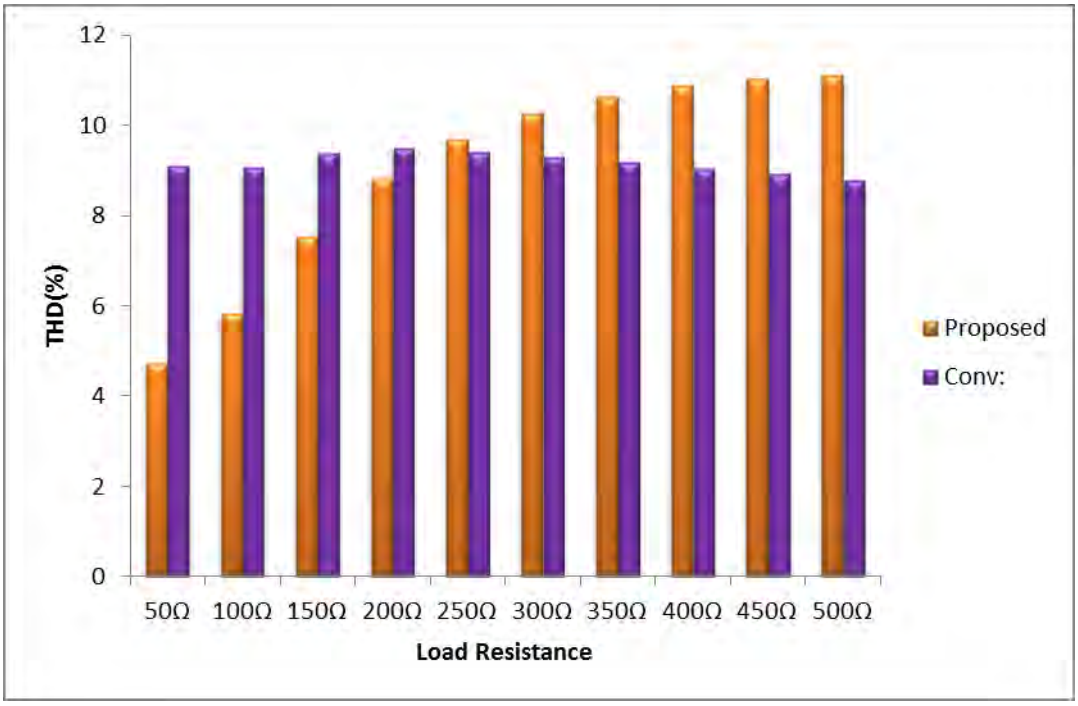


Fig. 6.66. Comparison of input current THD (%) between conventional and proposed scheme with load variation at f_s = 8 kHz. and D = 0.3

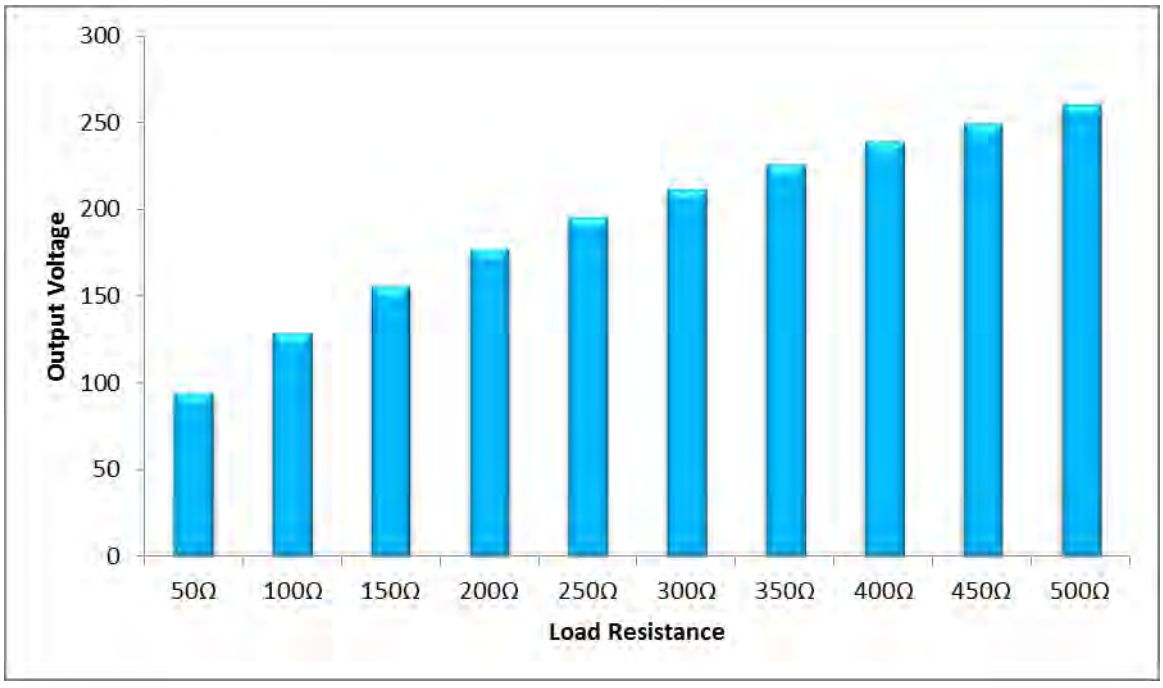


Fig. 6.67. Output Voltage of the proposed converter at f_s = 8000Hz. D = 0.3 with load variation.

6.4 The Proposed SEPIC Converter with Feedback Controller Circuit

It is observed in Fig. 6.67 that, the output voltage of the proposed SEPIC converter is changed with changing load values. For light load the output voltage is high and for heavy loads the output voltage decreases. This is not expected at high power application.

High power applications need regulated voltage under the variation of other parameters like load value. That's why feedback controller circuit is introduced to regulate the output voltage and to maintain good power factor and THD under the condition of load variation. Fig. 6.68 represents the block diagram of the total system which consists of the proposed converter with voltage and current controller at feedback path.

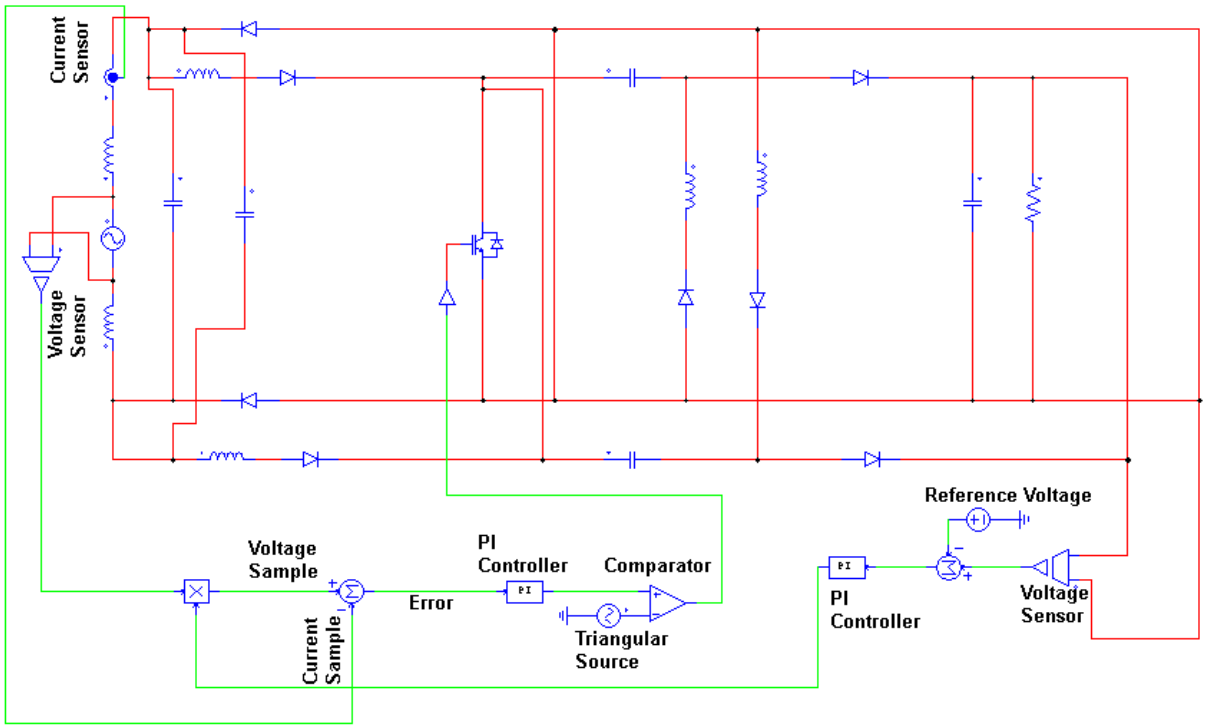


Fig.6.68 The Proposed SEPIC Converter with Feedback Controller Circuit.

Figs. 6.69 to 6.73 represent the waveform of input current and regulated output voltage for different load values. From the figures it is observed that the input current is nearly sinusoidal and the output voltage is also constant although load is changed.

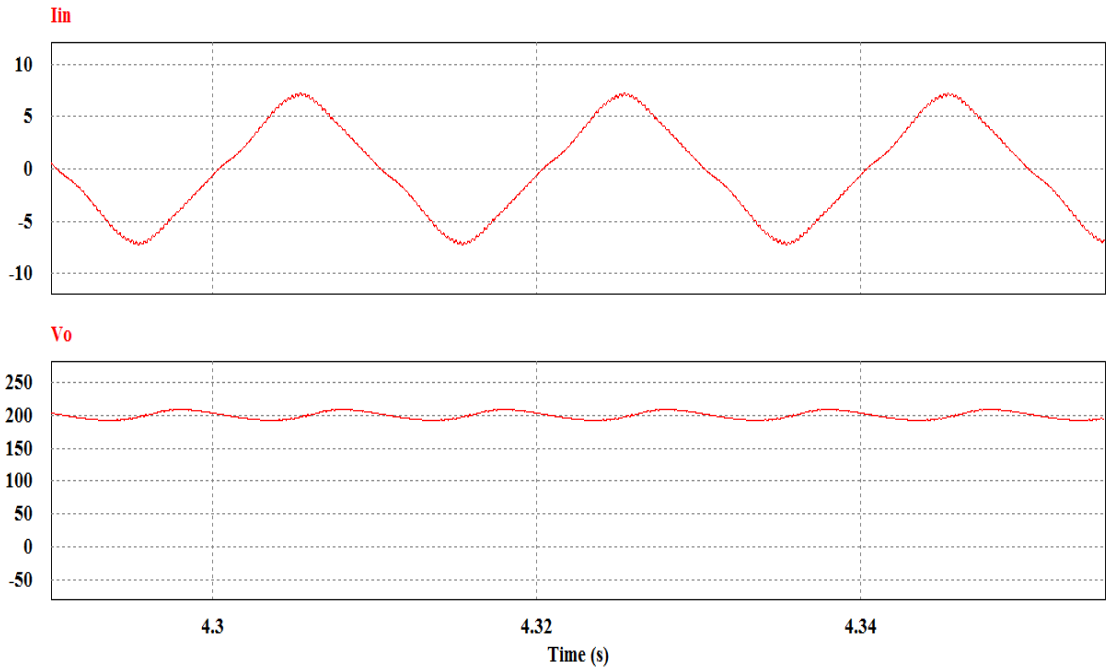


Fig.6.69 Input current and output voltage of proposed SEPIC converter with feedback controller for load resistance of 100 Ω

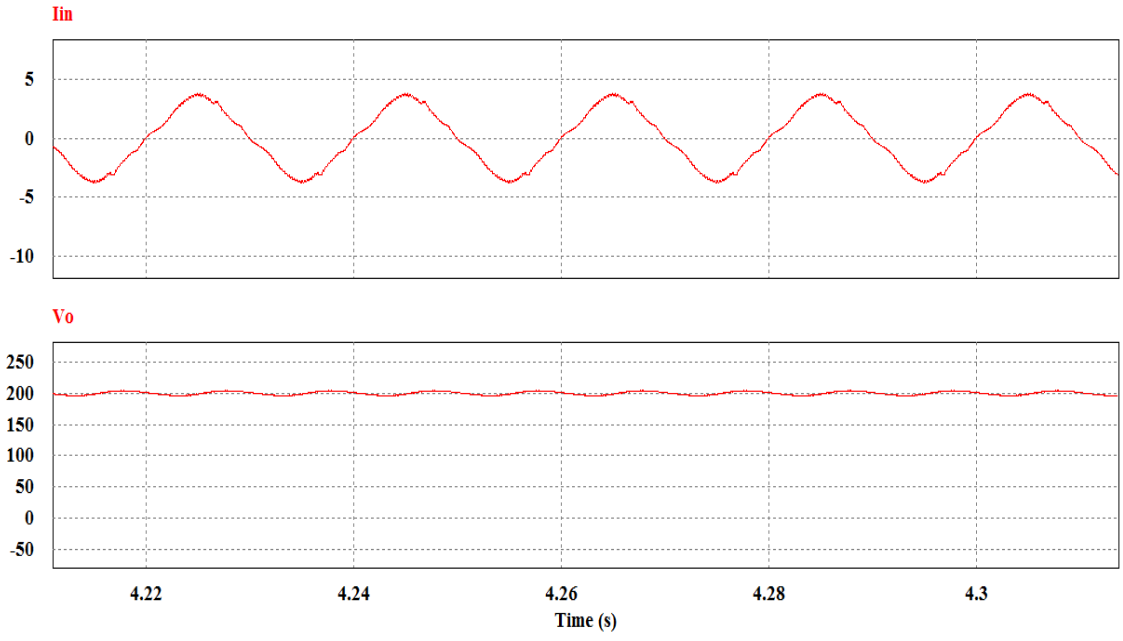


Fig.6.70 Input current and output voltage of proposed SEPIC converter with feedback controller for load resistance of 200 Ω

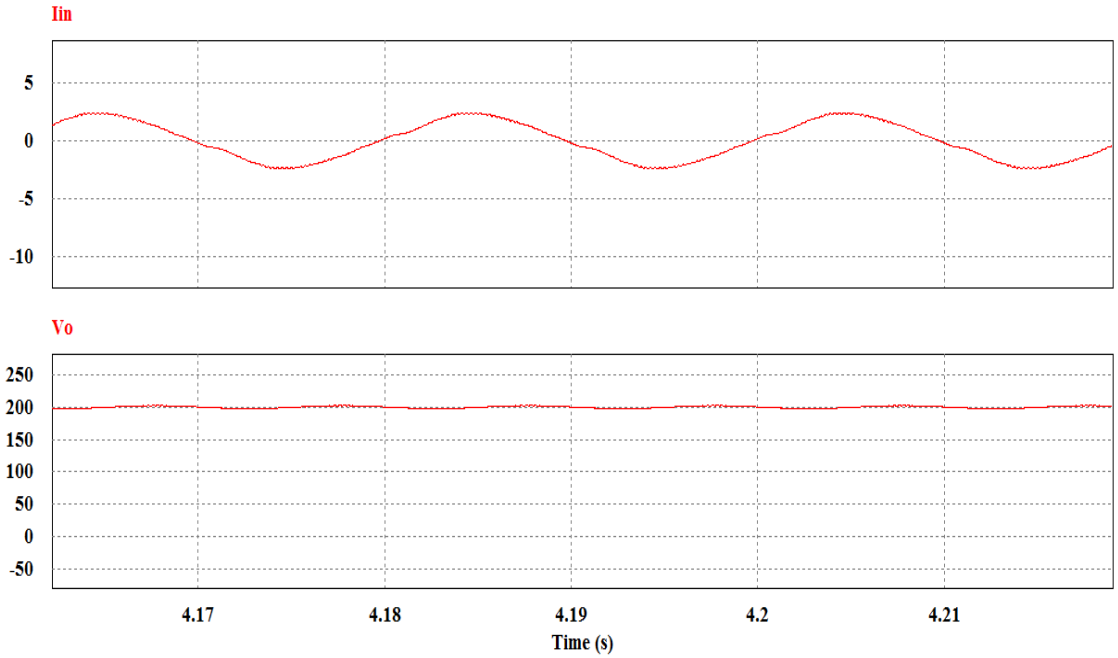


Fig.6.71 Input current and output voltage of proposed SEPIC converter with feedback controller for load resistance of 300 Ω

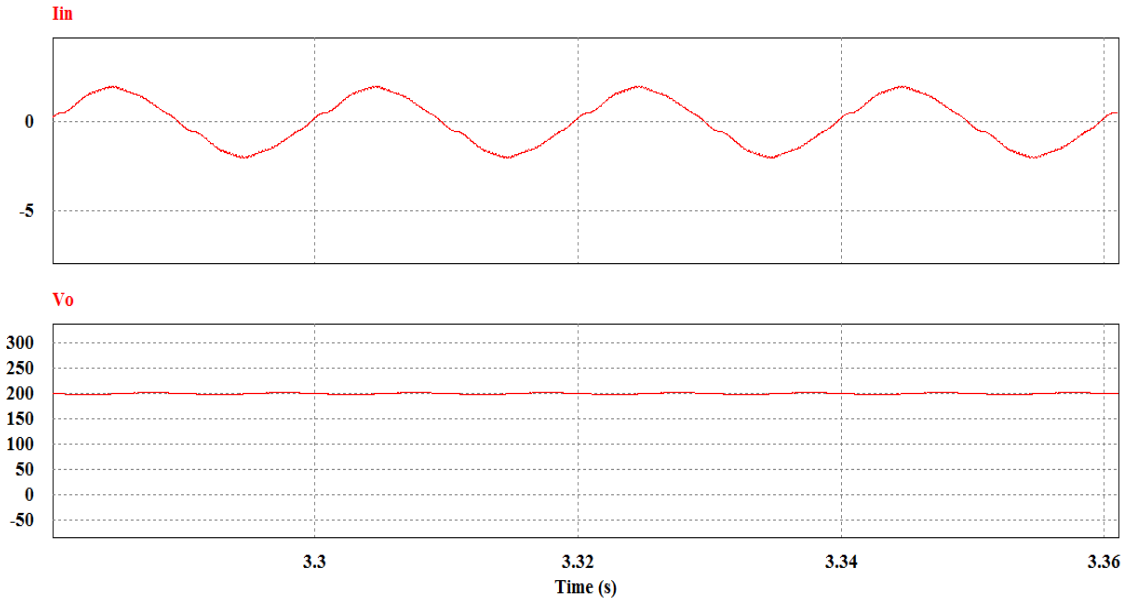


Fig.6.72 Input current and output voltage of proposed SEPIC converter with feedback controller for load resistance of 400 Ω

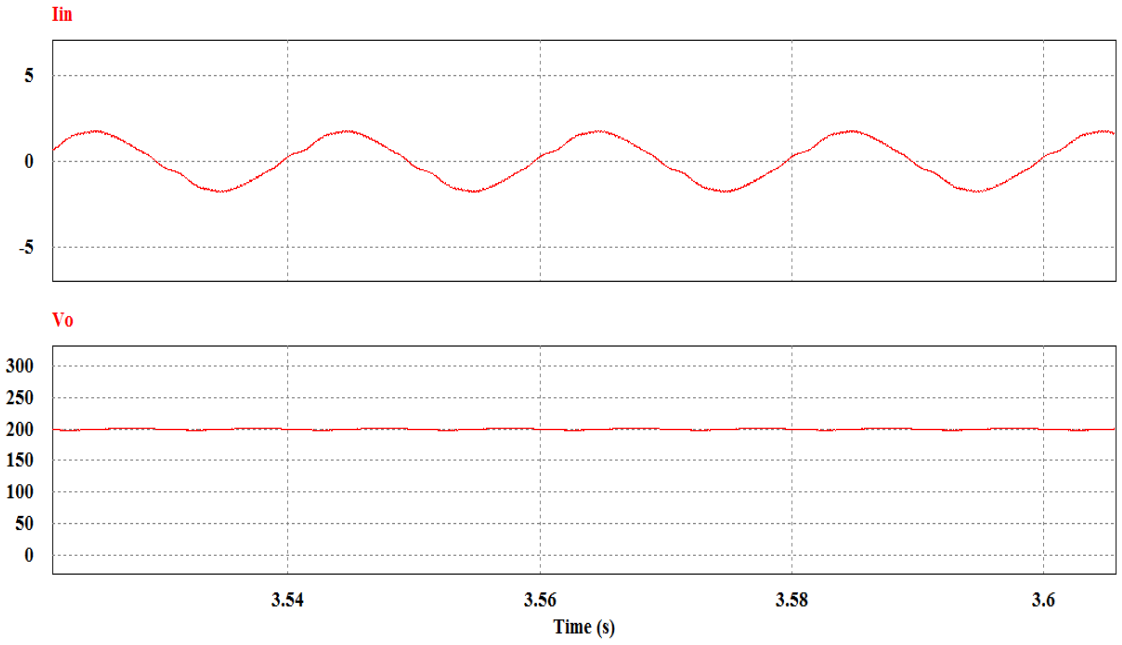


Fig.6.73 Input current and output voltage of proposed SEPIC converter with feedback controller for load resistance of 500 Ω

CHAPTER 7
CONCLUSION AND SUGGESTION FOR FUTURE WORK

7.1 Conclusion

The work presented in this thesis focus on the design and analysis of single phase Ĉuk and SEPIC AC-DC converter with improved performance. These two circuits chop the input current at the AC side in contrast to the conventional scheme, which chops the rectified output. The main advantage of the proposed circuits are that smaller input filter is required to achieve better performances in terms of low input current THD and high input power factor. The proposed converters provide control in terms of amplitude of the output voltage. Both of these two switch mode AC-DC converters consist of one switch. Single switch makes the control easier. The feedback controller circuit is also introduced with the proposed converters to regulate the output voltage and improve power factor while changing the load values.

The performances of the proposed topologies are evaluated in terms of THD, input power factor, and efficiency along the range of the duty cycle of the control signal. The wave forms of input currents and their corresponding spectrum is presented for both proposed and conventional one in different frequencies and duty cycles. Moreover the comparison between the proposed and conventional circuits in terms of THD, input power factor and efficiency are also presented in bar charts in this thesis. Results showed that, compared to conventional rectifier followed by a DC-DC converter, the proposed topologies are able to perform AC-DC conversion ensuring better power quality at higher efficiencies and are applicable for wider range of load voltage and frequency demands. The output voltage waveforms at different frequencies and duty cycles of these proposed converters are presented here. The waveforms of regulated voltage and input current at different loads are also presented for both converters.

7.2 Suggestion for Future Work

The proposed converters provide satisfactory results for the resistive load under consideration. In practice the electro-mechanical load connected to the output may show variation in their operating condition with time, which is known as the dynamic behavior. The behavior of the proposed converter may be analyzed under dynamic load. Future

extension of this work may include development of the mathematical model of the proposed topologies by developing the transfer functions for each converter. There is also a scope of reducing the number of inductor and capacitor with maintaining satisfactory THD, Input power factor and efficiency.

Moreover, most of the industries use three phase diode rectifier to convert AC to DC. The three phase version of these single phase circuits may be designed for optimized power qualities.

While performing the simulation the inductors and capacitors are assumed to be ideal, which have no resistances. But in real world it is not possible to have the inductors and capacitors without resistances. So real inductors and capacitors can be considered for simulation to get more accurate result.

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