QUANTUM MECHANICAL MODELING AND SIMULATION OF MONOLAYER WSe_2 CHANNEL FIELD EFFECT TRANSISTOR

A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science in Electrical and Electronic Engineering

by

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Approval

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Declaration

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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29.02.16

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(Saeed-Uz-Zaman Khan)

To my beloved parents

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All praise goes to the Almighty for giving me the patience and drive required to complete my M.Sc. research and finish the dissertation in due time.

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Abstract

In recent years, researchers have been working on Graphene and Monolayer Transition Metal Dichalcogenides like MoS_2 and WSe_2 to find the channel material for next generation ultimately scaled transistors. The absence of intrinsic band gap in Graphene sheet made researchers focus more on Dichalcogenides lately and as a result of that endeavor monolayer WSe_2 based pFET has been fabricated. This experimental device with high band gap (1.6 eV) showed higher carrier mobility (250 cm^2/Vs) than monolayer MoS_2 based devices. In recent literature methods of n-type and p-type doping of monolayer WSe_2 FET have been demonstrated, which led to the fabrication of high performance CMOS inverter solely based on monolayer WSe_2 channel. Despite of these promising experimental results, rigorous Transport and Electrostatic study of monolayer WSe_2 based FET is yet to appear in the literature. Moreover, at present no analytical model for current-voltage characteristics is available specifically for WSe_2 FET. The purpose of this work is to perform a simulation study of Quantum Mechanical electrostatics by solving Schrödinger-Poisson equations self-consistently using material parameters extracted from literature and to determine the transport characteristics using Fast Uncoupled Mode Space (FUMS) approach. The second objective of this work is to develop a compact Transport model for Monolayer WSe_2 FET. In this thesis work both objectives have been fulfilled and a fully numerical device simulator and a compact analytical transport model have been demonstrated. The numerical simulator has been used to study the transport performance of a monolayer WSe_2 FET structure with 20 nm of channel length. The performance analysis revealed excellent on and off state performances of the device with an impressive ON/OFF current ratio of 10^{10}, on current of 467.2 μA/μm, effective mobility of 300 cm^2/V.s, and SS of 77.72 mV/dec. The proposed device also demonstrated promising resistance to Short Channel Effects (SCEs) with a Drain Induced Barrier Lowering (DIBL) of 14.91 mV/V and a threshold voltage roll-off of 0.05 V for 0.7 V change in drain voltage. The compact analytical model developed in this work successfully tracks the transport characteristics of the monolayer WSe_2 device as well. The model estimates the inversion charge distribution in the channel and calculates the drain current using the drift-diffusion transport equation. To simplify the analytical expression, the model also makes Gradual Channel Approximation and assumes that the electrostatic potential in the channel is limited to quadratic variations only. The model also uses a Field Dependent Mobility Model suggested by the ALTAS simulation framework and considers the E-K diagram obtained from the Density Functional Theory (DFT) to calculate the Density of States for monolayer WSe_2. Results obtained from this physically accurate compact model are used for quick characterization of the proposed monolayer WSe_2 channel transistor. With the help of a gate voltage dependent “Fitting Function”, this model successfully estimates the transport characteristics and threshold voltage of monolayer the WSe_2 FET, which are in reasonable agreement with the numerical simulation.

Contents

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List of Abbreviations

1D	One-Dimensional
2D	Two-Dimensional
3D	Three-Dimensional
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
ATK	Atomistix Toolkit
CMOS	Complementary Metal Oxide Semiconductor
C-V	Capacitance-Voltage
CVD	Chemical Vapor Deposition
DFT	Density Functional Theory
DIBL	Drain Induced Barrier Lowering
FEM	Finite Element Method
FUMS	Fast Uncoupled Mode Space
GAA	Gate-All-Around
GGA	Generalized Gradient Approximation
ITRS	International Technology Roadmap of Semiconductors
LDA	Local Density Approximation
LDOS	Local Density of States
MOCVD	Metal Organic Chemical Vapor Deposition
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NCFET	Negative Capacitance Field Effect Transistor
NEGF	Non Equilibrium Green's Function
PAW	Projector Augmented Wave
PDE	Partial Differential Equation
PECVD	Plasma Enhanced Chemical Vapor Deposition
PL	Photoluminescence
PMMA	Polymethyl Methacrylate
QM	Quantum Mechanical
Q-V	Charge-Voltage

SBH	Schottky Barrier Height
SCE	Short Channel Effect
SOC	Spin Orbit Coupling
SOI	Silicon on Insulator
SS	Subthreshold Slope
TEM	Transmission Electron Microscope
TFET	Tunnel Field Effect Transistor
TMDC	Transition Metal Dichalcogenides
UMS	Uncoupled Mode Space
UTB	Ultra Thin Body
VASP	Vienna Ab-initio Simulation Package
XAS	X-Ray Absorption Spectroscopy
XPS	X-Ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction

List of Symbols

q	Elementary Charge
k	Boltzmann Constant
h	Plank's Constant
ħ	Reduced Plank Constant
T	Kelvin Temperature
L_{ch}	Gate Length
t_{ch}	Channel Thickness
t_{tox}	Top Gate Oxide Thickness
t_{box}	Bottom Gate Oxide Thickness
W	Channel Width
ε_{ch}	Dielectric Permittivity of WSe_2
ε_{tox}	Dielectric Permittivity of Top Gate Oxide
ε_{box}	Dielectric Permittivity of Bottom Gate Oxide
N_A	Uniform Doping Concentration in the Channel
N_{sd}	Uniform Doping Concentration in Source and Drain
N_{2D}	Inversion Charge Density in the Channel
N_{dos}	Effective Density of States
n_i	Intrinsic Carrier Concentration
Φ_{mt}	Work-Function of Top Gate Electrode
Φ_{mb}	Work-Function of Bottom Gate Electrode
V_{Gt}	Top Gate Bias
V_{Gb}	Bottom Gate Bias
V'_{Gt}	Effective Top Gate Bias
V'_{Gb}	Effective Bottom Gate Bias
V_S	Source Bias Voltage
V_D	Drain Bias Voltage
V_{bi}	Built-in Potential
V_{FBt}	Flat-Band Voltage of Top Gate Electrode

V_{FBb}	Flat-Band Voltage of Bottom Gate Electrode
χ_{ch}	Electron Affinity
E_g	Bandgap Energy
m^*	Effective Mass
μ_n	Effective Carrier (Electron) Mobility
μ_{n0}	Low Field Carrier (Electron) Mobility
C_{ox}	Gate Oxide Capacitance
$E_{\|\|}$	Lateral Electric Field from Source to Drain
g_s	Spin Degeneracy
g_i	Valley Degeneracy
VSATN	Saturated Carrier (Electron) Velocity

Chapter 1

Introduction

1.1 Current Trend and Challenges of CMOS Technology

In 1965 Intel's co-founder Gordon Moore famously predicted that the number of components per integrated chip will be doubled every year. He revised his prediction in 1975 [1] stating that the doubling will happen approximately in every two years. This prediction, known as "Moore's Law", has been acting as a guideline for the semiconductor industry to set their goals and made them push harder to break the technological boundaries through constant innovation.

As shown in Figure 1.1, number of transistors per chip grew steadily every year so far, as per Moore's Law. To sustain this growth the semiconductor industry had to face many challenges over the years. The first major blow came in early 2000 when the technology node shrunk below 90 nm. The high clock speed and smaller device dimension caused heat to get trapped inside the chips and gradually make them too hot to use. To counter the heating problem the industry halted the increase in clock speed and introduced multi-core processors to keep up with the Moore's law.

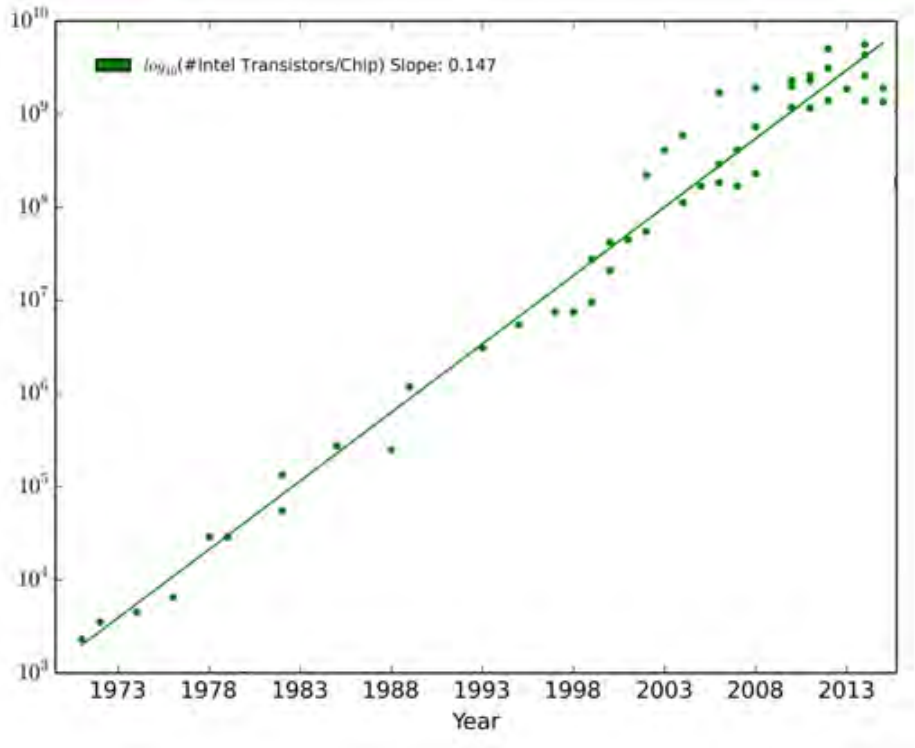


Figure 1.1: Intel's Microprocessor transistor count [2].

As technology node got smaller, gate length and oxide thickness got smaller as well, leading to Short Channel Effects (SCEs) and gate leakage current. The most common short channel effects are Channel Length Modulation, Drain Induced Barrier Lowering (DIBL), Threshold Voltage Roll-off and Velocity Saturation. Over the years, the semiconductor industry had came up with various modifications to the basic Si-based MOSFET structure to keep those non-ideal effects in check and continue scaling.

Channel Length Modulation, first observed in long channel MOSFETs, shortens the effective channel length of the device with the application of drain bias. But this effect is most prominent with short channel devices where it acts as one of the reasons for the finite positive slope of MOSFET's I_{ds}-V_{ds} curve in the saturation region. Shorter effective channel length causes various other SCEs and disrupts the constant electric field scaling approach. This effect can be countered by increasing the channel doping concentration.

Drain Induced Barrier Lowering (DIBL) is caused when device length is so small that the source to drain lateral electric field is no longer insignificant compared to the vertical electric field due to the gate voltage. This results in lowering of the top of the conduction band barrier with the drain voltage and gives an I_{ds}-V_{ds} curve with positive slope in the saturation region. Because of this effect the threshold voltage of the device becomes a function of the applied drain voltage. Increased gate control over the channel, either by means of thinner cannel or increased gate confinement, can get rid of this problem.

Another major short channel effect is Hot Carrier Effect or Impact Ionization, where increased lateral electric field due to shorter channel length causes the carrier electrons to gain much higher energies than average electrons in an n-MOSFET. These "Hot Electrons" hits Silicon atoms and creates electron-hole pairs due to impact ionization, which in turn creates a channel-to-substrate current. If the "Hot Electrons" gain enough energy it may even overcome the channel-oxide barrier and damage the gate oxide material. A physical isolation of the channel from the substrate and a thick high-κ oxide can prevent this effect.

Increased lateral electric field in the channel also causes Velocity Saturation, where the average velocity of charge carriers no longer increases linearly with the electric field. Velocity saturation is caused by increased scattering of highly energetic electrons and it eventually increases the transit time of carriers through the channel.

Another implication of the increased lateral electric field is avalanche breakdown, which occurs in the channel at the drain end. Avalanche breakdown causes current to flow from drain to source through the substrate underneath the channel, which results in channel breakdown at a lower drain voltage. Silicon-on-insulator (SOI) and Ultra Thin Body (UTB) channel MOSFET can reduce this problem significantly.

Gate Oxide Breakdown is another non-ideal effect associated with the aggressive scaling of transistors. With the reduction of the feature length of a transistor generation, gate oxide thickness gets smaller as well, making it more prone to electrostatic breakdown. This is major

reason of modern day transistor failure and poses a severe challenge to the device reliability. Use of thick high-κ gate oxides can improve the breakdown problem while keeping the gate capacitance at the level demanded by the constant scaling. Thicker gate oxides also reduce the Quantum Mechanical tunneling at the channel-oxide interface and minimize the gate leakage current. Intel is already using high-κ gate oxide in their transistors for 45 nm technology node and beyond.

Random Dopant Fluctuation is another major issue with shorter device dimension. A 10 nm channel Si-MOSFET has only 20 to 23 Silicon atoms in between the source and drain, which makes uniform doping of the channel very difficult and threshold voltages vary from transistor to transistor in a process.

Subthreshold Current is one of the important factors affecting the scaling of transistors. Since the operating voltage is very low for present day devices, the threshold voltage is not much higher than the off-voltage. This gives rise to significant drain current even be low the threshold voltage and is one of the major reasons of heating in off-state devices. The severity of this unwanted current is represented by Subthreshold Slope (SS) which indicates the voltage required in milivolt to reduce the drain current by a factor of ten below the threshold voltage. Unfortunately traditional MOSFET structure cannot go below a SS of 60 mV/dec. Transistor structures with higher degree of gate control like Gate-all-round (GAA) FET and FinFET can hardy reach that theoretical limit of SS. Only viable option to reduce the SS below 60 mV/dec is the use of Negative Capacitance FET (NCFET) or Tunnel FET (TFET), which is technologically not feasible yet.

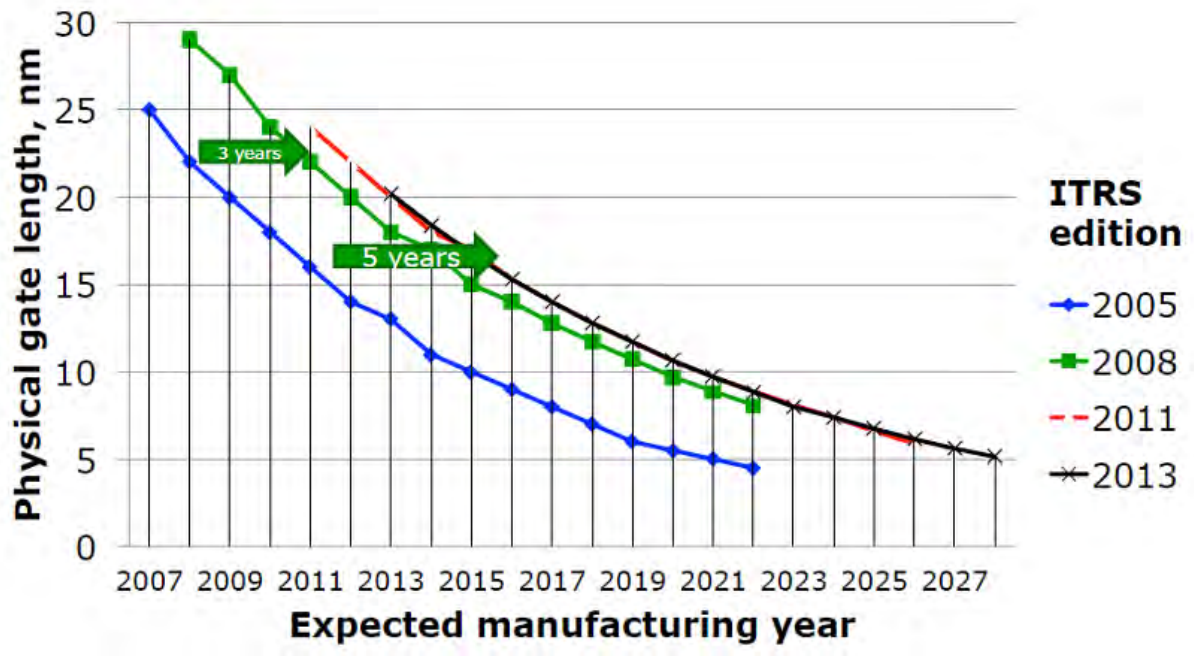


Figure 1.2: ITRS roadmap [3] for transistor scaling in terms of physical channel length.

The semiconductor industry coped with the SCEs and other non-ideal effects mentioned above by using strained Si-Ge channel for 90 nm and high-κ gate oxides beyond 45 nm technology nodes. From 2011, Intel started to use Tri-gate Silicon transistors in their 22 nm technology nodes, allowing them to have better gate control on the device channel and reduce the SCEs. Intel will be using the same Tri-gate Silicon transistors technology in their upcoming processors beyond the 22 nm node. Intel's latest 'Kaby Lake' microprocessors are scheduled to be released by the end of 2016 which will have 14 nm transistors [4]. The 14 nm technology node will be using Silicon Tri-gate transistors as well, with a physical fin-length of 8 nm [5].

As technology node goes down to 10 nm, 7 nm and eventually to 5 nm, to keep up with the Moore's law the physical gate length of the transistors needs to be shrunk as well. According to ITRS 2013 roadmap [3], by the year 2028 the physical gate length of transistors will be 5 nm (Figure 1.2) which means only around 10 Silicon atoms in the channel. Beyond 10 nm node Tri-gate Silicon channel transistors will not suffice to overcome the power dissipation and scaling challenges and new material and structures will be needed. Intel's Innovation Enabled Technology Pipeline (Figure 1.3) also supports the need for alternate channel materials and novel structures for future generation transistors.

Figure 1.3: Intel's innovation enabled technology pipeline infographic (Courtesy Intel [2]).

To overcome the electrostatics and power challenges global research efforts have been devoted by researchers to innovate new materials for semiconductor application. These materials range from Organic Materials, III-V Compound Materials, Graphene and other 2D

materials. Along this line of effort came the innovation of Monolayer Transition Metal Dichalcogenides (TMDCs) as prospective candidates for the next generation of transistors.

1.2 Two Dimensional Material Channel MOSFETs

Traditional transistor structures have already touched their scaling limit and only viable solution to uphold Moore's law lies in 3D structure like Fin-FET and Gate-all-around FET or Ultra Thin Body (UTB) Channel FETs. Although in extreme scaling limits UTB channel FETs easily outsmart 3D devices, it is not easy to deposit a defect free UTB channel in sub-5 nm gate length regime when the semiconductor material has Zinc-blende or Diamond structure. Use of single layered 2D semiconductors [6] like Graphene or monolayer Transition Metal Dichalcogenides (TMDCs) [7-11], Phosphorine [12-13] and Silicene [14] as UTB channel solves that problem, as despite being only an atomic layer thick, they exhibit minimal roughness, dangling bonds and defect states.

1.2.1 Motivation for Choosing TMDCs

Among the single layered semiconductors, Graphene is not suitable as transistor because of the absence of intrinsic bandgap in Graphene. Although methods of opening bandgap in Graphene like forming Nano Ribbons [15-17], applying strain [18-21] and/or electric field [22-25] have been explored, sufficient bandgap for getting a suitable on/off current ratio is yet to achieve. As an immediate solution to this problem comes the monolayer TMDCs, as they have a very high bandgap in addition to their single layered hexagonal unit cell like Graphene [26-28].

In recent years, among the monolayer TMDCs, Molybdenum Disulphide (MoS_2) and Tungsten Diselenide (WSe_2), have gained broad interest as transistor channel materials [29-31]. Their high bandgaps and sub-1 nm thickness makes them the most suitable candidate for next generation low power transistors. Apart from the application in memory devices and microprocessors, flexibility, transparency, and pristine interfaces made TMDCs ideal candidates for display electronics [32] and bio/gas sensors [33-34]. The TMDC based FET has matured quite a lot over the years with the demonstration of large scale CVD growth technique [35] and demonstration of both n-type and p-type FETs based on MoS_2 and WSe_2 [26, 36-37] FETs with record on-state and off-state performances. In addition, tremendous research efforts are being given to improve the performance of TMDC FETs addressing the residual issues like high contact resistances with source/drain metals, high interface trap density, low electron and hole mobility and inefficient air-stable doping methods [38].

Other recent 2D materials like Phosphorine and Silicene is at elementary stages of development at present and their transport and scaling performances are not established yet.

This makes TMDCs like MoS_2 and WSe_2 the best possible solution to the ultimate scaling obligations of future transistors for the time being.

1.2.2 Motivation for Choosing WSe_2

Despite of showing promise for low power application, MoS_2 based transistors are less suitable for high performance operation since monolayer MoS_2 has a high electron and hole effective mass and low carrier mobility [39].

Recent studies indicates that MoS_2 FETs with high-κ dielectric has very low carrier mobility of about 60 $cm^2/V{\cdot}s$ due to remote phonon scattering [30, 40]. According to Liu et al. [41] phonon scattering limits the ballistic performance of monolayer MoS_2 FET even at sub-10 nm technology nodes. Moreover, monolayer MoS_2 FETs are yet to demonstrate the scaling performance required to comply with the ITRS roadmap [27, 41-42].

In search of high mobility monolayer channel material which conforms to ITRS roadmap, many other Transition Metal Dichalcogenides are being explored [28] and as a result of that endeavor monolayer WSe_2 based p-FET has been fabricated (Figure 1.4a) [26].

Bulk WSe_2 is quite stable and oxidation resistant than its Sulphide counterpart in case of a humid environment [37, 43]. Bulk WSe_2 crystal also demonstrated carrier mobilities around 500 $cm^2/V.s$ [9]. The experimental monolayer WSe_2 device by Fang et al. [26] with high band gap (1.6 eV) showed higher effective carrier mobility (250 $cm^2/V.s$) than monolayer MoS_2 based devices. In recent literature methods of n-type (Figure 1.4b) [44] and p-type (Figure 1.4c) [45] doping of monolayer WSe_2 FET have been demonstrated, which led to fabrication of high performance CMOS inverter (Figure 1.4d) [46] solely based on monolayer WSe_2 channel.

In 2011 Yoon et al. [27] published rigorous Quantum Mechanical (QM) simulation study of short channel (L_G= 19 nm) monolayer MoS_2 transistor using Fast Uncoupled Mode Space (FUMS) [47-48] based Non-equilibrium Green's Function (NEGF) [49] approach, to predict the performance of such devices. In this thesis similar approach has been followed to perform an extensive QM simulation analysis of monolayer WSe_2 channel transistors.

Besides experimental and physical modeling, compact analytical modeling of monolayer TMDCs is of paramount importance in order to explore the full potential of these materials for ultra-scaled device applications. Cao et al. [38] recently proposed a generalized compact transport model for 2D TMDCs that takes into various non-ideal device effects into account. However, this model is not specific to WSe_2 FETs and the assumptions and simplifications utilized to develop this model deserve some attention specific to WSe_2. In this work a better model specific to monolayer WSe_2 has been developed which correctly predicts the performance and transport properties for WSe_2.

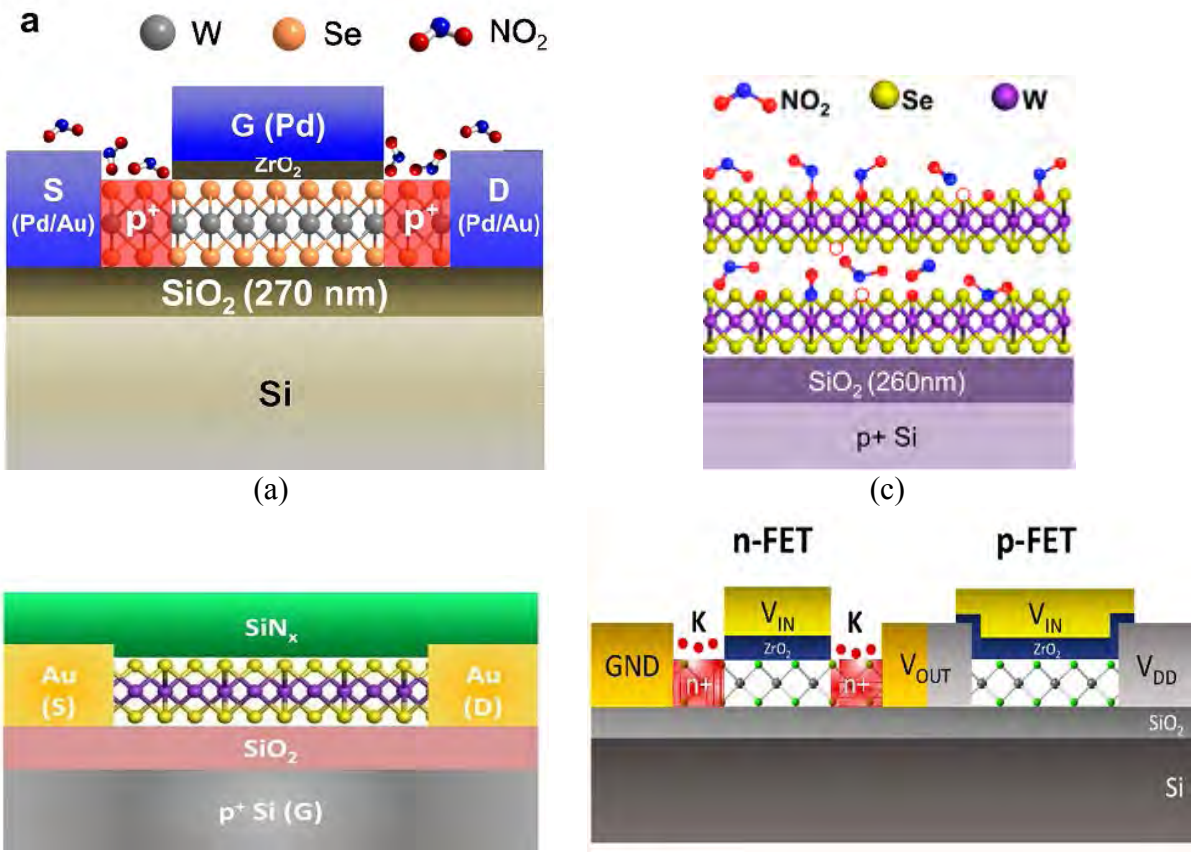


Figure 1.4: (a) Monolayer WSe_2 based p-FET by Fang et al. [26] **(b)** Air stable p-doped WSe_2 FET by Chen et al. [44] **(c)** n-doped WSe_2 FET by Zhao et al. [45] **(d)** CMOS inverter implemented on same WSe_2 flake by Tosun et al. [46].

1.3 Thesis Objectives

The primary objectives of this work can be divided into following four parts-

- First, to develop a 1D self-consistent Schrödinger-Poisson solver for simulating the Electrostatics of monolayer WSe_2 channel Field Effect Transistor.

- Second, to develop a Fast Uncoupled Mode Space (FUMS) approach based 2D numerical transport simulator using Non-equilibrium Green's Function (NEGF) Formalism for fully depleted monolayer WSe_2 channel Field Effect Transistor.

- Third, to develop a compact current–voltage model for monolayer WSe_2 channel Field Effect Transistor considering different secondary effects.

- Fourth and final, to assess the viability of monolayer WSe_2 channel Field Effect Transistors for future electronic applications by evaluating various performance parameters like threshold voltage, on current, on/ off current ration, drain induced barrier lowering and subthreshold swing.

1.4 Thesis Organization

The entire thesis is organized into five chapters. A brief outline of each chapter is described below.

The first chapter discusses the current technological status of transistors and briefly sheds lights on the scaling issues and need for futuristic innovations in every aspect of semiconductor devices to uphold the technological progression professed by Moore's law. It also introduces the context of the innovation behind monolayer Transition Metal Dichalcogenide (TMDC) channel MOSFETs.

The second chapter summarizes the research and technological progress achieved so far to make monolayer WSe_2 channel MOSFETs a reality. It presents a brief overview of the literature related to device simulation, material development, fabrication and device characterization of monolayer WSe_2 FETs.

The third chapter describes the development of a numerical quantum mechanical Electrostatic and Transport simulator for the monolayer WSe_2 device. At the first part of this chapter the device structure is defined along with governing equations and theoretical discussions on the electrostatic and transport characteristics is performed. This section is followed by configuration methods of related software platform for the simulator. The next section presents some key results obtained from the simulator developed and benchmarks the accuracy of the simulator. Finally various performance parameters are extracted from the simulated results to evaluate the feasibility of the proposed structure in terms of transport characteristics.

The fourth chapter introduces a simplified compact analytical drain current-voltage model from fundamental treatment of charge-potential system of the device. This chapter rigorously studies the mathematical formulation of the device system and introduces physically justifiable assumptions to simplify the problem. This chapter gradually develops a closed form analytical model of the current-voltage problem and defines few fitting parameters to benchmark its output. Finally, few key results from the analytical model have been demonstrated at the last part of this chapter.

The fifth and last chapter of this thesis outlines the conclusion of this thesis work. It also briefly describes prospective fields of future improvements and modifications to this work.

Chapter 2

Exploration of the Monolayer WSe_2 FET

2.1 Simulation

2.1.1 Material Level Simulation

Monolayer WSe_2 has very different properties than their bulk form. For example, bulk WSe_2 has an indirect bandgap of 1.2 eV, whereas monolayer WSe_2 has a 1.6 eV direct bandgap [39, 50]. To seek for the suitable TMDC with desired property, material level simulation is necessary. Solving the band structure using first principle DFT simulation can provide that valuable insight to the material properties of monolayer TMDCs. Open source softwares like Quantum Espresso [51] can perform such simulations. Commercial tools like Atomistix ToolKit (ATK) [52] are also available.

In 2014 Zhao et al. [45] utilized First Principle Density Functional Theory (DFT) [53-54] calculations to study their experimental p-doped WSe_2 transistor. For the simulation, they have considered plane wave basis sets and Projector Augmented Wave (PAW) pseudopotentials [54-55] in the Vienna Ab-initio Simulation Package (VASP) [53, 56-57].

In 2013 Liu et al. [37] studied role of metal contacts in designing high performance monolayer n-type WSe_2 Transistors using Ab-initio DFT calculations. The simulation indicated that the d-orbitals of the contact metal play a vital role in creating low resistance ohmic contacts with monolayer WSe_2. In addition to the presence of d-orbitals, smaller work function of the contact metal compared to WSe_2 affinity is necessary for the best possible n-WSe_2-metal contact.

In 2014 Kang et al. [58] computationally studied metal contacts to monolayer Transition Metal Dichalcogenide semiconductors. Their work employed the Kohn-Sham DFT [55] to compute the band structure of Monolayer WSe_2 because it offers significant computational advantages over other Ab-initio methods. Although, Kohn-Sham DFT sometimes underestimates the bandgap of the materials for most common exchange-correlation potentials like the generalized gradient approximation (GGA) [59] and the local density approximation (LDA) [60], this work revealed that LDA alone is sufficient to get the theoretically and experimentally accurate bandgap of 1.6eV [61].

In 2012 Kang et al. [28] performed numerical DFT calculations using Atomistix ToolKit (ATK) [52]. This work calculated optimized geometries, PDOS, electron densities and tunnel

barriers of metal-TMDC contacts using DFT to discover that Pd is the best source(drain)-contact metal for monolayer intrinsic WSe_2 and forms p-type contact.

In 2013 Liu et al. [39] performed Ab-initio DFT calculations on metal-WSe_2 system to study the performance of monolayer WSe_2 FET. For metal they have chosen Ag (111) since it has a small-work-function which forms good contacts for n-type devices. Calculation revealed that although natural WSe_2 is intrinsic, it can be n-doped by depositing Ag onto the monolayer.

In 2015 Sengupta et al. [62] showed the effects of electron-phonon scattering on the performance of monolayer n-WSe_2 MOSFET using material parameters obtained from LDA-DFT calculations. They concluded that the performance of the monolayer WSe_2 FET is less prone to phonon scattering and has a ballisticity of 83% for a 10 nm channel. On the other hand, in the presence of scattering there can be a 21–36% increase in the intrinsic time delay as well.

In 2016 Su et al. [63] employed the Vienna Ab-initio DFT calculations to study the electronic properties of MoS_2/WSe_2 heterobilayers and the effect of both the external in-plane biaxial strain and out-of-plane compressive strain on it.

In 2015 Hosseini et al. [64] calculated the bandstructure of WSe_2 using LDA-DFT mechanism in the SIESTA code [65] and studied the effect of strain on the electronic bandstructure and low field mobility. The study revealed sharp increase in the mobility of WSe_2 with relatively small tensile strain. Whereas, a relatively small increase in compressive strain results in initial decrement of the mobility, which then increases again with further increase in compressive strain.

In 2014 Desai et al. [66] studied the strain-induced indirect to direct bandgap transition in multilayer WSe_2. Their experimental results demonstrated a drastic enhancement in Photoluminescence intensity for multilayer WSe_2 under uniaxial tensile strain, which is attributed to an in direct to direct bandgap transition. DFT calculations supported the experimental results and revealed very small energy difference exists between the direct and indirect bandgaps of WSe_2 and the transition is easily controllable using practically achievable stain on the channel.

In 2016 Wang et al. [67] made a comparative study of the interfacial properties of monolayer and bilayer WSe_2 with different metals using the DFT band structure calculation. The study found that, in the absence of the spin-orbital coupling (SOC) Pd contact has the minimum hole Schottky Barrier Heght (SBH). Whereas with SOC, WSe_2-Pt interface has the minimum hole SBH and thus acts as a p-type Ohmic contact.

In 2013 Duerloo et al. [68] employed DFT calculations to estimate the piezoelectric coefficients WSe_2 along with few other monolayer TMDCs. The study revealed that monolayer TMDCs possesses greater piezoelectric coefficients compared to commonly used Wurtzite piezoelectrics.

In 2015 Allain et al. [69] used DFT calculations to show that, due to orbital overlap and reduced tunnel barriers, edge contacts lead to a shorter bonding distance than top contacts for both the monolayer and multi-layer TMDs.

In 2014 Yuan et al. [70] studied the spin–valley-coupled circular photogalvanic current generation in WSe_2 using VASP DFT package. They have demonstrated a spin-coupled valley photocurrent in a WSe_2 electric-double-layer transistor and found that the direction and magnitude of the current is dependent on the degree of circular polarization and external electric field.

In 2013 Liang et al. [71] reported Quasiparticle band-edge energy and band offsets of monolayer WSe_2 using first-principle DFT calculations. In addition to bandgap calculations, absolute band-edge energies with respect to the vacuum level have been estimated.

In 2015 Zhou et al. [72] investigated the phonon transport of monolayer WSe_2 employing DFT with the phonon Boltzmann transport equation. The study found that, compared to other 2D materials the monolayer WSe_2 has relatively lower thermal conductivity, which is attributed to its Debye frequency and heavy atom mass.

In 2015 Jiang et al. [73] used Ab-initio quantum simulation to estimate the transport performance and scaling limit of the sub-10 nm monolayer TMDC TFETs. They found that, in terms of high-performance and low-operating-power WTe_2-TFET offers the the most promising results compared to WSe_2 and other TMDC TFETs.

In 2015 Dai et al. [74] used DFT computations to study bandgap tunability of the multilayer WSe_2 sheets with the application of external electric fields. The study concluded that the bandgap of WSe_2 sheet decreases with the increment of the vertical electric field and gradually turns it metallic at about of 0.6–2.0 V/nm electric field, depending on the number of layers present in the sheet.

In 2013 Mishra et al. [42] studied the dependence of the performance of TMDC FETs on materials and number of layers, using Vienna Ab-initio Simulation Package (VASP) and ballistic quantum transport calculations. The study of 5 nm channel TMDC FET with a 2 nm underlap at both side of the gate revealed excellent switching performance but lacked the peak current required by ITRS roadmap at this level of scaling.

2.1.2 Device Level Simulation

Once the material parameters are in hand the performance of the device to be made with that material can be evaluated. Different physical parameters and dimensions needed to be optimized for better performance of the device. These are done by device level simulation of

monolayer TMDC FETs. As an electron device, both the electrostatics and transport properties of monolayer TMDC FETs are required to be studied to get the optimal structure with greatest performance.

2.1.2.1 Simulation of Electrostatics

To obtain the Electrostatics of the device, 1-D Schrödinger and Poisson equations is solved self-consistently in the direction perpendicular to the channel. This is done by coupling COMSOL Multiphysics [75] and MATLAB [76]. Introduction of COMSOL Multiphysics allows dealing with complex geometry. Only the partial differential equations of Schrödinger and Poisson are solved in COMSOL environment. The numerical data are exported to MATALB in real time at every iteration and all the numerical coupling and calculations are done inside MATLAB. Upon convergence this simulation gives complete electrostatics of the device including C-V characteristics, surface-potential, charge profile, effect of D_{it} and fixed oxide charge etc. So far no work in the literature investigates the detailed electrostatics of the monolayer WSe_2.

2.1.2.2 Simulation of Transport Properties

Transport simulation can be done using FUMS [47-48] approach. Here, Poisson equation is to be solved for a 2D cross section along the channel. Schrödinger equation is to be solved only for one 1D cross section perpendicular to the channel, from which the solution of the Schrödinger equation across the channel can be approximated applying Perturbation Theory. The channel is treated as fully depleted and channel charge is calculated using NEGF Formalism. Upon convergence, the simulator can provide Ballistic drain current-voltage characteristics, Threshold Voltage, Transconductance profile, Subthreshold Swing and other performance parameters. This simulator can accurately model SCEs like Drain Induced Barrier Lowering (DIBL) and Threshold Voltage Shifting. Here also, the differential equations can be solved by COMSOL and coupling and calculations can be done in MATLAB environment.

In 2013 Chang et al. [77] compared ballistic transport characteristics of monolayer WSe_2 with other TMDCs using atomistic full-band NEGF simulations with Tight Binding potentials obtained from DFT. They considered n-type TMDCs with channel length of 15 nm deposited on a 50 nm thick SiO_2 substrate, 2.8 nm thick HfO_2 as top oxide and n-type doping concentration of 7×10^{13} cm^{-2} at source and drain. The NEGF simulations revealed excellent off-state and short channel performances of the TMDC FETs in terms of SS and DIBL.

In 2013 Mishra et al. [42] studied the transport performances of TMDC devices by using Non-equilibrium Green's Function (NEGF) formalism to calculate the charge and then self-consistently solving the Poisson's equation. Their analysis revealed scaling potential of TMDC FETs up to 5 nm channel length with excellent on/off current ratio of 10^6, SS of 65

mV/dec and transconductance of 150 μS/μm. The study also revealed that, increasing the number of layers in TMDC FETs does not increase the on current as the channel loses the gate control with the increasing number of channel layer.

In 2014 Cao et al. [30] presented dissipative quantum transport simulations using Non-equilibrium Green's Function (NEGF) formalism to study the scalability and performance of monolayer/multilayer 2D FETs. The study covered the effects of gate underlap, scattering strength and carrier effective mass and concluded that the high mobility and low effective mass of WSe_2 is suitable for both high-performance and low-standby-power transistor applications up to 5.9 nm technology node. The work used HfO_2 as both the top and bottom gate oxide and ensured a high source/drain doping of 6.5×10^{13} cm^{-2} in order to maintain ohmic source/drain contacts. According to this study, 2D FETs has the potential to follow the ITRS roadmap up to the year 2026.

In 2015 Ilatikhameneh et al. [78] developed a scaling theory for electrically doped 2D transistors using full band atomistic NEGF simulations that revealed that for WSe_2 TFET the same EOT but different oxide thicknesses can result in three order of magnitude difference in on-current. The work also revealed that both physical thickness of the oxides and spacing between the gates are major performance parameters for electrically doped 2D TFETs, with the former being most important.

In 2014 Majumdar et al. [79] simulated a non-planar double gate FET structure with monolayer TMDC channel using an effective mass based Hamiltonian (H) and NEGF formalism. The proposed FinFET-compatible non-planar structure has SiO_2 as fin oxide surrounding the TMDC channel. The source/drain doping, EOT of the oxide and monolayer thickness of the channel are considered 9×10^{12} cm^{-2}, 0.7nm and 0.65 nm respectively. Simulation revealed that, both over-the-barrier thermionic and direct source-drain tunneling currents govern the characteristics of such ultra scaled devices.

In 2013 Kumar et al. [80] investigated the electron transport properties of layered TMDC FETs with non-equilibrium Green's Function (NEGF) formalism using DFT Hamiltonian. The transport characteristics are calculated using the well known Landauer-Buttiker formula [81].

In 2014 Zhang et al. [82] performed a simulation study on valley-polarized current generation and transport in monolayer WSe_2 transistors. To simulate the TMDC transistor, this work used DFT calculations carried out within the Keldysh non equilibrium Green's function (NEGF) formalism [83–85]. It was estimated that to make WSe_2 valley transistors with perfect valley polarization at least 50-100 nm channel length is required depending on the applied gate bias voltage.

2.2 Analytical and Compact Modeling

Analytical and compact modeling can give better insight into the operation of a device. For monolayer TMDCs classical transport models will not be appropriate because of the presence of high degree of confinement. The quantum model can be easily formulated by assuming that the potential drop at the ultrathin channel in the confinement direction is negligible. Also, the potential across the channel can be accurately approximated as a quadratic function of the dimension. Using this approximation and solving Schrödinger and Poisson equation analytically can give the surface potential profile and hence the current transport across the channel. For modeling threshold voltage only semiclassically approximated charge can be used to obtain simplified closed form equation. Once the primary analytical model is developed various secondary effects like Mobility Degradation and Interface Traps etc. can also be incorporated into the model.

In 2012 Jiménez et al. [86] presented a physics-based model for the surface potential and drain current for monolayer TMDC FET. The work took the 2D density-of-states of the monolayer TMDC and its impact on the quantum capacitance into account and modeled the surface potential. The authors further developed an expression for the drain current considering the drift-diffusion mechanism. The analytical expressions of surface potential and drain current derived in this work are applicable for both the subthreshold and above threshold regions of operation. Although the analytical model is benchmarked against a prototype TMDC transistor, it has some major limitations like non-scalability due to lumped capacitor network based intrinsic device characteristics and in sufficient differentiation between Fermi potential (voltage) and electrostatic potential in the model.

In 2014 Cao et al. [38] presented an analytical I-V model for 2D TMDC FETs as well. The model takes physics of monolayer TMDCs into account and offers a single closed form expression for all three i.e. linear, saturation, and subthreshold regions of operation. The authors also incorporated various non-ideal secondary effects like interface traps, mobility degradation, and inefficient doping in the model, although that resulted in current equations having an integral form instead of closed form. The compact analytical model has been benchmarked against both numerical device simulation and experimental result.

In 2015 Najam et al. [87] introduced a surface potential-based low-field drain current compact model for 2D TMDC FET taking dielectric interface traps into account. In this work, the derived drain current model is capable of self-consistently calculating the surface potential of the device and interface trap charge Q_{it} with the help of an experimentally reported interface trap distribution. The final current equation has a closed form and works well for all regions of operation.

2.3 Fabrication and Testing

Over the years many groups have experimentally demonstrated monolayer WSe_2 channel transistors. These work ranges from basic WSe_2 MOSFETs to advanced devices like WSe_2 based TFET, TMDC Heterostructure FET and so on. In this section few of those works have been introduced from the literature.

In 2012 Fang et al. [26] reported high performance p-type monolayer WSe_2 FET with chemically doped source and drain contacts and high-κ gate dielectrics. The FET had a Si substrate with 270 nm SiO_2 bottom oxide, 17.5 nm ZrO_2 top gate dielectric and Pd metal gate. At room temperature, the monolayer transistors exhibited an effective hole mobility of ~250 cm^2/V.s, subthreshold swing of ~60 mV/dec, and on-off current ratio of 10^6 with a channel length of 9.4 μm.

In 2015 Movva et al. [88] demonstrated dual-gated p-type few-layer WSe_2 FET with high work-function Pt source/drain contacts, Pd top gate and a hexagonal boron nitride top-gate dielectric. The devices achieved hole mobility and on-off current ratio of 140 cm^2/V.s and 10^7 respectively at room temperature. The WSe_2 layer is deposited on a SiO_2/Si substrate with a effective channel length of 6 μm and supported a maximum drive current of 5 μA/μm at -5 V top gate bias voltage.

In 2014 Tosun et al. [46] demonstrated a CMOS inverter by implementing both n and p-type inverter on the same WSe_2 flake for the first time. In the p-FET, high work function Pt is used to inject hole at the source contact of WSe_2. Whereas, the n-FET is formed by degenerately doping the Pt-WSe_2 contact by Potassium (K). Both the n and p-type FETs achieved an on-off current ratio of 10^4 and the DC gain of the inverter was measured to be greater than 12. The inverter had ZrO_2 top gate dielectric and 10 nm thick WSe_2 flake grown on SiO_2/Si substarte. The effective channel length was 2 μm with a gate underlap and overlap at the source/drain contacts of n and p-FET respectively.

In 2013 Banerjee et al. [39] demonstrated a back gated monolayer WSe_2 n-FET on a 72 nm Al_2O_3/Si substrate. The device utilized Ag (10 nm)/Au (100 nm) for source/drain contact which provides excellent contact resistances with doped monolayer WSe_2. The fabricated n-FET had channel length and width of 1.5 μm and 1 μm respectively and displayed on-current of 110 μA/μm and mobility of 48 cm^2/V.s.

In 2014 Zhao et al. [45] demonstrated air stable p-type doped WSe_2 FET using covalent functionalization. The p-FET had a 7 nm thick WSe_2 flake grown on 260 nm thick SiO_2 on Si substrate using mechanical exfoliation with a varying channel length from 500 nm -2 μm. P-doping of WSe_2 was achieved through the chemical absorption of NO_x at 150˚C leading to a maximum hole concentration of 10^{19} cm^{-3}. This degenerate p-type doping enabled 5 orders of magnitude contact resistance reduction at Pd-WSe_2 source/drain contacts.

In 2014 Chen et al. [44] demonstrated air stable n-doped 2 μm channel WSe_2 FET using positively charged SiN_x films at 150˚C. The top SiN_x and bottom SiO_2 gate dielectrics had thicknesses of 50 m and 260 nm respectively. The SiN_x film with positive charge centers is deposited on the WSe_2 surface using Plasma Enhanced Chemical Vapor Deposition (PECVD) which electrostatically induced electrons at the WSe_2 channel. The fixed positive charge is controllable by flows and ratios of NH_3 and SiH_4 gases used to form the SiN_x. Highest fixed positive charge at SiN_x top layer and electron mobility in the WSe_2 channel achieved is this device are 1.75×10^{12} cm^{-2} and 70 $cm^2/V.s$ respectively.

In addition to those devices described above, MoS_2/WSe_2 [89-90] and SnS_2/WSe_2 [91] heterojunction transistors have been demonstrated recently by Prof. Palacios's group in MIT. The same group demonstrated high performance WSe_2 CMOS devices in 2015 [92]. In 2015 Li et al. [93] proposed a $WSe_2/SnSe_2$ heterojunction Thin-TFET structure which displayed a remarkable 14 mV/dec subthresold swing and 300 μA/μm on current.

2.3.1 Deposition

Deposition of Monolayer WSe_2 can be done on a SiO_2/Si, Graphene or BN substrate by 'Mechanical Exfoliation' of bulk TMDC crystal or Chemical Vapor Deposition (CVD) process. Over the year several methods have been introduced in the literature to deposit the height quality monolayer WSe_2 in an easily controllable and scalable manner.

In 2012 Fang et al. [26] applied 'Mechanical Exfoliation' method to deposit monolayer WSe_2 from bulk WSe_2 crystals on a 270 nm thick SiO_2/Si substrate. Atomic Force Microscope (AFM) measurements revealed the thickness of the monolayer to be around 0.7 nm, which agrees with the crystallographic data of WSe_2. The growth process is described below-

1. Using mechanical exfoliation via scotch tape WSe_2 layers are transferred onto a Si/SiO_2 substrate.
2. Transferred WSe_2 is submerged in acetone for 1 hour to remove the tape residues.
3. Source/drain metal contacts is deposited by lithography and metallization of Pd/Au of length 20-30 nm.
4. Gate electrodes is then patterned by E-beam Lithography using PMMA positive resist and keeping 300 - 500 nm underlap near the source/drain contacts.
5. As the top gate dielectric, 17.5 nm thick ZrO_2 is deposited at 120 ºC using ALD process.
6. Pd top gate is deposited using metallization.
7. Device is exposed to a NO_2 to p-dope the underlapped S/D regions for better contact resistances. Channel remains almost intrinsic but can be p-doped by exposing it to NO_2 environment before the ZrO_2/Pd is placed.

In 2013 Huang et al. [94] demonstrated synthesis of large-area and highly crystalline WSe_2 monolayers for device application using gas phase selenization of WO_3 in a hot-wall CVD chamber. The process of WSe_2 synthesis (as shown in Figure 2.1) is described below-

1. WO_3 powder is placed in hot-wall CVD furnace.
2. Sapphire substrate is placed inside the deposition chamber in the direction of the flow.
3. Furnace is heated up to 950˚C.
4. Selenium (Se) and Ar/H_2 gas mixture is passed through the hot CVD furnace over the sapphire substrates. H_2 plays an important role in activating the Selenization process.
5. Near the furnace where temperature is around 850˚C, triangular WSe_2 flakes with lateral domain dimension from 10 μm and to 50 μm is deposited on the Sapphire substrates. These large flakes are mostly monolayer, with occasional presence of bilayer WSe_2 as well.
6. On the Sapphire substrates slightly distant from the furnace have temperatures around 750˚C. On these substrates, monolayer WSe_2 film with relatively small domain size (lateral dimension < 5 μm) is grown. The thicknesses of these films are 0.73 nm, which is in agreement with the thickness of mechanically exfoliated monolayer WSe_2.

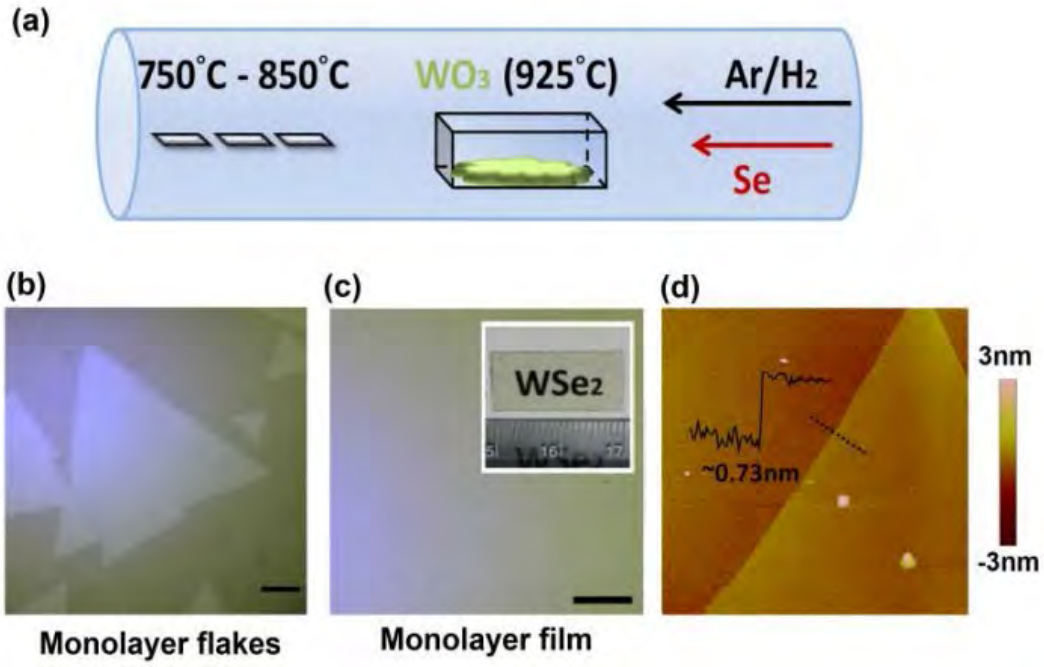


Figure 2.1: Synthetic large scale growth of monolayer WSe_2. **(a)** CVD growth of WSe_2 in the process of Selenization of WSe_2 powers in a hot-wall CVD furnace. **(b)** Monolayer WSe_2 flakes on Sapphire substrate at 850˚C (optical microscope image). **(c)** Monolayer WSe_2 films on Sapphire substrate at 750˚C (optical microscope image). **(d)** AFM image of monolayer WSe_2 on a Sapphire substrate grown at 850˚C. (Image courtesy Huang et al. [94])

In 2014 Eichfeld et al. [95] demonstrated a scalable synthesis method of large-area, mono and few-layer WSe_2 using Metal Organic Chemical Vapor Deposition (MOCVD). This method allows better control of the vapor-phase chemistry unlike the WO_3 powder vaporization CVD technique described earlier. In addition, a wide range of substrates including Epitaxial and CVD Graphene, Sapphire, and Boron Nitride are acceptable in this method. This work also studied the impact of temperature, pressure, Se:W ratio, and substrate on the atomic structure and properties of the deposited WSe_2. The growth process is described below-

1. The deposition process starts with the placement of Tungsten Hexacarbonyl ($W(CO)_6$) and Dimethylselenium ($(CH3)_2Se$) precursors in a vertical cold wall reactor with an induction heated susceptor.
2. The precursors are transported into reactor using a bubbler manifold which allows independent control over each precursor concentration.
3. H_2/N_2 mixtures are used as carrier gas.
4. The sample precursors are heated to 500˚C and kept at this temperature for 15 min to remove any water vapor. The temperature was increased at a rate of 80˚C/min.
5. The temperature of the precursors is then raised to growth temperature ranging from 600˚ to 900˚C and then they are introduced to the reaction chamber.
6. Monolayer WSe2 is allowed to grow on the substrate at a pressure of 100 to 700 Torr for 30 minutes.
7. Se and W concentrations are varied by the flow rate of carrier gas and the pressures of the bubblers. Bubblers temperature was kept constant at 23˚C.
8. Upon completion of the growth the samples are cooled down to ambient temperature.

In 2015 Wang et al. [96] presented a scheme to create 2D van der Waals heterostructures by pick-up and transfer method using prepatterned hexagonal Boron Nitride (hBN) mask capable of creating complex heterostructure. Material grown in this method does not require thermal annealing, which allows use of materials with low melting point. Through independent gating of the contact region by ionic liquid, this work demonstrated highest Hall mobility of 330 $cm^2/V.s$ to date in a few-layer WSe_2 device.

In 2014 Lin et al. [97] reported the synthetic growth of crystalline monolayer WSe_2 on Epitaxial Graphene. Characterization of the grown material revealed high-quality WSe_2 monolayers and atomically sharp WSe_2-Grahene interface. Transport measurements along the growth direction also proved the existence of interlayer gap induced barrier at the WSe_2-graphene interface in addition to the expected conduction band offset. The work concluded that, the structural, chemical, and optical properties of WSe_2 grown on Epitaxial Graphene are as good, if not better than the mechanically exfoliated WSe_2 films.

2.3.2 Choice of Top Gate Oxide

Direct deposition of various High-κ materials like Hexagonal BN, Al_2O_3, HfO_2 and ZrO_2 are possible on TMDCs using ALD [26, 39, 44, 45-46, 88].

2.3.3 Choice of S/D Metal

Choice of S/D metal is a critical for TMDCs. It is found to be extremely difficult to form ohomic metal contact with monolayer TMDCs. Although various metal like Pd, Ag, Ni, Au, Ti etc. can form Schottky Barrier contact with monolayer TMDCs, to keep the contact resistance low special consideration must be made. For example, WSe_2 channel with Pd S/D gives a low contact resistance for hole transport but high contact resistance for electron transport, since it has a high work function [26, 28, 58].

On the other hand Ti or Au S/D allows both electron and hole transport with poor magnitude [26]. This ambipolar transport makes Ti or Au with monolayer TMDCs unusable for digital logic and low power applications. Due to extreme Fermi Level Pining in monolayer TMDCs and metal interfaces, using same metal for both n and p-type transport is not possible. For example, Pd with WSe_2 shows p-transport whereas MoS_2 with Pd shows n-transport dominantly. To make n-transport possible through WSe_2, Au should be used with degenerately doping S/D contacts [46]. The In and Ag based contacts exhibit the smallest contact resistivity and the highest drive current in WSe_2 channel [37]. Degenerately doping S/D contacts improve the contact resistances by decreasing the SB height and barrier thickness. p-type doping of WSe_2 using metallic (Pt) Nano-particless has also been demonstrated [98].

2.3.4 Doping

Channel Doping can be done electrostatically by biasing the back gate with appropriate voltage. But that usually requires high back gate voltages. Alternatively, for n-doping the channel PECVD can also be used to deposit top oxide (for example SiN_x) [44] with positive fixed charge centers which will attract electrons in the channel. On the other hand, it is possible to heavily p-dope WSe_2 by exposing it to NO_2 at temperature as high as 150°C for 4-12 hrs and allowing chemisorptions [45].

Physical absorption of electron-withdrawing and -donating species like NO_2 and K respectively can also dope the channel to p-type [26] and n-type [46]. But this kind of surface doping technique is not stable when exposed to ambient air and hence the active regions need to be encapsulated after doping. S/D contact regions (gate underlap regions at both side of the channel) are also needed to dope heavily to achieve low contact resistance [46]. This also can be done by degenerate surface doping.

2.3.5 Characterization and Testing

To characterize the monolayer WSe_2 device and determine different performance parameters various testing and measurements are performed. All electrical measurements and characterization on WSe_2 FETs are usually performed under vacuum condition to preserve the surface doping concentrations in the channel. Raman spectroscopy, Atomic Force Microscopy (AFM), and cross-sectional Transmission Electron Microscopy (TEM) is used to confirm the number of layers in the deposited WSe_2 flakes and the film thickness [95, 99]. In addition to these, to characterize various structural, chemical and geometric properties of WSe_2 monolayer X-ray Absorption Spectrum (XAS), X-ray Photoelectron Spectrum (XPS), X-ray Diffraction (XRD) is used [45]. Photoluminescence (PL) characterization is performed for compositional and optical analysis [45]. To check the surface topology and growth quality of the WSe_2 optical microscopy is used [94]. For electrical measurement, semiconductor parameter analyzer is used.

Chapter 3

Quantum Mechanical Electrostatics and Transport Simulation

In this chapter, a Quantum Mechanical electrostatics and transport simulation study on monolayer WSe_2 FET has been performed and different performance parameters have been calculted. Firstly, 1-D Schrodinger-Poisson equations have been solved self-consistently [100] along the direction perpendicular to the channel to get the gate capacitance-voltage characteristics of the device. Then, ballistic transport characteristics were obtained by Fast Uncoupled Mode Space (FUMS) approach using Non-Equilibrium Green's Function (NEGF) formalism [47-48].

3.1 Device Structure

The device structure considered in this work is a downscaled nFET version of the device fabricated by Fang et al. [26]. It has a 0.7 nm thick monolayer WSe_2 channel of length 20 nm deposited on a 5 nm thick layer of SiO_2. A 3 nm thick layer of ZrO_2 serves as the top oxide of the device (Figure 3.1). The metallic (Au) source/drain length is taken as 10 nm. Above the top oxide a metallic top gate of Palladium (Pd) is placed. The channel doping density is $1x10^{25}$ m^{-3}.

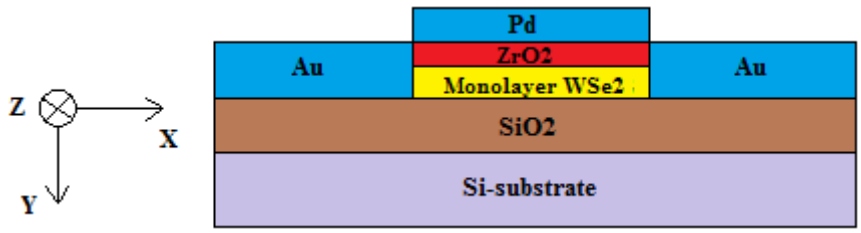


Figure 3.1: 2D cross section of the monolayer WSe_2 channel FET with channel length of 20 nm and top and bottom oxide thickness of 3 nm and 5 nm respectively.

3.2 Simulator Development

3.2.1 Self-consistent Electrostatic Simulation

To obtain the electrostatics of the device, 1D Schrödinger and Poisson equations are solved self-consistently in the direction perpendicular to the channel (along y-axis). Schrödinger's equation as given by the effective mass approximation,

$$(-\frac{\hbar^2}{2m_{ds}^*}\nabla^2 - qV(y))\psi_j(y) = E_j\psi_j(y) \tag{3.1}$$

where, q is the charge of electron, m_{ds}^* is the density of states effective mass and E_j and ψ_j are the minimum energy and corresponding wave function of the j^{th} sub-band respectively.

Poisson's equation is given by,

$$-\nabla.\ (\varepsilon\,\nabla V) = \rho \tag{3.2}$$

where, V is the channel potential, ε is the channel dielectric permittivity and ρ is the channel charge density.

3.2.1.1 Self-Consistent Charge Calculation

In the electrostatics simulator, Schrodinger and Poisson equation are solved self-consistently [100] considering wave function penetration and other quantum effects. Firstly, Schrodinger equation is solved for the equilibrium band structure. Then from the derived energy states and wave functions, inversion carrier concentration in the channel region is calculated from the following expression,

$$n(x, y) = \sum_j \int_{Ej}^{\infty} D_j(E)\, f_j(E)\, |\psi_j(x, y)|^2\, dE \tag{3.3}$$

where, j is the number of sub-band, $D_j(E)$ is 1D density of states and $f_j(E)$ is Fermi-Dirac distribution function with respect to Fermi level of the channel region. $D_j(E)$ and $f_j(E)$ are respectively given by the well-known equations,

$$D_j(E) = \frac{m_{ds}^*}{\pi\hbar^2}\sum_j \theta(E - E_j) \tag{3.4}$$

$$f_j(E) = \frac{1}{1+e^{\left(\frac{(E-E_F)}{kT}\right)}} \tag{3.5}$$

here, $\theta(E - E_j)$ is the unit step function. Using the inversion charge from Equation 3.3, charge density $\rho(y)$ is calculated as-

$$\rho(y) = q(-n(y) - N_A) \tag{3.6}$$

where, N_A is the p-type doping concentration of the channel region. With the charge density from Equation 3.6, Poisson's equation is solved and the band structure is modified using the newly obtained potential profile. Starting with zero initial charge profile, the charge and potential profile of the 1D cross section is updated after each iteration using *mixing coefficient* ($\alpha = 0.04$) until self-consistency is achieved. The updated value of potential profile is calculated using the following formula,

$$V^i_{final} = V^{i-1}_{final} \times \alpha + V^i_{new} \times (1-\alpha) \tag{3.7}$$

where, V^{i-1}_{final} and V^i_{new} is the potential profile of $(i-1)^{th}$ and i^{th} iteration respectively. Once the solution converges, the charge distribution inside the device can be determined.

3.2.1.2 C-V Characterization

For 1D cross section, constant potential distribution along z-direction (along the width of the device) is assumed. Gate capacitance per unit channel area is,

$$C_G = \frac{dQ_{WSe_2}}{dV_G} \tag{3.8}$$

where, Q_{WSe_2} is the charge deposited inside WSe_2 which is obtained from,

$$Q_{WSe_2} = \int_y \rho(y)dy \tag{3.9}$$

C-V characterization is done only for inversion region. The C-V characteristics are found from the rate of change of Q-V curve. The curve tend to saturate to the value of top gate oxide capacitance,

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{t_{tox}} \tag{3.10}$$

here, t_{tox} is the top gate oxide thickness and $\varepsilon_0 \varepsilon_r$ is the dielectric permittivity of the channel.

3.2.2 Transport Simulation with First Uncoupled Mode Space (FUMS) Based NEGF Approach

The 2D Transport simulator is developed using FUMS [47-48] approach. Here, 2D Poisson equation is solved using initially approximated charge to get the potential energy *U(x,y)*. Then average potential energy along the confinement direction (y-axis) is obtained as,

$$\overline{U(y)} = \frac{1}{L_x}\int_0^{L_x} U(x,y)dx \tag{3.11}$$

where, L_x is the length of the device. This average potential is substituted into the 1D Schrödinger equation along the confinement direction-

$$\left[-\frac{\hbar^2}{2m_y^*}\frac{d^2}{d^2y} + \overline{U(y)}\right]\overline{\psi^m}(y) = \overline{E_{sub}^m}\,\overline{\psi^m}(y) \tag{3.12}$$

which gives the average subband energy ($\overline{E_{sub}^m}$) and wave function ($\overline{\psi^m}(y)$) for m[th] subband. In FUMS [47] approach, the wave function is considered same as $\overline{\psi^m}(y)$ throughout the transport direction (along x-axis). Whereas the Eigen Energies are approximated using First Order Perturbation Theory [48]-

$$E_{sub}^m(x) = \overline{E_{sub}^m} + \int_y U(x,y)|\overline{\psi^m}(y)|^2dy - \int_y \overline{U(y)}|\overline{\psi^m}(y)|^2dy \tag{3.13}$$

From the $E_{sub}^m(x)$ 1D device Hamiltonian (H) [48] along the transport direction is formed. Now the retarded Green's function can be calculated as-

$$G^m(E) = (EI - H - \Sigma_S^m(E) - \Sigma_D^m(E))^{-1} \tag{3.14}$$

where, I is an identity matrix, $\Sigma_S^m(E)$ and $\Sigma_D^m(E)$ are the self energy matrices representing interaction of the channel with source and drain contacts. The spectral density matrices at source and drain contacts can be calculated as-

$$A_S^m(E) = G^m(E)\Gamma_S^m(E)G^{m\dagger}(E) \;\; and \;\; A_D^m(E) = G^m(E)\Gamma_D^m(E)G^{m\dagger}(E) \tag{3.15}$$

where, $\Gamma_S^m(E)$ and $\Gamma_D^m(E)$ are the spectral broadening matrices at source and drain contacts given by-

$$\Gamma_S^m(E) = i\left(\Sigma_S^m(E) - \Sigma_S^{m\dagger}(E)\right) \;\; and \;\; \Gamma_D^m(E) = i\left(\Sigma_D^m(E) - \Sigma_D^{m\dagger}(E)\right) \tag{3.16}$$

The 2D electron density can now be calculated as-

$$n_x^m = \frac{1}{2\pi a} 2\left(\frac{2m_z^* k_B T}{\pi \hbar^2}\right)^{1/2} \int_{-\infty}^{\infty} \left[\mathfrak{F}_{-1/2}\left(\frac{\mu_S - E}{k_B T}\right) diag\left(A_S^m(E)\right)\right.$$

$$\left. + \mathfrak{F}_{-1/2}\left(\frac{\mu_D - E}{k_B T}\right) diag\left(A_D^m(E)\right)\right] dE \tag{3.17}$$

where, m_z^* is the transverse effective mass (along z-axis), μ_S and μ_D are source and drain Fermi levels respectively and a is the size of the unit cell of monolayer WSe_2. Function $\mathfrak{F}_{-1/2}$ denotes Fermi-Dirac integral of order $-1/2$. 3D electron density is obtained by multiplying n_x^m with the transverse wave function $|\overline{\psi^m}(y)|^2$.

$$n_{3D}^m(x, y) = n_x^m \, |\overline{\psi^m}(y)|^2 \tag{3.18}$$

The total electron density is obtained by summing the above equation for all subbands. The ballistic current is calculated as-

$$I = \frac{q}{2\pi\hbar} 2\left(\frac{2m_z^* k_B T}{\pi \hbar^2}\right)^{1/2} \int_{-\infty}^{\infty} \left[\mathfrak{F}_{-1/2}\left(\frac{\mu_S - E}{k_B T}\right) - \mathfrak{F}_{-1/2}\left(\frac{\mu_D - E}{k_B T}\right)\right] T(E) dE \tag{3.20}$$

where, T(E) is obtained by summing the transmission coefficient $T^m(E)$ over all subbands. $T^m(E)$ is given by-

$$T^m(E) = trace(\Gamma_S^m(E) G^m(E) \Gamma_D^m(E) G^{m\dagger}(E)) \tag{3.21}$$

3.2.3 COMSOL Multiphysics

To solve the Schrödinger and Poisson equation PDE solver of COMSOL Multiphysics [75] has been used. Firstly the device geometry was drawn in COMSOL with each segment (drain, source, channel, oxide etc.) of the device defined as separate subdomain. Then the material parameters are included in the 'Subdomain Settings'. The boundary conditions (bias voltage, wave functions) of the device are then added using the 'Boundary Settings'. After that 'Mesh' is initialized and refined to define the numerical data point that will define the geometry. Finally, the built-in FEM solver in COMSOL is invoked to solve the PDE problem. Once that is complete, the COMSOL file is used to generate separate MATLAB 'm-files' for both Schrödinger and Poisson equations. These files contain all the physics and geometry of the device which can be compiled in MATLAB with COMSOL in coupled mode. The results from COMSOL generated m-files are then used to complete the self-consistent loop in MATLAB which calculates the necessary carrier density, band profile to sustain the simulation until convergence occurs.

3.2.3.1 Solving Poisson's Equation

In COMSOL Multiphysics, Poisson's equation in general co-efficient form in three dimensions is given by

$$-\nabla.\ (c\,\nabla u) = f \tag{3.22}$$

Where, c is the Diffusion Co-efficient, f is the source term and u is the independent variable. Comparing with the original Poisson's equation in Equation 2 we get,

$c \equiv \varepsilon_0\varepsilon_r$ is the dielectric permittivity

$u \equiv V(y)$ is the electrostatic potential

$f \equiv \rho(y)$ is the charge density

For 1D,

$$\nabla \equiv y\frac{\partial}{\partial y} \tag{3.23}$$

At the external boundaries of the gates *Dirichlet* i.e. fixed voltage boundary condition is used. *Neumann* i.e. continuous electric flux boundary condition is used at all internal boundaries.

3.2.3.1 Solving Schrödinger's Equation

Schrödinger's e quation defined i n C OMSOL M ultiphysics i n ge neral co-efficient fo rm i s given by,

$$-\nabla.(c\nabla u) + au = \lambda u \tag{3.24}$$

Comparing with the original Schrödinger's equation in Equation 1 we get,

$$c \equiv \frac{\hbar^2}{2m_{ds}^*} \tag{3.25}$$

a ≡ Electrostatic potential, V

λ ≡ Eigen Energies, E_j

u ≡ Wave function, ψ_j

For S chrödinger's e quation, a ll bounda ries a re ke pt a s ope n bounda ries t o a llow w ave function penetration.

3.2.4 Material Parameters

To model the monolayer WSe_2 channel FET, band structure and material parameters available in the literature from first principle DFT simulations of Monolayer WSe_2 sheets have been used. Same electron effective mass has been considered for both longitudinal and transverse direction of monolayer WSe_2. Also only one subband and lowest conduction valley was taken into consideration.

Figure 3.2(a) and 3.2(b) displays Bulk WSe_2 and monolayer sheet of WSe_2 respectively [101]. The Bulk material has an indirect bandgap of 1.2 eV [102-103] and layers are connected by van der Walls force. On the other hand, the monolayer WSe_2 has significantly higher bandgap of 1.6 eV [102-103]. Although the Se-W atoms are not in one plane as shown in (b), the bird's eye view of Monolayer WSe_2 shows the signature Graphene-like hexagonal lattice structure of monolayer Transition Metal Dichalcogenides (i.e. MoS_2, WSe_2). Table 3.1 summarizes some of the monolayer WSe_2 channel parameters.

Figure 3.3(a) shows the E-k diagram of monolayer to 3-layers of WSe_2 obtained from first principle DFT simulations [101] using ATK. On the other hand, Figure 3.3(b) displays he simulated [101] E-k diagram of bulk WSe_2. The bulk bandgap shown in the Figure 3.3(b) is 0.9eV, which is slightly underestimated from the bulk bandgap reported abobe. This apparent underestimation of bandgap is an artifact of DFT simulations [104]. The E-k diagrams in Figure 3.3 clearly show the transition of WSe_2 from indirect to direct bandgap material as the number of layer reduces.

Table 3.1: Monolayer WSe_2 Parameters Extracted from Literature

Property	Value
Thickness [26]	0.7 nm
Bandgap, E_g [101]	1.6 eV
Dielectric Permittivity [50]	7.25 $\parallel$ 5.16 $\perp$
Electron Affinity [101]	3.9 eV
m^*_e [101]	$0.33m_0$
m^*_h [101]	$0.45m_0$

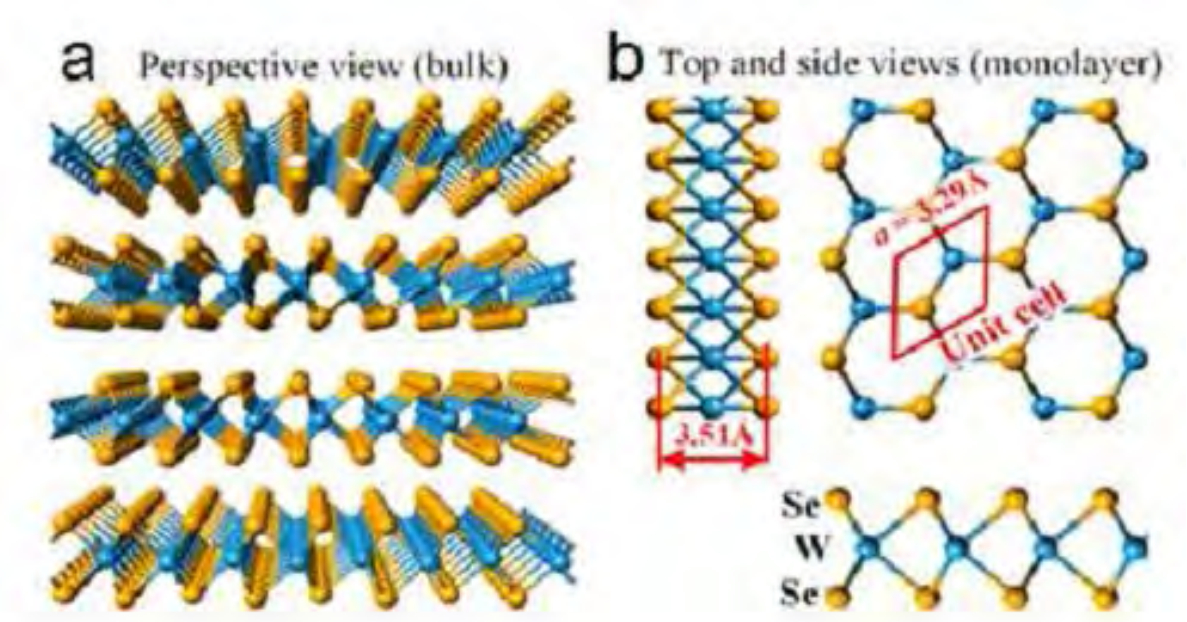


Figure 3.2: (a) Bulk WSe_2 and **(b)** monolayer sheet of WSe_2 [101].

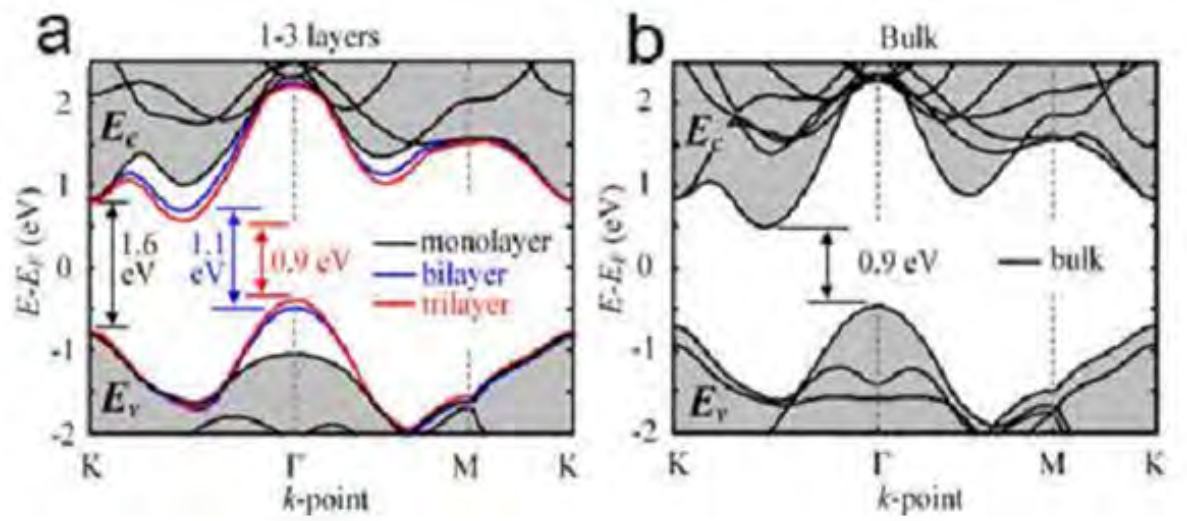


Figure 3.3: E-k diagram of **(a)** few layers of WSe_2 and **(b)** bulk WSe_2 obtained from the atomistic simulation of WSe_2 [101] using DFT simulation in ATK [52]. It is to be noted that, the bulk bandgap shown here is slightly underestimated than the actual bulk bandgap of 1.2 eV, which is an inherent limitation of DFT simulations.

3.3 Results and Discussions

3.3.1 Simulator Validation

The simulator is validated by comparing results from this simulator to the reported results of Yoon et al [27]. The device simulated by Yoon et al. is a monolayer MoS_2 based transistor with gate length of 15 nm having 2 nm gate under lap at each side of the channel. It has metallic source/drain and top gate. The top oxide is 2.8 nm thick HfO_2 and SiO_2 serves as the bottom oxide. The exact device is simulated with this simulator and the 1st subband energy profile across the channel has been compared for V_G=0 and V_D=0.5 V in Figure 3.4. The match is quite convincing at the top of the barrier. Although there is a slight mismatch at the drain end, this will not affect the current output much since it depends mostly on the height of the barrier near source end.

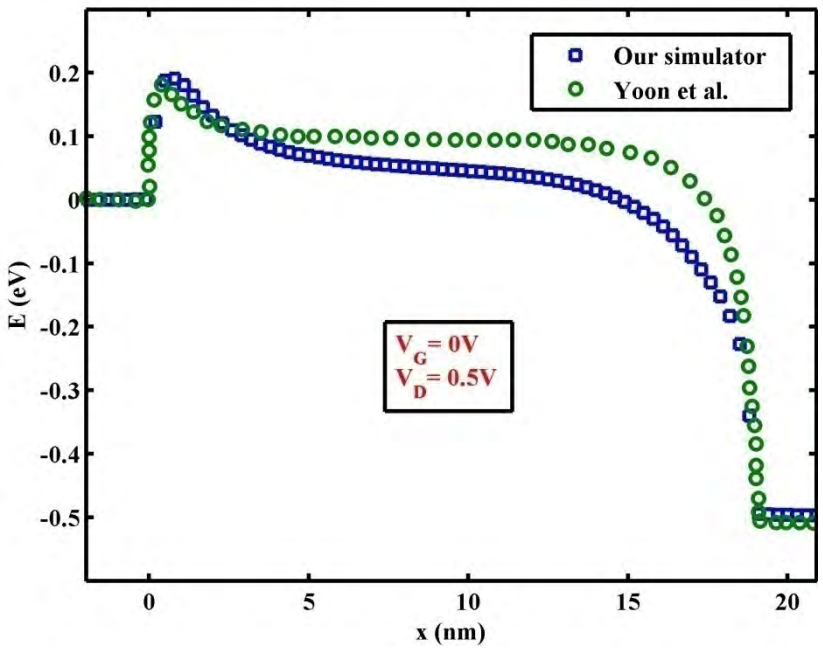


Figure 3.4: First subband energy across the channel for the monolayer MoS_2 channel device by Yoon et al. [27] at V_G=0 and V_D=0.5 V. Simulator described in this section gives similar results.

3.3.2 Electrostatic and Transport Characteristics

In this section some of the key results from Electrostatics and Transport Simulation described in this chapter will be presented.

3.3.2.1 Effect of Gate Voltage on 1st Subband Energy Profile

Figure 3.5 shows variation of 1st subband energy along the channel with different gate bias voltage combinations. In Figure 3.5(a), the drain voltage is kept fixed at 0V and gate bias is varied from -0.2V to 0.8V at 0.2V interval. In Figure 3.5(b), the drain voltage is kept fixed at 0.4V and gate bias is varied from -0.2V to 0.8V at 0.2V interval as well. These figures show that, change in top of the barrier is very rapid at lower gate voltages, indicating presence of low Subthreshold Swing below the threshold voltage.

3.3.2.2 Effect of Drain Voltage on 1st Subband Energy Profile

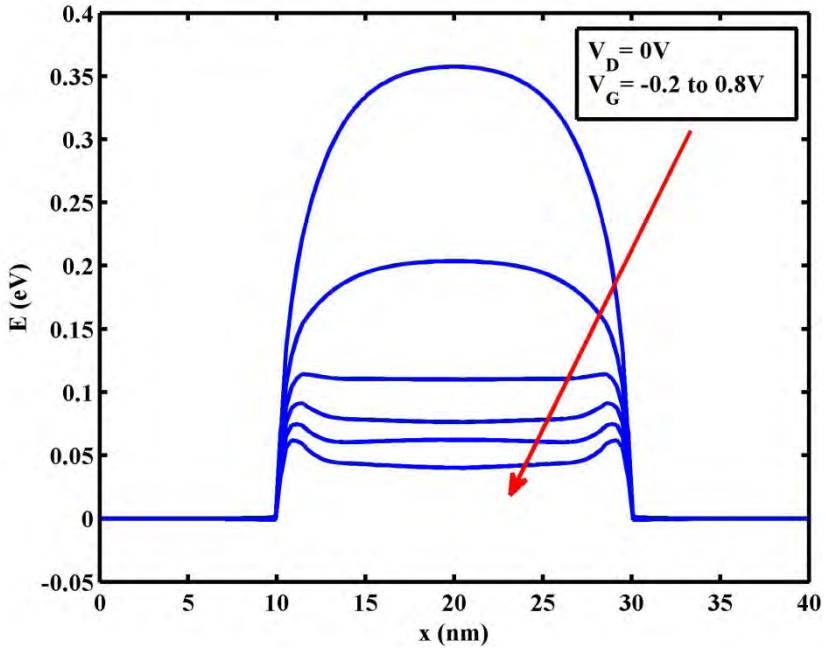
Figure 3.6 shows variation of 1st subband energy along the channel with different drain bias voltage combinations. In Figure 3.6(a), the gate voltage is kept fixed at 0V and drain bias is varied from 0V to 0.4V at 0.1V interval. In Figure 3.6(b), the gate voltage is kept fixed at 0.4V and gate bias is varied from 0V to 0.4V at 0.1V interval as well. These figures show that, variation of drain voltage does not affect the top of the barrier much, indicating presence of strong gate control over the channel and hence low DIBL.

3.3.2.3 Capacitance-Voltage and Current-Voltage Characteristics

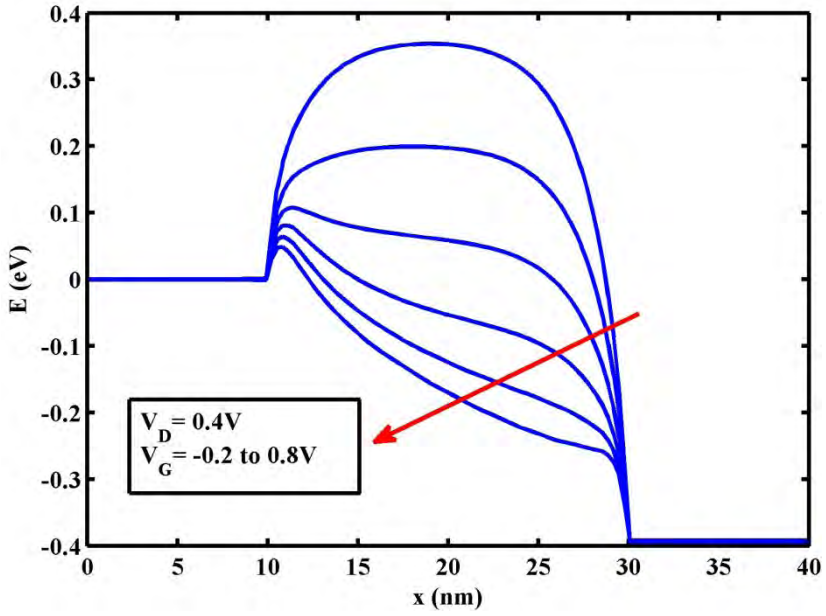
Figure 3.7(a) shows the drain current-voltage (I-V) characteristics of the device for different gate voltages. Peak current of 467.2 μA/μm is observed at $V_G=V_D=0.8$ V. The saturation region of the I-V curve also indicates low DIBL. On the other hand, Figure 3.7(b) shows the gate capacitance-voltage (C-V) characteristics of the device. The curve saturates at about 0.009 F/m^2, which is significantly lower than the gate oxide capacitance of 0.0369 F/m^2. This supports the presence of quantum capacitance in the channel in series with the gate oxide capacitance [105].

3.3.2.4 Transfer Characteristics and Transconductance

Figure 3.8(a) shows the transfer characteristics (I_d-V_{gs}) of the device for different drain voltages. Figure 3.8(b) on the other hand displays the tansconductance of the device under different drain voltages. The maximum tansconductance 887.7 μS/μm is obtained at drain voltage of 0.8V with a gate voltage of 0.6V.

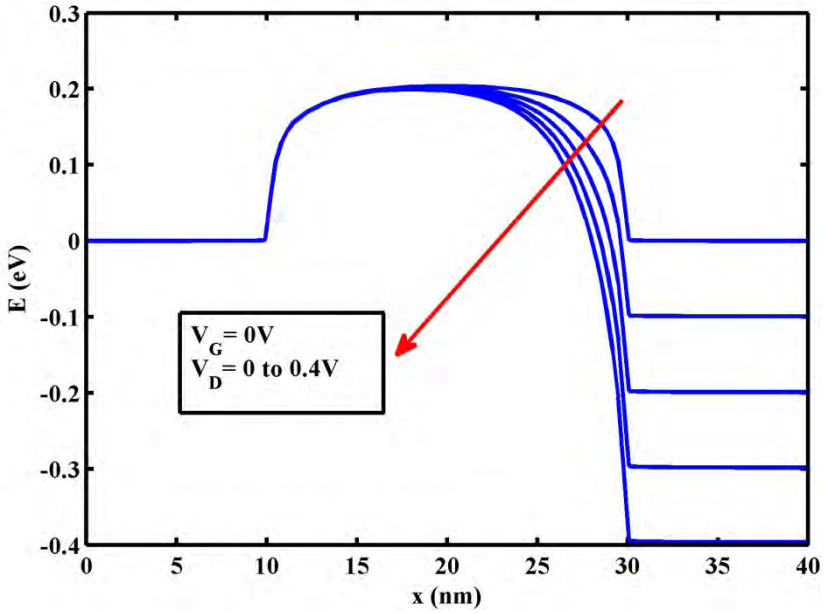


(a)

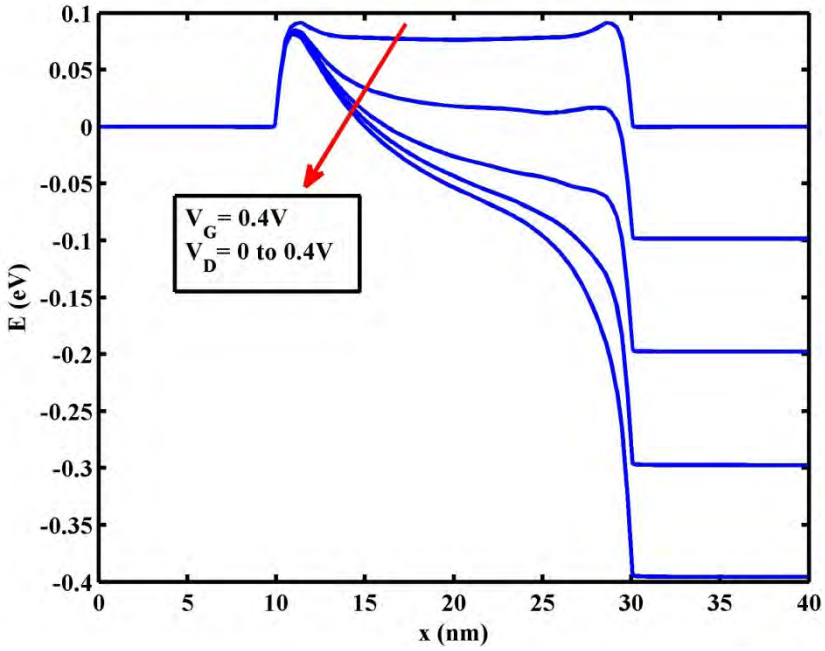


(b)

Figure 3.5: First subband energy profile across the channel with different gate bias conditions and fixed drain voltage of **(a)** 0V and **(b)** 0.4V.

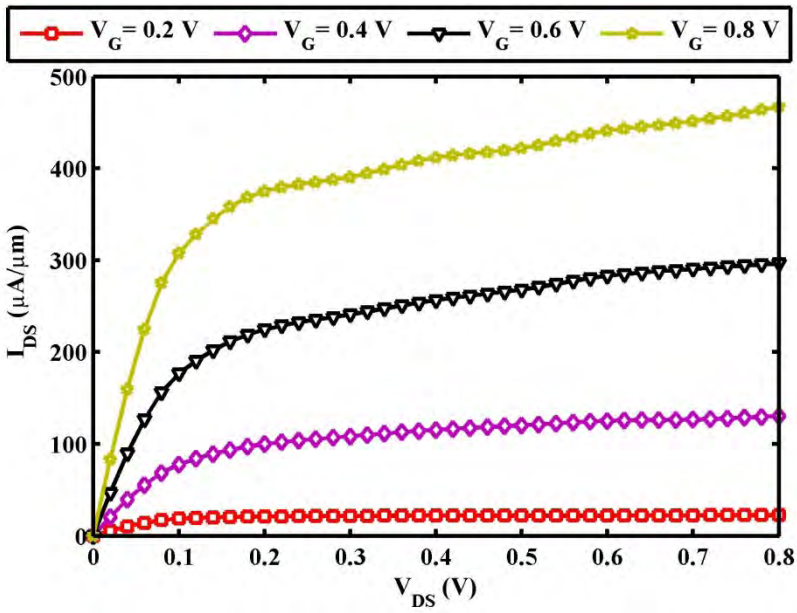


(a)

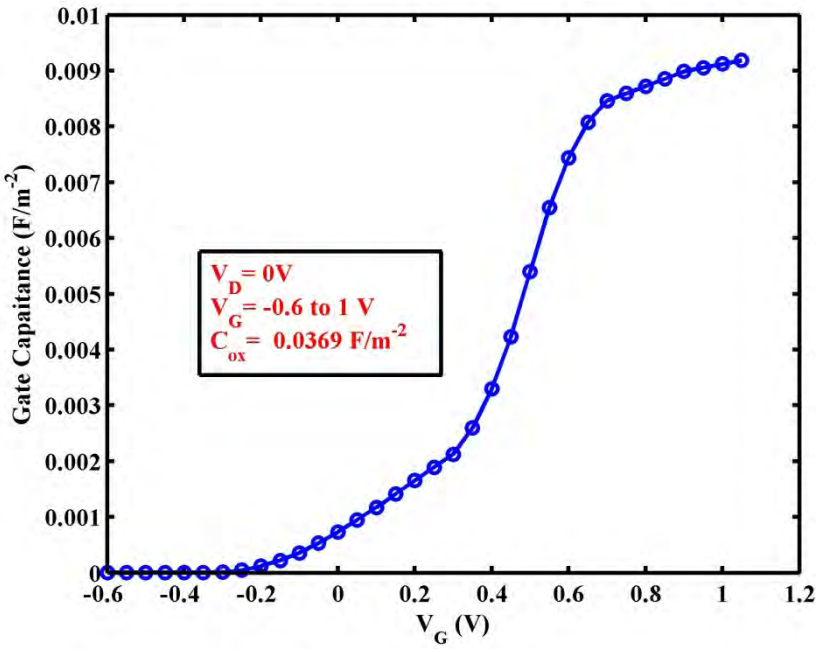


(b)

Figure 3.6: First subband energy profile across the channel with different drain bias conditions and fixed gate voltage of **(a)** 0V and **(b)** 0.4V.

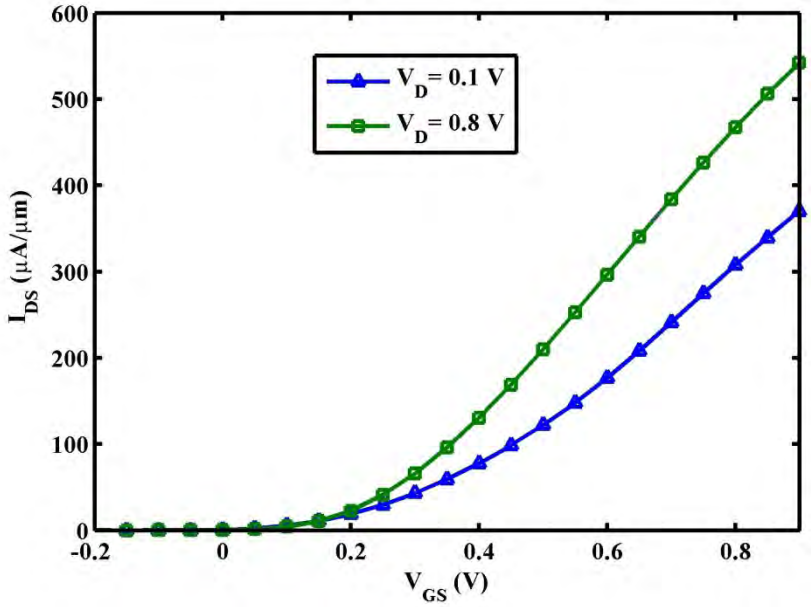


(a)

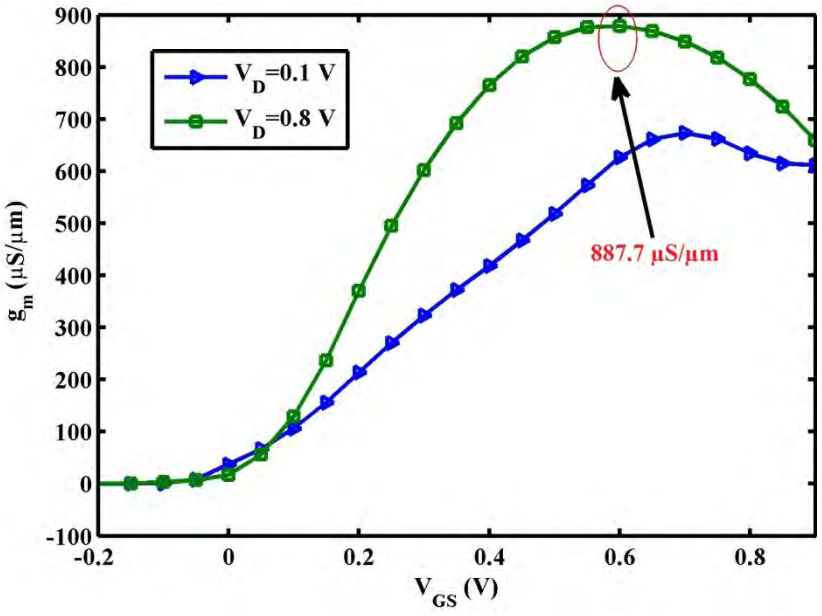


(b)

Figure 3.7: (a) Drain cu rrent-voltage ch aracteristics at d ifferent gate b iases **(b)** gate capacitance-voltage characteristics at zero drain voltage.



(a)



(b)

Figure 3.8: (a) Transfer characteristics **(b)** transcoductance profile at different drain voltages.

3.3.3 Parameter Extraction

In Figure 3.9 -3.12 different transport performance parameters of the device are extracted.

3.3.3.1 Extraction of Threshold Voltage (V_{th})

From Figure 3.9 the threshold voltage of the device is extracted from the x-incept of the extrapolated rising region of the $I_{ds} - V_{gs}$ curve. The threshold voltage varies with the drain bias voltage. For drain voltage of 0.8V threshold voltage is found to be 0.23V and for drain bias voltage of 0.1V it is 0.28V.

3.3.3.2 Extraction of Drain Induced Barrier Lowering (DIBL)

Drain Induced Barrier Lowering (DIBL) is calculated from $\log_{10}(I_{ds}) - V_{gs}$ as shown in Figure 3.10. DIBL is estimated as $\frac{\nabla V_{th}}{\nabla V_{DS}}$ [106], where ∇v_{th} is lateral shift of the $\log_{10}(I_{ds}) - V_{gs}$ curves in the subthreshold regime and ΔV_{DS} is the difference in corresponding drain voltages. Following the procedure DIBL is calculated as 14.91 mV/V, which is significantly lower than any conventional FET.

3.3.3.3 Extraction of Subthreshold Slope (SS)

Subthreshold Swing (SS) is calculated from the slope of $\log_{10}(I_{ds}) - V_{gs}$ curve [107] shown in Figure 3.11. From Figure 3.11 the SS is calculated as 77.72 mV/dec. This value is quite promising and very close to the theoretical limit of 60 mV/dec of such devices. SS can be further improved by using gate oxides with higher dielectric constants.

3.3.3.4 Extraction of On/Off Current Ratio

Figure 3.12 demonstrates that maximum ON/OFF current ratio of $\sim 10^{10}$ is obtainable form this device with an ON and OFF voltage of 0.8V and -0.6V respectively.

3.3.3.5 Extraction of Effective Mobility (μ_{eff})

Effective mobility of the device can be extracted from the equation [26] below using simulated current and extracted threshold voltage-

$$\mu_{eff} = \frac{\partial I_{Ds}}{\partial V_{DS}} \frac{L_{ch}}{C_{ox}(V_{GS} - V_{th} - 0.5V_{DS})} \tag{3.26}$$

Using Equation 3.26, the effective mobility of the device is found to be 300 cm^2/V.s.

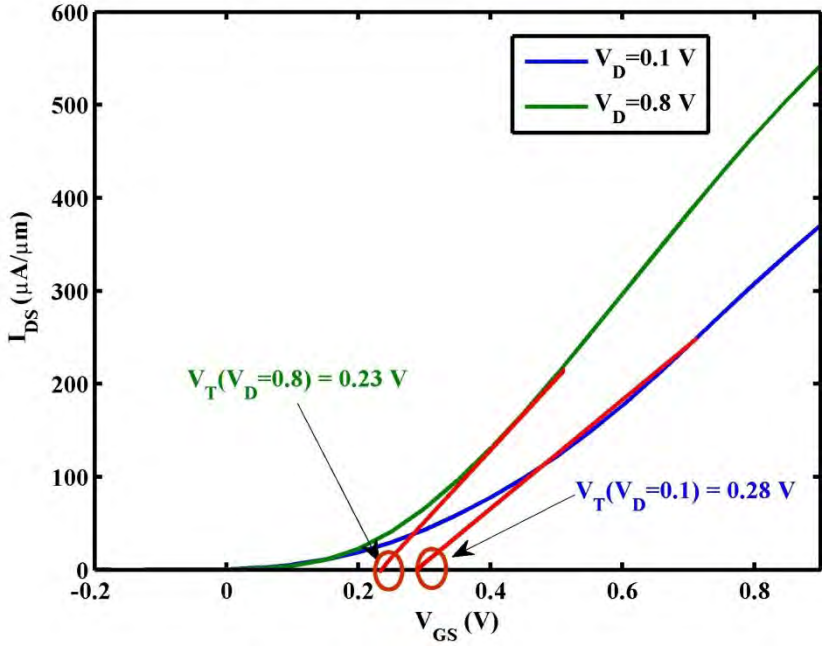


Figure 3.9: Threshold voltage extraction at different drain biases. For drain voltage of 0.8V threshold voltage is found to be 0.23V and for drain bias voltage of 0.1V it is 0.28V.

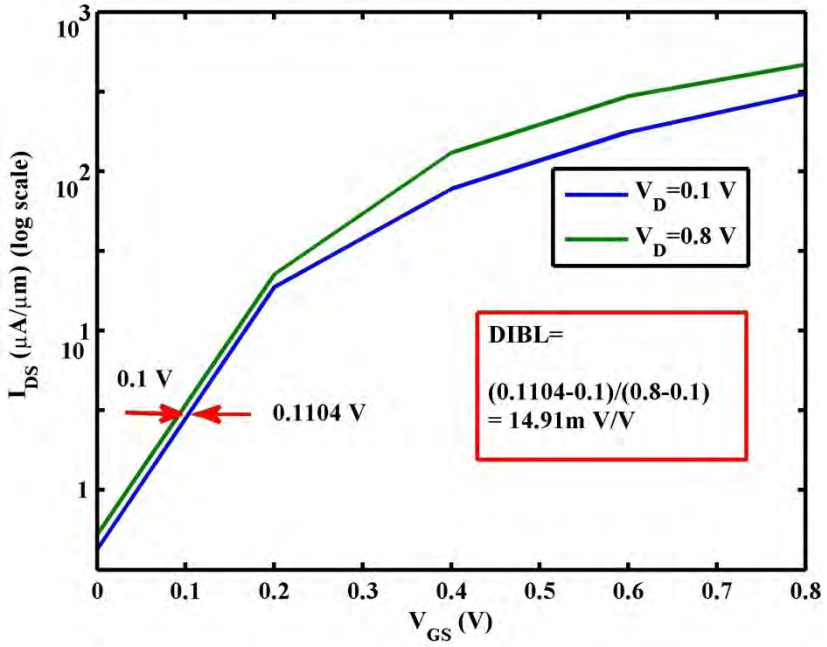


Figure 3.10: Drain Induced B arrier Lowering (DIBL) e xtraction f rom t he $\log_{10}(I_{ds}) - V_{gs}$ curve at drain voltages of 0.1V and 0.8V.

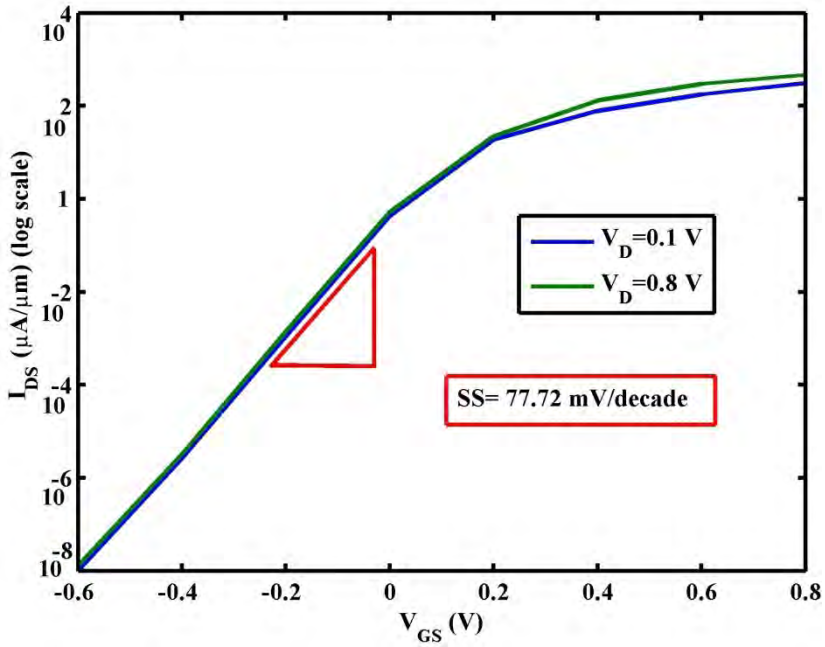


Figure 3.11: Subthreshold Swing (SS) extraction from the $\log_{10}(I_{ds}) - V_{gs}$ curve at drain voltages of 0.1V and 0.8V.

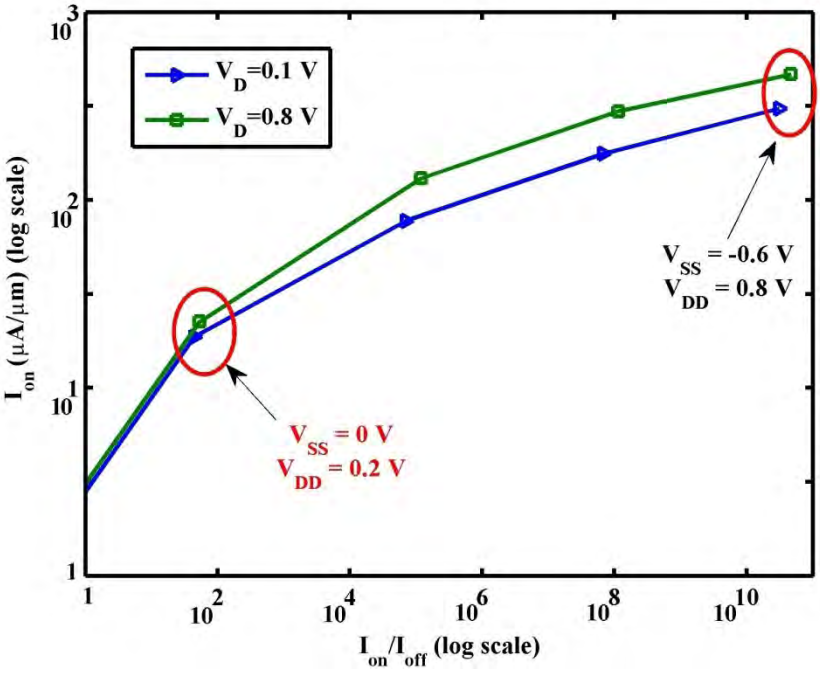


Figure 3.12: Extraction of on-off current ratio at drain voltages of 0.1V and 0.8V. The maximum on-off current ratio obtained is in the order of ~10^{10}.

3.3.4 Transport Properties below Threshold Voltage

Figure 3.13-3.16 displays transport properties at V_G= 0V , which is below the threshold voltage of the device. In Figure 3.13 the transmission co-efficient for first subband is shown. Figure 3.14(a) and 3.14(b) respectively shows Local Density of States (LDOS) at only source/drain terminal and throughout the channel. LODS peak at top of the barrier and source/drain energy levels, as expected.

Figure 3.15(a) shows the first subband energy profile and the energy resolved current density is shown in Figure 3.15(b). It is observed that below threshold voltage only energy levels at the top of the barrier contributes to the current. No tunneling current is present from source to drain. Figure 3.16(a) and 3.16(b) respectively shows 2D and 3D electron density in the device. For V_G= 0V 2D electron density at the middle of the channel is of order 10^{13} m^{-2}.

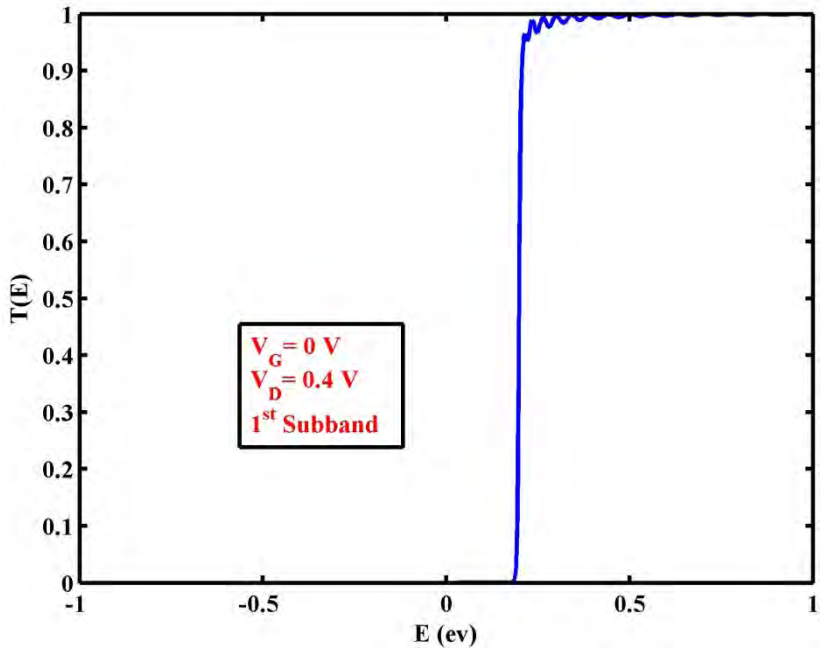
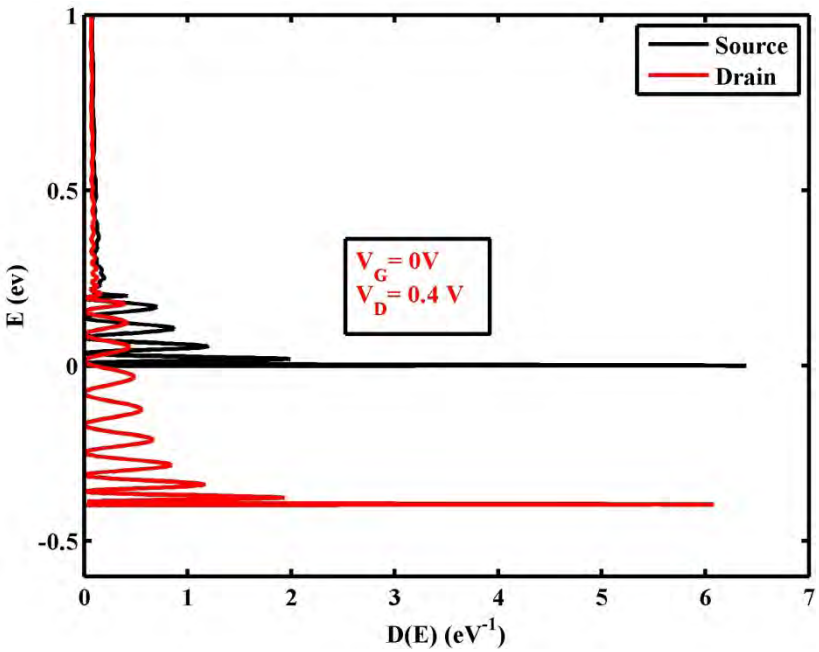
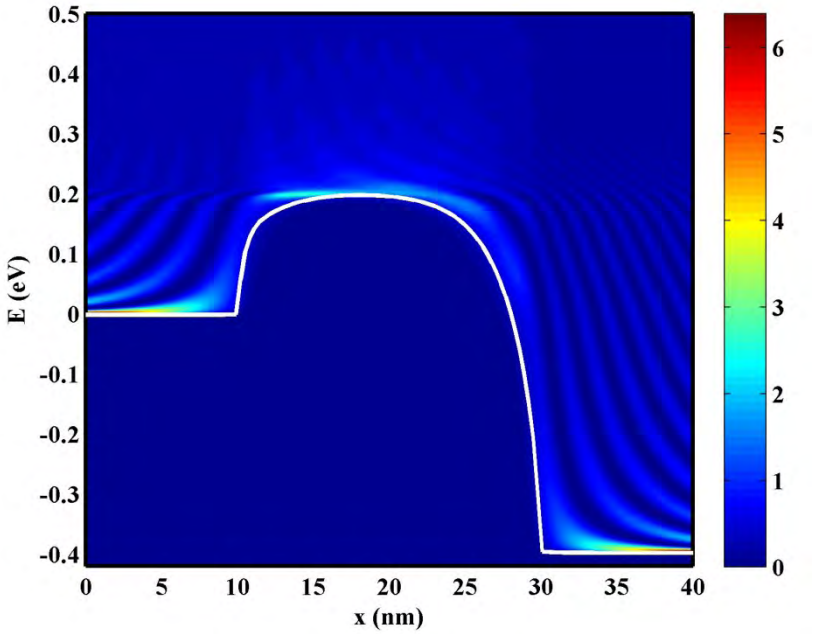


Figure 3.13: Transmission co-efficient for the device for gate and drain voltages of 0V and 0.4V respectively.

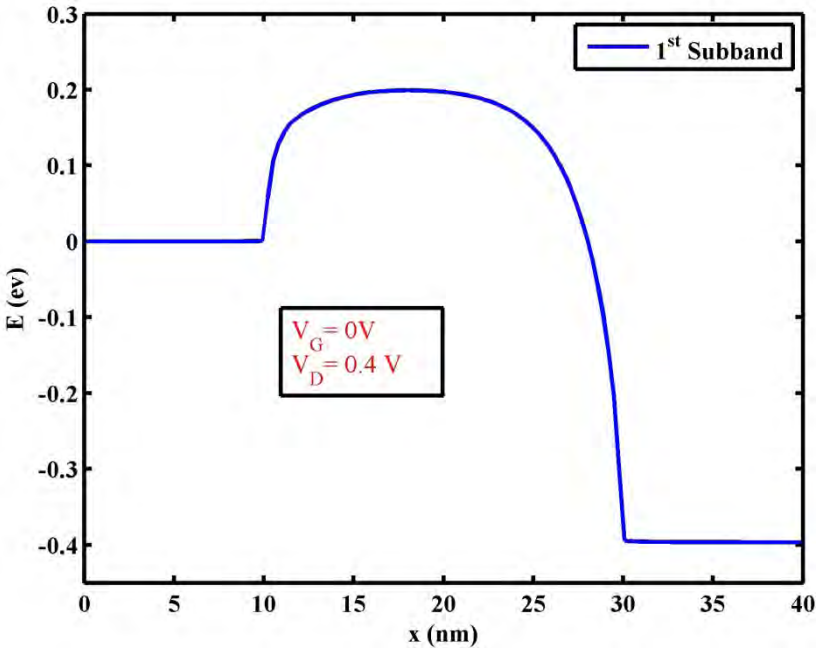


(a)

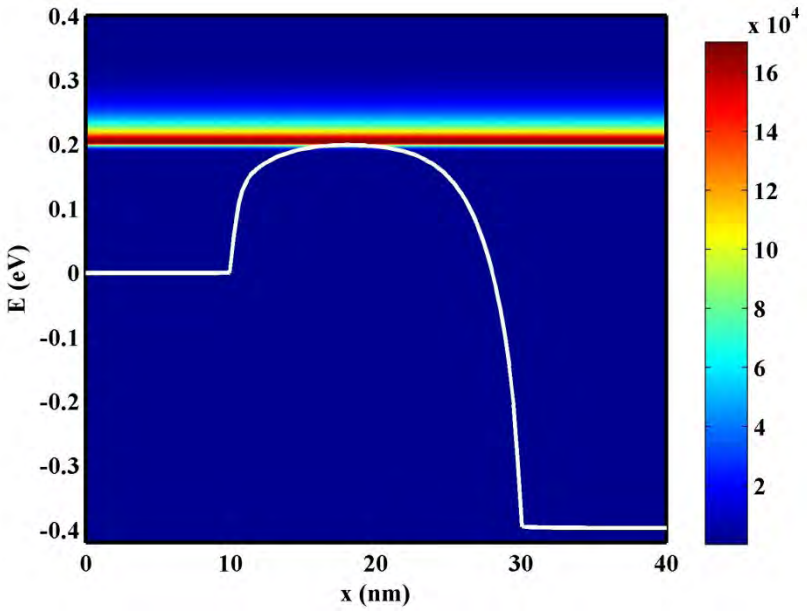


\ (b)

Figure 3.14: (a) LDOS at source and drain end **(b)** LDOS along the channel for gate and drain voltages of 0V and 0.4V respectively.

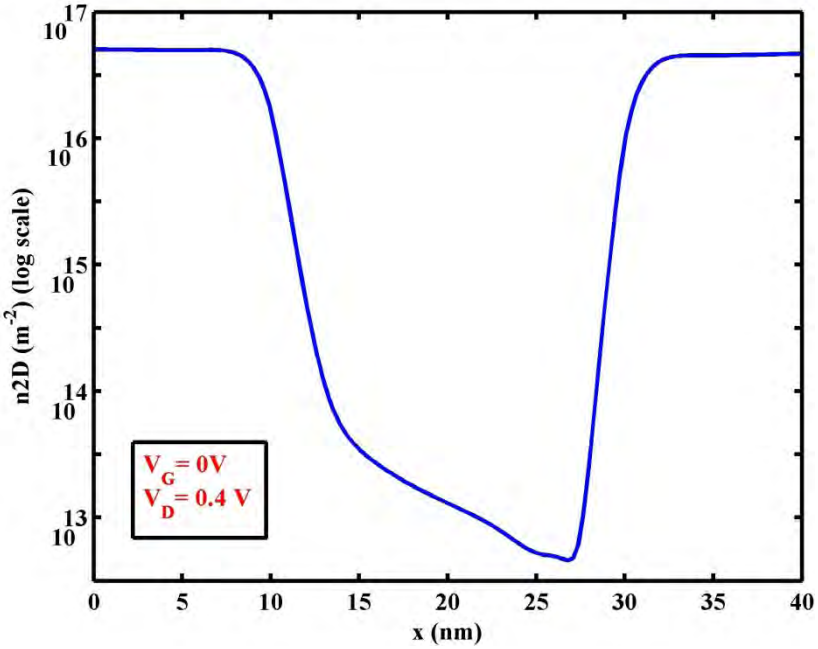


(a)

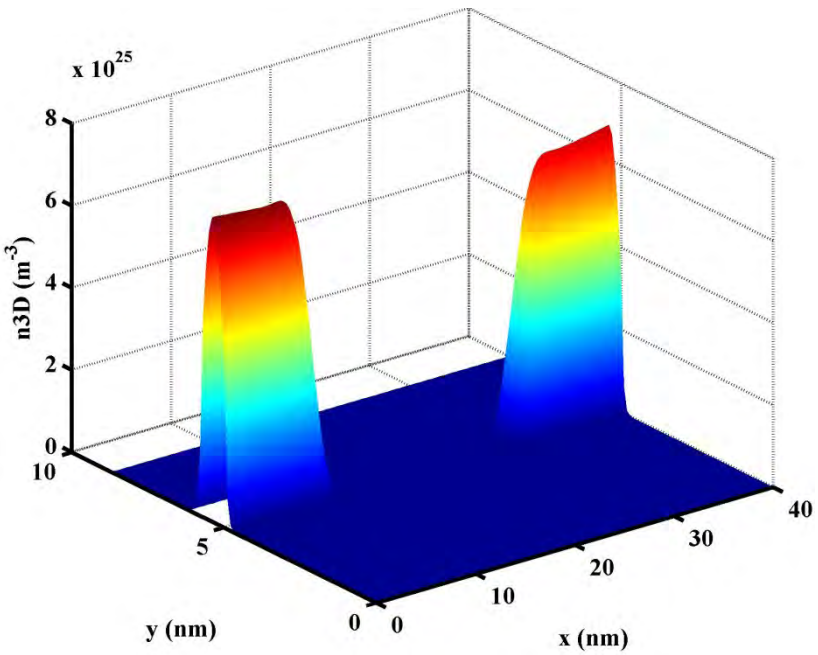


(b)

Figure 3.15: (a) First subband energy profile **(b)** Energy resolved current density of the device for gate and drain voltages of 0V and 0.4V respectively.



(a)



(b)

Figure 3.16: (a) 2-D electron density **(b)** 3-D electron density across the device for gate and drain voltages of 0V and 0.4V respectively.

3.3.5 Transport Properties above Threshold Voltage

Figure 3.17-3.20 displays transport properties at V_G= 0.5V , which is below the threshold voltage of the device. In Figure 3.17 the transmission co-efficient for first subband is shown. Figure 3.18(a) and 3.18(b) respectively shows Local Density of States (LDOS) at only source/drain terminal and throughout the channel. LODS peak at top of the barrier and source/drain energy levels, as expected.

Figure 3.19(a) shows the first subband energy profile and the energy resolved current density is shown in Figure 3.19(b). It is observed that below threshold voltage only energy levels at the top of the barrier contributes to the current. No tunneling current is present from source to drain. Figure 3.20(a) and 3.20(b) respectively shows 2D and 3D electron density in the device. For V_G= 0.5V 2D electron density at the middle of the channel is of order 10^{15} m^{-2}.

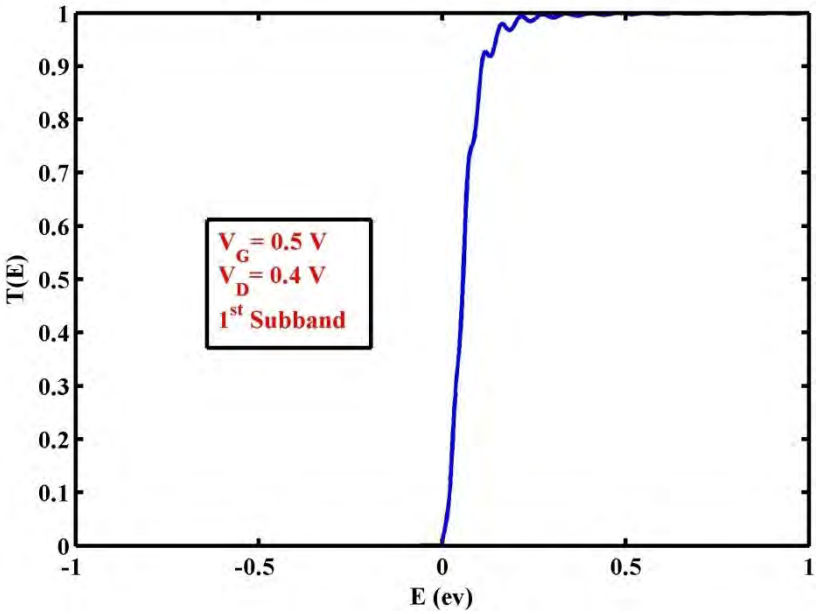
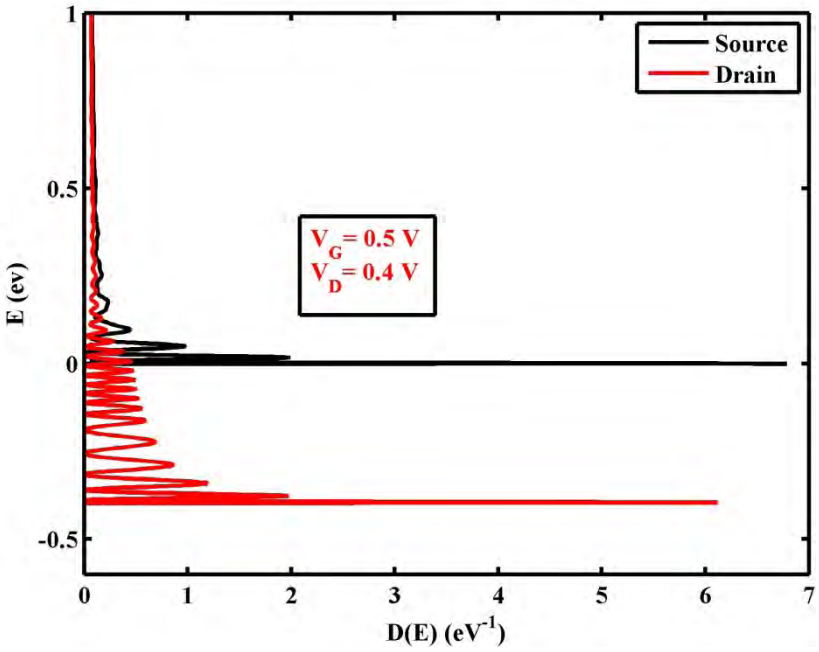
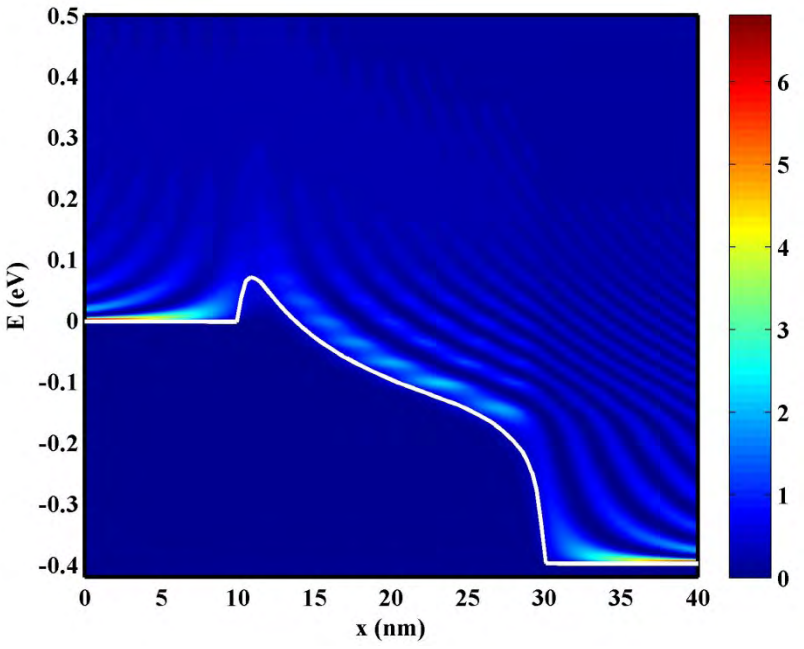


Figure 3.17. Transmission co-efficient for the device for gate and drain voltages of 0.5V and 0.4V respectively.

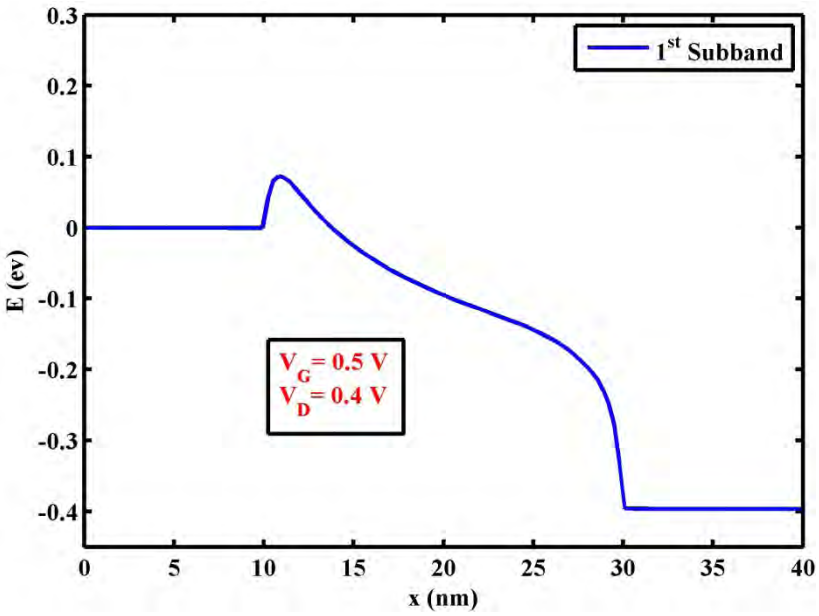


(a)

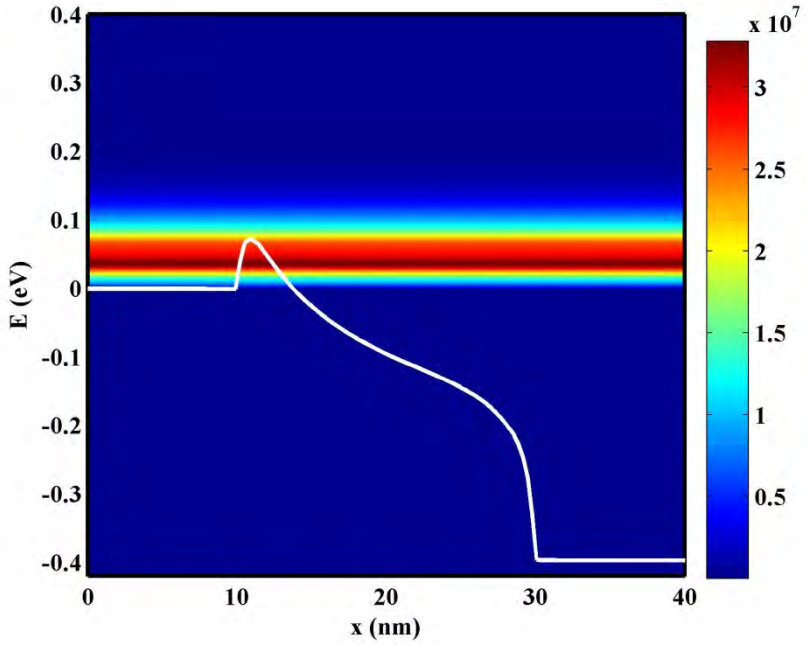


(b)

Figure 3.18: (a) LDOS at source and drain end **(b)** LDOS along the channel for gate and drain voltages of 0.5V and 0.4V respectively.

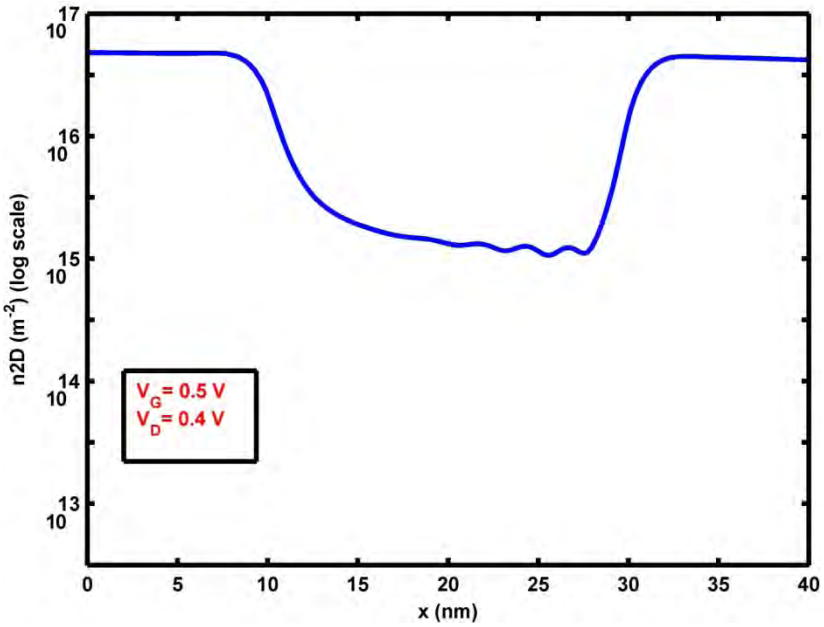


(a)

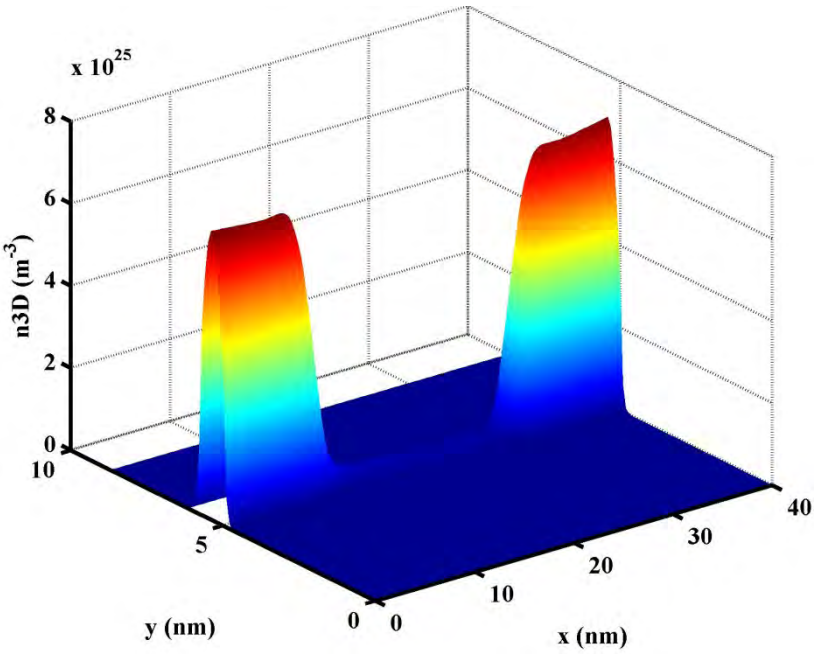


(b)

Figure 3.19: (a) First subband energy profile **(b)** Energy resolved current density of the device for gate and drain voltages of 0.5V and 0.4V respectively.



(a)



(b)

Figure 3.20: (a) 2-D electron density **(b)** 3-D electron density across the device for gate and drain voltages of 0.5V and 0.4V respectively.

3.3.6 Device Performance Parameters

Table 3.2 lists some of the performance parameters obtained from the transport simulation. The parameters indicate that monolayer WSe_2 FET has a very high on-off current ratio ($\sim 10^{10}$), which makes it suitable for low power applications. The extracted maximum effective mobility is also quite higher. The threshold voltage is found to be 0.23-0.28V for the proposed structure which can be tuned by changing doping profile and physical dimensions of the device. Also, using HfO_2 or other high-k material as top oxide, it is possible to get SS closer to theoretical lower limit of 60 mV/dec with this structure.

Table 3.2: Device Performance Parameters Obtained from Simulation

Property	Value
Threshold Voltage (V)	0.23 (@ V_D=0.8V)
SS (mV/dec)	77.72 (@ V_D=0.1V)
Maximum I_{on}/I_{off}	$\sim 10^{10}$
Peak Saturation Current (μA/μm)	467.2 (@ V_G=0.8V)
Maximum g_m (μS/μm)	887.7 (@ V_D=0.8V)
DIBL (mV/V)	14.91
Maximum Effective Mobility (cm^2/V.s)	300

Chapter 4

Analytical Modeling of Drain Current

In this section, a compact analytical drain current model will be developed. The main target is to formulate a single drain current Equation for all regions of operation i.e. depletion and inversion regions. In order to get consistent and accurate representation of terminal currents and charges in all regions of operations surface potential based MOSFET models shows better results than other alternatives like Threshold Voltage Based Models [108]. Surface potential based models are most suitable for simulating circuits with low power supply voltages and also allow physical modeling of the subthreshold region, which the threshold-voltage-based models can't model accurately. Hence, Surface potential based models are better alternative to the threshold voltage based models [109]. In addition to capturing currents in all regions of operation, the surface potential based model developed in this section will be able to capture short channel and non-ideal effects like drain induced barrier lowering, threshold voltage roll off, mobility degradation etc. For modeling terminal current of 2D material based MOSFET surface potential based approach has been used by Cao et al. [38], which provides consistent results with experimental I_d-V_{ds} characteristics. However Cao et al.'s work assumes the channel potential to be linear and as a result additional special formulation is needed to capture all the no ideal effects. In this model we intend capture all the non-ideal effect in a single current expression without taking any special formulation into account for every non ideal effects.

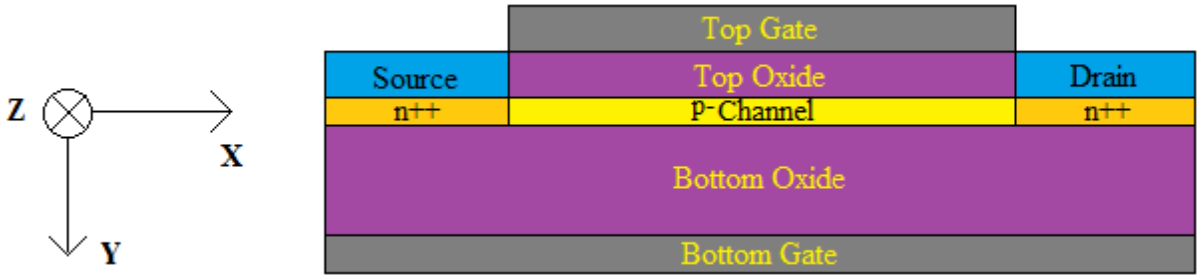


Figure 4.1: The MOSFET structure under consideration. It has a 2D material channel sandwiched between top and bottom oxides and corresponding top and bottom gates. The channel is p-doped. The source and drain are highly n-doped regions of the same 2D material.

4.1 Differential System Establishment

To represent the physics and operation of the device a differential system must be devised first. Figure 4.1 shows the n-type 2-D material MOSFET under consideration. Since the channel is very thin it is reasonable to assume that electrostatic potential $\varphi(x,y)$ in the channel does not change in the direction along the top and bottom gate [38]. That is it is safe to assume that in the channel potential $\varphi(x,y) \approx \varphi(x)$.

To get the differential system we need to apply the gauss's law in the infinitely small closed box shown in Figure 4.2. The box has height t_{ch} (depth of the 2D channel, ~ 0.65nm), width W and infinitely small length ∇x. From Gauss's Law the relationship between the charge density (Q) inside the enclosed box and the electric field outside the enclosed box ($\vec{E}$) can be founded as:

$$\oint_s \varepsilon \vec{E}.\overrightarrow{ds} = Q \tag{4.1}$$

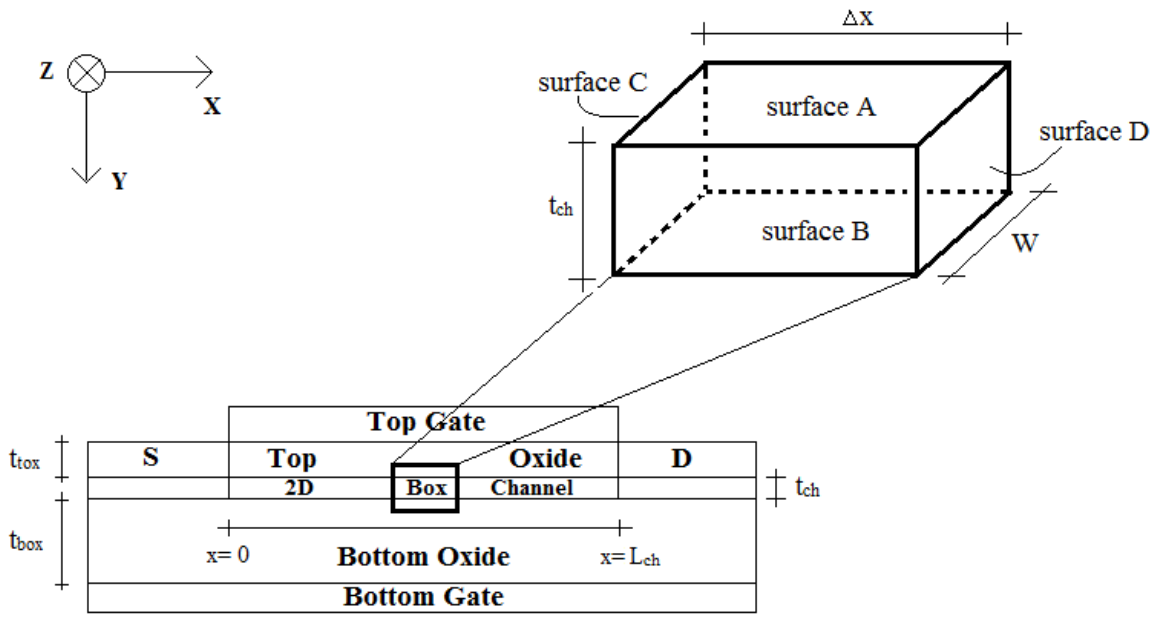


Figure 4.2: To establish the differential system for the 2D MOSFET an infinitesimal box is considered to which Gauss's Law ($\oint_s \varepsilon \vec{E}.\overrightarrow{ds} = Q$) is applied. The directions of the surface vectors are outward positive.

where, ε is the dielectric permittivity of the material at each surface of the encloser. Let us assume the infinity small box with width W, length Δx and depth of t_{ch} has a charge density of ΔQ. So, Equation 4.1 becomes,

$$\oint_s \varepsilon \vec{E}.\overrightarrow{ds} = \Delta Q \tag{4.2}$$

The left hand side of equation can be evaluated by considering each of the six sides of the box and the corresponding surface vectors. The positive directions of the surface vectors $\overrightarrow{ds}$ are outward from each surface.

The left hand side component of Equation 4.2 for surface A of Figure 4.2,

$$-\frac{V'_{Gt}-\varphi(x)}{t_{tox}}\varepsilon_{tox}\Delta xW \tag{4.3}$$

The left hand side component of Equation 4.2 for surface B of Figure 4.2,

$$\frac{\varphi(x)-V'_{Gb}}{t_{box}}\varepsilon_{box}\Delta xW \tag{4.4}$$

The left hand side component of Equation 4.2 for surface C of Figure 4.2,

$$\frac{d\varphi(x)}{dx}\varepsilon_{ch}t_{ch}W \tag{4.5}$$

The left hand side component of Equation 4.2 for surface D of Figure 4.2,

$$-\frac{d\varphi(x+\Delta x)}{dx}\varepsilon_{ch}t_{ch}W \tag{4.6}$$

Since there are no electric filed component along the z-axis of the box, contribution from surface E and F are zero. From Equation 4.3-4.6, ε_{tox} and ε_{box} are top and bottom oxide dielectric permittivities respectively. t_{tox} and t_{box} are top and bottom oxide thicknesses respectively. ε_{ch} is the dielectric permittivity of 2D material channel. V'_{Gt} and V'_{Gb} are respectively defined as,

$$V'_{Gt} = V_{Gt} - V_{FBt} \tag{4.7}$$

$$V'_{Gb} = V_{Gb} - V_{FBb} \tag{4.8}$$

Here, V_{Gt} and V_{Gb} are applied bias voltages at top and bottom gates respectively and $V_{FBt/b}$ are corresponding flat band voltages. $V_{FBt/b}$ are defined as,

$$V_{FBt} = \phi_{mt} - \phi_{ch} = \phi_{mt} - \left(\chi_{ch} + \frac{E_g}{2q} - \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)\right) \quad (4.9)$$

$$V_{FBb} = \phi_{mb} - \phi_{ch} = \phi_{mb} - \left(\chi_{ch} + \frac{E_g}{2q} - \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)\right) \quad (4.10)$$

Here, ϕ_{mt} and ϕ_{mb} are top and bottom metal gate work functions respectively and ϕ_{ch} is the 2D channel material work function. E_g, χ_{ch} and n_i are the bandgap, electron affinity and intrinsic carrier concentration of the channel material respectively. N_A, k, T and q are acceptor type dopant concentration per unit area, Boltzmann constant, Kelvin temperature and charge of electron respectively.

The right hand side of the Equation 4.2 can be defined as,

$$\Delta Q = q\Delta x W(-N_A - n_{2D}(x)) \quad (4.11)$$

Here, complete ionization of dopant atom is assumed under the desired range of temperature. Also, channel is assumed to be fully depleted. $n_{2D}(x)$ is the free inversion carrier (electron) concentration. Since the MOSFET under consideration is n-type, hole concentration is ignored. Putting values from Equation 4.3-4.6 and 4.11 into Equation 4.2 we get,

$$-\frac{V'_{Gt} - \varphi(x)}{t_{tox}}\varepsilon_{tox}\Delta x W + \frac{\varphi(x) - V'_{Gb}}{t_{tox}}\varepsilon_{box}\Delta x W + \frac{d\varphi(x)}{dx}\varepsilon_{ch}t_{ch}W - \frac{d\varphi(x+\Delta x)}{dx}\varepsilon_{ch}t_{ch}W = q\Delta x W(-N_A - n_{2D}(x)) \quad (4.12)$$

$$-\frac{V'_{Gt} - \varphi(x)}{t_{tox}}\varepsilon_{tox}\Delta x + \frac{\varphi(x) - V'_{Gb}}{t_{tox}}\varepsilon_{box}\Delta x + \frac{d\varphi(x)}{dx}\varepsilon_{ch}t_{ch} - \frac{d\varphi(x+\Delta x)}{dx}\varepsilon_{ch}t_{ch} = q\Delta x(-N_A - n_{2D}(x)) \quad (4.13)$$

$$-\frac{V'_{Gt}}{t_{tox}}\varepsilon_{tox}\Delta x + \frac{\varphi(x)}{t_{tox}}\varepsilon_{tox}\Delta x + \frac{\varphi(x)}{t_{tox}}\varepsilon_{box}\Delta x - \frac{V'_{Gb}}{t_{tox}}\varepsilon_{box}\Delta x - \varepsilon_{ch}t_{ch}\left(\frac{d\varphi(x+\Delta x)}{dx} - \frac{d\varphi(x)}{dx}\right) = -q\Delta x(N_A + n_{2D}(x)) \quad (4.14)$$

Since the box is infinitely small we can consider $\Delta x \to 0$. So, Equation 4.14 becomes,

$$-\left(\frac{V'_{Gt}}{t_{tox}}\varepsilon_{tox} + \frac{V'_{Gb}}{t_{tox}}\varepsilon_{box}\right) + \varphi(x)\left(\frac{\varepsilon_{tox}}{t_{tox}} + \frac{\varepsilon_{box}}{t_{tox}}\right) - \varepsilon_{ch}t_{ch}\frac{d^2\varphi(x)}{d^2x} = -q(N_A + n_{2D}(x)) \quad (4.15)$$

$$-\left(\frac{\varepsilon_{tox}}{t_{tox}\varepsilon_{ch}t_{ch}}V'_{Gt}+\frac{\varepsilon_{box}}{t_{tox}\varepsilon_{ch}t_{ch}}V'_{Gb}\right)+\varphi(x)\left(\frac{\varepsilon_{tox}}{t_{tox}\varepsilon_{ch}t_{ch}}+\frac{\varepsilon_{box}}{t_{tox}\varepsilon_{ch}t_{ch}}\right)-\frac{d^2\varphi(x)}{d^2x}$$
$$=-\frac{q}{\varepsilon_{ch}t_{ch}}(N_A+n_{2D}(x)) \quad (4.16)$$

$$\frac{d^2\varphi(x)}{d^2x}-\varphi(x)\left(\frac{\varepsilon_{tox}}{t_{tox}\varepsilon_{ch}t_{ch}}+\frac{\varepsilon_{box}}{t_{tox}\varepsilon_{ch}t_{ch}}\right)+\left(\frac{\varepsilon_{tox}}{t_{tox}\varepsilon_{ch}t_{ch}}V'_{Gt}+\frac{\varepsilon_{box}}{t_{tox}\varepsilon_{ch}t_{ch}}V'_{Gb}\right)=\frac{q}{\varepsilon_{ch}t_{ch}}(N_A+$$
$$n2D(x) \quad (4.17)$$

$$\frac{d^2\varphi(x)}{d^2x}-K\varphi(x)+G=\frac{q}{\varepsilon_{ch}t_{ch}}(N_A+n_{2D}(x)) \quad (4.18)$$

Where,

$$G=\frac{\varepsilon_{tox}}{t_{tox}\varepsilon_{ch}t_{ch}}V'_{Gt}+\frac{\varepsilon_{box}}{t_{tox}\varepsilon_{ch}t_{ch}}V'_{Gb} \quad (4.19)$$

$$K=\frac{\varepsilon_{tox}}{t_{tox}\varepsilon_{ch}t_{ch}}+\frac{\varepsilon_{box}}{t_{box}\varepsilon_{ch}t_{ch}} \quad (4.20)$$

$$\frac{d^2\varphi(x)}{d^2x}-K\varphi(x)+G=\frac{q}{\varepsilon_{ch}t_{ch}}N_A+\frac{q}{\varepsilon_{ch}t_{ch}}n_{2D}(x) \quad (4.21)$$

Where,

$$n_{2D}(x)=N_{dos}e^{-\frac{E_C(x)-E_F(x)}{kT}}=N_{dos}e^{\frac{q}{kT}(\varphi(x)-V(x))} \quad (4.22)$$

$E_c(x)=-q\varphi(x)$ is t he c onduction ba nd pr ofile a nd $E_F(x)=-qV(x)$ is th e q uasi F ermi level of the channel. N_{dos} is the effective density state of the channel material. Differentiating Equation 4.21 with respect to x,

$$\frac{d^3\varphi(x)}{d^3x}-K\frac{d\varphi(x)}{dx}=\frac{q}{\varepsilon_{ch}t_{ch}}\frac{dn_{2D}(x)}{dx} \quad (4.23)$$

$$\frac{d^3\varphi(x)}{d^3x}-K\frac{d\varphi(x)}{dx}=\frac{q}{\varepsilon_{ch}t_{ch}}\frac{d(N_{dos}e^{\frac{q}{kT}(\varphi(x)-V(x))})}{dx} \quad (4.24)$$

$$\frac{d^3\varphi(x)}{d^3x}-K\frac{d\varphi(x)}{dx}=\frac{q}{\varepsilon_{ch}t_{ch}}N_{dos}e^{\frac{q}{kT}(\varphi(x)-V(x))}\left[\frac{q}{kT}\frac{d\varphi(x)}{dx}-\frac{q}{kT}\frac{dV(x)}{dx}\right] \quad (4.25)$$

Substituting value of $\frac{q}{\varepsilon_{ch}t_{ch}}n_{2D}(x)$ from Equation 4.21 into Equation 4.25,

$$\frac{d^3\varphi(x)}{d^3x}-K\frac{d\varphi(x)}{dx}=\left[\frac{d^2\varphi(x)}{d^2x}-K\varphi(x)+G-\frac{q}{\varepsilon_{ch}t_{ch}}N_A\right]\left[\frac{q}{kT}\frac{d\varphi(x)}{dx}-\frac{q}{kT}\frac{dV(x)}{dx}\right] \quad (4.26)$$

The differential Equation 4.26 cannot be solved for a closed form analytical solution. To simplify the Equation, invoking gradual channel approximation we get $\frac{dV(x)}{dx} \approx 0$ [110]. This assumption is particularly valid for long channel 2D MOSFETs where lateral electric field (from drain to source) is weaker compared to the vertical electric filed from top to bottom gate. Equation 4.26 simplifies as,

$$\frac{d^3\varphi(x)}{d^3x} - K\frac{d\varphi(x)}{dx} = \left[\frac{d^2\varphi(x)}{d^2x} - K\varphi(x) + G - \frac{q}{\varepsilon_{ch}t_{ch}}N_A\right]\left[\frac{q}{kT}\frac{d\varphi(x)}{dx}\right] \tag{4.27}$$

Let us further simplify the Equation 4.27 by ignoring higher order variations of $\varphi(x)$ with x. As long as the channel is long and drain voltage is low, this assumption is also valid.

$$-K\frac{d\varphi(x)}{dx} = \left[\frac{d^2\varphi(x)}{d^2x} - K\varphi(x) + G - \frac{q}{\varepsilon_{ch}t_{ch}}N_A\right]\left[\frac{q}{kT}\frac{d\varphi(x)}{dx}\right] \tag{4.28}$$

$$\frac{q}{kT}\frac{d\varphi(x)}{dx}\left[\frac{d^2\varphi(x)}{d^2x} - K\varphi(x) + G - \frac{q}{\varepsilon_{ch}t_{ch}}N_A + K\frac{kT}{q}\right] = 0 \tag{4.29}$$

$$\frac{d\varphi(x)}{dx}\left[\frac{d^2\varphi(x)}{d^2x} - K\varphi(x) + G - \frac{q}{\varepsilon_{ch}t_{ch}}N_A + K\frac{kT}{q}\right] = 0 \tag{4.30}$$

We get two solutions from Equation 4.30. First one,

$$\frac{d\varphi(x)}{dx} = 0 \tag{4.31}$$

$$\varphi(x) = constant \tag{4.32}$$

which is a solution for the special case when drain voltage (V_D) and source voltage (V_S) are both zero. A more general solution of Equation 4.30 can be found from the second part-

$$\frac{d^2\varphi(x)}{d^2x} - K\varphi(x) + G - \frac{q}{\varepsilon_{ch}t_{ch}}N_A + K\frac{kT}{q} = 0 \tag{4.33}$$

Let us take,

$$A = \frac{kT}{q}K + G - \frac{q}{\varepsilon_{ch}t_{ch}}N_A \tag{4.34}$$

$$\frac{d^2\varphi(x)}{d^2x} - K\varphi(x) + A = 0 \tag{4.35}$$

$$\frac{d^2\varphi(x)}{d^2x} - K\varphi(x) = -A \tag{4.36}$$

Equation 4.36 is a linear differential Equation with constant co-efficient. A closed form solution of this differential Equation is possible. Let's assume the differential operators,

$$\frac{d}{dx} \equiv D \; and \; \frac{d^2}{d^2x} \equiv D^2 \tag{4.36}$$

Equation 4.36 becomes,

$$(D^2 - K)\varphi(x) = -A \tag{4.37}$$

Now writing the auxiliary Equation of Equation 4.37 we get,

$$D^2 - K = 0 \tag{4.38}$$

$$\therefore D = \pm\sqrt{K} \tag{4.39}$$

So, the complementary function of Equation 4.37,

$$CF = C_1 e^{\sqrt{K}x} + C_2 e^{-\sqrt{K}x} \tag{4.40}$$

Here, $C_1$and C_2 are constants which can be determined by using the boundary conditions of the MOSFET. We can get the particular integral of Equation 4.37 as,

$$PI = \frac{-A}{D^2 - K} \tag{4.41}$$

$$= \frac{-A.e^{0.x}}{D^2 - K} \tag{4.42}$$

$$= \frac{-A.e^{0.x}}{(0)^2 - K} \tag{4.43}$$

$$\therefore PI = \frac{A}{K} \tag{4.44}$$

The complete solution of the Equation 4.37 is,

$$\varphi(x) = CF + PI \tag{4.45}$$

$$\varphi(x) = C_1 e^{\sqrt{K}x} + C_2 e^{-\sqrt{K}x} + \frac{A}{K} \tag{4.46}$$

4.2 Evaluating the Constants C_1 and C_2

For source and drain region, $n_{2d} = N_{D(source)} = N_{D(drain)} = N_{sd}$, where N_{sd} is the n-type source and drain doping concentration per unit area. For source at $x = 0$,

$$n_{2D}(0) = N_{sd} = N_{dos} e^{\frac{q}{kT}(\varphi(0) - V(0))} \tag{4.47}$$

Where,

$$\varphi(0) = V(0) + \frac{kT}{q} \ln\left(\frac{N_{sd}}{N_{dos}}\right) \tag{4.48}$$

$$V(0) = V_S + V_{bi} \tag{4.49}$$

Here, V_{bi} is the built in potential at the source(or drain)-channel interface given by,

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_{sd} N_A}{n_i^2}\right) \tag{4.50}$$

$$\therefore \varphi(0) = V_S + V_{bi} + \frac{kT}{q} \ln\left(\frac{N_{sd}}{N_{dos}}\right) \tag{4.51}$$

For drain at $x = L_{ch}$ similar to source we get,

$$n_{2D}(L_{ch}) = N_{sd} = N_{dos} e^{\frac{q}{kT}(\varphi(0L_{ch}) - V(L_{ch}))} \tag{4.52}$$

$$\varphi(L_{ch}) = V(L_{ch}) + \frac{kT}{q} \ln\left(\frac{N_{sd}}{N_{dos}}\right) \tag{4.53}$$

$$V(L_{ch}) = V_D + V_{bi} \tag{4.54}$$

$$\therefore \varphi(L_{ch}) = V_D + V_{bi} + \frac{kT}{q} \ln\left(\frac{N_{sd}}{N_{dos}}\right) \tag{4.55}$$

At $x = 0$ Equation 4.46 becomes,

$$\varphi(0) = C_1 + C_2 + \frac{A}{K} \tag{4.56}$$

At $x = L_{ch}$ Equation 4.46 becomes,

$$\varphi(L_{ch}) = C_1 e^{\sqrt{K} L_{ch}} + C_2 e^{-\sqrt{K} L_{ch}} + \frac{A}{K} \tag{4.57}$$

Rearranging Equation 4.56 and 4.57 we get,

$$C_1 + C_2 = \varphi(0) - \frac{A}{K} \tag{4.58}$$

$$C_1 e^{\sqrt{K}L_{ch}} + C_2 e^{-\sqrt{K}L_{ch}} = \varphi(L_{ch}) - \frac{A}{K} \tag{4.59}$$

Multiplying Equation 4.58 by $e^{-\sqrt{K}L_{ch}}$ and subtracting Equation 4.59 we get,

$$C_1 = \frac{\left(\varphi(0)-\frac{A}{K}\right)e^{-\sqrt{K}L_{ch}} - \left(\varphi(L_{ch})-\frac{A}{K}\right)}{e^{-\sqrt{K}L_{ch}} - e^{\sqrt{K}L_{ch}}} \tag{4.60}$$

Multiplying Equation 4.58 by $e^{\sqrt{K}L_{ch}}$ subtracting Equation 4.59 we get,

$$C_2 = \frac{\left(\varphi(0)-\frac{A}{K}\right)e^{\sqrt{K}L_{ch}} - \left(\varphi(L_{ch})-\frac{A}{K}\right)}{e^{\sqrt{K}L_{ch}} - e^{-\sqrt{K}L_{ch}}} \tag{4.61}$$

Substituting the values of $C_1$and C_2 into Equation 4.46 we get the complete solution of $\varphi(x)$,

$$\varphi(x) = \left[\frac{\left(\varphi(0) - \frac{A}{K}\right)e^{-\sqrt{K}L_{ch}} - \left(\varphi(L_{ch}) - \frac{A}{K}\right)}{e^{-\sqrt{K}L_{ch}} - e^{\sqrt{K}L_{ch}}}\right] e^{\sqrt{K}x} + \left[\frac{\left(\varphi(0) - \frac{A}{K}\right)e^{\sqrt{K}L_{ch}} - \left(\varphi(L_{ch}) - \frac{A}{K}\right)}{e^{\sqrt{K}L_{ch}} - e^{-\sqrt{K}L_{ch}}}\right] e^{-\sqrt{K}x} + \frac{A}{K} \tag{4.62}$$

Here, $\frac{A}{K}$ can be evaluated from Equations 4.20 and 4.34 as,

$$\frac{A}{K} = \frac{\frac{kT}{q}\left(\frac{\varepsilon_{tox}}{t_{tox}\varepsilon_{ch}t_{ch}} + \frac{\varepsilon_{box}}{t_{box}\varepsilon_{ch}t_{ch}}\right) + \left(G\frac{\varepsilon_{tox}}{t_{tox}\varepsilon_{ch}t_{ch}}V'_{Gt} + \frac{\varepsilon_{box}}{t_{tox}\varepsilon_{ch}t_{ch}}V'_{Gb}\right) - \frac{q}{\varepsilon_{ch}t_{ch}}N_A}{\frac{\varepsilon_{tox}}{t_{tox}\varepsilon_{ch}t_{ch}} + \frac{\varepsilon_{box}}{t_{box}\varepsilon_{ch}t_{ch}}} \tag{4.63}$$

4.3 Drain Current Modeling

Carrier transport is governed by the drift-diffusion Equation [38, 111] as described by,

$$I_x(x) = qWn_{2D}(x)\mu_n(x)\frac{dV(x)}{dx} \tag{4.64}$$

Here, $\mu_n(x)$ is the channel electron mobility. For the 2D material MOSFET considered here, current is uniform through drain to source and gate leakage current is ignored. Let's assume uniform drain current as I_{DS}. So we can write, $I_x(x) = I_{DS}$ and Equation 3.64 becomes,

$$I_{DS} = qWn_{2D}(x)\mu_n(x)\frac{dV(x)}{dx} \tag{4.65}$$

In this stage we need an estimation of $V(x)$ in terms of x to calculate the current. The most simplified approximation can be a liner profile of $V(x)$ as described by the Equation,

$$V(x) = Mx + C \tag{4.66}$$

From Figure 4.3 the constants M and C can be evaluated as,

$$M = \frac{(V_D - V_S)}{L_{ch}} \tag{4.67}$$

$$C = V_S + V_{bi} \tag{4.68}$$

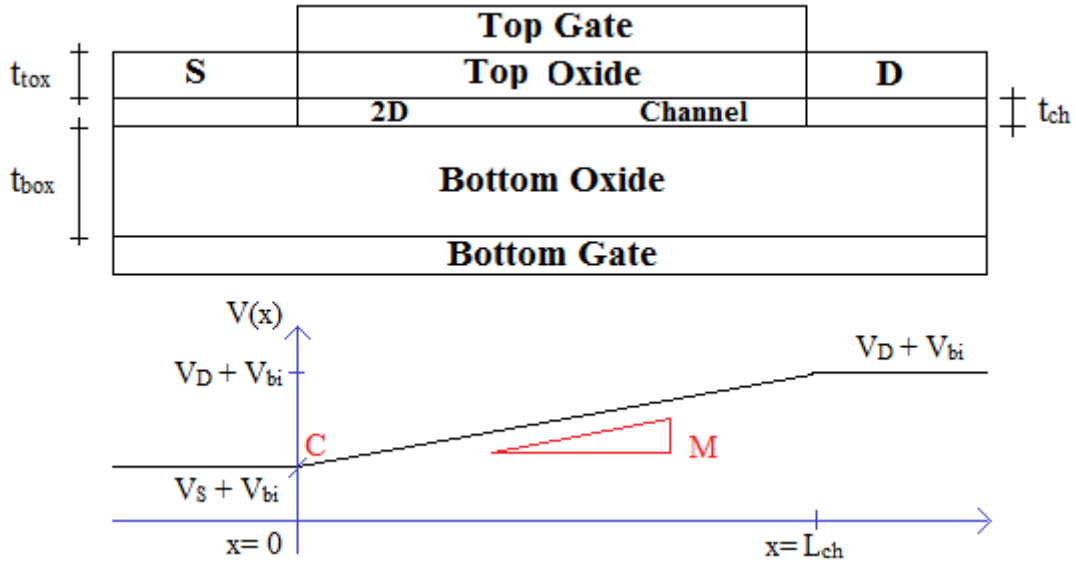


Figure 4.3: Approximation of potential $V(x)$ inside the 2D channel.

The value of M is consistent with our previous gradual channel approximation. With longer L_{ch} and lower V_D, M gets smaller and dependence of $V(x)$ on x diminishes to give $\frac{dV(x)}{dx} \approx 0$. However, in the value of M and C from Equations 4.67 and 4.68, gate voltage dependence of quasi Fermi level is missing. To incorporate the effect of gate voltage an empirical fitting function $F(V_G)$ can be considered with C. So, the final form of C becomes,

$$C = V_S + V_{bi} + F(V_G) \tag{4.69}$$

Now,

$$\frac{dV(x)}{dx} = M \tag{4.70}$$

So, Equation 4.65 becomes,

$$I_{DS} = qWn_{2D}(x)\mu_n(x)M \tag{4.71}$$

Integrating Equation 3.71 with respect to x from $x = 0$ to $x = L_{ch}$ we get,

$$\int_{x=0}^{x=L_{ch}} I_{DS}\, dx = qWM \int_{x=0}^{x=L_{ch}} n_{2D}(x)\, \mu_n(x) dx \tag{4.72}$$

Assuming a filed dependent mobility μ_n which does not depend on x we get,

$$\int_{x=0}^{x=L_{ch}} I_{DS}\, dx = qWM\mu_n \int_{x=0}^{x=L_{ch}} n_{2D}(x)\, dx \tag{4.73}$$

The lateral electric field ($E_{||}$) dependence of the mobility (μ_n) will come from a standard mobility model as used in ATLAS [112]:

$$\mu_n = \frac{\mu_{n0}}{\left[1+\left[\frac{\mu_{n0}E_{||}}{VSATN}\right]^{BETAN}\right]^{\frac{1}{BETAN}}} \tag{4.74}$$

Here,

μ_{n0} = Low field mobility

$VSATN$ = Electron saturation velocity in the electric field

$BETAN$ = Fitting Parameter

$E_{||}$ = Lateral electric field from drain to source = $\frac{V_D - V_S}{L_{ch}}$

Now, substituting $n_{2D}(x)$ from Equation 4.22 into Equation 4.73 we get,

$$I_{DS}\int_{x=0}^{x=L_{ch}} dx = qWM\mu_n \int_{x=0}^{x=L_{ch}} N_{dos} e^{\frac{q}{kT}(\varphi(x)-V(x))}\, dx \tag{4.75}$$

$$I_{DS}[x]_{x=0}^{x=L_{ch}} = qWM\mu_n N_{dos} \int_{x=0}^{x=L_{ch}} e^{\frac{q}{kT}(\varphi(x)-V(x))}\, dx \tag{4.76}$$

$$I_{DS} = \frac{qWMN_{dos}}{L_{ch}}\mu_n \int_{x=0}^{x=L_{ch}} e^{\frac{q}{kT}(\varphi(x)-V(x))}\, dx \tag{4.77}$$

Substituting values of $\varphi(x)$, $V(x)$ and μ_n into Equation 4.77 we get the final expression of the drain current in integral from as,

$$I_{DS} = \frac{qWMN_{dos}}{L_{ch}} \frac{\mu_{n0}}{\left[1+\left[\frac{\mu_{n0}E_{||}}{VSATN}\right]^{BETAN}\right]^{\frac{1}{BETAN}}} \int_{x=0}^{x=L_{ch}} e^{\frac{q}{kT}\left(C_1 e^{\sqrt{K}x}+C_2 e^{-\sqrt{K}x}+\frac{A}{K}-Mx-V_S-V_{bi}-F(V_G)\right)}\, dx \tag{4.78}$$

Drain current per unit channel width,

$$I_{DS} = \frac{qMN_{dos}}{L_{ch}} \frac{\mu_{n0}}{\left[1+\left[\frac{\mu_{n0}E_{||}}{VSATN}\right]^{BETAN}\right]^{\frac{1}{BETAN}}} \int_{x=0}^{x=L_{ch}} e^{\frac{q}{kT}\left(C_1 e^{\sqrt{K}x}+C_2 e^{-\sqrt{K}x}+\frac{A}{K}-Mx-V_S-V_{bi}-F(V_G)\right)}\, dx \tag{4.79}$$

The integral in Equation 4.79 do not have a closed form solution and must be evaluated numerically to get the final current. The fitting function $F(V_G)$, low field mobility (μ_{n0}) and $BETAN$ can be used as fitting parameters to match the analytical current with experimental or simulated current.

4.4 Calculation of Effective Density of States N_{dos}

Effective density of states of 2D semiconductors can be represented as [38],

$$N_{dos} = \sum_i \frac{g_s g_i m_i^*}{2\pi\hbar^2} \tag{4.80}$$

Here,

g_s= Spin degeneracy
g_i = Valley degeneracy
m_i^* = Effective mass
$\hbar$ = Reduced Plank's constant
i = Valley index

From the E-K diagram of WSe_2 shown in Figure 4.4, it is apparent that the energy difference between the lowest valley and the second lowest valley is very small (~8 meV). So, in calculating N_{dos} we need to consider two lowest conduction band valleys. If the energy difference between two lowest valleys is taken as ∇E_C, then Equation 4.80 becomes,

$$N_{dos} = \frac{g_s g_1 m_1^*}{2\pi\hbar^2} + \frac{g_s g_2 m_2^*}{2\pi\hbar^2} e^{-\frac{\nabla E_C}{kT}} \tag{4.81}$$

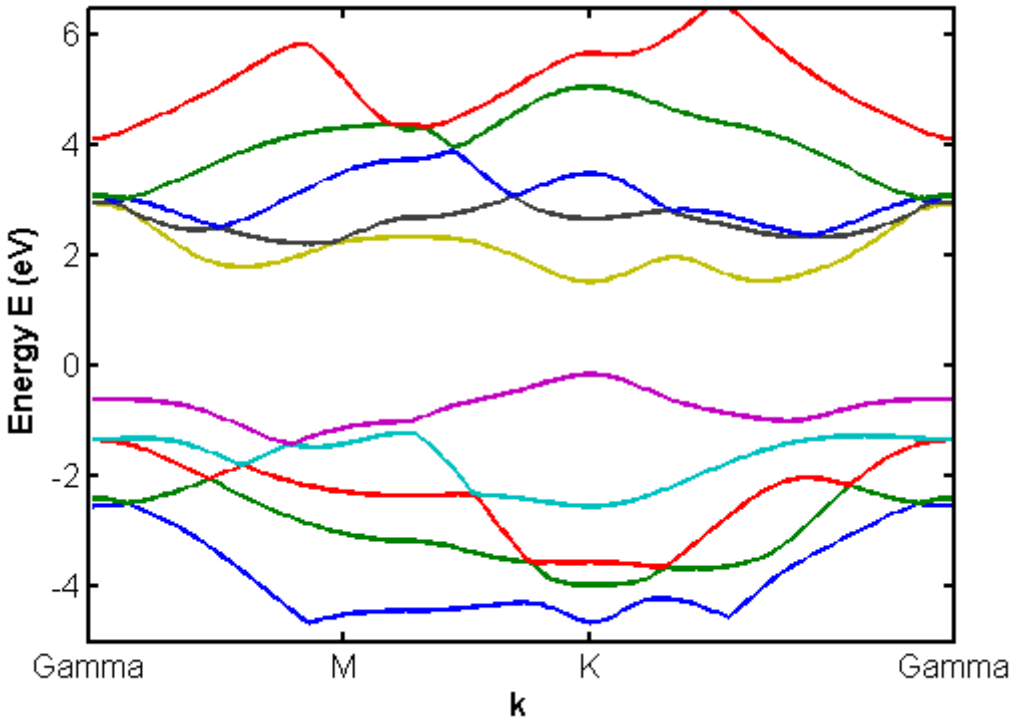


Figure 4.4: E-k diagram of WSe_2 obtained from first-principle DFT simulations in Quantum Espresso software [51]. The diagram shows lowest conduction valley at K-point. The nearest low point is somewhere between K and Γ point. The energy difference between those two lowest valleys is approximately 8 meV.

4.5 Model Verification

The compact analytical model proposed in this chapter is verified against the self-consistent simulated current from the Chapter 3. To make a valid comparison exactly same sets of device and material parameters are used. Drain current, inversion charge density, channel potential are evaluated in MATLAB using Equation 4.79, 4.22 and 4.62 respectively.

3.5.1 Device Dimension Used

Table 4.1: Physical Dimension of the Analytical Device

Parameter	Symbol	Value
Channel Thickness	t_{ch}	0.65 nm
Channel Length	L_{ch}	20 nm
Channel Width	W	10 nm
Channel Doping	N_A	2.2 x 10^{16} m^{-2}
Source/Drain Doping	N_{sd}	3.25 x 10^{17} m^{-2}
Top Oxide Thickness	t_{tox}	3 nm
Bottom Oxide Thickness	t_{box}	5 nm

4.5.2 Device Materials Used

Table 4.2: Material Used in the Analytical Device

Device Segment	Material
Channel	Monolayer p-WSe_2
Top and Bottom Gate	Palladium (Pd)
Top Oxide	ZrO_2
Bottom Oxide	SiO_2
Source/Drain	Monolayer n++ WSe_2

4.5.3 Material Parameters Used

Table 4.3: Material Parameters for the Analytical Device

Parameter	Symbol	Value
Monolayer WSe_2 Electron Effective Mass	m^*	0.33 x 9.1 x 10^{-31} kg
Monolayer WSe_2 Dielectric Permittivity	ε_{ch}	5.2 x 8.854 x 10^{-12} Fm^{-1}
Monolayer WSe_2 Bandgap	E_g	1.6 eV
Monolayer WSe_2 Electron Affinity	χ_{ch}	3.9 eV
Pd Work Function	Φ_m	5.1 eV
ZrO_2 Dielectric Permittivity	ε_{tox}	12.5 x 8.854 x 10^{-12} Fm^{-1}
SiO_2 Dielectric Permittivity	ε_{box}	3.9 x 8.854 x 10^{-12} Fm^{-1}

4.5.4 Benchmarking and Fitting Parameters Selection

Figure 4.5 shows the transfer characteristics of the analytical device obtained from Equation 4.79 along with the transfer characteristics from the self-consistent simulation in Chapter 3. To match both characteristics fitting function $F(V_G)$, low field mobility (μ_{n0}) and $BETAN$ have been configured as:

Table 4.4: Fitting Parameters for the Compact Analytical Drain Current Model

Parameter	Symbol	Value
Fitting Function	$F(V_G)$	$-0.3867{V'_{Gt}}^4 + 0.794{V'_{Gt}}^3 - 0.3803{V'_{Gt}}^2 - 0.1260V'_{Gt} - 0.0034$
Low Field Mobility	μ_{n0}	40 x 10^{-4} $m^2/V.s$
Fitting Constant $BETAN$	$BETAN$	2.5
Electron Saturation Velocity	VSATN	2.2 x 10^5 ms^{-1}

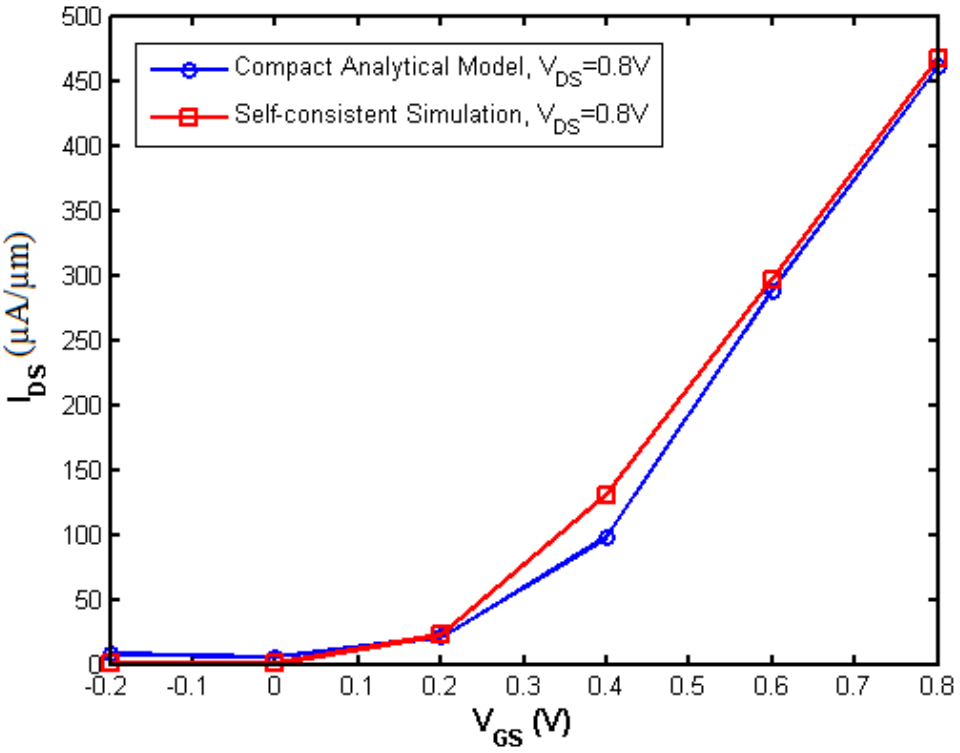


Figure 4.5: Current from the analytical model is matched with the simulated results by using appropriate fitting parameters.

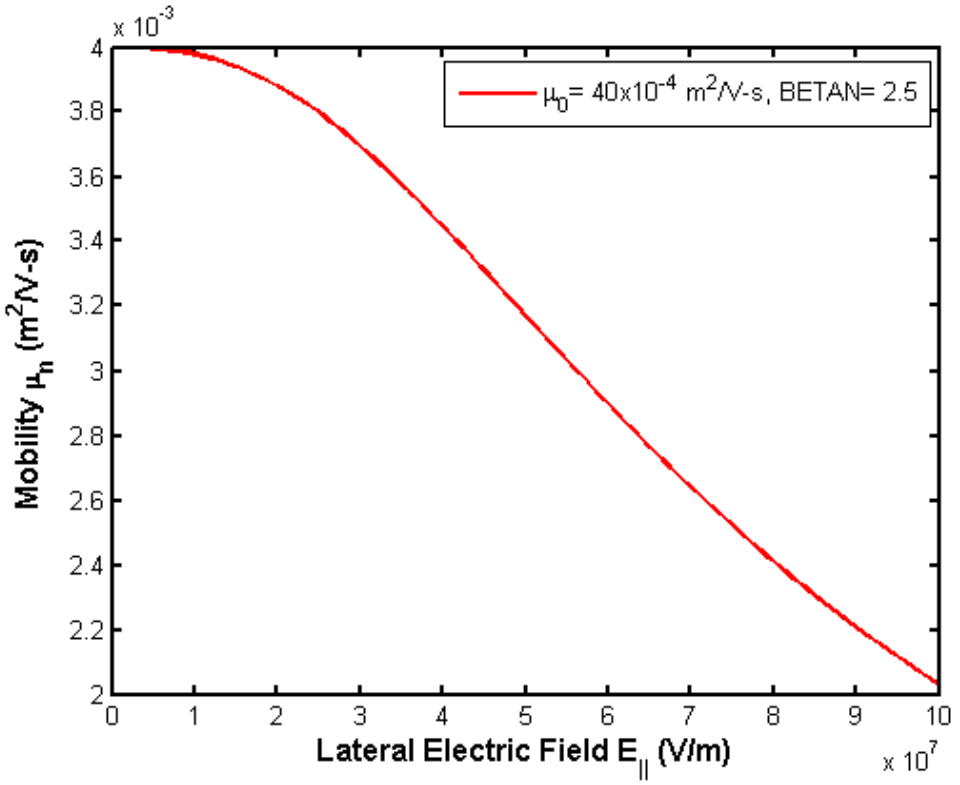


Figure 4.6: Field dependent mobility used to evaluate the analytical current.

4.6 Results and Discussions

The results in this section are obtained using a simplified Fitting Function, $F(V_G)$= - $\frac{V'_{Gt}}{7.6}$.

4.6.1 Transport Characteristics of the Analytical Device

Figure 4.7 and 4.8 displays the channel potential $\varphi(x)$ under different top gate bias conditions. The bottom gate voltage is kept at zero volts. Figure 4.8 demonstrates the effect of lateral electric field by showing minor change in the channel potential at the drain end despite of same gate voltage.

Figure 4.9 shows the inversion electron density in per unit area of the channel for top gate voltage of 0.8V. Figure 4.10 displays the full output characteristics (I_d-V_{ds}) of the device under different top gate voltage. The transfer characteristics (I_d-V_{gs}) of the device is shown in Figure 4.11 for different drain bias conditions.

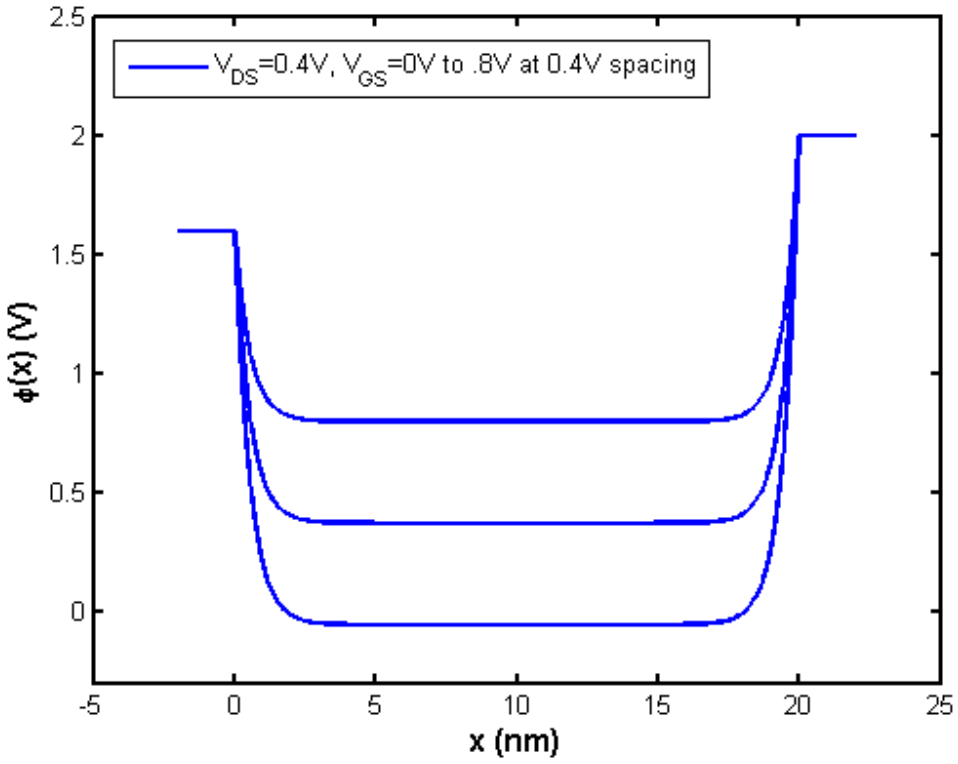


Figure 4.7: Channel potential $\varphi(x)$ under different top gate bias conditions. Bottom gate is fixed at 0V. Drain voltage is fixed at 0.4V. Gate voltage is varied from 0 to 0.8V.

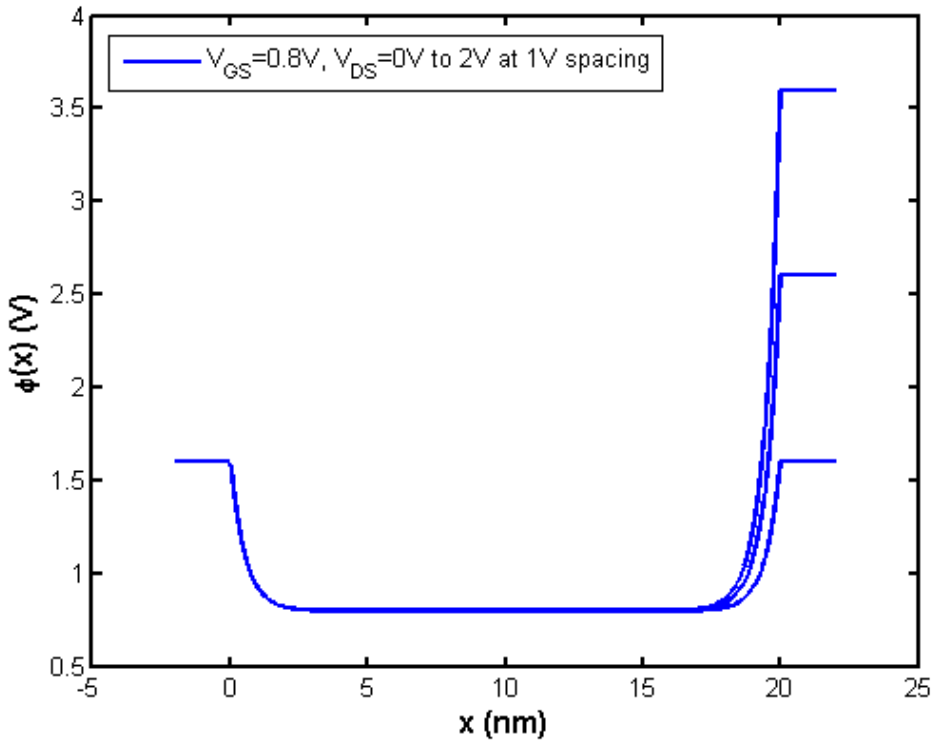


Figure 4.8: Channel po tential $\varphi(x)$ under di fferent d rain bi as c onditions. B ottom g ate i s fixed at 0V. Top gate voltage is fixed at 0.8V. Drain voltage is varied from 0 to 2V.

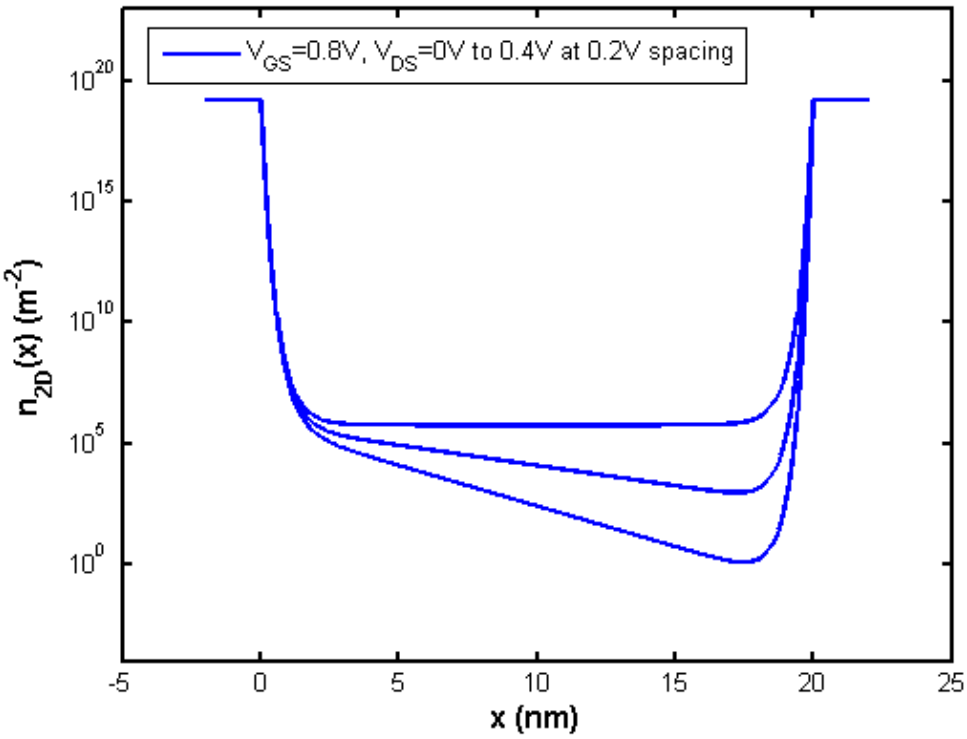


Figure 4.9: Channel i nversion car rier (electron) d ensity $n_{2D}(x)$ under d ifferent d rain b ias conditions. Top gate voltage is fixed at 0.8V. Drain voltage is varied from 0 to 0.4V.

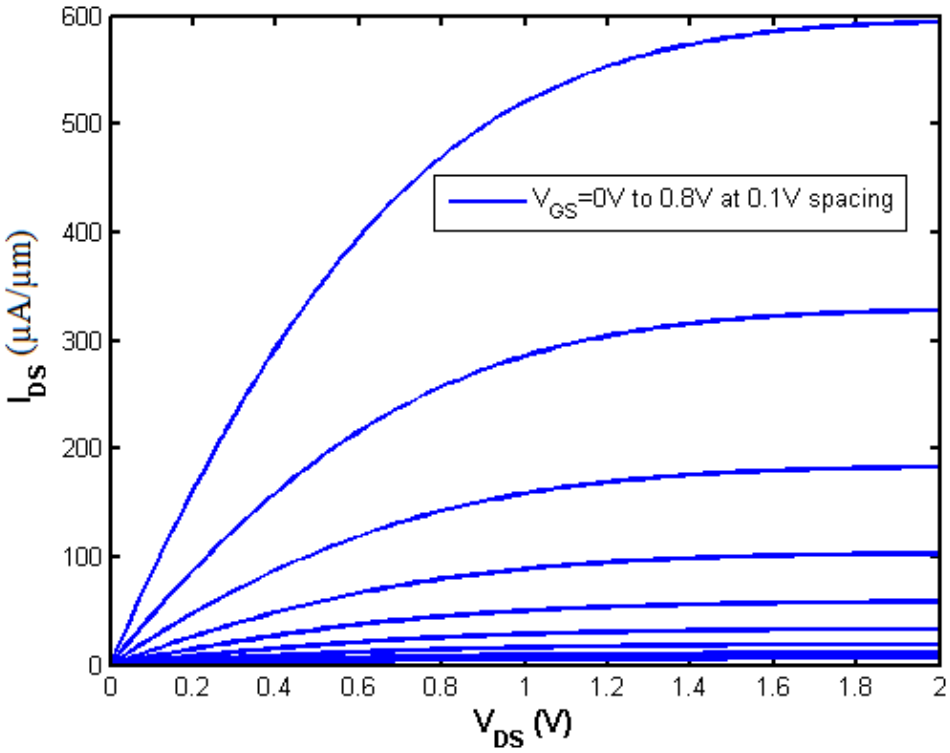


Figure 4.10: Output characteristics (I_d-V_{ds}) of the device under different top gate voltage. Bottom gate is fixed at 0V.

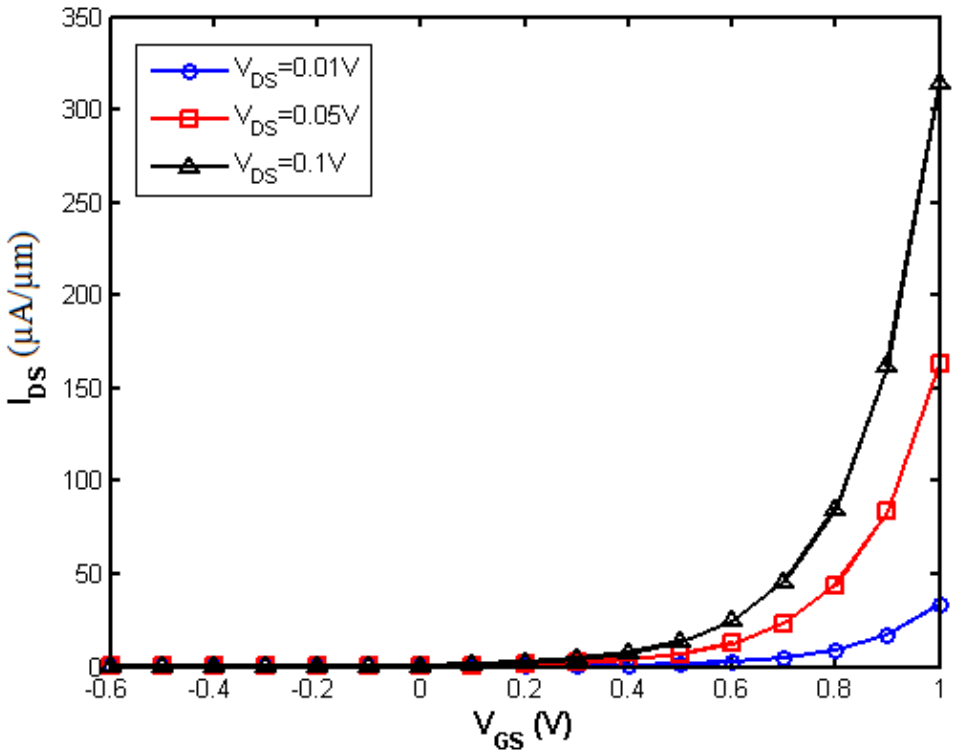


Figure 4.11: Transfer characteristics (I_d-V_{gs}) of the device under different drain voltage. Bottom gate is fixed at 0V.

4.6.2 Threshold Voltage Extraction

Threshold voltage is extracted from the $\sqrt{I_{ds}} - V_{gs}$ curve as shown in Figure 4.12. The x-intercept of the rising portion of the $\sqrt{I_{ds}} - V_{gs}$ curve indicates the threshold voltage. Figure 4.12, threshold voltages were calculated as 0.3 V, 0.36 V and 0.5 V respectively for 0.1 V, 0.05 V and 0.01V drain bias. This dependence of threshold voltage on drain bias arises from the effect of lateral electric in the channel due to shorter channel length.

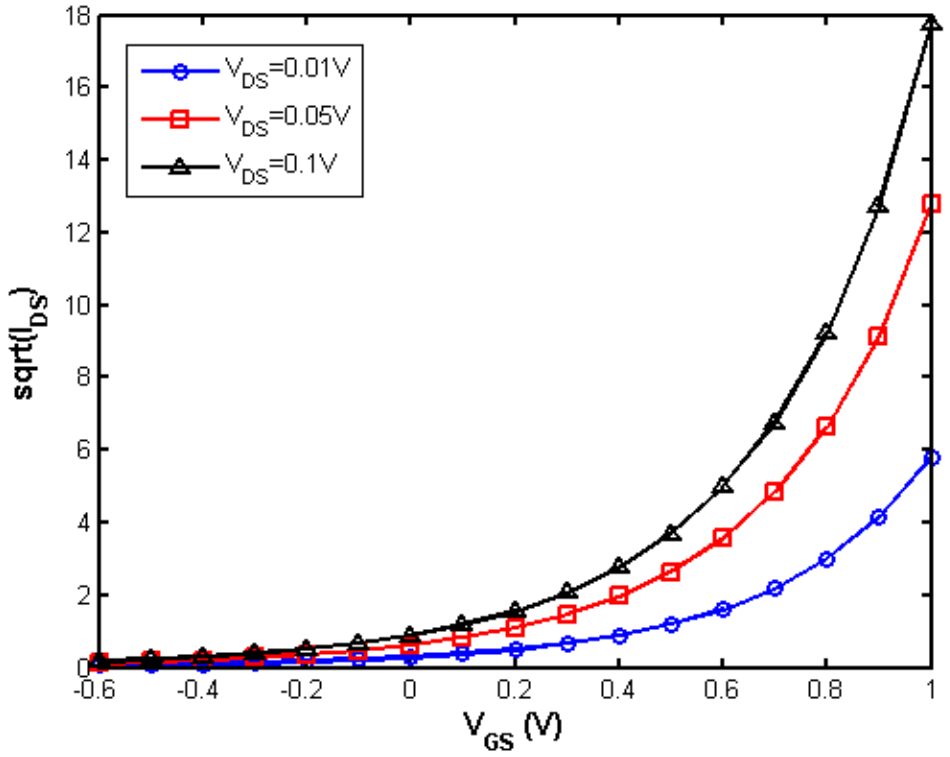


Figure 4.12: Threshold voltage extraction from the $\sqrt{I_{ds}} - V_{gs}$ curve for different drain voltages. Bottom gate is fixed at 0V.

4.6.3 Limitations of the Analytical Model

Since the 2D channel is assumed fully depleted under all bias voltages, this model cannot predict the behavior of the device in the subthreshold region. It overestimates the current at lower gate voltages, which eventually leads to overestimation of Subthreshold Swing (SS) and off-current. Also, on-off current ratio is gets underestimated for the same reason. These limitations can be overcome by estimating depletion region and depletion charge dynamically for each gate bias voltage.

Due to the gradual channel approximation, the effect of lateral electric field is ignored in the estimated channel potential. In the current calculation the effect of lateral electric field is brought back with a linear approximation. This assumption is particularly convenient for lower drain voltages but in higher drain voltage this results in overestimation of DIBL of the device. To solve this problem, effects of lateral electric field must be included in the solution of channel potential. However, this will result in numerical evaluation of the differential system of the device instead of a closed form analytical solution.

Chapter 5

Conclusion

This chapter summarizes the whole work and proposes some unexplored facts of this work which can be put under extensive research.

5.1 Summary

In this work, firstly a numerical simulator has been developed to study the electrostatics and quantum transport of monolayer WSe_2 FET. The simulator uses FUMS-NEGF formalism to calculate the ballistic transport characteristics of the monolayer WSe_2 FET. Whereas, the electrostatics is characterized by solving coupled 1D Schrödinger-Poisson's equations. The developed simulator is fully physically accurate and can be extended to calculate the ultimate performance limit of WSe_2 FET and study the effects of different physical parameter variation on the performance of the device. Using the simulator, an ultimately scaled monolayer WSe_2 FET structure has been proposed and performance parameters of that device have been extracted. The proposed structure is a downscaled n-FET version of an experimental WSe_2 FET, having 20 nm long monolayer channel, 10 nm long Au S/D contacts, 10 nm thick metallic Pd top gate, and 3 nm thick ZrO_2 and 5 nm thick SiO_2 top and bottom oxides respectively. Rigorous Quantum Mechanical simulation of the proposed structure revealed ON/OFF current ratio of 10^{10}, on current of 467.2 μA/μm, effective mobility of 300 $cm^2/V.s$, DIBL of 14.91 mV/V and SS of 77.72 mV/dec. In the second part of this work, a compact analytical transport model has been developed in addition to the numerical transport model. The analytical model solves the Poisson's equation for the inversion charge density to get the electrostatic potential in the channel. Current is then calculated by solving the drift-diffusion equation. The model makes "Gradual Channel Approximation" and "Quadratic Electrostatic Potential Approximation" to simplify the solution procedure, making it best suited for long channel devices with low drain bias voltages. To keep the model physically accurate for monolayer WSe_2 FET, appropriate density of states obtained from the first principle DFT simulation has been considered. The outcome of the model has been benchmarked against the numerical simulation results from the first part of this thesis with the help of few fitting parameters. In a nutshell, this thesis makes a comprehensive analytical and simulation study of monolayer WSe_2 developing physically accurate tools specifically for this purpose. The study confirms excellent ON and OFF state performances of monolayer WSe_2 FET and reveals it's potential for being the ultimate transistor for the next generation high speed low power applications.

5.2 Suggestions for Future Work

- In the numerical simulation, the 2D material channel is considered fully depleted under all gate bias condition. Although this assumption is true for strong inversion region, it introduces error in subthreshold current calculation. In future this limitation can be addressed by using a dynamic depletion width with applied gate voltages.

- To avoid computational complexity, FUMS approach is used for calculating the carrier concentration. For very high drain voltage where lateral electric field is very high this introduces errors in estimated band profile. To avoid this problem, Uncoupled Mode Space (UMS) approach can be utilized where multiple vertical cross section of the channel is considered to estimate the band profile of the channel.

- The developed estimates only ballistic current through the device. To evaluate more accurate transport performance of the device scattering can be introduced using Butikker probes inside the channel.

- The compact analytical model ignores the third order variations of the channel potential for simplicity. For a more accurate result, higher order variations of the potential can be considered by solving the governing differential equations numerically.

- The compact analytical model proposes a single model for all regions of operation of a device. Breaking this model into two separate models for subthreshold region and inversion region respectively can lead to more accurate results.

- The quasi Fermi level is assumed to be liner in the derived analytical model. For higher drain voltage assuming a parabolic quasi Fermi level with respect to the channel dimension can provide better estimation of charge carriers at those voltages, although the computational complexity will increase greatly.

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Appendix A

Journal Article Published

Saeed Uz Zaman Khan and Quazi D. M. Khosru. "Quantum Mechanical Electrostatics and Transport Simulation and Performance Evaluation of Short Channel Monolayer WSe_2 Field Effect Transistor." *ECS Transactions*, vol. 66, no. 14, pp. 11-18, 2015.

Quantum Mechanical Electrostatics and Transport Simulation and Performance Evaluation of Short Channel Monolayer WSe_2 Field Effect Transistor

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In this work a numerical electrostatics and transport simulator is developed for monolayer WSe_2 channel Field Effect Transistor (FET) considering Quantum Mechanical effects. For the electrostatics simulation 1-D Schrödinger-Poisson equations are solved self-consistently in the direction perpendicular to the channel. Whereas, the transport simulation employs Fast Uncoupled Mode Space (FUMS) approach with Non-Equlibrium Green's Function (NEGF) formalism. The simulator explored 20 nm long monolayer WSe_2 channel FET with top and bottom oxide thickness 3 and 5 nm respectively. This device showed excellent ON-state performance with maximum ON current reaching up to 467.2 A/m and maximum transconductance of 887.7 S/m. On the other hand, the OFF-state and short channel performances also showed promise with 10^{10} ON/OFF current ratio, 77.72 mV/dec Subthreshold Slope (SS) and 14.91 mV/V Drain Induced Barrier Lowering (DIBL). The overall performance reveals great potential of this monolayer WSe_2 FET in many low power and high speed applications.

Introduction

To counter the performance degradation of extremely scaled Field Effect Transistors (FETs) due to Short Channel Effects (SCEs), ultrathin body channel material with high band gap is essential (1). In recent years, researchers have been working on Graphene and monolayer Transition Metal Dichalcogenides like MoS_2, WSe_2 to find the channel material for next generation ultimately scaled transistors. Although, Graphene fulfills the condition of thin body channel and it has excellent carrier mobility, the absence of intrinsic band gap in Graphene sheet made researchers focus on Dichalcogenides like MoS_2. Despite of showing promise for low power application, MoS_2 based transistors are less suitable for high performance operation since monolayer MoS_2 has a high electron and hole effective masses and low carrier mobilities (2). In search of high mobility monolayer channel material, many other transition metal Dichalcogenides are being explored (3) and as a result of that endeavor monolayer WSe_2 based pFET has been fabricated (1). This experimental device with high band gap (1.6 eV) showed higher carrier mobility (250 cm^2/Vs) than monolayer MoS_2 based devices. In recent literature methods of n-type and p-type doping of monolayer WSe_2 FET have been demonstrated (4-5), which led to fabrication of high performance CMOS inverters solely based on monolayer WSe_2 channel (6). Despite of these promising experimental results, rigorous transport and electrostatic study of monolayer WSe_2 based FET is yet to appear in the

literature. In this work, we have performed a Quantum Mechanical electrostatics and transport simulation study on monolayer WSe_2 FET and calculated different performance parameters.

Firstly, 1-D Schrodinger-Poisson equations have been solved self-consistently (7) along the direction perpendicular to the channel to get the gate capacitance-voltage characteristics of the device. Then, ballistic transport characteristics were obtained by Fast Uncoupled Mode Space (FUMS) approach using Non-Equilibrium Green's Function (NEGF) formalism (8-9).

Device Structure

The device structure considered in this work is a downscaled nFET version of the device fabricated by Fang et al. (1). It has a 0.7 nm thick monolayer WSe_2 channel of length 20 nm deposited on a 5 nm thick layer of SiO_2. A 3 nm thick layer of ZrO_2 serves as the top oxide of the device (Figure 1). The metallic (Au) source/drain length is taken as 10 nm. Above the top oxide a metallic top gate of Palladium (Pd) is placed. The channel doping density is $1x10^{25}$ m^{-3}.

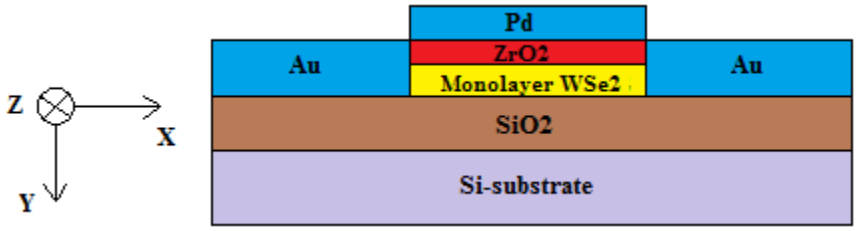

Figure 1. 2-D cross section of the monolayer WSe_2 channel FET with channel length of 20 nm and top and bottom oxide thickness of 3 nm and 5 nm respectively.

Simulator Development and Validation

To obtain the electrostatics of the device, 1-D Schrödinger and Poisson equations are solved self-consistently in the direction perpendicular to the channel (along y-axis). The charge density in the oxide region is zero and in the channel region it is given by-

$$\rho(y) = q\sum_i \int_{E_i}^{\infty} D(E)f(E)|\psi(y)|^2 dE \qquad [1]$$

where, q is the charge of electron, $D(E)$ and $f(E)$ are 2-D Density of State and Fermi-Dirac distribution function respectively. E_i and ψ_i are Eigen energy and wave function corresponding to i^{th} subband. Channel charge and Gate Capacitance are given by-

$$Q_{channel} = \int_y \rho(y)dy \;\; and \;\; C_G = \frac{dQ_{Channel}}{dV_G} \qquad [2]$$

The 2-D Transport simulator is developed using FUMS approach. Here, 2-D Poisson equation is solved using initially approximated charge to get the potential energy $U(x,y)$.

Then average potential energy along the confinement direction (y-axis) is obtained as,

$$\overline{U(y)} = \frac{1}{L_x}\int_0^{L_x} U(x,y)dx \qquad [3]$$

where, L_x is the length of the device. This average potential is substituted into the 1-D Schrödinger equation along the confinement direction-

$$\left[-\frac{\hbar^2}{2m_y^*}\frac{d^2}{d^2y} + \overline{U(y)}\right]\overline{\psi^m}(y) = \overline{E_{sub}^m}\,\overline{\psi^m}(y) \qquad [4]$$

which gives the average subband energy ($\overline{E_{sub}^m}$) and wave function ($\overline{\psi^m}(y)$) for m^{th} subband. In FUMS approach, the wave function is considered same as $\overline{\psi^m}(y)$ throughout the transport direction (along x-axis). Whereas the Eigen Energies are approximated using First Order Perturbation Theory-

$$E_{sub}^m(x) = \overline{E_{sub}^m} + \int_y U(x,y)|\overline{\psi^m}(y)|^2dy - \int_y \overline{U(y)}|\overline{\psi^m}(y)|^2dy \qquad [5]$$

From the $E_{sub}^m(x)$ 1-D device Hamiltonian (H) along the transport direction is formed. Now the retarded Green's function can be calculated as-

$$G^m(E) = (EI - H - \Sigma_S^m(E) - \Sigma_D^m(E))^{-1} \qquad [6]$$

where, I is a n identity matrix, $\Sigma_S^m(E)$ and $\Sigma_D^m(E)$ are the self energy matrices representing interaction of the channel with source and drain contacts. The spectral density matrices at source and drain contacts can be calculated as-

$$A_S^m(E) = G^m(E)\Gamma_S^m(E)G^{m\dagger}(E) \;\; and \;\; A_D^m(E) = G^m(E)\Gamma_D^m(E)G^{m\dagger}(E) \qquad [7]$$

where, $\Gamma_S^m(E)$ and $\Gamma_D^m(E)$ are the spectral broadening matrices at source and drain contacts given by-

$$\Gamma_S^m(E) = i\left(\Sigma_S^m(E) - \Sigma_S^{m\dagger}(E)\right) \;\; and \;\; \Gamma_D^m(E) = i\left(\Sigma_D^m(E) - \Sigma_D^{m\dagger}(E)\right) \qquad [8]$$

The 2-D electron density can now be calculated as-

$$n_x^m = \frac{1}{2\pi a}2\left(\frac{2m_z^* k_B T}{\pi\hbar^2}\right)^{1/2}\int_{-\infty}^{\infty}\left[\mathfrak{F}_{-1/2}\left(\frac{\mu_S - E}{k_B T}\right)diag\left(A_S^m(E)\right)\right.$$

$$\left. + \mathfrak{F}_{-1/2}\left(\frac{\mu_D - E}{k_B T}\right)diag\left(A_D^m(E)\right)\right]dE \qquad [9]$$

where, m_z^* is the transverse effective mass (along z-axis), μ_S and μ_D are source and drain Fermi levels respectively and a is the size of the unit cell of monolayer WSe_2. Function $\mathfrak{F}_{-1/2}$ denotes Fermi-Dirac integral of order $-1/2$. 3-D electron density is obtained by multiplying n_x^m with the transverse wave function $|\overline{\psi^m}(y)|^2$.

$$n_{3D}^m(x,y) = n_x^m\,|\overline{\psi^m}(y)|^2 \qquad [10]$$

The total electron density is obtained by summing the above equation for all subbands. The ballistic current is calculated as-

$$I = \frac{q}{2\pi\hbar} 2\left(\frac{2m_z^* k_B T}{\pi\hbar^2}\right)^{1/2} \int_{-\infty}^{\infty} \left[\mathfrak{F}_{-1/2}\left(\frac{\mu_S - E}{k_B T}\right) - \mathfrak{F}_{-1/2}\left(\frac{\mu_D - E}{k_B T}\right)\right] T(E) dE \qquad [11]$$

where T (E) is obtained by summing the transmission coefficient $T^m(E)$ over all subbands. $T^m(E)$ is given by-

$$T^m(E) = trace(\Gamma_S^m(E) G^m(E) \Gamma_D^m(E) G^{m\dagger}(E)) \qquad [12]$$

Material Parameters

To model the monolayer WSe_2 channel FET, we used band structure and material parameters available in the literature from first principle DFT simulations of Monolayer WSe_2 sheets. We considered same electron effective mass for both longitudinal and transverse direction of monolayer WSe_2. We also took only one subband and lowest conduction valley into consideration. Table I summarizes some of the monolayer WSe_2 channel parameters.

TABLE I. Monolayer WSe_2 Parameters

Property	Value	Property	Value
Thickness (1)	0.7 nm	Electron Affinity (10)	3.9 eV
Bandgap, E_g (10)	1.6 eV	m^*_e (10)	$0.33m_0$
Dielectric Contant (11)	7.25 ∥ 5.16 ⊥	m^*_h (10)	$0.45m_0$

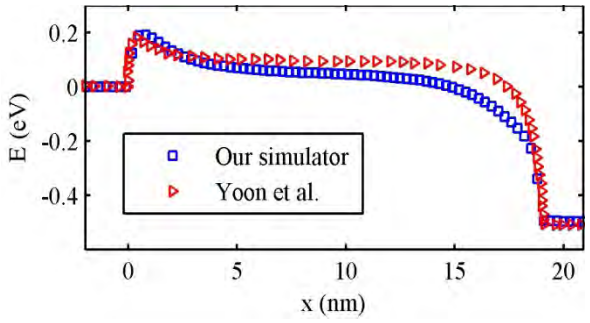

Figure 2. First subband energy across the channel for the monolayer MoS_2 channel device by Yoon et al. (2) at V_G=0 and V_D=0.5 V. Our simulation gives similar results.

Simulator Validation

The simulator is validated by comparing results from our simulator with the reported results of Yoon et al (2). The device simulated by Yoon et al. is a monolayer MoS_2 based transistor with gate length of 15 nm having 2 nm gate underlap at each side of the channel. It has metallic source/drain and top gate. The top oxide is 2.8 nm thick HfO_2 and SiO_2 serves as the bottom oxide. We simulated the exact device with our simulator and compared the 1st subband energy profile across the channel for V_G=0 and V_D=0.5 V in figure 2. The match is quite convincing at the top of the barrier. Although there is a

slight mismatch at the drain end, this will not affect the current output much since it depends mostly on the height of the barrier near source end.

Results and Discussion

Figure 3 shows variation of 1st subband energy along the channel with different bias voltage combination. The figure shows that variation of drain voltage does not affect the top of the barrier much, indicating presence of strong gate control over the channel and hence low DIBL. Figure 4a shows the drain current-voltage (I-V) characteristics of the device for different gate voltages. Peak current of 467.2 A/m is observed at $V_G=V_D=0.8$ V. The saturation region of the I-V curve also indicates low DIBL. On the other hand, figure 4b shows the gate capacitance-voltage (C-V) characteristics of the device. The curve saturates at about 0.009 F /m^2, which is significantly lower than the gate oxide capacitance of 0.0369 F /m^2. This supports the presence of quantum capacitance in the channel in series with the gate oxide capacitance.

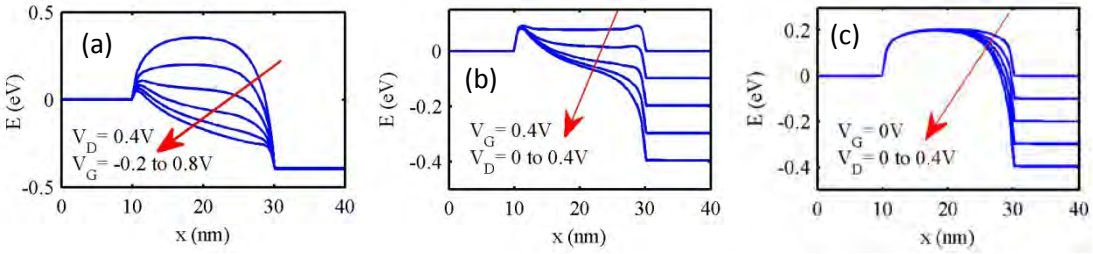

Figure 3. (a-c) First subband energy profile across the channel with different bias conditions.

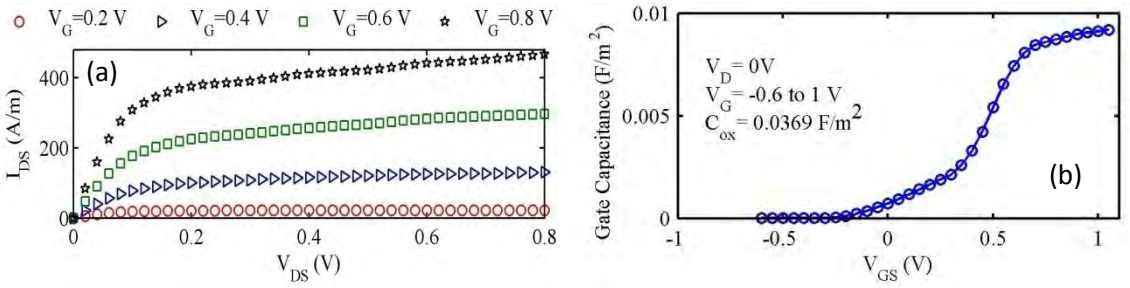

Figure 4 . (a) Drain current-voltage characteristics at different gate biases (b) gate capacitance-voltage characteristics at zero drain voltage.

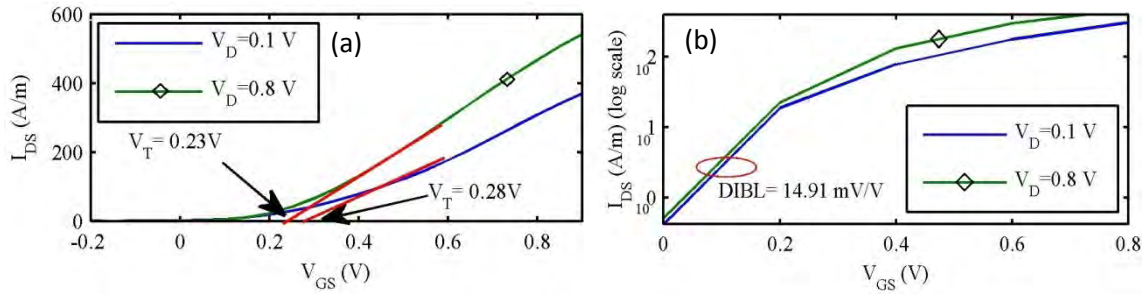

Figure 5. Extraction of (a) Threshold voltage and (b) DIBL at different drain biases.

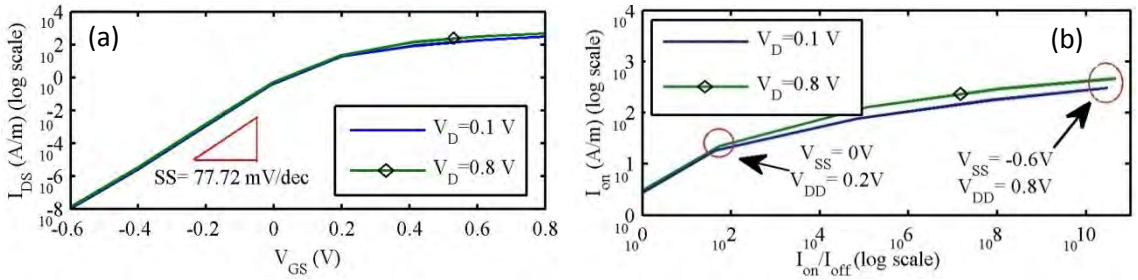

Figure 6. Extraction of (a) Subthreshold Slope (SS) and (b) ON/OFF current ratio at different drain biases.

Parameter Extraction

In figure 5 and 6 different transport performance parameters of the device are extracted. From figure 5a the threshold voltage is extracted as 0.23-0.28V. Figure 5b shows a DIBL of 14.91 mV/V, which is significantly lower than any conventional FET. In figure 6a, the Subthreshold Slope (SS) of the device is extracted as 77.72 mV/dec from the I_D-V_{GS} curve. On the other hand, figure 6b demonstrates that maximum ON/OFF current ratio of ~10^{10} is obtainable form this device with an ON and OFF voltage of 0.8V and -0.6V respectively.

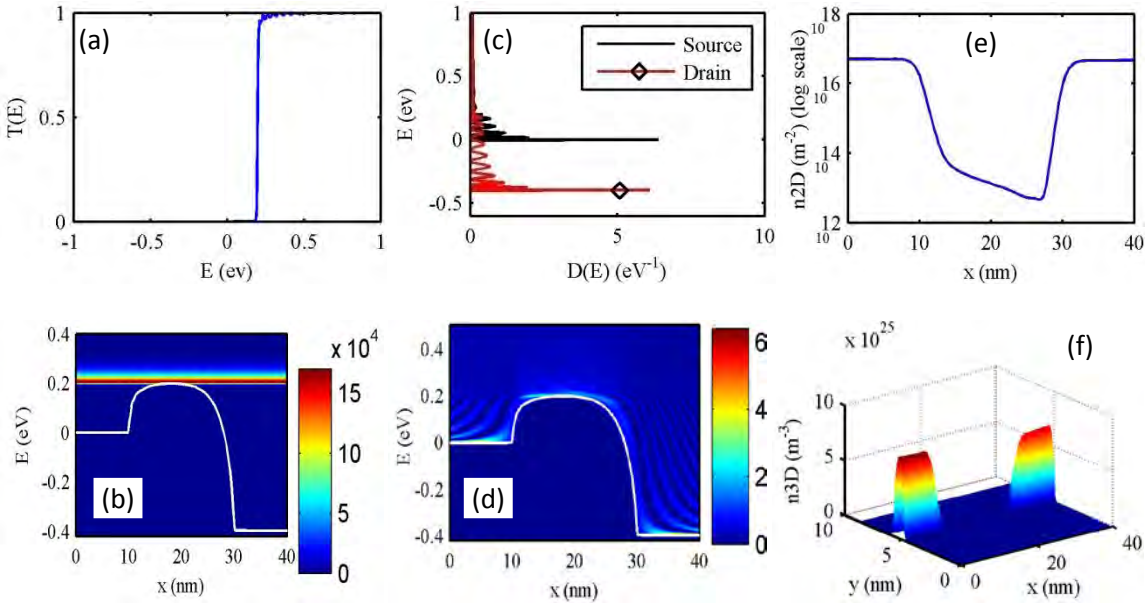

Figure 7. (a) Transmission co-efficient (b) Energy resolved current density (c) LDOS at source and drain end (d) LDOS along the channel (e) 2-D electron density (f) 3-D electron density across the device for gate and drain voltages of 0V and 0.4V respectively.

Transport Properties below Threshold Voltage

Figure 7 displays transport properties at V_G= 0V, which is below the threshold voltage of the device. In figure 7a the transmission co-efficient for first subband is shown. From the energy resolved current density in figure 7b it is observed that below threshold

voltage only energy levels at the top of the barrier contributes to the current. No tunneling current is present from source to drain. Figure 7c and 7d respectively shows Local Density of States (LDOS) at only source/drain terminal and throughout the channel. LODS peak at top of the barrier and source/drain energy levels, as expected. Figure 7e and 7f respectively shows 2-D and 3-D electron density in the device. For V_G= 0V 2-D electron density at the middle of the channel is of order 10^{13} m^{-2}.

Transport Properties above Threshold Voltage

Figure 8 displays transport properties at V_G= 0.5V. In figure 8a the transmission co-efficient for first subband is shown, which has shifted towards lower energy levels than the transmission co-efficient in figure 7a. Energy resolved current density in figure 8b shows contribution of tunneling in the transport. Local Density of States (LDOS) at only source/drain terminal and throughout the channel is shown by Figure 8c and 8d respectively. Figure 8e and 8f shows 2-D and 3-D electron density at ON condition. For V_G= 0.5V 2-D electron density at the middle of the channel is of order 10^{15} m^{-2}, which is significantly higher than electron density for V_G= 0V, as expected.

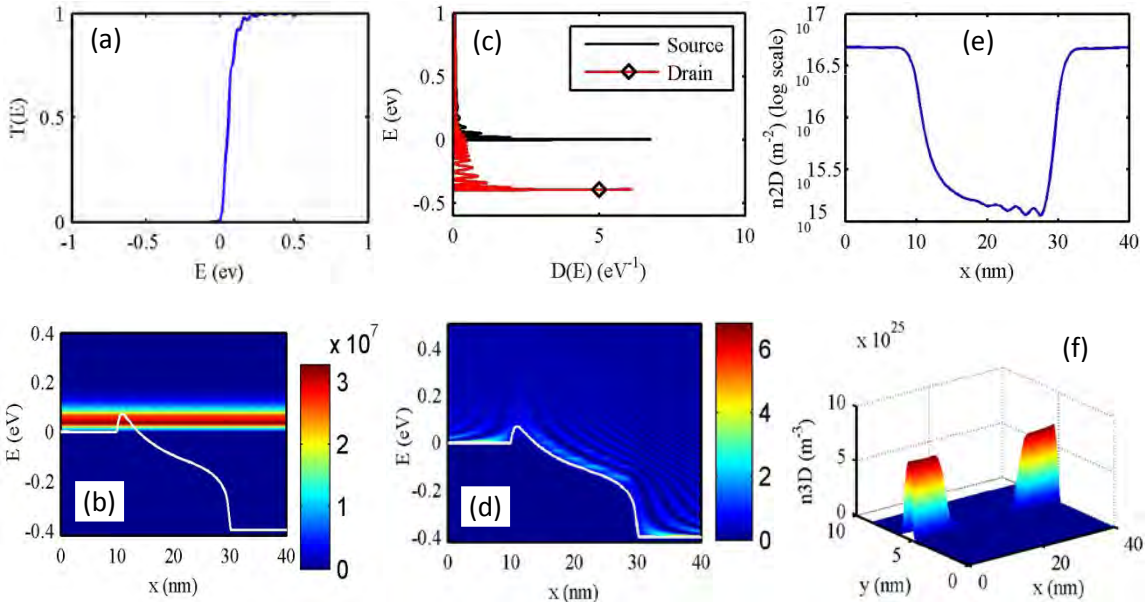

Figure 8. (a) Transmission co-efficient (b) Energy resolved current density (c) LDOS at source and drain end (d) LDOS along the channel (e) 2-D electron density (f) 3-D electron density across the device for gate and drain voltages of 0.5V and 0.4V respectively.

Table II lists some of the performance parameters obtained from the transport simulation. The parameters indicate that monolayer WSe_2 FET has a very high on-off current ratio (~10^{10}), which makes it suitable for low power applications. The extracted maximum effective mobility is also quite higher. The threshold voltage is found to be 0.23-0.28V for the proposed structure which can be tuned by changing doping profile and physical dimensions of the device. Also, using HfO_2 or other high-k material as top oxide, it is possible to get SS closer to theoretical lower limit of 60 mV/dec with this structure.

TABLE II. Device Performance Parameters

Property	Value	Property	Value
Threshold Voltage (V)	0.23 (@ V_D=0.8V)	Maximum g_m (S/m)	887.7 (@ V_D=0.8V)
SS (mV/dec)	77.72 (@ V_D=0.1V)	DIBL (mV/V)	14.91
Maximum I_{on}/I_{off}	~10^{10}	Maximum Effective Mobility (cm^2/Vs)	300
Peak Saturation Current (A/m)	467.2 (@ V_G=0.8V)		

Conclusions

In this work we have developed a numerical simulator to study the electrostatics and quantum transport of monolayer WSe_2 FET which can be extended to calculate the ultimate performance limit of WSe_2 FET and study the effects of different physical parameter variation on the performance of the device. We also proposed an ultimately scaled monolayer WSe_2 FET structure and extracted the performance parameters of that device. Rigorous Quantum Mechanical simulation revealed ON/OFF current ratio of 10^{10}, on current of 467.2 A/m, effective mobility of 300 cm^2/Vs, DIBL of 14.91 mV/V and SS of 77.72 mV/dec for the proposed device. With excellent ON and OFF state performances, monolayer WSe_2 FET has the potential for being the ultimate transistor for the next generation high speed low power applications.

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