PHYSICS BASED 2-D ANALYTICAL MODEL OF TRIPLE MATERIAL DOUBLE GATE TUNNEL FIELD EFFECT TRANSISTOR

by

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Approval Certificate

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সামিয়া সাফা

(Samia Safa)

Dedicated to

My beloved family.....

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I would first like to thank Almighty Allah for His continuous blessings upon me, especially in my educational life, and for bringing me to the position where I am at this very moment.

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Abstract

Tunnel FETs are attractive new devices for low-power applications due to their low off-current and their potential for a small subthreshold swing. In this work, analytical models of potential, electric field, drain current and gate threshold voltage have been proposed for Triple Material Double Gate (TMDG) TFET structure. Surface potential and electric field are formulated by exploiting Gauss's law in the lightly doped body region. A closed form expression of band-to-band tunneling current is developed by utilizing tunneling generation rate and the derived electric field model. An analytical model of gate threshold of TMDG TFET is derived from the surface potential equation based on its physical definition for TFETs. The developed models are then generalized for single and multiple material gate TFET structures. A numerical model of TMDG TFET structure is developed using ATLAS, Silvaco device simulator. The device parameters are chosen carefully based on the literature, so that the structure can provide high ON current, low leakage current and can suppress the ambipolar behavior of the device. The proposed models are then verified against the TCAD simulation results. The effects of varying device parameters and bias conditions on device performance are also analyzed. Based on the analysis, the validity range of the proposed models are defined and a solution to extend this validity range is suggested. The effect of Si film thickness on device's electrical characteristics is also studied, the physics governing it is detailed and an optimum value of Si film thickness is suggested. Analytical models are crucial in understanding the characteristics of a device and the proposed models will be helpful for designing circuits containing single material gate and multiple material gate TFET devices.

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Chapter 1

Introduction

Small swing devices are being researched intensively for the power crisis currently faced by conventional metal-oxide-semiconductor field-effect transistors (MOSFETs), due to their ever-increasing static power consumption. The reasons behind this crisis are explained, and then some currently used solutions are presented.

1.1 CMOS Solid State Switching Devices

In 1928, a patent was filed for a "device for controlling current" shown in Fig. 1.1 [1], a variant of a device that is now known as the MOSFET. Because of the difficulty to get a good oxide-semiconductor interface, it took until 1959 before the first MOSFET was fabricated [2]. But now, after many years of research and development a single chip now contains up to 6.8 billion of these devices. Being almost 90 years old, the semiconductor industry and its products are now a landmark of human civilization.

At the heart of the success story behind the MOSFET is the concept of scal-

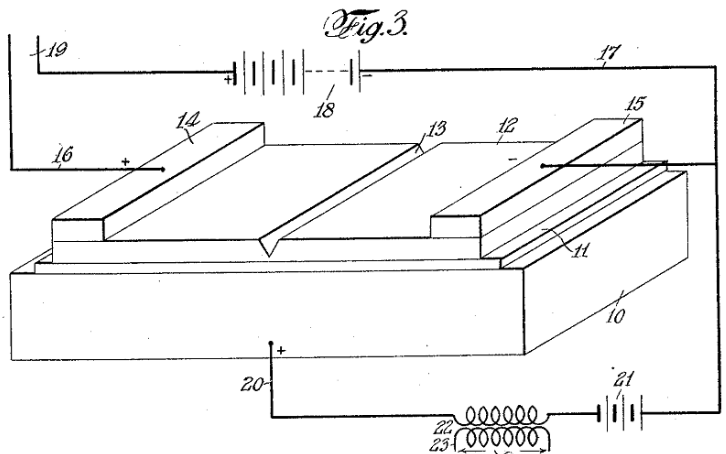

Fig. 1.1: Illustration from J.E. Lilienfeld's patent [1].

ing. For the past 50 years, the electronics industry has kept pace with Moore's Law [3], roughly doubling the number of transistors on a chip every two years. To maintain this trend, the size of individual transistors, known as MOSFETs, fabricated in complementary metal oxide semiconductor (CMOS) technology were reduced for each technology generation or node. The guidelines for reducing the dimensions of the transistor were originally developed by Dennard in 1974 [4] and were roughly followed for nearly three decades. In this "conventional scaling era", the reduction in size of each transistor increased speed while maintaining a constant power density. From a manufacturing perspective, adding more transistors for a given chip area lowered the cost per transistor. This threefold benefit to scaling CMOS revolutionized electronics and enabled technological advancement at a rapid pace.

Around the early-mid 2000's, conventional scaling ended and the industry moved to a power constrained scaling era [5]. In this era, the supply voltage (V_{DD}) of devices has not scaled with the other device parameters and dimensions.

This is because the threshold voltage (V_{TH}) must scale with the supply voltage in order to maintain a sufficient ON/OFF ratio. However, scaling of the threshold voltage results in an exponential increase in OFF state leakage. This is illustrated in Fig. 1.2 [6]. Two drain current vs. gate-source voltage ($I_D - V_{GS}$) transfer curves are shown for a MOSFET device at a high supply voltage (blue) and low supply voltage (red). In order to maintain the same ON current (I_{ON}), the threshold voltage must decrease with the supply voltage. This reduction of threshold voltage exponentially increases the OFF current. This increase in OFF current is guaranteed because of the constant subthreshold swing (SS) of the MOSFET.

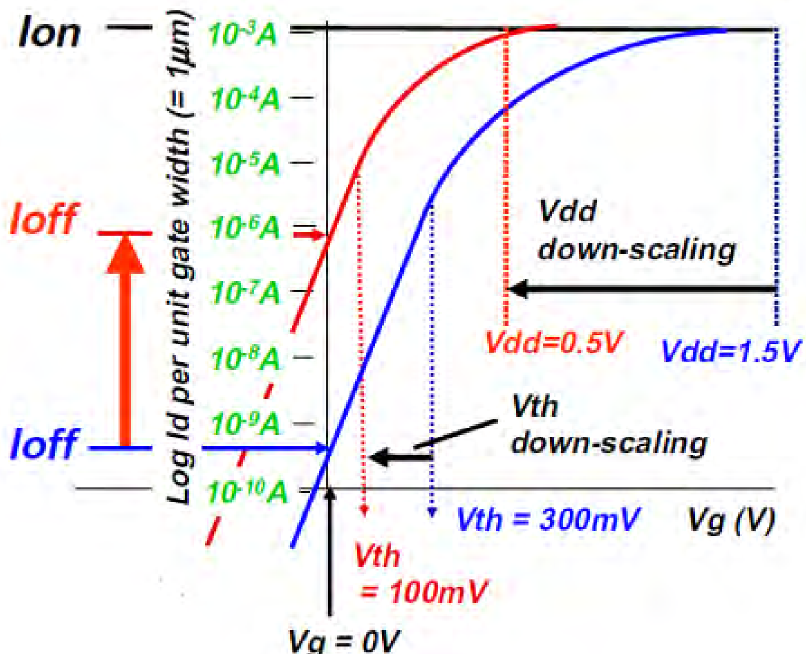

Fig. 1.2: Two MOSFET $I_D - V_{GS}$ curves operated at a high supply voltage (blue) and low supply voltage (red). To maintain the same I_{ON}, the threshold voltage of the red curve must decrease. This results in exponentially increased I_{OFF} because of the constant SS [6].

Subthreshold swing is a measure of the inverse slope of the $I_D - V_{GS}$ curve

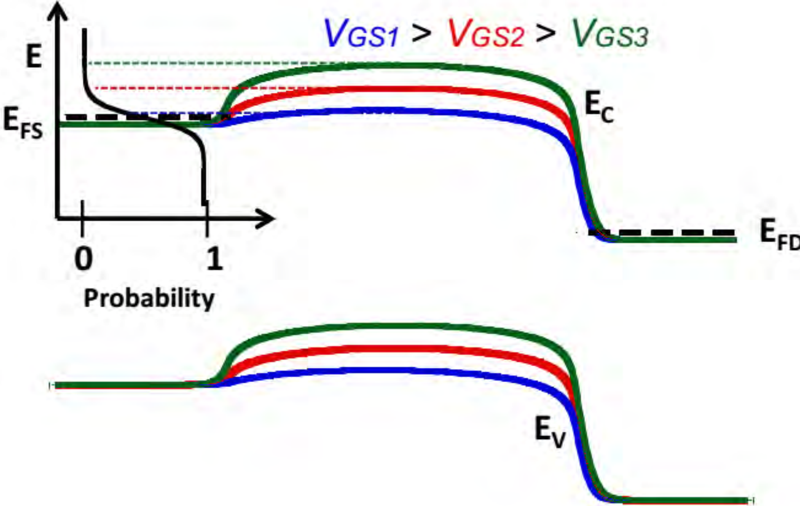

Fig. 1.3: Energy band diagram along the channel of a MOSFET with three different gate voltages applied. The Fermi-Dirac distribution function is sketched with respect to the source Fermi level to illustrate the electron occupation as a function of energy in the source.

below threshold, defined by

$$SS = \left(\frac{d\ln I_D}{dV_{GS}}\right)^{-1} \tag{1.1}$$

Due to the thermionic nature of the drain current in a MOSFET, there is a theoretical minimum value for a MOSFET of $(kT/q)ln(10) = 60mV/decade$, where k is Boltzmanns constant, T is temperature in Kelvin, and q is the electron charge. Conceptually, this can be understood with the aid of the energy band diagram along the channel of a MOSFET as shown in Fig. 1.3. Here, the Fermi level in the source is shown schematically with the Fermi-Dirac distribution function superimposed, illustrating the probability of finding an electron in the source at a given energy. Since the function asymptotically approaches zero, there are always some

electrons in the source with energy greater than the channel barrier. These high energy or hot electrons define the drain current in the OFF state and the distribution of electrons above the barrier varies exponentially as the surface potential is lowered. It is for this reason that SS is limited by kT and has a minimum of 60 mV/dec.

As a consequence of constant voltage scaling, power density increases if the circuit speed increases or if the transistor density increases. This is troubling particularly in today's world of mobile electronics where battery life and cooling constraints set limits on allowable power dissipation. These limitations have led to the industry's adoption of multi-core processors, which can increase the number of $MOPS/mW$ (million operations per second per milliwatt). In order to continue scaling of CMOS devices, new innovations and device designs will be required to overcome the challenges reviewed above.

1.2 Proposed Alternatives to CMOS-based Logic

To achieve good ON/OFF performance at a lower supply voltage, it is necessary to find a way to scale down the subthreshold swing. That is, overcome the $60mV/dec$ limit in SS of MOSFETs. In order to do this, a new current mechanism that does not involve carriers traveling over a potential barrier needs to be used. Fig. 1.4 qualitatively shows the benefit of a low SS for an alternative device. A steeply switching device allows for a lower threshold voltage (hence a lower power supply voltage, V_{DD}) and the possibility of a lower I_{OFF} which decreases the passive power consumption.

There have been some revolutionary innovations already adapted into CMOS

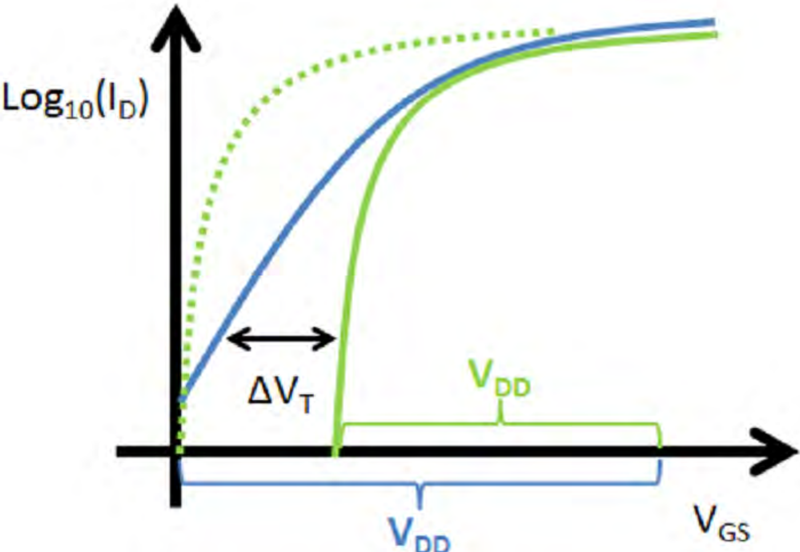

Fig. 1.4: A steeply switching device proves a compelling goal for a MOSFET replacement. The blue curve represents a traditional MOSFET $I-V$ transfer characteristic. The solid green curve comparatively highlights the main benefit of a steeper transfer characteristic: a reduction in the power supply voltage, V_{DD}. Presumably, a steeper SS characteristic can be threshold-voltage shifted (as depicted in the dashed green curve) [8].

devices in the most recent technology nodes. Mechanically-strained channels were introduced to increase mobility and enhance drive currents [7] around the $90nm$ node. At the $45nm$ node, high-k gate dielectrics and metal gates were introduced to improve electrostatics and suppress gate oxide leakage currents as the equivalent gate-oxide thickness decreased [9]. Most recently, Intel introduced Broadwell transistors at the $14nm$ node to improve energy efficiency [10]. Alternative transistor designs such as the tunneling based field-effect transistors [11, 12], impact ionization MOS [13, 14], ferroelectric FETs [15, 16] and electromechanical devices [17–23] have been proposed and demonstrated to achieve $SS < 60mV/dec$. Among these, the tunneling field effect transistor (TFET) and

electro-mechanical devices show the most promise for low power electronics applications.

1.2.1 Electromechanical Devices

The abrupt "pull-in" effect in electromechanical systems has been harnessed to realize new switching device designs with higher I_{ON}/I_{OFF} ratio for a given gate voltage swing. These devices utilize a movable beam for switching, and they can roughly be divided into two categories: the nano-electro-mechanical system (NEMS) field effect transistor and the micro-electro-mechanical system (MEMS) relay. While some MEMS switches seem to be just two-terminal devices, which might have extremely small values of swing [24] but are limited in terms of applications in circuits, others are three-terminal devices that could potentially replace conventional MOSFETs. There are many possible designs for this type of switch. One possibility is to fabricate a flexible cantilever beam connected electrically to the source terminal, which is activated by a gate electrode underneath, and pulled down to touch the drain electrode in the on-state [21]. Another possibility is to use a more typical MOSFET layout, with source, channel, and drain, as in the two devices shown in Fig. 1.5. The Fig. 1.5(a) has an air gap between the gate dielectric and the gate contact and the gate itself moves up (off-state) and down (on-state) [17]. Fig. 1.5(b) has source and drain regions on the substrate, and a moving gate/channel which can be pulled down into contact with the source and drain in the on-state [23]. Fig. 1.6 shows the transfer characteristics of the device shown in Fig. 1.5.

MEMS and NEMS switches are interesting due to their potentially high ON-

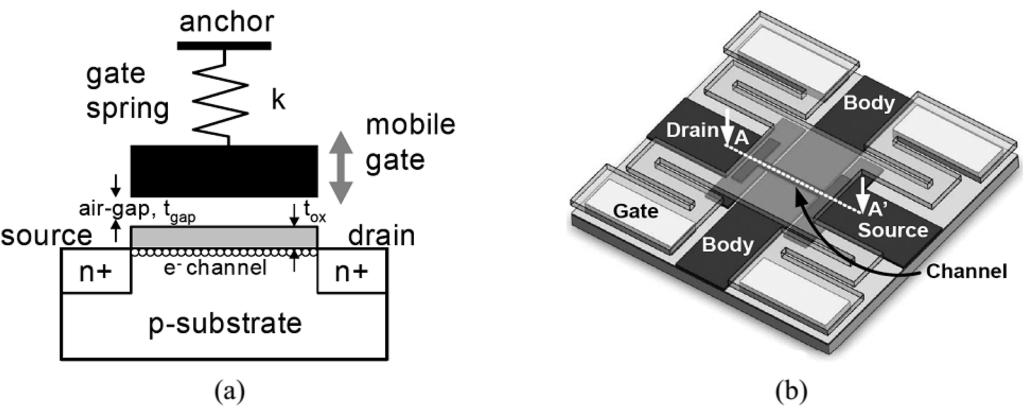

Fig. 1.5: Two possible designs for MOSFET-like MEMS relays, with a source, drain, and gate. (a) From [17]. (b) From [23].

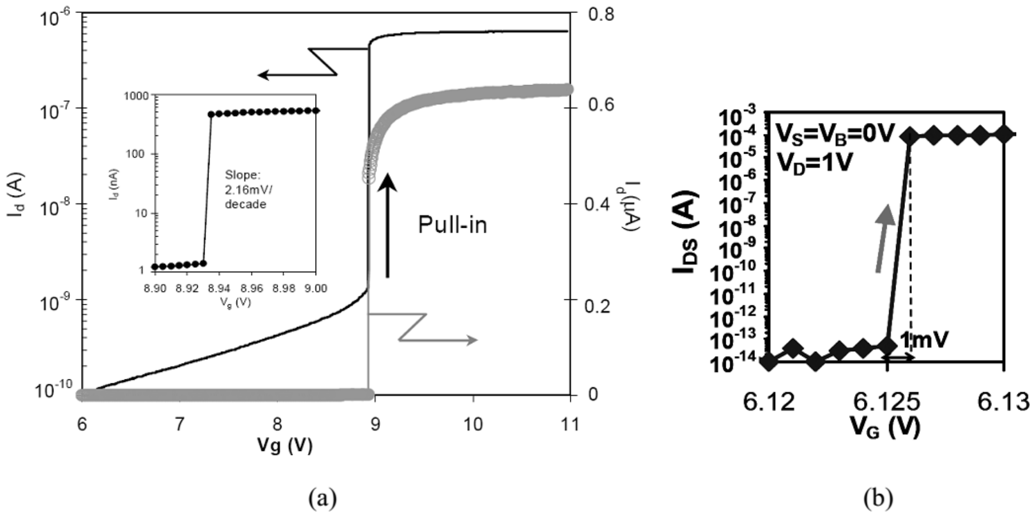

Fig. 1.6: Measured $I_{DS} - V_{GS}$ characteristics for the MEMS switches shown in Fig. 1.5(a) and (b), respectively, demonstrating extremely small subthreshold swings. The swing in this type of device is set by the voltage step size, has no fundamental limit, and can approach zero. (a) Junction leakage is still present for this relay design [17]. (b) Off-state current is much lower for a design in which the source and/or drain is physically separated from the MOSFET channel [23].

currents, very low OFF-currents, and small subthreshold swings. Their disadvantages include lower speed [21] and reliability problems due to their mechanical nature, such as structural damage where the two pieces need to touch each other and then come back apart thousands or millions of times [24].

1.2.2 Tunneling Field Effect Transistor (TFET)

Among all the alternative transistor designs, the tunnel field effect transistor (TFET) is the most promising due to its relative simplicity and resemblance to the conventional MOSFET. The TFET utilizes band-to-band tunneling (BTBT) current to achieve a more abrupt on-to-off transition than what is achievable through thermionic emission. Fig. 1.7 shows the energy band diagram of the TFET in on and off states.

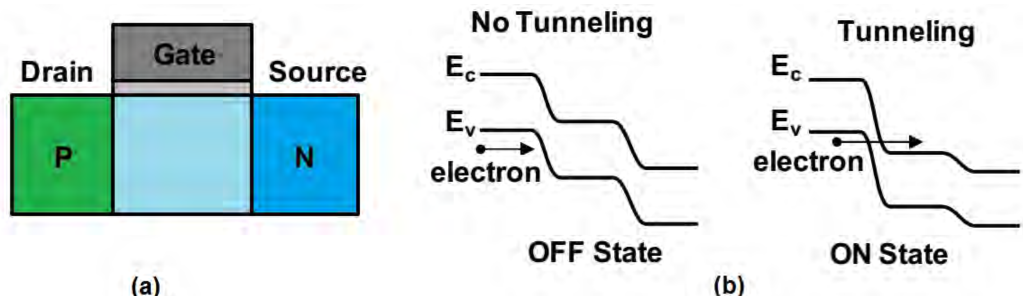

Fig. 1.7: (a)Schematic diagram of a tunneling field effect transistor and (b) its energy band diagram in the off and on states.

In a TFET, the predominant current flow is by tunneling through a barrier rather than by thermionic emission over a barrier as in a MOSFET. Fig. 1.8 shows the TFET energy band diagram, with the Fermi-distribution function shown schematically, analogous to Fig. 1.3. In the source, the valence band edge acts as a filter, i.e. there are no electrons in the high energy tail of the Fermi-Dirac

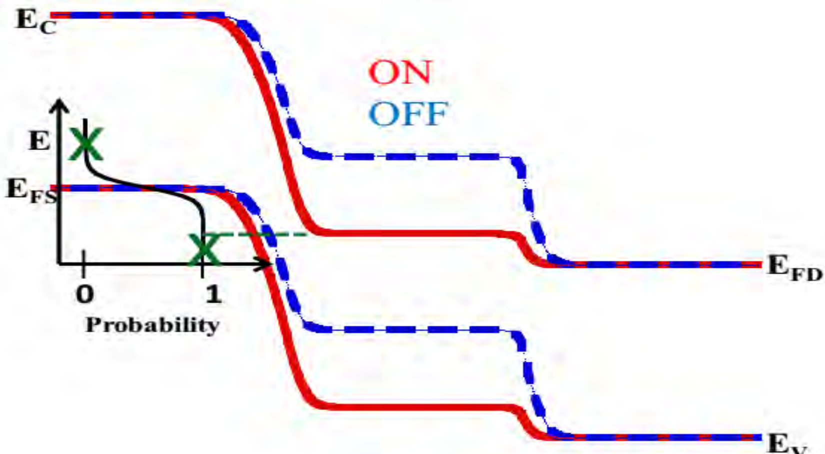

Fig. 1.8: Energy band diagram along the channel of a representative lateral TFET. ON state is shown in solid red and OFF state in dashed blue. The Fermi-Dirac distribution function is overlaid on the source Fermi level. In the ON state, the upper tail is cut off by the band gap and the lower tail suppressed by the large tunnel barrier across the channel. (green x's) [25].

distribution function because there is no density of states in the band gap. Similarly, the conduction band edge in the channel suppresses electrons in the source below this energy from tunneling. This energy filtering effect of the band edges results in "cold" carriers contributing to the current and hence, SS in a TFET is not expected to be limited by T and it can potentially achieve lower SS values, which has already been experimentally demonstrated [11]. However, a TFET achieves SS$<60mV/dec$ only at low current levels and that SS increases as I_{DS} increases [26–28]. Consequently, at high V_{DD} ($1V$) values, a silicon TFET has a significantly lower on-state current I_{ON} ($1\mu A/\mu m$ at $1V$) than a silicon MOSFET ($1mA/\mu m$ at $1V$). This remains a principal challenge for TFET designers. Another major shortcomings of this device is ambipolar conduction which makes its application difficult as a switching device.

1.3 Motivation and Objectives

Analytical models are powerful tools which can provide fast results, together with further insight on the working principles of the device; it is useful to design, simulate and fabricate a new device. TFET is a promising device which has low OFF-state leakage currents, and a better immunity to SCE due to a built-in tunnel barrier, and can provide a steep SS. Therefore, modeling potential of triple material double gate (TMDG) TFET is of great interest. Only a few analytical models of electric potential and drain current have been developed for this structure [29–31]. In [29], potential model is derived utilizing variable separation technique by solving 2-D Poisssons equation. In [30], 2-D Poisssons equation is solved employing Young's approximation for the formulation of potential model. An equation of drain current is also developed in this literature. Similar approach is used in [31] to find equation of potential for surrounding gate triple material TFET structure. So far no analytical model is developed for TMDG TFET structure based on the device physics. Although models are derived for surface potential and drain current, no analytical model is reported for the gate threshold voltage of TMDG TFET structure.

The objectives of this work are:

1. To develop physics based analytical models of electric potential, electric field, drain current, and gate threshold voltage for TMDG TFETs.

2. To develop 2D numerical simulation model of TMDG TFET using SILVACO ATLAS.

3. To verify the proposed analytical model with SILVACO ATLAS simulation

results.

4. To study and investigate the effects of model parameter variation on the performance of TMDG TFET and verify the results with SILVACO ATLAS simulation results.

The proposed analytical models of different useful device parameters of TMDG TFET can be used to investigate the circuit performance containing this device.

1.4 Thesis Organization

This dissertation consists of six chapters. The first chapter focuses on the limitations faced by the popular MOSFET switching devices due to aggressive scaling. Most promising alternatives for MOSFET devices and their shortcomings are mentioned. Finally, the motivation and objectives of this work is presented in this chapter. The second chapter includes the state-of-art of TFETs which is then followed by the TMDG TFET structure considered in this work and the operating principle of this structure.

The third chapter discloses surface potential and electric field model formulation procedures of TMDG TFET structure by exploiting Gauss's law. The surface potential model is extended to a 2-D potential model by considering parabolic approximation. The expression of band-to-band tunneling current is developed by utilizing tunneling generation rate and the derived electric field model. An analytical model of gate threshold of TMDG TFET is formulated from the surface potential equation based on its physical definition for TFETs. The developed models are then generalized for single and multigate TFET structures. The fourth

chapter gives a brief introduction to the Silvaco ATLAS simulator used for developing the numerical model of TMDG TFET considered in this study. The method of extracting the tunneling parameters of the device from the experimental data is described later. Threshold voltage extraction from the simulation results and necessary de-noising procedures are also included in this chapter.

The fifth chapter measures the accuracy of the developed models by comparing the results of analytical models with the TCAD simulation results. The effects of varying bias conditions and device parameters on surface potential, electric field, drain current and gate threshold voltage are analyzed. Based on these analysis, the validity conditions of the proposed models are extracted and a solution to extend the validity range of the models is suggested. Finally, the effect of Si film thickness on electrical characteristics of the device is studied, the physics governing it is detailed and an optimum value of Si film thickness for optimized device performance is suggested for future fabrication of TMDG TFET structures.

The last chapter marks the end of the dissertation with a summary of the work done. It also mentions the scopes for further improvement of the work and provides a suggestion of the possible areas which can be explored in future.

Chapter 2

TMDG TFET

2.1 Introduction

As technology and scientific insight move forward, new possibilities open themselves to mankind. In this section, the working principle of an electronic switch exploiting the quantum mechanical tunneling process is investigated. The electronic device under investigation in this work is called the triple material double gate (TMDG) tunnel field-effect transistor (TFET) and could provide a big improvement over existing MOSFET technology.

2.2 History and State-of-the-art of the TFET

Quinn *et al.* at Brown University [32] were the first to propose the gated p-i-n structure of a Tunnel FET in 1978, and suggested the usefulness of this device for spectroscopy. Banerjee *et al.* at Texas Instruments [33] studied the behavior of a three-terminal silicon tunnel device using a p^{-}-region instead of an i-region under

the gate. Takeda et al. at Hitachi [34] created a band-to-band tunneling MOS device on silicon that they called the B^2T-MOSFET, and showed the lack of V_{TH} roll-off when scaling, and the temperature dependence of the device characteristics. Baba at NEC [35] fabricated Tunnel FETs which he called Surface Tunnel Transistors, using MBE to create mesa structures in III-V materials. In 1995, Reddick and Amaratunga at Cambridge [36] published measured characteristics of silicon Surface Tunnel Transistors. They were motivated by the desire for devices that would be faster than conventional MOSFETs, as tunneling devices are, and that could be scaled down more easily without running into problems such as punchthrough. They are sometimes erroneously given credit for being the first to make silicon Tunnel FETs. In 1997, Koga and Toriumi at Toshiba [37] proposed a post-CMOS three-terminal silicon tunneling device with the same structure as a Tunnel FET, though the experimental results which were presented showed a device that was forward-biased.

In 2000, Hansch *et al.* at the University of the German Federal Armed Forces in Munich [38] showed experimental results from a reverse-biased vertical silicon tunneling transistor made with MBE, with a highly-doped boron delta-layer to create an abrupt tunnel junction, and noted the saturation behavior in the $I_D - V_G$ characteristics. Aydin and Zaslavsky at Brown Univ., along with their collaborators in New York and France [26] fabricated Lateral Interband Tunneling Transistors on SOI in 2004. These devices used a different Tunnel FET structure without an intrinsic region, instead placing the gate over a p-n junction, claiming that this would reduce gate capacitance and therefore increase speed. The authors also claim that there should be no current saturation for these devices. Similar devices on bulk silicon had already been investigated by Grove and Fitzgerald in 1965

[39].

In 2004, band-to-band tunneling was demonstrated in carbon nanotube (CNT) FETs by Appenzeller *et al* [40]. In order to create the energy bands necessary for tunneling, a back gate and a top gate were used. The researchers claimed that the one-dimensionality of the CNTs led to extremely different band bending conditions than those in 3-D semiconductors. A subthreshold swing smaller than the $60mV/dec$ limit of conventional MOSFETs was reported for the first time, which was a momentous occasion, even if the low swing value was only between a couple of points at very low current values. A year later, Appenzeller *et al.* [41] published a comparison of several CNT transistors, and concluded that the Tunnel FET, now with only one gate, was the superior device and showed conventional-looking $I_{DS} - V_{DS}$ output characteristics while still achieving a subthreshold swing of less than $60mV/dec$.

Bhuwalka *et al.* at the University of the German Federal Armed Forces in Munich [12] published the first of many articles about their vertical Tunnel FET on silicon with a SiGe delta layer, grown by MBE in 2004. The SiGe replaced the silicon delta layer already used by Hansch, and in theory, the smaller bandgap should have reduced the tunnel barrier width and increased tunneling current in the on-state as well as lowering the subthreshold swing. In 2006, the same group proposed a lateral Tunnel FET on SiGe on insulator [42], and showed through simulation that on-current would increase with the percentage of Ge in the SiGe. No experimental results have been published to date by this group for these devices. In 2006, Zhang *et al.* at Notre Dame [43] remarked once again what others before them had noticed that theoretically, it is indeed possible for Tunnel FETs to have a subthreshold swing lower than $60mV/dec$. The structure they studied was

a gated p-n diode, but the general equations they put forth, and the band-to-band tunneling behavior, would be the same as for a gated p-i-n structure.

In 2007, Verhulst *et al.* at IMEC showed by simulation that shortening Tunnel FET gate length, so that the gate covers the source-side junction where tunneling takes place, but does not cover the majority of the intrinsic region, has the benefits of decreasing off-current (tunneling through the drain-side junction) and reducing speed, with a small or no reduction in the on-current, depending on the device design [44]. In the same year, Toh at the National University of Singapore published a study of double-gate Tunnel FET silicon body thickness optimization, in which he showed an optimal device thickness for maximum on-current [45]. Nagavarapu *et al.* at UCLA suggested a pnpn device design in 2008, in which a narrow region of the opposite doping is introduced into the Tunnel FET source just under the gate edge. This narrow region acts as a source of electrons, and increases the band bending and the electric field at the tunnel junction, thus increasing on-current [46].

2009 had been a busy year for the Tunnel FETs. Schlosser *et al.* at the University of the German Federal Armed Forces in Munich studied the simulated advantages of putting an extremely high-*k* dielectric on a Tunnel FET, and the benefits of the fringing fields when the dielectric is only over the intrinsic region [47]. Vadizadeh *et al.* at the University of Tehran presented a simulation study of Tunnel FETs in which a high-*k* dielectric covered the tunnel junction, and the rest of the intrinsic region was covered by a low-*k* dielectric [48]. This technique led to little improvement in device characteristics, however; most of the shown improvement actually came from a shift in the gate work function which shifted their I-V curves along the voltage axis. Patel *et al.* at UC Berkeley simulated an

interesting device whose band-to-band tunneling takes place perpendicularly to the gate dielectric surface, and showed that it would have a very small subthreshold swing and a high on-current [49]. Their device has an ultra-shallow n+ pocket at the surface of the p+ drain (for an n-type device), and the gate overlaps this pocket. When gate voltage is applied, carriers tunnel upward from the p+ source into the n+ pocket, and then drift to the drain.

There were also some fabricated Tunnel FET results in 2009. Sandow *et al.* from Forschungszentrum Jülich published experimental data for p-type Tunnel FETs on SOI, showing the effects of varying source and drain doping levels, gate dielectric thickness, and device length [50]. Kazazis *et al.*, with his colleages at Brown University and in France, fabricated Tunnel FETs on thin GeOI that showed very high leakage, with $I_{ON}/I_{OFF} < 100$ [51]. Moselund *et al.* at IBM's Zurich Research Laboratory fabricated Tunnel FETs on silicon nanowires with a wrap-around gate, using two different gate dielectrics: SiO_2 and HfO_2 [52]. The nanowires were grown vertically and doped *in-situ*, and then deposited on a prepatterned substrate where the gate dielectric was deposited and the drain, source, and gate contacts were made. Improvements in subthreshold swing and on-current were seen with the use of a high-*k* dielectric.

In order to enhance the ON current, various design improvements in terms of band gap engineering, hetero junction TFETs strained silicon, novel architectures like P+N+I-N, gate all around structure have been proposed [53–58]. Effect of gate material on energy band profile and overall performance of TFET has been studied in [59, 60]. In 2011, Saurabh *et al.* introduced the idea of dual material double gate TFETs and showed that it is possible to achieve better ON current, smaller leakage current and improved SS with this structure [61]. Unfortunately,

the ambipolar effect cannot be completely inhibited using this configuration. In the same year, Liang *et al.* proposed a novel triple material gate (TMG) TFET structure which shows a higher on current, a reduced SS, a suppressed ambipolar conduction and better switching characteristics [62]. In 2015, Saraswathi *et al.* showed that a gate-all-around TMG TFET structure shows better immunity to short channel effects and hot carrier effects [31].

2.3 Device Structure

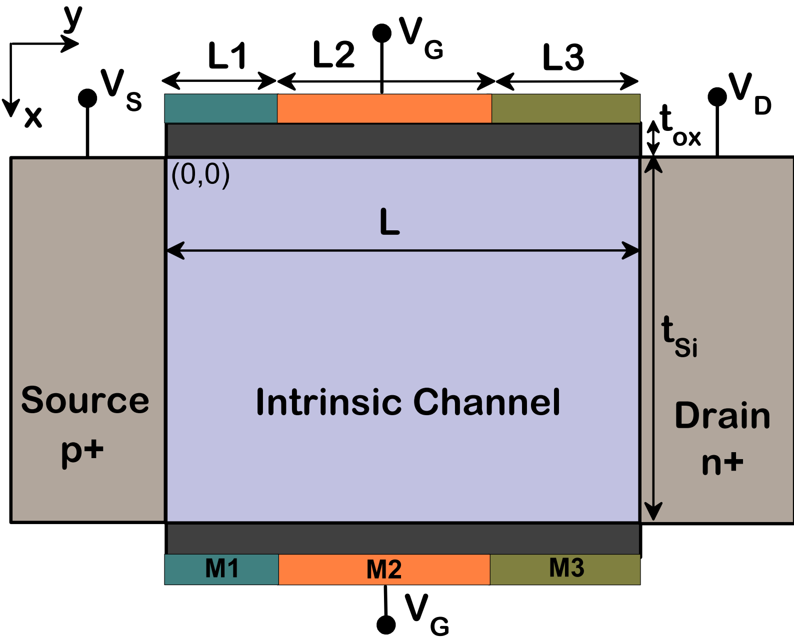

Fig. 2.1: Schematic diagram of TMDG TFET.

The schematic of TMDG TFET structure considered in this work is shown in Fig. 2.1. Source is highly p-type doped with doping concentration of N_{source} and drain region is n-type doped with doping concentration of N_{drain}. The channel is

lightly n-type doped with doping concentration of N_{Ch}. Three metals $M1$, $M2$, and $M3$ with different workfunctions ϕ_{m1}, ϕ_{m2}, and ϕ_{m3} respectively form the gate. To improve the ON-current to OFF-current ratio, ϕ_{m2} is kept higher compared to ϕ_{m1} and ϕ_{m3} [30]. The total gate length of the device is $L = L_1 + L_2 + L_3$ where L_1, L_2, and L_3 are length of metal gate $M1$, $M2$, and $M3$ respectively. The thickness of oxide film is t_{ox} and silicon film thickness is t_{si}.

2.4 Operating Principle of TFETs

Current conduction mechanism in Tunnel FET devices is solely based on tunneling process. The gate near the source region is responsible for tunneling mechanism between source/body junctions. Conduction band and valence bands of the TMDG TFET during on-state and off-state are shown in Fig. 2.2. The electric field in the source-channel junction increases due to increase in band bending in that region because of less value of ϕ_{m1}. A higher value of ϕ_{m2} creates a barrier in the channel and a lower value of ϕ_{m3} creates a bandpass filter structure [71]. The height of this barrier is tunable by the gate voltage. During OFF-state ($V_{GS} = 0V$ and $V_{DS} = 1V$), no overlap occurs between the occupied band of the source and the unoccupied band of the channel, so the tunneling process will not take place and also the barrier in the channel region blocks the reverse tunneling of the carriers; therefore, the OFF-current is very low. When gate voltage is large enough, the conduction band of channel region goes below the valence band of source region and a sufficiently high lateral electric field is created at the source-channel junction. In the ON-state ($V_{GS} = 1V$ and $V_{DS} = 1V$), the barrier width is small enough to allow tunneling and the electric field forces the electrons to tun-

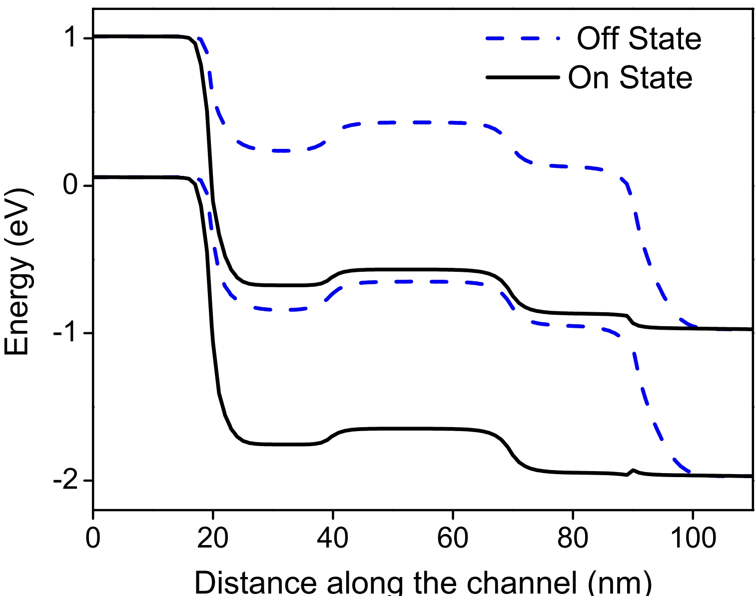

Fig. 2.2: Energy band diagram of TMDG TFET at OFF-state ($V_{GS} = 0V$ and $V_{DS} = 1V$) and ON-state ($V_{GS} = 1V$ and $V_{DS} = 1V$).

nel from valence band of source region to the conduction band of channel region. The tunneled electrons then move towards the drain end through drift diffusion mechanism.

Chapter 3

Analytical Model of TMDG TFET

3.1 Introduction

Analytical models are important to predict the behavior of devices. The formulation of analytical models of fundamental TMDG TFET characteristics are exihibited in this chapter. The derivation of 1-D surface potential is carried out by exploiting Gauss's law in the lightly doped channel region. The 1-D model is then extended to 2-D potential model by using parabolic approximation which is followed by the development of electric field model. The expression of electric field is used to calculate the band-to-band tunneling current by extracting tunneling generation rate. Finally, the physical definition of gate threshold voltage of TFETs is addressed and an analytical model is developed based on that definition.

3.2 Electric Potential Distribution

3.2.1 Surface Potential

Surface potential is defined as the electrostatic potential energy of surface confined charges. To find the surface potential, Gauss's law can be applied to a Gaussian box of height t_{Si} and width Δy in the lightly doped body region as shown in Fig. 3.1. Neglecting mobile charges and source-channel, drain-channel depletion regions, the following equation can be derived [72]:

$$\frac{\epsilon_{si}t_{si}}{\eta}\frac{\partial E_{sf(i)}(y)}{\partial y} + \epsilon_{ox}\frac{V'_{GS(i)} - \psi_{sf(i)}(y)}{t_{ox}} + \epsilon_{ox}\frac{V'_{GS(i)} - \psi_{sb(i)}(y)}{t_{ox}} = qN_{Ch}t_{si} \quad (3.1)$$

where, $E_{sf(i)}(y)$ is electric field at top oxide-semiconductor interface and $i = 1, 2,$

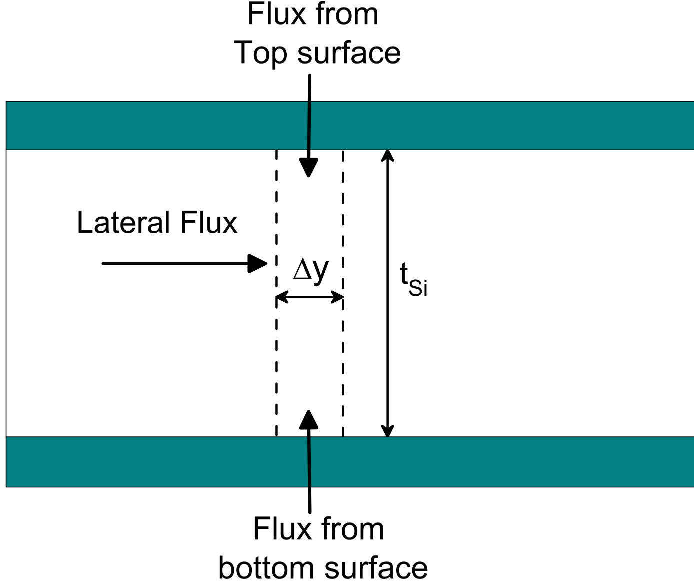

Fig. 3.1: Gaussian box in the channel region of TMDG TFET.

and 3 delimit three channel region under $M1$, $M2$, and $M3$ respectively. $\psi_{sf(i)}(y)$ and $\psi_{sb(i)}(y)$ are potential at top and bottom oxide-semiconductor interface respectively. η is the channel spreading parameter which is weakly dependent on channel thickness and doping. The value of η is constant varying between 1 and 1.3 [73] and can be extracted from simulation or experiment. In this work, $\eta = 1$ is used. $V'_{GS(i)}$ is calculated as

$$V'_{GS(i)} = V_{GS(i)} - V_{FB(i)}$$

$V_{FB(i)}$ is the flatband voltage which is a function of metal and semiconductor workfunction:

$$V_{FB(i)} = \phi_{m(i)} - \phi_S$$

where, $\phi_{m(i)}$ is metal workfunction and ϕ_S is semiconductor workfunction. ϕ_S can be expressed as

$$\phi_S = \chi_{si} + \frac{E_G}{2}$$

Here, χ_{si} is electron affinity and E_G is semeconductor bandgap.

The right-hand side of Eq. (3.1) represents the net charge in the Gaussian box. The electric flux entering the Gaussian box in lateral direction is represented by the first term on the left-hand side of (3.1). The second and third term of Eq. (3.1) on the left-hand side represent the electric flux entering the Gaussian box from top and bottom surface.

The bottom interface potential, $\psi_{sb(i)}(y)$ can be expressed in terms of $\psi_{sf(i)}(y)$

by solving 1-D Poisson's equation in x-direction of Fig. 2.1.

$$\psi_{sb(i)}(y) = \psi_{sf(i)}(y) - E_{sf(i)}(y)t_{si} - \frac{qN_{Ch}t_{si}^2}{\epsilon_{si}} \tag{3.2}$$

Surface electric field can be obtained by applying electric displacement vector continuity condition at top oxide-semiconductor interface.

$$E_{sf(i)}(y) = \frac{\epsilon_{ox}}{\epsilon_{si}}\frac{(V'_{GS(i)} - \psi_{sf(i)}(y))}{t_{ox}} \tag{3.3}$$

Substituting (3.2), (3.3) in (3.1) a simple second order non-homogeneous differential equation of surface potential is obtained,

$$\frac{\partial^2\psi_{sf(i)}(y)}{\partial y^2} - \alpha^2\psi_{sf(i)}(y) = \beta_{(i)} \tag{3.4}$$

with

$$\alpha^2 = \eta\,\frac{C_{ox}}{t_{si}^2C_{si}}\left(2 + \frac{C_{ox}}{C_{si}}\right)$$

$$\beta_{(i)} = \eta\,\frac{qN_{Ch}}{2\epsilon_{si}}\left(2 + \frac{C_{ox}}{C_{si}}\right) - \alpha^2V'_{GS(i)}$$

where, C_{ox} and C_{si} are oxide capacitance and silicon film capacitance respectively calculated as

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}\,, \qquad C_{si} = \frac{\epsilon_{si}}{t_{si}}$$

The solution of (3.4) for channel region under $M1$, $M2$ and $M3$ can be ex-

pressed as,

$$\psi_{sf1}(y) = A_1 \exp(\alpha y) + B_1 \exp(-\alpha y) - \frac{\beta_1}{\alpha^2}, \qquad 0 \le y \le L_1 \tag{3.5}$$

$$\psi_{sf2}(y) = A_2 \exp(\alpha y) + B_2 \exp(-\alpha y) - \frac{\beta_2}{\alpha^2}, \qquad L_1 \le y \le L_2 \tag{3.6}$$

$$\psi_{sf3}(y) = A_3 \exp(\alpha y) + B_3 \exp(-\alpha y) - \frac{\beta_3}{\alpha^2}, \qquad L_2 \le y \le L_3 \tag{3.7}$$

To determine the values of A_1, B_1, A_2, B_2, A_3, and B_3 the following boundary conditions are applied at source edge, drain edge of the channel and at the point where the metals contact with each other:

$$\psi_{sf1}(0) = -\frac{KT}{q} \ln \frac{N_{source}}{N_{Ch}} = -V_{bi} \tag{3.8}$$

$$\psi_{sf3}(L) = \frac{KT}{q} \ln \frac{N_{drain}}{N_{Ch}} + V_{DS} = V'_{bi} + V_{DS} \tag{3.9}$$

$$\psi_{sf1}(L_1) = \psi_{sf2}(L_1) \tag{3.10}$$

$$\psi_{sf2}(L_1 + L_2) = \psi_{sf3}(L_1 + L_2) \tag{3.11}$$

$$\frac{\partial \psi_{sf1}(L_1)}{\partial y} = \frac{\partial \psi_{sf2}(L_1)}{\partial y} \tag{3.12}$$

$$\frac{\partial \psi_{sf1}(L_1 + L_2)}{\partial y} = \frac{\partial \psi_{sf2}(L_1 + L_2)}{\partial y} \tag{3.13}$$

The first two boundary conditions ensure that potential at source and drain interface of the channel will be equal to the Fermi level of source and drain region respectively. The remaining boundary conditions ensure the continuity of potential and electric displacement at the points where the metals contact. The constants

of (3.5), (3.6) and (3.7) are obtained as,

$$A_1 = \frac{\sigma_1 - \sigma_2 exp(-\alpha L) - \gamma}{2sinh(\alpha L)}$$

$$B_1 = \frac{-\sigma_1 + \sigma_2 exp(\alpha L) + \gamma}{2sinh(\alpha L)}$$

$$A_2 = A_1 + \frac{\Delta V_{FB}}{2exp(\alpha L_1)}$$

$$B_2 = B_1 + \frac{\Delta V_{FB}}{2exp(-\alpha L_1)}$$

$$A_3 = A_2 + \frac{\Delta V'_{FB}}{2exp(\alpha L')}$$

$$B_3 = B_2 + \frac{\Delta V'_{FB}}{2exp(-\alpha L')}$$

where,

$$L' = L_1 + L_2$$

$$\sigma_1 = V'_{bi} + V_{DS} + \frac{\beta_3}{\alpha^2}, \quad \sigma_2 = \frac{\beta_1}{\alpha^2} - V_{bi}$$

$$\Delta V_{FB} = V_{FB2} - V_{FB1}, \quad \Delta V'_{FB} = V_{FB3} - V_{FB2}$$

$$\gamma = \Delta V_{FB} cosh(\alpha(L - L_1)) + \Delta V'_{FB} cosh(\alpha(L - L'))$$

Replacing the values of the constants in (3.5), (3.6) and (3.7) the surface potential under three metal gates can be found.

The derived analytical model of $\psi_{sf(i)}$ can be used for dual material double gate TFETs [74] by considering either $\phi_{m1} = \phi_{m2}$ or $\phi_{m2} = \phi_{m3}$. If we consider $\phi_{m1} = \phi_{m2} = \phi_{m3}$ in the derived model of $\psi_{sf(i)}$, the model reduces to the surface potential model of single material gate TFETs [75]. Therefore, this surface po-

tential model can be used as a generalized model for single and multiple material gate TFET structures.

3.2.2 2D Potential Model

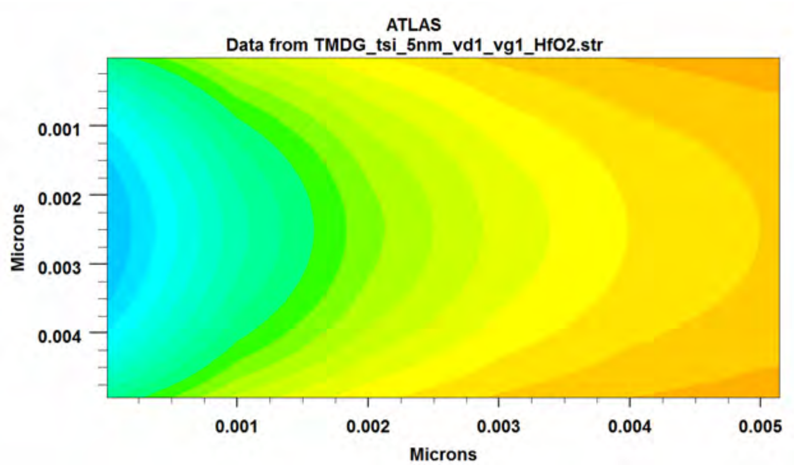

Fig. 3.2: Electric potential distribution in TMDG TFET.

Electric potential profile of TMDG TFET is shown in Fig. 3.2 during ON-state. The potential profile is parabolic and therefore, the two-dimensional potential is assumed to be a second-order polynomial [76], i.e.,

$$\psi_1(y,x) = \psi_{sf1}(y) + C_1(y)x + D_1(y)x^2 \,, \qquad 0 \le y \le L_1 \tag{3.14}$$

$$\psi_2(y,x) = \psi_{sf2}(y) + C_2(y)x + D_2(y)x^2 \,, \qquad L_1 \le y \le L_2 \tag{3.15}$$

$$\psi_3(y,x) = \psi_{sf3}(y) + C_3(y)x + D_3(y)x^2 \,, \qquad L_2 \le y \le L_3 \tag{3.16}$$

In the channel, the following boundary conditions at the top and bottom oxide

interface can be applied to find the value of $C_i(y)$ and $D_i(y)$ [$i = 1, 2,$ and 3].

$$\left.\frac{\partial\psi_1(y,x)}{\partial x}\right|_{x=0} = \frac{C_{ox}}{\epsilon_{Si}}[\psi_{sf1}(y) - V'_{GS1}] \tag{3.17}$$

$$\left.\frac{\partial\psi_2(y,x)}{\partial x}\right|_{x=0} = \frac{C_{ox}}{\epsilon_{Si}}[\psi_{sf2}(y) - V'_{GS2}] \tag{3.18}$$

$$\left.\frac{\partial\psi_3(y,x)}{\partial x}\right|_{x=0} = \frac{C_{ox}}{\epsilon_{Si}}[\psi_{sf3}(y) - V'_{GS3}] \tag{3.19}$$

$$\left.\frac{\partial\psi_1(y,x)}{\partial x}\right|_{x=t_{Si}} = -\frac{C_{ox}}{\epsilon_{Si}}[\psi_{sf1}(y) - V'_{GS1}] \tag{3.20}$$

$$\left.\frac{\partial\psi_2(y,x)}{\partial x}\right|_{x=t_{Si}} = -\frac{C_{ox}}{\epsilon_{Si}}[\psi_{sf2}(y) - V'_{GS2}] \tag{3.21}$$

$$\left.\frac{\partial\psi_3(y,x)}{\partial x}\right|_{x=t_{Si}} = -\frac{C_{ox}}{\epsilon_{Si}}[\psi_{sf3}(y) - V'_{GS3}] \tag{3.22}$$

The values of $C_i(y)$ and $D_i(y)$ are obtained as

$$C_1(y) = \frac{C_{ox}}{\epsilon_{Si}}[\psi_{sf1}(y) - V'_{GS1}]$$
$$C_2(y) = \frac{C_{ox}}{\epsilon_{Si}}[\psi_{sf2}(y) - V'_{GS2}]$$
$$C_3(y) = \frac{C_{ox}}{\epsilon_{Si}}[\psi_{sf3}(y) - V'_{GS3}]$$

$$D_1(y) = -\frac{C_{ox}}{\epsilon_{Si}t_{Si}}[\psi_{sf1}(y) - V'_{GS1}]$$
$$D_2(y) = -\frac{C_{ox}}{\epsilon_{Si}t_{Si}}[\psi_{sf2}(y) - V'_{GS2}]$$
$$D_3(y) = -\frac{C_{ox}}{\epsilon_{Si}t_{Si}}[\psi_{sf3}(y) - V'_{GS3}]$$

3.3 Electric Field

Electric field is defined as the electric force per unit charge. The electric-field distribution along the channel length can be obtained by differentiating the surface potential. The lateral electric field can be written as,

$$E_{y1}(y) = -\left.\frac{\partial \psi_1(y,x)}{\partial y}\right|_{x=0} = -\alpha[A_1 \exp(\alpha y) - B_1 \exp(-\alpha y)]\,,\ \ 0 \le y \le L_1 \tag{3.23}$$

$$E_{y2}(y) = -\left.\frac{\partial \psi_2(y,x)}{\partial y}\right|_{x=0} = -\alpha[A_2 \exp(\alpha y) - B_2 \exp(-\alpha y)]\,,\ \ L_1 \le y \le L_2 \tag{3.24}$$

$$E_{y3}(y) = -\left.\frac{\partial \psi_3(y,x)}{\partial y}\right|_{x=0} = -\alpha[A_3 \exp(\alpha y) - B_3 \exp(-\alpha y)]\,,\ \ L_2 \le y \le L_3 \tag{3.25}$$

The vertical electric field can be written as,

$$E_{x1}(y) = -\frac{\partial \psi_1(y,x)}{\partial x} = -[C_1(y) + 2xD_1(y)]\,, \qquad 0 \le y \le L_1 \tag{3.26}$$

$$E_{x2}(y) = -\frac{\partial \psi_2(y,x)}{\partial x} = -[C_2(y) + 2xD_2(y)]\,, \qquad L_1 \le y \le L_2 \tag{3.27}$$

$$E_{x3}(y) = -\frac{\partial \psi_3(y,x)}{\partial x} = -[C_3(y) + 2xD_3(y)]\,, \qquad L_2 \le y \le L_3 \tag{3.28}$$

3.4 Drain Current: Band-to-Band Tunneling Current

TFET is a reverse biased p-i-n diode and the current is small if no BTBT is present, in which case the current is referred as the off-current. As soon as BTBT occurs, the resulting on-current will dominantly exceed the off-current. In semi-classical simulators, BTBT is modeled by the introduction of an extra generation term (G) in the drift-diffusion equation. When the BTBT current contribution is dominant, the TFET current can be computed as the sum over all charge generated in the device:

$$I_{DS} = q \int G \, \mathrm{d}V$$

with $\mathrm{d}V$ an elementary volume in the device and G the generation rate expressed in number of carriers per unit volume per unit time. The tunneling current per unit width can be calculated as

$$I_{DS} = q \iint G \, \mathrm{d}x\mathrm{d}y \tag{3.29}$$

The most popular model to calculate the generation rate is Kane's Model [77, 78], which determines the BTBT generation rate of carrier tunneling from the valence band of the source to the conduction band of the channel, as

$$G = A_k \, E^D \, exp\left(-\frac{B_k}{E}\right) \tag{3.30}$$

where E is the local electric field; D is 2.5 for the indirect and 2 for the direct tunneling processes; A_k and B_k are the tunneling process-dependent parameters.

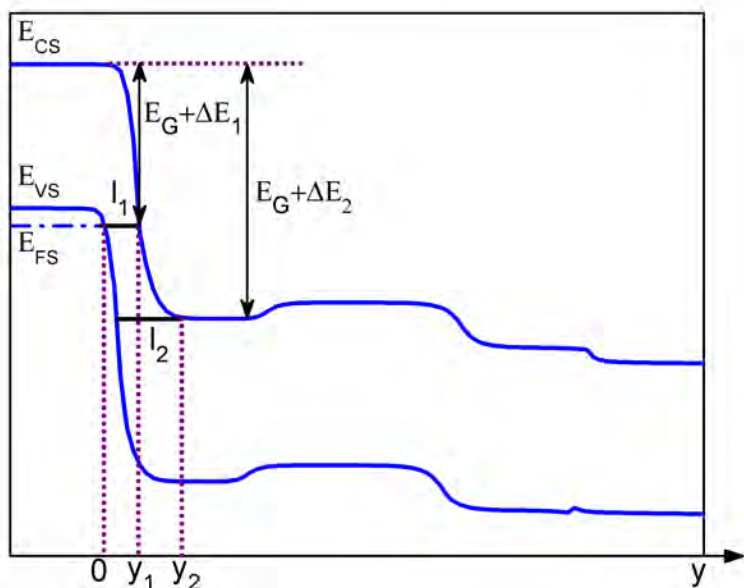

Fig. 3.3: Tunnel path between the valence band of the source and the conduction band of the channel region.

In this work, silicon based TMDG TFETs are considered, hence $D = 2.5$ is used. Although analytical model for indirect tunneling process is developed, it can be easily extended to the direct tunneling process and the drain current can be computed as [79]

$$I_{DS} = q \iint A_k\, E\, E_{avg}^{D-1}\, exp\left(-\frac{B_k}{E_{avg}}\right)\, \mathrm{d}x\, \mathrm{d}y \tag{3.31}$$

Here, E_{avg} is the average electric field and can be calculated as

$$E_{avg} = \frac{E_g}{q l_{path}}$$

l_{path} is the tunneling path which varies from l_1 to l_2 as shown in Fig. 3.3. Due to high doping concentration, the source depletion region can be ignored [80], therefore $l_1 = y_1$ and $l_2 = y_2$. At $y = y_1$, the difference between the

source conduction band and channel conduction band is $E_g + \Delta E_1$, where $\Delta E_1 = E_{VS} - E_{FS}$. ΔE_1 can be calculated by using Joyce and Dixon approximation [81]

$$\Delta E_1 = kT\left[ln(z) + \frac{1}{\sqrt{8}}z - \left(\frac{3}{16} - \frac{1}{\sqrt{27}}\right)z^2 + \left(\frac{1}{8} + \frac{5}{24\sqrt{2}} - \frac{\sqrt{2}}{3\sqrt{3}}\right)z^3 - \cdots\right] \tag{3.32}$$

here, $z = N_{source}/N_v$. N_v is the effective density of state of source valence band.

At $y = y_2$, the difference between the source conduction band and channel conduction band reaches $E_g + \Delta E_2$, where, $E_g + \Delta E_2 = E_{VS} - E_{VC}$ and $\Delta E_2 = V_{bi}$ [30].

The value of y_1 can be calculated by equating the potential at $y = y_1$ with $(E_g + \Delta E_1)/q$.

$$\psi_{sf1}(y)\bigg|_{y=y_1} = \frac{E_g + \Delta E_1}{q}$$

Using (3.5) and neglecting higher order terms, y_1 can be calculated as

$$y_1 = \left[\frac{E_g + \Delta E_1}{q} - (A_1 + B_1 - \beta_1/\alpha^2)\right]\bigg/\bigg[\alpha(A_1 - B_1)\bigg] \tag{3.33}$$

Similarly, to find the value of y_2, the potential at $y = y_2$ is equated to $(E_g + \Delta E_2)/q$.

$$\psi_{sf1}(y)\bigg|_{y=y_2} = \frac{E_g + \Delta E_2}{q}$$

Using (3.5) and neglecting higher order terms, y_2 is obtained as

$$y_2 = \left[\frac{E_g + \Delta E_2}{q} - (A_1 + B_1 - \beta_1/\alpha^2)\right]\bigg/\bigg[\alpha(A_1 - B_1)\bigg] \tag{3.34}$$

The tunneling window to tunnel the carrier across the junctions can be found

by setting the limit of integration to y_1 and y_2 [82]. The tunneling current can be calculated as,

$$I_{DS} = \frac{A_k E_G^{D-1}}{q^{D-2}} \int_{x=0}^{x=t_{Si}} \int_{y=y_1}^{y=y_2} \frac{E}{y^{D-1}} exp\left(-\frac{B_k q}{E_g} y\right) \, \mathrm{d}x \, \mathrm{d}y \tag{3.35}$$

The local electric field, $E = \sqrt{E_x^2 + E_y^2}$. For well scaled devices, the dominant tunneling paths are lateral and it is reasonable to assume that tunneling primarily takes place along the channel length direction [83]. Therefore, only lateral field can be taken into account in the calculation of tunneling current. Besides, the tunneling path exists only under $M1$, hence we can consider $E_{y1}(y)$ from (3.23) in the resultant expression of E.

In (3.35), y ranges from y_1 to y_2, in this interval variation of the exponential term is dominant compared with polynomial term y^{D-1} [79]. Therefore, integration is performed over the exponential term to compute the drain current. After considering several simplification and ignoring higher order terms, the analytical expression of drain current can be formulated as

$$I_{DS} = \frac{A_k E_G^D}{B_k q^{D-2}} t_{Si} \left[N(y_1)M(y_1) - N(y_2)M(y_2) - \frac{E_G}{B_k} \alpha^2 (A_1 + B_1)(M(y_1) - M(y_2)) \right] \tag{3.36}$$

where $M(y)$ and $N(y)$ are defined as

$$M(y) = \frac{exp\left(-\frac{B_k q}{E_g} y\right)}{y^{D-1}}$$

$$N(y) = \alpha(A_1 - B_1) + \alpha^2 (A_1 + B_1) y$$

3.5 Gate Threshold Voltage

3.5.1 Definition of V_{TH} for TMDG TFET

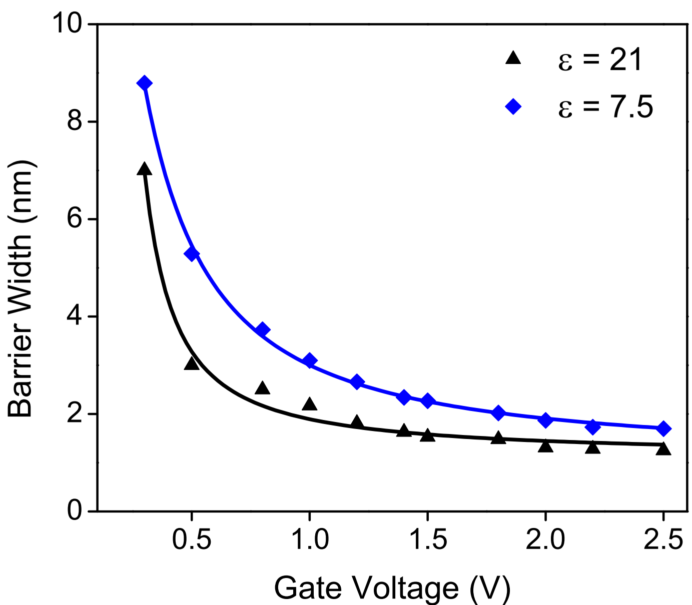

Fig. 3.4: Variation of energy barrier width with applied gate bias for $\epsilon_{ox} = 21, 7.5$ at $V_{DS} = 1V$.

Although the physics determining the current flow inside a Tunnel FET is not the same as in a conventional MOSFET, the switching behavior of two devices is similar enough that it is tempting to analyze a Tunnel FET as if it were a MOSFET. Most typical CMOS benchmarking parameters are equally applicable to a Tunnel FET, so there is no problem when looking at OFF-current, ON-current, I_{ON}/I_{OFF} ratio, transconductance, gate leakage, etc. There is one parameter, however, that is more connected to the nanoscale physics processes going on inside the device: the threshold voltage, V_{TH}.

The V_{TH} is one of the most important electrical parameters of a solid-state

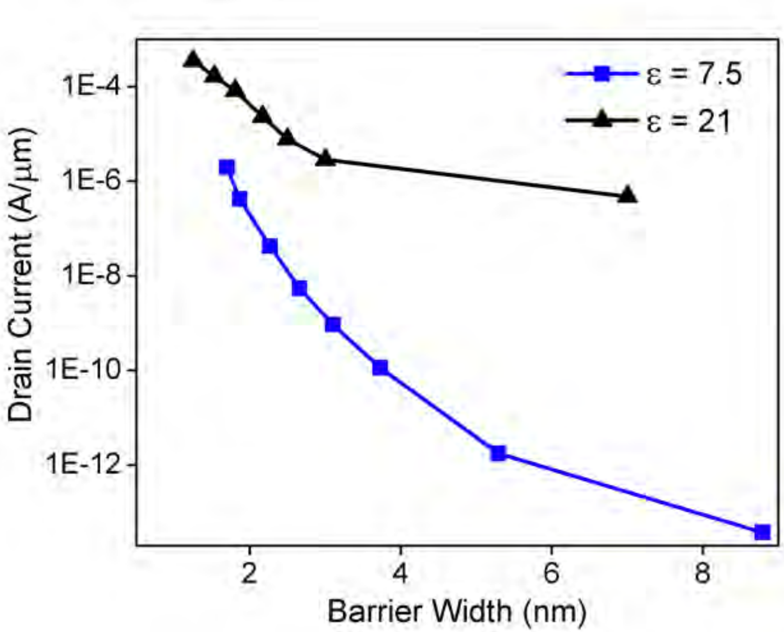

Fig. 3.5: Drain current vs. energy barrier width, w_b for different values of the gate dielectric permittivity at $V_{DS} = 1V$.

switch. Constant current method had been used to extract threshold voltage for TFETs due to its simplicity and independence from the accuracy of a drain current model [84–86]. Unfortunately, this method uses an arbitrary current value ($I_D = 10^{-7}A/\mu m$) and has almost no physical meaning, despite its practical interest.

The tunneling current of TFET can be controlled by modulating the energy barrier width, w_b. Modulation of w_b can be controlled by the applied gate voltage which is shown in Fig. 3.4. Here, energy bands across the TFET body are considered and the narrowest barrier width on those bands at source side is measured to extract the values of w_b. Due to exponential dependence of tunneling probability on barrier width, this technique works well when the applied voltage is above several hundred mV. Fig. 3.5 shows the dependence of ON-current on w_b in TFETs for two different gate dielectric materials. From Fig. 3.5, it is evident that when

constant current method is applied, the V_{TH} corresponds to a w_b of 7nm for $\epsilon = 21$ at $V_{DS} = 1V$, which is still in the region of a strong dependence of the barrier on the gate voltage [Fig. 3.4]. This technique for extracting a threshold voltage is not based on a physical transition inside the device – it is arbitrary. Therefore, a new definition of V_{TH} is suggested in [87]:

The Tunnel FET threshold voltage is the voltage marking the transition between an exponential dependence, and a linear dependence, of drain current on applied bias. This also marks the transition between the strong control and weak control of the tunneling energy barrier width at the tunnel junction by that voltage.

This new technique uses the second derivative of the $I_D - V_{GS}$ characteristics to find the transition point on the curve, hence V_{TH}. Beyond its physical meaning, this extraction method has the advantage that it does not depend upon the accuracy of a particular analytical model, but rather can be extracted directly from experimental data. The details of the technique will be explained in section 4.5.

3.5.2 V_{TH} Modeling

Tunneling barrier width exhibits a transition from strong dependence to weak dependence on gate voltage at gate threshold voltage. At this inflection point, $y = w_b$ and

$$\psi_{sf1}(y) = V_{DS} + \frac{kT}{q} \ln \frac{N_{drain}}{N_{Ch}}$$

The threshold voltage of TMDG TFET can be modeled by substituting these values into (3.5).

$$V_{TH} = \rho + \frac{(V'_{bi} + V_{DS})(1 - \Theta_1) - V_{bi}\Theta_2 - \gamma}{1 - \Theta_1 + \Theta_2} + \frac{V_{FB3} - V_{FB1}(\Theta_1 - \Theta_2)}{1 - \Theta_1 + \Theta_2} \quad (3.37)$$

where,

$$\rho = \frac{qN_{ch}t_{si}}{2C_{ox}}$$

$$\Theta_1 = \frac{sinh(\alpha L)}{sinh(\alpha w_b)}$$

$$\Theta_2 = \frac{sinh(\alpha(L - w_b))}{sinh(\alpha w_b)}$$

If we consider $\phi_{m1} = \phi_{m2} = \phi_{m3}$ in the derived model of V_{TH}, the model reduces to the threshold voltage model of single material gate TFETs [75]. This model can also be modified for double material gate TFETs by considering either $\phi_{m1} = \phi_{m2}$ or $\phi_{m2} = \phi_{m3}$ [88]. Therefore, this threshold voltage model can be used as a generalized model.

Chapter 4

Numerical Model of TMDG TFET

4.1 Introduction

Numerical modeling is a powerful method to assess the device characteristics. It provides a way to visualize dynamic behavior of a physical system by establishing a set of mathematical equations. With increasing complexity like this work of TMDG TFET, the number of equations may get very large than expected. For TMDG TFETs, numerical modeling will be time consuming but they come up with greater accuracy. In this work, Silvaco ATLAS 2012 [63] has been used to simulate the numerical model of TMDG TFET structure. At the beginning of this section, a brief overview of the simulation tool is presented. The considerations during defining the TMDG TFET device structure, the models included during simulation and methods of interpreting the simulation results are exhibited in the following section. Later, the extraction method of tunneling parameters from the available experimental data is described. Finally, the method used for extracting threshold voltage from the TCAD simulation results are explained.

4.2 Overview of Silvaco Atlas

ATLAS is a physically-based two and three dimensional device simulator. It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation. This is achieved by approximating the operation of a device onto a two or three dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, onto this grid one can simulate the transport of carriers through a structure. This means that the electrical performance of a device can be modeled in DC, AC or transient modes of operation.

Physically-based simulation has become very important for two reasons. One, it is almost always much quicker and cheaper than performing experiments. Two, it provides information that is difficult or impossible to measure. The drawbacks of physically-based simulation are that all the relevant physics must be incorporated into a simulator. Also, numerical procedures must be implemented to solve the associated equations.

ATLAS is best used with the VWF INTERACTIVE TOOLS which include DECKBUILD, TONYPLOT, and other tools. DECKBUILD provides an interactive run time environment. TONYPLOT supplies scientific visualization capabilities. For using physically-based device simulation tools one must specify the problem to be simulated. In ATLAS, device simulation problems are specified by defining:

- The physical structure to be simulated.
- The physical models to be used.

- The bias conditions for which electrical characteristics are to be simulated.

4.3 Numerical Simulation

The order in which statements occur in an ATLAS input file is important. There are five groups of statements that must occur in the correct order. Otherwise, an error message will appear, which may cause incorrect operation or termination of the program. The group of statements are:

- Structure Specification.
- Material Models Specification.
- Numerical Method Selection.
- Solution Specification.
- Results Analysis.

The order of statements within the mesh definition, structural definition, and solution groups is also important. Otherwise, it may also cause incorrect operation or termination of the program.

4.3.1 Defining The Structure

To define a device through the ATLAS command language, one must first define a mesh. This mesh or grid covers the physical simulation domain. The mesh is defined by a series of horizontal and vertical lines and the spacing between them. Then, regions within this mesh are allocated to different materials as required to

construct the device. After the regions are defined, the location of electrodes is specified. The final step is to specify the doping in each region.

Specifying a good grid is a crucial issue in device simulation but there is a trade-off between the requirements of accuracy and numerical efficiency. Accuracy requires a fine grid that resolves the structure in solutions. Numerical efficiency is greater when fewer grid points are used. Therefore, the most efficient way is to allocate a fine grid only in critical areas and a coarser grid elsewhere. The three most important factors to look for in any grid are:

- Ensure adequate mesh density in high field areas.
- Avoid obtuse triangles in the current path or high field areas.
- Avoid abrupt discontinuities in mesh density.

Fig. 4.1 shows the device structure developed using ATLAS and Fig. 4.2 shows the meshing across the device. A very fine mesh is considered near the tunneling junction.

4.3.2 Defining Material Parameters and Models

Once the mesh, geometry, and doping profiles are defined, one can modify the characteristics of electrodes, change the default material parameters, and choose which physical models ATLAS will use during the device simulation. To accomplish these actions, CONTACT, MATERIAL, and MODELS statements are used respectively.

An electrode in contact with semiconductor material is assumed by default to be ohmic. If a workfunction is defined, the electrode is treated as a Schottky

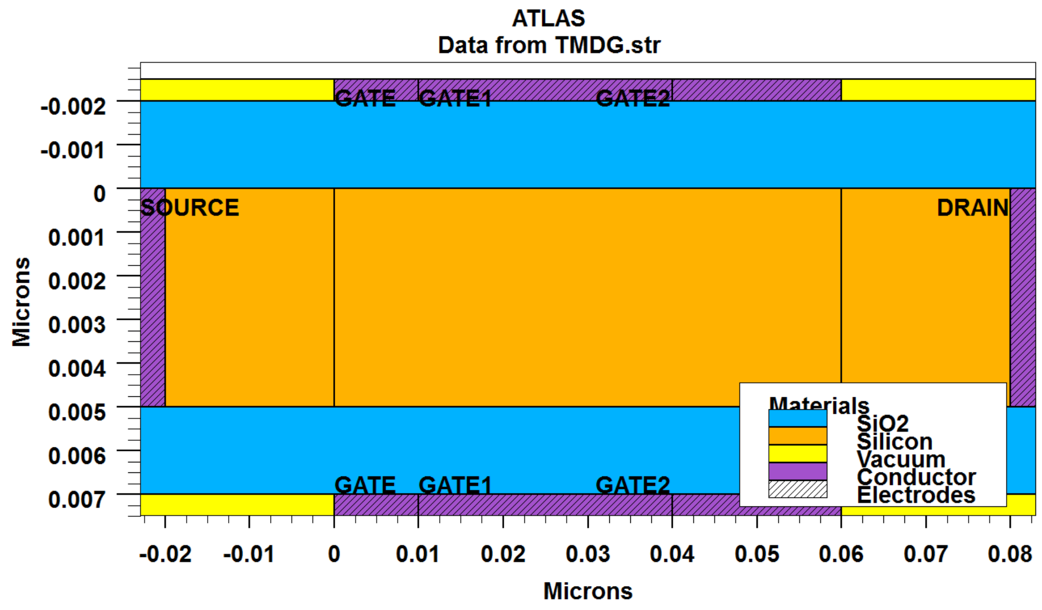

Fig. 4.1: TMDG TFET structure created using ATLAS device simulator.

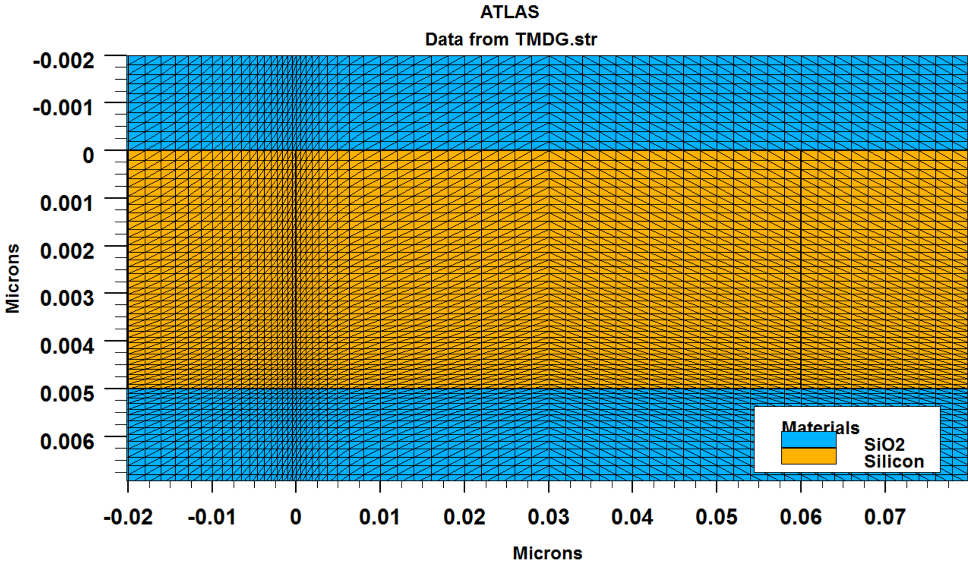

Fig. 4.2: TMDG TFET structure with meshing.

contact. The CONTACT statement is used to specify the metal workfunction of one or more electrodes. The NAME parameter is used to identify which electrode will have its properties modified.

All materials are split into three classes: semiconductors, insulators and conductors. Each class requires a different set of parameters to be specified. For semiconductors, these properties include electron affinity, band gap, density of states and saturation velocities. There are default parameters for material properties used in device simulation for many materials. The MATERIAL statement allows one to specify its own values for these basic parameters. Specified values can apply to a specified material or a specified region.

Physical models are specified using the MODELS statement. The physical models can be grouped into five classes: mobility, recombination, carrier statistics, impact ionization, and tunneling. The models used in this work are:

- **Fermi-Dirac (FERMI)**

  Electrons in thermal equilibrium at temperature T_L with a semiconductor lattice obey Fermi-Dirac statistics. That is the probability $f(\varepsilon)$ that an available electron state with energy ε is occupied by an electron is:

  $$f(\varepsilon) = \frac{1}{1 + exp\left(\frac{\varepsilon - E_F}{kT_L}\right)}$$

  where E_F is a spatially independent reference energy known as the Fermi level and k is Boltzmann's constant. Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials.

- **Bandgap Narrowing (BGN)**

  In the presence of heavy doping, greater than $10^{18} cm^{-3}$, experimental work has shown that the pn product in silicon becomes doping dependent [64]. As the doping level increases, a decrease in the bandgap separation occurs, where the conduction band is lowered by approximately the same amount as the valence band is raised. In ATLAS, this is simulated by a spatially varying intrinsic concentration. Bandgap narrowing effects in ATLAS are enabled by specifying the BGN parameter of the MODELS statement.

- **Parallel Electric Field Dependence (FLDMOB)**

  As carriers are accelerated in an electric field their velocity will begin to saturate when the electric field magnitude becomes significant. This effect has to be accounted for by a reduction of the effective mobility since the magnitude of the drift velocity is the product of the mobility and the electric field component in the direction of the current flow. Caughey and Thomas Expression [65] is used to implement a field-dependent mobility. This provides a smooth transition between low-field and high field behavior. Specifying the FLDMOB parameter on the MODELS statement invokes the field-dependent mobility. FLDMOB should always be specified unless one of the inversion layer mobility models are specified.

- **Shockley-Read-Hall Recombination (SRH)**

  Phonon transitions occur in the presence of a trap (or defect) within the forbidden gap of the semiconductor. This is essentially a two step process, the theory of which was first derived by Shockley and Read [66] and then by Hall [67].

- **Concentration Dependent Lifetime SRH (CONSRH)**

  The constant carrier lifetimes that are used in the SRH recombination model can be made a function of impurity concentration. This model is activated with the CONSRH parameter of the MODELS statement.

- **Auger's Recombination Model (AUGER)**

  Auger recombination occurs through a three particle transition whereby a mobile carrier is either captured or emitted. The underlying physics for such processes is unclear and normally a more qualitative understanding is sufficient [68].

- **Kane's Band-to-Band Tunneling Model (BBT.KANE)**

  If a sufficiently high electric field exists within a device local band bending may be sufficient to allow electrons to tunnel, by internal field emission, from the valence band into the conduction band. An additional electron is therefore generated in the conduction band and a hole in the valence band. Kane's model is used during the formulation of analytical model, therefore, it is also used in developing the numerical model. To enable this model BBT.KANE on the MODELS statement is specified.

4.3.3 Selecting Numerical Methods

Several different numerical methods can be used for calculating the solutions to semiconductor device problems. Different combinations of models will require ATLAS to solve up to six equations. For each of the model types, there are basically three types of solution techniques:

- decoupled (GUMMEL),

- fully coupled (NEWTON) and
- BLOCK

The GUMMEL method will solve for each unknown in turn keeping the other variables constant, repeating the process until a stable solution is achieved. The NEWTON method solve the total system of unknowns together. Generally, the GUMMEL method is useful where the system of equations is weakly coupled but has only linear convergence. The NEWTON method is useful when the system of equations is strongly coupled and has quadratic convergence. The NEWTON method may, however, spend extra time solving for quantities, which are essentially constant or weakly coupled. NEWTON also requires a more accurate initial guess to the problem to obtain convergence. GUMMEL can often provide better initial guesses to problems. It can be useful to start a solution with a few GUMMEL iterations to generate a better guess. Then, switch to NEWTON to complete the solution. This approach is used in this work.

4.3.4 Obtaining Solutions

ATLAS can calculate DC, AC small signal, and transient solutions. Obtaining solutions is similar to setting up parametric test equipment for device tests. Usually the voltages on each of the electrodes in the device need to be defined. ATLAS then calculates the current through each electrode. ATLAS also calculates internal quantities, such as carrier concentrations and electric fields throughout the device.

In all simulations, the device starts with zero bias on all electrodes. Solutions are obtained by stepping the biases on electrodes from this initial equilibrium condition. Due to the initial guess strategy, voltage step sizes are limited. In DC

solutions, the voltage on each electrode is specified using the SOLVE statement. When the voltage on a particular electrode is never defined on any SOLVE statement and voltage is considered zero.

To obtain convergence for the equations used, a good initial guess need to be supplied for the variables to be evaluated at each bias point. The ATLAS solver uses this initial guess and iterates to a converged solution. If a reasonable grid is used, almost all convergence problems in ATLAS are caused by a poor initial guess to the solution. During a bias ramp, the initial guess for any bias point is provided by a projection of the two previous results. Problems tend to appear near the beginning of the ramp when two previous results are not available. If one previous bias is available, it is used alone. Generally, coupled solutions require a good initial guess, whereas decoupled solutions can converge with a poor initial guess.

4.3.5 Result Interpretation

ATLAS produces three different types of output files:

- **Run-Time Output**

  Run-time output is provided at the bottom of the DeckBuild Window. If it is run as a batch job, the run-time output can be stored to a file.

- **Log Files**

  Log files store the terminal characteristics calculated by ATLAS. These are current and voltages for each electrode in DC simulations. In transient simulations, the time is stored. In AC simulations, the small signal frequency and the conductances and capacitances are saved. Log files contain only the

terminal characteristics. They are typically viewed in TONYPLOT.

- **Solution Files**

  Solution files or structure files provide an image of the device at a particular bias point (DC solution or transient solution point). This provides the ability to view any evaluated quantity within the device structure in question, from doping profiles and band parameters to electron concentrations and electric fields. These files are plotted using TONYPLOT.

4.4 Extraction of Tunneling Parameters

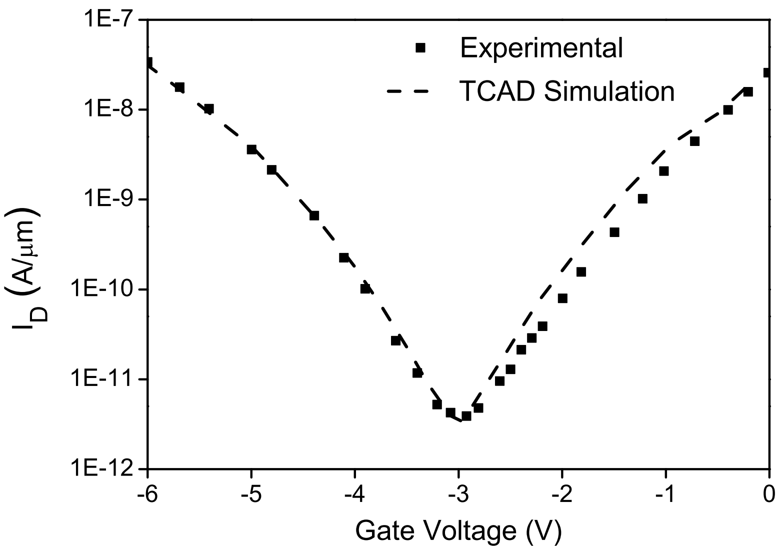

Fig. 4.3: Reproduction of experimental result from [69].

Kane's band-to-band tunneling model uses two tunneling parameters: A_{kane} and B_{kane}. Since no experimental data is available for TMDG TFET structure, these tunneling parameters are calibrated by accurately reproducing the experi-

mental results published in [69]. Fig. 4.3 compares the experimental data and the TCAD simulation results. The values of the extracted parameters are $A_{kane} = 4 \times 10^{19} eV^{1/2}/cm.s.V^2$ and $B_{kane} = 41 MV/cm.eV^{3/2}$.

4.5 Extraction of Threshold Voltage

Transconductance Change (TC) method, widely used for non-linear device [70], has been used to extract the value of threshold voltage, V_{TH} from TCAD simulation results. In this method, V_{TH} is the gate voltage corresponding to the maximum of transconductance derivative, dg_m/dV_{GS}. This method can locate the voltage which indicates a transition between strong and weak control of tunneling barrier width.

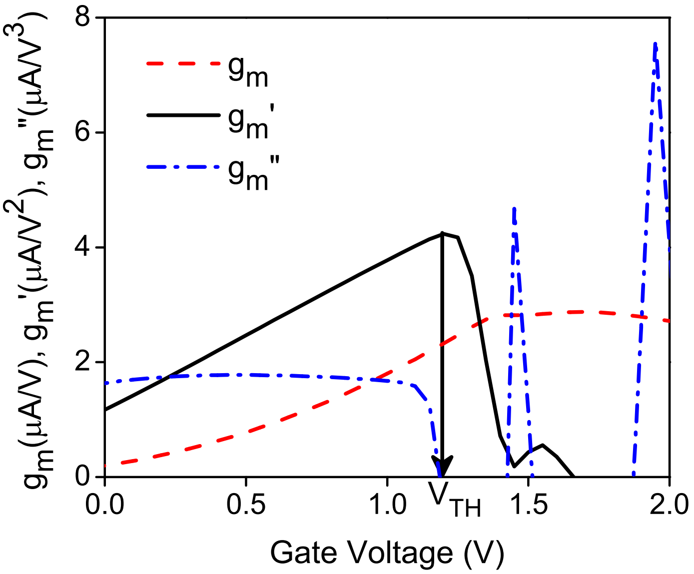

Fig. 4.4: Extraction of V_{TH} using TC method.

Fig. 4.4 shows the 1st order (g_m), 2nd order (g'_m) and 3rd order derivatives (g''_m) of drain current for La_2O_3 dielectric at $V_{DS} = 1V$. At $V_{GS} = 1.18V$, a peak point in the g'_m curve and an inflection point in the g_m curve occurs representing the transition point between quasi-exponential dependence and linear dependence of I_D on V_{GS}. This transition point corresponds to the threshold voltage. It is worth noting that this voltage also corresponds to the zero of the third derivative. This derivative plot contained much numerical derivative noise, which makes its practical use quite impossible. In this work, an extremely simple curve de-noising method has been used where,

$$dg_{i,de-noised} = \frac{dg_{i-1} + 2dg_i + dg_{i+1}}{4} \tag{4.1}$$

Chapter 5

Results and Discussion

5.1 Introduction

This chapter shows the effects of physical parameter variation on potential, electric field, drain current and threshold voltage. The modulation of these electrical characteristics under different biasing conditions are also analyzed here. The results from analytical model are compared with TCAD simultion results to validate the proposed models. In the last section, dependence of band-to-band tunneling current on Si film thickness and the physics governing it is detailed. Finally, an optimum Si film thickness for TMDG TFET structure is suggested based on its effect on electrical parameters.

5.2 Device parameter

The TMDG TFET considered in this study has source doping of $N_{source} = 10^{20} cm^{-3}$, channel doping of $N_{Ch} = 10^{16} cm^{-3}$ and drain doping of $N_{drain} = 10^{19} cm^{-3}$. Us-

ing this type of asymmetrical doping profile, ambipolar effect can be suppressed [89]. The gate length of the device is $L = 60nm$ with $L_1 = 10nm$, $L_2 = 30nm$, and $L_3 = 20nm$ [30]. Three metals $M1$, $M2$, and $M3$ with workfunctions $\phi_{m1} = 4.4eV$ (e.g. W, Ti), $\phi_{m2} = 4.6eV$ (e.g. Mo), and $\phi_{m3} = 4.3eV$ (e.g. Ag) respectively form the gate. The oxide and silicon film thickness are $t_{ox} = 2nm$ and $t_{si} = 5nm$ respectively. The gate dielectrics considered in this study are SiO_2 ($\epsilon_{ox} = 3.9$), Si_3N_4 ($\epsilon_{ox} = 7.5$), HfO_2 ($\epsilon_{ox} = 21$), and La_2O_3 ($\epsilon_{ox} = 27$).

5.3 Analytical Model Validation

5.3.1 Electric Potential

The variation of surface potential along channel length for the proposed model and TCAD simulation is shown in Fig. 5.1. The surface potential is highest under $M3$ as ϕ_{m3} is lowest among the metal gates. Similarly, due to having highest workfunction, surface potential under $M2$ is the lowest. Along the length of the channel under a specific metal gate, potential remains almost constant and varies at the metal junctions. Potential does not abruptly changes to drain Fermi level at the end of lightly doped body; rather it continues to vary at drain-body junction. From Fig. 5.1, it is evident that the proposed model is in good agreement with the simulation results for all biasing conditions except at $V_{GS} = 1.5V$ for which higher degree of deviation is observed. There is slight deviation at source-body and drain-body junctions as depletion regions are not considered during formulating the model. Since the doping concentration in source and drain is very high, the width of the depletion region will be very small. Therefore, the effect of depletion

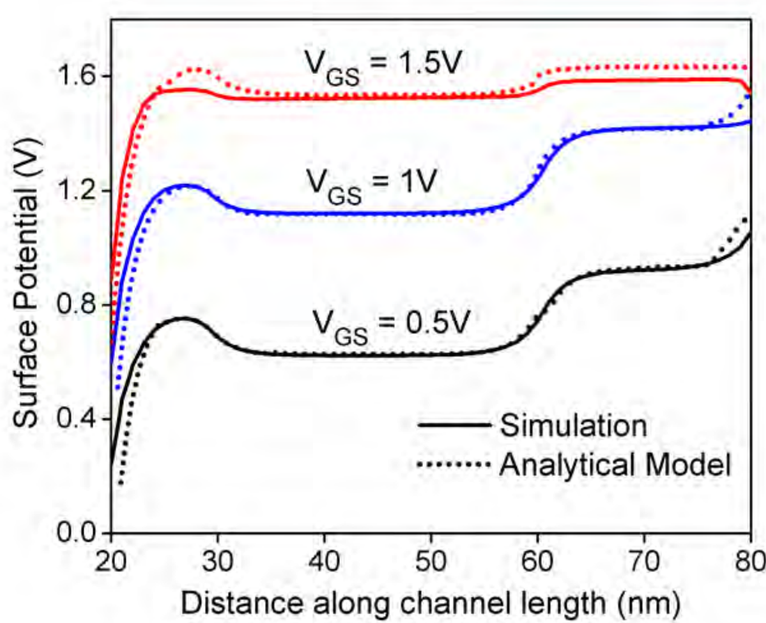

Fig. 5.1: Surface potential along channel length for $V_{GS} = 0.5,\ 1,$ and $1.5V$ with $V_{DS} = 1V$ and $\epsilon_{ox} = 21$. Dotted lines shows the surface potentials from analytical model.

regions are not included.

Fig. 5.2 shows the effect of drain voltage on surface potential. As V_{DS} increases, the potential increases only under the $M3$. Therefore, the tunneling junction which is present at the source side is less affected by the V_{DS} [90].

From Fig. 5.1 it might be predicted that ψ_{sf} increases with increasing gate voltage. On the other hand, Fig. 5.2 predicts that ψ_{sf} under $M1$ is independent of V_{DS}. To verify these predictions, variation of ψ_{sf} under $M1$ with V_{GS} for different V_{DS} are observed. Surface potential at the middle of $M1$ is considered for generating Fig. 5.3. For any particular V_{DS}, surface potential increases with gate voltage upto some specific value of V_{GS}. Beyond that value of V_{GS}, surface potential starts to saturate. V_{GS} at which ψ_{sf} starts to saturate is called inversion

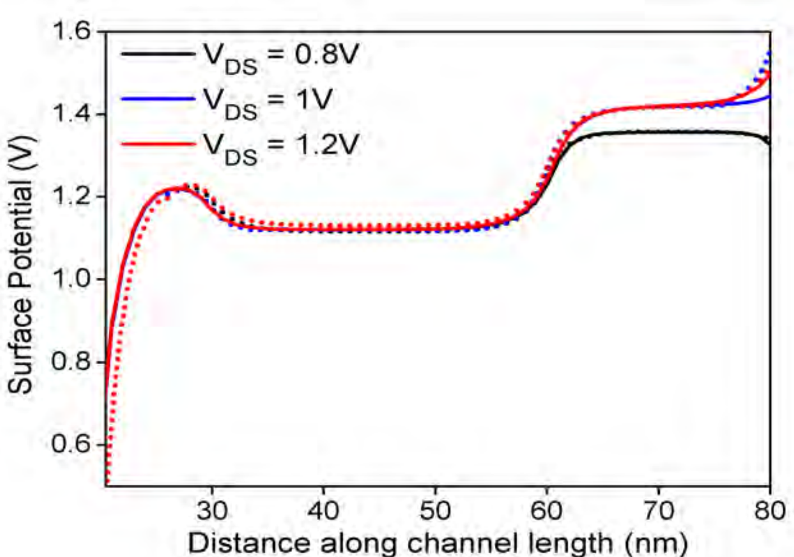

Fig. 5.2: Surface potential along channel length given by analytical model (dotted lines) and TCAD simulations (solid lines) for $V_{DS} = 0.8,\ 1$, and $1.2V$ with $V_{GS} = 1V$ and $\epsilon_{ox} = 21$.

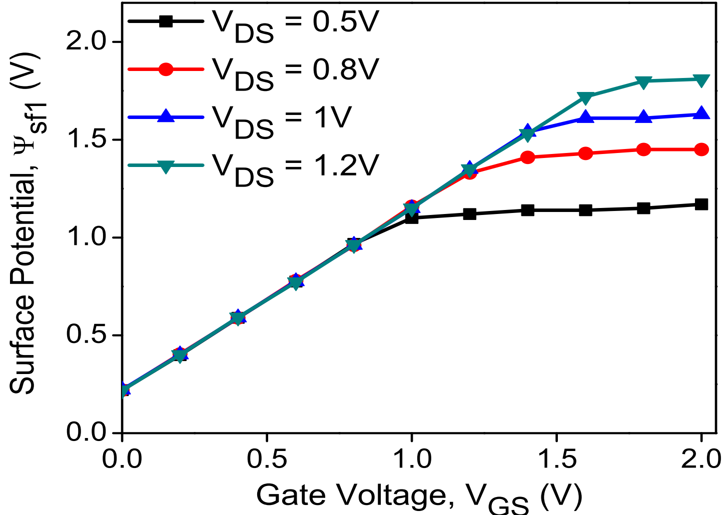

Fig. 5.3: Variation of Surface potential with V_{GS} for $V_{DS} = 0.5,\ 0.8,\ 1$, and $1.2V$ and $\epsilon_{ox} = 21$.

voltage, V_{inv}. Formation of inversion charge layer is the underlying reason for the saturation of ψ_{sf}. Inversion charge layer shields the surface channel from the gate electrode electrically, which can be easily inferred based on MOSFET physics. Due to this saturation effect, analytical model result shows higher deviation from TCAD simulation result for $V_{GS} = 1.5V$. The saturation value of surface potential shifts upward as V_{DS} is increased. It can be concluded that ψ_{sf} is independent of V_{DS} and increases with V_{GS}, if V_{GS} is lower than V_{inv}. When V_{GS} is higher than V_{inv}, ψ_{sf} saturates and becomes dependent on V_{DS}: ψ_{sf} increases as V_{DS} increases.

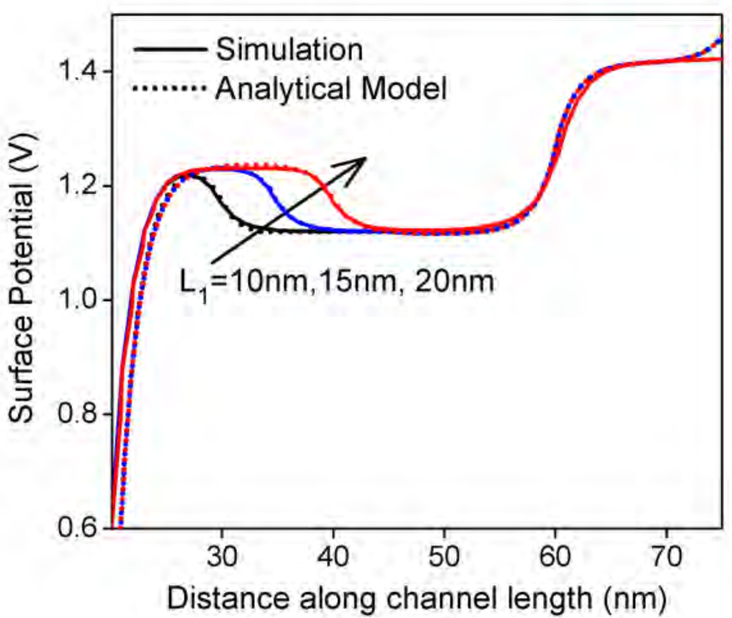

Fig. 5.4: Surface potential along channel length for $L_1 = 10,\ 15$, and $20nm$ with $V_{GS} = 1V$, $V_{DS} = 1V$ and $\epsilon_{ox} = 21$.

The changes in surface potential when L_1 is varied keeping the total channel length fixed, are shown in Fig. 5.4. The same value of ψ_{sf} under the metal gates are maintained when metal gate lengths are varied. ψ_{sf} near source-channel region

also does not vary as the length of $M1$ is varied. From Fig. 5.4 it is evident that the proposed model is in good agreement with the TCAD simulation results when metal gate lengths are varied. The effects of three gate dielectric material SiO_2 (ϵ_{ox} = 3.9), Si_3N_4 (ϵ_{ox} = 7.5), and HfO_2 (ϵ_{ox} = 21) on ψ_{sf} are depicted in Fig. 5.5. When ϵ_{ox} is increased, there is notable increase in the value of ψ_{sf} under $M1$ due to the increased capacitance and better gate coupling given by high-k dielectric.

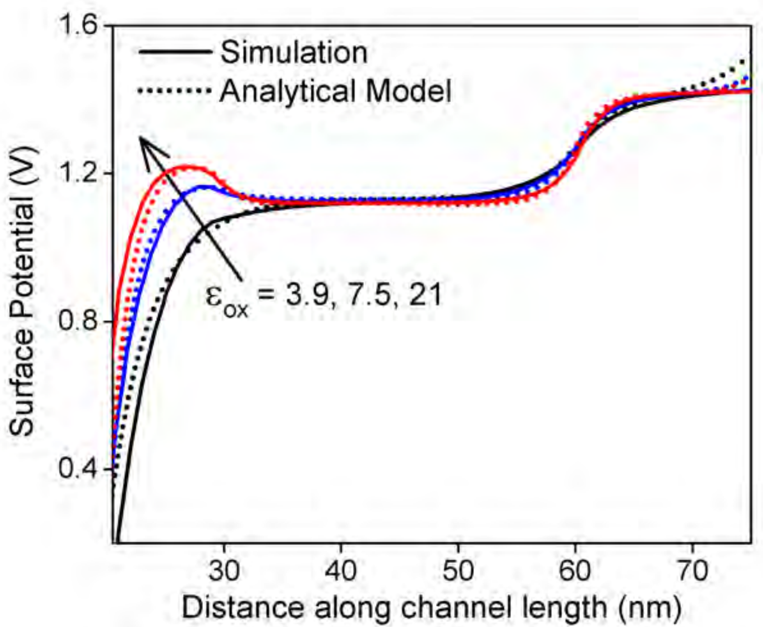

Fig. 5.5: Surface potential along channel length for ϵ_{ox} = 3.9, 7.5, and 21 with $V_{GS} = 1V$ and $V_{DS} = 1V$.

The proposed model can be generalized for single and multiple material gate TFFET structures. Fig. 5.6 shows the variation of ψ_{sf} for dual material double gate (DMDG) and single material double gate (SMDG) TFET structures. Here, device parameters for simulation is used as mentioned in [74] for DMDG and [75] for SMDG structure. Plots are generated with $V_{GS} = 1V$ and $V_{DS} = 1V$. Good

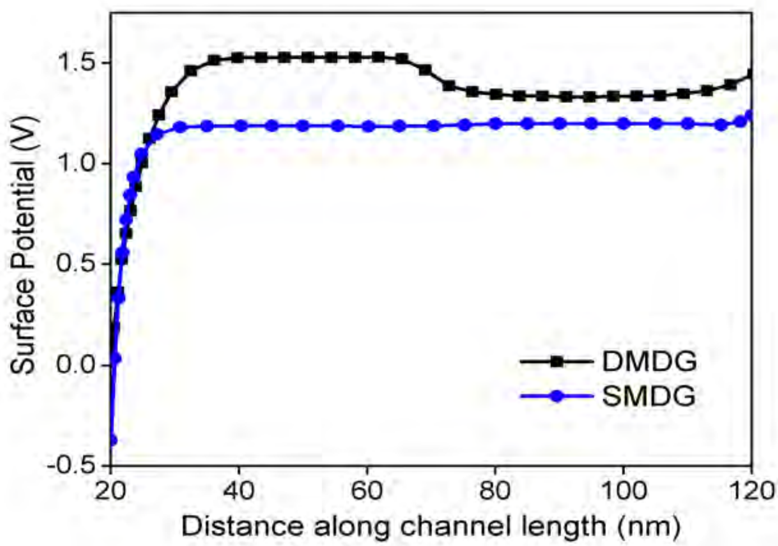

Fig. 5.6: Surface potential along channel length for DMDG and SMDG TFET structure given by the developed model (symbols) and analytical models from [74] and [75] (solid lines).

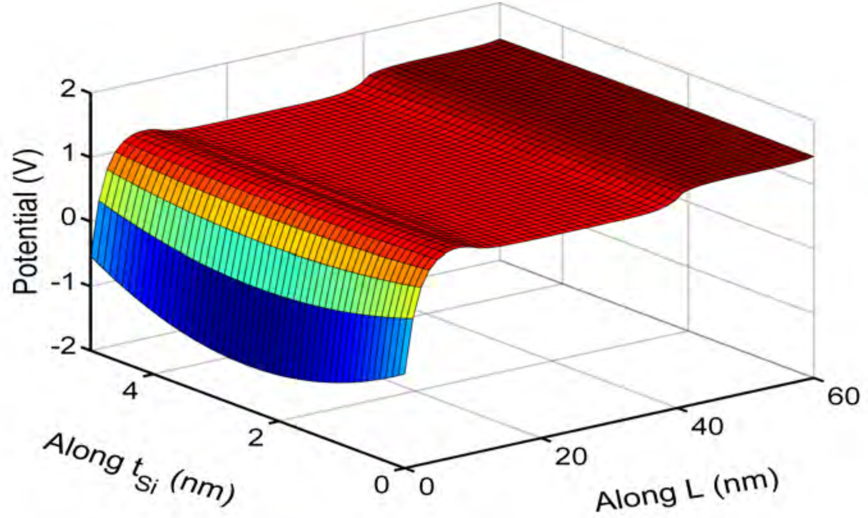

Fig. 5.7: 2-D electric potential from developed model for $V_{GS} = 1V$, $V_{DS} = 1V$ and $\epsilon_{ox} = 21$.

agreement of the derived model with analytical models of [74] for DMDG and [75] for SMDG TFET structure ensures that the proposed model is a generalized one.

Fig. 5.7 shows the variation of 2-D surface potential given by the analytical model for $V_{GS} = 1V$ and $V_{DS} = 1V$.

5.3.2 Electric Field

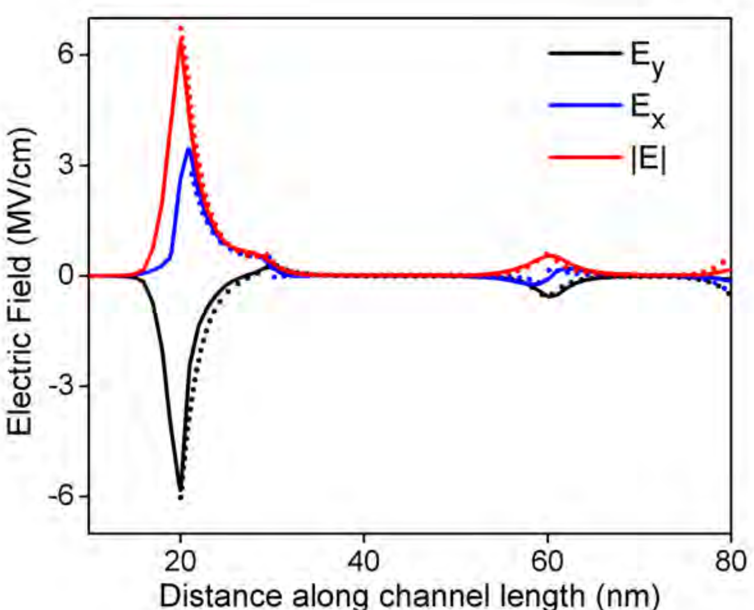

Fig. 5.8: Horizontal field (E_y), vertical field (E_x) and resultant electric field ($|E|$) along channel length given by the developed model (dotted lines) and the TCAD simulation (solid lines) with $\epsilon_{ox} = 21$, $V_{GS} = 1V$ and $V_{DS} = 1V$.

The horizontal electric field (E_y), vertical electric field (E_x), and the resultant electric field ($|E|$) given by the derived model and TCAD simulations are exhibited in Fig. 5.8. The electric field is maximum at the tunneling junction which indicates the presence of sufficient tunneling of electrons. Better carrier transport

efficiency is achieved in TMDG structures owing to the two peaks in electric field profile located at the two metal junctions compared with a single peak in DMDG structures. These peaks attribute better average electric field across the channel. The additional peaks in the electric field causes rapid acceleration to the carriers present in the channel, thus ensuring a higher gate transport efficiency to supply more numbers of carriers to the drain.

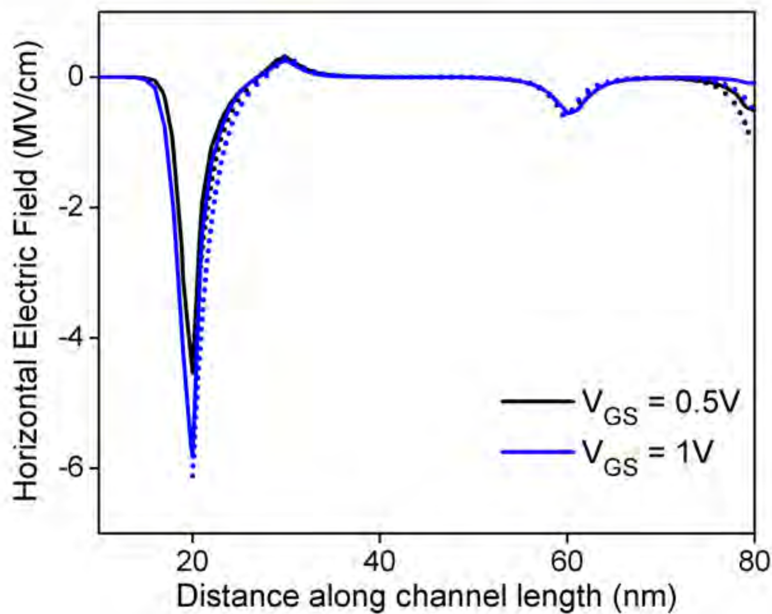

Fig. 5.9: Horizontal field (E_y) along channel length from the developed model (dotted lines) and the TCAD simulation (solid lines) for V_{GS} = 0.5 and $1V$ with $V_{DS} = 1V$ and $\epsilon_{ox} = 21$.

Although vertical electric field contributes to the average electric field, lateral electric field plays the major role in the tunneling process for TFETs. Therefore, effect of biasing and device parameter variation is studied for horizontal component of the electric field. The effect of V_{GS} on horizontal electric field is depicted in Fig. 5.9. At $V_{DS} = 1V$, as V_{GS} is increased from $0.5V$ to $1V$, E_y increases from

4.5MV/cm to 5.8MV/cm. Doubling the gate voltage increases the lateral field by 1.3 times and will also increase the band-to-band tunneling current. These increase in electric field will continue as long as V_{GS} is lower than V_{inv}. When V_{GS} is below V_{inv}, the potential is independent of V_{DS} and this will be also applicable for the electric field.

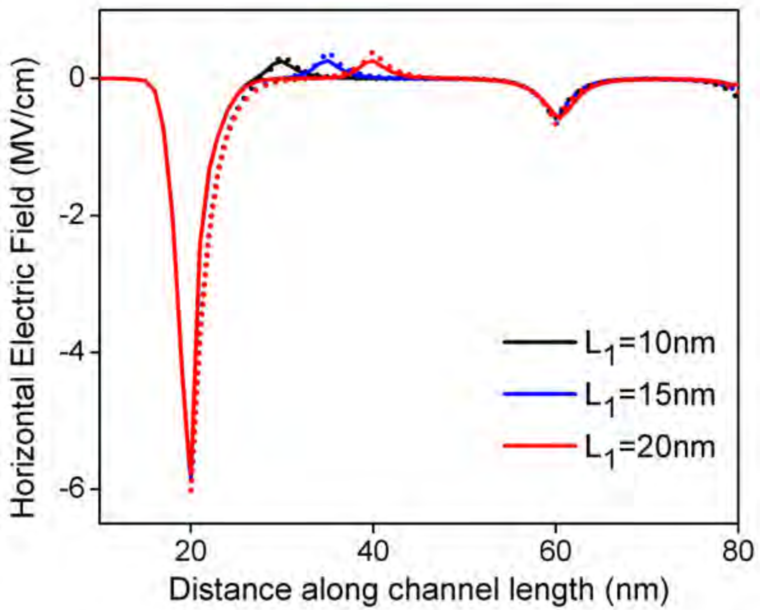

Fig. 5.10: Variation of horizontal field (E_y) along channel length from the developed model (dotted lines) and the TCAD simulation (solid lines) for $L_1 = 10, 15,$ and $20nm$ with $V_{GS} = 1V$, $V_{DS} = 1V$ and $\epsilon_{ox} = 21$.

The effect of gate length variation while keeping L_3 and L constant, is studied in Fig. 5.10. The value of E_y at tunneling junction do not vary as the length of L_1 is varied. Only a shift in the position of the peak occurs as the location of metal junction changes. For a smaller value of L_1, the peak of its E_y is nearest to the source region. It ensures a peak in its electron velocity nearest to the source side, resulting in the maximum improvement in the carrier transport efficiency [91].

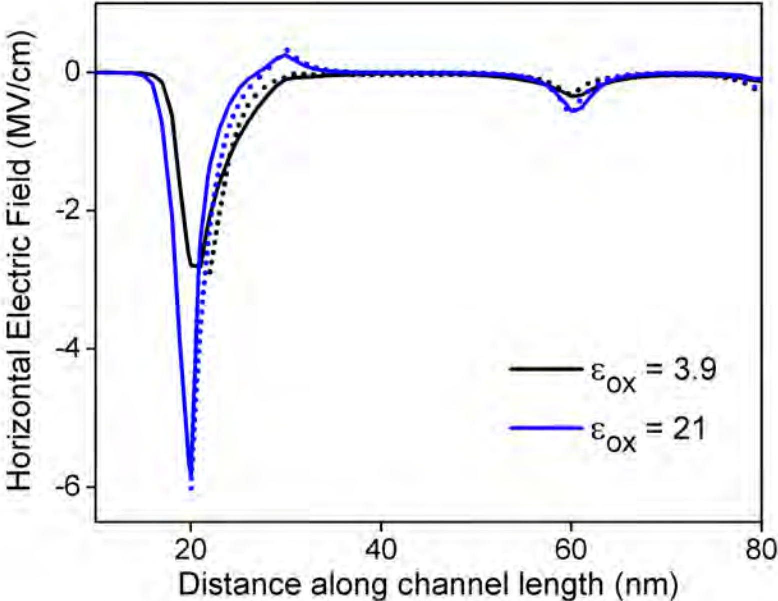

Fig. 5.11: Horizontal field (E_y) along channel length from the developed model (dotted lines) and the TCAD simulation (solid lines) for ϵ_{ox} = 3.9, 7.5, and 21 with $V_{GS} = 1V$ and $V_{DS} = 1V$.

The dependence of E_y on gate dielectric is exhibited in Fig. 5.11. For high-k dielectric the value of electric field at the tunneling junction increases. This increase in electric field will aid more to the tunneling of carriers through the energy barrier, resulting in more band-to-band tunneling current. High-k dielectric also increase the value of E_y peaks which will contribute to the carrier transport efficiency.

The 2-D average electric field and its component given by the formulated model is shown in Fig. 5.12, Fig. 5.13, and Fig. 5.14.

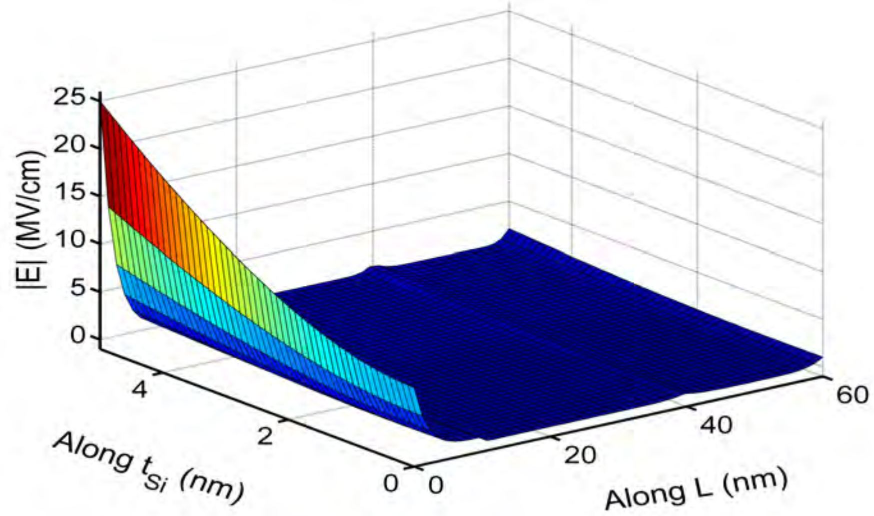

Fig. 5.12: 2-D average electric field from the derived analytical model for $V_{GS} = 1V$, $V_{DS} = 1V$ and $\epsilon_{ox} = 21$.

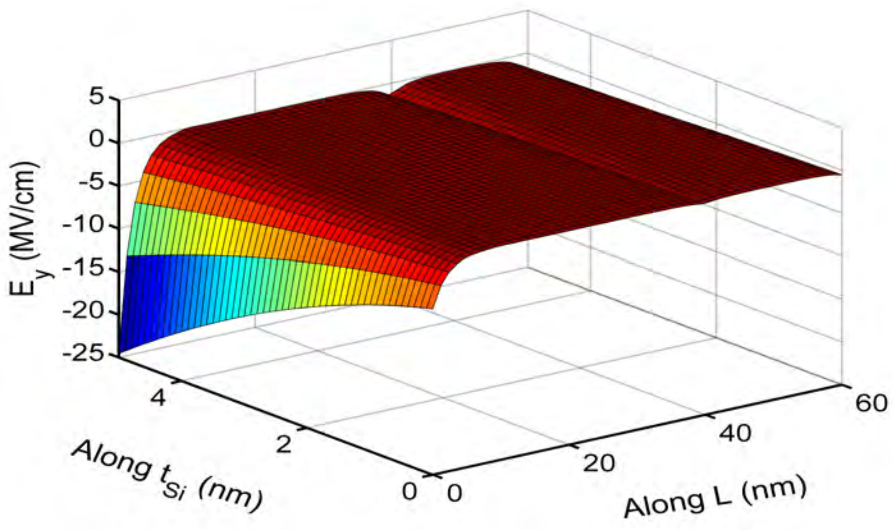

Fig. 5.13: 2-D horizontal field given by the developed model for $V_{GS} = 1V$, $V_{DS} = 1V$ and $\epsilon_{ox} = 21$.

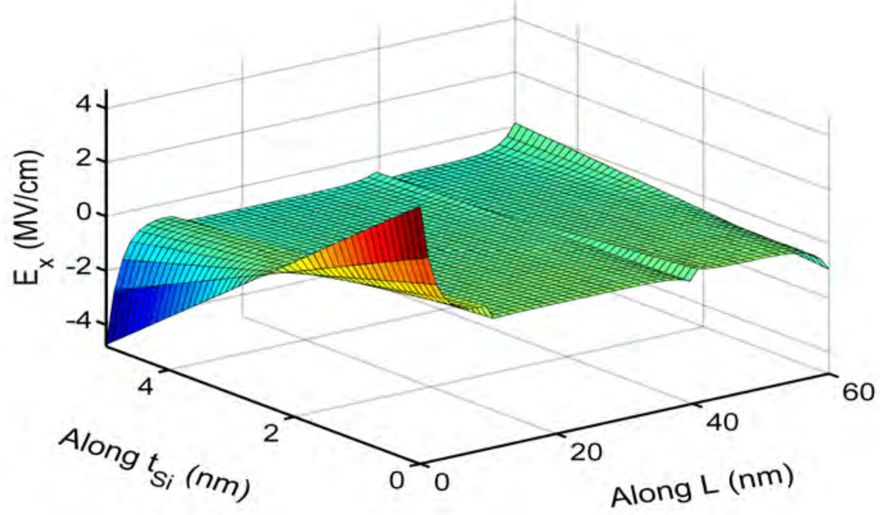

Fig. 5.14: 2-D vertical field from the developed model for $V_{GS} = 1V$, $V_{DS} = 1V$ and $\epsilon_{ox} = 21$.

5.3.3 Tunneling Current

The modulation of tunneling current with different biasing condition and device parameter variation has been analyzed for the formulated analytical model and TCAD simulation. Fig. 5.15 shows the transfer characteristic curve for $V_{DS} = 1V$ and $\epsilon_{ox} = 21$. In terms of biasing, V_{GS} is the main controlling parameter for the tunneling current. At very low V_{GS}, large tunneling barrier exist and no tunneling of electron occurs from the valence band of the source to the conduction band of the channel. Under this situation, only leakage current exist in the device. When V_{GS} is high enough to bring the conduction band of the channel below the valence band of the source, electron tunnels from source to channel, resulting in band-to-band tunneling current. After tunneling, electric field near the tunneling junction and under the metal junctions drift it towards drain. As V_{GS} is increased

further, the barrier width decreases and tunneling current increases. An increase of V_{GS} from $0V$ to $1.5V$ can increase the tunneling current from $3.4x10^{-10}A/\mu m$ to $1.7x10^{-4}A/\mu m$ causing a boost of $5x10^5$ times. There is slight deviation between the formulated model and TCAD simulation because in the formulation only lateral field at the surface is considered for the simplicity of the model.

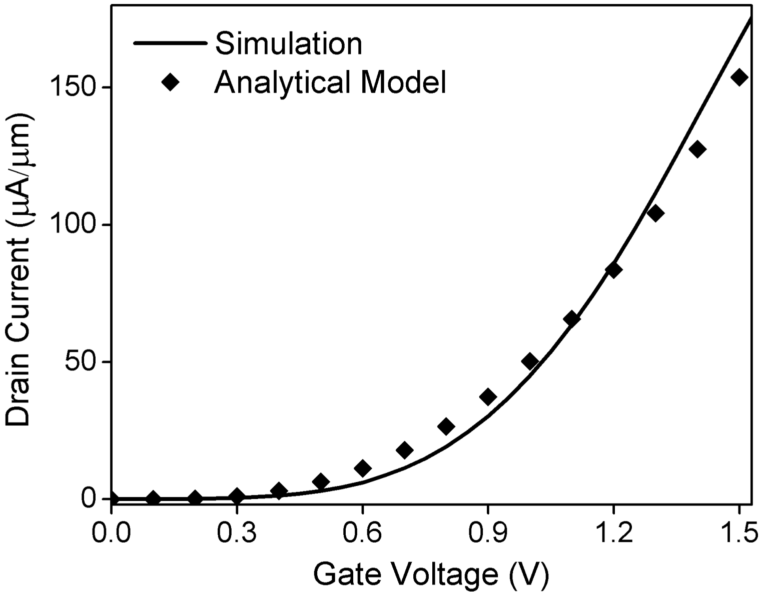

Fig. 5.15: Transfer characteristics curve given by the proposed model and TCAD simulation for $V_{DS} = 1V$ and $\epsilon_{ox} = 21$.

Based on the previous discussions on the effect of V_{DS} on TFET characteristics, it has been found that device characteristics are less sensitive to this biasing parameter as long as V_{GS} is below V_{inv}. The effect of V_{DS} on drain current is shown in Fig. 5.16 which is also in agreement with the previous argument. When V_{GS} is above V_{inv}, there will be thermal injection of electrons from drain into the channel [92] and the tunneling electrons will no longer be the sole contributor of drain current.

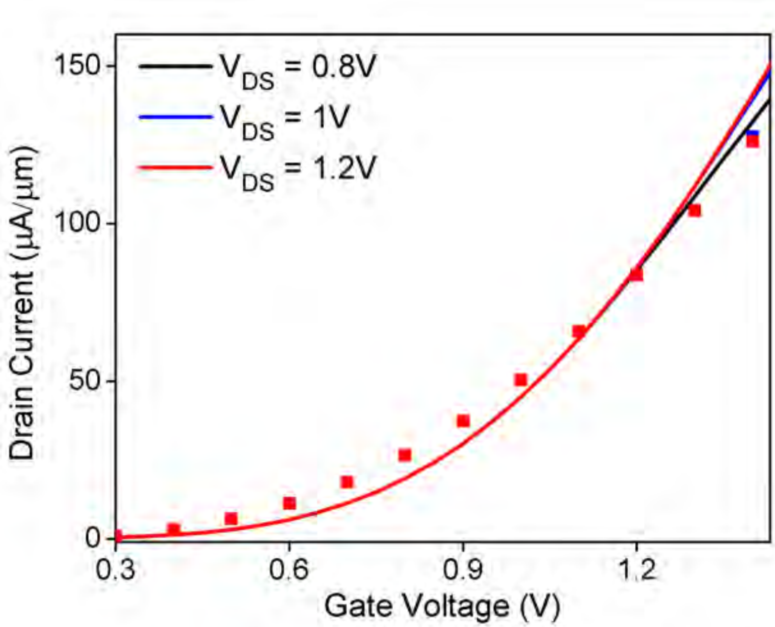

Fig. 5.16: I_D vs V_{GS} curve proposed by the analytical model (symbols) and TCAD simulation (solid lines) for $V_{DS} = 0.8,\ 1,$ and $1.2V$ with $\epsilon_{ox} = 21$.

For analyzing previous electrical characteristics, L_1 has been varied keeping the total gate length constant and no major variation at the tunneling junction has been observed. For drain current, the effect of total gate length variation keeping $L_1 : L_2 : L_3$ constant is depicted in Fig. 5.17 from which it is evident that drain current is independent of gate length.

The effect of gate dielectric on the band-to-band tunneling current is shown in Fig. 5.18 for SiO_2 ($\epsilon_{ox} = 3.9$), Si_3N_4 ($\epsilon_{ox} = 7.5$), and HfO_2 ($\epsilon_{ox} = 21$). For high-k dielectric gate capacitance increases, resulting in higher ON-current at the cost of higher leakage current. Although, low value of gate dielectric can provide low OFF-current and higher I_{ON}/I_{OFF} ratio, the ON-current is very low.

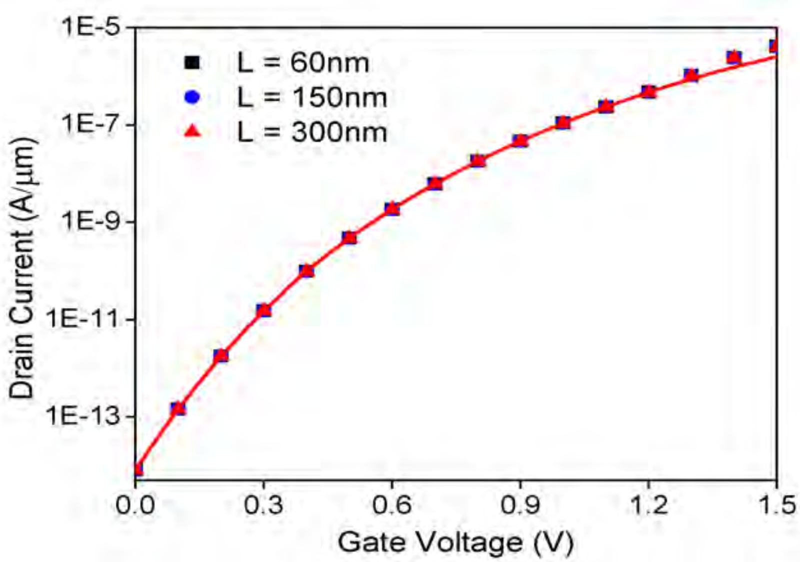

Fig. 5.17: Transfer characteristics (log scale) for varying channel length given by the analytical model (symbols) and TCAD simulation (solid lines) with $V_{DS} = 1V$ and $\epsilon_{ox} = 7.5$.

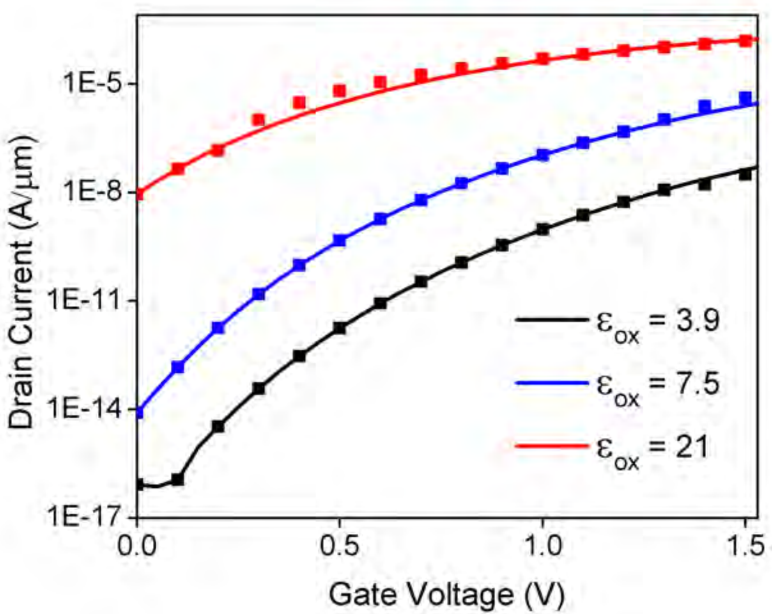

Fig. 5.18: Variation of I_D with V_{GS} given by the analytical model (symbols) and TCAD simulation (solid lines) for $\epsilon_{ox} = 3.9,\ 7.5$, and 21 with $V_{DS} = 1V$.

5.3.4 Gate Threshold Voltage

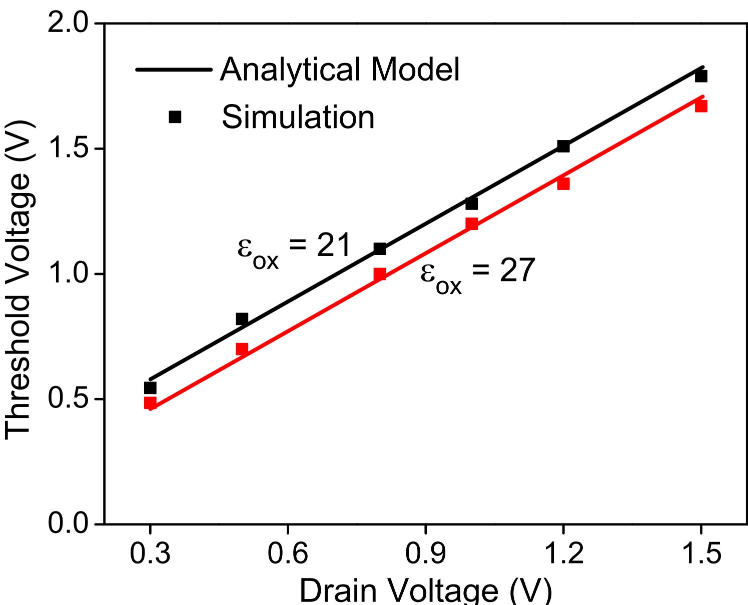

Fig. 5.19: V_{TH} vs V_{DS} for different ϵ_{ox}.

The effect of varying drain voltage, channel length, gate dielectric material and Si film thickness on gate threshold voltage is studied. The variation of V_{TH} with applied drain bias for two high-k dielectric: $\epsilon_{ox} = 21, 27$ is depicted in Fig. 5.19. The model results are in good agreement with simulation results. Higher value of drain voltage results in higher value of threshold voltage. This happens because at higher drain voltage the gate retains quasi exponential control of the current over a larger voltage range. Same phenomena is observed in Fig. 5.20.

The effect of gate length scaling on V_{TH} is investigated in Fig. 5.21. It can be seen that V_{TH} is independent of device length. This is due to the limit effect of gate length on V_{TH}. In TFET, the maximum electric field is always at the source-body junction, and is independent of the device length.

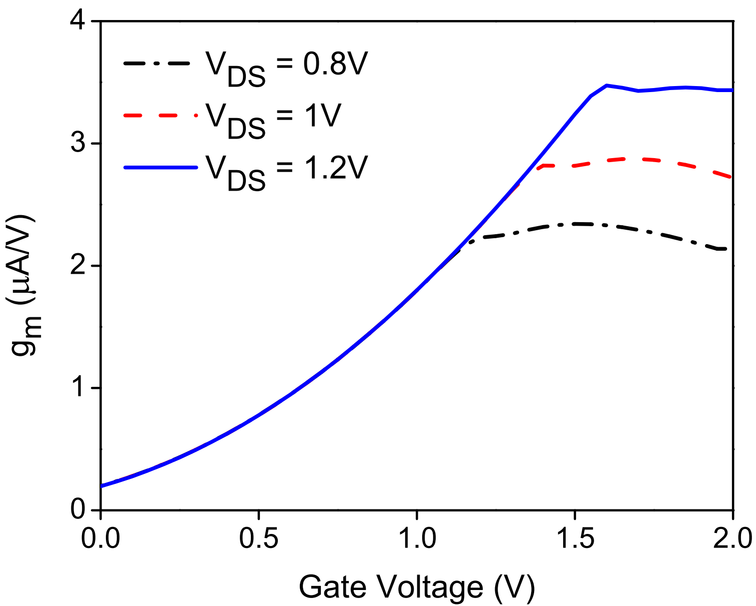

Fig. 5.20: Modulation of transconductance with gate voltage.

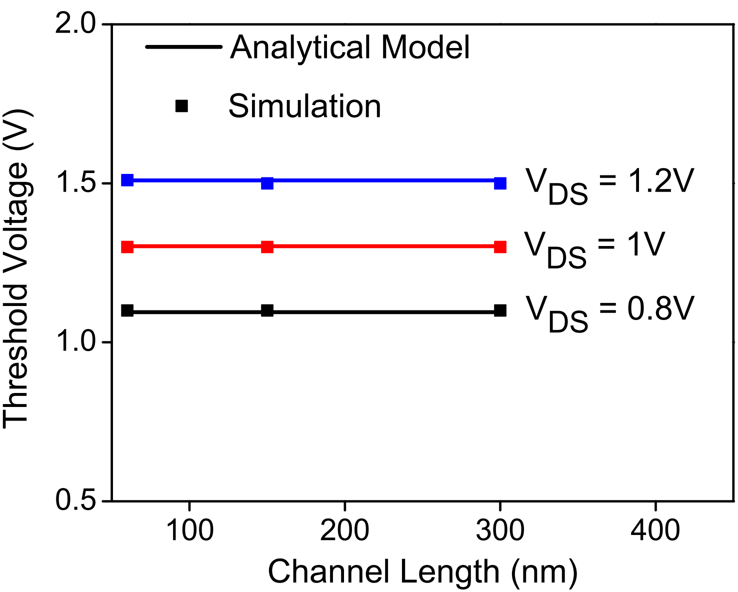

Fig. 5.21: Variation of V_{TH} with channel length.

The effect of Si layer thickness on V_{TH} is investigated in Fig. 5.22. When the Si film becomes thinner, it changes the electric field lines. The gate control of the barrier width in the tunnel junction increases which in turn results in a decreased V_{TH}.

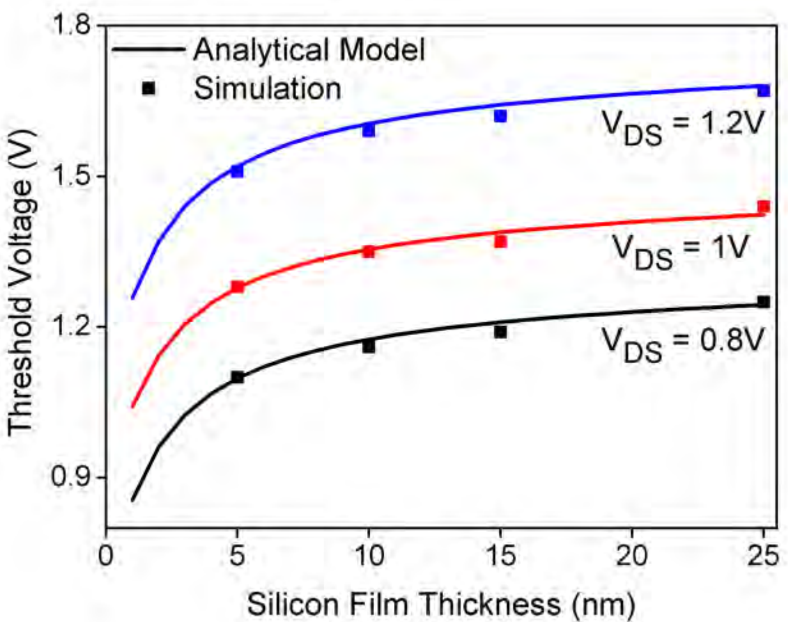

Fig. 5.22: Dependence of V_{TH} on silicon film thickness at $V_{DS} = 1V$ and $\epsilon_{ox} = 21$.

Fig. 5.23 depicts that high-k dielectric improves the threshold voltage. The proposed model can effectively represent this effect. This happens because high-k dielectric aids the gate to have better capacitive control over the barrier width at tunnel junction. Fig. 5.24 shows that increasing the value of ϵ_{ox} shifts the current curve to the left as anticipated.

The proposed model is a generalized model for single and multiple material gate TFET structure. Fig. 5.25 shows the variation of V_{TH} with drain bias for SMDG and DMDG TFET structures. Besides, comparison with analytical model

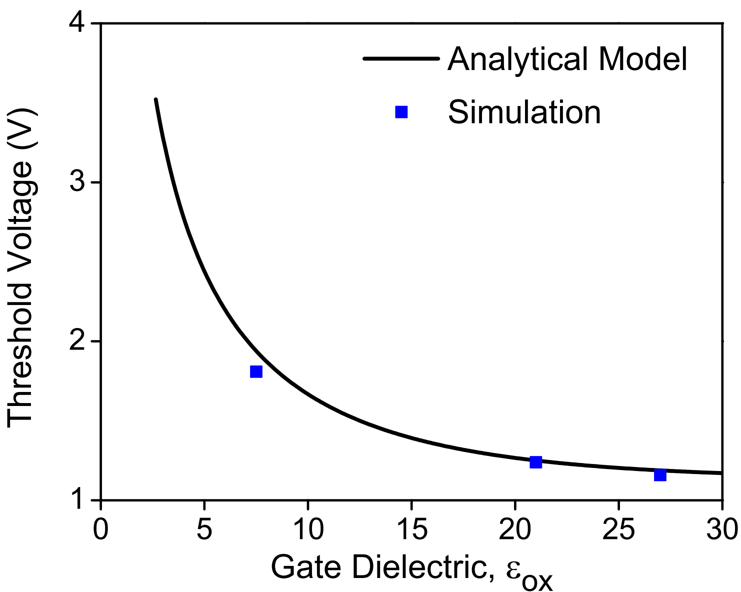

Fig. 5.23: Variation of V_{TH} with changing gate dielectric for $V_{DS} = 1V$.

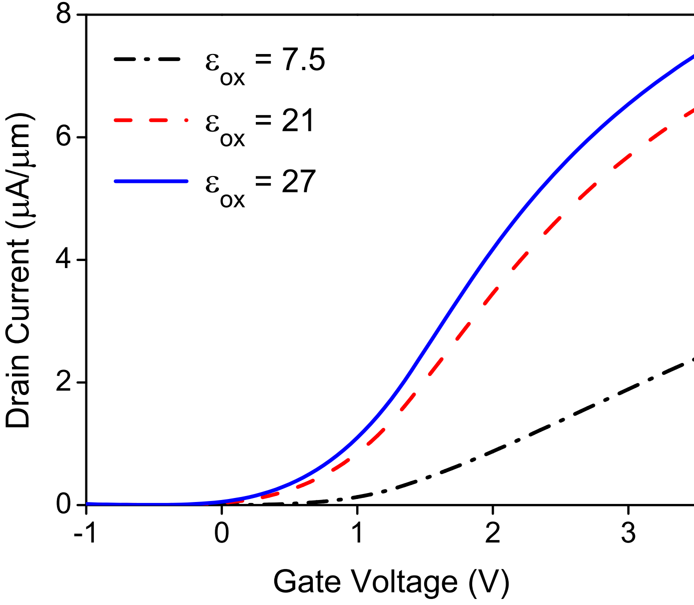

Fig. 5.24: Transfer characteristics curve for different gate dielectric.

of [75] for SMDG and [88] for DMDG depicts that the proposed model is a generalized one.

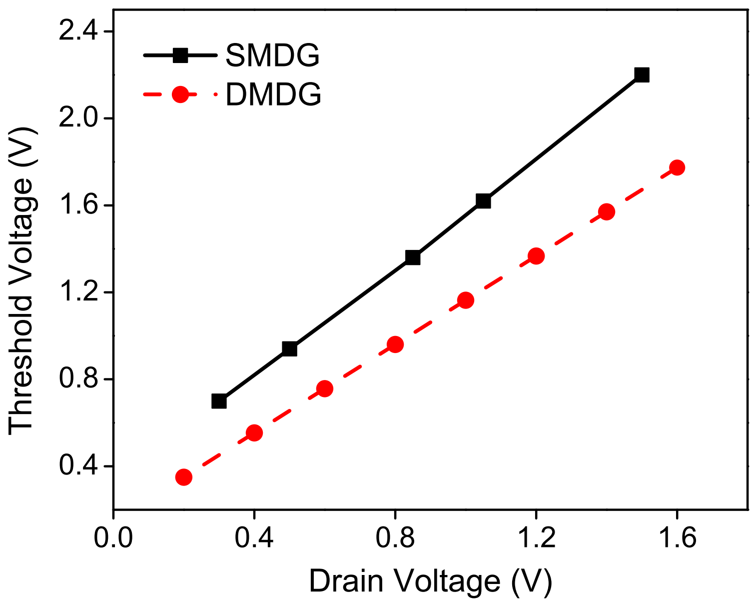

Fig. 5.25: V_{TH} curve for SMDG and DMDG structures. Symbols represent analytical model of [75] for SMDG and [88] for DMDG structure.

In the proposed model, we did not include the effect of inversion charge. Inversion voltage represents the onset of saturation of surface potential with respect to V_{GS} [92]. Fig. 5.3 shows the variation of surface potential with gate bias. Comparison of Fig. 5.3 and Fig. 5.19 indicates that inversion occurs after threshold point. Therefore, exclusion of the effect of inversion charge does not have major effect on the accuracy of threshold voltage. Besides, quantum effect is neglected in our model which introduces 1% error [93].

5.4 Si Film Thickness Optimization

The effects of Si film thickness on electric field, electric potential, tunneling barrier width, and drain current are studied by performing simulation in Silvaco Atlas.

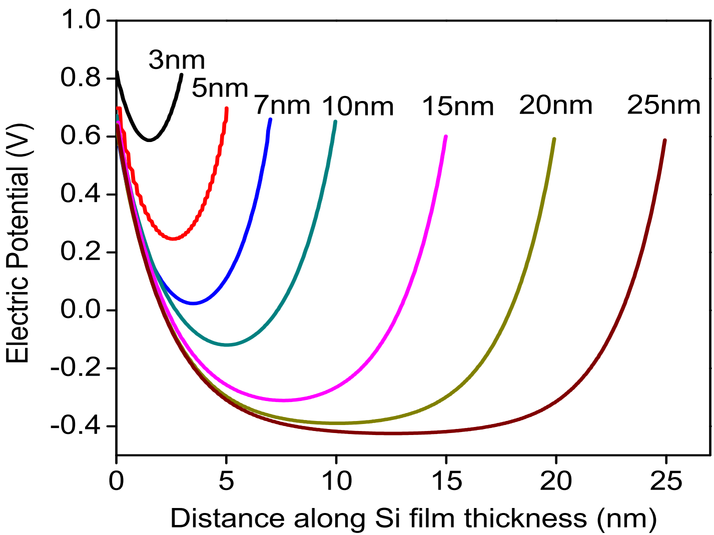

Fig. 5.26: Electric potential along x direction near source-channel tunneling junction.

Fig. 5.26 and Fig. 5.27 show the electric potential and electric field vertical to channel length and close to the tunneling region for different t_{Si}. Electric potential and electric field are highest at the surface and account for a great part of total drain current. However, a subsurface portion of Si film contributes a substantial part of the total drain current. From these figures, it is evident that gate-to-channel coupling at $x = t_{Si}/2$ is strong below film thickness of $7nm$. Therefore, when t_{Si} is lower than $7nm$, electric potential and electric field at the center of Si film can result in sufficient band-to-band tunneling.

At the surface, tunneling barrier width, w_b is the smallest due to strongest gate

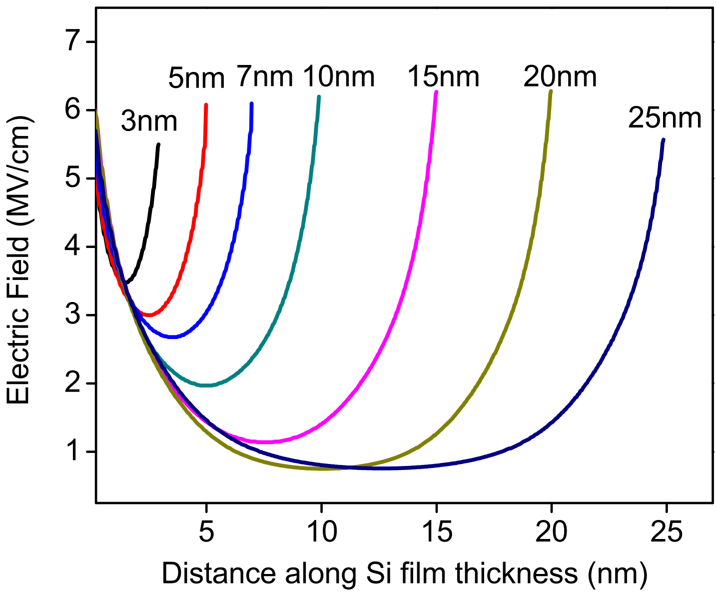

Fig. 5.27: Electric field along x direction near band-to-band tunneling region of source-channel interface.

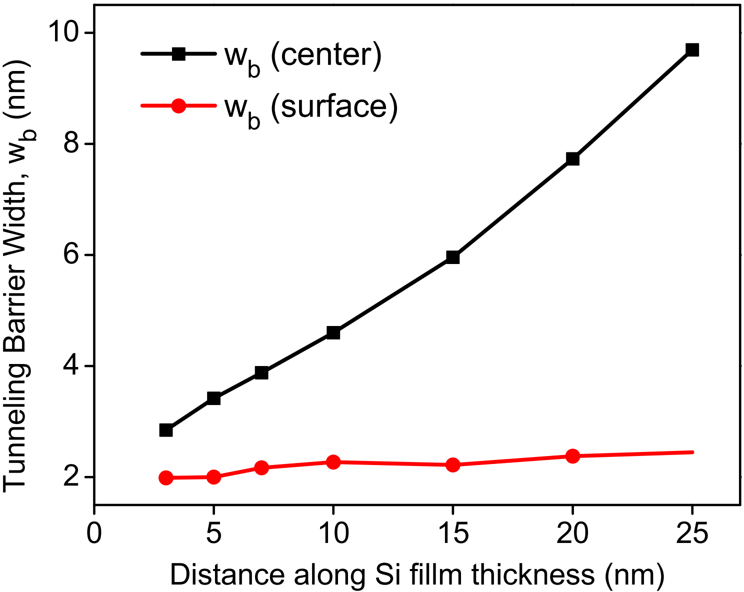

Fig. 5.28: Energy barrier width, w_b at the surface and at the center ($x = t_{Si}/2$) of Si film for different t_{Si}.

control which is depicted in Fig. 5.28. The gate control becomes weaker towards the center of the film which in turn results in wider w_b and reduce the tunneling probability. From Fig. 5.28 it is evident that coupling of two gate electrodes is strong up to $10nm$.

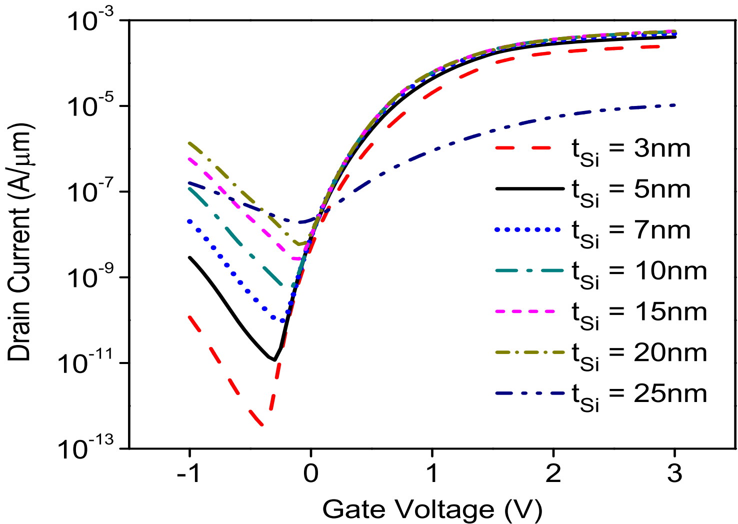

Fig. 5.29: Effect of t_{Si} on Transfer characteristics.

The transfer characteristics of TMDG TFET for different t_{Si} is shown in Fig. 5.29. At t_{Si} of $3nm$, the electric potential at the center of the film is very high but due to volume limiting, on-state drain current, I_{ON} is low. I_{ON} increases as t_{Si} is increased due to availability of larger volume for band-to-band tunneling but at a cost of higher OFF current, I_{OFF}. I_{ON} increases slightly when t_{Si} is increased from $7nm$ to $20nm$ which is shown in Fig. 5.30. This happens because at t_{Si} above $7nm$ electric potential at center cannot result in enough tunneling to increase the drain current. When t_{Si} is above $20nm$, I_{ON} starts to drop due to weaker double gate-to-channel coupling effect [45].

The effect of t_{Si} variation on average current density, J_{avg} is depicted in Fig.

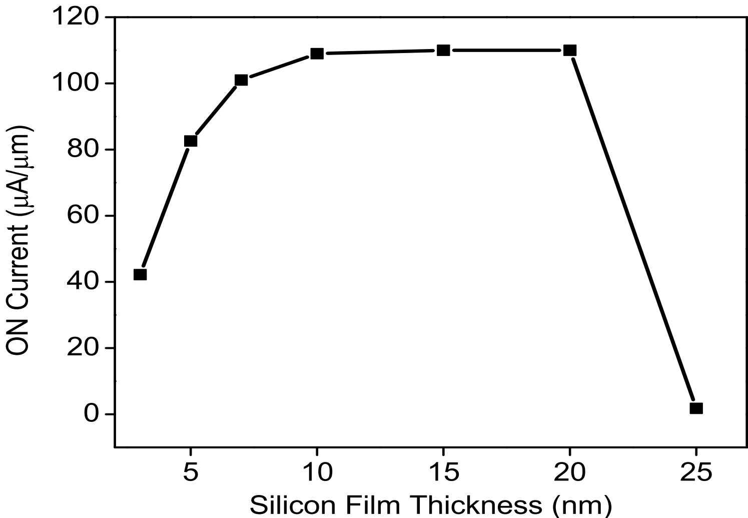

Fig. 5.30: Modulation of I_{ON} by Si film thickness.

5.31. J_{avg} can be calculated as

$$J_{avg} = \frac{I_{ON}}{t_{Si}} \tag{5.1}$$

J_{avg} increases as the film thickness is reduced and is maximum when t_{Si} is $5nm$. Due to volume limiting effect, J_{avg} decreases below $5nm$.

Fig. 5.32 shows the I_{ON}/I_{OFF} for different t_{Si}. I_{ON}/I_{OFF} decreases as t_{Si} increases. This is because I_{OFF} increases with t_{Si} due to increased trap and defect density in device. According to ITRS (2014), for low power devices I_{ON}/I_{OFF} of 10^5 is needed. TMDG TFETs with $t_{Si} < 15nm$ meet this requirement. Although highest I_{ON}/I_{OFF} is at $t_{Si} = 3nm$, at this t_{Si}, I_{ON} is comparatively low.

From the above discussions, it can be suggested that t_{Si} should be in the range of $5nm - 7nm$. I_{ON} is low below this range. Above this range, I_{ON} does not increase significantly and larger t_{Si} reduces the I_{ON}. This range also meets the criterion for I_{OFF} ($10^{-9}A/\mu m$) mentioned in ITRS (2014).

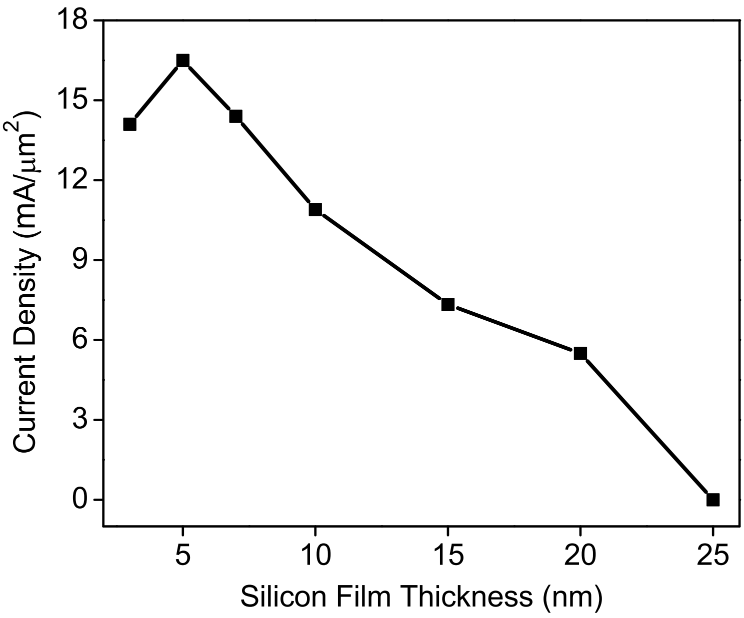

Fig. 5.31: Variation of average current density with Si film thickness.

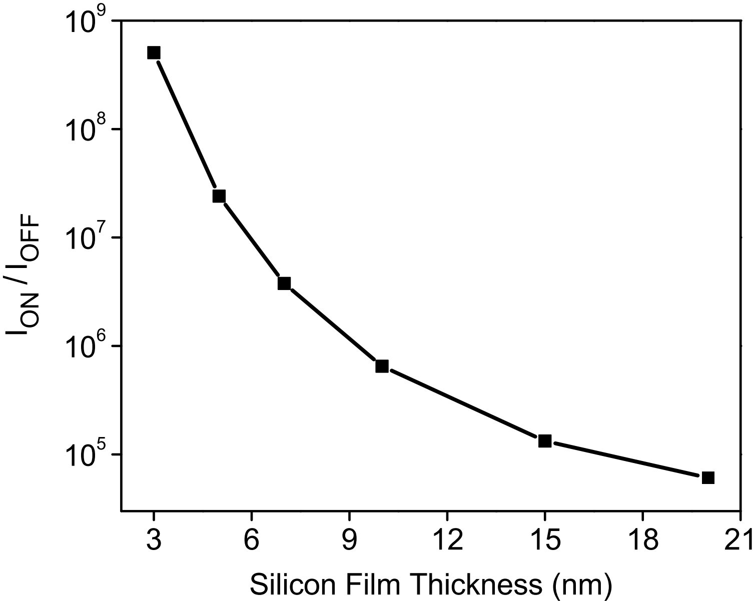

Fig. 5.32: I_{ON}/I_{OFF} for different Si film thickness.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this dissertation, 2D analytical models of potential and electric field for triple material double gate TFET structures are proposed. The proposed model of electric field is used to calculate the distribution of tunneling generation rate. Since the band-to-band tunneling current depends on many parameters, appropriate simplifications are considered for formulating a closed form model of this characteristic. A physical definition is taken into account for deriving the expression of gate threshold voltage from surface potential model. Later these models are generalized for single material and double material gate TFET structures.

A numerical model of triple material double gate TFET structure is developed in Sivaco Atlas. The TCAD simulation results are used to validate the accuracy of the proposed models. Device parameters i.e. channel length, film thickness, and gate dielectric material are varied to study their effects on the electrical characteristics of TFET. The effect of changing biasing conditions are also analyzed

and validity range of the developed models are discovered. The derived models can predict the device characteristics with reasonable accuracy compared to the TCAD simulation results when the gate voltage is below the inversion voltage. Beyond inversion voltage, the device physics is not solely governed by the tunneling mechanism, there is thermal injection of carriers from drain. Under such situation, the formulated models will show deviation from the actual device behavior. A solution to increase the value of inversion voltage and hence extend the legality of the model is also suggested, that is by increasing the bias at the drain side.

Transconductance change method, widely acceptable for non-linear devices, is used to extract the value of threshold voltage from simulation results. The proposed model shows good agreement with the simulation results. From the analysis it can be suggested that thin Si film and high-k dielectric aids to improve the threshold voltage characteristics. In formulating the threshold voltage model, inversion layer charges are not included. TCAD simulations show that inversion occurs after threshold. Therefore, exclusion of inversion charges does not affect the accuracy of the proposed threshold voltage model.

A through analysis on the effect of Si film thickness on device performance is performed based on the TCAD simulation results and device physics governing it is detailed. A silicon film thickness between 5-7nm is suggested for boosting the device performance in terms of ON-current, OFF-current, and I_{ON}/I_{OFF} ratio.

When extremely high source doping is used, degeneration of the energy band cannot cut off the higher energy tail of the Fermi distribution. In such cases, band profile of TFET resembles to that of a MOSFET. In this work, source doping of 10^{20} cm^3 is used which do not introduce high level of degeneracy. But if very

high level of doping is used, the model will fail to predict the behavior of the device since the device will no longer depend only on band-to-band tunneling mechanism.

The quantum effects are also not incorporated in the derivation of the models. Literature shows that neglecting the quantum effects introduce only 1% error. In such situation, calculation complexity is greatly reduced without sacrificing the accuracy of the results significantly.

Analytical models are necessary for circuit design and device performance optimization. The proposed models can be helpful in designing and analyzing TFET with single material gate and multiple material gate structures.

6.2 Future Works

There is certainly much more scope of work which can be done in the field of TFET. The biggest future challenge is to successfully design and fabricate fully-optimized Tunnel FETs of both n-type and p-type, that show low OFF-currents beyond what is possible for conventional MOSFETs, high ON-currents, and average subthreshold swings of less than 60 mV/decade at room temperature. Further work will also be necessary in order to develop accurate analytical and compact models for Tunnel FETs. Unavailability of experimental data has been a constraint in shaping the analytical models for multiple material gate TFET structures more accurately. Only a few experimental data for single material gate TFET structures have been published so far. More calibration and tuning of the models is possible once more experimental data is available.

This work can be further extended by including the effect of depletion layers

in formulating the model which can reflect more precise results at the source-body and drain-body junctions. Optimization of device parameters other than Si film thickness can also be performed for triple material double gate TFET structures. AC simulations and relevant model development can also be performed for establishing a better understanding of the dynamic characteristics of Tunnel FETs.

It is convincing from the researches that once Tunnel FETs have been investigated and developed more fully, and p and n-type Tunnel FETs with highly optimized characteristics have been fabricated, these promising devices will live up to their potential. It can be expected that these devices, or some variation upon them, will bring lower power consumption and better energy-efficiency to computers, appliances, and devices everywhere.

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