SECTION A

1. There are many books in central library of BUET in different subjects. Each book must have a ISBN number, title, name of authors, subject and number of copies. A book can have multiple copies and each copy is identified by an accession number. The descriptive attributes of each copy of book are edition, price and data of purchase. A publisher publishes many books and a book is published by only one publisher. A publisher is identified by publisher id and described by name, country of origin, address and contact numbers.

Book suppliers supply many copies of books to the library by tender in each year. A tender has an id, name, total price and year. For each copy of books, you must store the record of which copy of book has been supplied by which supplier in which tender. A supplier is identified by supplier id and described by name, address and contact numbers.

One copy of a book (book-copy) can be issued to multiple borrowers in different times and a borrower can borrow multiple number of book-copies. Borrowers can be teachers, students or staffs. Each borrower must have a borrower id, name, contact number and address. Teachers are described by joining date and designation. Students are described by session, level and term. Staffs are described by office name.

When a book-copy is issued to borrower, some information such as issued data, accession number, borrower id, length of period for issue and return date are needed to enter into the database. At the same time, the status of the borrowed book should be labeled as issued and will be cleared after return by the borrower.

(i) Draw an ERD for the above library management system of BUET.
(ii) Transform the ERD into tables showing all primary keys and foreign keys.

2. (a) Given three relations as follows:

\[ \text{customer (customer id, name, street, city)} \]
\[ \text{account (account name, type, balance)} \]
\[ \text{transaction (customer id, account number, date, amount)} \]

(i) Write relational algebra expression using cartesian product to find customer id, date and amount of all transactions made by customer id "C005".

Contd .......... P/2
(ii) Rewrite the expression of Q. 2(a)(i) using natural join.
(iii) Write the equivalent relational algebra expression for the following SQL statement:

```
select a.customer id, b.account number, name, street, city
from customer as a, account as b, transaction as c
where a.customer id = c.customer id and b.account number = c.account
number and date = '01-JAN-2017' and amount > 10000
```

(b) Given the relation schema of CSE department course database as follows:

```
course (course number, title, credit hour, level, term, pre-requisite course number)
takes (course number, student id)
student (student id, name, CGPA)
```

(i) Write SQL statement to find the list of only those students who have taken all the courses of level 3 and term 1.
(ii) Write SQL statement to find the list of courses that are not taken by any student.
(iii) Write SQL statement to find the student id and the number of courses taken for those students with CGPA higher than 3.5.

3. (a) Explain the application of left, right and full outer joins with examples.

(b) Given the employee database as follows:

```
Employee (employee name, house number, street, city)
Works (employee name, company name, salary)
Company (company name, city)
Manages (employee name, manager name)
```

Write SQL: DDL for the above employee database with the following constraints:

(i) A new employee name can be entered into the database only in the employee table and employee name cannot be duplicate.
(ii) Manager name must be any of the employee name.
(iii) City can be only Dhaka, Chittagong, Rajshahi or Khulna.
(iv) No. two employees can have same house number, street and city.
(v) A company name cannot be duplicate and an employee cannot work in a company such that company name is not present in company table.

(c) Given three relations as follows:

```
customer (customer id, name, street, city)
account (account number, type, balance)
transaction (customer id, account number, date, amount)
```

Contd …….. P/3
A view has been created on the above schema as follows:

create view cust-balance as
select a.customer id, balance
from customer as a, account as b, transaction as c
where a.customer id = c.customer id and b.account number = c.account number

Discuss the possible problems if insertion is allowed through the view cust-balance.

4. (a) A car rental company maintains a database for all vehicles in its current fleet. For all vehicles, it includes the vehicle identification number, license number, manufacturer, size (height, width and length) and color. Special data are included for certain types of vehicles:

- Trucks: load capacity, type
- Sports car: power, renter age
- Bus: number of passengers, seat-type (array of 40 seats of different types)

(i) Construct an SQL: 99 schema definition for this database using appropriate inheritance.

(ii) Write constructor functions for the above schema and insert statement to insert data into the tables.

(b) Given a set F of functional dependencies on a relation schema R(A, B, C) as follows:

A → BC
B → C
A → B
AB → C

(i) Compute the canonical cover for F.
(ii) Decompose R into R1 and R2 such that the decomposition is loss-less. What are the normal forms of the decomposed relations R1 and R2?

(c) Given a set F of functional dependencies on a relation schema r1(A, B, C, G, H, I) as follows:

A → B
A → C
CG → H
CG → I
B → H

Compute the attribute closure (AG)+ and show that AG is a candidate key of r1.
There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Briefly explain each of the ACID properties in DBMS.  (8)
(b) What are the components of disk latency?  (2)
(c) The Megatron 777 disk has the following characteristics:  (2+2+1=5)
   - There are ten surfaces, with 10,000 tracks each.
   - Tracks hold an average of 1000 sectors of 512 bytes each.
   - The disk rotates at 10,000 rpm.
   - The time it takes the head to move n tracks is 1+0.001 n milliseconds.
Now answer the following questions:
   (i) What is the capacity of the disk?
   (ii) What is the maximum seek time?
   (iii) What is the average rotational latency?

(b) Suppose, another Megatron 777 disk incurs average rotational latency of 8.3 milliseconds. To move the head assembly between cylinders takes 1 millisecond to start and stop, plus one additional millisecond for every 500 cylinders traveled. Now, the disk controller receives multiple disk access requests:

<table>
<thead>
<tr>
<th>Cylinder No.</th>
<th>First time available (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>0</td>
</tr>
<tr>
<td>3000</td>
<td>0</td>
</tr>
<tr>
<td>7000</td>
<td>0</td>
</tr>
<tr>
<td>2000</td>
<td>20</td>
</tr>
<tr>
<td>8000</td>
<td>30</td>
</tr>
<tr>
<td>5000</td>
<td>40</td>
</tr>
</tbody>
</table>

Show the finishing time and latency for each request if disk controller follows elevator algorithm.

(c) What is stable storage? Briefly explain the idea of reading and writing policy in a stable storage.  (2+4+4=10)

6. (a) In RAID level 4 scheme, 1 redundant disk is used no matter how many data disks are there. The problem is, when any block is written, we also need to update the redundant disk. Briefly explain an optimal policy for updating the redundant disk with an example (consider, 1 byte of data is written). Also, explain the logic behind adopting such policy.  (15)

Contd .......... P/5
CSE 303

Contd., Q. No. 6

(b) Is it possible to implement unclustered-sparse indexing scheme? If so, give an example. Otherwise, shortly explain the reason.

(c) What is the key property of a good hash function? How can you choose such a function?

(d) Consider the following B+ tree. Now, show (you do not need to explain) what happens after each of the following successive operations:

7. (a) The following figure shows a linear hash table with 3 records. We assume hash function $h$ produces 4 bits and we represent records by the value produced by $h$ when applied to the search key of the record. Here, $i$ is the number of lower order bits of the hash function currently used and $n$ is the current number of buckets. Each bucket can hold maximum of 2 records. We shall adopt the policy of choosing $n$, so that there are no more than $1.7^n$ records in the file.

![Figure for Question 6(d)](image)

![Figure for Question 7(a)](image)

Contd .......... P/6
Now, show (step by step) what happens after successive insertion of 0101, 0001 and 0111. Show the necessary calculation whenever a new bucket is required. Overflow blocks can be used if necessary.

(b) Write down the pseudocode for a sort-based union algorithm, that computes $R \cup S$. Also mention its runtime and constraints in terms of $B(R)$, $B(S)$ and $M$. Here, $B(R)$, $B(S)$ is the number of blocks in $R$ and $S$; $M$ is the number of blocks of each sublist to be sorted.

(c) Write down the key properties of B+ tree.

8. (a) Discuss three problems of non-serializable execution with necessary examples.

(b) Consider a schedule $S$: $r_2(A)$; $r_1(B)$; $w_2(A)$; $r_2(B)$; $r_3(A)$; $w_1(B)$; $w_3(A)$; $w_2(B)$. Show that, there is no serial schedule conflict-equivalent to $S$.

(c) What is deadlock in database transaction? Give an example.

(d) Mention the requirements of using shared and exclusive locks.

(e) Consider the following schedules of transactions $T_1$, $T_2$ and $T_3$.

$$r_1(A); r_2(B); r_3(C); w_1(B); w_2(C); w_3(D);$$

Now, insert shared and exclusive locks and place necessary unlocks to maximize concurrency.
SECTION – A

There are FOUR questions in this section. Answer any THREE.

1. (a) Discuss some extensibility mechanisms of UML diagram.
   (12)

(b) What are the different types of output document of a system? Explain with examples.
   (12)

(c) Let’s assume that, your company developed a system for which the development cost is $50,000. Your system analyst tells you that the operating cost for the next year is $5,000 and in each year the operating cost will increase by $1000. The expected cash inflow is given in the following table:

<table>
<thead>
<tr>
<th>Year</th>
<th>Cash inflow</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$18,000</td>
</tr>
<tr>
<td>2</td>
<td>$22,000</td>
</tr>
<tr>
<td>3</td>
<td>$26,000</td>
</tr>
<tr>
<td>4</td>
<td>$33,000</td>
</tr>
<tr>
<td>5</td>
<td>$41,000</td>
</tr>
<tr>
<td>6</td>
<td>$50,000</td>
</tr>
</tbody>
</table>

Considering discount rate of 11% calculate the payback period. Also calculate its ROI (Return on Investment) for these 6 years.

(d) Write short note on "Ishikawa Diagram".
   (7 2/3)

2. The following is a narrative description of the business process of a bank:

   There are two types of uses in a Bank: Normal user and Foreign User. Both users can create account, deposit money and withdraw money. For money withdrawal there are certain rules. A user can make a withdrawal of maximum 3,00,000 taka per day. At each transaction the highest limit of withdrawal is 1,00,000 taka. A user can make a maximum of 5 withdrawals per day. After every three months, interest is added to the account balance. If an account balance reaches 20,00,000 taka, for every deposit to that account 2% bonus is applied. The foreign user has one extra capability. He can convert his taka to foreign currency.

   The use cases of this scenario are:
   (i) Create account
   (ii) Deposit money
   (iii) Withdraw money
   (iv) Update balance
   (v) Calculate bonus
   (vi) Calculate interest and
   (vii) Convert to foreign currency.

   Contd ......... P/2
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Contd... Q. No. 2

Now answer the following questions based on the above scenario.

(a) Draw the use case diagram of this system.

(b) Write use case narrative for the use case "withdraw money".

(c) Draw sequence diagram for the use case "withdraw money".

(d) List all the entity classes of this system. Draw state chart diagram of the most important entity class in your consideration.

3. (a) Write short notes on the following software vulnerabilities. Also provide example and way around on these vulnerabilities.
   (i) Buffer Overflow Attack
   (ii) SQL Injection

(b) What are the checklists for a code reviewer to review the Non-Functional requirements of a project? Explain in short.

(c) The following code takes a user choice from the user. If the choice is I, it increments the value of x which is initialized as 5. If the choice is anything else, value for x is decremented.

Now rewrite this code so that the code follows the MVC principle.

```java
package withoutmvc;
import java.util.Scanner;

public class WithoutMVC {
	public static void main(String[] args) {
		int choice;
		int x=5;
		System.out.println("Enter your choice: ");
		Scanner sc=new Scanner(System.in);
		choice=sc.nextInt();
		if(choice==1) x = incx(x);
		else x = decx(x);
		System.out.println("New value: "+x);

		public static int incx(int x) {
			x++;
			nreturn x;
		}
		public static int decx(int x) {
			x--;
			nreturn x;
		}
	}
```
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4. (a) Donald Trump is a rookie UI designer. He designed the following registration page of an e-commerce site (e.g. amazon.com) where the user can browse through various items and buy items. Point out all the problems associated with this page in details.

(b) What are the steps of system construction and implementation? Mention only the steps. You do not need to explain them.

(c) Write down Schneiderman's 8 Golden Rules for UI design in short.

(d) Consider the following design of an EMI Calculator. In this system, the user inputs his loan amount, interest rate and tenure. The system calculates the EMI. Point out the problems associated with this design and draw a paper prototype of this page to solve these problems.
SECTION - B

There are FOUR questions in this section. Answer any THREE.

5. (a) Describe eager and lazy initialization of singleton class. :  
Give an example where lazy initialization should be preferred over eager initialization.  
(b) Briefly describe Spiral process model.  
Write down the arguments in favor of and in opposition to Spiral process model.  
(c) Assume that you are trying to implement syntax highlighting in a programming language editor. To perform this, you need to be able to parse different kinds of files such as .c, .cpp, .java, .html etc. All the parsers implement an interface named Parser which contains all the functions required to parse a file. When a file is selected, you will decide which parser to use based on the extension of the file. Now which design pattern should be followed to implement the selection process? Write appropriate java implementation of your solution. [Hint: You don't need to write the parsers. Clearly mention the assumptions you have made.]  
(d) Draw the UML class diagram of "Class Adapter Pattern". Write down the pros and cons of Object Adapter Pattern and Class Adapter Pattern.

6. (a) Write short notes on the following:  
i. Sprint  
ii. Backlog  
iii. Pair Programming  
iv. Code Refactoring  
v. Spike Solution  
(b) Explain how "Extreme Programming (XP)" follows the agility principles.  
(c) Using the following decision tree find out the decision that a project manager should take in order to complete "System X".  
(d) Describe Pareto Principle.  

Contd ............ P/5
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7. (a) Write down the five steps of test-driven development. Demonstrate all the steps sequentially with the help of an example. (5+10=15)

(b) Draw a PERT chart using the durations and dependencies of the tasks shown in the following table. Report the critical path and estimated project completion time. (15)

<table>
<thead>
<tr>
<th>Task</th>
<th>Dependency</th>
<th>Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td>C</td>
<td>A</td>
<td>3</td>
</tr>
<tr>
<td>D</td>
<td>B,C</td>
<td>5</td>
</tr>
<tr>
<td>E</td>
<td>C</td>
<td>1</td>
</tr>
<tr>
<td>F</td>
<td>D</td>
<td>4</td>
</tr>
<tr>
<td>G</td>
<td>E, F</td>
<td>3</td>
</tr>
<tr>
<td>H</td>
<td>G</td>
<td>2</td>
</tr>
<tr>
<td>I</td>
<td>G</td>
<td>2</td>
</tr>
<tr>
<td>J</td>
<td>H, I</td>
<td>5</td>
</tr>
<tr>
<td>K</td>
<td>J</td>
<td>6</td>
</tr>
</tbody>
</table>

(c) Describe how distributed VCS and centralized VCS store all the different versions of a repository? Draw necessary diagrams to describe your answer. (10)

(d) Team A found 342 errors during the software engineering process prior to release. Whereas team B found 184 errors. What additional measures would have to be made for projects A and B to determine which of the teams eliminated errors more efficiently? What metrics would you propose to help in making the determination? (3+3+2/3=6+2/3)

8. (a) Differentiate between the following pairs: (3×5=15)

i. fork vs git clone

ii. git pull vs git fetch

iii. git branch vs git checkout

iv. master vs HEAD

v. Centralized VCS vs Distributed VCS

(b) Draw two diagrams depicting the monolithic and microservice architectural design of a taxi-hailing application project. (Make appropriate assumptions about the functionalities and features of the applications.) (4+4+7=15)

Describe which drawbacks of the monolithic architecture are solved by the microservice architecture.
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(c) Perform function-point analysis using the data in the table given below and estimate the total cost of the project. Assuming that the project adjustment factor is 17, programmers in the organization can complete 18 function point per month, and each programmer charges $5,200 per month for this service.

\[
\text{(10)}
\]

<table>
<thead>
<tr>
<th>Functions</th>
<th>Count per Complexity</th>
<th>Weight By Complexity</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simple</td>
<td>Average</td>
</tr>
<tr>
<td>Inputs</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>Outputs</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>Files</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Inquires</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>Interfaces</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

(d) Which class design principle does the code in figure 8(d) violates? Re-write the code to remove the violation of the principle.

\[
\text{(62/3)}
\]

```java
class GraphicEditor{
    public float getArea(Shapes s){
        if(s.m_type == 1)return s.width*s.width;
        else if(s.m_type == 2)return 3.1416*s.r*s.r;
    }
}

class Shape{
    int m_type;
}

class Rectangle extends Shape{
    int width;
    Rectangle(int width){
        super.m_type = 1;
        this.width = width;
    }
}

class Circle extends Shape{
    int r;
    Circle(int radius){
        super.m_type = 1;
        this.r = radius;
    }
}
```

---

Figure for question 8(d)
1. (a) Does left factoring a grammar helps in removing ambiguity of that grammar? Explain your answer with examples.

(b) James Bond was one of the best spies in the history of British Secret Intelligence Service MI6. MI6 are searching for their next James Bond. To check a candidate potential, MI6 are giving the Flex code named “JamesBondLex.l” (Given in the figure for Question 1(b)) to the candidate to explore. They are asking the candidate to write the contents of a text file named “DecByPotentiaINextJamesBond.txt”, that is produced when the generated scanner from the Flex code is run over the input file named “EncByMI6.txt” (Given in the figure for Question 1(b)).
Now, write down the correct and complete answer that a potential candidate should provide in reply to M16’s tricky (!) question.

(c) Suppose, Kishor is developing a secret complier. He has named it “Tin Goyenda Complier”. He wants to allow the complier to take floating point indexes for arrays. In which step of his development, he has to take care of it?

2. (a) Eliminate left-recursion from the following grammar:

\[
\begin{align*}
K & \rightarrow \text{KungfuPanda} / \text{Kungfu Furious5} / O_w \text{O gway} \\
F & \rightarrow \text{KFT} / \text{KFM} / \text{KFMa} / \text{KFV} / \text{KFC} \\
O_w & \rightarrow \text{KFmasterofmaster} / \text{FKshifumaster} / O_w \text{dragonKF} / \text{warriorKF} \\
P & \rightarrow \text{Po} / \varepsilon \\
T & \rightarrow \text{Tigress} / \varepsilon \\
M & \rightarrow \text{Monkey} \\
M_s & \rightarrow f M_antis \\
V & \rightarrow f Viper \\
C & \rightarrow f Crane
\end{align*}
\]

(b) Whether a lexical analyzer will be able to handle the error in the following C/C++ statement or not? Justify your answer.

\[
f(a == f(a))[a+ = 1;]
\]

(c) “If there is a production \( A \rightarrow \alpha By \) where FIRST(\( y \)) contains \( \varepsilon \), then everything in FOLLOW(A) is in FOLLOW(B).” – Justify this statement using illustrative examples.

3. (a) Consider the following grammar to answer the following questions:

\[
\begin{align*}
T & \rightarrow \text{hreeIdiotsTF} / \text{virus} \\
F & \rightarrow \text{farhanT} / \text{rajuT} / \varepsilon \\
I & \rightarrow \text{rancho}
\end{align*}
\]

(i) Compute the FIRST and FOLLOW of all non-terminals in the given grammar.

(ii) Construct the corresponding LL parsing table.

(iii) State whether the given grammar is suitable to be parsed using the predictive parsing method or not. Use the previously constructed LL parsing table to give your answer. (Assume \( T \) is the starting state of the grammar)
(b) Explain the terms linker and loader. For C/C++ programs, elaborate the relationship of these with the followings: (2x5=10)
   (i) header files
   (ii) macros
   (iii) libraries
(c) Why intermediate code is generated between the front and back end of a compiler? Explain with examples. (5)

4. (a) When does a lexical analyzer use Panic recovery mode? State three other approaches for lexical error-recovery. (4+3=7)
(b) Describe buffer pairs with sentinels? What will be the, maximum length of a lexeme that a lexer can handle if the size of each buffer in the buffer pair is N? Explain with examples. (5+2+5=12)
(c) ‘Bassett Events’ is one of the famous event planning companies of the world. It has two types of managers who organize events in different ways. Managers of first kind have such employees who perform the job only after the managers have given them necessary instructions related to organizing. This type of managers usually hears the whole plan from their clients, discusses with their employees, provides related instructions and then assures the occurrence of the event. On the other hand, second type of managers organize the event step by step listening to their clients, discuss with their employees to check whether it is possible or not and makes the job of that particular step done if it is possible. Now answer the followings. (4+6+6=16)
   (i) Find similarities between these two type of managers with Complier and Interpreter.
   (ii) Give a brief comparison of the compilation and running process of a C, Python and Java program.
   (iii) Give a brief comparison of Compiler and Interpreter in respect to performance and error diagnostic.

SECTION-B

There are FOUR questions in this section. Answer any THREE questions.

5. (a) Write down the general strategy to implement any Syntax Directed Translation Scheme. Illustrate with an example. (10)
(b) What is the difference between parse tree and abstract syntax tree? Write down a Postfix SDT using parser-stack to construct abstract syntax tree for the following context free grammar. The symbols have their usual meaning.

\[
\begin{align*}
S & \rightarrow id \mid \text{E} \mid \text{E}[E] \mid \text{E} \\
E & \rightarrow \text{E} + \text{T} \mid \text{T} \\
T & \rightarrow \text{T} \times \text{F} \mid \text{F} \\
F & \rightarrow \text{id} \mid \text{E} \mid \text{num}
\end{align*}
\]

(c) Convert the following SDD into SDT.

<table>
<thead>
<tr>
<th>Productions</th>
<th>Semantic Rules</th>
</tr>
</thead>
<tbody>
<tr>
<td>S \rightarrow \text{while (B) S}</td>
<td>begin = newlabel()</td>
</tr>
<tr>
<td></td>
<td>B. true = newlabel()</td>
</tr>
<tr>
<td></td>
<td>B. false = S. next</td>
</tr>
<tr>
<td></td>
<td>S. next = begin</td>
</tr>
<tr>
<td></td>
<td>S. code = label (begin)</td>
</tr>
<tr>
<td></td>
<td>//B. code //label (B.true)</td>
</tr>
<tr>
<td></td>
<td>//S. code</td>
</tr>
<tr>
<td></td>
<td>//gen('goto' begin)</td>
</tr>
</tbody>
</table>

(d) Why in L-attributed grammar an inherited attribute associated with a symbol of a production body cannot be defined using any synthesized associated with the head of the production? Explain with example.

6. (a) Draw spaghetti stack interpretation of symbol table for the code snippet. Mention line number in each entry of the spaghetti stack.

```plaintext
1 int a, b;
2 int fun 1(int x, int y){
3     int a, x;
4         int b, y;
5     }
6     int a, x, y;
7     }
8 }
9 { 10 11 int fun 2 (int c, int d){
12     int a, b, c;
13 }
```

(b) Write an attribute grammar that recognizes strings consisting of a, b, c and produces the number of substrings that correspond to the regular expression ab + c in the input string. For example, if the input string is 'abbccacb', then the output will be 2. You can use any arithmetic, bitwise or logical operators in the semantic rules. Show the annotated parse tree for the input string 'abbccacb'.

\[
S \rightarrow S_a \mid S_b \mid \text{Sa} \mid \text{ab} \mid \text{c}
\]
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Contd., Q. No. 6

(c) Briefly explain the difference between static and dynamic scoping. (5)

7. (a) For the following grammar how many conflicts will be reported by yacc/bison? Specify the type of each conflict along with reason of its occurrence.

\[ a \rightarrow b \mid c \mid \text{PLUS} \mid \text{MINUS} \]
\[ b \rightarrow b \ \text{MINUS} \ b \mid \text{PLUS} \]
\[ c \rightarrow c \ \text{PLUS} \ c \mid \text{MINUS} \]

(b) Why left recursive productions are preferred to right recursive productions for shift reduce parsing? Explain with examples. (7)

(c) Determine whether the input strings ‘001001; and ‘001011’ are derived from the following grammar by showing each step of shift/reduce parsing. You have to show the action, contents of the stack and portion of currently considered input at each step. (8+7=15)

\[ S \rightarrow CC, \ C \rightarrow 0 \ C \mid 1 \]

(d) Eliminate left recursion from the following SDT. (5)

\[ A \rightarrow A, Y \{ A.a = g(A, a, Y, y) \} \]
\[ A \rightarrow X \{ A.a = f(X, x) \} \]

8. (a) Write down the semantic rule for translating for loop statement into three address code for the following production. You have three attributes true, false and code associated with the grammar symbol \( B \) and two attributes code and next associated with the grammar symbol \( S \). The symbols have their usual meaning. (10)

\[ S \rightarrow \text{repeat } S \text{ until } B \]

(b) Construct three address code for the expression \( a = -(b + c) + -d \) according to the following SDD. Also show them in triples data structure. (10)

<table>
<thead>
<tr>
<th>PRODUCTION</th>
<th>SEMANTIC RULES</th>
</tr>
</thead>
<tbody>
<tr>
<td>( S \rightarrow \text{id} = E )</td>
<td>( S.\text{code} = E.\text{code} \mid )</td>
</tr>
<tr>
<td></td>
<td>( \text{gen}(\text{top.get(id.lexeme)}) \Rightarrow \text{E addr} )</td>
</tr>
<tr>
<td></td>
<td>( E.\text{addr} = \text{new Temp} () )</td>
</tr>
<tr>
<td>( E \rightarrow E_1 + E_2 )</td>
<td>( E.\text{code} = E_1.\text{code} \mid E_2.\text{code} \mid )</td>
</tr>
<tr>
<td></td>
<td>( \text{gen}(E.\text{addr} \Rightarrow E_1.\text{addr} \Rightarrow \text{E addr} \Rightarrow E_2.\text{addr}) )</td>
</tr>
<tr>
<td>( \mid - E_1 )</td>
<td>( E.\text{addr} = \text{new Temp} () )</td>
</tr>
<tr>
<td></td>
<td>( E.\text{code} = E_1.\text{code} \mid )</td>
</tr>
<tr>
<td></td>
<td>( \text{gen}(E.\text{addr} \Rightarrow \text{minus} \Rightarrow E_1.\text{addr}) )</td>
</tr>
<tr>
<td>( \mid (E_1) )</td>
<td>( E.\addr = E_1.\addr )</td>
</tr>
<tr>
<td></td>
<td>( E.\text{code} = E_1.\text{code} )</td>
</tr>
<tr>
<td></td>
<td>( E.\text{addr} = \text{top.get(id.lexeme)} )</td>
</tr>
<tr>
<td>( \mid \text{id} )</td>
<td>( E.\text{code} = '' )</td>
</tr>
</tbody>
</table>
CSE 309

Contd... Q. No. 8

(c) Write a YACC program which takes a binary number as input and prints the 2's complement of the number. For example, if 1010 is given as input (terminated by new line), then the YACC program will output 0110. You do not need to write the Lex program and should use appropriate token name in your YACC program. Mention the data type associated with semantic values of grammar symbols. You only have to write the middle portion of the YACC program.

(d) Construct the DAG for the expression $x - y + (x - y) \times (x + y)$. 

(10) 

(5)
1. (a) Define bandwidth of a signal. Sketch two time-domain signals such that bandwidth of one signal is greater than the other. Justify your answer using the definition of bandwidth. 

(b) Prove that for a real-time signal, the amplitude spectrum is an even function and the phase spectrum is an odd function.

(c) Let \( \Delta(t) \) represents a triangular pulse as shown in the figure below. The Fourier transform of \( \Delta(t) \) is given as: 
\[
\Delta(t) \Leftrightarrow \frac{\pi}{2} \sin \left( \frac{2\pi f}{4} \right).
\]
Now, using duality property, find the Fourier transform of the time function: \( \text{sinc}^2(t) \) in terms of the function \( \Delta(t) \). Also, draw the spectrum.

(d) Give a proof for why an ideal low pass filter is physically unrealizable.

(e) Consider a Linear Time Invariant (LTI) system that functions as a differentiator, i.e., given a signal \( g(t) \) as input, its output will be \( \frac{d}{dt} g(t) \). Derive and write down the transfer function of the system.

2. (a) List three important advantages digital communication over analog communication.

(b) State and prove Nyquist's sampling theorem. In light of the proof, explain why in practice – (i) a signal is passed through a band-Limiting filter before sampling, and (ii) sampling rate is higher than the Nyquist rate.
(c) Describe how companding achieves non-uniform quantization without actually changing the uniform level spacing in the quantizer. Explain intuitively how a quantizer with companding causes Signal-to-Noise Ratio (SNR) to be independent of input power.  

3. (a) Let $G(f)$ be the Fourier transform of a real-time signal $g(t)$. In discrete Fourier Transform (DFT), we compute $G(f)$ at some finite frequencies from the samples of $g(t)$. Let $g(t)$ be sampled over the duration $0 \leq t \leq T_0$ at uniform intervals of $T_s$ seconds resulting in $N_0$ samples. Then the formula for computing DFT is as follows:

$$G_q = \sum_{n=0}^{N_0-1} g_n e^{-j2\pi q/n}$$

Now answer the following.

(i) Derive the above formula from the expression of $G(f)$.

(ii) Prove that, $f_0 = \frac{1}{T_0}$.

(iii) Compute DFT for the following sample values of $g(t)$. Write down the values of sample frequencies, $f$ and computed values of $G(f)$.

<table>
<thead>
<tr>
<th>$t$</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g(t)$</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
</tr>
</tbody>
</table>

(iv) What considerations should be made while selecting values for $T_s$ and $T_0$? Explain.

(b) How does a good ‘predictor’ design improve the performance of a Differential Pulse Code Modulation (DPCM) system? Explain.

(c) Consider a signal, $m(t) = \text{Acos}(\omega t)$ is input to a Delta Modulation (DM) system. What should be the step size, $E$ such that no slope overload occurs in the system for $m(t)$? How the step size can be made adaptive in a DM system?

4. (a) Give a real life example where Time Division Multiplexing (TDM) is used. Why pulse/bit stuffing may be required in a TDM multiplexer? Explain the difference between positive pulse stuffing and negative pulse stuffing? How does a receiver detect a stuffed bit in each case of positive and negative pulse stuffing?  

(b) Why does ‘Inter-symbol Interference (ISI)’ occur in a digital transmission system? Give an example of a pulse of bandwidth $B$ Hz that can be used to transmit $2B$ pulses per second in presence of ISI. Explain how it works. How such a pulse can be generated using a transversal filter? Explain using a block diagram and necessary illustrations.
CSE 311

SECTION - B

There are FOUR questions in this section. Answer any THREE.

5. (a) Suppose, an AM signal is described by \([A + m(t)] \cos \omega_t\), Where \(A \gg m(t)\). Show that, the message \(m(t)\) can be recovered at the receiver from this AM signal by squaring it and then passing the resulting signal through a low-pass filter.

(b) Explain the necessity of Costas phase-locked loop in the demodulation of DSB-SC signals with a suitable example.

(c) Explain the operation of Costas phase-locked loop with approximate block diagram.

(15) (10) (10)

6. (a) Derive the time domain representation of SSB signal with appropriate figures. Then based on this representation, design a SSB modulation technique using block diagram.

(b) The modulator and demodulator for VSB signal are shown below:

Now derive the required characteristics of the transfer function \(H(f)\) of the sideband shaping filter of modulator with appropriate figures

(15) (20)

7. (a) Derive the bandwidth estimation of WBFM signal with appropriate figures using staircase approximation approach.

(b) Consider a FM signal \(\cos \left( \omega_o t + k \int_{0}^{t} m(\alpha) d\alpha \right)\).

Draw a block diagram showing necessary components to convert the signal into

\(\cos \left( \omega_o t + 3k \int_{0}^{t} m(\alpha) d\alpha \right)\).

And also for each component, clearly mention its function along with corresponding input and output signals.

Contd ........... P/4
8. (a) What is ‘Digital Line Coding’? Describe using examples how digital line coding techniques determine the following characteristics of transmitted signals.
   (i) Bandwidth consumption
   (ii) Power consumption
   (iii) Synchronization Capability
   (iv) DC value suppression capability

   (b) Mathematically prove that a FM modulator can be constructed using a PM modulator. Draw the block diagram of such FM modulator.

   (c) How can we improve the spectral efficiency of amplitude modulation using Quadrature Amplitude Modulation (QAM) technique? Explain with the block diagram of appropriate modulator and demodulator.
1. Consider a CPU which has PC, MAR, MDR, IR, ALU and Instruction Decoder. There are six general purpose registers R0, R1, R2, R3, R4, R5 and a temporary register TEMP inside the CPU. The CPU gets one input directly from the bus and the other input through a register Y. The output of the ALU is sent to the bus through a register Z. The ALU can perform ten arithmetic-logic operations and has a special input for Carry-in.

(a) Draw a block diagram of single bus datapaths inside the CPU following the description above.

(b) Show step-wise control signals for executing the instruction

**Add (R3), R1**

which adds the contents of a memory location pointed to by Register R3 to Register R1. Assume that the instruction is stored in memory and PC contains the address of the instruction.

(c) Design a control word for the CPU above such that the number of bits in the control word is significantly smaller than the number of control signals.

(d) What are the relative merits of horizontal and vertical microinstruction formats?

2. Answer the following questions based on MIPS architecture shown in Figure 1.

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**Figure 1: Figure for Question 2**
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Contd ... Q. No. 2

(a) Write the functions of the control signals ALUSrc, ALUOp, RegDst, MemWrite and RegWrite. (5)

(b) Explain how the ALU control bits are set depending on the ALUOp control bits and the function codes for the R-type instruction. (10)

(c) Describe the datapaths for R-type instructions. (10)

(d) How is the content of the PC updated for the branch (beq) instruction? (5)

(e) What are the two inputs of the MUX at the input of the ALU? (5)

3. (a) What do you mean by the principle of locality of reference? Discuss the role of the principle of locality of reference in designing memory hierarchy. (5)

(b) Answer the following questions for a memory system that uses 32-bit address at the byte level, and a cache that uses a 64-byte line size. (15)

 (i) Assume a direct cache with a tag field in the address of 20 bits. Show the address format and determine the number of addressable units, the number of blocks in main memory, and the number of lines in the cache.

(ii) Assume an associative cache. Show the address format and determine the number of addressable units, the number of blocks in main memory, the number of lines in the cache and the size of the tag.

(iii) Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the number of addressable units, the number of blocks in main memory, the number of lines in a set, the number of sets in the cache, and the number of lines in the cache.

(c) The access time of the cache $M_1$ of a single cache memory system is 6ns/bit during hit and that of the main memory $M_2$ is 900ns/bit during miss. Calculate the block transfer time and the access efficiency of the memory system at the hit ratio of 0.8. (5)

(d) Describe SISD, SIMD and MISD architectures with block diagrams. (10)

4. (a) What are pipeline hazards? Explain a structural pipeline hazard with a time-space diagram. What type of pipeline hazards occurs in the following code segment? How can it be overcome? (10)

```
    lw $t1, 0($t0)
    lw $t2, 4($t0)
    add $t3, $t1,$t2
    sw $t3, 12($t0)
    lw $t4, 8($t0)
    add $t5, $t1,$t4
    sw $t5, 16($t0)
```

Contd ............... P/3
(b) Perform the necessary modification of the single-cycle data path in Figure 2 for pipeline implementation by inserting Pipeline Registers, Forwarding Unit and Hazard Detection Unit. Describe the modification step by step and draw the final modified datapath with all necessary control signals.

(c) Compare the characteristics of typical CISC and RISC architectures.

(d) Consider a bus-based shared memory multiprocessor system. It is constructed using processors with speed of $10^6$ fetches/sec. and a bus with a peak bandwidth of $10^5$ fetches/sec. The caches are designed to support a hit rate of 90%.

(i) What is the maximum number of processors that can be supported by this system?

(ii) What hit rate is needed to support a 20-processor system?

Figure 2: Figure for Question 4(b)
5. (a) “Computer architectures have invented several great ideas in the last 60 years of computer design. These ideas are so powerful that they have lasted long after the first computer that used them, with newer architects demonstrating their admiration by imitating their predecessors.” These ideas include:

(i) Design for Moore’s Law
(ii) Use abstraction to simplify design
(iii) Make the common case faster
(iv) Performance via parallelism
(v) Performance via pipelining
(vi) Performance via prediction
(vii) Hierarchy of memories
(viii) Dependability via redundancy

You are given several design features of MIPS and other modern computing systems in the following. Now, please identify that which of the above great ideas are behind these design decisions.

(i) While implementing instructions at hardware level, it is possible to implement all the instructions as single cycle instructions. However, modern designers do not use this single-cycle design as it is inefficient. (hint: for single cycle implementation, the clock cycle must have the same length for every instruction and the longest instruction determine the clock cycle length.)

(ii) Modern computers use a technique called prefetching. “In prefetching, a block of data is brought into the cache before it is actually referenced. Many microprocessors use hardware prefetching to access the block needed in the future that may be difficult for software to notice”.

(b) Lenovo x3650 M5 server containing a 32 cores (Intel Xeon E5-2699v4) obtained the following results in SPEC test. Find the spec ratio for the computer.

<table>
<thead>
<tr>
<th>Program Name</th>
<th>Execution Time</th>
<th>Reference Time</th>
<th>Spec Ratios</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench</td>
<td>236</td>
<td>9770</td>
<td></td>
</tr>
<tr>
<td>bzip2</td>
<td>375</td>
<td>9650</td>
<td></td>
</tr>
<tr>
<td>gcc</td>
<td>208</td>
<td>8050</td>
<td></td>
</tr>
<tr>
<td>mcf</td>
<td>133</td>
<td>9120</td>
<td></td>
</tr>
<tr>
<td>gobmk</td>
<td>337</td>
<td>10490</td>
<td></td>
</tr>
<tr>
<td>hammer</td>
<td>105</td>
<td>9330</td>
<td></td>
</tr>
<tr>
<td>sjeng</td>
<td>340</td>
<td>12100</td>
<td></td>
</tr>
<tr>
<td>libquantum</td>
<td>2</td>
<td>20720</td>
<td></td>
</tr>
<tr>
<td>h264ref</td>
<td>379</td>
<td>22130</td>
<td></td>
</tr>
<tr>
<td>omnetpp</td>
<td>119</td>
<td>6250</td>
<td></td>
</tr>
<tr>
<td>astar</td>
<td>195</td>
<td>7020</td>
<td></td>
</tr>
<tr>
<td>xalanbmk</td>
<td>86</td>
<td>6900</td>
<td></td>
</tr>
<tr>
<td>Spec ratui (SpecInt2006)</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

Contd .......... P/5
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Contd ... Q. No. 5

(c) Assume a processor with 3 GHz clock rate is executing a program that requires following instructions,

<table>
<thead>
<tr>
<th>Instructions</th>
<th>FP</th>
<th>INT</th>
<th>L/S</th>
<th>BRANCH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction Count ($\times 10^6$)</td>
<td>40</td>
<td>80</td>
<td>90</td>
<td>15</td>
</tr>
<tr>
<td>CPI</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

(i) Calculate the execution time of the program.
(ii) By how much must we improve the CPI of FP instructions if we want the program to run two times faster?
(iii) By how much is the execution time program changed (improved or degraded) if the CPI of INT and FP instruction is increased by 20% and the CPI of L/S and Branch is reduced by 10%?

6. (a) A simple MIPS assembly code snippet and it's corresponding MIPS machine code is given below. Note that, the former one is not complete. Please complete it with appropriate MIPS assembly code.

(b) What support does MIPS instruction set architecture provide for synchronization? Explain with an example.

(c) The following four design principles have been guiding the instruction-set designers to find a balance between the number of instructions needed to execute a program, the number of clock cycles needed by an instruction, and the speed of the clock.

   (i) Simplicity favors regularity
   (ii) Smaller is faster
   (iii) Good design demands good compromise
   (iv) Make the common case faster

- You are given several design features of MIPS instruction-set architecture in the following. Now, please identify that which of the above principles are behind these design decisions.
(i) keeping instruction immediate value in a range of 16-bits
(ii) always requiring three register operands in arithmetic instructions
(iii) using PC-relative addressing for conditional branching
(iv) keeping 32 registers rather than many more
(v) keeping the register fields in the same place in each instruction format

7. (a) Please draw the illustrations of the five MIPS addressing modes. Also give an example instruction for each of the five addressing modes.

(b) Consider the following block diagram of a floating point addition hardware.

- Using the given hardware, simulate the floating addition algorithm by filling up the following tables. The two numbers for addition are, \((-0.25)_{10}\) and \((0.625)_{10}\)

<table>
<thead>
<tr>
<th>Step</th>
<th>Sign</th>
<th>Exponent</th>
<th>Fraction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step1: Exponent Matching</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Step2: Significant Addition</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Step3: Normalization</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Step4: Rounding</td>
<td></td>
<td></td>
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</tbody>
</table>

Contd ........... P/7
8. (a) The following table illustrates the various combinations of two operands for binary addition-subtraction. Please identify the overflow conditions in that table. Then, formulate the overflow boolean variable as a logical function of various input variables (You don’t need to simplify the function).

\[ O \quad S_A \quad S_B \quad S_R \quad V \]

\[
\begin{array}{cccc}
0 & 0 & 0 & 0 \\
0 & 0 & 1 & 1 \\
0 & 1 & 0 & 0 \\
0 & 1 & 1 & 0 \\
1 & 0 & 0 & 0 \\
1 & 0 & 1 & 1 \\
1 & 1 & 0 & 0 \\
1 & 1 & 1 & 1 \\
\end{array}
\]

Here,

\[
\text{Operation, } O = \begin{cases} 
0, & A + B \\
1, & A - B 
\end{cases}
\]

\[
\text{Sign bit of Operand A, } S_A = \begin{cases} 
0, & A \geq 0 \\
1, & A < 0 
\end{cases}
\]

\[
\text{Sign bit of Operand B, } S_B = \begin{cases} 
0, & B \geq 0 \\
1, & B < 0 
\end{cases}
\]

\[
\text{Sign bit of Result R, } S_R = \begin{cases} 
0, & R \geq 0 \\
1, & R < 0 
\end{cases}
\]

\[
\text{Overflow, } V = \begin{cases} 
1, & \text{Overflow occurred} \\
0, & \text{No overflow possible} 
\end{cases}
\]

Contd ………. P/8
(b) In the following figure, a single bus computer architecture was drawn where, various devices like processor, memory, and I/O devices are connected with each other via a single BUS. Please note that, these devices do not operate at a similar rate. Then, how can you redesign this single bus computer architecture so that these devices can interact with each other smoothly using this single bus. Just draw your redesigned single bus computer architecture.

(c) Consider the following multiplication hardware.

-Using the given hardware, simulate the unsigned multiplication algorithm by filling up the following tables for Multiplicand, 0110 and Multiplier, 0110.
<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
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<td>3</td>
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<td>4</td>
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</tbody>
</table>

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