L-2/T-1/CSE **Date: 08/08/2017**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-2/T-1 B. Sc. Engineering Examinations 2015-2016

Sub: **CSE 481** (VLSI design)

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) Briefly describe the behaviors of an NMOS in different regions of operation. **(10)**

(b) I-V Characteristics graph of an ideal 4/2λ NMOS is given in Figure 1(b). (i) Calculate β. (ii) Calculate the value of μCox. (iii) Sketch the curve for V_{gs} = 0.9 V. Clearly show the saturation point, saturation current and voltage as shown. (All the symbols have their usual meanings). **(3+3+4=10)**

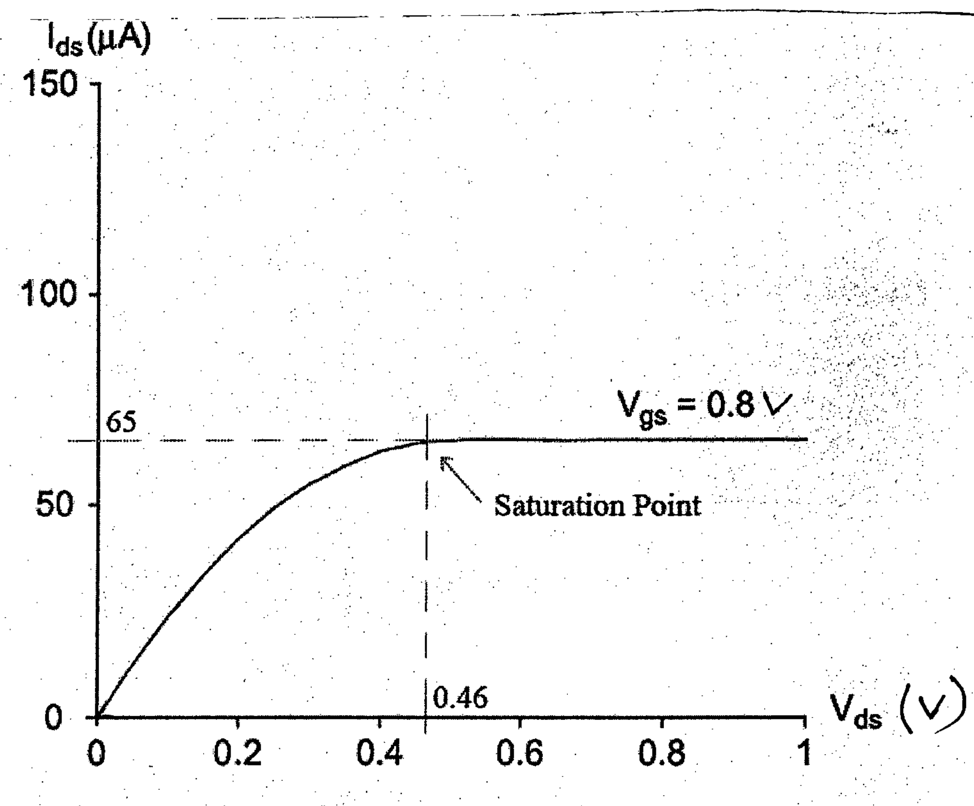

Figure - 1(b)

(c) Derive the ideal I-V characteristic equation for an MOS transistor. **(15)**

2. (a) What are pull-up and pull-down networks in a static CMOS design? Describe with the help of a 3-input NOR gate. **(5+5=10)**

(b) Sketch static CMOS gates for the following inverting functions. **(5+5=10)**

(i) $Y = \overline{A \cdot (B+C) + D \cdot E}$

(ii) $Y = \overline{A + B + C \cdot D \cdot E + F}$

(c) What are the different ways of designing non-inverting functions? Briefly explain with their advantages and disadvantages. **(15)**

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CSE 481

3. (a) What is a fully restored logic gate? Design a full restoring tristate buffer. Describe its working procedure with the truth table. **(2+4+2=10)**

(b) Draw a negative level sensitive D latch and a negative-edge triggered D flip-flop. Explain the difference between them using the timing diagrams. **(5+5=10)**

(c) (i) Explain reserved layer model and unreserved layer model for Detailed routing. **(4+6+5=15)**

(ii) Give examples of 3 layer HVH, VHV and unreserved layer routing models with figures.

(iii) Show the pictorial representation of the following terms: terminal, via, track, branch, trunk, dogleg.

4. (a) Formulate the floorplan design problem as a Mixed Integer Linear Program using the module non-overlapping constraint and dimension constraint. Mention the changes when the rotation of the blocks is allowed. **(10)**

(b) What is the Normalized Polish expression for slicing floorplan? What are the properties of the Normalized Polish expression? Show an example of each property. **(4+6=10)**

(c) Consider "52V134VH6VH" as a normalized polish expression of a floorplan containing six blocks. The heights and widths of each block is given in Figure 4(c). Compute the dimension of the floorplan on the slicing floorplan tree (rotation of the blocks are allowed). **(15)**

Block	Width	Height
1	5	2
2	1	3
3	3	1
4	2	1
5	4	1
6	3	3

Figure – 4(c)

SECTION-B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Formulate the partitioning problem for full custom design style. How would you modify the formulation for the component replication scheme? **(10+5=15)**

(b) Explain the Kernigham-Lin (KL) algorithm with an example. Illustrate the common edge problem for this algorithm and describe how we can solve it. **(5+5=10)**

(c) What problem of the KL algorithm is solved by the Goldberg-Burstein algorithm? Explain with an example how the Goldberg-Burstein algorithm solves this problem. **(4+6=10)**

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6. (a) Provide the pseudo-code and explain the simulated annealing algorithm. **(8+10=18)**

(b) Describe the impact of the initial temperature and temperature decrease function on the result and time requirement of simulated annealing. **(5)**

(c) Provide a table to illustrate the differences between different VLSI design styles (full-custom, standard cell, gate array, FPGA) regarding the area, performance, and fabrication layers. **(12)**

7. (a) Formulate the floorplanning problem. Extend the floorplanning problem for chip planning and pin assignment. **(4+2+4=10)**

(b) Explain slicing floor-planning and slicing tree with an illustrative example. **(5)**

(c) Illustrate the stages of global and detailed routing with a flow chart. **(10)**

(d) Explain 2D and 3D switchboxes with pin locations and their purposes. **(5+5=10)**

8. (a) Explain the grid and channel intersection graph models for global routing with illustrative examples. **(8+8=16)**

(b) Describe Hadlock's mage routing algorithm. What are the time and space complexities of this algorithm? **(7+2=9)**

(c)Discuss how the Acker's coding scheme reduces the memory requirement of Lee's maze routing algorithm. **(5)**

(d) "Hightower's line-probing algorithm will always find a path if one exists." Do you agree with this statement? Explain. **(5)**

L-2/T-1/CSE **Date: 05/08/2017**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-2/T-1 B. Sc. Engineering Examinations 2016-2017

Sub: **MATH 245** (Complex Variable and Statistics)

Full Marks: 210 Time: 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks

Symbols used have their usual meaning.

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) Let $f(z)=u+iv$ be differentiable at a nonzero point $z_0=r_0e^{i\theta_0}$. Show that $f'(z_0)=e^{-i\theta}(u_r+iv_r)=-\frac{i}{z_0}(u_\theta+iv_\theta)$ where $u_r, v_r, u_\theta, v_\theta$ are evaluated at (r_0,θ_0). **(18)**

(b) Find the bilinear transformation which maps the points $z_1=-i, z_2=0$ and $z_3=i$ into $w_1=-1, w_2=i$ and $w_3=1$, respectively. **(12)**

(c) Show that Euler's formula $e^{i\theta}=\cos\theta+i\sin\theta$ continues to hold when θ is replaced by z. **(5)**

2. (a) Show that $Log\left(-1+i\sqrt{3}\right)^2 \neq 2Log\left(-1+i\sqrt{3}\right)$. **(8)**

(b) Solve $\cosh z=-2$ by equating the real and imaginary parts in the equation. **(10)**

(c) Show that $u(x,y)=\frac{1}{2}\log\left(x^2+y^2\right)$ is harmonic in some domain. Hence find a function $v(x,y)$ such that $f(z)=u+iv$ is analytic in that domain. Also, express $f(z)$ in terms of z. **(17)**

3. (a) Use Cauchy's integral formula to evaluate the integral $\int_C \frac{z}{\left(9-z^2\right)(z+i)}dz$, where C is the circle $|z|=2$, taken in the positive sense. **(12)**

(b) Expand $f(z)=\frac{z+1}{z-2}$ in a Taylor series in powers of z and state the region where the expansion is valid. **(8)**

(c) State Laurent's theorem. Find two Laurent series of $f(z)=\frac{1}{(z+1)(z+3)}$ valid in the regions (i) $1<|z|<3$ and (ii) $0<|z+1|<2$. **(15)**

4. (a) Evaluate the integral $\int_C \bar{z}\,dz$ around **(12)**

(i) the circle $|z-2|=3$, and (ii) the ellipse $|z-3|+|z+3|=10$.

(b) Evaluate the following integrals by Cauchy's residue theorem where C is the circle $|z|=3$ taken in the counterclockwise sense: **(23)**

(i) $\int_C \frac{1+z^2}{(z-1)^2(z+2i)}dz$, (ii) $\int_C \frac{\sin z}{z^2\left(z^2+4\right)}dz$ (iii) $\int_C \frac{\sinh z}{z^4}dz$

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SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. Evaluate the following integrals using residues and contours: **(17+18)**

(a) $\int_0^\infty \frac{\cos(3\theta)}{5+4\cos\theta}\, d\theta$ (b) $\int_0^\infty \frac{dx}{(a^2+x^2)^2}$

6. (a) Define Skewness and Kurtosis with classifications. Using moments calculate the coefficients of Skewness and Kurtosis from the following distribution given below and comment on the result obtained. **(17)**

Profits (in Taka)	10-20	20-30	30-40	40-50	50-60
No. of companies	18	20	30	22	10

(b) The following table shows the experience (X) and the performance rating (Y) of 5 persons: **(18)**

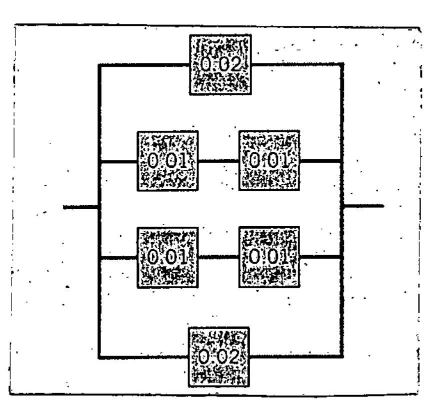
X	16	12	18	4	3
Y	87	88	89	68	58

(i) Fit a linear regression model Y on X.

(ii) Find sum of squares for regression (SSR) and total sum of squares (SST).

(iii) Is the linear model appropriate for given data? Justify your result using coefficient of determination.

7. (a) The following circuit operates if and only if there is a path of functional devices from left to right. Assume that devices fail independently and that the probability of failure of each device is as shown below. What is the probability that the circuit does not operate? **(10)**



MATH 245/CSE

Contd... Q. No. 7

(b) A U-shaped component is to be formed from the three parts A, B, and C. The picture is shown below. The length of A is normally distributed with a mean of 10 millimeters and a standard deviation of 0.1 millimeter. The thickness of parts B and C is normally distributed with a mean of 2 millimeters and a standard deviation of 0.05 millimeter. Assume all dimensions are independent. **(10)**

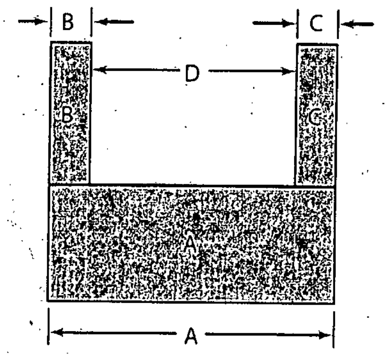


Figure: The U-shaped component.

(i) Determine the mean and standard deviation of the length of the gap D.

(ii) What is the probability that the gap D is less than 5.9 millimeters? (Necessary table attached).

(c) The masses of 1500 ball bearings are normally distributed, with a mean of 22.40 g and a standard deviation of 0.048 g. If 300 random samples of size 36 are drawn from this population, determine the expected mean and standard deviation of the sampling distribution of means if the sampling is done with replacement and without replacement. How many of the random samples would have their means (i) between 22.39 and 22.41 g, (ii) greater than 22.42 g and (iii) less than 22.38 g or more than 22.41 g? (Necessary table attached). **(15)**

8. (a) If X is a binomial random variable with probability distribution $b(x;n,p)$. When $n \to \infty, p \to 0$ and $np \to \mu$ remains constant then prove that $b(x;n,p) \to p(x,\mu)$. In a certain industrial facility accidents occur infrequently. It is known that the probability of an accident on any given day is 0.005 and accidents are independent of each other. What is the probability that **(20)**

(i) in any given period of 400 days there will be an accident on one day and

(ii) There are at most three days with an accident.

(b) A random sample of 100 recorded deaths in Bangladesh during the past year showed an average life span of 61.8 years. Assuming a population standard deviation of 4.9 years, does this seem to indicate that the mean life span today is greater that 60 years? Use a 0.05 level of significance. (Necessary table attached) **(15)**

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Table A.3 (continued) Areas under the Normal Curve

z	.00	.01	.02	.03	.04	.05	.06	.07	.08	.09
0.0	0.5000	0.5040	0.5080	0.5120	0.5160	0.5199	0.5239	0.5279	0.5319	0.5359
0.1	0.5398	0.5438	0.5478	0.5517	0.5557	0.5596	0.5636	0.5675	0.5714	0.5753
0.2	0.5793	0.5832	0.5871	0.5910	0.5948	0.5987	0.6026	0.6064	0.6103	0.6141
0.3	0.6179	0.6217	0.6255	0.6293	0.6331	0.6368	0.6406	0.6443	0.6480	0.6517
0.4	0.6554	0.6591	0.6628	0.6664	0.6700	0.6736	0.6772	0.6808	0.6844	0.6879
0.5	0.6915	0.6950	0.6985	0.7019	0.7054	0.7088	0.7123	0.7157	0.7190	0.7224
0.6	0.7257	0.7291	0.7324	0.7357	0.7389	0.7422	0.7454	0.7486	0.7517	0.7549
0.7	0.7580	0.7611	0.7642	0.7673	0.7704	0.7734	0.7764	0.7794	0.7823	0.7852
0.8	0.7881	0.7910	0.7939	0.7967	0.7995	0.8023	0.8051	0.8078	0.8106	0.8133
0.9	0.8159	0.8186	0.8212	0.8238	0.8264	0.8289	0.8315	0.8340	0.8365	0.8389
1.0	0.8413	0.8438	0.8461	0.8485	0.8508	0.8531	0.8554	0.8577	0.8599	0.8621
1.1	0.8643	0.8665	0.8686	0.8708	0.8729	0.8749	0.8770	0.8790	0.8810	0.8830
1.2	0.8849	0.8869	0.8888	0.8907	0.8925	0.8944	0.8962	0.8980	0.8997	0.9015
1.3	0.9032	0.9049	0.9066	0.9082	0.9099	0.9115	0.9131	0.9147	0.9162	0.9177
1.4	0.9192	0.9207	0.9222	0.9236	0.9251	0.9265	0.9279	0.9292	0.9306	0.9319
1.5	0.9332	0.9345	0.9357	0.9370	0.9382	0.9394	0.9406	0.9418	0.9429	0.9441
1.6	0.9452	0.9463	0.9474	0.9484	0.9495	0.9505	0.9515	0.9525	0.9535	0.9545
1.7	0.9554	0.9564	0.9573	0.9582	0.9591	0.9599	0.9608	0.9616	0.9625	0.9633
1.8	0.9641	0.9649	0.9656	0.9664	0.9671	0.9678	0.9686	0.9693	0.9699	0.9706
1.9	0.9713	0.9719	0.9726	0.9732	0.9738	0.9744	0.9750	0.9756	0.9761	0.9767
2.0	0.9772	0.9778	0.9783	0.9788	0.9793	0.9798	0.9803	0.9808	0.9812	0.9817
2.1	0.9821	0.9826	0.9830	0.9834	0.9838	0.9842	0.9846	0.9850	0.9854	0.9857
2.2	0.9861	0.9864	0.9868	0.9871	0.9875	0.9878	0.9881	0.9884	0.9887	0.9890
2.3	0.9893	0.9896	0.9898	0.9901	0.9904	0.9906	0.9909	0.9911	0.9913	0.9916
2.4	0.9918	0.9920	0.9922	0.9925	0.9927	0.9929	0.9931	0.9932	0.9934	0.9936
2.5	0.9938	0.9940	0.9941	0.9943	0.9945	0.9946	0.9948	0.9949	0.9951	0.9952
2.6	0.9953	0.9955	0.9956	0.9957	0.9959	0.9960	0.9961	0.9962	0.9963	0.9964
2.7	0.9965	0.9966	0.9967	0.9968	0.9969	0.9970	0.9971	0.9972	0.9973	0.9974
2.8	0.9974	0.9975	0.9976	0.9977	0.9977	0.9978	0.9979	0.9979	0.9980	0.9981
2.9	0.9981	0.9982	0.9982	0.9983	0.9984	0.9984	0.9985	0.9985	0.9986	0.9986
3.0	0.9987	0.9987	0.9987	0.9988	0.9988	0.9989	0.9989	0.9989	0.9990	0.9990
3.1	0.9990	0.9991	0.9991	0.9991	0.9992	0.9992	0.9992	0.9992	0.9993	0.9993
3.2	0.9993	0.9993	0.9994	0.9994	0.9994	0.9994	0.9994	0.9995	0.9995	0.9995
3.3	0.9995	0.9995	0.9995	0.9996	0.9996	0.9996	0.9996	0.9996	0.9996	0.9997
3.4	0.9997	0.9997	0.9997	0.9997	0.9997	0.9997	0.9997	0.9997	0.9997	0.9998

Table for question no (7 and 8)

L-2/T-1/CSE **Date: 09/08/2017**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-2/T-1 B. Sc. Engineering Examinations 2016-2017

Sub: **CSE 205** (Digital Logic Design)

Full Marks: 210 Time: 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks.

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) $f(A,B,C,D,E)=\sum(0,1,2,8,9,15,17,21,24,25,27,31)$. Minimize the function f using Q-M method. Find essential prime implicants and prime implicants. **(20)**

(b)Design a negative logic 4 bit parity checker and generator. **(6)**

(c) Using NOR gate solve $p \wedge (q \vee r) \wedge ((p \wedge q) \rightarrow r)$. **(5)**

(d) What is the difference between r's and (r–1)'s complement? (r is the base) **(4)**

2. (a) Using 4 bit adders design a 3 bit multiplier whereas 3 bit variables are $X(X_1, X_2, X_3)$ and $Y(Y_1, Y_2, Y_3)$. Explain the design. **(15)**

(b) Design a circuit which computes A–B and A+B when the circuit inputs are A and B. A and B are of 4 bit BCD value. Explain the design. **(15)**

(c)For a carry look-ahead adder circuit what advantage do we get if we use it instead of a 4 bit simple full adder? For "not" gate with 2 ns propagation delay and other basic gates with 4 ns propagation delay what will be the total propagation delay? **(5)**

3. (a) "A lower order code will get priority" — Design and explain a priority encoder with negative enable for 9 bits. **(10)**

(b) Using only 2 to 4 line decoder solve a function $f(A,B,C,D)=\pi(3,5,9,15,12,4,1)$ 2×4 line decoder has active low enable and outputs are active low. (if gates are required then use the minimum No. of gates) **(10)**

(c) How can be a decoder used as a demultiplexer? Explain with an example. **(5)**

(d) Design and explain a 2 bit magnitude comparator. **(10)**

4. (a) Using k-map solve $f(x_1,x_2,x_3,x_4,x_5)=\sum(0,2,4,5,6,7,8,10,14,17,18,21,29,31)+d\sum(11,20,22)$. Find essential prime implicants. (Show the reduction steps). **(15)**

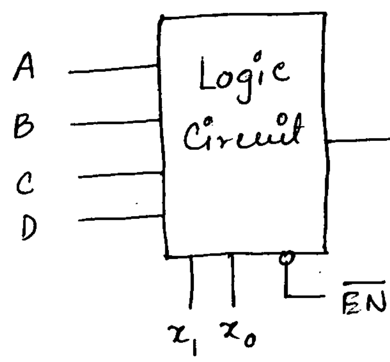
(b) Using only 4 to 1 line 2 bit multiplexers design $f(w,x,y,z)=\pi(2,4,5,7,11,12,13)$. (if gates are required use the minimum number of gates) **(12)**

Contd P/2

CSE 205

Contd... Q. No. 4

(c) Design a Binary to Excess-3 converter using the following logic circuit. **(8)**



If $x_1x_0 = 00$ A's value will go to Y

If $x_1x_0 = 01$ Y will have B's value

If $x_1x_0 = 10$ Y will have C's value

If $x_1x_0 = 11$ Y will have D's value.

SECTION-B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) A sequential circuit has two JK Flip-Flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are: **(4+7+4=15)**

$$J_A = A.x + B.y$$

$$K_A = A.B + x.y$$

$$J_B = A.x$$

$$K_B = A.B.x + B.y$$

$$z = A.x.y + B.x.y$$

For the above mentioned circuit,

(i) Draw the logic diagram of the circuit.

(ii) Derive the state table.

(iii) Draw the state diagram.

(b) Design a clocked sequential circuit that recognizes the input sequence 1010, including overlap such that for input x = 0101010001101001010 0 the corresponding output is z = 00001010000001000010. Design the circuit using T Flip-Flops and basic gates. **(20)**

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6. (a) Draw the logic diagram of a 3-bit universal shift register with mode selection inputs s_2, s_1 and s_0. The register operates according to the following function table: **(15)**

Mode Control			Register Operation
s_2	s_1	s_0	
0	0	0	No change
0	0	1	Invert all bits
0	1	0	Set all bits to 0
0	1	1	Set all bits to 1
1	0	0	Parallel load
1	0	1	Shift left
1	1	0	Shift right
1	1	1	No change

(b) Design a JK Flip-Flop using a T Flip-Flop and basic gates. **(10)**

(c) Design a serial adder that computes the sum of two 4-bit binary numbers A and B stored in individual shift registers. The result of the addition is stored in the shift register representing A. Use sequential logic design procedure to design the serial adder. **(10)**

7. (a) An asynchronous sequential circuit has two internal states and one output. The two excitation functions and one output function describing the circuit are, respectively, **(15)**

$$Y_1 = x_1x_2 + x_1y_2' + x_2'y_1$$

$$Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1$$

$$Z = x_2 + y_1$$

Draw the logic diagram of the circuit and derive the transition table.

(b) Consider the following transition table: **(10)**

y \ x_1x_2	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Design the circuit with NAND SR latches and gates.

(c) What is race condition? Explain different types of races with examples. **(10)**

Contd P/4

CSE 205

4. (a) You are given the following state table of a synchronous sequential circuit. **(12+3=15)**

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	c	0	0
b	d	a	1	0
c	f	f	0	0
d	e	b	1	0
e	g	g	1	0
f	c	c	0	0
g	b	h	1	0
h	h	c	0	0

(i) Find the reduced state table using an implication table.

(ii) Draw the equivalent minimized state diagram.

(b) Design a synchronous counter with the sequence given below: **(10)**

$$1 \rightarrow 4 \rightarrow 5 \rightarrow 7 \rightarrow 2 \rightarrow 1$$

You need not take any measure for the unused states.

(c) A MOD-12 counter counts from 0000 to 1011. Design the MOD-12 ripple counter with positive edge-triggered JK Flip-Flops and basic gates. **(10)**

L-2/T-1/CSE **Date: 16/08/2017**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-2/T-1 B. Sc. Engineering Examinations 2016-2017

Sub: **CSE 203** (Data Structures)

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) Write a function to find the smallest element in a max binary heap. **(5)**

   (b) What is a tree? Write a linear-time algorithm for finding the height of a tree. Analyze the time-complexity of the algorithm. **(10)**

   (c) Compare adjacency matrix and adjacency lists representations of a graph. **(10)**

   (d) Consider the weighted graph G as shown in Figure 1. Then draw the adjacency lists of the weighted graph G. Whenever there is a choice of vertices to explore, always pick the one that is alphabetically first. **(10)**

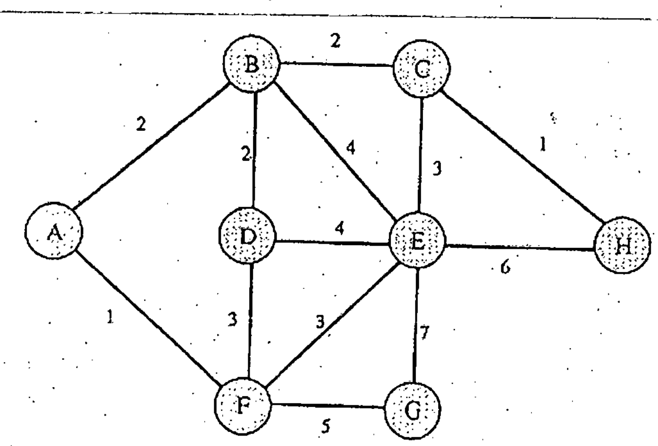


Figure 1: A weighted graph G.

2. (a) Write the differences between a standard queue and a priority queue. Write two functions that implement the Decrease-Key and Increase-Key operations in a Max-heap. **(10)**

   (b) Write an algorithm that sorts the keys of a binary search tree. **(10)**

   Draw the binary search tree that results after successively inserting the keys 43, 34, 48, 59, 65, 73, 88, 81, 92, 79 into an initially empty binary search tree. Also draw a binary search tree of height three using these keys.

   (c) Explain the three cases of the deletion operation in a binary search tree with illustrative examples. **(15)**

CSE 203

3. (a) Given a single linked-list and two integers m and k. Write a function that first finds the node with item value m and then deletes next k nodes from the linked list. **(10)**

(b) Write two procedures for finding the successor element and the predecessor element in a binary-search tree. **(10)**

(c) Write push and pop functions of two stacks that are implemented in a single array. Write the preorder, inorder and postorder traversal sequences of the binary tree whose Euler tour traversal sequence is *a e h i h e a c b f b g b c d j d c a*. Also draw the binary tree. **(15)**

4. (a) Write enqueue and dequeue functions of a FIFO queue that is implemented by a single linked list. **(10)**

(b) Prove that a min binary heap can be built in linear-time. **(10)**

(c) What is an in-place sorting? Write an in-place sorting algorithm. Analyze the worst case and the best case time-complexities of the algorithm. **(15)**

SECTION-B

There are **NINE** questions in this section. Answer any **SEVEN**.

5. (a) Define big O-notation, Ω-notation and Θ-notation. **(6+9)**

(b) Arrange the following functions in ascending order of growth rate. That is, if function $f(n)$ precedes function $g(n)$ in your list, then $f(n)$ should be $O(g(n))$. Provide justifications.

$$f_1 = \sqrt{n},\ f_2 = \log_2 n,\ f_3 = 2^{\sqrt{\log_2 n}},\ f_4 = n!,\ f_5 = n^n,\ f_6 = 2^n$$

6. Suppose you are choosing among the following three (possibly hypothetical) algorithms for multiplying two $n \times n$ matrices: **(15)**

- Algorithm A (Strassen's algorithm) solves the problem by dividing each $n \times n$ matrix into four $n/2 \times n/2$ matrices, makes seven recursive calls to compute intermediate results and then combines them in $\Theta(n^2)$ time to get the result.
- Algorithm B solves the problem by dividing each $n \times n$ matrix into twelve $n/3 \times n/3$ matrices, makes nine recursive calls to compute intermediate results and then combines them in $\Theta(n^2)$ time to get the result.
- Algorithm C solves the problem by first multiplying two $(n-1) \times (n-1)$ matrices, then combining the result with two vectors of size n in time $\Theta(n^2)$.

Determine asymptotic running times of the three algorithms (use the master theorem if applicable). Which one would you choose?

Contd P/3

7. (a) Prove that any comparison based sorting algorithm requires $\Omega(n \log n)$ comparisons in the worst case. **(7+8)**

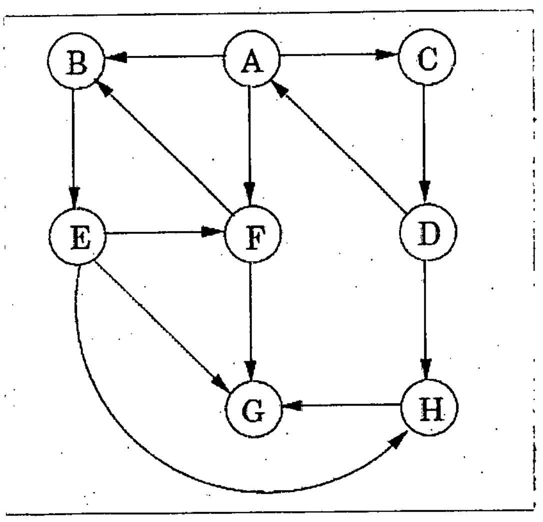
   (b) Describe a sorting algorithm that achieves the above lower bound i.e. runs in $O(n\log n)$ in the worst case.

8. Design linear time algorithms for the following. Briefly describe the ideas (pseudo-code is not needed). **(7+8)**

   (a) Given an undirected graph G and a particular edge $(u\ v)$ in it, determine whether G has a cycle containing $(u\ v)$.

   (b) Given an undirected and unweighted graph G, a particular edge (u,v) and two vertices s and t, determine whether there is a shortest path from s to t containing the edge (u,v).

9. Run depth first search (DFS) on the following graph starting from vertex A and show discovery and finishing times for each vertex as well as edge types. Decompose the graph into strongly connected components (SCCs). **(15)**



10. You are given a set of points by $P = \{p_1, \ldots, p_n\}$, where p_i has coordinates (x_i, y_i) and for two points p_i, $p_j \in P$, we use $d(p_i, p_j)$ to denote the standard Euclidean distance between them. Give an algorithm to find a pair of points p_i, p_j that minimizes $d(p_i, p_j)$ which runs in $O(n\log n)$ time. Justify the running time of your algorithm. **(15)**

11. (a) Huffman's algorithm is used to obtain an encoding of alphabet $\{a, b, c\}$ with frequencies f_a, f_b, and f_c. In each of the following cases, either give an example of frequencies (f_a, f_b, f_c) that would yield the specified code, or explain why the code cannot possibly be obtained (no matter what the frequencies are). **(6+9)**

    (i) Code: $\{0, 10, 11\}$

    (ii) Code: $\{0, 1, 00\}$

    (iii) Code: $\{10, 01, 00\}$.

Contd P/4

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Contd... Q. No. 11

(b) Following is a set of characters and corresponding frequencies:

Character	Frequency
A	24
B	12
C	10
D	8
E	9
F	37

Construct Huffman codes for the characters using the greedy algorithm.

12. Suppose you are given n white and n black dots, lying on a line. The dots are equally spaced but they may appear in any order of black and white (black and white may be interleaved). Design a greedy algorithm to connect each black dot with a (different) white dot so that the total length of wires used to connect the dots is minimal. The length of wire used to connect two dots is equal to their distance along the line. Prove that your algorithm is optimal. **(15)**

●	●	○	●	○	○	○	●
1	2	3	4	5	6	7	8

For example, an optimal solution to solve the above example is (1,3), (2,5), (4,6), (7,8) with total wire length = 2+3+2+1=8.

13. Recall the Weighted Interval Scheduling Problem from class. You are given n intervals with the starting and finishing times of the i-th interval given by s_i and f_i respectively and it is associated with a value v_i. A subset of the intervals is compatible if no two of them overlap in time. The goal is to find a compatible subset of intervals, S to maximize the sum of the values of the selected intervals, $\sum_{i\in S} v_i$. Give a dynamic programming algorithm to solve the problem. Your algorithm (including any pre-processing needed) should run in O($nlogn$) time. **(15)**

L-2/T-2/CSE **Date : 16/07/2017**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-2/T-1 B. Sc. Engineering Examinations 2016-2017

Sub : **EEE 263** (Electronic Devices and Circuits)

Full Marks: 280 Time : 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks.

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) Determine the differential equation solved by the circuit given in Fig. for Q. No. 1: **(21⅔)**

   (i) When the capacitor C is absent.

   (ii) When the capacitor C is present. At what value of C the circuit becomes a non-inverting amplifier?

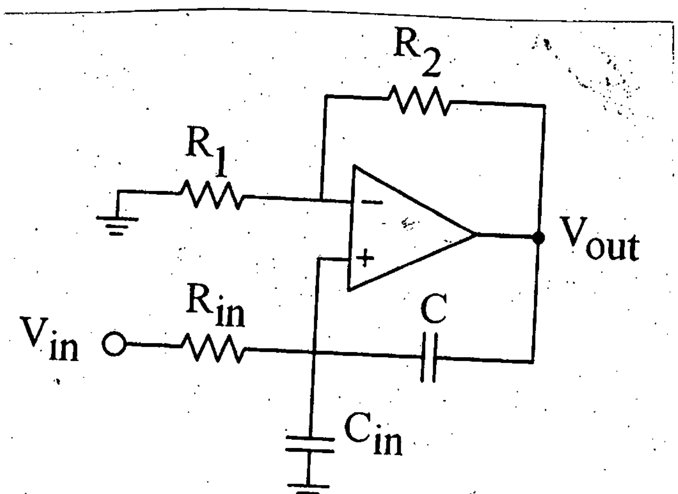


Fig. for Q. No. 1

(b) A circuit is to be designed where depending on the range of input voltage a digital sequence is passed to a computer. The ranges and the corresponding digital sequences are given in Table for Q. No. 1(b). **(25)**

Table for Q. No. 1(b)

Range	Digital Sequence
0–1.2 V	010
1.2 – 3.2 V	110
3.2 – 3.5 V	001
3.5 – 5 V	111

Design a circuit using Op-Amp and Digital Circuits (gates, multiplexers) to perform the task.

Assume a 5 V level to be digital 1 and 0 V level to be digital 0.

Contd P/2

2. (a) Determine the type of filter that is shown in the circuit in Fig. for Q. No. 2(a) by computing the transfer function in frequency domain. **(20)**

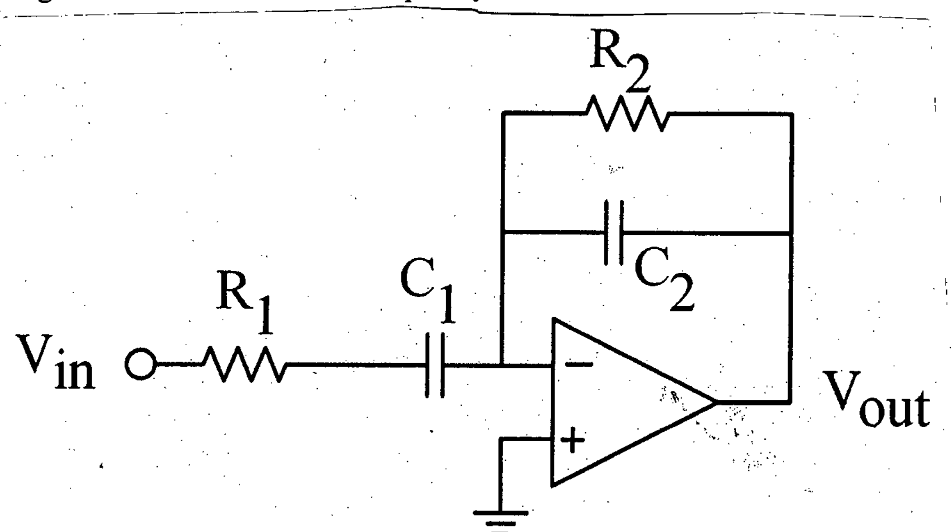


Fig. for Q. No. 2(a)

(b) Determine the Op-Amp circuit that generates the transfer characteristics shown in Fig. for Q. No. 2(b). **(11⅔)**

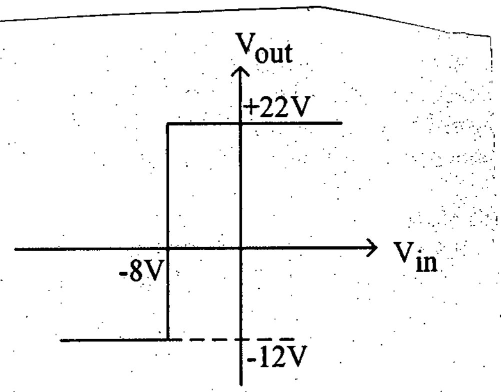


Fig. for Q No. 2(b)

(c) Determine an Op-Amp circuit realization for given input wave shapes V_1 and V_2, and output wave shape V_{out} in Fig. for Q. No. 2(c). **(15)**

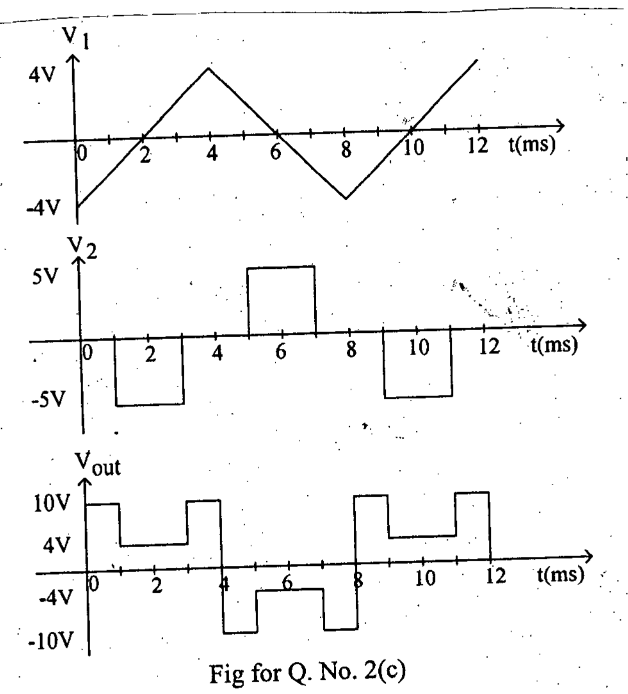
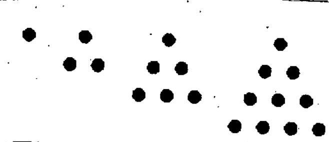


Fig for Q. No. 2(c)

3. (a) Design a 4-bit up counter using T flip flops. It should include a control pin called $\overline{UP}/DOWN$. When $\overline{UP}/DOWN = 0$ the circuit should behave as an up counter and when $\overline{UP}/DOWN = 1$ the circuit should behave as a down counter. The circuit should also have a synchronous active low $\overline{RESET}$ pin. **(20)**

(b) Triangular numbers are sequences that can be formed by continuous summation of the natural numbers. A visual representation of the first four triangular numbers are given in Fig. for Q. No. 3(b). **(11⅔)**



The triangular numbers
1, 3, 6, 10, ...

Fig. for Q. No. 3(b)

Design a simplest possible logic circuit that outputs 1 whenever it detects a 4 bit triangular number.

(c) Show how D Flip Flop and T Flip Flop can be constructed from J-K Flip Flops. **(15)**

4. (a) Show a CMOS implementation of edge triggered D Flip Flops with asynchronous reset. **(25)**

(b) Derive complex gate for the following logic functions: **(21⅔)**

(i) $f(X_1, X_2, X_3, X_4) = \sum m(0,4,6,8,9,15) + D(3,7,11,13)$

(ii) $\bar{f} = (A+B)(C+D)(\bar{A}+B+D)$

Use as few transistors as possible.

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Consider a half-wave peak rectifier fed with a voltage having a triangular waveform with 20 V peak-to-peak amplitude, zero average and 1-kHz frequency. Load resistance R = 100 Ω and the filter capacitor C = 100 μF. Assume that, the diode has a forward voltage drop of 0.7 V when conducting. Find- **(20)**

(i) Average dc output voltage
(ii) Time interval during which the diode conducts
(iii) Average diode current during conduction
(iv) Maximum diode current.

Contd P/4

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Contd... Q. No. 5

(b) For the circuit shown in Fig. for Q. 5(b) find and sketch the voltage transfer characteristics with proper labelling. Utilize the constant-voltage drop model (0.7 V) for each conduction diode. **(13)**

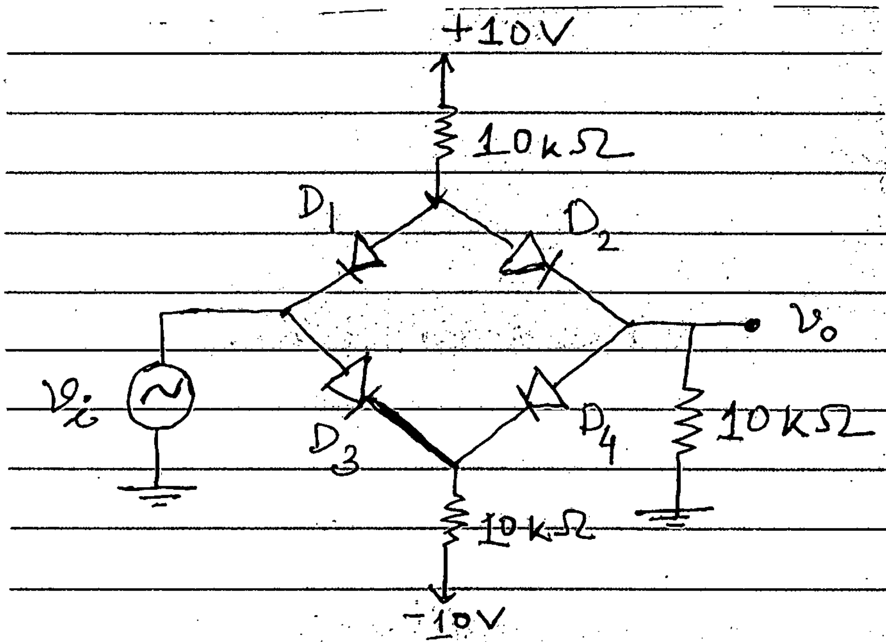

Fig. for Q. 5(b)

(c) For the circuit shown in Fig. for Q. 5(c), plot v_O versus v_i and i_1 versus v_i over the range $-10 \le v_i \le +10$ V. Assume the diodes to be ideal. **(13⅔)**

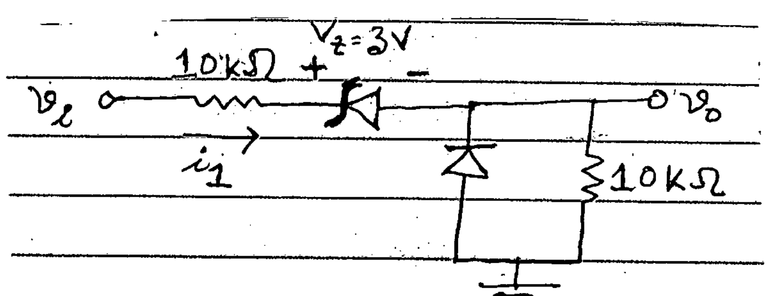

Fig. for Q. 5(c)

6. (a) Draw the voltage transfer characteristics by qualitatively analyzing the circuit shown in Fig. for Q. 6(a). **(15⅔)**

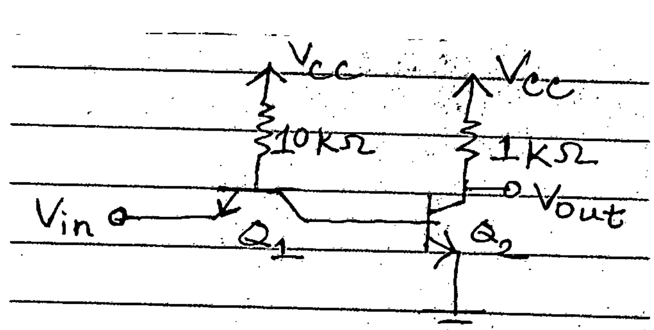

Fig. for Q. 6(a)

Contd P/5

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Contd... Q. No. 6

(b) Find I_C and V_{CE} for the circuit shown in Fig. for Q. 6(b). Assume, $\beta = 100$. **(16)**

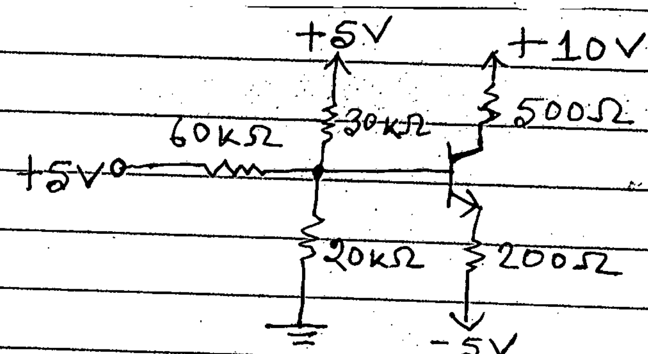

Fig. for Q. 6(b)

(c) Design the circuit shown in Fig. for Q. 6(c) to provide $I_C = 3$ mA and $V_{CE} = 1.5$ V for $\beta = 90$. Use $V_{CC} = 3$ V and a current through R_2 is equal to the base current. **(15)**

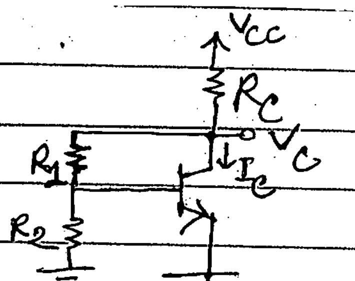

Fig. for Q. 6(c)

7. (a) Consider the circuit shown in Fig. for Q. 7(a). For all the MOSFETs $|V_t| = 1$ V, $\mu_n Cox = 50\ \mu A/V^2$, $L = 1\ \mu m$ and $W = 10\ \mu m$. Find V and I. If Q_3 and Q_4 are made to have W = 100 μm, find out V and I in that case. **(26)**

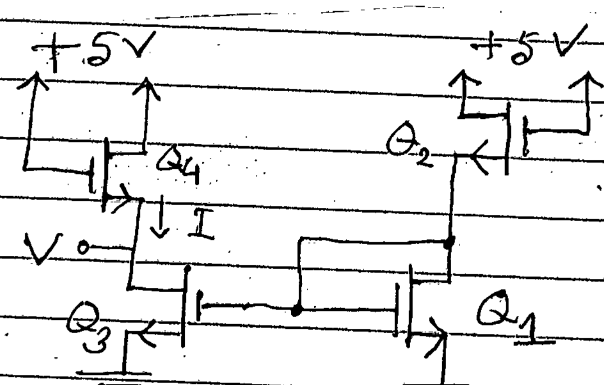

Fig. for Q. 7(a)

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Contd... Q. No. 7

(b) Consider the circuit shown in Fig. for Q. 7(b) with transistor parameters $K_{n_1} = 500$ $\mu A/V^2$, $K_{n_2} = 200$ $\mu A/V^2$, $V_{T_1} = V_{T_2} = 1.2\,V$. Design the circuit such that $I_{D_1} = 0.1\,mA$, $I_{D_2} = 0.3\,mA$, $V_{DS_1} = V_{DS_2} = 5\,V$. **(20⅔)**

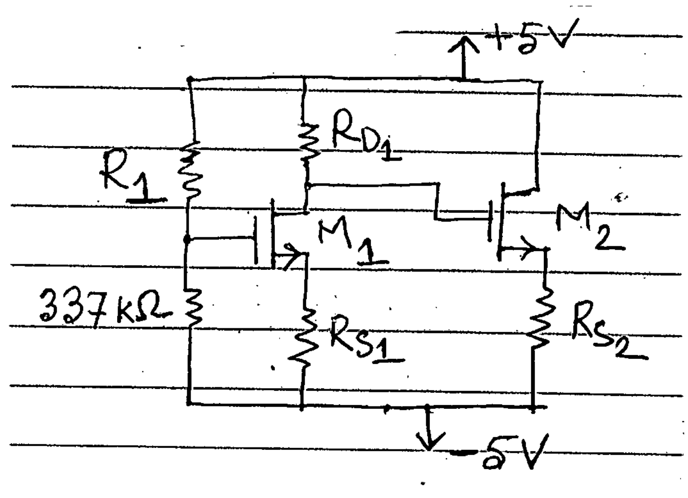

Fig. for Q. 7(b)

8. (a) For the circuit shown in Fig. for Q. 8(a), determine small signal parameters g_m, r_π, and r_e for both the transistors, the overall small signal voltage gain $A_v = \frac{v_0}{v_s}$, input resistance R_{in} and output resistance R_{out}. Here, $\beta = 120$. **(36⅔)**

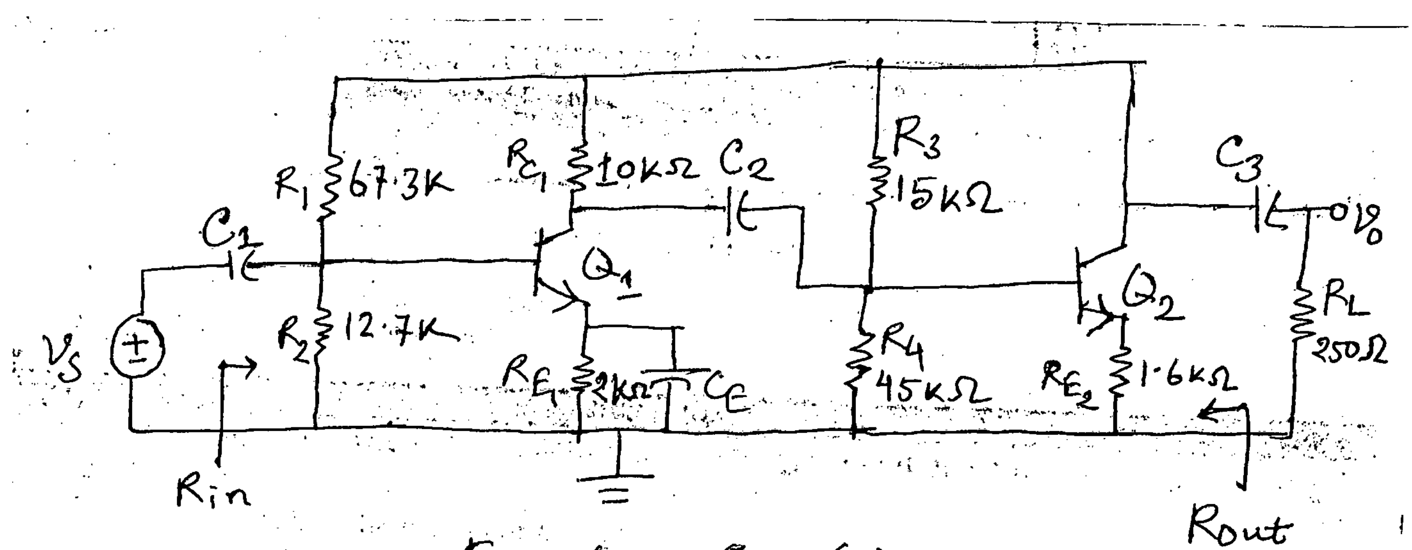

Fig. for Q. 8(a)

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Contd... Q. No. 8

(b) Determine the Boolean expression for V_0 in terms of the four input voltages for the circuit shown in Fig. for Q. 8(b). **(10)**

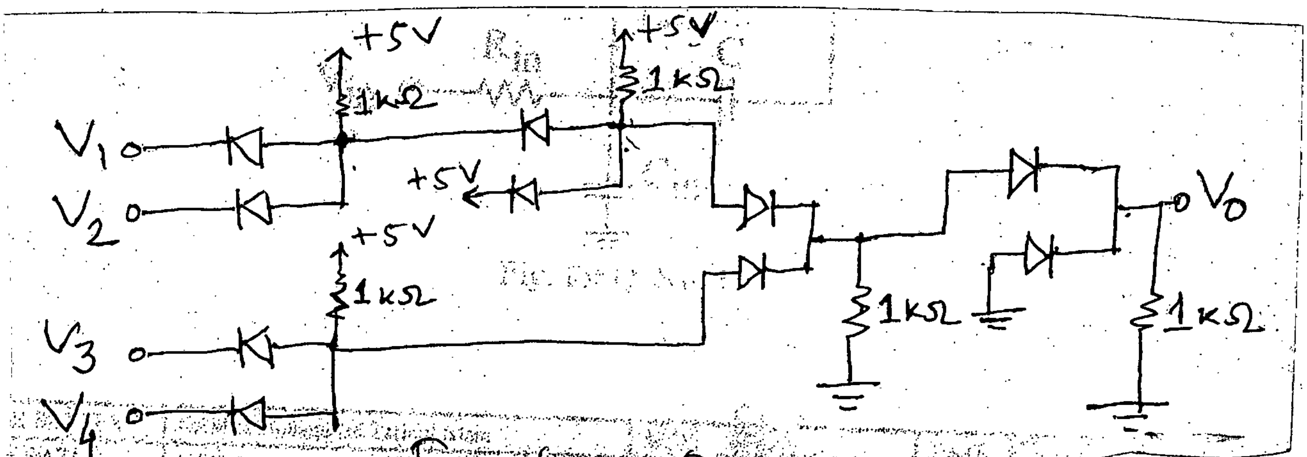

Fig. for Q. 8(b)
