A SIGNAL REFORMING ALGORITHM BASED THREE-PHASE PLL UNDER UNBALANCED AND DISTORTED CONDITIONS IN THE GRID

A thesis submitted in partial fulfillment of the requirement for the degree of

Masters of Science in Electrical and Electronic Engineering

by

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Approval

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It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Acknowledgement

All praise goes to the Almighty for giving me the patience and drive required to complete my M.Sc. research and finish the dissertation in due time.

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Abstract

Fast and accurate estimation of the grid voltage phase angle is crucial for grid synchronization of power converters, flexible AC transmission systems (FACTS) devices, power line conditioners, regenerative drives, uninterrupted power supplies, distributed generations and energy storage systems. Several phase-angle estimation methods, such as- Fourier analysis, frequency locked loop, notch filter, least-error squares, and demodulation, have been developed for phase-angle estimation. Although these methods are accurate at nominal frequency, they require modification of design when the frequency is altered. Synchronous reference frame phase-locked loop (SRF-PLL) is the simplest and the fastest in phase-angle estimation of purely sinusoidal balanced three-phase voltage system. But its accuracy decreases when the system is not balanced or is affected by the presence of harmonics.

In this thesis, a signal reforming algorithm based three-phase phase-locked loop (PLL) has been developed to estimate the phase angles of an unbalanced and harmonics affected three-phase voltage system by combining a harmonics attenuation algorithm, a signal reforming algorithm and the conventional SRF-PLL algorithm into a single PLL system. This technique attenuates the harmonic components from the three-phase signal and then reforms the unbalanced three-phase signal into a balanced one. This makes the conventional synchronous reference frame PLL (SRF-PLL) suited for accurate estimation of the phase angle of one phase. The phase angles of the other two unbalanced phases are also calculated accurately without using additional PLLs. The developed PLL works perfectly even when the frequency of the system is varied. The developed PLL has been tested in MATLAB/Simulink environment for different types of imbalances and distortions. The harmonics attenuation technique is simpler and faster. The signal reforming algorithm is effective in all unbalanced conditions. The developed PLL algorithm not only solves the phase estimation difficulties of the conventional SRF-PLL working under harmonics affected unbalanced grid conditions, but also avoids the use of three single-phase PLLs to estimate the phase angles of a three-phase voltage system.

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List of Abbreviations

Abbreviation	Description
AC	Alternating Current
CBF	Complex Band-pass Filter
DC	Direct Current
DDSRF-PLL	Decoupled DSRF-PLL
DSC-PLL	Delayed Signal Cancellation based PLL
DSOGI-PLL	Dual SOGI-PLL
DSRF-PLL	Double SRF-PLL
DVR	Dynamic Voltage Restoration
EPLL	Enhanced PLL
FACTS	Flexible AC Transmission System
FFPS	Fundamental Frequency Positive Sequence
FIFO	First-In-First-Out
ISC	Instantaneous Symmetrical Component
LPN	Low-Pass Notch
LVRT	Low Voltage Ride Through
OSG	Orthogonal Signal Generator
PI	Proportional Integral
PLL	Phase-Locked Loop
PSC	Positive Sequence Calculation

Abbreviation	Description
PV	Photo Voltaic
PWM	Pulse-Width Modulation
SOGI	Second-Order Generalized Integrator
SRF	Synchronous Reference Frame
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
UPS	Uninterrupted Power Supply
VCO	Voltage-Controlled Oscillator

List of Symbols

Symbol	Nomenclature
v_a, v_b, v_c	Instantaneous voltage of the *a*, *b*, and *c* phase respectively
v_{a1}, v_{b1}, v_{c1}	Maximum amplitude of v_a, v_b, v_c respectively
v_a^R, v_b^R, v_c^R	Reformed instantaneous voltage of the *a*, *b*, and *c* phase respectively
v_α, v_β	Voltage components on α-β orthogonal axis respectively
v_d, v_q	Direct axis and quadrature axis voltage components
A, B, q, c	Multiplication factors
t	Time
ω_o	Nominal value of the grid voltage fundamental frequency
ω_{vco}	Free running frequency of the Voltage Controlled Oscillator
$\Delta\omega$	Fundamental frequency deviation from nominal value
ω_i	Angular frequency of the input
ω_e	Estimated value of the grid voltage fundamental frequency
φ_o	Phase of the signal at nominal frequency
φ_e	Phase error
θ	Phase-angle of the grid voltage
$\Delta\theta_1$	Phase-angle deviation from the balanced phase-angle between phase *a* and phase *b*
$\Delta\theta_2$	Phase-angle deviation from the balanced phase-angle between phase *a* and phase *c*

Symbol	Nomenclature
$e_o(t)$	Phase error signal
T	Combined transfer function of Clarke and Park transformation
$H(s)$	Transfer function of the loop filter of the PLL
K	Gain parameter of the loop filter
K_p	Proportional gain of the loop filter
K_i	Integral gain of the loop filter
h	Order of the harmonics
h_{max}	Maximum order of the harmonic component prevailing at the voltage signal
N	Sampling index
T_s	Sampling period
v_a^k	Voltage signal of the *a* phase after *k-th* stage of filtering
$a_1{}^k$	Amplitude of the fundamental component of the voltage signal at *a* phase after *k-th* stage of filtering
$a_h{}^k$	Amplitude of the *h-th* harmonic component of the voltage signal at *a* phase after *k-th* stage of filtering
$v_a{}^{k''}$	Double derivative of the voltage signal of the *a* phase after *k-th* stage of filtering
$H_{h_{max}}(z)$	Transfer function of a unit block of the harmonic attenuation system in *z*-domain to eliminate h^{th} harmonics.
G	Gain constant of the unit block of harmonic attenuation system

Symbol	Nomenclature
$H(z)$	Transfer function of the harmonic attenuation system in *z*-domain.
x_{b1} , x_{b2}	Amplitudes of the reformed voltage of the *b*-phase calculated from the solution of quadratic equations
x_{c1} , x_{c2}	Amplitudes of the reformed voltage of the *c*-phase calculated from the solution of quadratic equations
e_1, e_2, e_3, e_4	Error values of the sum of derived solution voltages of the three phases

This chapter starts by presenting the importance on phase-angle estimation in Section 1.1. Technical reviews of relevant works have been introduced in Section 1.2. Section 1.3 contains the objectives of this thesis work. The methodologies and the tools used for the research work have been presented in Section 1.4. Section 1.5 consists of the contribution of the research work and list of publications obtained from the thesis. Finally, the outline of the thesis is described in Section 1.6.

1.1 Importance of Phase-Angle Estimation

The power system can be easily affected by the addition of non-linear loads [1]-[2]. The positive-sequence fundamental phase-angle of the utility voltage is a critical piece of information for the devices that are used in the operation of power conversion and conditioning applications. Hence, they need an accurate phase estimation scheme to work properly. The phase-angle information is often used to construct a reference carrier wave to synchronize the on/off commutations of power devices, calculate and control the flow of active/reactive power or transform the feedback variables to a reference frame suitable for control purpose.

Fast and accurate phase angle estimation is essential for the control of grid-connected power converters [3]-[6], flexible AC transmission systems (FACTS) [7]-[9], power line conditioners [10]-[12], regenerative drives [13]-[14], active power filters [15]-[16], uninterrupted power supplies [17]-[18], distributed generations [19]-[21] and energy storage systems [22]. The detected information of such a fundamental component, either in magnitude and phase angle or as a vector of the grid voltage and fundamental frequency, is used for the synchronization of converter output variables, for power flux calculations, and for the transformation of state variables into rotating frames.

Grid connected power converters convert DC current into AC current and provide real and reactive power to the grid [4],[6]. To calculate the amount of real power and reactive power to be injected into the power-grid by the power converters, the information on phase-angles of the phases of the power-system is required.

A power line conditioner improves the quality of the power that is delivered to electrical load/ equipment by refining the input signal and removing noise from the signal [11]. The information on the phase-angle of the signal is required in this regard.

In UPS system, it is necessary to guarantee proper synchronization between the inverter output voltage and the primary source voltage [18]. In parallel redundant UPS arrangements, a very precise synchronization is also required prior to each UPS connection to the protected bus in order to avoid catastrophic transients.

For applications involving load compensation, the DC to AC converter of the STATCOM is manipulated as a controlled current source [23]-[24]. The phase-angle information is required either to generate the reference current template or to synchronize the PWM voltage waveform with that of the utility.

Distributed generation system mainly includes wind and PV systems. These systems have some requirements and restrictions under faulty conditions in order to remain connected to the network. Such requirement are known as Low Voltage Ride Through (LVRT) [25]-[26]. Solutions based on the installation of STATCOMs and DVRs, as well as on advanced control functionalities for the existing power converters of distributed generation plants, have contributed to enhance their response under faulty and distorted scenarios and, hence, to fulfill these requirements. In order to achieve satisfactory results with such systems, it is necessary to count on accurate and fast grid voltage synchronization algorithm.

Weak, variable-frequency power system exists in small distributed generation island and in isolated mobile power systems [27]-[28]. Typically, multiple generators are attached to an AC bus and synchronized using phase detector that estimated the approximate system frequency and phase. Methods of synchronization similar to those used for generators are also applied to parallel power converters that are powered from DC sources. These AC power converters inherently rely heavily on phase detection to achieve and maintain synchronism since they do not have physical rotating inductance.

In all these applications, in order to maintain proper operation, the information on amplitude and phase-angle has to be obtained as fast and accurate as possible, which is even more challenging in the presence of disturbance in the utility voltage.

1.2 Literature Review

With the increasing applications of numerous grid-connected systems, phase-angle estimation has become a crucial aspect. A large number of researches have been conducted in this field, producing different techniques and methods.

Several open-loop based grid synchronization techniques are reported in the technical literature [29]-[32]. Some advanced techniques are based on Fourier transformation [10], [33], frequency locked loop [34]-[36], least-error squares [37]-[38], weighted least-square-estimation [39]-[41], notch filter [42]-[43], extended Kalman filter [44]-[46] and space vector filtering [47]-[48] etc. These techniques perform satisfactorily when the grid frequency is close to the nominal value. However, as the input frequency shifts, the deviation of frequency will deteriorate the performance of these techniques. Though, improvements are introduced and employed, the increase of dynamic recovery time and the too much computational complexity is always inevitable. A novel Fourier transformation based grid-synchronization method has been proposed in [10]. The grid phase-angle can be estimated properly and effectively by combining a frequency detector, a reference signal generator and a low-pass notch (LPN) filter. But when the grid frequency shifts, the LPN filter is to be modified accordingly. To incorporate with the adaptive regulation, a cascaded series of fourth-order LPN filters is needed, which is a complex system for grid synchronization and also requires very powerful processors.

Instead of open-loop based techniques, the closed-loop based phase-locked loops (PLL) are more preferable. Closed-loop based PLLs are the most widespread grid synchronization algorithms due to their simplicity and flexibility. Numerous PLLs have been proposed and developed. The basic scheme used in three-phase systems is the Synchronous Rotating Frame PLL (SRF-PLL) [49]–[55]. In SRF-PLL, the three-phase grid voltage is first transformed into synchronous rotating frame as direct axis and quadrature axis voltage component and then the phase-angle is estimated by feeding back and regulating the quadrature axis voltage component to zero. Under ideal sinusoidal grid conditions, the SRF-PLL performs effectively at a very high bandwidth, providing rapid and accurate phase angle estimation. However, if the input signal is distorted by three phase imbalances or harmonics, the bandwidth of the SRF-PLL needs to be reduced to perform proper filtering. Specially, to cancel the fundamental negative sequence from imbalances, which acts as a second order component and is located at the low frequency segment of v_q, the bandwidth should be dramatically reduced further to generate an acceptable result [62]-[65].

Advanced PLL schemes have been developed to achieve better performance. Most of these have been developed to extract the fundamental positive sequence from the primary voltage signal. In [62] and [63], double-SRF-PLL (DSRF-PLL) and decoupled DSRF-PLL (DDSRF-PLL) have been presented. The DDSRF-PLL applies two rotating synchronous reference frame, which have the same angular speed but in opposite directions for the rotation transformation and then a decoupling network is designed to extract the fundamental positive sequence of the grid voltage. SRF-PLL with a sinusoidal signal integrator have been proposed in [64] and a double second-order generalized integrator based PLL is proposed in [65]. These advanced PLLs have filtering stages within or before the control loop of SRF-PLL. Although, they exhibit excellent performances, these algorithms have too much computational complexity. Delayed signal cancellation based PLL (DSC-PLL) is documented in [66]-[70] to eliminate the negative-sequence component in unbalanced grids and also to cancel any given harmonics, but improper sampling rate or frequency shift of the system can result in error during estimation and also multiple digital signal processors are required to implement these complex algorithms.

Another important issue for the closed-loop based PLLs is system modeling. The scheme of advanced PLLs mostly put a specific filtering stage within or before the control loop of SRF-PLL, named in-loop filtering and pre-filtering. System modeling is always essential to design the filtering stage and to evaluate the performance of these PLLs. According to the reference frame, the system modeling can be carried out under natural (*abc*), stationary ($\alpha\beta$) and synchronous (*dq*) reference frames. Modeling of these pre-filtering type PLLs mostly assume that the pre-filtering stage and the SRF-PLL as two independent entity. To improve the dynamic performance of these two segments, in [71] the author has developed an efficient approach to design the control parameters combining the SRF-PLL and the pre-filtering stage in a single entity. As to the in-loop filtering types, where the filtering stage is integrated, they are modeled as an entity.

A design oriented study of advanced SRF based in-loop filtering type PLLs has been demonstrated in [72]. Several PLLs are modeled and analyzed in detail, after which parameter design guidelines are provided. Similarly, on basis of system modeling, performance analysis and design guidelines of moving average filter based PLLs are illustrated in [73]. A PLL method consisting of a cascaded interconnection of two PLL schemes, named UH-PLL and conventional SRF-PLL is documented in [74]. A solution to eliminate the negative sequences of the three-phase unbalanced voltage waveforms is presented in [56]. It reforms the

unbalanced three-phase voltage system into a balanced one when only amplitudes are unbalanced. However, both the amplitude and phase imbalances may occur under unsymmetrical fault conditions [75]-[85] and the reported techniques are not suitable for accurate phase estimation in these conditions.

The presence of harmonics in grid-voltage is a major cause for inaccurate phase-angle estimation. Depending upon the phase-angle or frequency detection algorithm, harmonics are either completely eliminated or sufficiently attenuated. The use of active and passive low-pass filters are the conventional means of harmonics elimination. Several active filters [86]-[89] and passive filters [90]-[93] have been proposed for grid-connected converters and micro-grids to compensate for harmonics. But these filters will cause phase-delay of signal which is also dependent on the system frequency. Hence, these types of filters are not suitable for phase-angle or frequency estimation of harmonics affected signals. In [94], a delta-connected filtering winding has been used for harmonic elimination. An adaptive delay bank filter has been proposed in [95] for SRF-PLL. In [96], a PI controller based shunt active filter has been claimed useful for harmonic elimination. These filters cause phase-shift of their input signals. For accurate phase-angle detection under harmonic affected condition, it is necessary to develop a suitable algorithm to either eliminate or attenuate the harmonic components before they are processed for phase-angle estimation.

1.3 Objectives of the Thesis

The primary objective of this thesis is develop a new PLL algorithm based on three-phase SRF-PLL under the amplitude and phase imbalances in the three-phase grid voltage including harmonics. A conventional SRF-PLL is not able to estimate the phase-angle accurately if any form of distortion and imbalance is present. This thesis aims at increasing the over-all performance under such circumstances.

This thesis aims at developing a signal reforming algorithm that can reform the three-phase unbalanced grid-signal with amplitude and phase imbalances into the three-phase balanced signal without discarding the information on amplitude and phase-angle of the original voltage signal. By reforming the unbalanced signal into a balanced one, the reformed signal can be made suitable for ordinary SRF-PLL.

The thesis also aims at developing a relatively simple algorithm for harmonics attenuation suitable for the SRF-PLL. Use of traditional filter for harmonics elimination alters the phase-angle of the filtered signal, which causes error in phase-angle estimation. On the other hand, if it is possible to reduce the amount of harmonics without altering the phase-angle, it can assist the signal reforming algorithm. Hence, it has become another objective of this thesis.

In a summary, this thesis aims at improving the performance of the three-phase PLL by developing a signal reforming and a harmonics attenuating algorithm and combining them with a conventional SRF-PLL.

1.4 Thesis Methodology

The thesis has been conducted by following a step by step set of methodologies. At first, a three-phase SRF-PLL has been developed in MATLAB/Simulink environment. Then, the frequency adaptive harmonics attenuation algorithm has been mathematically developed and implemented to reject the negative effects caused by the harmonics. The IEEE standard 519-2014 [97] has been followed for setting up the specification for the harmonics. European standard EN50160 [98] has also been followed for some cases. The signal reforming algorithm has been mathematically derived and simulated to obtain a balanced three-phase voltage system from an unbalanced one. The phase angle imbalance information between two phases has also been extracted using this algorithm. The phase detector of the PLL has been implemented based on the Clark and Park transformations [99]. A proportional and integral controller has been used as the loop filter. The fundamental frequency obtained from the output of the loop filter has been integrated to obtain the phase angle of the reference phase voltage. One sine and one cosine function have been used as the oscillators. The performance of the PLL has been investigated under different grid events such as voltage sag, voltage swell, frequency step, frequency jump, phase jump etc. The outputs at different stages of the PLL have been measured and error analyses have been performed. A conventional SRF-PLL reported in the technical literature has also been developed and the performance of it has been compared with the developed one.

1.5 List of Publications

The contributions of this research work have been published in peer reviewed international conferences. The list of these papers is as follows-

[1] F. Sadeque, M. S. Reza and M. M. Hossain, "A signal reforming algorithm based three-phase PLL under unbalanced grid conditions", in *Proceedings of IEEE International Conference on Renewable Energy Research and Applications* (*ICRERA*), Birmingham, UK, 20-23 November, 2016, pp. 940-945.

[2] F. Sadeque, M. S. Reza and M. M. Hossain, "Three-phase phase-locked loop for grid voltage phase estimation under unbalanced and distorted conditions", in *Proceedings of IEEE Power and Energy Conference at Illinois* (*PECI*), Illinois, USA, 23-24 February, 2017, pp. 1-7.

1.6 Thesis Organization

The thesis entitled, 'A Signal Reforming Algorithm Based Three-Phase PLL under Unbalanced and Distorted Conditions in the Grid', is organized as follows-

Chapter 1 introduces the necessity of phase angle estimation in the field of power system analysis and grid synchronization by presenting its significant contribution in numerous power system devices and utilities. The chapter also discusses some widely used and conventional means of phase-angle estimation introduced in different research works. Finally, it briefly discusses the objective of this thesis and the methodologies that have been carried out.

Chapter 2 starts with the basic principle of phase-locked loop. Then, it briefly discusses on several PLL algorithms that are commonly used. A detailed discussion on conventional three-phase SRF-PLL has also been introduced here. Some simulation results have been provided here to demonstrate the performance of this PLL under different grid circumstances.

Chapter 3 contains the detailed analysis of the developed PLL. The analysis includes basic design of the PLL structure, signal reforming and harmonics attenuation algorithm and the selection of proportional and integral gain parameters.

Chapter 4 provides the simulation results to support the accuracy, efficiency and robustness of the developed PLL under different adverse grid voltage conditions.

Chapter 5 concludes the thesis work by summarizing the achievement from this thesis work and providing suggestion on future work.

This chapter starts with the basic structure of phase-locked loop in Section 2.1. In Section 2.2 some commonly used single-phase and three-phase PLL algorithms have been discussed. The basic structure and working principle of the conventional three-phase SRF-PLL has been elaborately described and its performance under various circumstances have been demonstrated in Section 2.3.

2.1 The Basic Structure of Phase-Locked Loop

The Phase-locked loop (PLL) is one of the most efficient techniques for tracking phase-angle and frequency of a signal. It is widely used in power system devices and communication devices for phase-angle and frequency estimation. A PLL has three basic components-

- A voltage-controlled oscillator (VCO),
- A multiplier serving as phase detector or phase comparator, and
- A loop filter

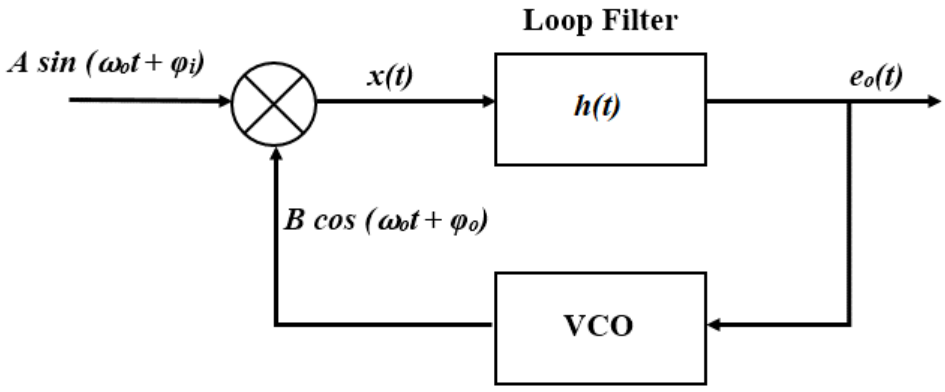

Figure 2.1: Block diagram of a Phase-Locked Loop.

Fig. 2.1 shows the block diagram of a typical PLL [100]. The operation of the PLL is similar to that of a feedback system. The signal fed back tends to follow the input signal. If the signal fed back is not equal to the input signal, a difference, known as error, will change the signal fed back until it is close to the input signal. In a PLL, the phase angle is fed back and compared

with the input signal. The VCO adjusts its own frequency until it is equal to that of the input signal. At that point, the frequency and the phase of the input and output signals are in synchronism, with or without a constant phase difference.

The voltage-controlled oscillator is an oscillator whose frequency can be controlled by an external voltage. In a VCO, the oscillation frequency varies linearly with the input voltage. If a VCO input voltage is $e_o(t)$, its output is a sinusoid of frequency ω given by,

$$\omega(t) = \omega_{vco} + ce_o(t) \tag{1}$$

where, c is a constant of the VCO and ω_{vco} is the free-running frequency of the VCO. The multiplier output is further low-pass-filtered by the loop filter and then applied to the input of VCO. This voltage changes the frequency of the oscillator and keeps the loop locked.

Let the input signal to the PLL be $Asin(\omega_o t + \varphi_i)$, and let the VCO output be a sinusoid $Bcos(\omega_o t + \varphi_o)$. The multiplier output $x(t)$ is given by,

$$x(t) = ABsin(\omega_o t + \varphi_i)\cos(\omega_o t + \varphi_o) \tag{2}$$

$$x(t) = \frac{AB}{2}\sin(\varphi_i - \varphi_o) + \frac{AB}{2}\sin(2\omega_o t + \varphi_i + \varphi_o) \tag{3}$$

$$e_o = \frac{AB}{2}\sin(\varphi_i - \varphi_o) \tag{4}$$

The last term on the right-hand side of (3) is suppressed by the loop filter of the PLL. Hence the other term is the value of e_o, which is an input to the VCO, where $(\varphi_i - \varphi_o)$ is the phase error, φ_e. This phase error governs the locking of the two signals. The PLL tracks the input sinusoid and when the phase error is 0, the PLL is said to have locked the input signal and the output of VCO. The frequency and the phase angle can be directly derived from the output [101]-[103].

2.2 Commonly Used PLL Algorithms

Phase-Lock Loops are the most widely used algorithms for phase-angle and frequency estimation. Due to its increased popularity for fast operation, reliability and accuracy, numerous PLL algorithms have been developed. These PLLs can be categorized into two groups – single-phase PLLs and three-phase PLLs. Some commonly used PLL algorithms developed for power system parameter estimation are follows-

2.2.1: Single-Phase Inverse Park PLL

Single phase inverse park PLL [104] is the most efficient phase-angle detection PLL algorithm. Fig. 2.2 shows the block diagram of a single phase PLL. The single phase inverse Park PLL transforms a voltage signal into two orthogonal components, commonly knowns as alpha-beta (α-β) transformation on a stationary reference frame. The task is performed by the Orthogonal Signal Generator (OSG) block.

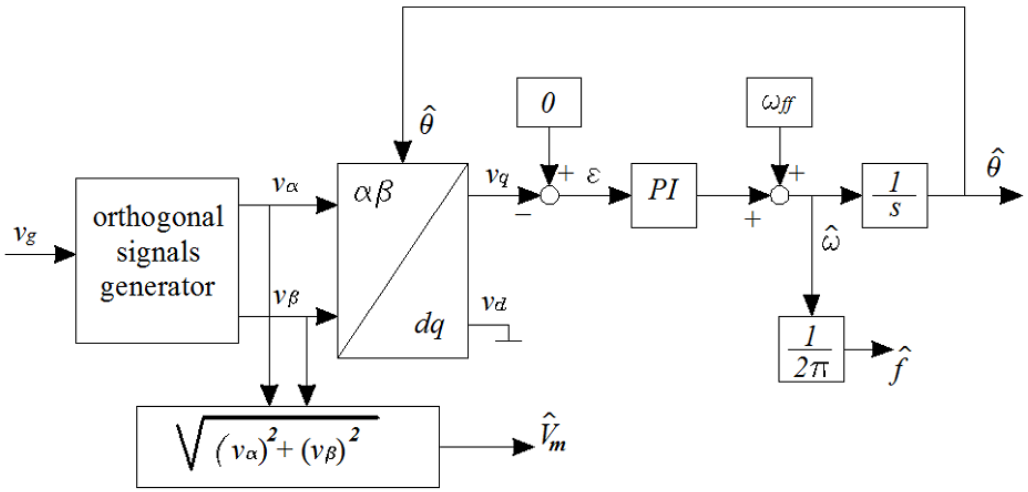

Figure 2.2: Block diagram of a single-phase PLL.

For the input signal v_g, the orthogonal components are,

$$v_\alpha = v_g sin\theta;\ v_\beta = v_g cos\theta \tag{5}$$

where, $\theta = \omega_o t + \varphi_o$ is the phase-angle and ω_o is the nominal angular frequency.

Then Park transformation [105] is applied on it to convert the stationary reference frame to a rotating reference frame. The direct axis (*d*) or quadrature axis (*q*) is then fed to a Proportional and Integral (PI) controller having a reference of zero. The PI controller output is integrated to get the estimated instantaneous phase-angle for the PLL output signal. The estimated phase angle gets synchronized with the instantaneous phase-angle of the utility grid once the *q* axis component is driven to zero.

There are various method to design the loop PI filter. The second-order loop is commonly used as good trade-off between the filter performance and the system stability. A filter with lower value of bandwidth produces a longer synchronization time. On the other hand, with a higher value of bandwidth, the filter is able to synchronize quickly, but with a possibility of distortions being added.

Although the single-phase PLL is accurate in phase-angle estimation, its algorithm is quite complex. Specially, the orthogonal signal generator require the use of transport delay to introduce a phase shift of 90 degree with respect to the fundamental frequency, which is a difficult to develop.

2.2.2: Single-Phase Second Order Generalized Integrator Based PLL

The structure of Second Order Generalized Integrator (SOGI) based PLL [106] differs from the Inverse Park based PLL in the way the orthogonal signal is produced. Fig. 2.3 shows the diagram of a single-phase SOGI based PLL. It has a simple structure based on the use of a double integrator and requires not only the grid voltage but also an angular frequency.

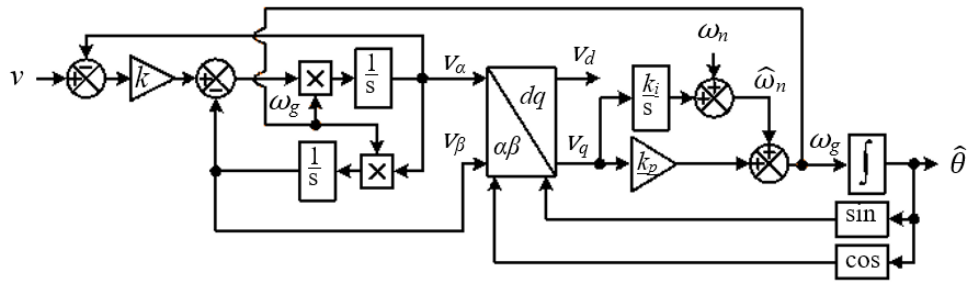

Figure 2.3: Block diagram of the single-phase SOGI based PLL.

The integrators represents two second-order filters with an adjustable bandwidth and resonance frequency equal to the frequency of the input signal. If the grid frequency is at the resonance frequency of the SOGI, the signal v_α has the same phase and amplitude as the fundamental of the input signal and v_β is orthogonal to v_α.

Therefore, the SOGI requires an adaptive tuning with respect to its resonance frequency. This can be achieved by using the frequency provided by the feedback control loop of the PLL structure; but in this way, the behavior of the whole PLL structure will be affected by the transients of the SOGI and the feedback control loop.

2.2.3: Single-Phase Transport Delay PLL

Fig. 2.4 shows the block diagram of the PLL-dq-FIFO [107]. It uses a first-in-first-out (FIFO) register to build the quadrature component for the *dq* transformation. Due to its fixed length delay, it is not able adjust the input voltage frequency during off-nominal condition, leading to phase angle estimation errors. An alternative way to generate the quadrature component is the Hilbert transformation. But it is very difficult to develop within the frequency range of 50-60 Hz.

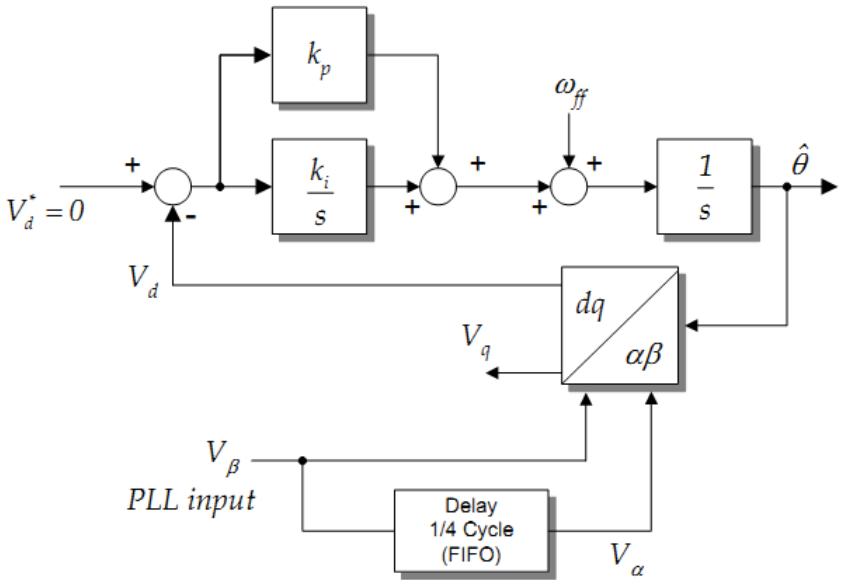

Figure 2.4: Block diagram of single-phase transport delay PLL.

2.2.4: Single-Phase Enhanced PLL

Fig. 2.5 shows the block diagram of the single-phase Enhanced PLL (EPLL). This PLL is based on adaptive filter theory [108]-[109]. Basically, it reconstructs, in real time, the fundamental component of the input signal by estimating its amplitude, phase and frequency through the steepest descent algorithm. In other words, this PLL has a non-linear phase detector. The gain *K* controls the convergence speed of the estimated amplitude.

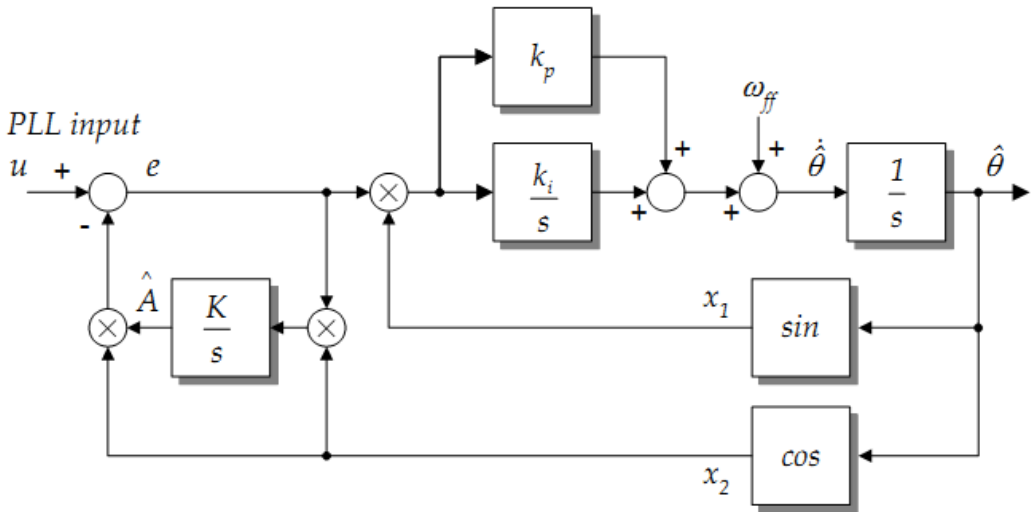

Figure 2.5: Block diagram of single-phase enhanced PLL.

The adaptive filter theory is based on the idea that an output signal of a system can be reconstructed (or estimated) modifying the gains of a linear combiner as a function of an error, which in turn is the difference between the estimated signal and the systems output. In the EPLL context, the desired signal is the grid voltage, and the estimated signal is built with the estimated phase angle, as well as the inputs to the filter.

2.2.5: Three-Phase SRF-PLL

The three-phase synchronous reference frame PLL transforms the three-phase voltage signal into direct voltage component and quadrature voltage component by Clarke's and Park's Transformation [91] and then its phase angle is estimated by regulating the quadrature component to zero. Under ideal sinusoidal grid conditions, the SRF-PLL performs effectively at a very high bandwidth, providing rapid and accurate phase angle estimation. However, if the signals are distorted by phase imbalance or harmonics, the bandwidth of the SRF-PLL needs to be reduced to perform proper filtering. The details of SRF-PLL will be discussed at a later section.

2.2.6: Decoupled Double SRF-PLL

The DDSRF-PLL, published in [62]-[63], has been developed for improving the conventional SRF-PLL. Fig. 2.6 shows the block diagram. This synchronization system exploits two synchronous reference frames rotating at the fundamental utility frequency, one counter-clockwise and another one clockwise, in order to achieve an accurate detection of the positive and negative sequence components of the grid voltage vector when it is affected by unbalanced grid faults.

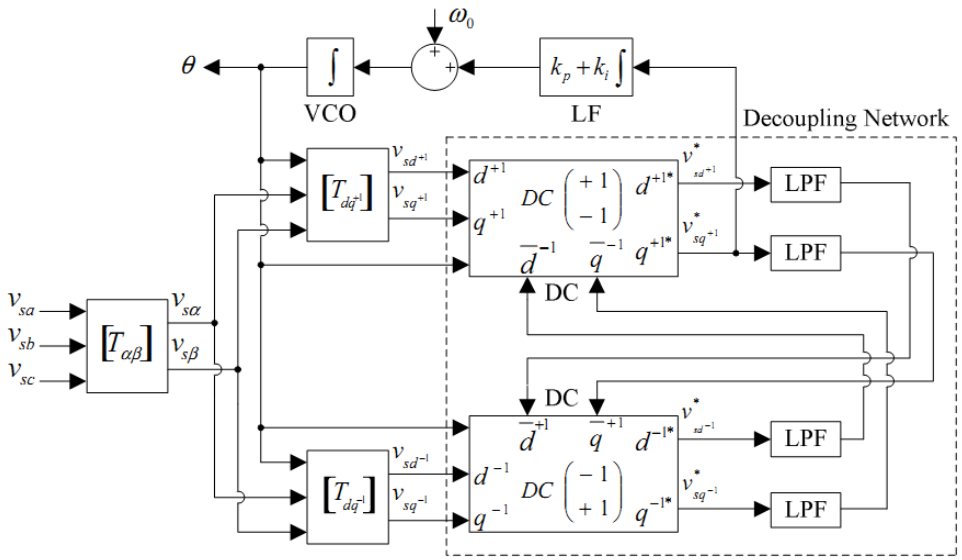

Figure 2.6: Block diagram of three-phase DDSRF-PLL.

When the three-phase grid voltage is unbalanced, the fundamental positive-sequence voltage vector appears as a DC voltage on the dq^{+1} axes of the positive-sequence SRF and as AC voltages at twice the fundamental utility frequency on the dq^{-1} axes of the negative-sequence SRF. In contrast, the negative-sequence voltage vector will cause a DC component on the negative-sequence SRF and an AC oscillation on the positive-sequence SRF. Since the amplitude of the oscillation on the positive-sequence SRF matches to the DC level on the negative-sequence SRF, and vice versa, a decoupling network is applied to signals on the *dq* positive/negative SRF axes in order to cancel out such ac oscillations. Low-pass filters (LPF) are used for extracting the DC component from the signal on the decoupled SRFs axes. These DC components collect information about the amplitude and phase-angle of the positive- and negative-sequence components of the grid voltage vector.

The PI controller of the DDSRF-PLL works on the decoupled *q*-axis signal of the positive-sequence SRF and performs the same function as in a SRF-PLL, aligning the positive-sequence voltage with the *d*-axis. This signal is free of AC components due to the effect of the decoupling networks and the bandwidth of the loop controller can be consequently increased [21].

2.2.7: Dual Second Order Generalized Integrator PLL

The operation of the DSOGI-PLL for estimating the positive and negative-sequence components of the grid voltage vectors is based on using the Instantaneous Symmetrical Components (ISC) method on the $\alpha\beta$ stationary reference frame, as explained in [93]. The ISC method is developed by the positive sequence calculation (PSC) block.

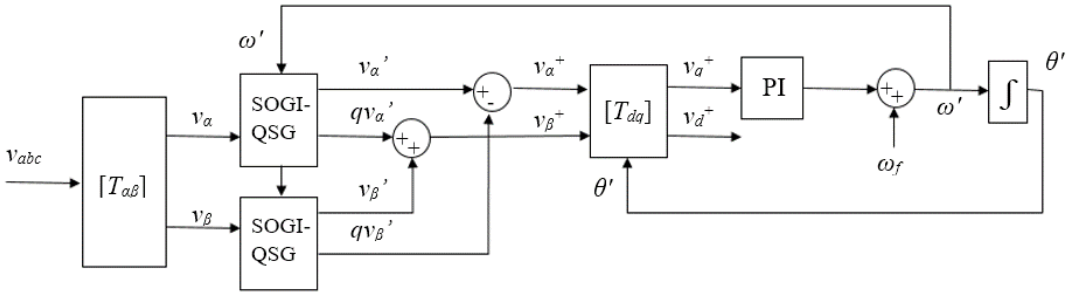

Figure 2.7: Block diagram of three-phase DSOGI-PLL.

To apply the ISC method, it is necessary to have a set of signals, v_α-v_β, representing the input voltage vector on the $\alpha\beta$ stationary reference frame together with another set of signals, qv_α *and* qv_β, which are in-quadrature and lagged with respect to v_α and v_β. In the DSOGI-PLL, the signals to be supplied to the ISC method are obtained by using a dual second order generalized integrator (DSOGI). At its output, the DSOGI provides four signals, which are the filtered version of v_α, v_β, qv_α, *and* qv_β. A conventional SRF-PLL estimates the positive-sequence voltage vector, $v^+_{\alpha\beta}$, to make this synchronization system frequency adaptive. This voltage is translated to the rotating SRF and the signal on the *q*-axis is applied at the input of the loop controller and the fundamental grid frequency and phase-angle of the positive sequence voltage are estimated.

2.2.8: Three-Phase Enhanced PLL

Fig. 2.8 shows the block diagram of a three-phase enhanced PLL (3EPLL). There are multiple extensions of the three-phase EPLL. An ordinary 3EPLL is equivalent to the SRF-PLL with the capability of accommodating various modifications due to its outer closed-loop feedback structure [110]. It can address the direct current component and harmonics within its loop structure.

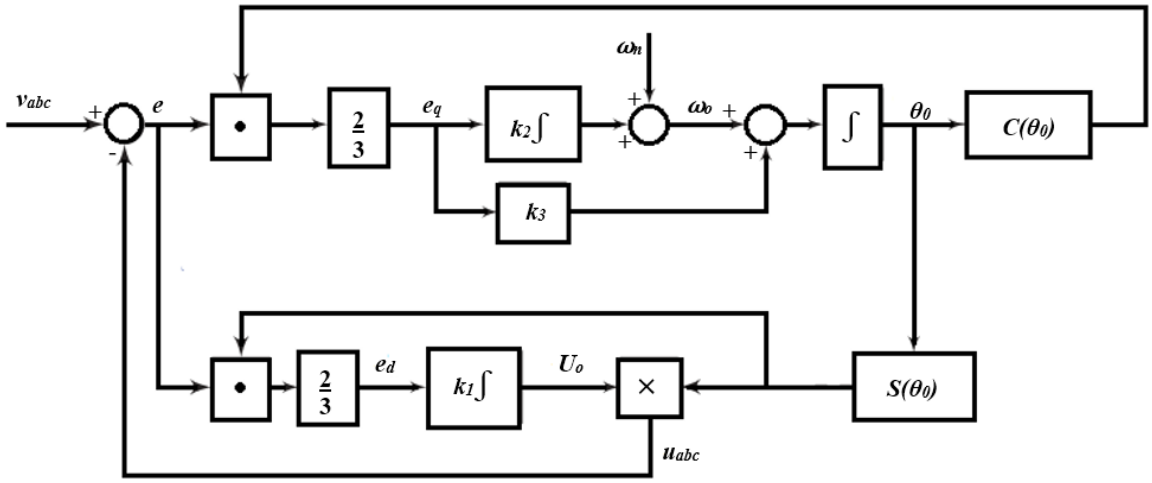

Figure 2.8: Block diagram of three-phase EPLL.

Each phase voltage is processed independently by the EPLL. This block filters the input signal and generates two sinusoidal outputs of the same amplitude and frequency, where the later one is led by 90 degree. The resulting signals constitute the input for the computational unit. Finally, the instantaneous positive-sequence voltage component can be estimated by means of using the ISC method.

2.3 The Conventional Three-Phase SRF-PLL and Its Performance

The conventional SRF-PLL transforms the three-phase sinusoidal voltage signal, denoted by v_a, v_b and v_c and expressed as in (6), into the direct axis component and quadrature axis component, v_d and v_q, under synchronous rotating reference frame through the rotating transformation. The transfer function, T is the combination of Clarke Transformation and Park Transformation [91] relating v_a, v_b and v_c, with v_d and v_q through (7) and is defined in (8).

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} sin(\omega_o t + \varphi_o) \\ sin(\omega_o t + \varphi_o - \frac{2\pi}{3}) \\ sin(\omega_o t + \varphi_o + \frac{2\pi}{3}) \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} v_q \\ v_d \end{bmatrix} = [T] \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{7}$$

$$T = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{8}$$

$$\theta = \omega_o t + \varphi_o \tag{9}$$

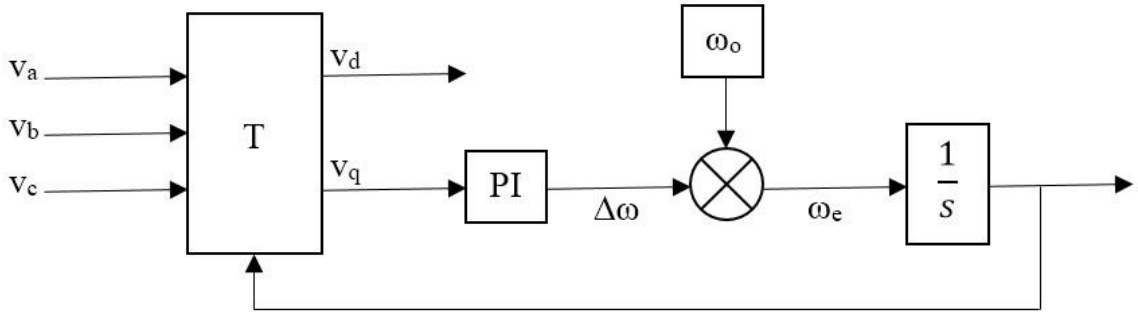

Figure 2.9: Block diagram of the conventional SRF-PLL.

Fig. 2.9 shows the block diagram of the conventional SRF-PLL, where ω_0 is the nominal value of the grid voltage fundamental frequency, $\Delta\omega$ is the fundamental frequency deviation from its nominal value and ω_e is the estimated value of the grid voltage fundamental frequency. Eventually, ω_e becomes equal to the fundamental frequency of the grid voltage at steady state. The value of v_q is regulated to zero and the phase angle of the grid voltage, θ is estimated. It is also the phase angle for rotating transformation in (8) and is expressed as in (9).

The conventional SRF-PLL can track the phase-angle of a three-phase system quickly and accurately at a very high bandwidth under balanced sinusoidal grid condition. It can estimate the phase-angle properly even when there is a sudden amplitude step or/and phase-angle shift. Fig. 2.10 shows the performance of the conventional SRF-PLL under 50% amplitude step and $\pi/2$ radian phase-angle shift of all the three phases at 0.1 second. The gain parameters of the proportional integral (PI) controller have been adjusted to maintain a higher value of bandwidth. The proportional gain, K_p has been set to 50 and the integral gain, K_i has been set to 98696. The v_q versus time curve in Fig. 2.10(b) shows that the value of quadrature component suddenly became unstable at the time of fault and then quickly became stabilized to zero within 3ms. It means, the response time of the conventional SFR-PLL is around 3ms. The estimated phase angle of phase-*a* is shown in Fig. 2.10(c).

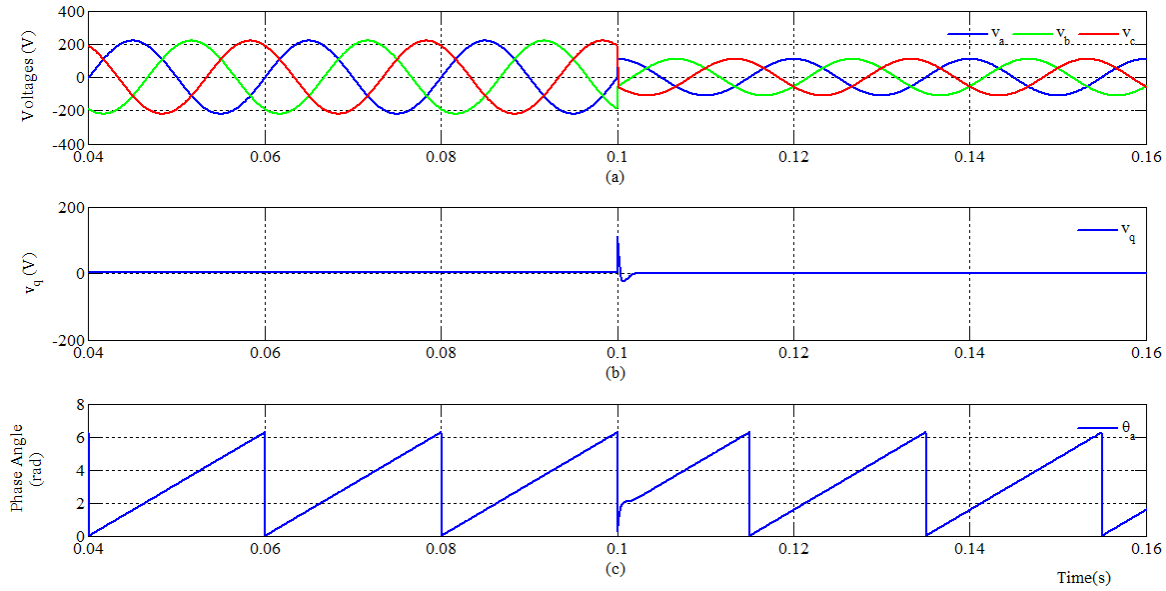

Figure 2.10: Performance of the conventional SRF- PLL under symmetrical fault conditions (50% amplitude step, $\pi/2$ phase jump) at high bandwidth. (a) three-phase voltage waveforms; (b) v_q versus time; (c) estimated phase angle of v_a.

Fig. 2.11 shows the performance of the conventional SRF-PLL at high bandwidth when the amplitudes of the three-phases have different amplitude jumps. In this simulation the amplitudes of the three-phases, v_a, v_b and v_c have changed to 80%, 50% and 30% of their original values respectively at 0.1 second. However, the phase angle differences between the three phases have been kept unaltered as in their balanced state. The phase-difference between them remained $2\pi/3$ radian. Fig. 2.11(b) shows the value of v_q has become slightly unstable after the fault. The effect is also displayed on Fig. 2.11(c). It shows that the conventional SRF-PLL cannot estimate the phase-angle of a three-phase system when the amplitudes of the phases are not equal despite being the phase-angle differences have been unaltered.

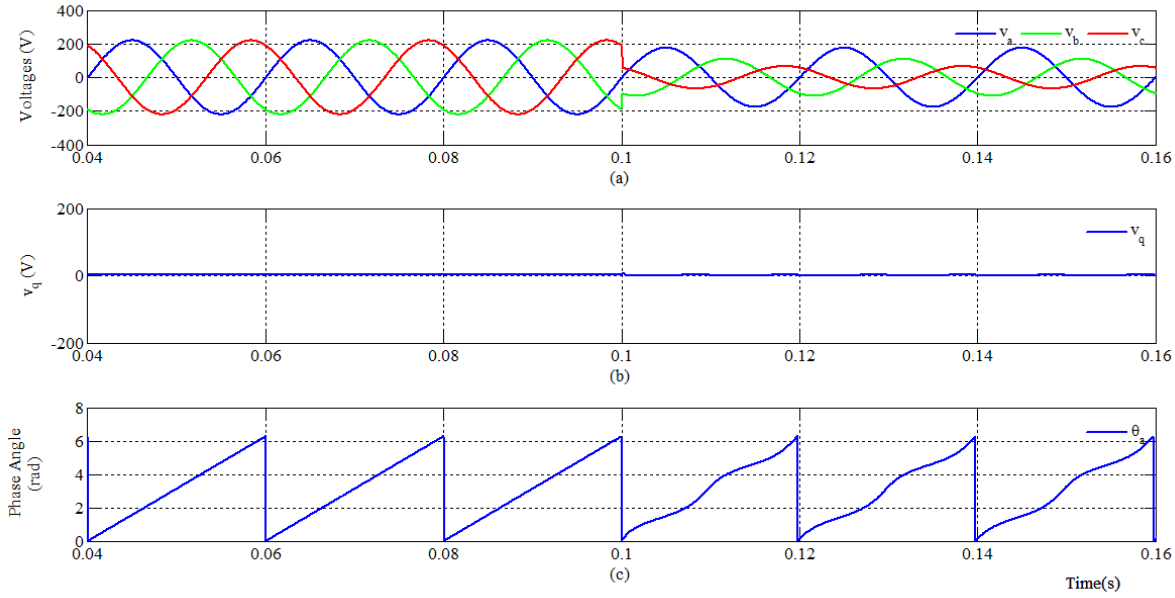

Figure 2.11: Performance of the conventional SRF- PLL under only unequal amplitudes of the phases at high bandwidth (a) three-phase voltage waveforms; (b) v_q versus time; (c) estimated phase angle of v_a.

The conventional SRF-PLL has been tested for the unbalanced conditions when the amplitudes of the three-phases are equal while the phase-angle differences between the phases have been altered. Fig. 2.12 gives the outcome of the same SRF-PLL operated under such unbalanced condition. Here, the phase-*b*, denoted by v_b suffers a clockwise phase shift of $\pi/6$ radians and the phase-*c*, v_c, suffers a counter-clockwise phase-shift of $\pi/4$ radians. Meanwhile, the amplitudes of the three-phases have remain equal. This unbalanced conditions have been triggered at 0.1 second of simulation. Fig. 2.12(b) shows the v_q vs time curve, which has a noticeable amplitude variation of v_q. The phase-angle estimation is shown in Fig. 2.12(c).

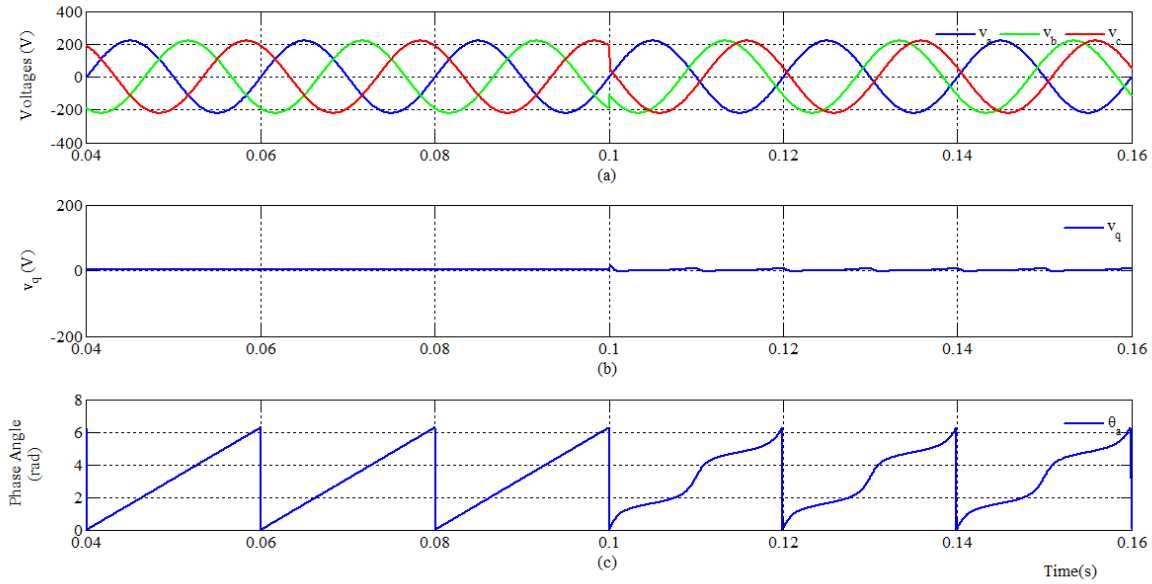

Figure 2.12: Performance of the conventional SRF- PLL under only unequal phase difference between the phases at high bandwidth (a) three-phase voltage waveforms; (b) v_q versus time; (c) estimated phase angle of v_a.

Fig. 2.13 shows the performance of the conventional SRF-PLL under both unequal amplitudes and unequal phase angle differences in between the three phases. Here, the amplitude of v_a, v_b and v_c have become 80%, 50% and 30% of their original values respectively at 0.1 second. Also, the two phases have shifted away by $\pi/6$ and $\pi/4$ radians respectively from phase-a. Fig 2.13 show that, the amplitude of v_q is not stabilized to zero and the estimated phase angle is also incorrect.

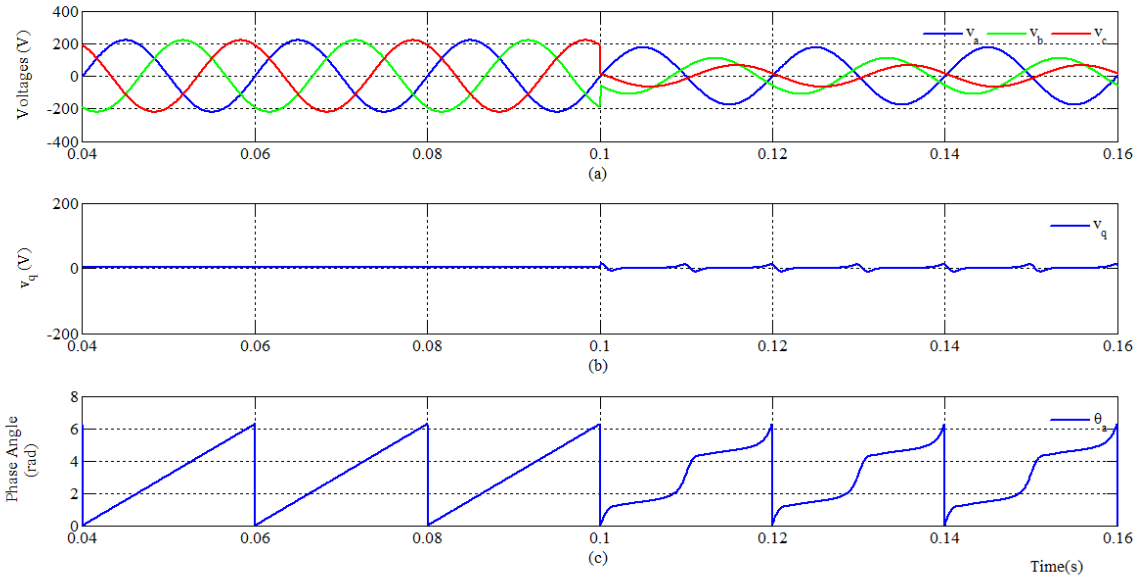

Figure 2.13: Performance of the conventional SRF-PLL under both unequal amplitude and unequal phase differences between the phases at high bandwidth (a) three-phase voltage waveforms; (b) v_q versus time; (c) estimated phase angle of v_a.

Although the conventional three-phase SRF-PLL is not successful in any form of imbalances in the three phases (either amplitude or/and phase angle difference imbalance), the PLL works perfectly under undistorted grid condition at high bandwidth. However, three-phase systems are often affected by harmonics. Even with a balanced system, the harmonic components are responsible for the failure of its phase-angle estimation process. Under such distorted conditions, the SRF-PLL can still be developed to accurately estimate the phase-angle at reduced bandwidth to perform proper filtering by the PI controller of the PLL.

Fig 2.14 and Fig 2.15 show the performance of the SRF-PLL under harmonics affected conditions at high and at reduced bandwidth respectively. For both the cases, the values of the harmonics components are set from the limit of IEEE 519-2014 standard. Also, for both the cases, the three phases have 50% amplitude step and $\pi/2$ radian phase jump.

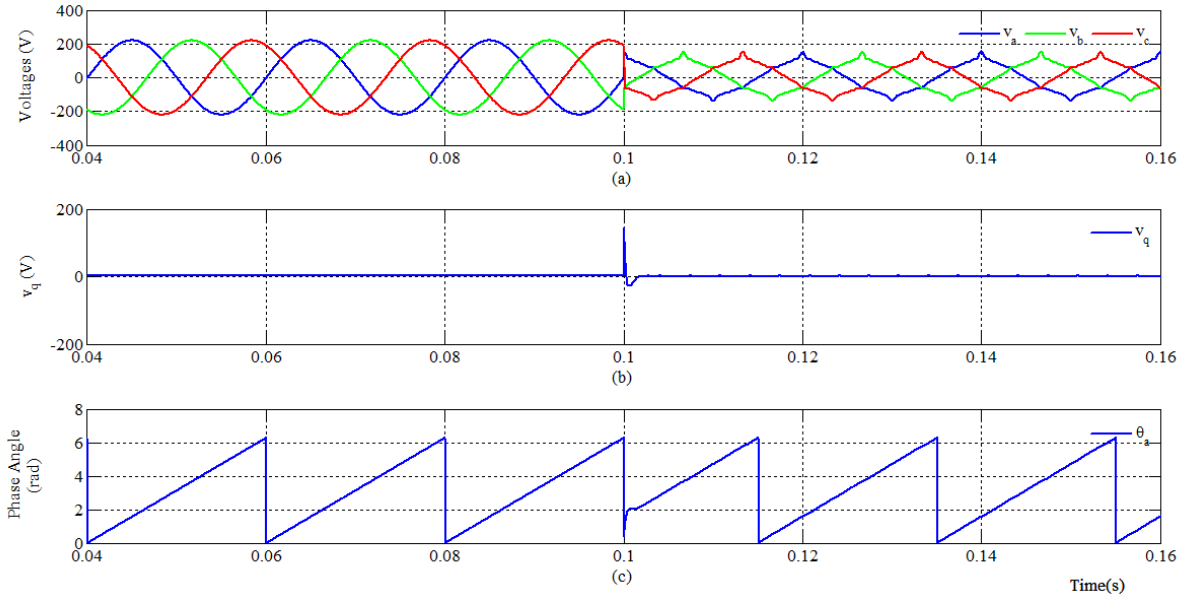

Figure 2.14: Performance of the conventional SRF- PLL under symmetrical fault conditions with harmonics (50% amplitude step, $\pi/2$ phase jump) at high bandwidth. (a) three-phase voltage waveforms; (b) v_q versus time; (c) estimated phase angle of v_a.

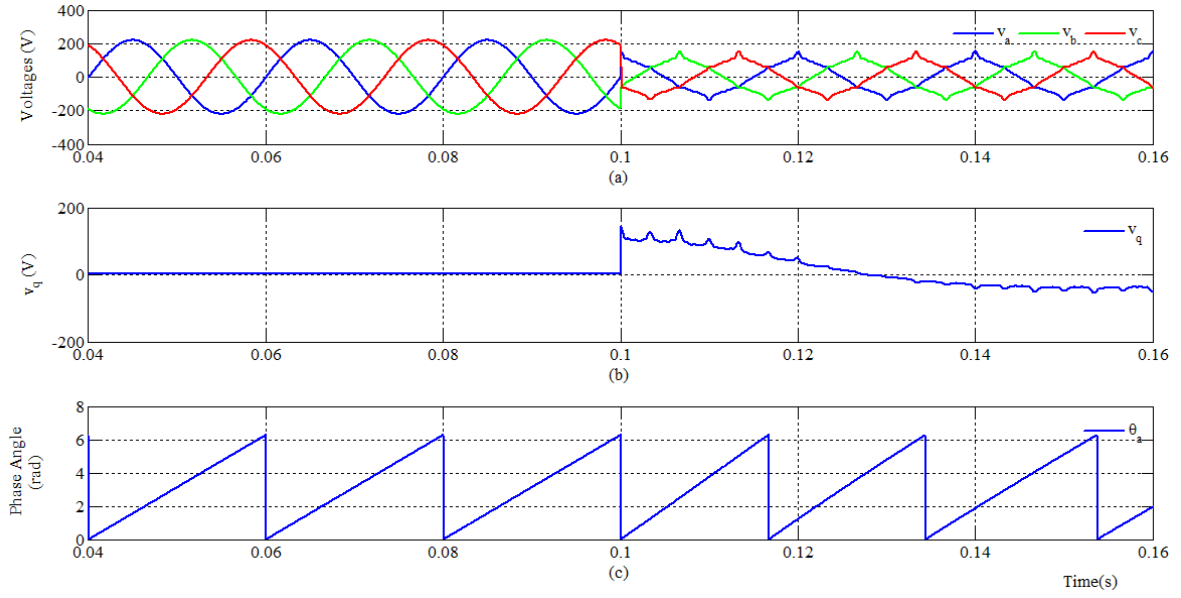

Figure 2.15: Performance of the conventional SRF- PLL under symmetrical fault conditions with harmonics (50% amplitude step, $\pi/2$ phase jump) at very low bandwidth. (a) three-phase voltage waveforms; (b) v_q versus time; (c) estimated phase angle of v_a.

Under these grid conditions, the perturbation of the v_q are directly inherited by the phase estimation control loop in the scheme without bandwidth reduction and the detected phase angles are heavily distorted as displayed in Fig. 2.14(c). To attenuate this perturbations, especially the second order component from the three-phase fundamental imbalances, the bandwidth is reduced by modifying the PI compensator as K_p = 0.5 and K_i = 20. A relatively smooth estimated phase-angle to an acceptable level is found in Fig. 2.15(c). However, it must be noted that the response time of the SRF-PLL has been excessively prolonged to around 40ms, which declines the usefulness of this bandwidth reduction.

On the other hand, even with the reduced bandwidth, the conventional SRF-PLL, cannot estimate the phase-angle of a system when higher order harmonics and any form of imbalances like unbalanced amplitudes and/or unbalanced phase-angle difference coexist. Fig. 2.16 demonstrates the performance of the SRF-PLL at high bandwidth when the three-phase balanced system has been affected by harmonics along with the amplitudes of the phases and the phase-angle differences between the phases being unequal.

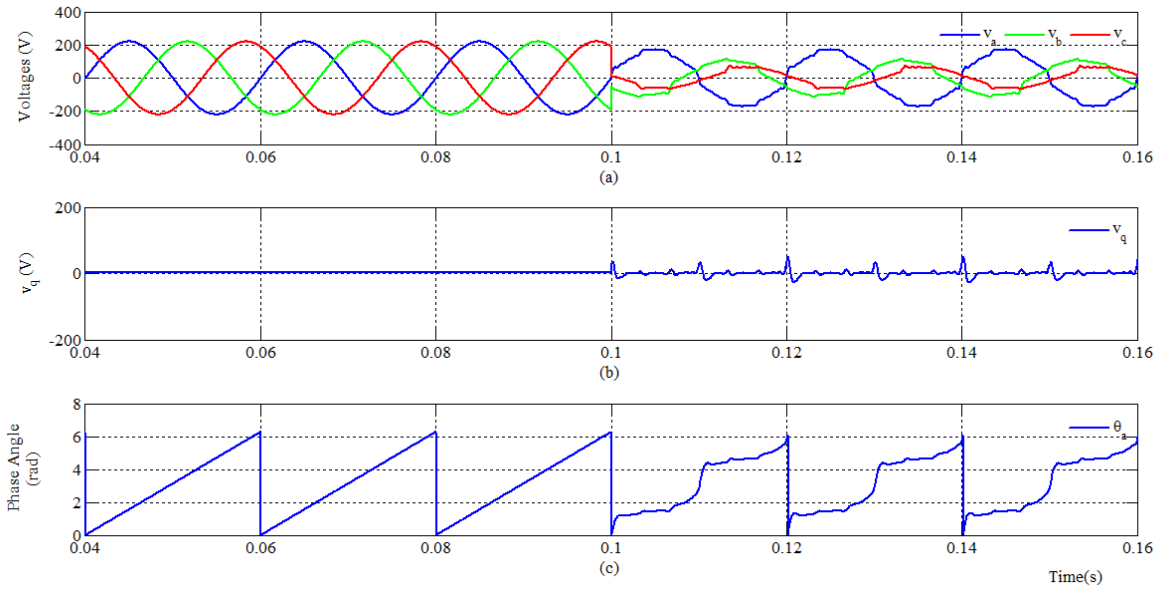

Figure 2.16: Performance of the conventional SRF- PLL in the presence of harmonics under both unequal amplitude and unequal phase differences between the phases at high bandwidth. (a) three-phase voltage waveforms; (b) v_q versus time; (c) estimated phase angle of v_a.

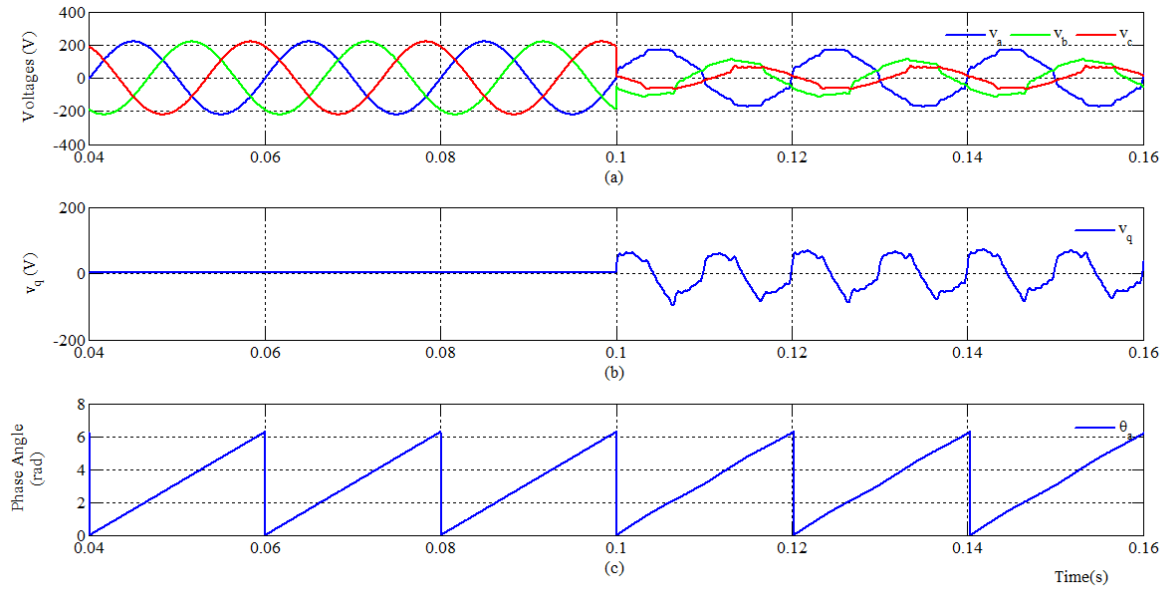

Figure 2.17: Performance of the conventional SRF- PLL in the presence of harmonics under both unequal amplitude and unequal phase differences between the phases at low bandwidth (a) three-phase voltage waveforms; (b) v_q versus time; (c) estimated phase angle of v_a.

Fig. 2.17 shows the performance of the same SRF-PLL operating under the same conditions as in for Fig. 2.16 except that the bandwidth of the PLL has been reduced to a much lower value. In both the cases, the conventional SRF-PLL inaccurately estimated the phase-angle of the three-phase system.

With the performance analysis presented so far, it is understood that, the conventional SRF-PLL performs effectively to capture the phase angle information only under balanced sinusoidal grid conditions. But, it is not good enough for the cases, when any form of three-phase imbalances and harmonic components exist. Although improvement can be achieved by reducing the bandwidth of the control loop, the recovery time will be excessively prolonged to an unacceptable level. However, if the harmonic components can be attenuated and the three-phase imbalances can be eliminated before the phase-angle estimation, the second order component of v_q will disappear. In that case, the high bandwidth of SRF-PLL can also be ensured and hence, the fast response with higher accuracy can be guaranteed. This brings up the concept of embedding the signal reforming algorithm and filter-less harmonics attenuation technique into the conventional SRF-PLL.

This chapter contains a complete step by step discussion on the phase-locked loop that has been developed as an outcome of this thesis work. Section 3.1 consists of the basic block diagram of the developed PLL. The harmonics attenuation algorithm along with its mathematical model has been discussed in Section 3.2. Section 3.3 explains the determination process of phase-angle deviation from ideal state. The signal reformation algorithm has been elaborately discussed in Section 3.4. Section 3.5 provides the calculation for the selection of parameter values for the proportional integral controller of the PLL.

3.1 Block Diagram of the Developed PLL

As already mentioned, the three-phase SRF-PLL is the simplest and the most efficient algorithm for phase-angle and frequency estimation of a balanced sinusoidal three-phase system, even with a slight amplitude jump, phase deviation and frequency shift distortion. But, it cannot effectively cope with the three-phase imbalances and harmonics. The developed PLL algorithm in this thesis work mainly focuses on reforming of the three-phase input signal, which dedicates to remove the unbalanced component before phase-angle estimation. But during the reforming process it never discards the information on the phase-angle differences in-between the phases. Also, when the system is under harmonics, the proposed method attenuates the harmonic components to refine the signal up-to a satisfactorily level of purity.

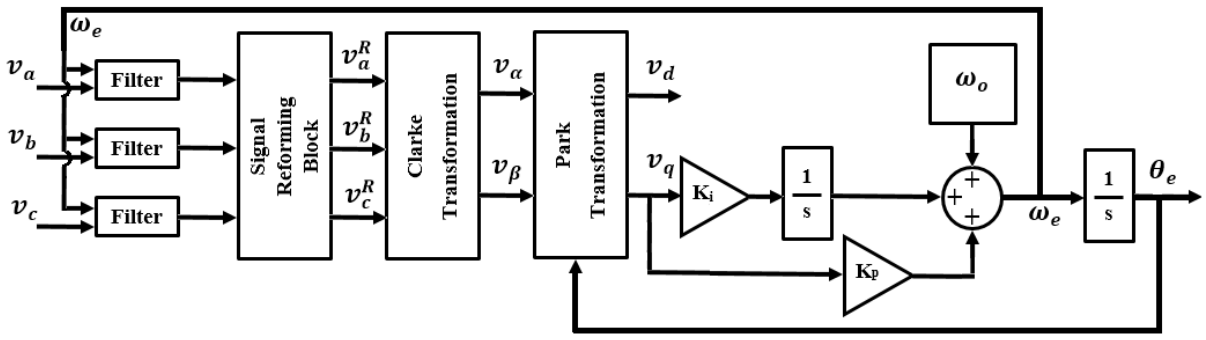

Figure 3.1: Block diagram of the developed three-phase phase-locked loop.

Fig. 3.1 represents the block diagram of the developed three-phase PLL. The developed PLL consists of harmonics attenuating units, a signal reforming block and a conventional SRF PLL. These three units are integrated as a single entity. First, the harmonic components of the voltages are reduced by the filter. A harmonic attenuation technique has been developed, which is much simpler than any filter algorithm, so that the input three-phase signal can be refined by attenuating the amplitudes of the higher order components. Then, the signals are made balanced by the signal reforming algorithm, and finally the phase-angle is estimated by the SRF-PLL. v_a, v_b, and v_c are the harmonics affected unbalanced three-phase voltages, whose harmonics are reduced and then the signals are reformed into v_a^*, v_b^* and v_c^* as the balanced voltages and then transformed into v_q and v_d. By regulating v_q to zero, ω_e is determined and phase angle θ is measured [62]. The design procedure of the developed algorithm can be divided into following four sections –

- Attenuation of harmonics
- Determination of phase-angle deviation
- Signal reformation by amplitude and phase-angle correction
- Selection of K_p and K_i for the SRF-PLL

3.2 Attenuation of Harmonics

Attenuation of harmonic components is the first stage of the designed PLL. These are designated as 'Filter' block in Fig. 3.1 as they are serving the same purpose of filters, although with some different characteristics, specially dedicated for the signal reforming technique. The filter block reduces the amplitudes of the harmonic components from the input grid voltage signals so that the zero crossing points and peaks can be determined and the signal reforming block can easily reform the signal. The developed algorithm assumes that the harmonics are according to the IEEE Standard 519-2014 [97]. European Standard EN50160 [98] will also be followed for harmonics specification with this algorithm. Since the filter blocks for three of the phases are functionally same, detailed analysis of one of the three phases has been illustrated here. Let v_a be a harmonic affected signal as expressed in (10).

$$v_a = a_1 \sin(\omega_e n T_s) + \sum_{h=2}^{25} a_h \sin(h\omega_e n T_s) \tag{10}$$

Here, h denotes the order of the harmonics which is assumed up to 25th order based on the IEEE 519-2014 standard, n is the sampling index, ω_e is the estimated angular frequency, which is, here equal to nominal frequency, ω_o and T_s is the sampling period. The proposed harmonics attenuation algorithm is based on cascaded combination of unit filter blocks. Each block eliminates one harmonic component and reduces the other lower order components. For the first block, (10) can be expressed as (11).

$$v_a^0 = {a_1}^0 \sin(\omega_e n T_s) + \sum_{h=2}^{25} {a_h}^0 \sin(h\omega_e n T_s) \tag{11}$$

Here, the superscripts on the amplitudes of the harmonic components are denoting their amplitudes after the number of unit blocks as the superscripts are mentioning. Differentiating (11) twice with respect to time, we get (12)

$$v_a^{0\prime\prime} = -{a_1}^0 \omega_e^2 \sin(\omega_e n T_s) - \sum_{h=2}^{25} {a_h}^0 \omega_e^2 h^2 \sin(h\omega_e n T_s) \tag{12}$$

Now, dividing (12) by $\omega_e^2 h_{max}^2$ and adding the result with (11), we get the new value of the refined signal, v_a^1, as expressed in (13) and (14). The value of h_{max} is the maximum order of the harmonics assumed to be prevailing in the signal.

$$v_a^1 = (a_1^0 - \frac{a_1^0}{h_{max}^2})\sin(\omega_e n T_s) + \sum_{h=2}^{24} {a_h}^1 \sin(h\omega_e n T_s) \tag{13}$$

Or,

$$v_a^1 = a_1^1 \sin(\omega_e n T_s) + \sum_{h=2}^{24} {a_h}^1 \sin(h\omega_e n T_s) \tag{14}$$

Here, a_1^1 and ${a_h}^1$ denotes the amplitude of the fundamental and the harmonics components respectively after passing through the first block. In (13), the harmonics component of highest order of (12) is eliminated. This process can be continued till all the harmonics are totally eliminated by serially cascading one unit filter block after other, each block having its own value of h_{max}. However, in this process the fundamental component will also be attenuated. But this attenuation is comparatively much less than the harmonic components of higher order and hence, with each block being pass, the signal will become more refined.

A conventional SRF-PLL can accurately estimate the phase-angle of a three-phase system, even when there is a small amount of harmonics [56]. Assuming that, k number of blocks have been utilized for refining a harmonics affected signal, after k^{th} filter block, the output signal can be expressed as in (15)-

$$v_a^k = a_1^k \sin(\omega_e n T_s) + \sum_{h=2}^{25-k} {a_h}^k \sin(h\omega_e n T_s) \tag{15}$$

Here, all the $a_h{}^k$ are the coefficients of the remaining harmonics components, whose values are relatively small compared to $a_1{}^k$. The second order differentiation is performed numerically according to (16).

$$v_a''(n) = \frac{v_a(n) + v_a(n - 2T_s) - 2v_a(n - T_s)}{{T_s}^2} \tag{16}$$

The block diagram of a single unit of the harmonics attenuation system is shown in Fig. 3.2. For the attenuation of h^{th} harmonics, the transfer function of the block diagram in Fig. 3.2 is expressed as in (17) –

$$H_{h_{max}}(z) = 1 + \frac{1 - z^{-1}}{T_s} . \frac{1 - z^{-1}}{T_s} . G \tag{17}$$

Where h_{max} is the order of the maximum harmonic component, T_s is the sampling period, and G is a gain constant whose value is set according to (18).

$$G = \frac{1}{\omega_e^2 h_{max}^2} \tag{18}$$

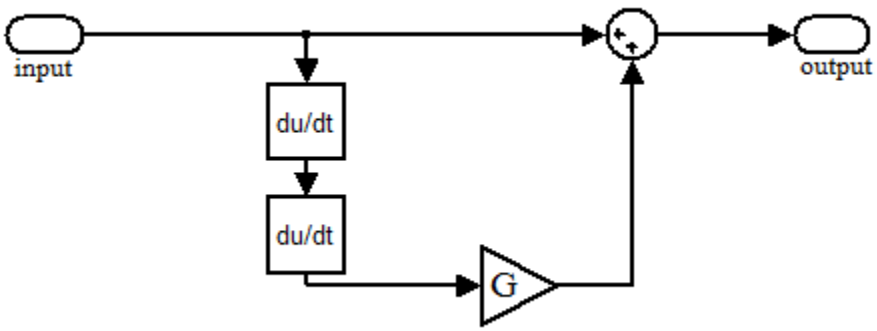

Figure 3.2: Block diagram of a single unit for the harmonics attenuation technique.

The whole system is a cascaded series connection of this unit block. After the signal being passed through several blocks, the harmonics components responsible for hampering the detection of zero crossing and peak points are attenuated to a negligible amplitude compared to the fundamental component.

The overall transfer function of the harmonics attenuation system is –

$$H(z) = H_{h_{max}}(z).H_{h_{max}-1}(z).H_{h_{max}-2}(z) \dots .H_2(z) \quad (19)$$

Fig. 3.3 shows the bode plot of the system expresses in (19) for ω_e = 100π, h_{max} = 25 and T_s = 0.0005 second.

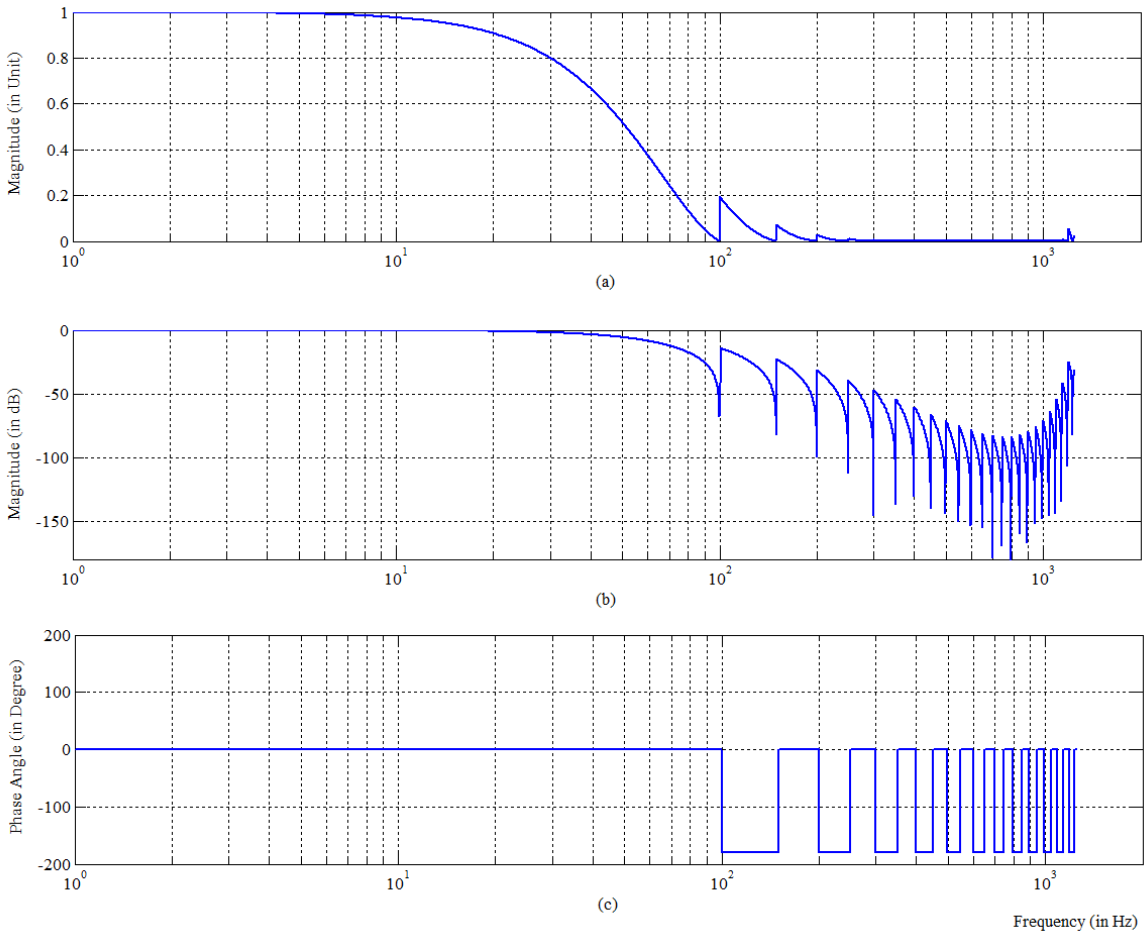

Figure 3.3: Performance of the designed harmonics attenuation algorithm (a) Frequency (Hz) vs Magnitude (in Unit), (b) Frequency (Hz) vs Magnitude (in dB), (c) Frequency (Hz) vs Phase Angle (in Degree).

Fig. 3.4 shows the performance of the developed harmonics attenuation technique. After the signal being passed through each additional block of the filtering stage, the refined signal is used to calculate the frequency and phase angle by the developed PLL algorithm. The maximum error in frequency and phase angle after each block are plotted in Figs. 3.4(a) and 3.4(b) respectively. As determined from the calculation, the errors are reduced with the increase of the number of blocks. Thus, the amplitudes of the harmonics components get attenuated. For the case of Fig. 3.4, EN 501650 standard limit has been followed to set the harmonics in the grid-voltage.

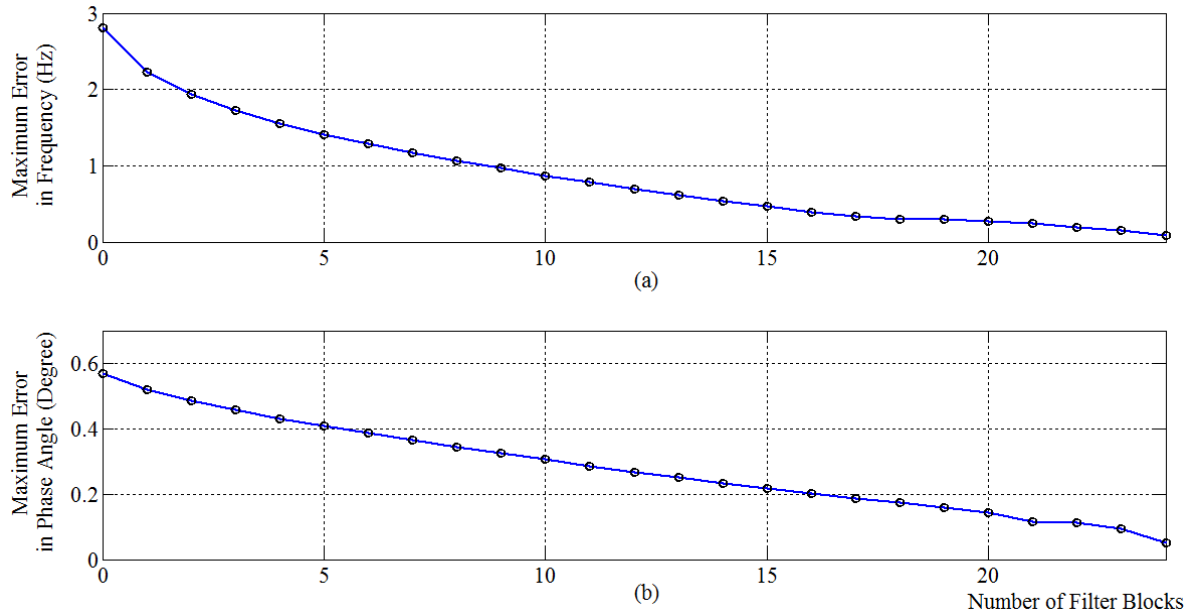

Figure 3.4: Performance of the proposed technique. (a) Estimated maximum frequency error versus number of filter blocks. (b) Estimated maximum phase error versus number of filter blocks.

Any ordinary filter will require the information from at least one period of the signal which is not permissible for the operation of the SRF-PLL. Also, ordinary filters change the phase-angle of a signal, which is very difficult to estimate. The developed method is less complex and requires comparatively less data. Also, since the attenuation algorithm follows the second order differentiation according to (16), there is apparently no phase delay between the input and output signal at the two ends of the whole filtering stage.

Although the technique has been developed to function properly when the system frequency, ω_o, matches the estimated frequency, ω_e, the technique is also useful in cases when the system frequency drops from nominal value. However, if the frequency of the harmonics component is greater than the nominal frequency, the proposed method will gradually diverge from accuracy.

This problem has been solved with the inclusion of frequency feed-back loop in the design. The information on the estimated frequency is fed back to the filter units and the filters update the ω_e of the $\omega_e^2 h_{max}^2$ divisor by the modified frequency. The system continue to updates it value until the value of v_q is not stabilized to zero and ceases its oscillation. Thus, the problem with the system frequency higher than the nominal frequency is solved.

3.3 Determination of Phase-Angle Deviation

Let, v_a, v_b and v_c be the instantaneous grid voltages after the harmonics attenuation and $v_a{}^R$, $v_b{}^R$ and $v_c{}^R$ be the instantaneous grid voltages after reformation as expressed in (20) and (21) respectively, where q is a multiplying factor. v_{a1}, v_{b1} and v_{c1} are the maximum amplitude of the three phases respectively.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} v_{a1}sin(\omega_o t + \varphi_o) \\ v_{b1}sin(\omega_o t + \varphi_o - \frac{2\pi}{3} - \Delta\theta_1) \\ v_{c1}sin(\omega_o t + \varphi_o + \frac{2\pi}{3} + \Delta\theta_2) \end{bmatrix} \tag{20}$$

$$\begin{bmatrix} v_a^R \\ v_b^R \\ v_c^R \end{bmatrix} = \begin{bmatrix} qv_{a1}sin(\omega_o t + \varphi_o) \\ qv_{a1}sin(\omega_o t + \varphi_o - \frac{2\pi}{3}) \\ qv_{a1}sin(\omega_o t + \varphi_o + \frac{2\pi}{3}) \end{bmatrix} \tag{21}$$

$\Delta\theta_1$ and $\Delta\theta_2$ of (20) are the phase-angle deviations from the ideal balanced three-phase system. Rest of the notations are same as introduced in Section 2.3. The phase diagram of the mentioned systems for (20) and (21) are shown in Fig. 3.5.

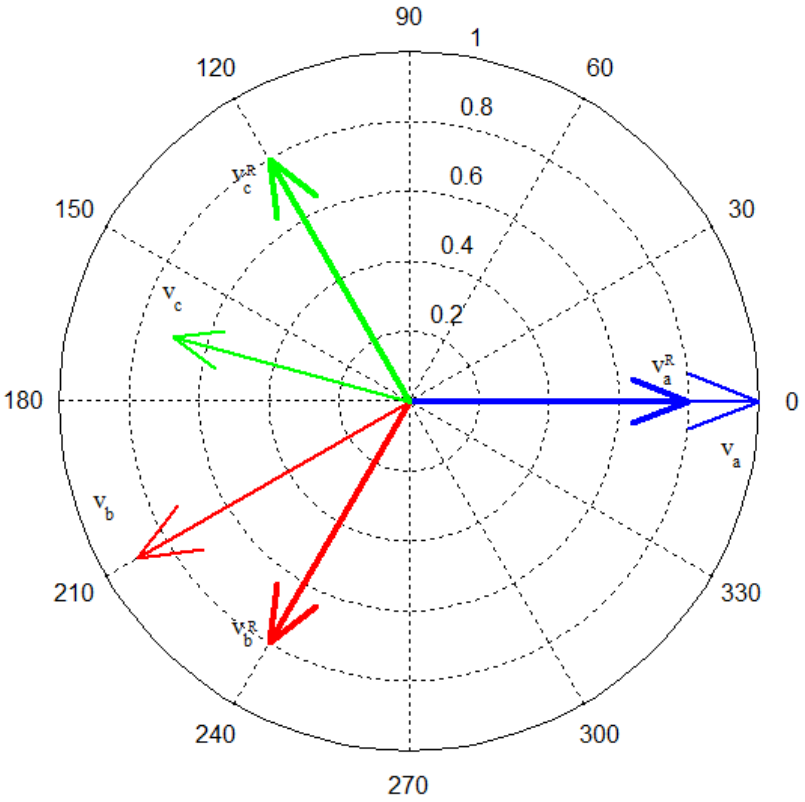

Figure 3.5: Phase diagram of the system. The thin line represents the unbalanced three-phase system and the thick line represents the reformed balance system. Phase *a*, *b* and *c* are represented by blue, red and green color respectively.

At first, one of the phases of the three-phase system is selected as reference signal. For this thesis, in order to determine $\Delta\theta_1$, v_a is selected as reference phase and the equation of v_b is expanded as in (22). At the beginning of each cycle of v_a, which is the first zero-crossing point of a cycle, the value of $sin(\theta)$ equals to 0 and the value of $cos(\theta)$ equals to 1. Therefore, (22) can be simplified to (23).

$$\sin(\theta)\cos(\frac{2\pi}{3}+\Delta\theta_1) - \cos(\theta)\sin(\frac{2\pi}{3}+\Delta\theta_1) - \frac{v_b}{v_{b1}} = 0 \qquad (22)$$

$$\sin(\frac{2\pi}{3}+\Delta\theta_1) = -\frac{v_b}{v_{b1}} \qquad (23)$$

The value of v_b is measured at the zero-crossing point of v_a. The maximum value of phase-*b*, v_{b1} is also measured. $\Delta\theta_1$ is determined from (23) by applying inverse sine operation. Since $\Delta\theta_1$ can have either positive or negative value, direct application of inverse sine function on (20) will create erroneous estimation.

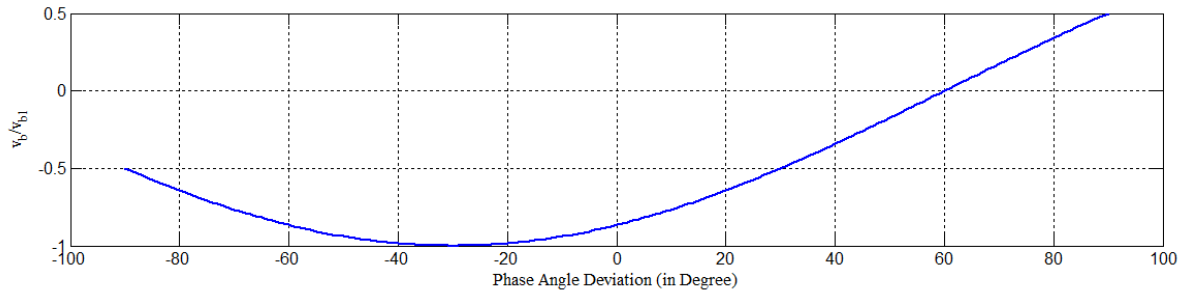

Figure 3.6: Phase Angle Deviation vs v_b/v_{b1} curve.

Fig. 3.6 plots the phase angle deviation versus normalized voltage curve. It can be inferred from Fig. 3.6 that, ambiguity will occur in angle calculation between -90 to -30 degree and -30 to 30 degree. The rest of the range, 30 to 90 degree, can be directly estimated. However, the phase-angle deviation can be directly calculated within the range of -30 to 90 degrees from (23) by adding an additional 60 degree after applying the inverse-sine operation on (23). Since the phase will not be on 1st quadrant, this addition is necessary.

Similarly, v_a is selected as reference phase and the equation of v_c is expanded as in (24), which becomes (25) at every first zero crossing point of v_a in each cycle. $\Delta\theta_2$ can be determined from (25) by applying inverse sine operation.

$$\sin(\theta)\cos(\frac{2\pi}{3}+\Delta\theta_2)+\cos(\theta)\sin(\frac{2\pi}{3}+\Delta\theta_2)-\frac{v_c}{v_{c1}}=0 \quad (24)$$

$$\sin(\frac{2\pi}{3}+\Delta\theta_2)=\frac{v_c}{v_{c1}} \quad (25)$$

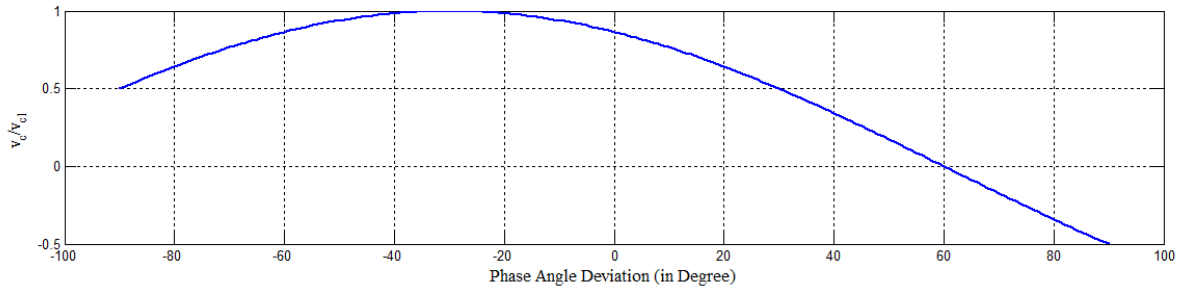

Figure 3.7: Phase Angle Deviation vs v_c/v_{c1} curve.

Fig. 3.7 shows the phase angle deviation versus normalized voltage curve. It can be inferred from Fig. 3.6 that, ambiguity will also occur in angle calculation between -90 to -30 degree and -30 to 30 degree. The rest of the range, 30 to 90 degree, can be directly estimated. However, the phase-angle deviation can be directly calculated within the range of -30 to 90 degrees from (25) by adding 60 degree to the negative value of the inverse-sine operation on (25).

The values of v_{b1} and v_{c1} are required for (23) and (25), respectively. For this purpose, the latest values of v_b and v_c have been stored in memory and they have been compared with their previous sets of stored values in a cycle. The maximum values of v_b and v_c are stored in memory as v_{b1} and v_{c1}, respectively. These values are used throughout the calculation process until any change in these maximum values is detected in any cycle. Similar procedure can be followed to determine the value of v_{a1}.

3.4 Signal Reformation by Amplitude & Phase-Angle Correction

The unequal phases-angle differences between the phases are made equal by eliminating the effect of $\Delta\theta_1$ and $\Delta\theta_2$ from v_b and v_c respectively. The expression for v_b in (20) is expanded as in (26) and (27). The value of $sin(\theta-2\pi/3)$ is determined by solving (27). The equation for the solution is expressed in (28).

$$sin(\theta-\frac{2\pi}{3})\,cos(\Delta\theta_1)-cos(\theta-\frac{2\pi}{3})\,sin(\Delta\theta_1)=\frac{v_b}{v_{b1}} \tag{26}$$

$$sin(\theta-\frac{2\pi}{3})\,cos(\Delta\theta_1)\pm\sqrt{\{1-sin^2(\theta-\frac{2\pi}{3})\}}sin(\Delta\theta_1)=\frac{v_b}{v_{b1}} \tag{27}$$

$$sin(\theta-\frac{2\pi}{3})=(\frac{v_b}{v_{b1}})cos(\Delta\theta_1)\pm sin(\Delta\theta_1)\sqrt{\{1-(\frac{v_b}{v_{b1}})^2\}} \tag{28}$$

Similarly, expanding the expression of v_c in (20) we get (29) and (30). The value of $sin(\theta+2\pi/3)$ can be determined by solving (30). The solution for (30) is expressed in (31).

$$sin(\theta+\frac{2\pi}{3})\,cos(\Delta\theta_2)+cos(\theta+\frac{2\pi}{3})\,sin(\Delta\theta_2)=\frac{v_c}{v_{c1}} \tag{29}$$

$$sin(\theta+\frac{2\pi}{3})\,cos(\Delta\theta_2)\pm\sqrt{\{1-sin^2(\theta+\frac{2\pi}{3})\}}sin(\Delta\theta_2)=\frac{v_c}{v_{c1}} \tag{30}$$

$$sin(\theta+\frac{2\pi}{3})=(\frac{v_c}{v_{c1}})cos(\Delta\theta_2)\pm sin(\Delta\theta_2)\sqrt{\{1-(\frac{v_c}{v_{c1}})^2\}} \tag{31}$$

Since both the equations, (28) and (31), are quadratic, each of them have two solutions. Let, x_{b1} and x_{b2} be the solutions of $sin(\theta-2\pi/3)$ calculated from (28) and x_{c1} and x_{c2} be the solutions of $sin(\theta+2\pi/3)$ calculated from (31). Since the sum of the three-phase voltages is zero when they are balanced, in order to find out the solutions of (28) and (31), a set of four equations, as in (32), (33), (34) and (35), are formed considering the combinations of x_{b1}, x_{b2}, x_{c1} and x_{c2}.

$$\frac{v_a}{v_{a1}} + x_{b1} + x_{c1} = e_1 \quad (32)$$

$$\frac{v_a}{v_{a1}} + x_{b1} + x_{c2} = e_2 \quad (33)$$

$$\frac{v_a}{v_{a1}} + x_{b2} + x_{c1} = e_3 \quad (34)$$

$$\frac{v_a}{v_{a1}} + x_{b2} + x_{c2} = e_4 \quad (35)$$

Where, e_1, e_2, e_3 and e_4 have been denoted as error values and only the correct combination has zero value. In practice, the proper combination will create minimum absolute value which is nearest to zero. The equation, whose right hand side is equal to or closest to 0 consists of the actual solution of (28) and (31). Thus, $sin(\theta)$, $sin(\theta - 2\pi/3)$ and $sin(\theta + 2\pi/3)$ can be determined. During the phase angle reformation process, the system has already been transformed into a three-phase system of normalized amplitude. Hence, amplitude reformation is an inherent advantage of this phase-angle reforming algorithm. Since, the maximum value of the reference phase has already been determined, multiplying these values with a factor of qv_{a1}, as expressed in (21), the values of v_a^R, v_b^R and v_c^R are obtained respectively. The constant q is any suitable real positive number. Thus, a balanced three-phase voltage system is reformed.

3.5 Selection of K_p and K_i for the PLL

The efficiency and the performance of a PLL depend on the performance of the loop filter. As shown in Fig. 3.1, the loop filter is typically a proportional-integral (PI) controller. This PI filter makes the PLL insensitive to grid voltage variations by dividing the v_q by an estimation of the amplitude of the voltage [68]. The characteristics of a PI filter is solely controlled by the proportional constant, K_p and the integral constant, K_i. This section will determine suitable values of these parameters from the transfer function of an SRF-PLL.

In [111], the author derived the transfer function of an SRF-PLL and showed that the conventional SRF-PLL is actually a first-order complex band-pass filter (CBF). A complex filter has asymmetrical frequency response around zero frequency, and therefore they can make distinction between the positive and negative sequences of the same frequency [112]-[114]. According to [111], for a constant estimated frequency, ω_e, the transfer function of the SRF-PLL can be expressed as (36), which is the equation of a first-order CBF.

$$G_{SRF\text{-}PLL}(s) = \frac{k}{(s - j\omega_e) + k} \tag{36}$$

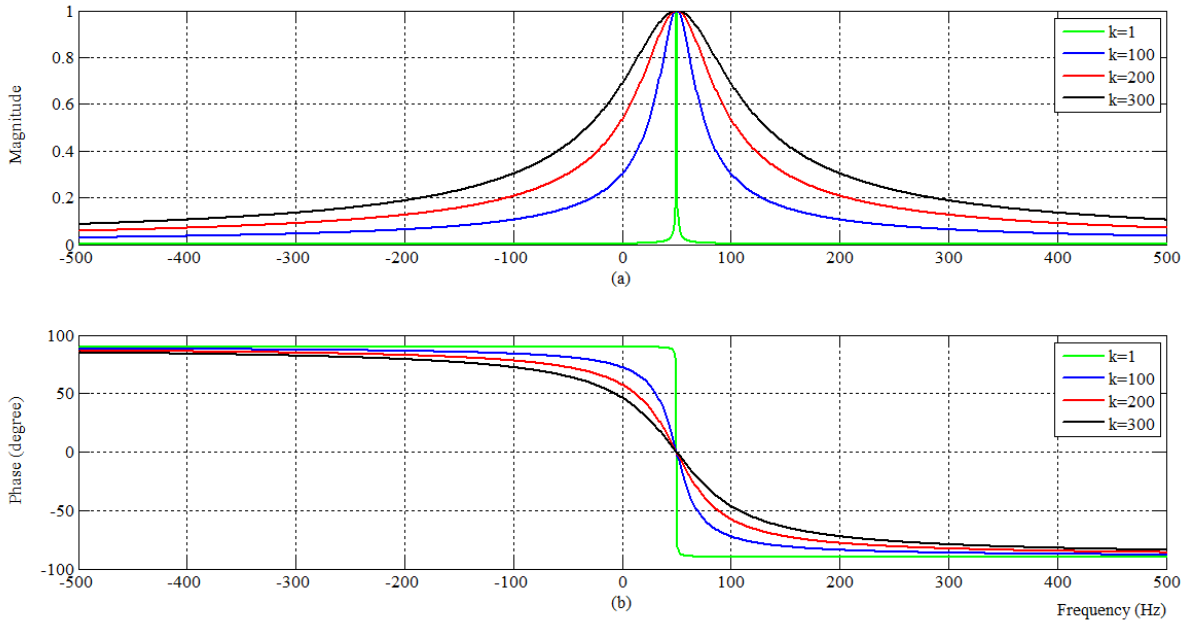

Figure 3.8: Frequency response of $G_{SRF\text{-}PLL}(s)$ for $\omega_e = 2\pi 50$ rad/s at different values of k. (a) Magnitude vs Frequency plot, (b) Phase vs Frequency plot.

Fig. 3.8 shows the frequency response of (36) for $\omega_e = 100\pi$ rad/s at different values of k. Here, the responses to negative frequencies in these plots can be interpreted as the response to the negative sequence vector signal. The SRF-PLLs frequency response is asymmetrical around zero frequency since it provides unity gain with zero phase shift at fundamental frequency of positive sequence, while providing a certain level of attenuation at the same frequency of negative sequence.

The SRF-PLL is a CBF (with center frequency ω_e) whose bandwidth is determined by the parameter k. The higher the value of k, the higher the bandwidth and, therefore, the lower the filtering capability. So, selection of k, is a trade-off between the filtering capability and the transient time. Fig. 3.9 shows the attenuation provided by the SRF-PLL at the fundamental frequency of negative sequence as a function of k. A suitable settling time can be approximated by the formula of settling time, $t_s = 4/k$. The figure clearly shows the trade-off between the filtering capability and transient time, and it is used for selecting a proper value for k.

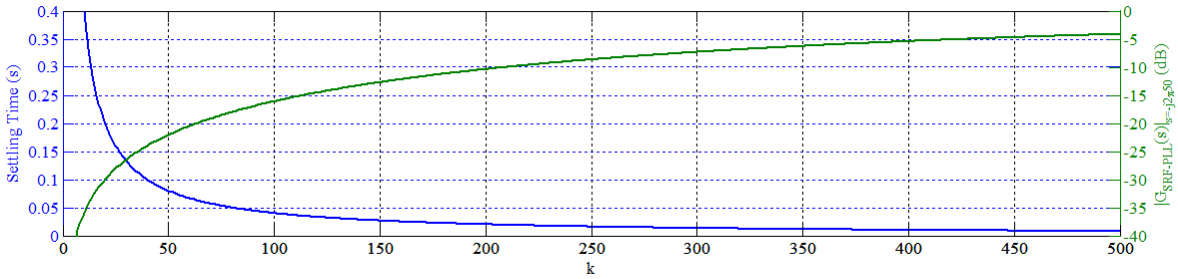

Figure 3.9: SRF-PLL settling-time in extraction of FFPS component as a function of k (labeling on the left); Attenuation provided by the SRF-PLL at the fundamental frequency of negative sequence as a function of k (labeling on the right).

$$G_{cl}(s) = \frac{K_p s + K_i}{s^2 + K_p s + K_i} \tag{37}$$

The proportional gain K_p and the integral gain K_i are determined after the value of k is settled. The closed loop transfer function relating the input and estimated phases is expressed as (37), which is a standard second order transfer function with a zero. Usually a suitable damping factor ζ is selected so that $k = 2\pi K_p = 2\zeta\omega_e$ and $K_i = \omega_n^2$ [115]-[116]. In this thesis work, the value of K_p and K_i are selected to be 50 and 98696 respectively for the developed algorithm with a settling time of 0.0127 second and a damping factor of 0.5.

In this chapter the simulation results for the developed PLL has been presented. Section 4.1 describes the environment of the simulation process. Several simulation results without the harmonics component in grid voltage are provided in Section 4.2. Section 4.3 provides the simulation results with harmonic components in grid voltage.

4.1 Simulation Environment

In order to test the performance of the developed PLL algorithm, numerous simulations are performed. All the simulations are performed in MATLAB/Simulink environment. The sampling frequency is set 20 kHz for the simulator. The values of K_p and K_i of the developed PLL have been set to 50 and 98696 respectively according to the selection procedure described in section 3.5. A three-phase, 50 Hz, 220 volt grid-voltage system have been created for the simulation whose amplitudes of the phases and the phase-angles can be altered at a specified moment. The grid voltage can also be affected by harmonics.

The simulations have been performed primarily under two major categories – unbalanced signals free of harmonics and signals with harmonics. For the first case, the signals are made unbalanced by altering amplitudes, phase-angles and frequency of the three-phase system. Several different conditions have been tested. The phase-angles of the system is then estimated by the developed PLL algorithm and the results are presented. For the latter case, harmonics are added to the grid-signal as well as maintaining the other imbalanced conditions.

The harmonics are set according to the EN 50160 and IEEE 519-2014 standards of permissible limit of harmonic components in grid voltage for distribution system. Although, most of the simulated conditions have been set according to the IEEE 519-2014 standard, which is IEEE recognized, the European standard has also been tested since it allows a higher value of total harmonic distortion (THD). The relative amplitudes of the harmonic components up to 25^{th} order have been tabulated in Table I and Table II for EN 50160 and IEEE 519-2014 standards respectively.

TABLE I

HARMONICS BASED ON EUROPEAN STANDARD EN 50160

Order	Relative Voltage (%)	Order	Relative Voltage (%)
2	2.0	14	0.5
3	5.0	15	0.5
4	1.0	16	0.5
5	6.0	17	2.0
6	0.5	18	0.5
7	5.0	19	1.5
8	0.5	20	0.5
9	1.5	21	0.5
10	0.5	22	0.5
11	3.5	23	1.5
12	0.5	24	0.5
13	3.0	25	1.5

TABLE II

HARMONICS BASED ON IEEE 519-2014 STANDARD

Order	Relative Voltage (%)	Order	Relative Voltage (%)
2	1.0	14	0.5
3	4.0	15	2.0
4	1.0	16	0.5
5	4.0	17	1.5
6	1.0	18	0.375
7	4.0	19	1.5
8	1.0	20	0.375
9	4.0	21	1.5
10	1.0	22	0.375
11	2.0	23	0.6
12	0.5	24	0.15
13	2.0	25	0.6

4.2 Case-A: Three-Phase Grid Voltage without Harmonics

4.2.1: Case-A1: Voltage Sag at All the Phases

In this case, all the three phases of the 220 Volt, 50 Hz three-phase balanced grid-voltage suffer from voltage sag. At 0.1 second, the amplitude of phase-*a*, phase-*b* and phase-*c* drops to 80%, 50% and 30% respectively of their nominal voltage. The phase-angles of the phases and frequency remain unaffected by the sag. The performance of the developed PLL is shown in Fig. 4.1, where the voltage is first reformed (Fig. 4.1(b)) and then the phase-angles are measured (Fig 4.1(d)). Fig. 4.1(c) is the v_q vs time curve, showing that the recovery time of the PLL under this condition is 0.0285 second.

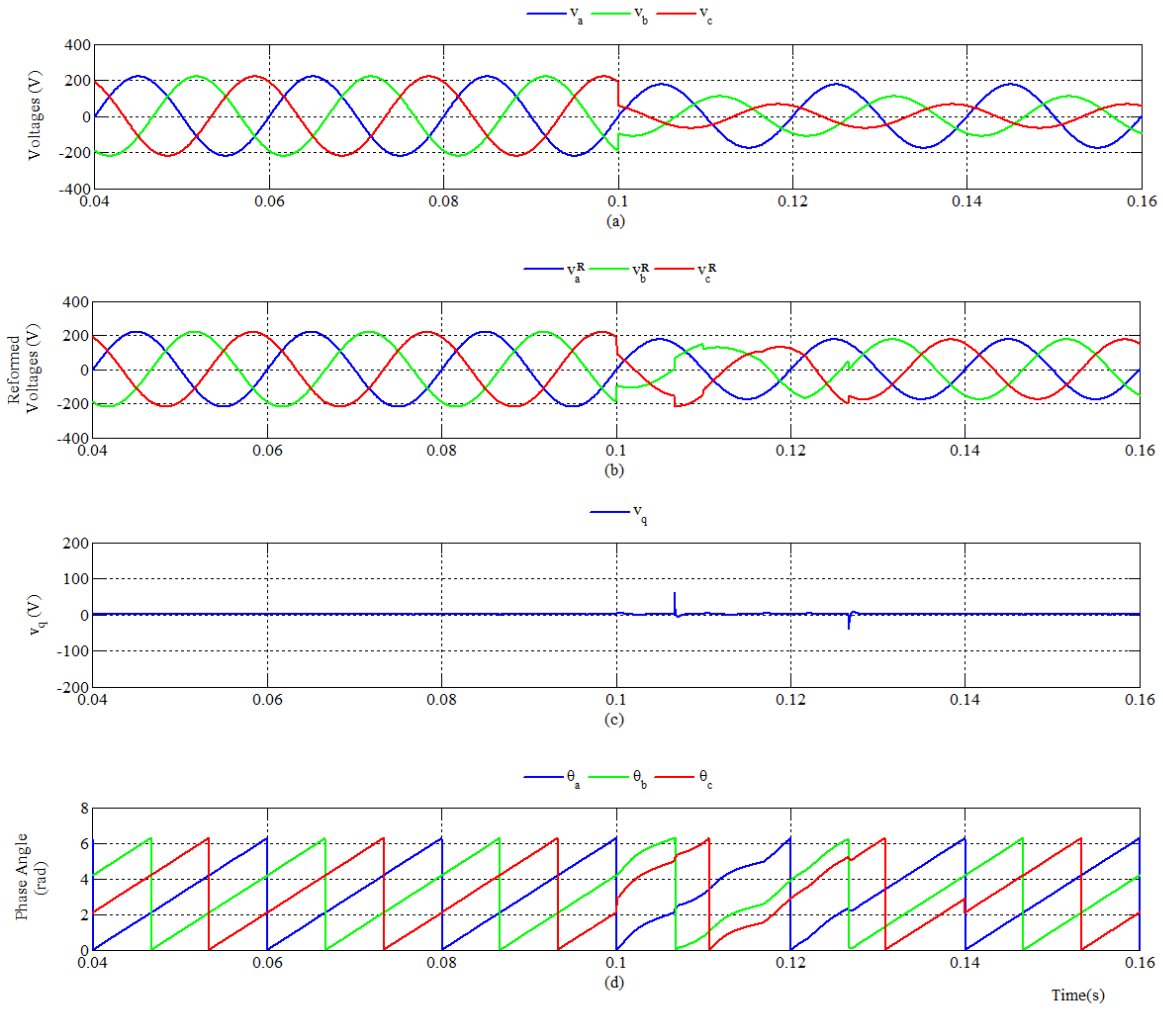

Figure 4.1: Performance of the developed PLL with voltage sag at all the phases. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.2.2: Case-A2: Voltage Swell at All the Phases

At this case, similar to case-A1, all the three phases of the 220 Volt, 50 Hz three-phase balanced grid-voltage suffer from voltage swell. The three phases, phase-*a*, phase-*b* and phase-*c* jumps up to 110%, 150% and 120% respectively of their nominal voltage at 0.1 second. The phase-angles of the phases and frequency remain unaffected as well. Fig. 4.2 depicts the performance of the developed PLL. Here, phase-*a* is considered as the base signal and the voltage is first reformed (Fig. 4.2(b)) and then the phase-angles are measured (Fig 4.2(d)). Fig. 4.2(c) is the v_q vs time curve, showing that the recovery time of the PLL under this condition is 0.0185 second. Here, the recovery time is faster than case-A1 because of the percentage change in all the three phases are relatively less in this case.

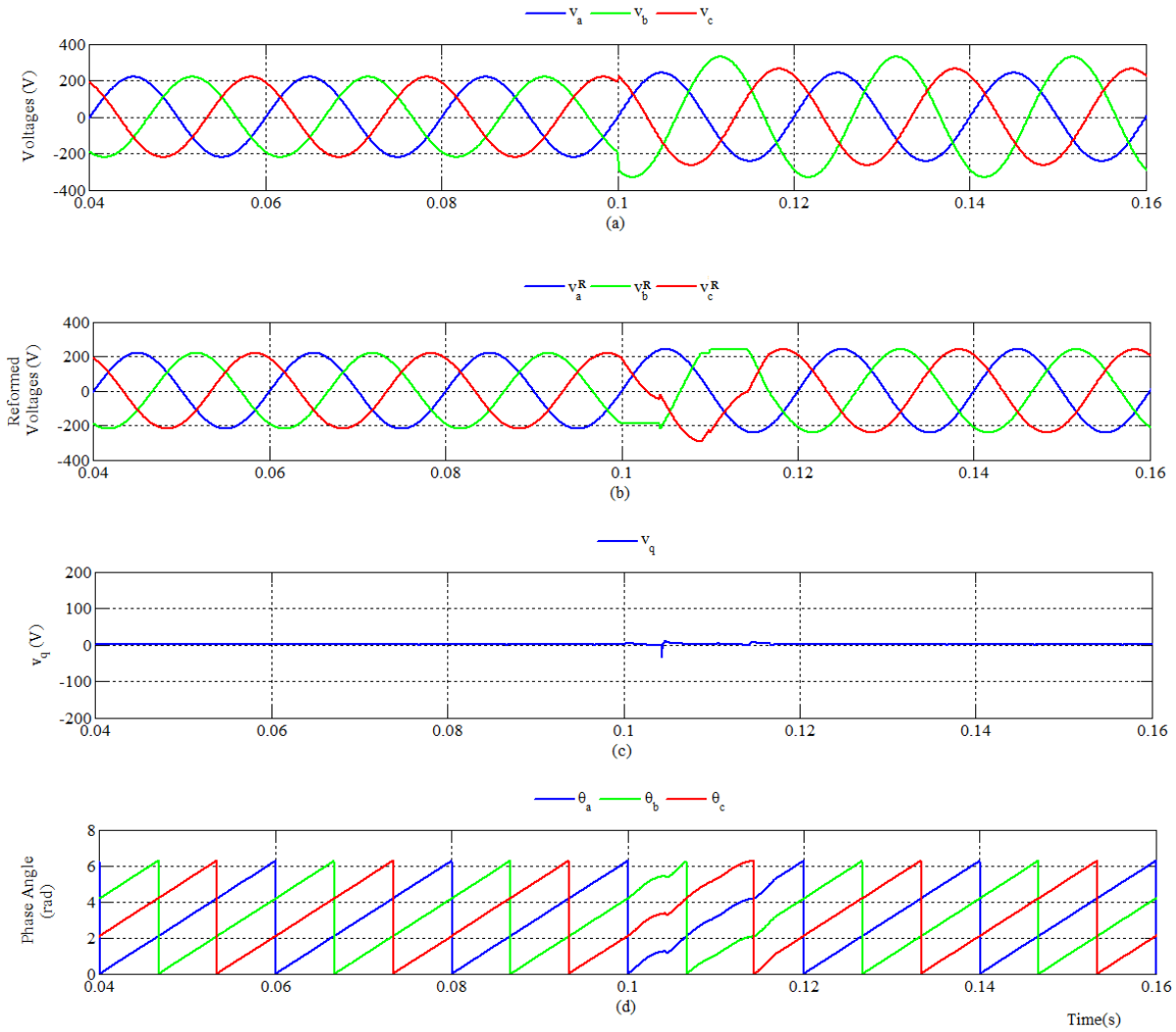

Figure 4.2: Performance of the developed PLL with voltage swell at all the phases. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.2.3: Case-A3: Simultaneous Voltage Sag and Voltage Swell at Different Phases

In this case, the three-phase system has suffered voltage sag in two of the phases and voltage swell in one phase. The phase-angle and the frequency remain unaltered. At 0.1 second, the voltage at phase-*b* swells up to 120% of its nominal value. The other two phases, phase-*a* and phase-*c*, drop to 70% and 40% respectively. The v_q vs time curve in Fig. 4.3(c) shows that the recovery time for this condition is also 0.0285 second. From case-A1, A2 and A3, it is noticed that the recovery time for estimation is higher and tends to attain a certain value when the change in amplitude is relatively high from nominal values.

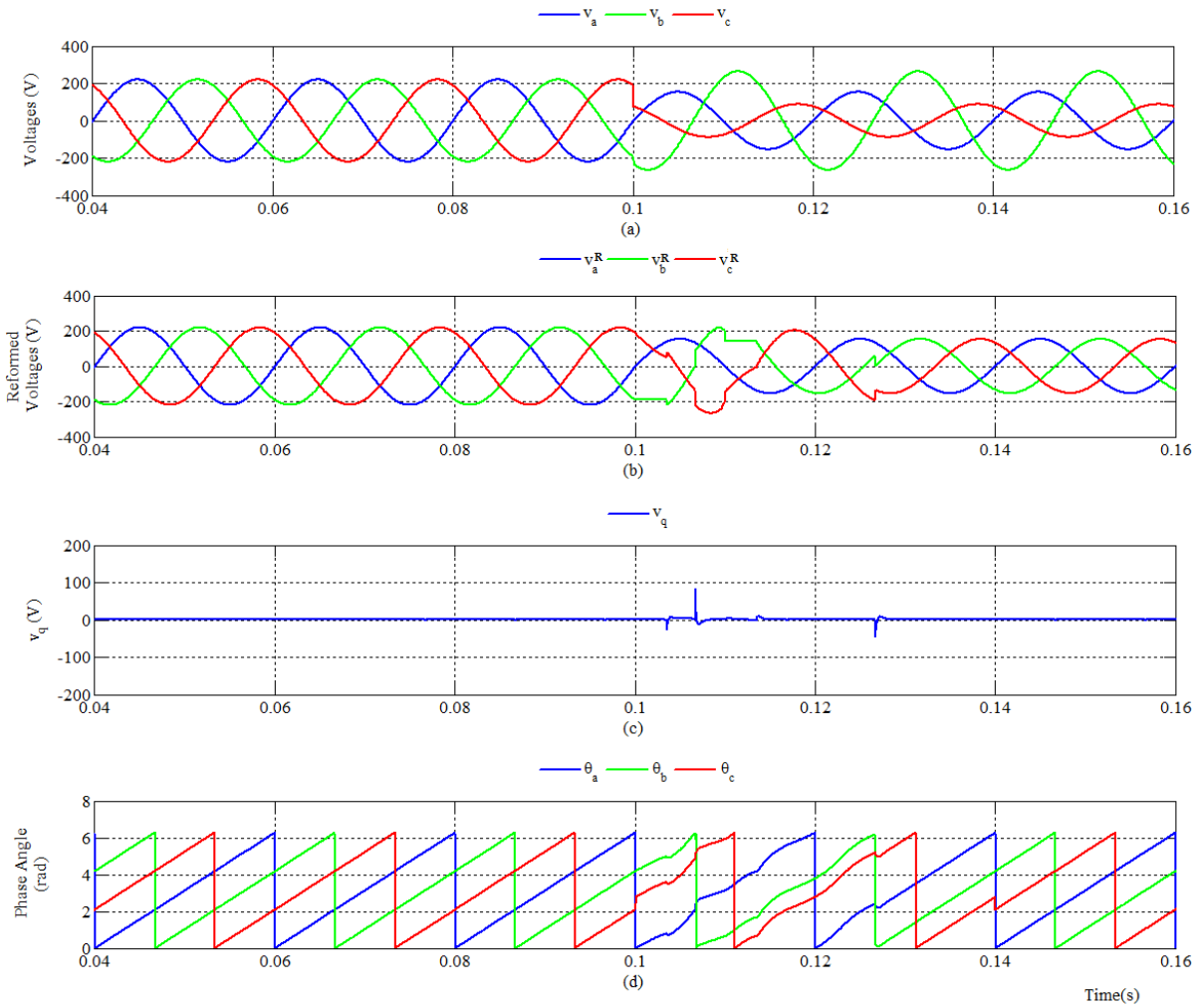

Figure 4.3: Performance of the developed PLL with voltage sag and voltage swell at different phases. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.2.4: Case-A4: Phase Shift of One Phase

In this case only one of the phases of the 220 Volt, 50 Hz three-phase balanced system suffers from sudden phase-shift at 0.1 second. The amplitudes of the phases are equal and the frequency is unaltered. Fig. 4.4 shows the response of the developed PLL when only phase-*b* shift 30° away from its nominal position. The recovery time is 0.0108 second. Fig 4.5 demonstrates another condition, when only the phase-*c* shifts 60° away from its nominal position. For the second case, the recovery time is only 0.005 second and the value of v_q is almost always zero. These two simulations reveal that the recovery time has dependency upon the phase-angle in between the phases. Though, the recovery is faster than the imbalance in amplitude.

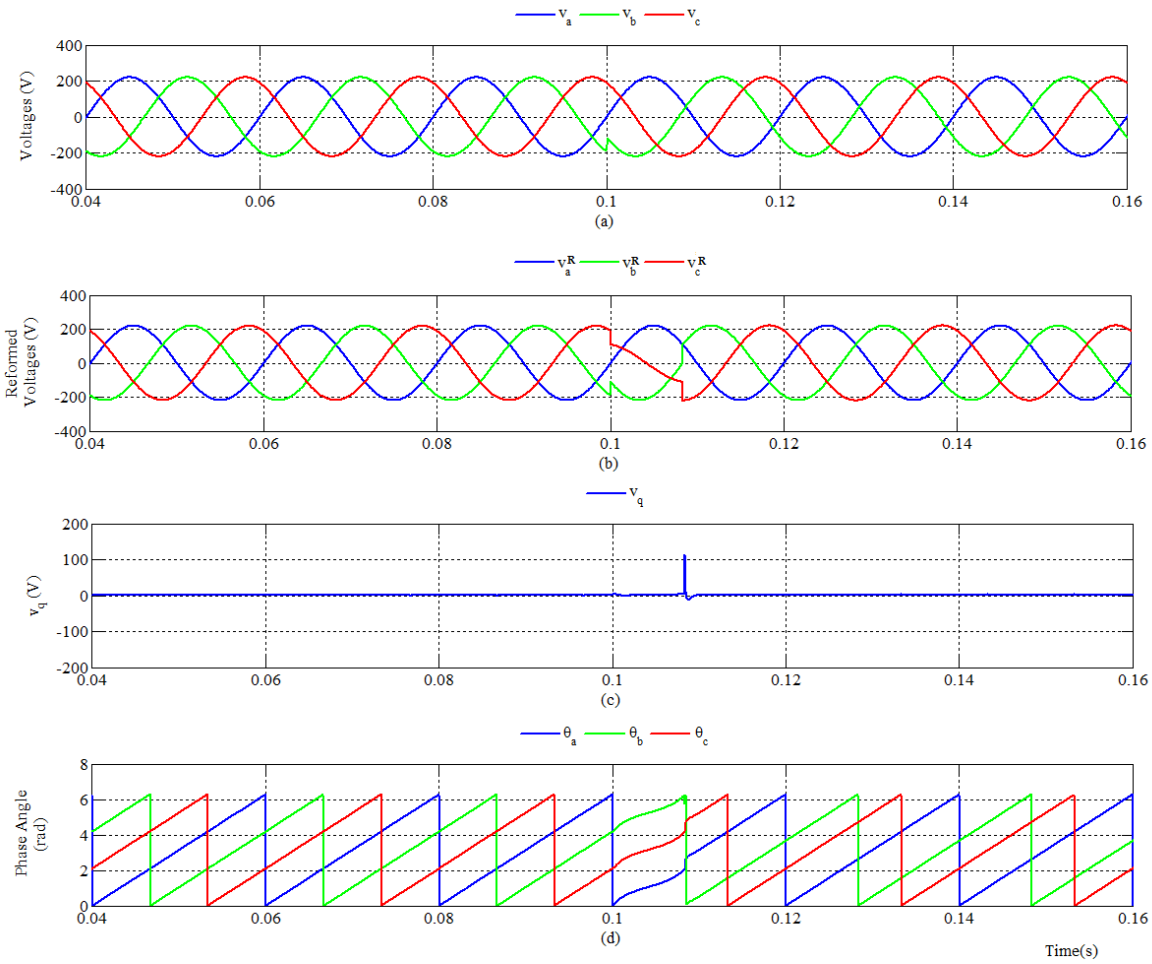

Figure 4.4: Performance of the developed PLL with sudden phase-shift of phase-*b*. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

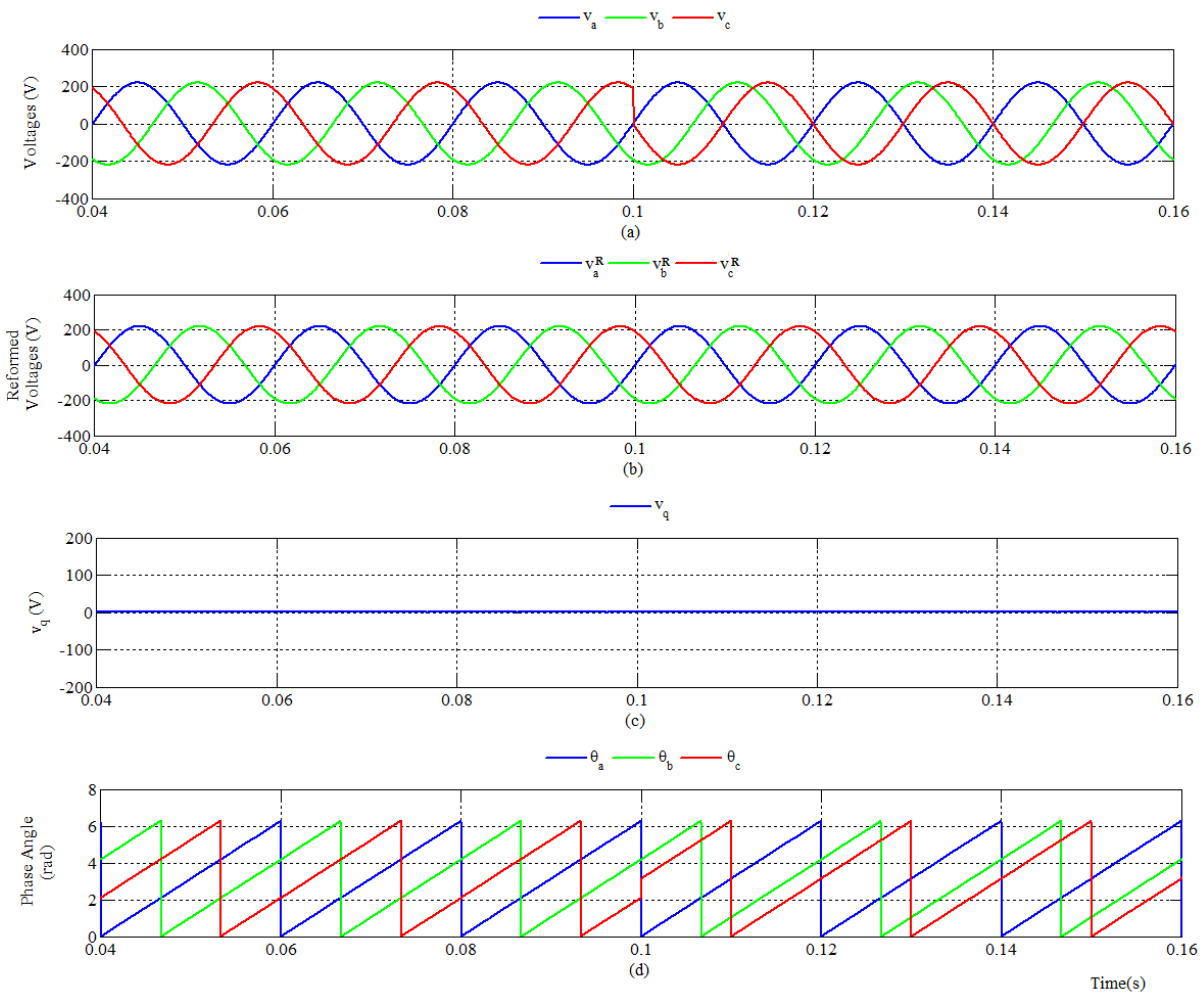

Figure 4.5: Performance of the developed PLL with sudden phase-shift of phase-*c*. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.2.5: Case-A5: Phase Shift of Two Phases

In this case, both the phase-*b* and phase-*c* suffers from a sudden phase shift of 60° and 30° respectively. The amplitudes of the three-phases remain equal and the frequency remains nominal. As shown in Fig. 4.5, the recovery time is 0.0126 second, a lot faster than the cases of amplitude imbalances. It is also possible that all the three phases of the system have been shifted from their positions. By considering one of them as base signal, the problem can be converted to same as case-A5.

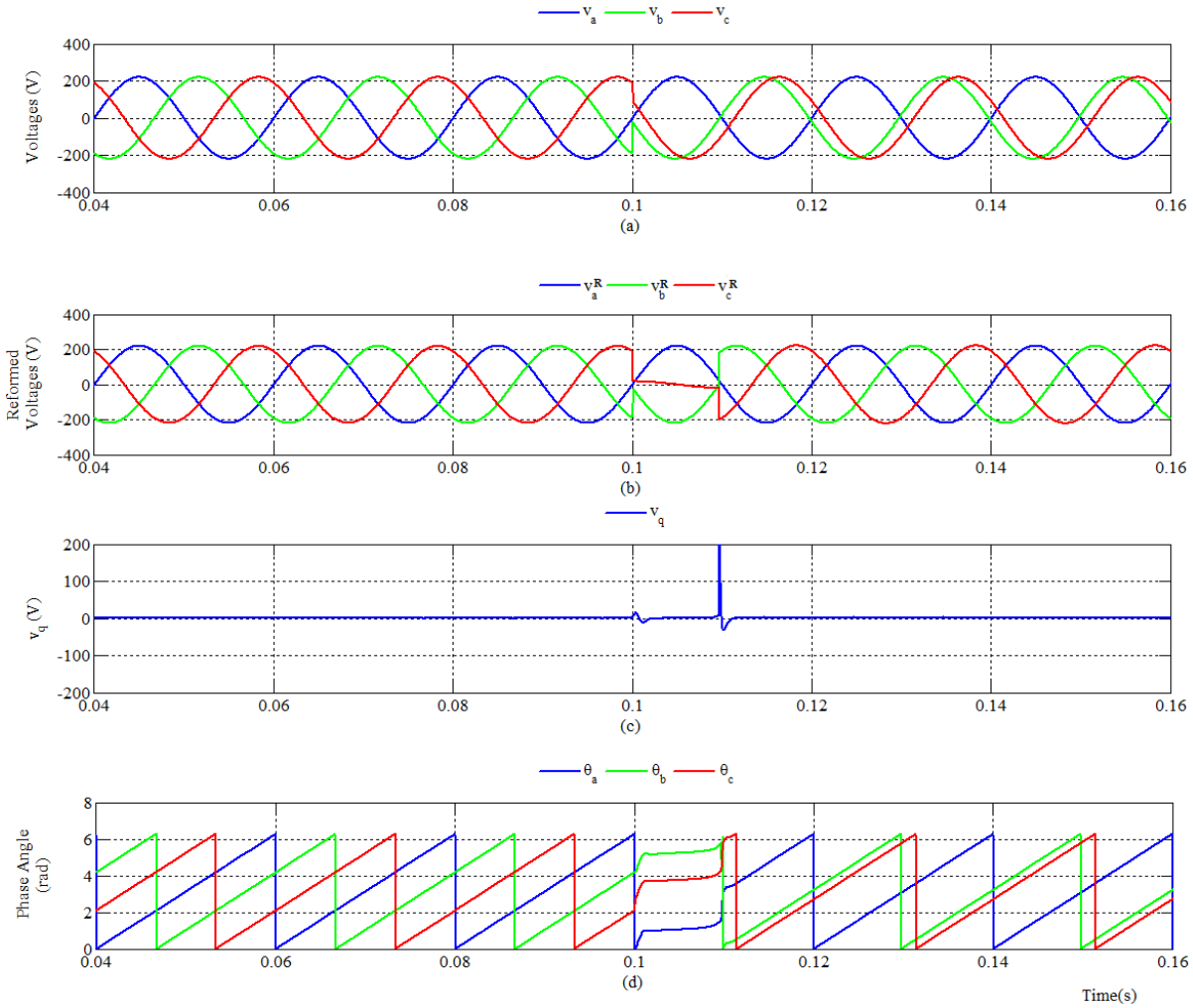

Figure 4.6: Performance of the developed PLL with sudden phase-shift of both phase-*b* and phase-*c*. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c

4.2.6: Case-A6: Simultaneous Amplitude Imbalance and Phase-Shift of All the Phases

In this case the 220 Volt, 50 Hz three-phase system has both the unequal amplitude and unequal phase-angle differences of the phases. For this simulation, phase-*a*, phase-*b* and phase-*c* undergoes 80%, 110% and 50% change in their amplitude respectively. At the same time, the two phases, phase-*b* and phase-*c* is shifted by 80° and 20°, shifting away from phase-*a*. Estimated phase angles are shown in Fig. 4.7(d). The response time is only 0.0242 second.

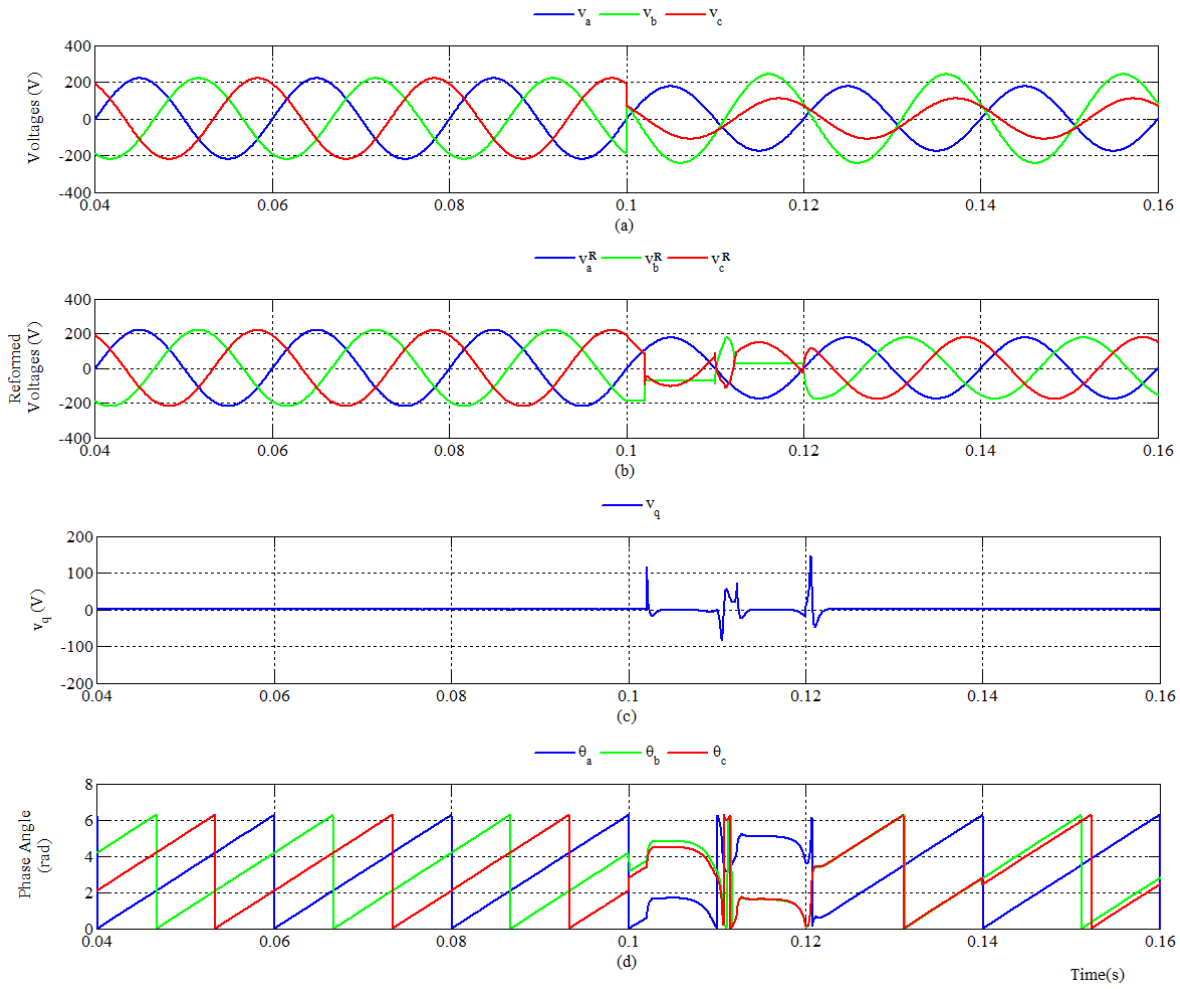

Figure 4.7: Performance of the developed PLL under unequal amplitude and unequal phase-angle differences of the phases (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.2.7: Case-A7: Balanced System at Frequency Other Than Nominal Value

The 50 Hz three-phase system has a sudden frequency drop from its nominal value at 0.1 second. For this simulation, a 5 Hz voltage drop has been chosen. The system is balanced otherwise. That is, the maximum amplitudes of the three phases are equal and the phase-angle differences between the phases are 120°. The performance is shown in Fig. 4.8 and the PLL can almost instantly estimate the system's phase-angle.

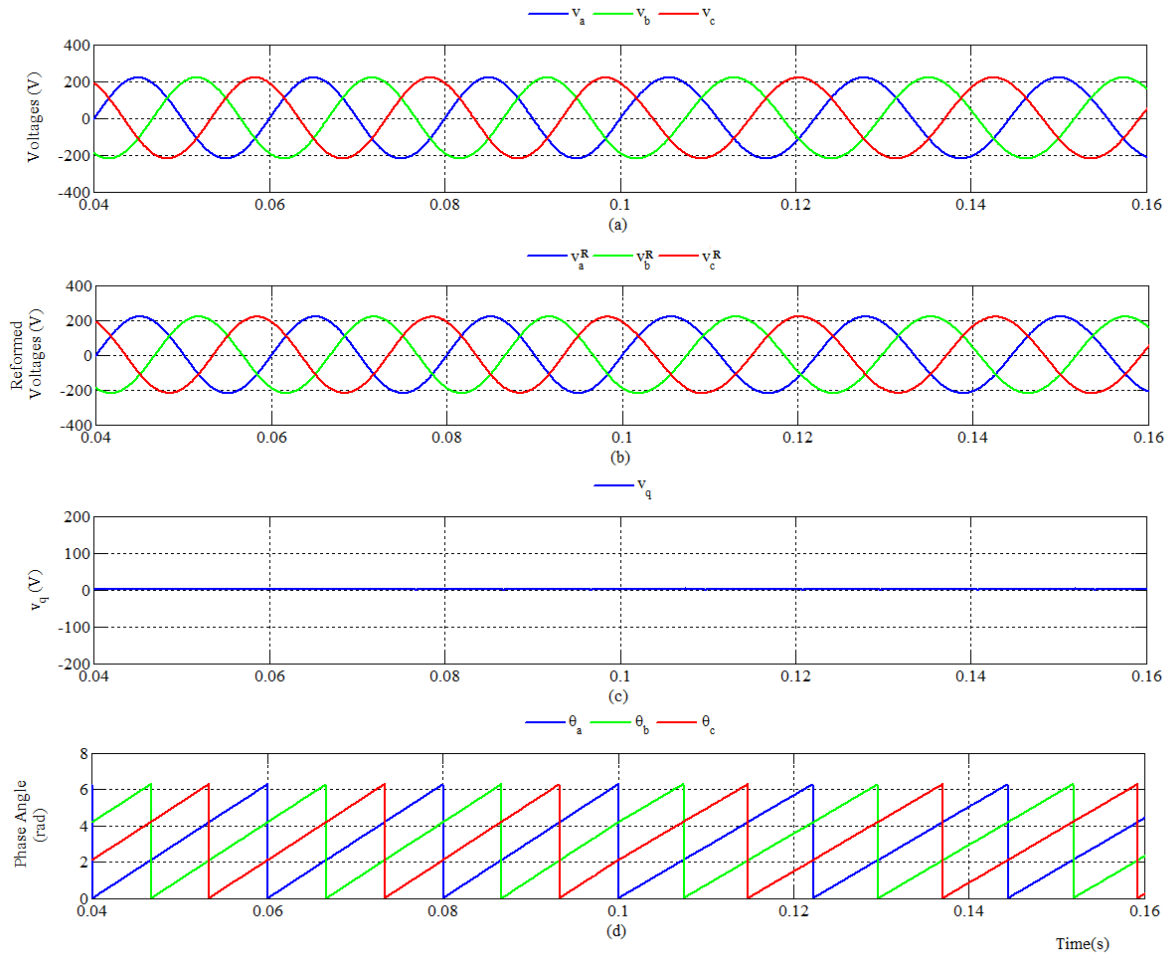

Figure 4.8: Performance of the developed PLL under balanced amplitude and equal phase-angle differences of the phases at 45 Hz. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

In the second case, the same balanced system has been used, except that, the frequency jumps by 5 Hz from its nominal value (from 50 Hz to 55 Hz). The performance is demonstrated in Fig. 4.9 and the recovery time is almost instant for this case also.

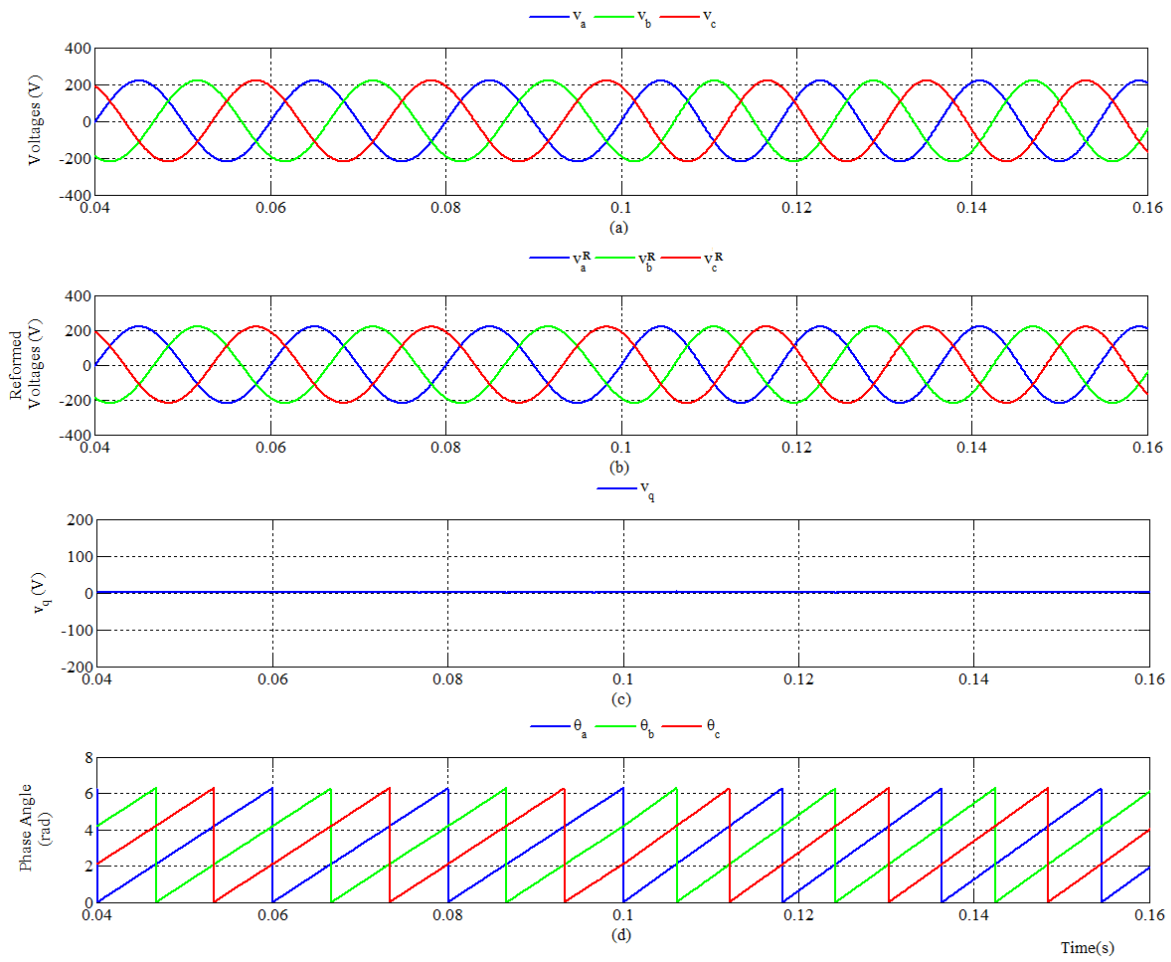

Figure 4.9: Performance of the developed PLL under balanced amplitude and equal phase-angle differences of the phases at 55 Hz. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.2.8: Case-A8: Amplitude Imbalance at Frequency Other Than Nominal Value

The 50 Hz three-phase system has a sudden frequency drop from its nominal value at 0.1 second. For this simulation, a 5 Hz voltage drop has been chosen. The amplitudes of the three phases are 80%, 50% and 30% of nominal their values respectively. The phase-angle differences between the phases remain same. The performance is shown in Fig. 4.10 and the recovery time for estimation is 0.0316 second.

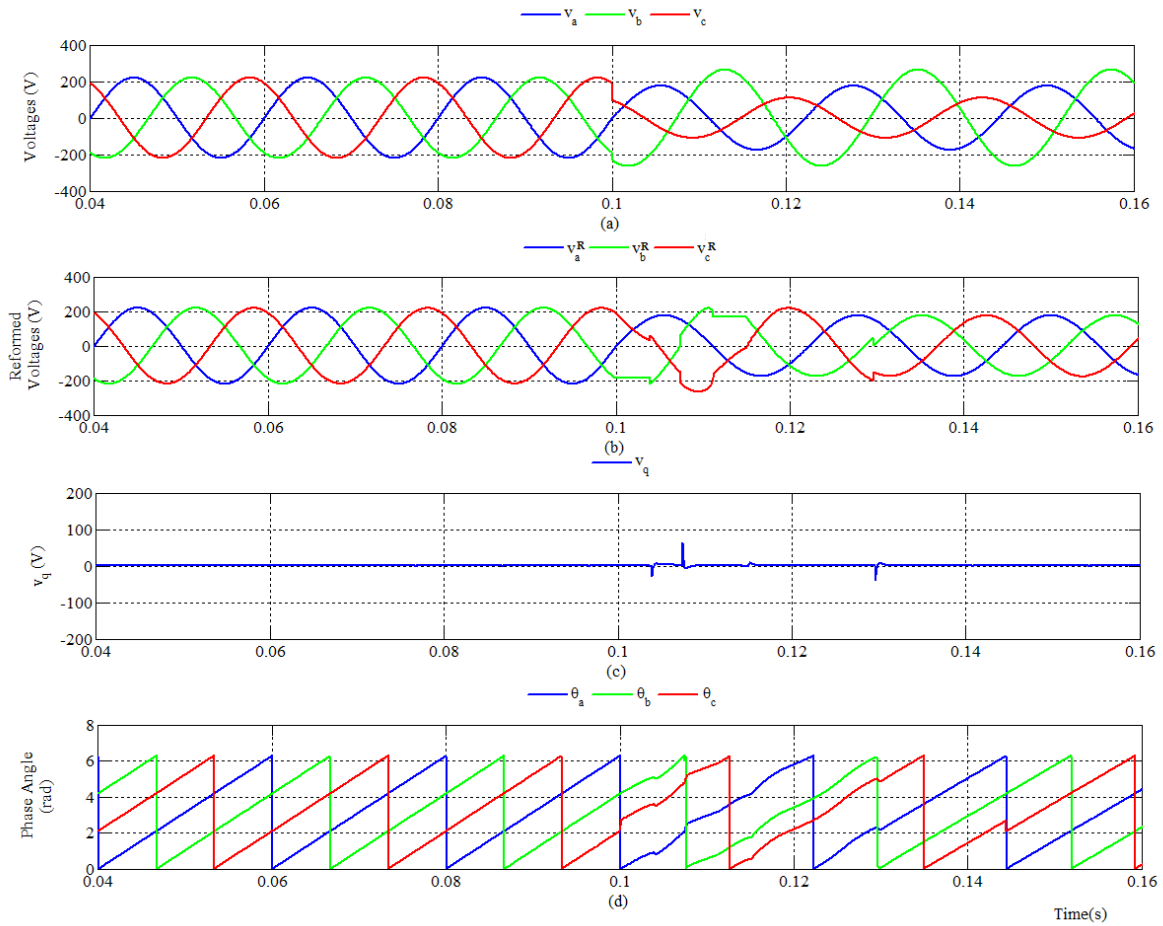

Figure 4.10: Performance of the developed PLL under amplitude imbalance but equal phase-angle differences of the phases at 45 Hz. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

In the second case, the same imbalanced system has been used, except that, the frequency jumps by 5 Hz from its nominal value (from 50 Hz to 55 Hz). The performance is demonstrated in Fig. 4.11 and the recovery time of the PLL for accurate phase-angle estimation is 0.0262 second.

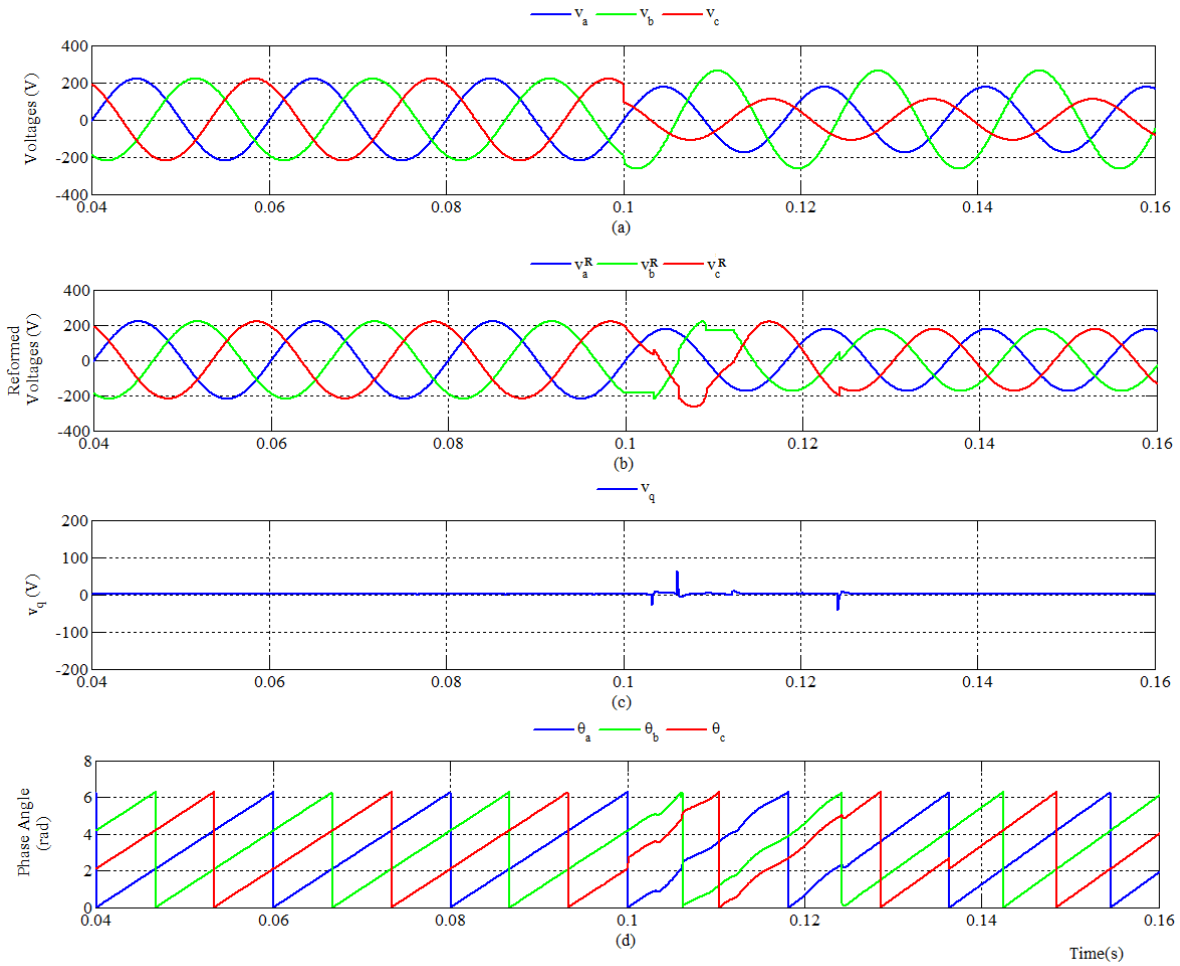

Figure 4.11: Performance of the developed PLL under amplitude imbalance but equal phase-angle differences of the phases at 55 Hz. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.2.9: Case-A9: Phase-Shift of the Phases at Frequency Other Than Nominal Value

In this case, the 50 Hz three phase system suffers a sudden frequency drop of 5 Hz at 0.1 second of simulation, when the phase-angle differences of the system is also altered. The amplitudes of the three phases remain properly balanced. For this case, the two phases (phase-*b* and phase-*c*) shift by 30° and 45° degree. Fig. 4.12 shows the performance of the developed PLL during this condition. It shows that, the PLL can successfully estimate the phase-angles of the system within 0.0109 second of disturbance of this type.

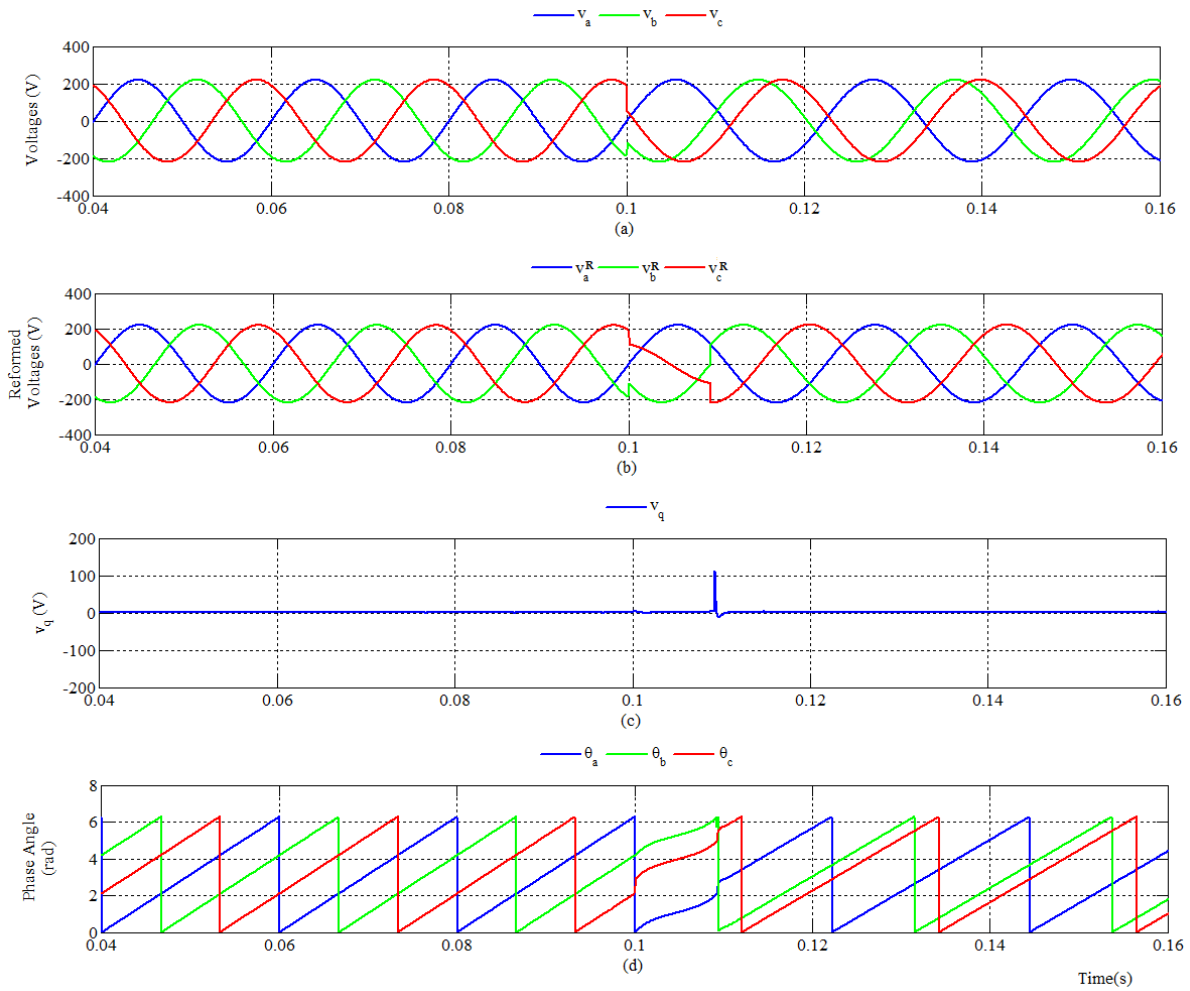

Figure 4.12: Performance of the developed PLL under balanced amplitudes of the phases but with unequal phase-angle differences at 45 Hz. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

In the second case, the 50 Hz three phase system suffers a sudden frequency jump of 5 Hz at 0.1 second of simulation, when the phase-angle differences of the system is also altered. The amplitudes of the three phases remain properly balanced. Also, for this case, the two phases (phase-*b* and phase-*c*) shift by 30° and 45° degree. Fig. 4.13 shows the performance of the developed PLL during this condition. It shows that, the PLL can successfully estimate the phase-angles of the system within 0.0109 second of disturbance.

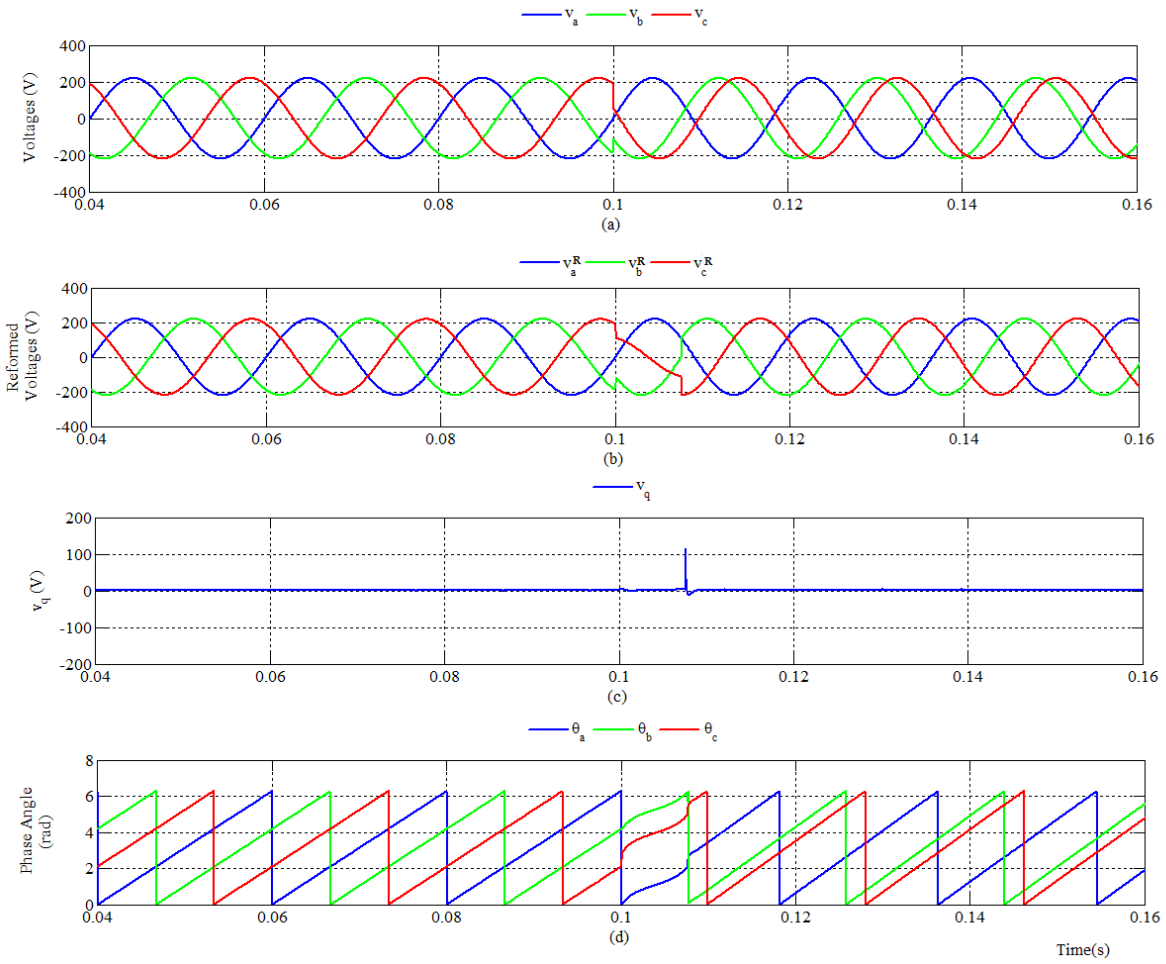

Figure 4.13: Performance of the developed PLL under balanced amplitudes of the phases but with unequal phase-angle differences at 55 Hz. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.2.10: Case-A10: Simultaneous Amplitude Imbalance and Phase-Shift of All the Phases at Frequency Other Than Nominal Value

The 50 Hz three-phase system has a sudden frequency drop from its nominal value at 0.1 second. For this simulation, a 5 Hz voltage drop has been chosen. The amplitudes of the three phases are 80%, 50% and 30% of nominal their values respectively. The two phases (phase-*b* and phase-*c*) also shift by 30° and 45° degree. The performance is shown in Fig. 4.14 and the recovery time for estimation is 0.0334 second.

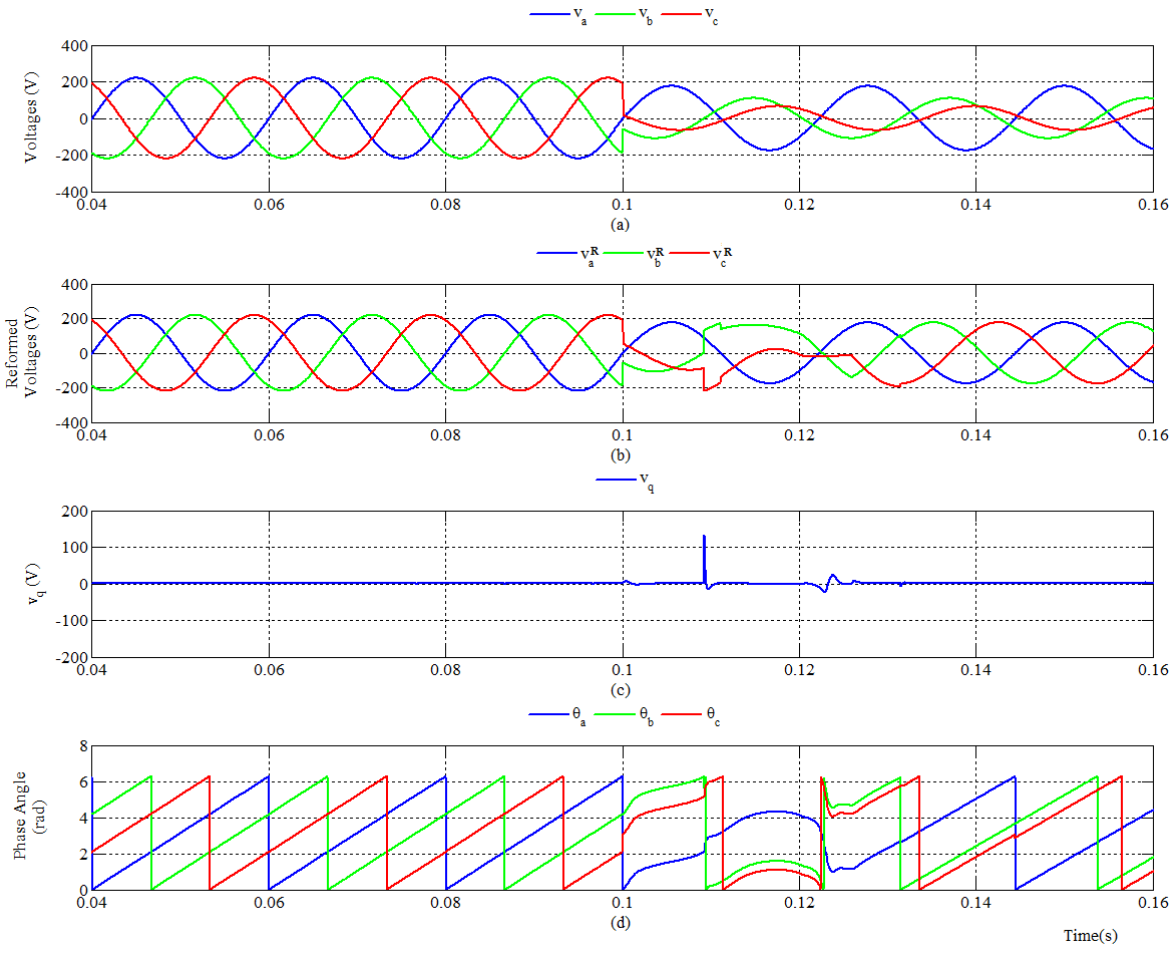

Figure 4.14: Performance of the developed PLL under unequal amplitude and unequal phase-angle differences of the phases at 45 Hz (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

In the second case, the same unbalanced system has been used, except that, the frequency jumps by 5 Hz from its nominal value (from 50 Hz to 55 Hz). The performance is demonstrated in Fig. 4.15 and the recovery time is 0.0278 second. The simulation results of Case-A7 to Case-A10 demonstrate that the developed PLL can also operate with accuracy when the frequency is not nominal. This characteristics of PLL has increased its application in the field of frequency and phase-angle estimation of grid voltage.

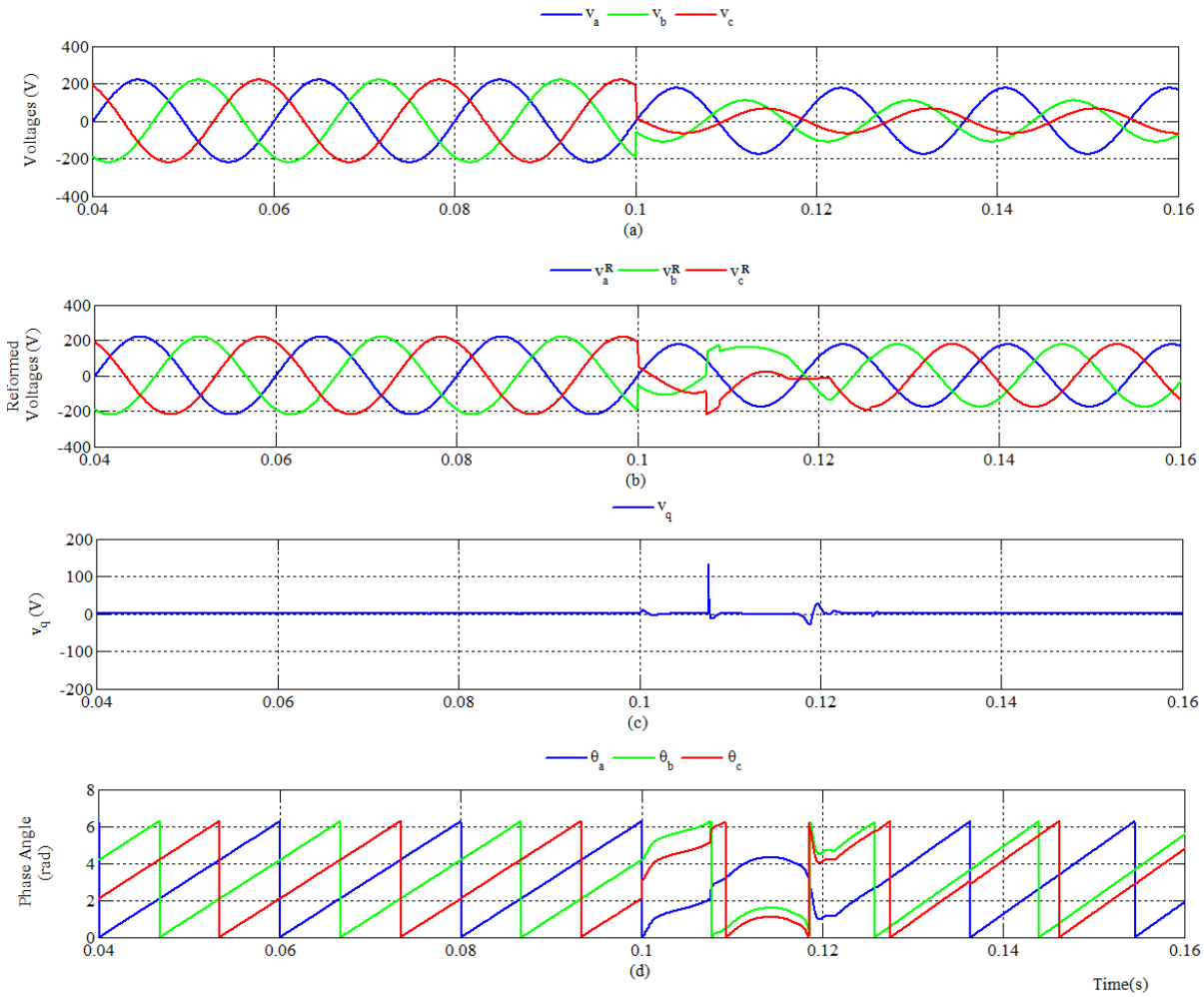

Figure 4.15: Performance of the developed PLL under unequal amplitude and unequal phase-angle differences of the phases at 55 Hz (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.3 Case-B: Three-Phase Grid Voltage with Harmonic Distortion

4.3.1: Case-B1: Balanced System Distorted by Harmonics

In this case, the performance of the developed PLL is observed when the grid is only under harmonics affected conditions. A 220 Volt, 50 Hz balanced three-phase system has been used for the simulation. Harmonics are added at 0.1 second of simulation. The maximum permissible amplitudes of harmonic components are set as per EN 50160 standard and IEEE 519-2014 standard. Although both standards are almost similar, the former one has THD higher than the latter one. For the rest of the cases, IEEE standard has been followed. Fig. 4.16 and Fig. 4.17 show the performance of the developed PLL under harmonics affected conditions respectively. For both cases, the recovery time is 0.0288 second.

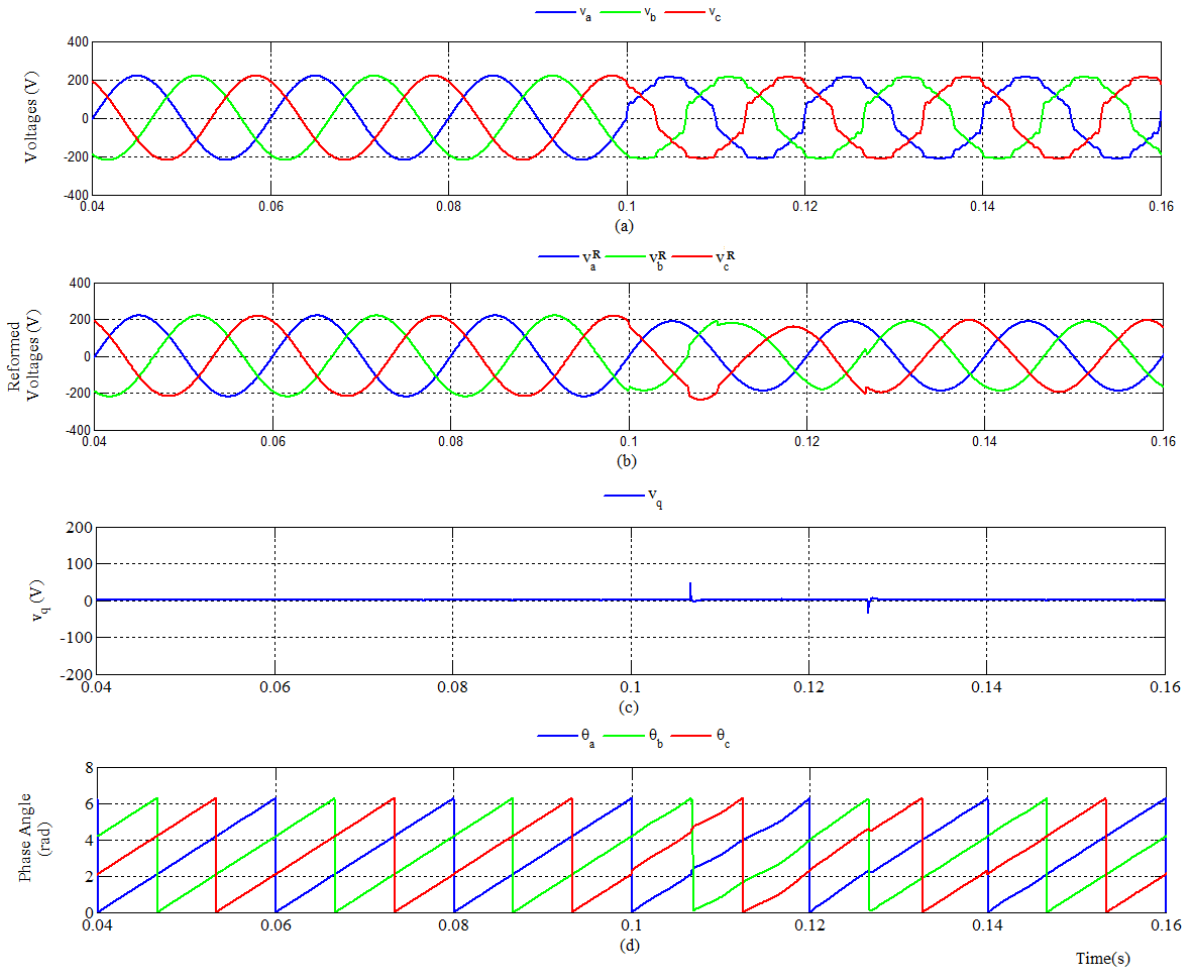

Figure 4.16: Performance of the developed PLL under harmonics affected condition (EN 50160 Standard) with a balanced system (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

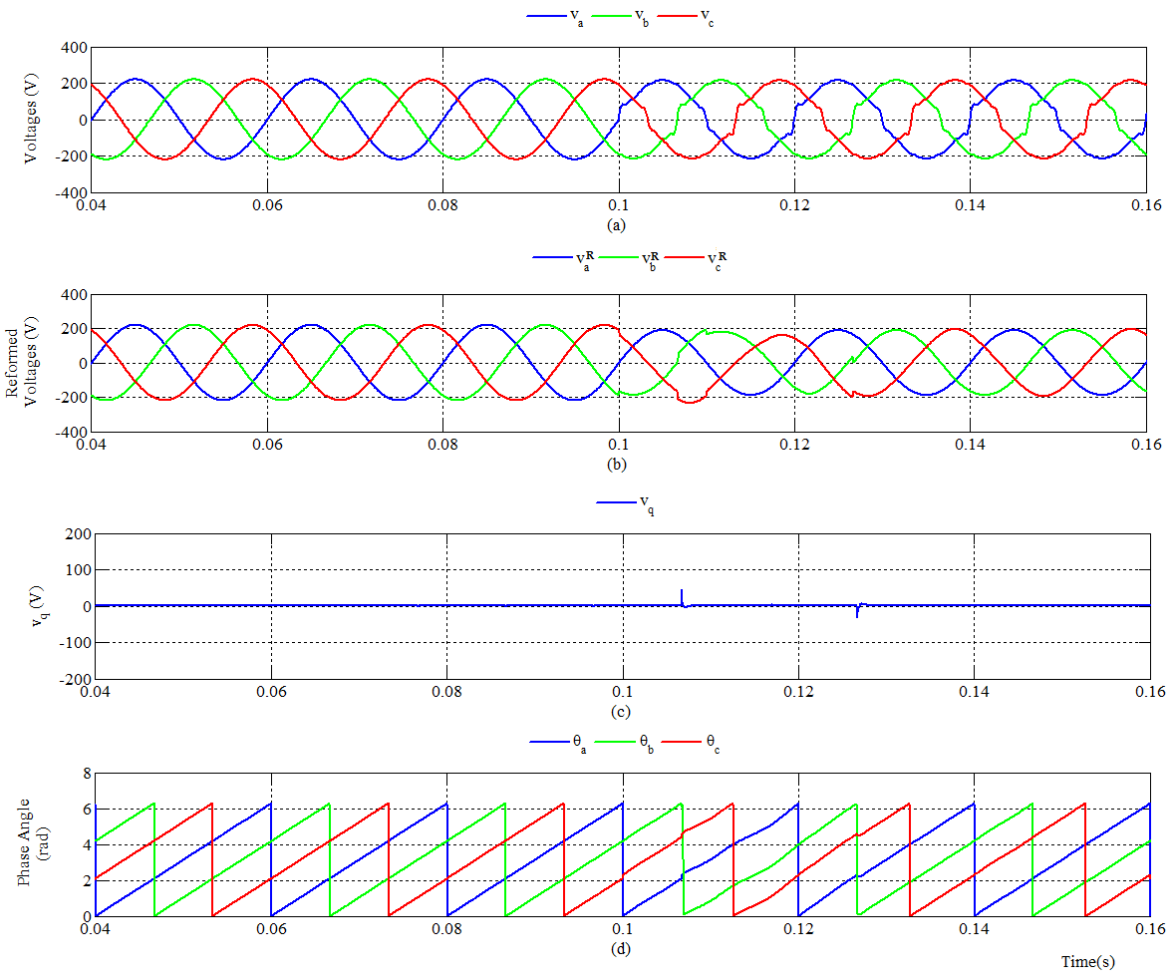

Figure 4.17: Performance of the developed PLL under harmonics affected condition (IEEE 519-2014 Standard) with a balanced system (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.3.2: Case-B2: Voltage Sag at All the Phases with Harmonic Distortion

In this case, the performance of the developed PLL is observed when all the phases of the system suffers from voltage sag at the presence of harmonics. At 0.1 second, phase-*a*, phase-*b* and phase-*c* of the 220 Volt, 50 Hz have voltage sag of 60%, 50% and 80% respectively of their nominal values. At the same time the system is affected by harmonics of maximum limit according to IEEE 519-2014 standard. Meanwhile, the phase-angle differences of the phases remain equal. The performance is shown in Fig. 4.18 with the properly reformed voltage (Fig. 4.18(b)) and estimated phase angle of the phases (Fig. 4.18(d)). The recovery time is 0.028 second.

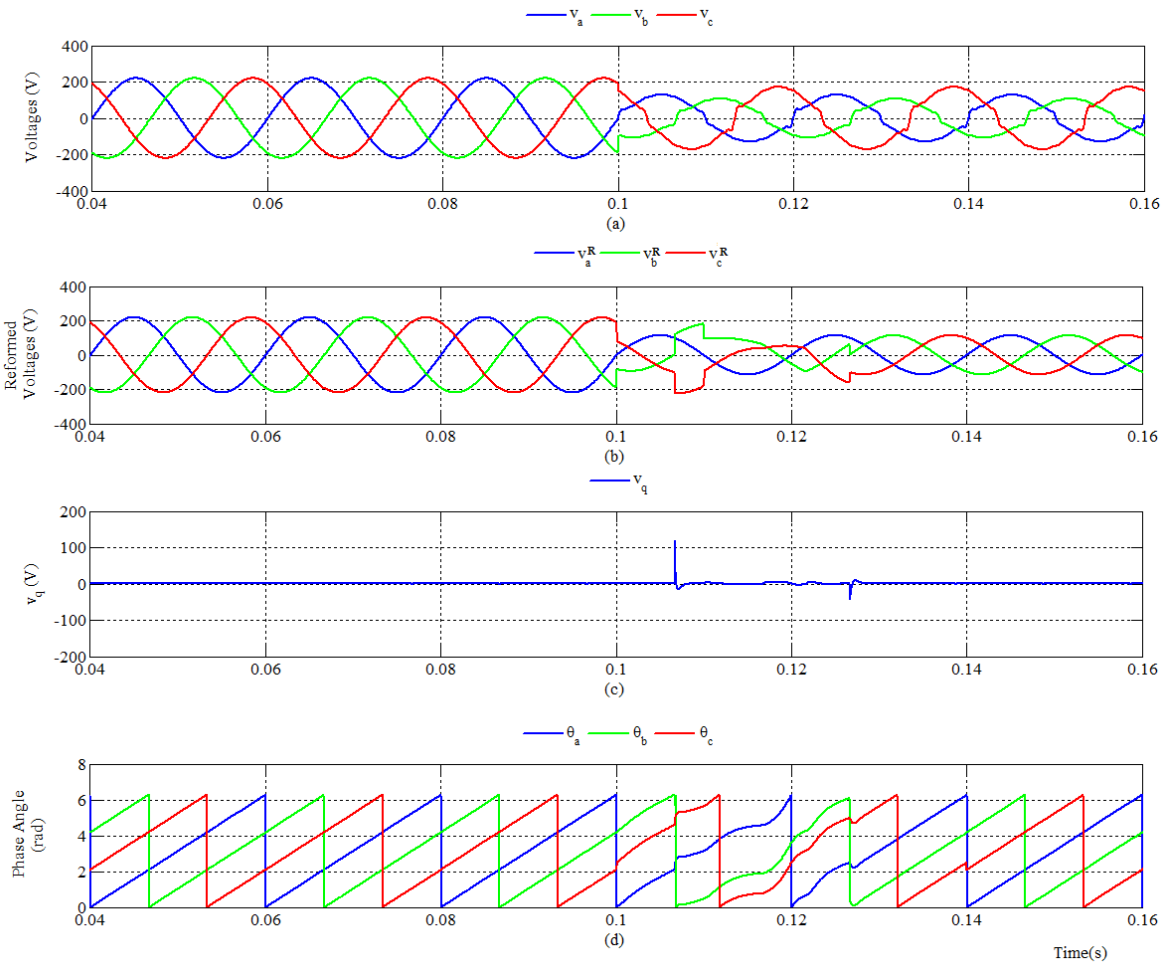

Figure 4.18: Performance of the developed PLL under harmonics affected condition (IEEE 519-2014 Standard) with a voltage sag at all the phases (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.3.3: Case-B3: Voltage Swell at All the Phases with Harmonic Distortion

The performance of the developed PLL is observed when all the phases of the system suffers from voltage swell with the presence of harmonics. At 0.1 second, phase-*a*, phase-*b* and phase-*c* of the 220 Volt, 50 Hz have voltage sag of 130%, 110% and 120% respectively of their nominal values. At the same time the system is affected by harmonics. The performance is shown in Fig. 4.19 with the properly reformed voltage (Fig. 4.19(b)) and estimated phase angle of the phases (Fig. 4.19(d)). The recovery time is 0.005 second. Since the amplitudes of the phases are relatively nearer to themselves, the recovery time decreased noticeable.

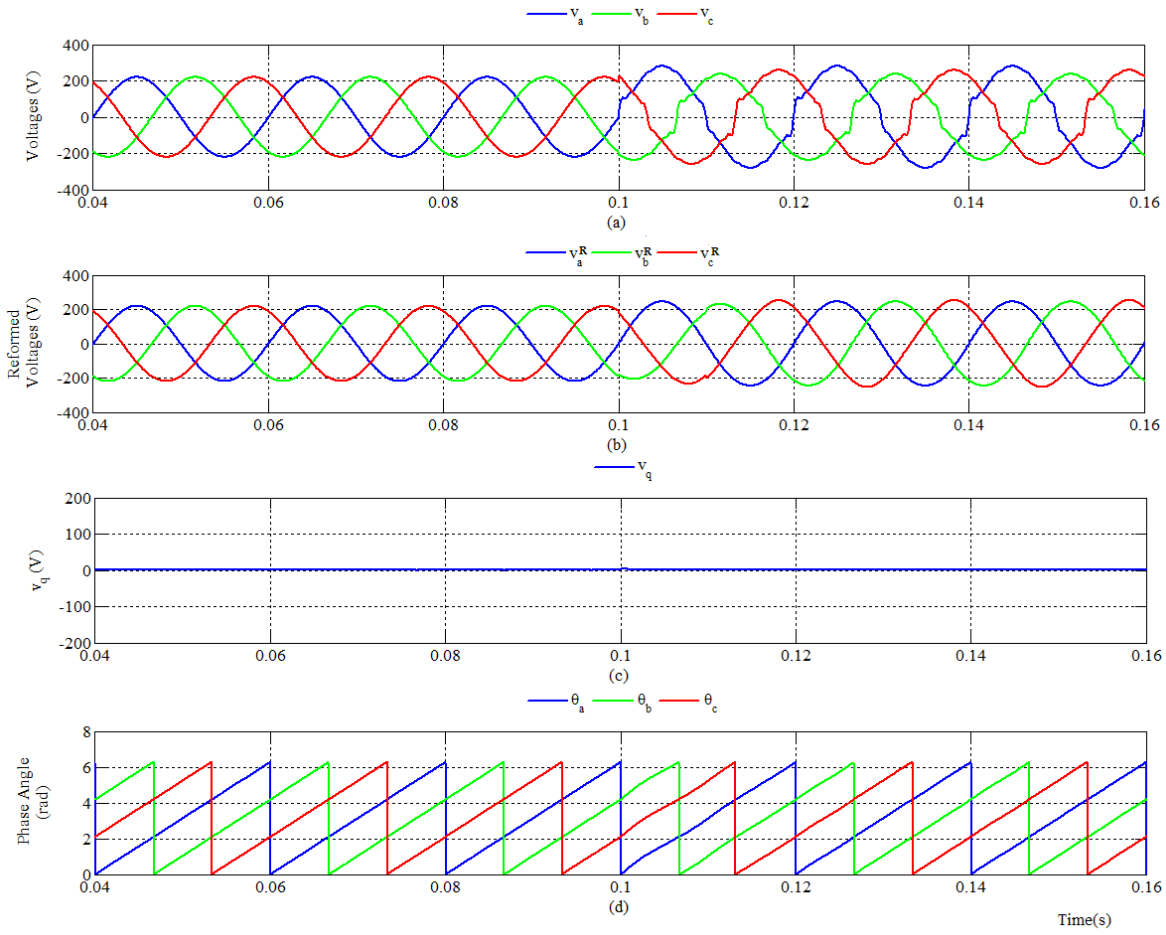

Figure 4.19: Performance of the developed PLL under harmonics affected condition (IEEE 519-2014 Standard) with a voltage swell at all the phases (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.3.4: Case-B4: Simultaneous Voltage Sag and Voltage Swell at Different Phases with Harmonic Distortion

At 0.1 second, the three phases change their amplitude to 80%, 120% and 60% respectively from their nominal values. The phase-angle differences remain equal and unchanged. The system is also harmonics affected. The performance of the developed PLL is observed in Fig. 4.20. The PLL can accurately estimate the phase angles within 0.0293 second of disturbance.

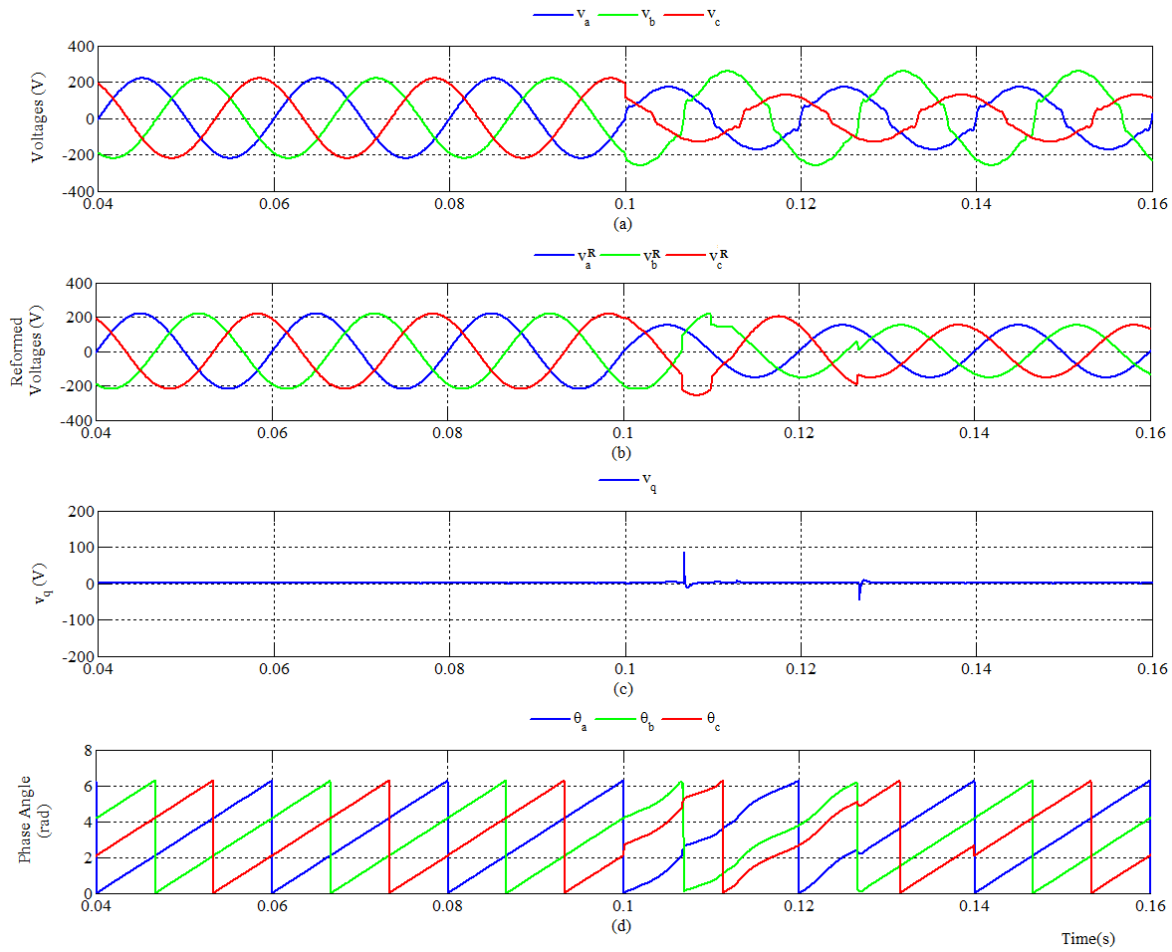

Figure 4.20: Performance of the developed PLL under harmonics affected condition (IEEE 519-2014 Standard) with different amplitudes at all the phases (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.3.5: Case-B5: Phase Shift of One Phase with Harmonic Distortion

In this case the balanced three-phase system suffers from phase-shift of one phases and becomes affected by harmonics at 0.1 second. Fig. 4.21 and Fig. 4.22 are two simulation results under this criteria. In Fig. 4.21(a), phase-*b* of the 220 Volt, 50 Hz system shifted by 45° from phase-*a*, while in Fig. 4.22(a), phase-*c* shifted by 25°. The harmonics is according to the maximum limit of IEEE 519-2014 standard. The response time for the mentioned two cases are 0.027 second and 0.0288 second.

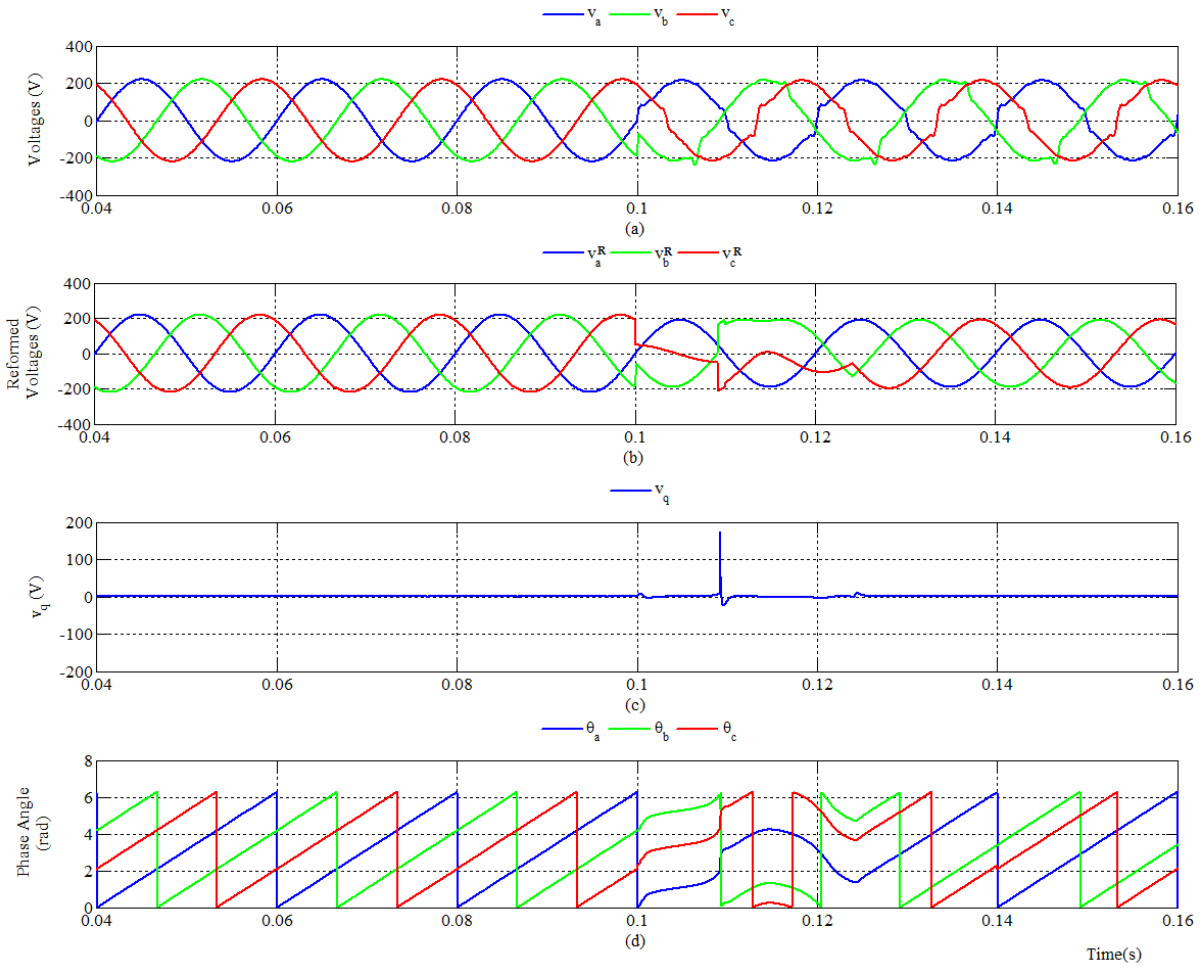

Figure 4.21: Performance of the developed PLL under harmonics affected condition with phase shift of phase-*b* (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

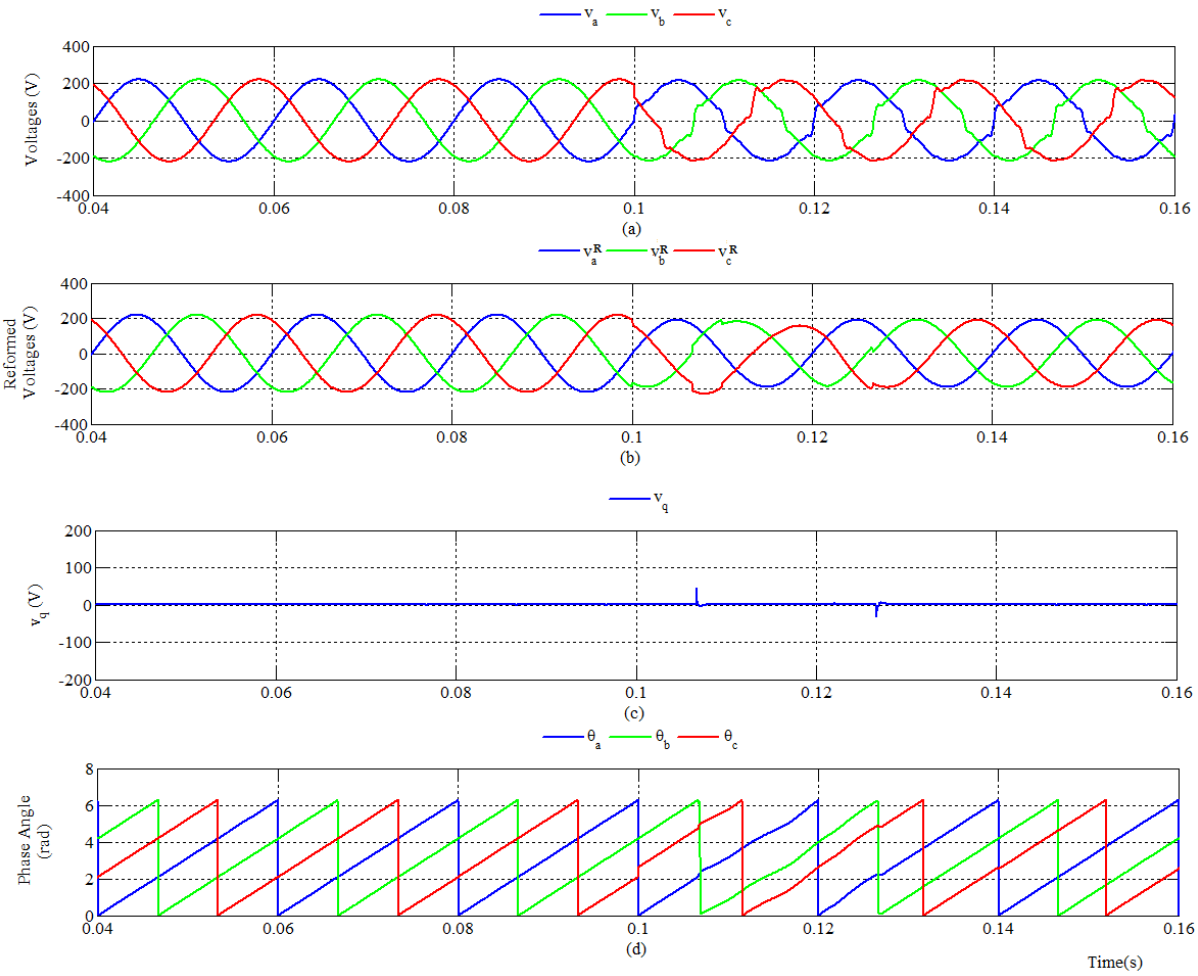

Figure 4.22: Performance of the developed PLL under harmonics affected condition with phase shift of phase-*c* (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.3.6: Case-B6: Phase Shift of Two Phases with Harmonic Distortion

In this case the balanced three-phase system suffers from phase-shift of all the phases and becomes affected by harmonics at 0.1 second. Fig. 4.23 shows the performance of the developed PLL when phase-*b* and phase-*c* suffers from phase shift of 20° and 50° respectively. The amplitudes of the harmonic components are from IEEE 519-2014 standards as usual. The performance is demonstrated in Fig. 4.23(b) and Fig. 4.23(c). The estimated phase-angles are shown in Fig. 4.23(d). The system responds accurately within 0.0293 seconds.

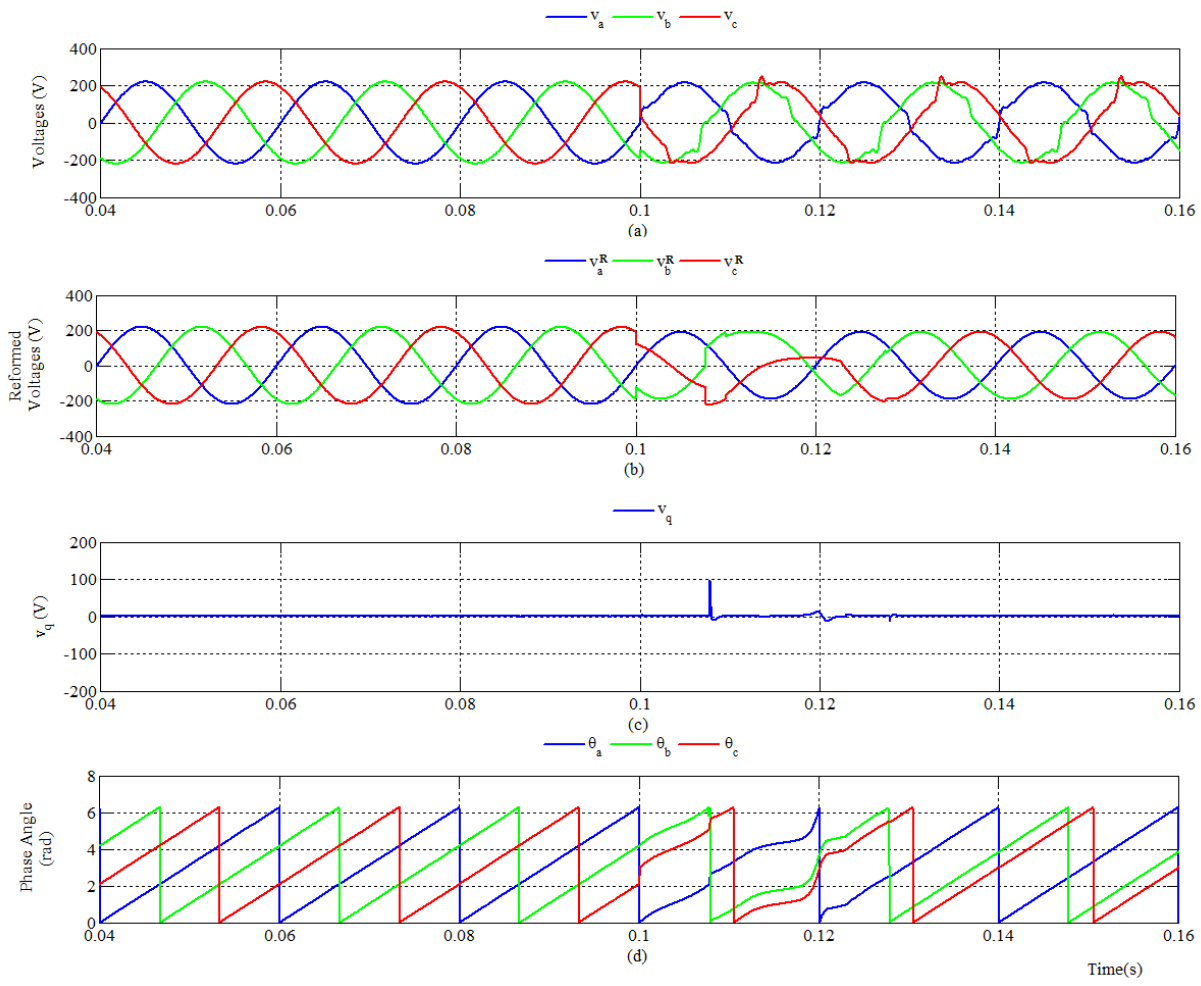

Figure 4.23: Performance of the developed PLL under harmonics affected condition with phase shift of all the phases. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.3.7: Case-B7: Simultaneous Amplitude Imbalance and Phase-Shift of All the Phases with Harmonic Distortion

The three-phase 220 Volt, 50 Hz signal simultaneously suffers from amplitude and phase-angle imbalances along with the disturbance of harmonic components. The amplitude of the three phase changes into 80%, 110% and 50% of their nominal values at 0.1 second. At the same time phase-*b* and phase-*c* shifts sway from phase-*a* by 30° and 45° respectively. The amplitude of harmonics are as in the previous cases. The performance of the PLL is demonstrated in Fig. 4.24 showing that it can estimate the phase angles of all the phases within 0.038 second.

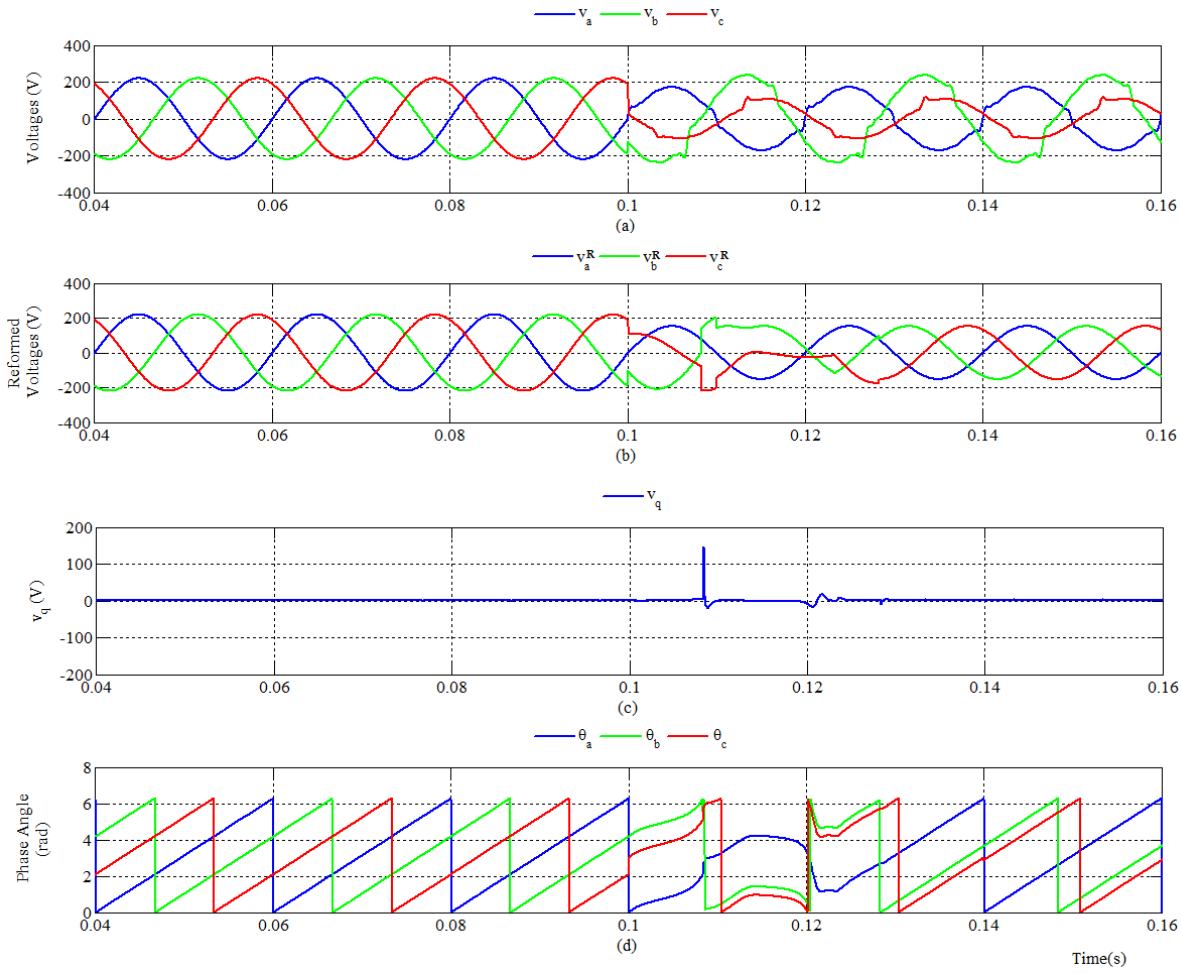

Figure 4.24: Performance of the developed PLL under harmonics affected condition with both amplitude imbalance and phase shift of all the phases. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.2.8: Case-B8: Harmonics Affected Balanced System at Frequency Other Than Nominal Value

In this case, the performance of the developed PLL is observed when the grid is harmonics affected and operating at a frequency lower than the nominal value. A 220 Volt, 50 Hz balanced three-phase system has been used for the simulation. Harmonics are added at 0.1 second of simulation. Also, at that moment, the frequency suddenly drops to 45 Hz from its nominal value. The maximum permissible amplitudes of harmonic components are set as per IEEE 519-2014 standard. Fig. 4.25 shows the performance of the developed PLL under harmonics affected standard respectively. The recovery time of the PLL is 0.0308 second.

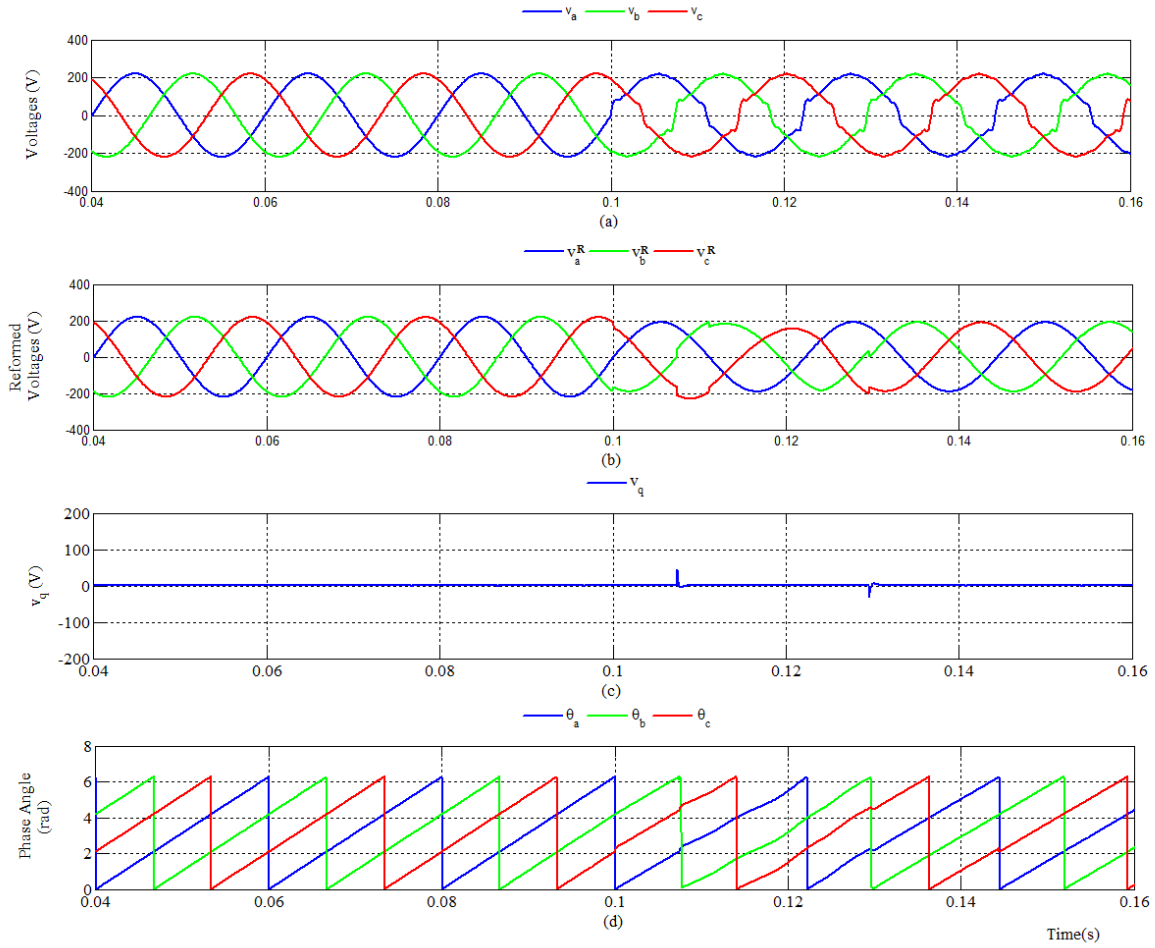

Figure 4.25: Performance of the developed PLL under harmonics affected condition with balanced three-phase system and at 45 Hz. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

In the second case, the same system is operated except, at fault, the frequency of the three-phase system jumps to 55 Hz from its nominal value. The performance of the developed PLL in this condition is shown in Fig. 4.26. The recovery time for estimation is 0.0269 second.

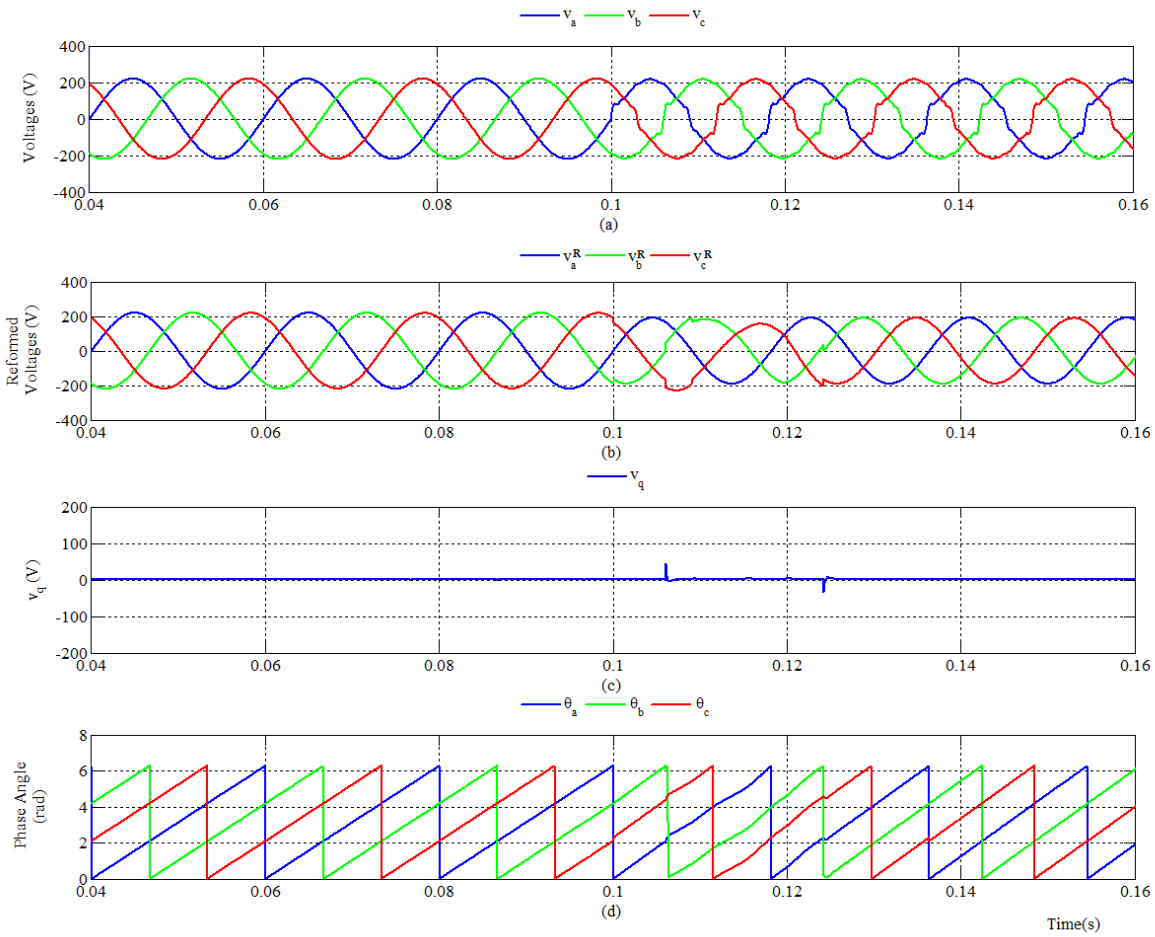

Figure 4.26: Performance of the developed PLL under harmonics affected condition with balanced three-phase system and at 55 Hz. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.2.9: Case-B9: Amplitude Imbalance with Harmonic Distortion at Frequency Other Than Nominal Value

The 50 Hz three-phase system has a sudden frequency drop from its nominal value at 0.1 second as well as being affected by harmonics. For this simulation, a 5 Hz voltage drop has been chosen. The amplitudes of the three phases are 80%, 50% and 30% of nominal their values respectively. The phase-angle differences between the phases remain equal. The performance is shown in Fig. 4.27 and the recovery time for estimation is 0.0316 second.

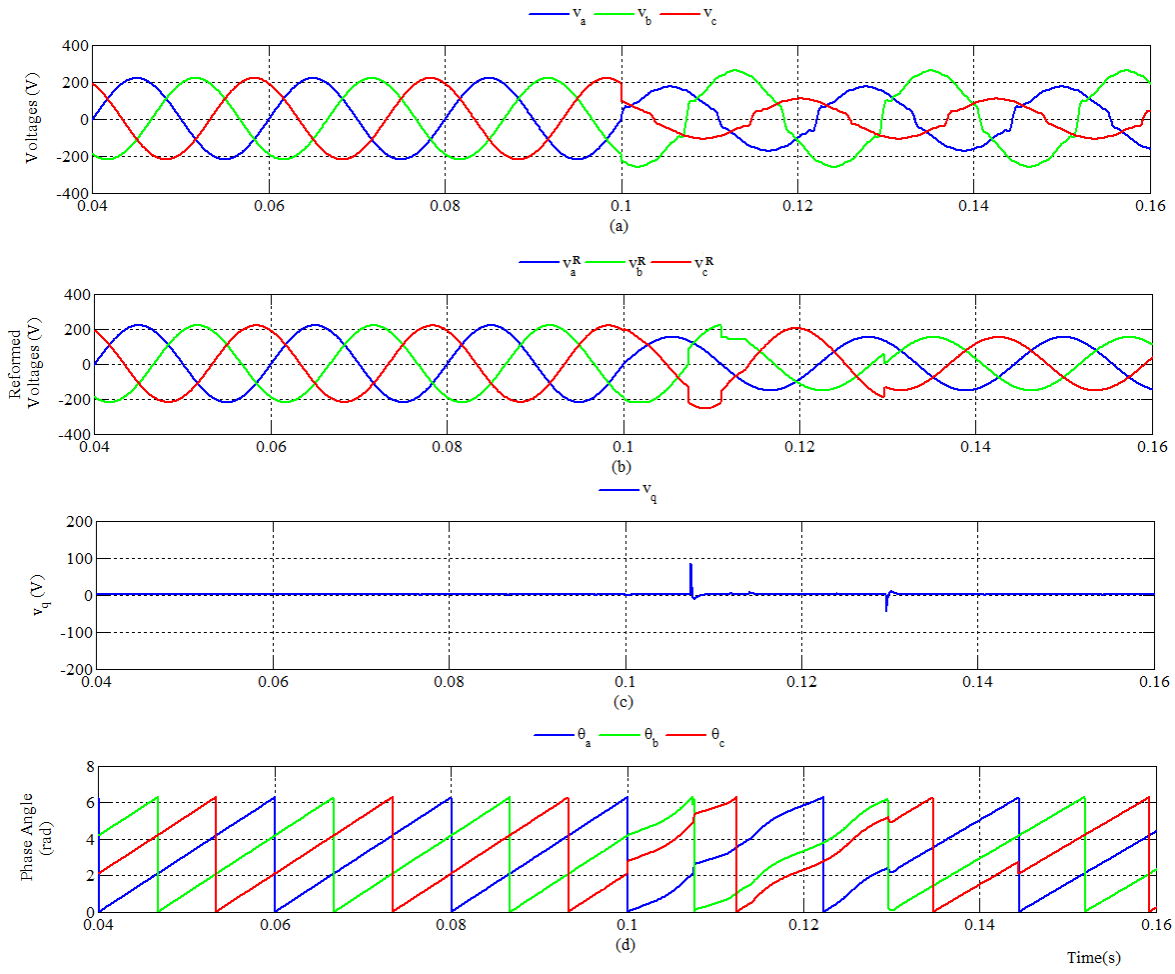

Figure 4.27: Performance of the developed PLL under amplitude imbalance but equal phase-angle differences of the phases at 45 Hz accompanied by harmonic distortion. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c

In the second case, the same imbalanced harmonics affected system has been used, except that, the frequency jumps by 5 Hz from its nominal value (from 50 Hz to 55 Hz). The performance is demonstrated in Fig. 4.28 and the recovery time of the PLL for accurate phase-angle estimation is 0.0269 second.

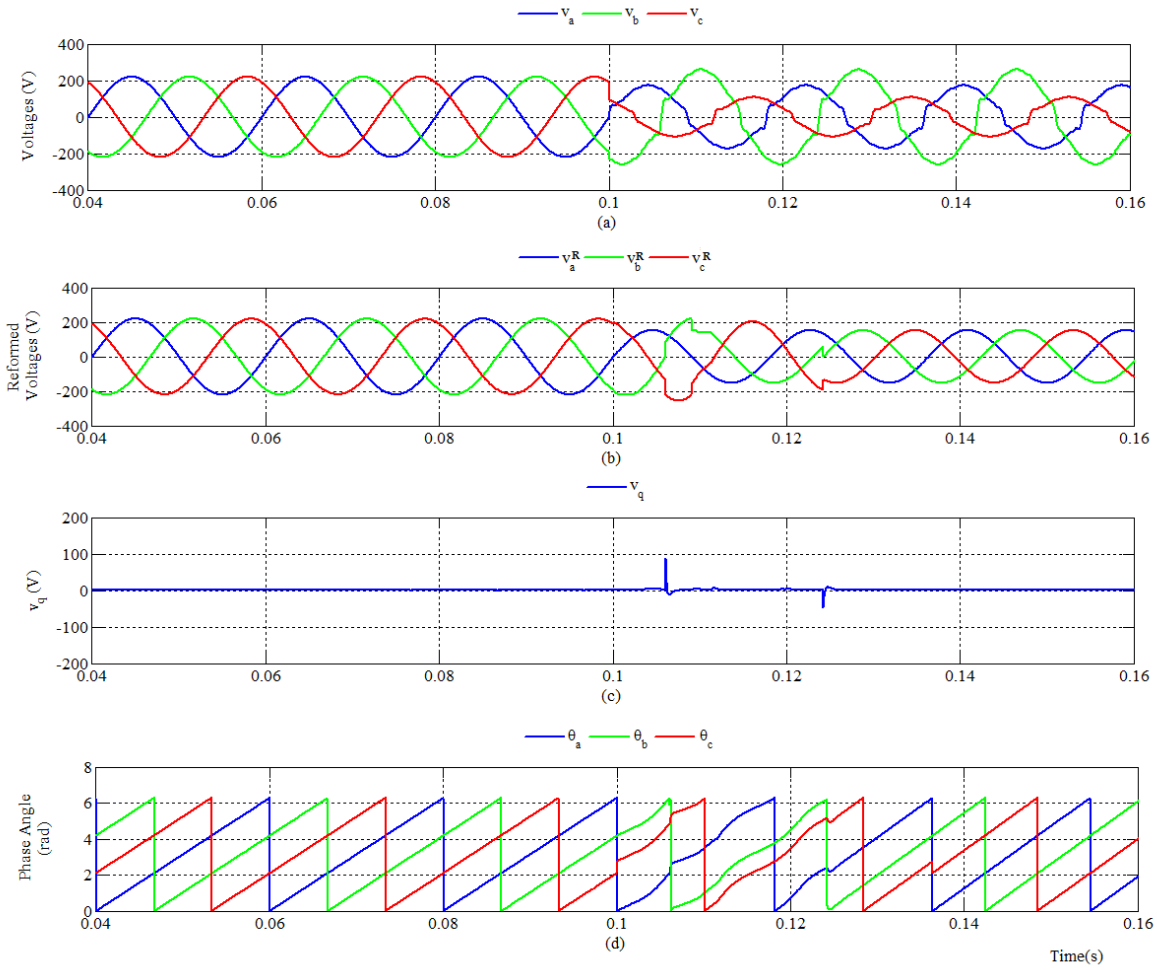

Figure 4.28: Performance of the developed PLL under amplitude imbalance but equal phase-angle differences of the phases at 55 Hz accompanied by harmonic distortion. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c

4.2.10: Case-B10: Phase-Shift of the Phases with Harmonic Distortion at Frequency Other Than Nominal Value

In this case, the 50 Hz three phase system suffers a sudden frequency drop of 5 Hz at 0.1 second accompanied by harmonic distortion. The phase-angle differences of the system is also altered while the amplitudes of the three phases remain properly balanced. For this case, the two phases (phase-*b* and phase-*c*) shift by 30° and 45° degree. Fig. 4.29 shows the performance of the developed PLL during this condition. It shows that, the PLL can successfully estimate the phase-angles of the system within 0.0322 second.

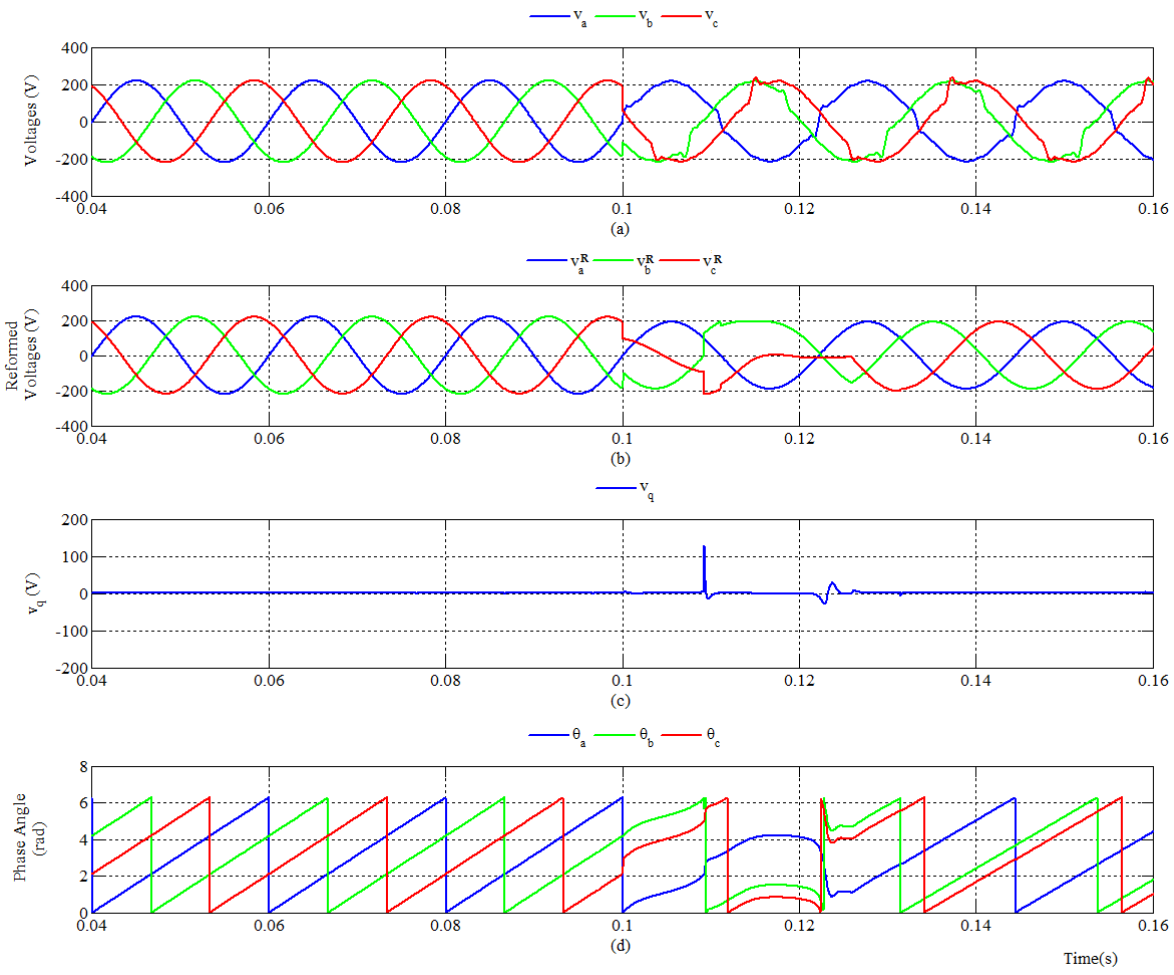

Figure 4.29: Performance of the developed PLL under balanced amplitudes of the phases but with unequal phase-angle differences at 45 Hz accompanied by harmonic distortion. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

In the second case, the 50 Hz harmonics affected three phase system suffers a sudden frequency jump of 5 Hz at 0.1 second of simulation, when the phase-angle differences of the system is also altered. The amplitudes of the three phases remain properly balanced. Also, for this case, the two phases (phase-*b* and phase-*c*) shift by 30° and 45° degree. Fig. 4.30 shows the performance of the developed PLL during this condition. It shows that, the PLL can successfully estimate the phase-angles of the system within 0.0266 second of disturbance.

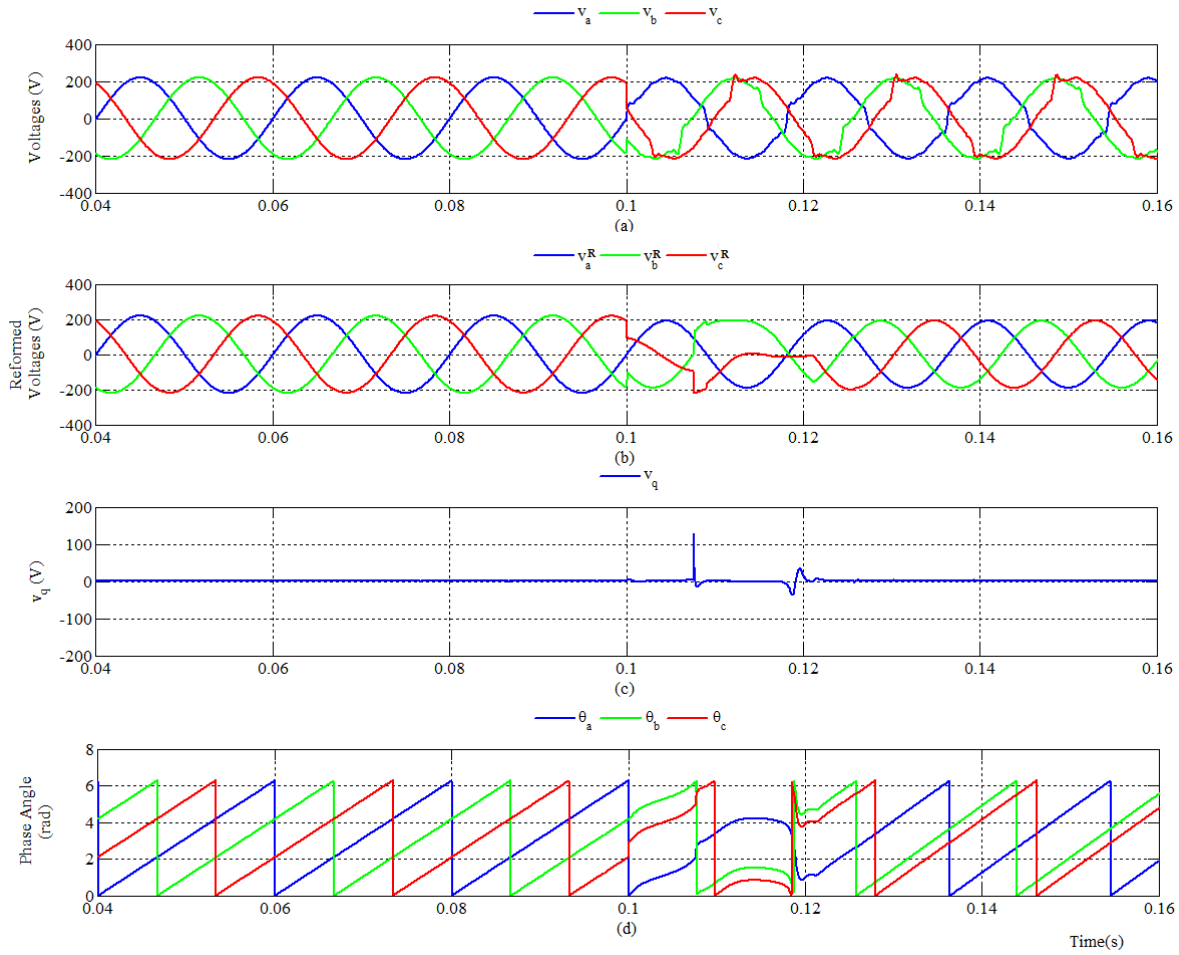

Figure 4.30: Performance of the developed PLL under balanced amplitudes of the phases but with unequal phase-angle differences at 55 Hz accompanied by harmonic distortion. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

4.3.11: Case-B11: Simultaneous Amplitude Imbalance and Phase-Shift of All the Phases Accompanied by Harmonic Distortion at Frequency Other than Nominal Value

The PLL is tested with the conditions described in case-B7 except the frequency is not 50 Hz. Instead, the frequency is changed to 45 Hz (Fig. 4.31) and 55 Hz (Fig. 4.32) and the performance of the system is observed. It has been found that, the developed PLL can work perfectly with a response time of 0.0304 second and 0.0322 second, respectively. For the second case, the feed-back loop assisted the frequency estimation. Although, the PLL has been tested for 5 Hz frequency swing, the permissible frequency swing in three-phase grid is much less than the test case.

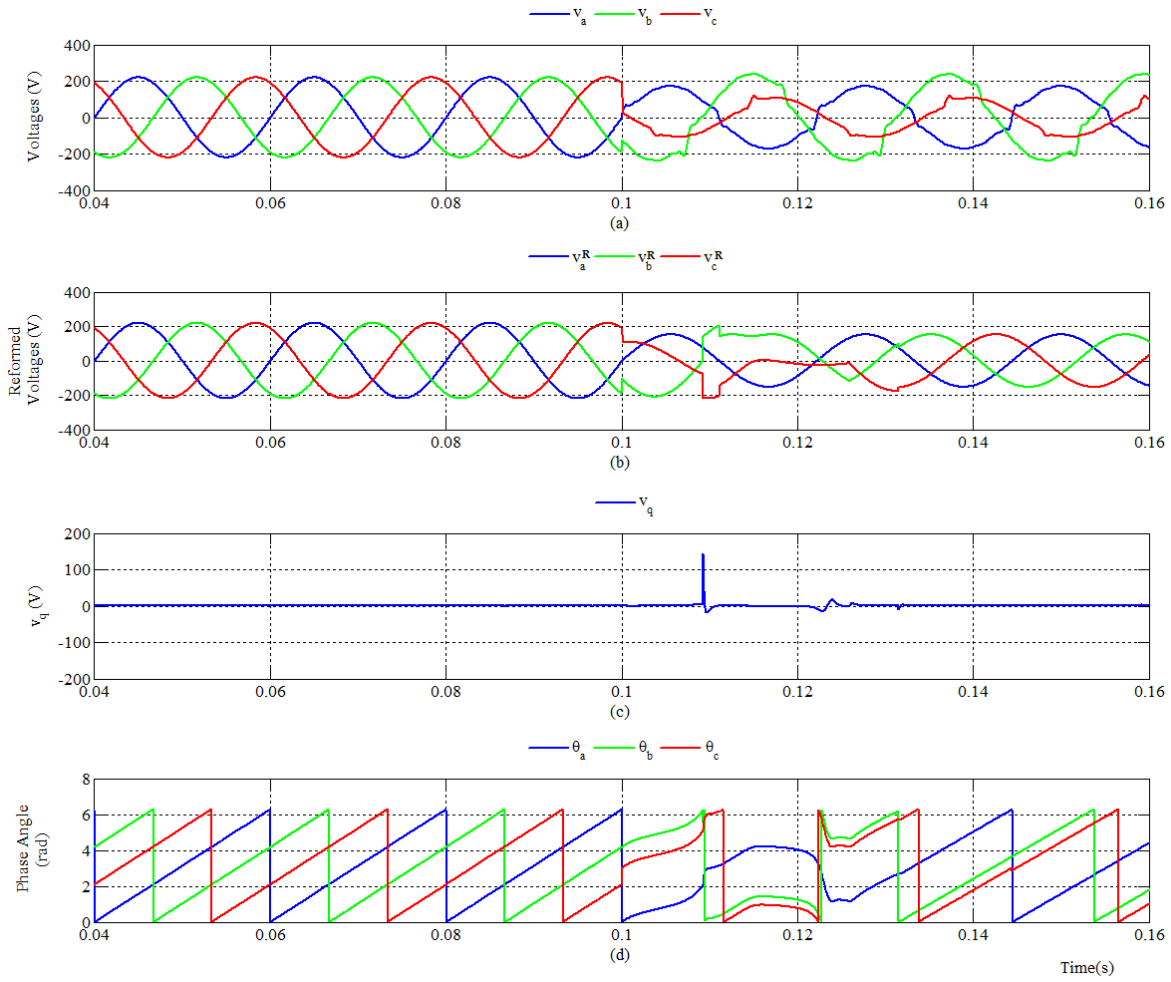

Figure 4.31: Performance of the developed PLL under unbalanced and distorted condition at lower than nominal frequency. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

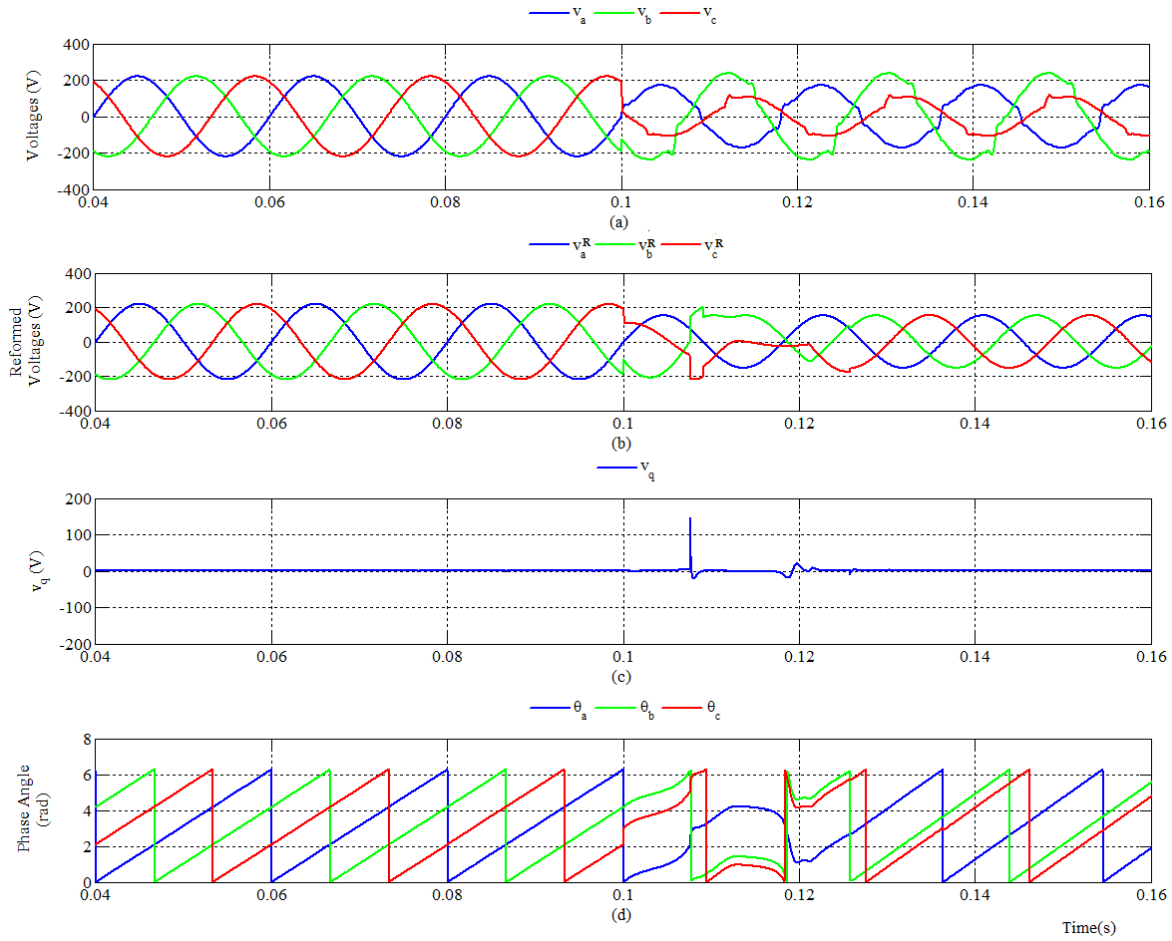

Figure 4.32: Performance of the developed PLL under unbalanced and distorted condition at higher than nominal frequency. (a) three-phase voltage waveforms; (b) three-phase voltage waveforms after reformation; (c) v_q versus time; (d) estimated phase angles of v_a, v_b and v_c.

This chapter concludes by summarizing the objective, methodology and achievements of this thesis in section 5.1. It also points out the key features of this research work in the same section. Section 5.2 suggests some directions for future research.

5.1 Summary

A signal reforming algorithm based three-phase PLL has been developed in this thesis work. The purpose of this work is to develop a new algorithm that can quickly and accurately estimate the phase-angles of the three-phase grid voltage under unbalanced and distorted grid conditions. The concept of phase-locked loop and some conventional single-phase and three-phase PLLs have been discussed. The performance of a conventional SRF-PLL under unbalanced and distorted conditions has been observed and the causes of its poor performance under such circumstances have been identified. The new method has been developed based on the drawbacks of the conventional PLLs. The algorithm has been verified in MATLAB/Simulink by observing its performance under several adverse conditions.

The developed PLL can endure the amplitude and phase-angle imbalances and can accurately estimate phase angles of the phases. It can also attenuate the harmonic components from the input grid voltage with its developed algorithm instead of using any conventional filter. The developed technique can successfully reform harmonics free balanced three-phase voltage system from a completely unbalanced and harmonics affected one. It also avoids the use of three single-phase PLLs to estimate the phase angles of a three-phase voltage system under both amplitude and phase angle unbalanced conditions and thus reduces the computational complexity. The developed algorithm is also efficient at off-nominal frequency. The response time of the proposed technique is found to be less than 2.0 fundamental cycles. Thus, the developed PLL can solve the phase-angle and frequency estimation problems during adverse conditions in the three-phase grid system.

5.2 Future Work

The research work and its outcome to develop the PLL algorithm in this thesis can be implemented in any DSP processor or FPGA board. Any research work requiring the information on phase-angle can adopt and utilize this algorithm without adding much complexity. The real-time estimated phase-angle and other information can also be utilized in numerous grid-connected devices and utilities as mentioned in Chapter 1. The control mechanism of these grid-connected devices and utilities can also be upgraded by adding this algorithm to their control logic.

The algorithm reported in this research work has some limitations. One notable limitation is that that it is only able to determine the phase-angle deviations of the phases within -30 to 90 degree; the range should be extended more. This happens due to having one value for two different phase-angle deviations. One way to solve this is by developing an algorithm to divide the boundary into several segments and cross-check for accurate value. Another way is to change the reference phase from *a* to *b* to *c*, and obtain the solution for each case. The final solution can be obtained by comparing and cross-checking the values. Both the operation requires a simple algorithm to perform the task.

Also, the harmonic attenuation algorithm is only developed for harmonics upto 25^{th} order. A generalized algorithm with selective nature can make this research-work much more dynamic.

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A.1: Block Diagram of the Whole System for Simulation

The whole set-up for the simulation and result analysis consists of a programmable three-phase voltage source, a three-phase filter block, a signal reforming block, an SRF-PLL block combining the rotational transformation block and PLL block, and a phase-angle estimation block to estimate the phase angles of all the phases.

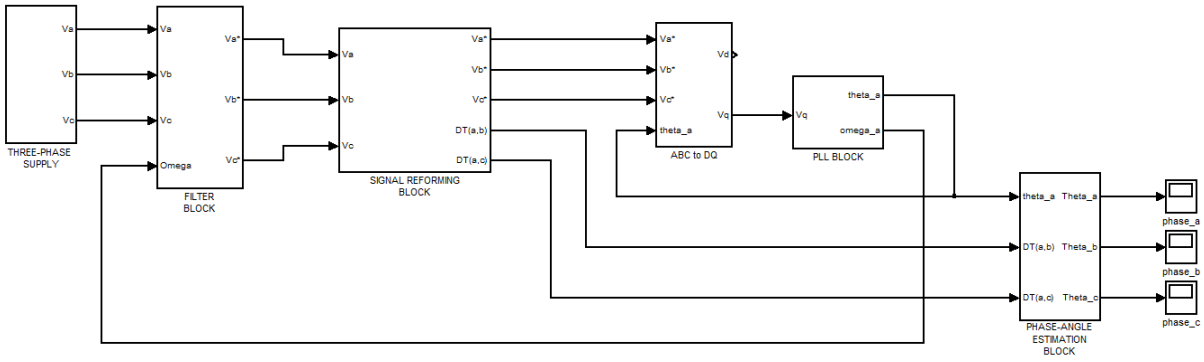

Figure A.1: Block diagram of the whole system for simulation.

A.2: Block Diagram of the PLL Block

The PLL block of Fig. A.1 is expanded as in Fig. A.2.

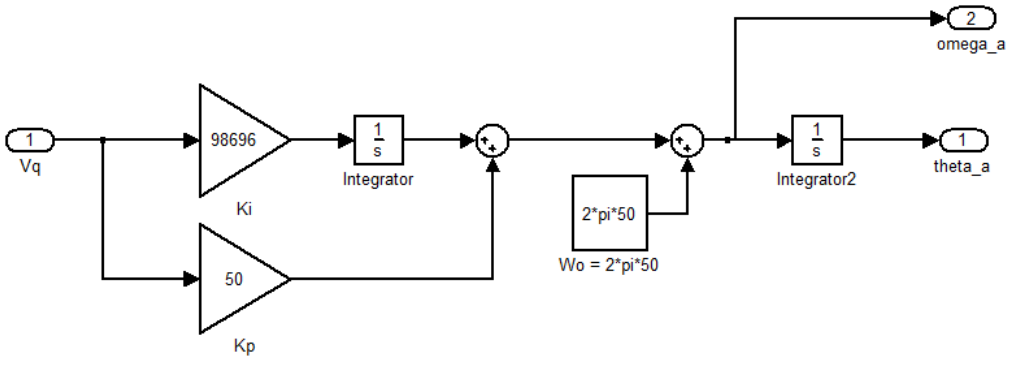

Figure A.2: Expanded block diagram of the PLL block.

A.3: Block Diagram of the Filter Block

Fig A.3 shows the block diagram of the filter structure. The filter block for each phase is developed by sequentially cascading 24 sets of unit filter blocks. The block diagram of the unit filter is shown in Fig. A.4.

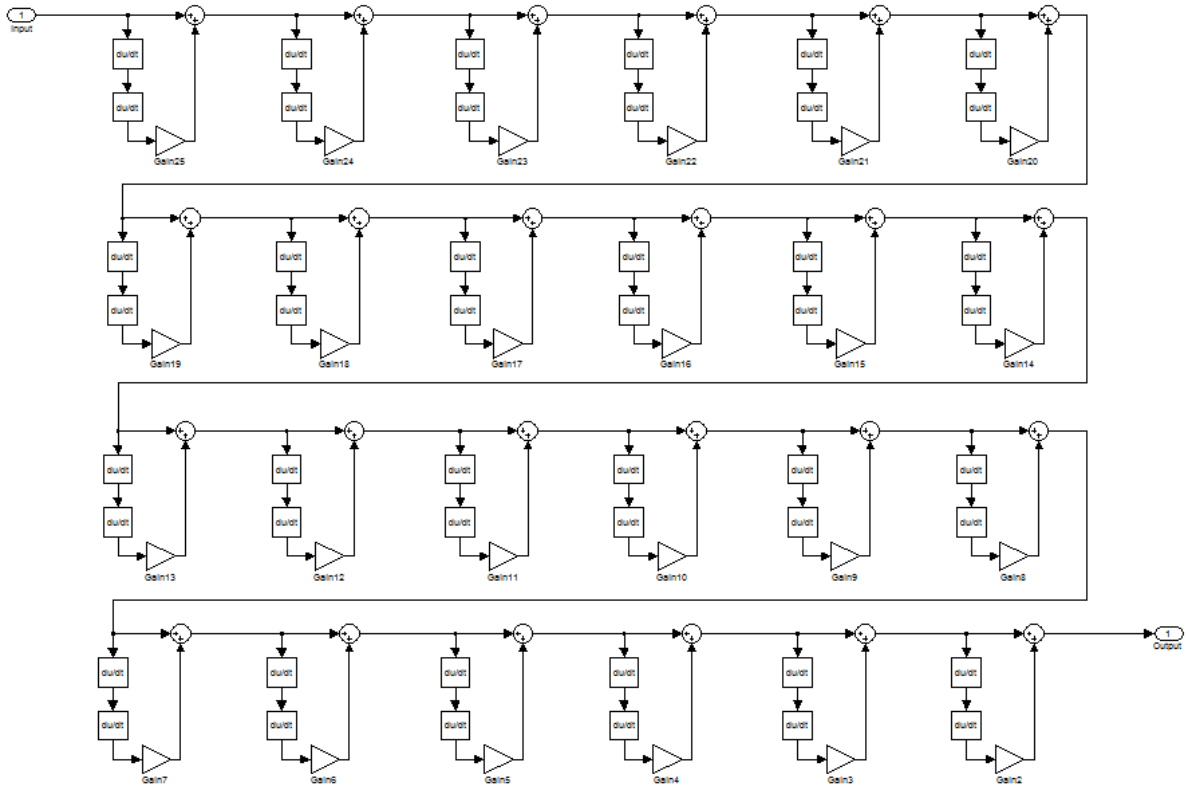

Figure A.3: Block diagram of the developed filter.

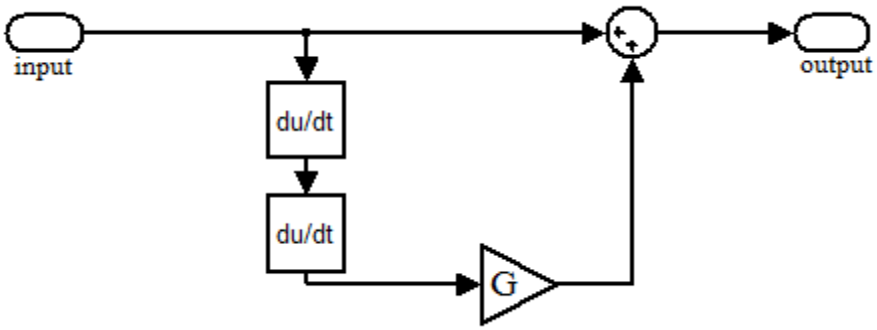

Figure A.4: Block diagram of a unit filter block.

B.1: MATLAB Code for Three-Phase Grid Voltage

```
function [Va, Vb, Vc]  = fcn(t) % This code generated the input signal
A= 220; % Line to Neutral Voltage
a= 1.0; % Voltage Sag/Swell of Phase A:  Here, 'a' can be any positive value
b= 1.0; % Voltage Sag/Swell of Phase B:  Here, 'b' can be any positive value
c= 1.0; % Voltage Sag/Swell of Phase C:  Here, 'c' can be any positive value
f= 0; % frequency swing: Other values used are f = +5 and f = -5
P1 = 0*(pi/180); % for Vb, sin(wt-120-theta): Where -30 <= P1 <= 90 degree
P2 = 0*(pi/180); % for Vc, sin(wt+120+theta) : Where -30 <= P2 <= 90 degree
P =  0*(pi/180); % Equal Phase Jump of All the Phases
Vap = zeros(1,25); % Variable Initialization
Vbp = zeros(1,25); % Variable Initialization
Vcp = zeros(1,25); % Variable Initialization
K = [       %IEEE 519-2014 Std. Harmonics
    1.0000 % Fundamental
    0.0100 % Harmonics
    0.0400
    0.0100
    0.0400
    0.0100
    0.0400
    0.0100
    0.0400
    0.0100
    0.0200
    0.0050
    0.0200
```

```
    0.0050
    0.0200
    0.0050
    0.0150
    0.00375
    0.0150
    0.00375
    0.0150
    0.00375
    0.0060
    0.0015
    0.006
];
k = K';
T = 0.1;   % Instance of Disturbance/Imbalance 0<T<0.2
if t< T
Va = A*sin(2*pi*50*t);
Vb = A*sin(2*pi*50*t-2*pi/3);
Vc = A*sin(2*pi*50*t+2*pi/3);
else
for i = 1:25 % Adding Disturbance
    Vap(i) = A*a*sin(2*pi*(50+f)*t*i+P-2*pi*i*f*T);
    Vbp(i) = A*b*sin(2*pi*(50+f)*t*i-2*pi*i/3-P1+P-2*pi*f*T*i);
    Vcp(i) = A*c*sin(2*pi*(50+f)*t*i+2*pi*i/3+P2+P-2*pi*f*T*i);
end
Va = Vap*k';
Vb = Vbp*k';
Vc = Vcp*k';
end
end
```

B.2: MATLAB Code for Signal Reforming Block

```
function [VA,VB,VC,DT1,DT2]  = fcn( Va, Vb, Vc) % Reforms the Signal
%%%%%%%%%%%%[Initialize Memory Unit ]%%%%%%%%%%%%%%
persistent Va0;
persistent Vb0;
persistent Vc0;
persistent Vb_ref;
persistent Va_max;
persistent Vb_max;
persistent Vc_max;
persistent Va0_max;
persistent Vb0_max;
persistent Vc0_max;
persistent maxaF;
persistent maxbF;
persistent maxcF;
persistent dT1;
persistent dT2;
persistent Vb_1;
persistent Vb_2;
persistent Vb_cross_flag;
persistent Vb_prev_1;
persistent Vb_prev_2;
%%%%%%%%%%%[Set Initial Values]%%%%%%%%%%%%%%
if isempty(Va0)
    Va0 = 0;
    Vb0 = 0;
    Vc0 = 0;
    Vb_ref = 0;
    Va0_max = 1;
```

```
    Vb0_max = 1;
    Vc0_max = 1;
    Va_max = 1;
    Vb_max = 1;
    Vc_max = 1;
    maxaF = 0;
    maxbF = 0;
    maxcF = 0;
    dT1 = 0;
    dT2 = 0;
    Vb_1 = 5;
    Vb_2 = 5;
    Vb_prev_1 = 0;
    Vb_prev_2 = 0;
    Vb_cross_flag = 0;
end
%%%%[ Finding DTEHTA2 and Va max ]%%%%%%%%
if (Va0 < 0 && Va >= 0)
    maxaF = 1;
    for dt = 0:pi/500:pi/2
        if ((Vc/Vc0_max)- sqrt(3)*cos(dt)/2 + sin(dt)/2< 0.001)
            dT2 = dt;
        end
    end
end

if ((Va >= Va_max) && maxaF ==1)
    Va_max = Va;
end
```

```
if (Va0 > 0 && Va <= 0)
    maxaF = 0;
    Va0_max = Va_max;
    Va_max = 1;
end
%%%%%%[ Finding DTEHTA1 and Vb max ]%%%%%
if (Vb0 < 0 && Vb >= 0)
    maxbF = 1;
    for dt = 0:pi/500:pi/2
        if ((Va/Va0_max)- sqrt(3)*cos(dt)/2 + sin(dt)/2< 0.001)
            dT1 = dt;
        end
    end
end
if ((Vb >= Vb_max) && maxbF ==1)
    Vb_max = Vb;
end
if (Vb0 > 0 && Vb <= 0)
    maxbF = 0;
    Vb0_max = Vb_max;
    Vb_max = 1;
end
%%%%%%%%%[ Finding Vc max ]%%%%%%%%%
if (Vc0 < 0 && Vc >= 0)
    maxcF = 1;
end

if ((Vc >= Vc_max) && maxcF ==1)
    Vc_max = Vc;
end
```

```
if (Vc0 > 0 && Vc <= 0)
    maxcF = 0;
    Vc0_max = Vc_max;
    Vc_max = 1;
end
%%%%%%%%[AMPLITUDE & PHASE REFORM]%%%%%%%%%%
Vb_ref = Vb/Vb0_max;
if (abs(Vb_ref) > 1)
    Vb_ref = 1;
end
Vb_1 = Vb_ref*cos(dT1) + sin(dT1)*sqrt(1-Vb_ref^2);

if ( Vb_prev_1 < -0.2 && Vb_1 >=0)
    Vb_1 = Vb_prev_1;
end
Vb_2 = Vb_ref*cos(dT1) - sin(dT1)*sqrt(1-Vb_ref^2);
if ( Vb_prev_2 < -0.2 && Vb_2 >=0)
    Vb_2 = Vb_prev_2;
end
if (abs(Vb_1 - Vb_2)< 0.02 && Vb_1 > 0 && Vb_2 > 0 )
    Vb_cross_flag = 1;
end

if (abs(Vb_1 - Vb_2)< 0.02 && Vb_1 < 0 && Vb_2 < 0 )
    Vb_cross_flag = 0;
end

Vb_prev_1 = Vb_1;
Vb_prev_2 = Vb_2;
```

```
VA = Va;

if (Vb_cross_flag == 1)
    VB = Vb_2*Va0_max;
else VB = Vb_1*Va0_max;
end

VC = -VA - VB;

DT1 = dT1;
DT2 = dT2;

%%%%%%%%%[Update Values]%%%%%%%%%%%%%

Va0 = Va;
Vb0 = Vb;
Vc0 = Vc;
Vb_1 = 5;
Vb_2 = 5;
```

B.3: MATLAB Code for *abc* to *dq* Transformation

```
function [Vd, Vq]  = fcn(Va, Vb, Vc, theta)
%%%%%%%%%% Vabc to Vdq %%%%%%%%%%%%%%%%%%%%%
T = 2/3*[cos(theta) cos(theta-(2*pi)/3) cos(theta+(2*pi)/3); -sin(theta) -sin(theta-(2*pi)/3) -
sin(theta+(2*pi)/3); 0.5 0.5 0.5 ];
A = T*[Va Vb Vc]';
Vd = A(2,:);
Vq = A(1,:);
```