A COMPACT ANALYTICAL MODEL FOR MONOLAYER TRANSITION METAL DICHALCOGENIDE CHANNEL FIELD EFFECT TRANSISTORS

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by

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Declaration

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Dedication

to my mother

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Abstract

In recent years, researchers have been very excited about the prospects of 2-D transition metal dichalcogenides (TMD) as a suitable semiconducting material for the channel in transistor devices. In order to evaluate their suitability in next generation transistors, it is important to understand their device level performance. A rigorous analytical model can play a significant role in this regard. In this work we have developed an analytical compact model for monolayer 2-D TMD channel MOSFETs that can replicate device performance in all regions of operation. In order to better understand the effects of monolayer TMD, we have developed two models, one for the subthreshold region and the other for the inversion region. The subthreshold model is centered around the scale length of the device. At first, an analytical expression for the scale length was derived from the eigenvalue equation. It was important to make sure that the derived expression of scale length precisely incorporates all the device and physical parameters. Gauss's law was applied in an infinitely small enclosure in the 2D channel which established a second order differential equation that governs the operation in 2D TMD FET. Channel potential and 2D carrier density was derived from the solution of this equation. Finally, the channel potential was used in the drift-diffusion equation to obtain an all-region closed-form solution for the drain current. Non-idealities were incorporated in this model by modifying intrinsic device parameters. We verified the applicability of our model by comparing our results with that of established numerical simulators and experimental reports. Our model properly replicated device performance for both long and short channel devices. Appropriate results were produced using this model for channel length as low as 10 nm.

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Chapter 1

Introduction

1.1 Current Trends of Nanoelectronics

One of the biggest breakthroughs of the 20th century was the invention of transistors. Transistors are the building block of today's microprocessors and computers and they have paved the way for the electronic revolution of this era. Since the invention in 1947, considerable efforts have been made to miniaturize the size of metal oxide semiconductor field effect transistors (MOSFETs). This allowed us to integrate billions of MOSFETs in a single chip with an area of 1 square centimeter. The motivation for this aggressive scaling comes from the famous prediction of Intel's cofounder Gordon Moore who said that the number of transistors per integrated chip (IC) will double every two years [1]. This famous prediction, popularly known as the 'Moore's Law' has remained the guideline for scientists and engineers in IC industry. From one technology node to the other, MOSFETs are conceived to be smaller, faster and less power consuming.

As shown in Figure 1.1, the number of MOSFETs has grown steadily so far, in compliance with the Moore's law. Thirty years of aggressive scaling have pushed the device dimensions close to the atomic range. The downscaling of MOSFETs has slowed down since the 65 nm node was reached. Issues related to the nanoscale dimensions of the devices started to arise. With smaller technology nodes, gate length and oxide thickness both shrunk heavily. This led to various short-channel effects (SCE) and gate leakage current [2].

The SCEs for the MOSFETs are important when the channel length becomes comparable to the width of the depletion region. When the gate length is scaled down, the gate starts to lose the electrostatic control over the channel, on the other hand the source-drain bias (VDS) gains a larger influence on the barrier. Such an effect is named drain-induced barrier lowering (DIBL). This loss of electrostatic integrity leads to a continuous increase of the current and decrease of the off-state potential. Moreover, the electron mobility is reduced due to collisions with the semiconductor/oxide interface. This surface scattering effect is enhanced by the increase of electric field in the confined regions, which pushes the

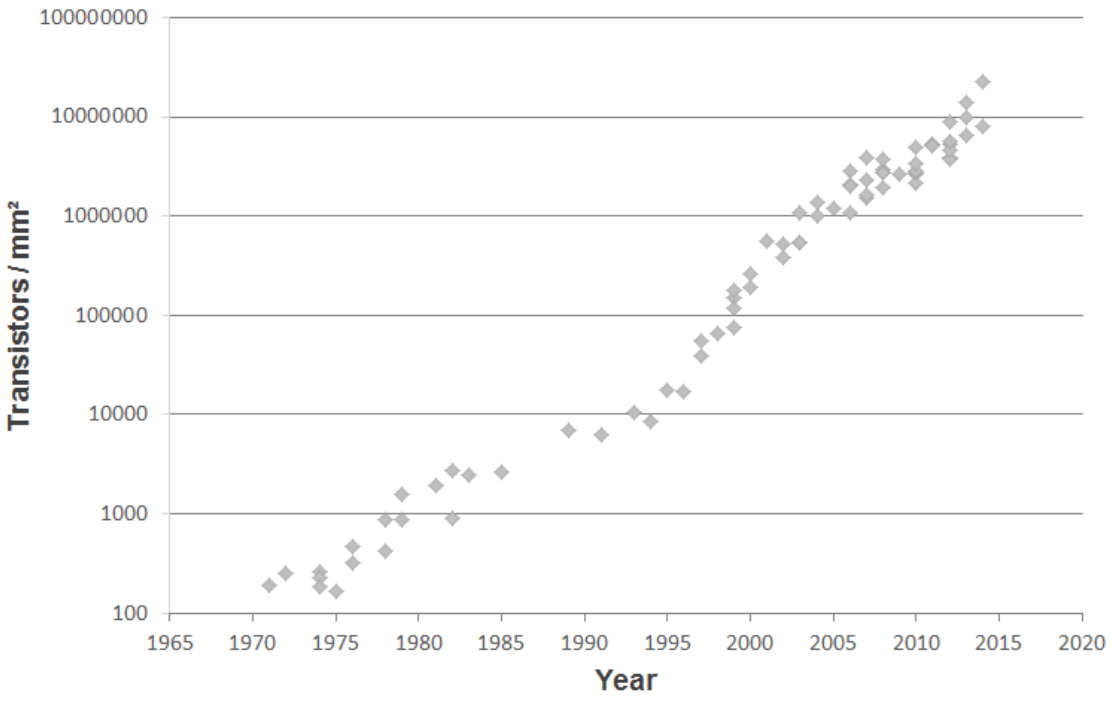

Figure 1.1: Density of transistors in Intel's IC

electrons toward the surface of the device. The reduction of electron mobility is also caused by the necessity of using high doping levels in such scaled MOSFET. Finally, the average velocity of carriers no longer linearly depends on the electric field in such small devices, which is called the velocity saturation effect.

Another factor that limits the scaling options in modern MOSFETs is the subthreshold current. Since operating voltage has been pulled down to a much small value in modern-day devices, the threshold voltage is barely higher than the off-state voltage. Thus a considerable amount of current flows through the channel during off state and the ratio of off- and on current is not high enough. The severity of this problem is quantized using the expression called Subthreshold Swing (SS) which indicates the reduction in voltage required to reduce the drain current by a factor of ten below the threshold value. Traditional MOSFETs cannot have SS below 60 mv/dec. All these inherent limitations have motivated the scientific community to investigate novel transistor structures with better gate control.

The electronics industry has resorted to strained Si-Ge channel with tri-gate structure to reduce the adverse short channel and nonideal effects. Also high-k gate oxides have been used to reduce tunneling while maintaining the desired level of capacitance. Intel's latest 'Coffe Lake' processors use 14 nm tri-gate Silicon transistors. Beyond 14nm, as we move

to 10 and 7nm, a new fin material will be required; probably Si-Ge, or perhaps just pure germanium. SiGe and Ge have higher electron mobility than Si, allowing for lower voltages, and thus reducing power consumption, tunneling, and leakage. SiGe has been used in commercial CMOS fabrication since the late ’80s, too, so switching from silicon will not be a massive shift. The primary reason that semiconductor industry has solely relied on Silicon for so long is that the entire industry is based on silicon. The amount of time, money, and R&D that would be required to deploy new machines for handling new materials that we know relatively little about would be astronomical.

The next era of processors will require less power consuming transistors with lower dimension. But it has already been established that Si cannot reach this desired level. Hence, scientists are looking for new materials that can replace Si in near future. Several potential candidates have surfaced in the past few decades- III-V compound semiconductors, Graphene, chalcogenides etc. In order to understand their true potential, we need to explore the application of these materials in conventional transistor structures.

1.2 Two Dimensional Semiconductors

Layered two dimensional (2-D) semiconductor materials have garnered significant attention in recent years. In the past 2-D materials were considered to be unstable. Reports suggested that 2-D materials would disintegrate in room temperature under thermal fluctuations. However, in 2004 Geim and Novoselov successfully isolated graphene by mechanical exfoliation technique and since then Graphene has been at the center of research thrust due to its amazing electronic, mechanical and optical properties [3][4].

While Graphene has been at the center of this research thrust due to its amazing electronic, mechanical and optical properties, an absence of bandgap in Graphene led to the extensive investigation of other layered 2-D semiconductors. Specially, the out-of-ordinary electronic properties of Graphene inspired the research community to concentrate on 2-D material based nanoelectronics. Since then, we have seen an exponential increase in the research activity in graphene and other 2DMs (such as the transition metal dichalcogenides [5][6], h-BN, black phosphorus [7], silicene and gemanene).

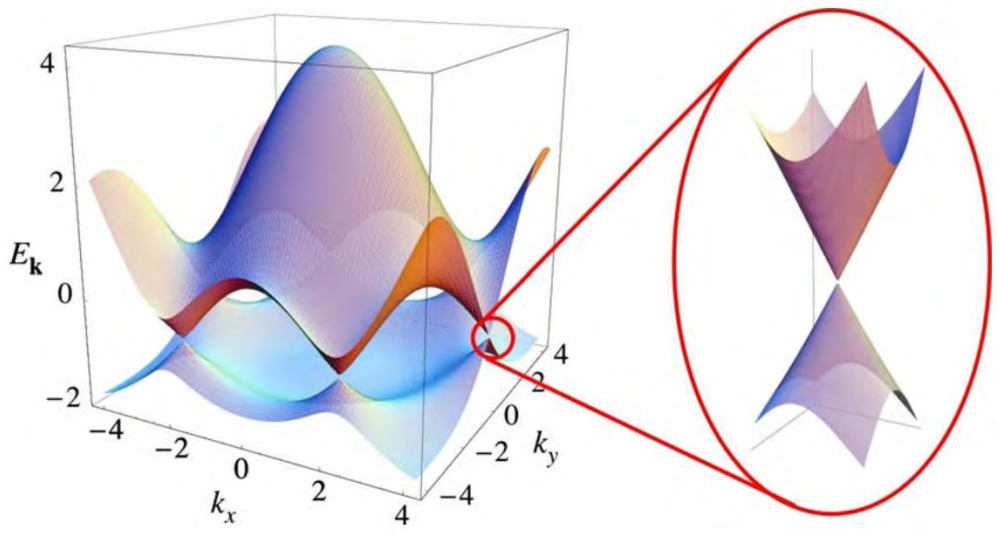

Figure 1.2: Electronic dispersion in the Graphene lattice. Left: energy spectrum. Right: zoom in of the energy bands close to one of the dirac points. Figure adapted from [8].

One of the most interesting aspects of the graphene is its low-energy band structure, which is linear around the K and K' points of the Brillouin zone, as shown in Figure 1.2. The Fermi energy exactly crosses the Dirac points which in turn causes the unconventional properties of Graphene with respect to 2-D electron gases (2DEG). Another interesting property of graphene is when laterally confined into nanoribbons, its electronic and transport properties are strongly affected by the geometry of the edges (armchair, zigzag or mixed) and the nature of their passivation [7][9]. For example, under certain conditions the ribbon can show a band gap, whose size is proportional to the inverse of the ribbon width. Such a gap might be important for applications in logic devices, which are however compromised by the huge mobility degradation due to the increase of the effective mass from one side, and the presence of edge roughness from the other [10]. Till date the biggest hindrance towards a successful adaptation of Graphene in transistor application has been its lack of band gap. The very low on-off current ratio thus makes its use impractical in logic devices.

After exploring Graphene for nearly a decade, concentration was shifted towards other 2D material families. One of the very promising 2-D material family is the transition metal dichalcogenides (TMDs) [11]. TMD materials such as molybdenum disulphide (MoS2) and tungsten diselenide (WSe2) have been proven to be viable alternative in the post-Silicon era due to having desirable bandgap, flexibility, transparency, and surface free of dangling

bonds [12]. Especially, monolayer 2-D TMDs have excellent prospect as channel material in nanoscale field-effect transistors (FETs).

1.2.1 Monolayer Transition Metal Dichalcogenides (TMDs)

Layered 2-D crystals, such as monolayers of transition metal dichalcogenides (TMDs) MX2 (e.g., M = Mo, W; X = S, Se, Te) and other metal chalcogenides MXx (e.g., M = Ga, Sn; X = O, S, Se) offer a native thickness of about 0.6 nm with a variety of bandgaps and band-alignments [11][12]. Furthermore, 2D crystals possess a sharp turn on of density of states at the band edges and have no surface dangling bonds; thus potentially enabling a low interfacial density of state, which are highly desired for achieving a sharp SS. Recent experimental results show that the band alignment in stacked monolayer 2D crystal heterostructures can be tuned by an external electric field perpendicular to the heterojunction. These properties uphold their candidacy for not only transistors and other logic devices, but also for the display devices [13] and various types of nano-sensors [14].

As shown in Figure 1.3, the TMDs have layered structures similar to graphite: covalently bonded 2-D X-M-X layers loosely coupled by weak van der Waals forces [15], [16]. Variation in the stacking sequence leads to five different polymorphs or phases [17], [18]. Among them, 1T and 2H are usually the most stable states. In the 1T phase, metal atoms are coordinated with six neighboring chalcogens, whereas the coordination in 2H is trigonal prismatic In general, the TMDs formed from metals of the groups IVB and VIB show semi-conducting properties, hence they are suitable materials for digital transistor applications.

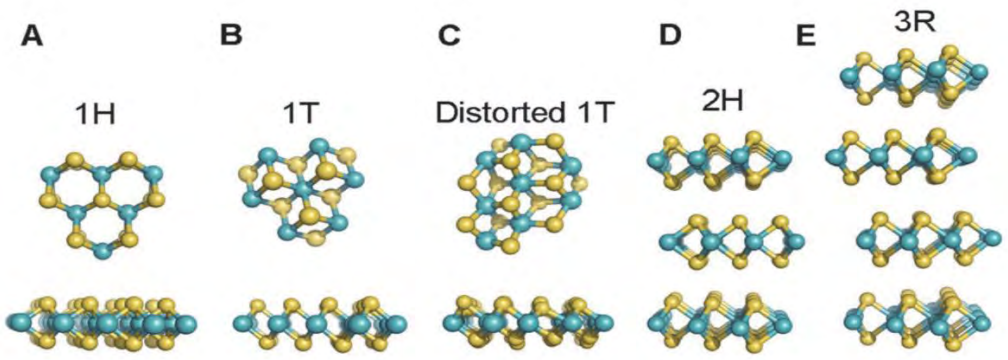

Figure 1.3: Different polymorphs or phases of single layer and stacked single layer TMDs. (A) 1H phase, (B) ideal (a×a) 1T phase, (C) distorted (2a×a) 1T phase, (D) 2H phase and (E) 3R phase. Figure adapted from [17].

1.2.2 Electronic Properties of 2-D TMDs

MoS2 is a typical and well-studied TMD material. Its layers consist of hexagons with the Mo and S2 atoms located at alternating corners as shown in Figure 1.3 [15], [19]. The most striking feature of bulk MoS_2 is that, compared to zero-bandgap graphene and insulating *h*-BN, it is a semiconductor with an indirect band gap of 1.29 eV [20]. Several studies have confirmed a transition from an indirect band gap to a direct band gap for MoS_2 as the thickness of bulk MoS_2 is decreased to that of a monolayer [21]. Similar transition is also demonstrated for other TMD materials[22]–[25].

Kuc et al. performed an extended study of the influence of quantum confinement on the electronic structures of monolayer and few-layer MS_2 (M = W, Nb, Re) using first-principles calculations [26]. They found that WS_2, which is similar to MoS_2, exhibits an indirect (bulk, E_g=1.3 eV) to direct (monolayer, E_g=2.1 eV) bandgap transition. Figure 1.4 exhibits the band alignment of various monolayer semiconducting TMDs.

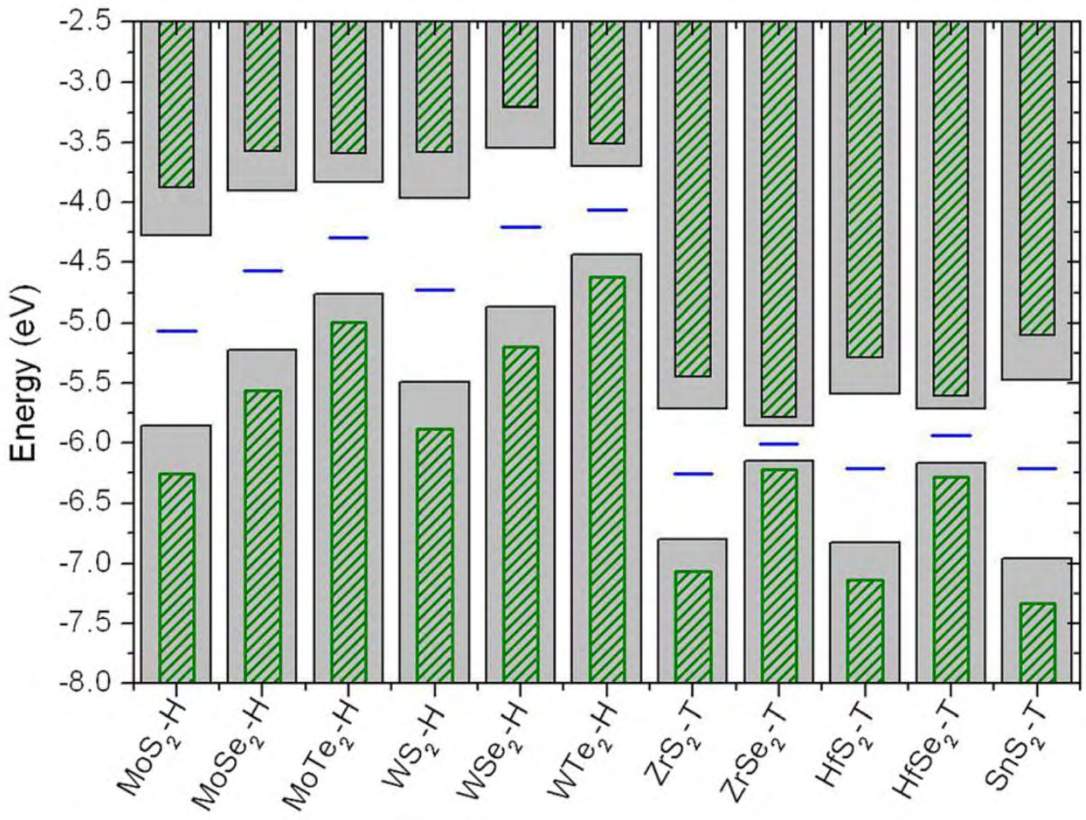

Figure 1.4: Band alignment of monolayer semiconducting TMDs. The Fermi level is indicated by the blue horizontal line and the vacuum is at 0V.

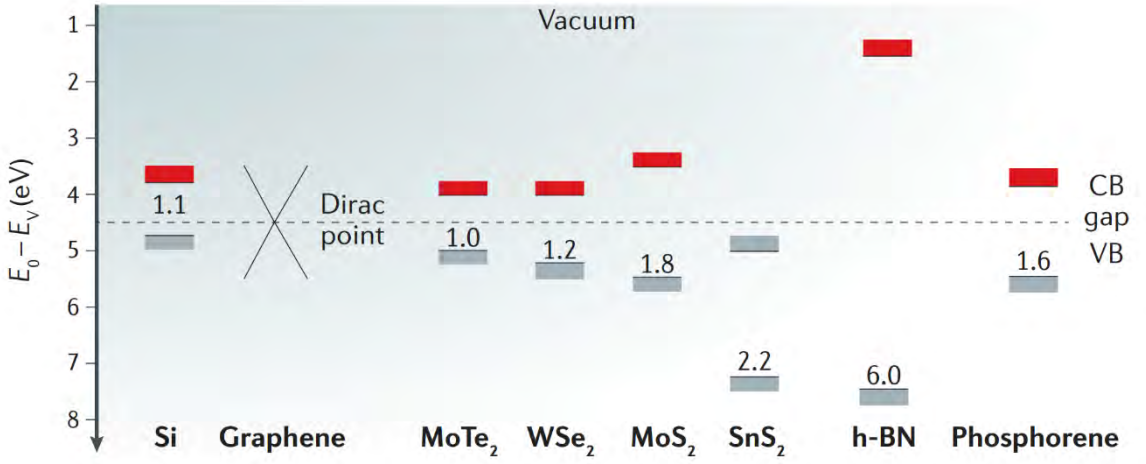

Figure 1.5: Bandgap of Graphene and various 2-D TMD materials with respect to Si. Figure adapted from [25].

Figure 1.5 demonstrates the bandgap of 2-D TMD materials and their position compared to Si. It is evident that these materials have bandgap akin to semiconductors. And most importantly their bandgap is tunable, as it can be controlled by changing the number of layers in the TMD material. Number of layers not only tunes bandgap, but also controls other physical properties. For example, electrical characterizations of single-layer MoS_2 have shown n-type conductivity with a room temperature mobility in the range of 10-50 $cm^2/(V\text{-}s)$ [27], [28]. Compared to the mobility 200-500 $cm^2/(V\text{-}s)$ of bulk MoS_2 sheets is rather low and comparable to that of graphene nanoribbons but still much lower than that of either pristine graphene or Si transistors [29]. Because of the low mobility, MoS2 transistors are probably more suited for low power applications rather than high performance usage [30].

1.3 Compact Models of 2-D TMD Channel MOSFETs

Large-scale production of complex circuits based on these devices requires efficient circuit simulation followed by layout design using EDA tools before realization. To perform efficient circuit simulation, a compact model is an essential requirement. The effect of the density of state (DOS) on capacitance and consideration of Fermi–Dirac (FD) statistics in place of Boltzmann statistics differentiate the modeling of these devices compared with the conventional Si channel MOSFET [31]. Several compact models have so far been proposed to replicate the circuit level performance of TMD channel FETs [32]–[36]. The capacitive

model proposed in [33] is based on drift-diffusion model and does not include non-idealities. In [36], an analytical I-V model is derived by simplifying surface potential. Results of this model deviates from that of numerical simulation for sub-30nm channel length. The short channel model proposed by Taur et al. utilizes the concept of scale length to calculate current in the subthreshold region [35]. However, the proposed linear relation between scale length and oxide thickness fails to incorporate important device parameters such as channel thickness and permittivity of oxide as well as channel material. Several compact subthreshold models have been proposed by redefining scale length in terms of abovementioned device and physical parameters [32], [34]. But eventually they also depend on numerical integration in order to calculate device current [37], [38].

1.4 Thesis Objectives

The primary objective of this work can be divided in following two parts.

- First, to develop a compact analytical I-V model for 2D TMD channel FETs including non-ideal conditions.
- Second, to formulate a comprehensive performance analysis of different 2D TMD semiconductors as channel material in FET architecture.

1.5 Thesis Overview

The entire thesis is divided in five chapters. A brief organization of each chapter is presented below.

The first chapter discusses the current technological status of transistors and briefly sheds lights on the scaling issues and need for futuristic innovations in every aspect of semiconductor devices to uphold the technological progression professed by Moore's law. It also introduces the context of the innovation behind monolayer Transition Metal Dichalcogenide (TMDC) channel MOSFETs.

The second chapter discusses the formulation of the subthreshold model for 2-D TMD channel MOSFET. At first a cubic equation is formed incorporating all physical and device parameters. The solution of this equation gives us the scale length. In the next part of this chapter we present a new analytical equation to calculate drain current at subthreshold region for both double-gate (DG) and semiconductor-on-insulator (SOI) TMD channel devices.

The third chapter introduces an all-region compact drain current model for our device. This chapter rigorously studies the mathematical formulation of the device's system and these system equations are used to develop the analytical model. Non-ideal phenomena are included later in the drain current equation.

Our model is verified with established numerical models and experimental results in the fourth chapter. The model demonstrates excellent agreement with reported results for both long and short channel devices.

In the final and fifth chapter conclusion is drawn and possible developments are discussed.

Chapter 2

Subthreshold Model

The subthreshold model for 2-D TMD channel FET is obtained by modifying the drain current equation in this region of operation. At first a cubic equation is formed incorporating all physical and device parameters. The solution of this equation gives us the scale length. In the next part we present a new analytical equation to calculate drain current at subthreshold region for both double-gate (DG) and semiconductor-on-insulator (SOI) TMD channel devices

2.1 2-D Channel Potential

The schematic model of a 2-D single layer TMD channel MOSFET is presented in Figure 2.1. The heavily doped Si substrate of the top-gated SOI structure can be replaced by a back electrode to obtain a double gate (DG) FET device. Since mobile charge density is negligible in the subthreshold region, the 2-D potential can be solved analytically [39]. The zero potential reference is fixed at the edge of source conduction band. The 2-D potential corresponding to the conduction band is,

$$\varphi(x,z) = V_{gs} + \chi - \varphi_m + \sum_{n=1}^{\infty} \frac{b_n \sinh\left[\frac{\pi(L-x)}{\lambda_n}\right] + c_n \sinh[\frac{\pi x}{\lambda_n}]}{\sinh[\frac{\pi L}{\lambda_n}]} \cosh[\frac{\pi z}{\lambda_n}] \qquad (2.1)$$

Here x is the channel direction and z is perpendicular to the film. V_{gs} is the gate voltage, χ is the electron affinity of semiconductor material and φ_m is gate work function. The channel potential $\varphi(x,z)$ is assumed to have no variation in the z direction due to the atomic scale thickness of channel material. The summation in the right-hand-side of Equation (2.1) consists of a series of eigen functions with discrete eigenvalues λ, which satisfy the following equation for odd values of n [40].

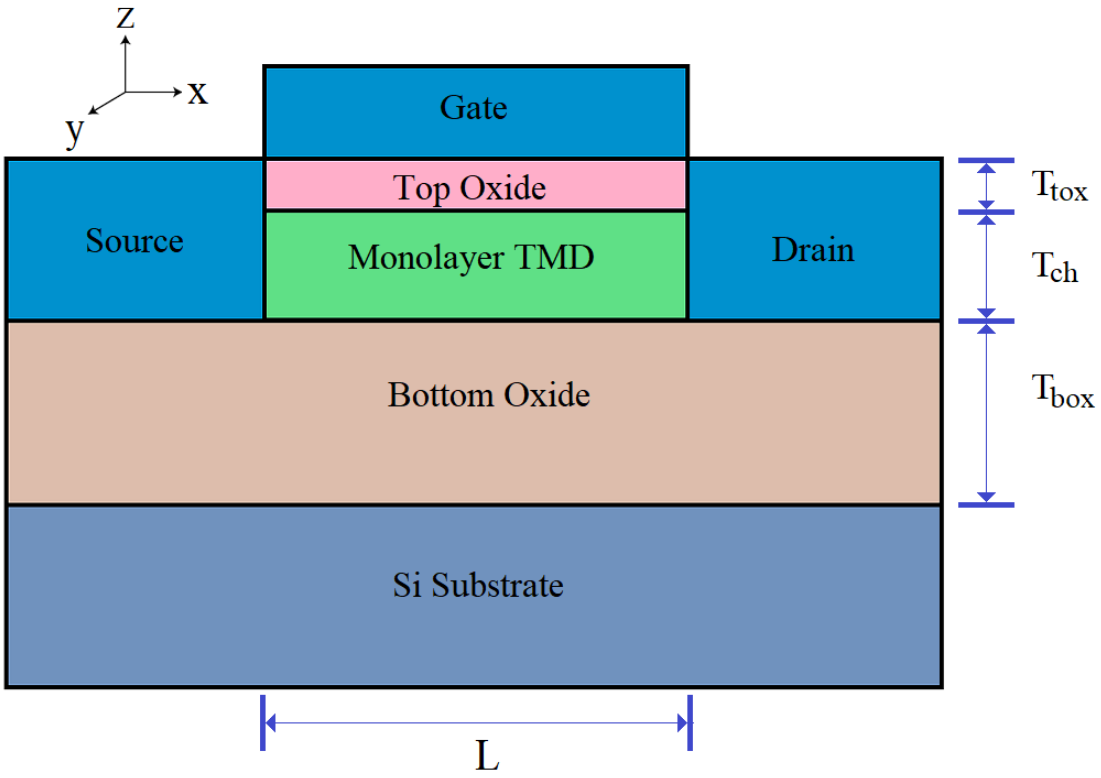

Figure 2.1: Schematic of a 2-D TMD channel MOSFET. T_{tox} and T_{box} are thickness of the top and back gate oxide layers, respectively. T_{ch} ≈.65 nm is the thickness of the monolayer TMD channel. Length of the channel is denoted by L. Note that the figure is not drawn to scale.

$$\tan\left(\frac{T_{ox}}{\lambda_n/\pi}\right)\tan\left(\frac{T_{ch}/2}{\lambda_n/\pi}\right)=\frac{\varepsilon_{ox}}{\varepsilon_{ch}} \tag{2.2}$$

where, T_{ox} and T_{ch} are the effective oxide thickness and channel thickness respectively, while ε_{ox} and ε_{ch} are the respective permittivity of the oxide and channel material. This generalized scale length formula is derived from [40]. For a SOI device, $T_{ox} = T_{tox}$. In DG type devices, $T_{ox} = T_{tox} = T_{box}$ is assumed. For 2-D materials, $T_{ch} \to 0$. Thus we can establish a linear relation between oxide thickness and scale length, irrespective of channel and oxide permittivity.

$$\lambda_n = 2T_{ox}, \frac{2T_{ox}}{3}, \frac{2T_{ox}}{5}, \dots\dots\dots \tag{2.3}$$

We can calculate the coefficients b_n and $c_n$by putting boundary conditions in Equation (2.1). In subthreshold, potential is known at both source and drain i.e. $\varphi(0,z) = 0$ and $\varphi(L,z) = V_{ds}$. Thus we get from Equation (2.1),

$$b_n = \frac{2{\lambda_n}^2 \tan\left(\frac{T_{ox}}{\lambda_n/\pi}\right) \sin\left(\frac{T_{ch}/2}{\lambda_n/\pi}\right)}{\pi^2 T_{ox}\left[\frac{T_{ch}}{2} + \frac{\sin\left(\frac{T_{ch}}{\lambda_n/\pi}\right)}{sin\left(\frac{\frac{T_{ox}}{2}}{\lambda_n/\pi}\right)}\right]}(\varphi_m - V_{gs} - \chi) \tag{2.4}$$

$$c_n = \frac{2{\lambda_n}^2 \tan\left(\frac{T_{ox}}{\lambda_n/\pi}\right) \sin\left(\frac{T_{ch}/2}{\lambda_n/\pi}\right)}{\pi^2 T_{ox}\left[\frac{T_{ch}}{2} + \frac{\sin\left(\frac{T_{ch}}{\lambda_n/\pi}\right)}{sin\left(\frac{\frac{T_{ox}}{2}}{\lambda_n/\pi}\right)}\right]}(V_{ds} + \varphi_m - V_{gs} - \chi) \tag{2.5}$$

The values of b_n and c_n decays exponentially with n. A little modification in b_1 and c_1 terms allows us to consider only the n=1 terms. Thus potential $\varphi(x)$ can be approximated to be,

$$\varphi(x) = (V_{gs} + \chi - \varphi_m)\{1 - \frac{\sinh\left[\frac{\pi(L-x)}{\lambda}\right]}{\sinh\left(\frac{\pi L}{\lambda}\right)}\} + (V_{ds} - V_{gs} - \chi + \varphi_m)\frac{\sinh\left(\frac{\pi x}{\lambda}\right)}{\sinh\left(\frac{\pi L}{\lambda}\right)} \tag{2.6}$$

Where scale length λ is the lowest order solution of Equation (2.2).

2.2 Scale Length Equation

Solution of Equation (2.2) requires numerical calculation. One straight-forward approach is to consider it to be equal to twice of oxide thickness, as shown in Equation (2.3) [35]. But this assumption it too crude and claims to have no effect of channel and oxide materials on the scale length. Thus we need a scale length equation that can properly incorporate all the device and physical parameters. Also as we have entered the era of sub-10nm devices, it is unwise to consider the 0.65 nm thickness of monolayer 2-D TMD to be zero.

One starting point for finding a proper scale length equation is to approximate Equation (2.2) using the assumption,

$$\tan\left(\frac{T_{ch}/2}{\lambda/\pi}\right) \approx \frac{T_{ch}/2}{\lambda/\pi}$$

Typical values of T_{ch} for monolayer 2D TMD validates this approximation. Thus Equation (2.2) becomes,

$$\tan\left(\frac{T_{ox}}{\lambda/\pi}\right)\left(\frac{T_{ch}/2}{\lambda/\pi}\right) \approx \frac{\varepsilon_{ox}}{\varepsilon_{ch}} \tag{2.7}$$

The tangent part can be divided in sine and cosine functions of scale length and the rest of the parameters are constant for a device.

$$\frac{\sin\left(\frac{T_{ox}}{\lambda/\pi}\right)}{\cos\left(\frac{T_{ox}}{\lambda/\pi}\right)} = \frac{2\lambda\varepsilon_{ox}}{\pi T_{ch}\varepsilon_{ch}} \tag{2.8}$$

By expanding both the sine and cosine functions in Taylor series, we get a polynomial equation. Since, $\lambda \approx 2T_{ox}$, only the first three terms of both polynomials are considered. Thus (2.8) can be rewritten as,

$$\frac{1}{120}p^3 + \left(-\frac{1}{6} - \frac{\varsigma}{24}\right)p^2 + \left(1 + \frac{\varsigma}{2}\right)p - \varsigma = 0 \tag{2.9}$$

where, $p = (\pi T_{ox}/\lambda)^2$ and $\varsigma = 2T_{ox}\varepsilon_{ox}/T_{ch}\varepsilon_{ch}$

Equation (2.9) is a cubic equation that can be solved analytically and the solution will give the value of scale length. This value of scale length properly incorporates all physical and device parameters.

2.3 Subthreshold Current Modeling

The subthreshold drain current can be obtained from channel potential using the formula derived from [39],

$$I_{DS} = 4\pi m\mu W \frac{(kT)^2}{h^2}\left[\frac{1-\exp(-V_{DS}/v_{th})}{\int_0^L \exp\left(-\frac{\varphi(x)}{v_{th}}\right)dx}\right] \tag{2.10}$$

Where, m is the effective mass, μ is carrier-mobility, k is Boltzmann's constant, h is Planck's constant, T is temperature, and $v_{th} = kT/q$ is the thermal voltage. It is difficult to reduce the integral in the denominator in Equation (2.10) into elementary functions. Thus previous works have resorted to numerical calculation.

Using the expression of channel potential obtained from Equation (2.6) , we can form the integral as the multiplication of three exponential functions.

$$\int_0^L \exp\left(-\frac{\varphi(x)}{v_{th}}\right)dx = \int_0^L \exp(-M)\exp(-\mathrm{N})\exp(-\mathrm{R})\,dx \tag{2.11}$$

where,

$$M = (V_{gs} + \chi - \varphi_m)/v_{th}$$

$$N = \frac{1}{v_{th}}\left(V_{gs} + \chi - \varphi_m\right)\frac{\sinh[\frac{\pi(L-x)}{\lambda}]}{\sinh\left(\frac{\pi L}{\lambda}\right)}$$

$$R = \frac{1}{v_{th}}\left(V_{ds} - V_{gs} - \chi + \varphi_m\right)\frac{\sinh\left(\frac{\pi x}{\lambda}\right)}{\sinh\left(\frac{\pi L}{\lambda}\right)}$$

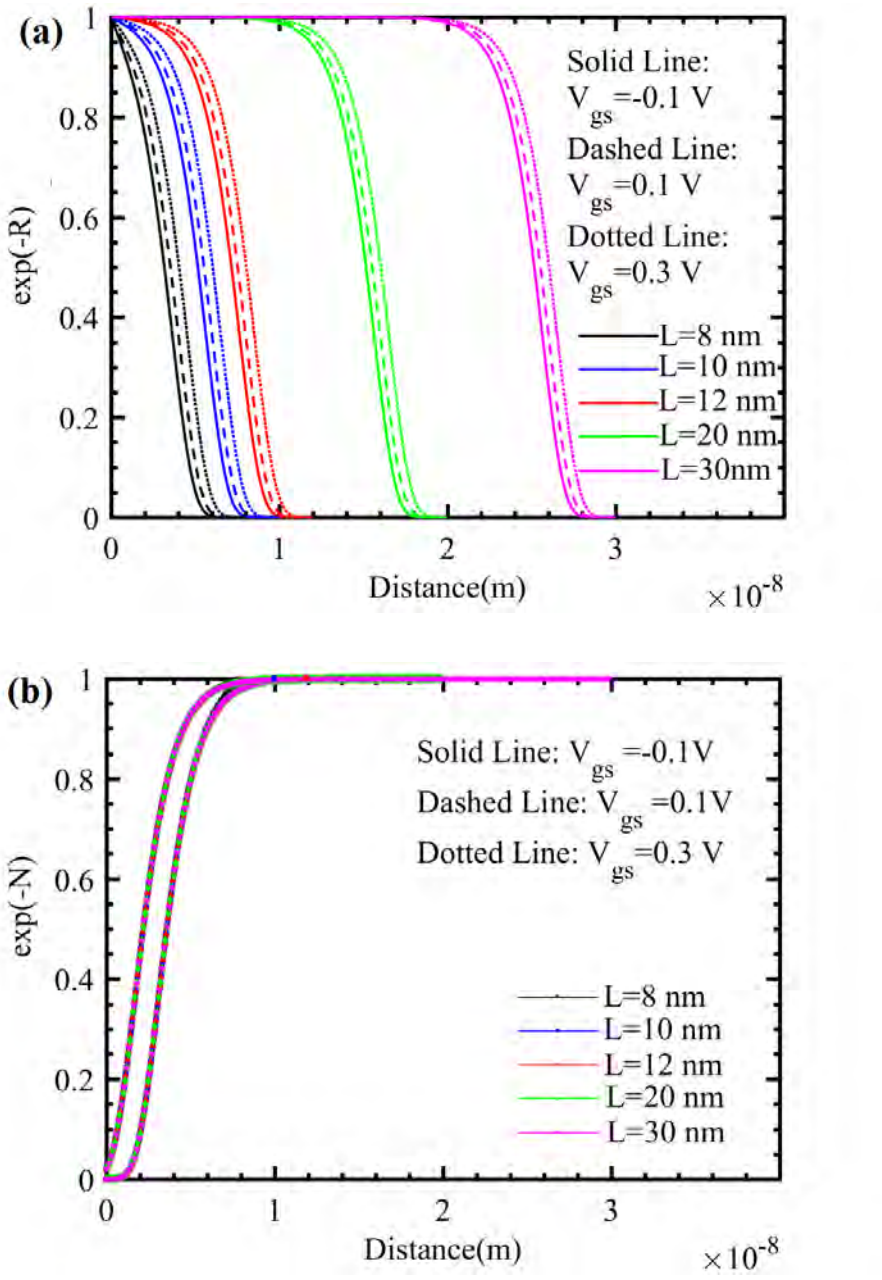

Figure 2.2: Variation of (a) exp(-R) and (b) exp(-N) functions of (6) in x direction for different gate voltages. There is a uniform decay of exp(-R) in the last 2 nm near the drain. On the other hand, exp(-N) does not vary with channel length.

The variation of these exponential functions along the channel direction x is plotted in Figure 2.2 for various channel lengths and bias conditions. For a given gate voltage, $\exp(-M)$ is a constant. It is evident from Figure 2.2 that while $\exp(-R)$ varies with channel length keeping a uniform relation, $\exp(-N)$ gives the same values for any length.

The uniform variation of $\exp(-R)$ suggests a linear relation between channel length and the integral of this exponential function. Because, the sine hyperbolic functions in the numerator of N and R assume non-zero value in distinct regions in the transport direction. For all channel lengths,

$$\frac{\sinh[\frac{\pi(L-x)}{\lambda}]}{\sinh\left(\frac{\pi L}{\lambda}\right)} \approx 0 \; for \; x > 8nm \tag{2.12}$$

And for L >10 nm,

$$\frac{\sinh\left(\frac{\pi x}{\lambda}\right)}{\sinh\left(\frac{\pi L}{\lambda}\right)} \approx 0 \; for \; x < (L-2)nm \tag{2.13}$$

This allows us to rewrite Equation (2.11) as,

$$\int_0^L \exp\left(-\frac{\varphi(x)}{v_{th}}\right) dx = \int_0^{8\,nm} \exp(-M)\exp(-\mathrm{N})\,dx + \int_{8\,nm}^{(L-2)\,nm} \exp(-M)dx + \int_{(L-2)nm}^{L} \exp(-M)\exp(-\mathrm{R})dx \tag{2.12}$$

If we add the first and the third term of the right hand side of Equation (2.12), we approximately get the denominator in Equation (2.10) for a FET with a channel length of 10 nm. The second term linearly varies with channel length, L. This reduces Equation (2.12) in,

$$\int_0^L \exp\left(-\frac{\varphi(x)}{v_{th}}\right) dx \approx \int_0^{10\,nm} \exp\left(-\frac{\varphi(x)_{10\,nm}}{v_{th}}\right) dx + \int_{10\,nm}^{L} \exp(-M)\,dx \tag{2.13}$$

where, $\varphi(x)_{10\,nm}$ is the channel potential for channel length, L_0=10 nm. Thus subthreshold current can be calculated for any L >10 nm using the following equation,

$$I_{DS} = [\frac{1}{I_{DS,L_0}} + \frac{\frac{h^2}{(kT)^2}\exp\left(-\frac{\varphi(x)}{v_{th}}\right)(L-L_0)}{4\pi m\mu W(1-\exp\left(-\frac{V_{DS}}{v_{th}}\right))}]^{-1} \tag{2.14}$$

where, I_{DS,L_0} is the drain current for a device with channel length L_0=10 nm under the conditions in which I_{DS} is being calculated. Figure 2.3 shows the subthreshold I_{DS} vs. V_{GS} curve obtained from Equation (2.14).

This model suggests that the calculation of drain current for any channel length greater than L_0 requires the numerical derivation of I_{DS,L_0}. However, it is evident from Equation (2.14) that I_{DS,L_0}can be calculated analytically if current for a longer device is known. For example, the analytical model proposed in the works of Cao et al. yields perfect results for L >30 nm. This model can be utilized to first calculate current for a long channel device. Then I_{DS,L_0} is calculated from Equation (2.14), which is later used to formulate the subthreshold model for devices with L >10 nm. The transfer characteristics in fig. 4 has been obtained this way.

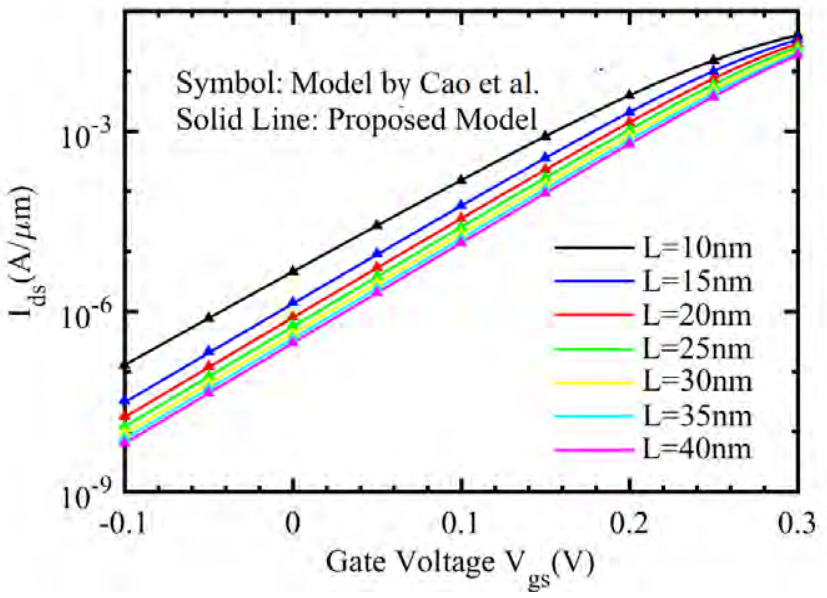

Figure 2.3: I_{ds} vs. V_{gs} in subthreshold for 2D TMD channel MOSFET calculated from Equation (2.14). V_{ds}=0.5 V.

Chapter 3

Analytical Modeling of Drain Current

An all-region analytical drain current model for 2-D TMD channel MOSFETs will be developed in this section. It is desirable to formulate a single drain current equation for all regions of operation. A good starting point for the all region model would be to derive an analytical formula of the surface potential. Surface potential based model are suitable for simulating devices with short channel length. Moreover, these type of models can be easily upgraded to include non-idealities like mobility degradation, interface traps, and non-ideal doping [36].

3.1 Establishing a Differential System

In order to capture the physics and operation of an electronic device, the first step is to formulate a differential system. Cao et al. presented the first differential model for 2D FET devices. It is safe to assume that the channel potential, $\varphi(x,z) \approx \varphi(x)$, since it has very small variation in the z-direction.

The differential system is established by applying Gauss's law in an infinitely small closed box shown in Figure 4.1. The height of the box is T_{ch}, width is W, and length is infinitesimally small Δx. Gauss's law states that the relation between the charge enclosed inside the box and electric field going out of the box can be formulated to be,

$$\oint_s \varepsilon \vec{E}.\overrightarrow{ds} = Q \tag{3.1}$$

Where, ε is the dielectric permittivity of the material at each surface of the encloser. The left hand side of the equation can be calculated by considering the electric field going out of each of the six surfaces of the box. The positive directions of the surface vectors $\overrightarrow{ds}$ are outward from each surface.

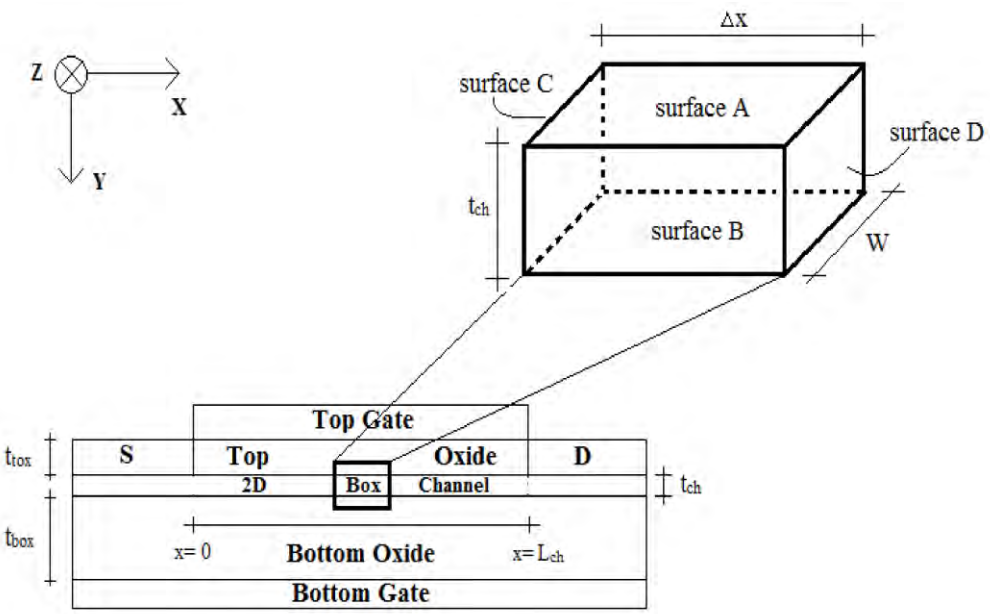

Figure 3.1: Schematic of a typical double gated 2D FET. The inset is the zoomed-in view of an infinitely small enclosure along the channel in which Gauss's law has been applied to formulate the differential system.

The left hand side component of Equation (3.1) for surface A of figure 3.1,

$$-\frac{V'_{gt}-\varphi(x)}{T_{tox}}\varepsilon_{tox}\Delta xW \tag{3.2}$$

The left hand side component of Equation (3.1) for surface B of figure 3.1,

$$\frac{\varphi(x)-V'_{gb}}{T_{box}}\varepsilon_{box}\Delta xW \tag{3.3}$$

The left hand side component of Equation (3.1) for surface C of figure 3.1,

$$\frac{d\varphi(x)}{dx}\varepsilon_{ch}T_{ch}W \tag{3.4}$$

The left hand side component of Equation (3.1) for surface D of figure 3.1,

$$-\frac{d\varphi(x+\Delta x)}{dx}\varepsilon_{ch}T_{ch}W \tag{3.5}$$

Here, $\varepsilon_{ch}, \varepsilon_{tox}, \varepsilon_{box}$ are the permittivity of channel material, top gate oxide and bottom gate oxide respectively. Contribution from E and F surfaces are zero since there are no electric field component along the y axis.

V'_{gt} and V'_{gb} are effective gate voltage, calculated after subtracting flat band voltages $V_{FBt/b}$ from the input gate bias $V_{gt/b}$.

$$V'_{gt} = V_{gt} - V_{FBt} \tag{3.6}$$

$$V'_{gb} = V_{gb} - V_{FBb} \tag{3.7}$$

Flat-band volatage can be defined as the work function difference between the top bottom electrodes and the TMD channel.

By substituting the electric fields from the above four equations in Equation (3.1) and doing some reorganizations, we can formulate the second order equation as,

$$\frac{d^2\varphi(x)}{dx^2} - \frac{\varphi(x)}{\lambda'^2} + \gamma = \frac{-Q_s}{\varepsilon_{ch}T_{ch}} \tag{3.8}$$

Here, charge density Q_s has been established as follows,

$$Q_s = C_{tox}\left(V'_{gt} - \varphi(x)\right) + C_{box}(V'_{gb} - \varphi(x)) \tag{3.9}$$

Where, $C_{tox} = \varepsilon_{tox}/T_{tox}$ and $C_{box} = \varepsilon_{box}/T_{box}$ are the gate oxide capacitances in top and bottom gates, respectively. The constant term in the differential equation is,

$$\gamma = \frac{C_{tox}V'_{gt} + C_{box}V'_{gb}}{\varepsilon_{ch}T_{ch}} \tag{3.10}$$

Also, the new scale length λ' is defined as,

$$\frac{1}{\lambda'^2} = \frac{C_{tox} + C_{box}}{\varepsilon_{ch}T_{ch}} \tag{3.11}$$

Rearranging this second order equation, we get,

$$\frac{d^2\varphi(x)}{dx^2} - \left(\frac{2C_{tox} + 2C_{box}}{\varepsilon_{ch}T_{ch}}\right)\varphi(x) + \frac{2C_{tox}V'_{gt} + 2C_{box}V'_{gb}}{\varepsilon_{ch}T_{ch}} = 0 \tag{3.12}$$

So the governing equation for obtaining the electrostatic potential is,

$$\frac{d^2\varphi(x)}{dx^2} - \frac{\varphi(x)}{l^2} + 2\gamma = 0 \tag{3.13}$$

where,

$$l = \sqrt{\frac{\varepsilon_{ch} T_{ch}}{2C_{tox} + 2C_{box}}} \tag{3.14}$$

Equation 3.14 is a linear differential equation with constant coefficients. A closed form solution of this differential system is possible. The general solution can be assumed to be,

$$\varphi_g(x) = c_1 \cosh\left(\frac{x}{l}\right) + c_2 \sinh\left(\frac{x}{l}\right) \tag{3.15}$$

Assuming, $c_1 = d_1 \sinh(\frac{L}{l})$ and $c_2 = d_2 - d_1 \cosh(\frac{L}{l})$, we can rewrite Equation 3.15 as,

$$\varphi_g(x) = d_1 \sinh(\frac{L}{l}) \cosh\left(\frac{x}{l}\right) + d_2 sinh(\frac{x}{l}) - d_1 \cosh(\frac{L}{l}) \sinh\left(\frac{x}{l}\right) \tag{3.16}$$

Thus channel length L is incorporated in the solution of electrostatic potential.

$$\varphi_g(x) = d_1 \sinh(\frac{L-x}{l}) + d_2 sinh(\frac{x}{l}) \tag{3.17}$$

We can further simplify this equation by redefining the d_1 and d_2 constants as follows,

$$\varphi_g(x) = e_1 \frac{\sinh(\frac{L-x}{l})}{\sinh(\frac{L}{l})} + e_2 \frac{sinh(\frac{x}{l})}{\sinh(\frac{L}{l})} \tag{3.18}$$

Here, e_1 and e_2 constants can be determined by employing boundary conditions of the MOSFET. The particular solution of Equation 3.13 can be obtained by assuming $\varphi_p(x) = A$. Thus,

$$0 - \frac{A}{l^2} + 2\gamma = 0 \tag{3.19}$$

So the complete solution for the electrostatic potential is,

$$\varphi(x) = e_1 \frac{\sinh(\frac{L-x}{l})}{\sinh(\frac{L}{l})} + e_2 \frac{sinh(\frac{x}{l})}{\sinh(\frac{L}{l})} + 2\gamma l^2 \tag{3.20}$$

3.2 Determining the Constants e_1 and e_2

Boundary conditions of MOSFET allows us to determine the source and drain potentials, which in return helps us calculate the constants e_1 and e_2. At source (x=0), the electrostatic potential,

$$\varphi(0) = V(0) + \frac{kT}{q}\ln(\frac{Q_s}{N_{DOS}}) \tag{3.21}$$

Where,

$$V(0) = V_s + V_{bi} \tag{3.22}$$

Here, V_{bi} is the source channel interface given by,

$$V_{bi} = \frac{kT}{q}\ln(\frac{Q_s N_A}{n_i^2}) \tag{3.23}$$

Q_s is the mobile electron density and N_{DOS} is the effective density of states. The relation between these two parameters is given by,

$$Q_s = \int_{E_c}^{\infty} DOS_{2D}(E) f(E - E_F) dE \approx N_{DOS} e^{\frac{q(\varphi - V)}{kT}} \tag{3.24}$$

For source and drain region, carrier concentration Q_s is given by the source and drain doping concentration. Thus the source and drain potential can be written as,

$$\varphi_s = \varphi(0) = V_s + V_{bi} + \frac{kT}{q}\ln(\frac{N_D}{N_{DOS}}) \tag{3.25}$$

$$\varphi_D = \varphi(L) = V_D + V_{bi} + \frac{kT}{q}\ln(\frac{N_D}{N_{DOS}}) \tag{3.26}$$

At x=0, Equation 3.20 becomes,

$$\varphi_s = \varphi(0) = e_1 + 2\gamma l^2 \quad (3.27)$$

At x=L, Equation 3.20 becomes,

$$\varphi_D = \varphi(L) = e_2 + 2\gamma l^2 \quad (3.28)$$

Thus the constants e_1 and e_2 can be calculated to be,

$$e_1 = \varphi_s - 2\gamma l^2 \quad (3.29)$$

$$e_2 = \varphi_D - 2\gamma l^2 \quad (3.30)$$

3.3 Calculation of Effective Density of States

Effective density of states for 2-D semiconductor materials is given by [36],

$$DOS_{2D} = \sum_i g_s g_i \, m_i^* / 2\pi\hbar^2 \quad (3.31)$$

Here,

g_s =spin degeneracy

g_i = valley degeneracy

m_i^* =effective mass of mobile carrier

ħ =Reduced Plank's constant

i= valley index

Due to the relatively large DOS (in the order of 10^{14} $eV^{-1}cm^{-2}$) of 2-D TMD materials, FETs based on them generally work on non-degenerate conditions. While considering spin degeneracy from the valleys, the second lowest valley is also considered since there are six such valleys in the first Brillouine zone and ΔE_c is only around 2kT. Other valleys are too high to contribute and thus neglected in the calculation of effective density of states.

Considering the above effects, the effective density of states is calculated to be,

$$N_{DOS} = \frac{g_s g_1 m_1^* kT}{2\pi\hbar^2} + \frac{g_s g_2 m_2^* kT}{2\pi\hbar^2} e^{-\frac{\Delta E_c}{kT}} \tag{3.32}$$

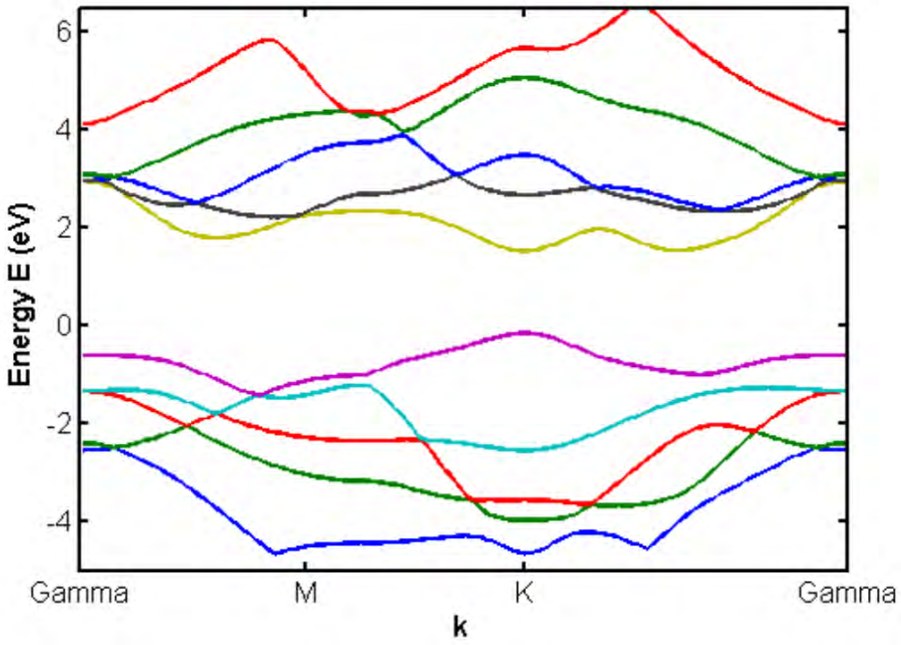

Figure 3.2: E-k diagram of WSe_2 obtained from first principle DFT simulation in Quantum Espresso Software. The diagram shows lowest conduction valley at K-point. The nearest low point is between K and Gamma points. The energy difference between these two lowest valets is around 50 meV.

3.4 Drain Current Modeling

Carrier transport is governed by the drift-diffusion equation,

$$I_{ds}(x) = \mu(x) W Q_s \frac{dV(x)}{dx} \tag{3.33}$$

Here, $\mu(x)$ is the channel electron mobility.

For a 2-D TMD channel MOSFET, it is safe to assume that the drain current remains constant throughout the channel. The pristine TMD-oxide contact ensures that the gate leakage current remains negligible. So, we can write, $I_{ds}(x) = I_{ds}$. Also if we consider a

constant electron mobility throughout the channel, $\mu(x)$ can be approximated as μ_0. Thus, Equation 3.33 can be modified as,

$$I_{ds} = \mu_0 W Q_s \frac{dV(x)}{dx} \tag{3.34}$$

Integrating Equation 3.34 with respect to x from x=0 to x=L we get,

$$\int_0^L I_{ds} dx = \mu_0 W \int_{x=0}^{x=L} Q_s dV(x) \tag{3.35}$$

We can change the limit of the integral in the right hand side by applying the source and drain voltages as limiting value for V.

$$I_{ds} = \mu_0 \frac{W}{L} \int_{V_s}^{V_D} Q_s dV \tag{3.36}$$

From Equation (3.24), we can write,

$$V = \varphi - \frac{kT}{q} \ln(\frac{Q_s}{N_{DOS}}) \tag{3.37}$$

From Equation (3.9) we can put the expression of charge density Q_s as,

$$V = \varphi - \frac{kT}{q} \ln(\frac{C_{tox}V'_{gt} + C_{box}V'_{gb} - (C_{tox} + C_{box})\varphi(x)}{N_{DOS}}) \tag{3.38}$$

Differentiating V with respect to potential φ,

$$\frac{dV}{d\varphi} = 1 + \frac{kT}{q} \frac{\frac{(C_{tox} + C_{box})\varphi(x)}{N_{DOS}}}{\frac{C_{tox}V'_{gt} + C_{box}V'_{gb} - (C_{tox} + C_{box})\varphi(x)}{N_{DOS}}} \tag{3.39}$$

$$\frac{dV}{d\varphi} = 1 + \frac{kT}{q} \frac{(C_{tox} + C_{box})\varphi(x)}{C_{tox}V'_{gt} + C_{box}V'_{gb} - (C_{tox} + C_{box})\varphi(x)} \tag{3.40}$$

$$\frac{dV}{d\varphi} = 1 + \frac{kT}{q} \frac{(C_{tox} + C_{box})\varphi(x)}{Q_s} \tag{3.41}$$

Using this final expression of $\frac{dV}{d\varphi}$ we can rewrite Equation (3.36),

$$I_{ds} = \mu_0 \frac{W}{L} \int_{V_s}^{V_D} Q_s \frac{dV}{d\varphi} d\varphi \tag{3.42}$$

$$I_{ds} = \mu_0 \frac{W}{L} \int_{\varphi_s}^{\varphi_D} Q_s \{1 + \frac{kT}{q} \frac{(C_{tox} + C_{box})\varphi(x)}{Q_s}\} d\varphi \tag{3.43}$$

$$I_{ds} = \mu_0 \frac{W}{L} \int_{\varphi_s}^{\varphi_D} (Q_s + \frac{kT}{q}(C_{tox} + C_{box})\varphi) d\varphi \tag{3.44}$$

$$I_{ds} = \mu_0 \frac{W}{L} \int_{\varphi_s}^{\varphi_D} \{C_{tox}V'_{gt} + C_{box}V'_{gb} - (C_{tox} + C_{box})\varphi + \frac{kT}{q}(C_{tox} + C_{box})\varphi\} d\varphi \tag{3.45}$$

$$I_{ds} = \mu_0 \frac{W}{L} \int_{\varphi_s}^{\varphi_D} \{C_{tox}V'_{gt} + C_{box}V'_{gb} + (\frac{kT}{q} - 1)(C_{tox} + C_{box})\varphi\} d\varphi \tag{3.46}$$

$$I_{ds} = \mu_0 \frac{W}{L} [\left(C_{tox}V'_{gt} + C_{box}V'_{gb}\right)(\varphi_D - \varphi_S) + \frac{kT - q}{2q}(C_{tox} + C_{box})(\varphi_D^2 - \varphi_S^2)] \tag{3.47}$$

We have utilized the potential profile derived before, by replacing V with φ. With the known source voltage V_s and drain voltage V_D, the lower limit φ_s and upper limit φ_d can be obtained by applying Newton-Raphson's approximation. Equation (3.47) can be used as the final closed form expression for the drain current under all regions of operations.

3.4.1 Velocity Saturation Effect

In long channel devices, effects of lateral electric field on velocity saturation is negligible. Moreover, TMD materials have been found to exhibit a relatively high critical electric field. Thus the effect of velocity saturation does not play a significant role in long channel 2-D TMD devices. However, the prominent vertical electric field in 2-D channel shifts the charge centroid toward the dangling bonds of the gate dielectric, increasing scattering and thus reducing the mobility. A rigorous mobility model for 2D FETs is still not available.

Hence, we used an widely accepted model for Si-MOSFET and applied it for 2-D TMD channel FETs.

The new corrected mobility μ is,

$$\mu = \frac{\mu_0}{\sqrt{1 + (\frac{\mu_0}{L v_{sat}}(\varphi_D - \varphi_S))^2}} \tag{3.36}$$

In order to incorporate this velocity model in the drain current equation, we need to put it inside the integral instead of treating it as a constant.

$$\mu = \frac{\mu_0}{\sqrt{1 + (\frac{\mu_0}{L v_{sat}}(\varphi_D - \varphi_S))^2}} \tag{3.36}$$

This last step requires numerical calculation to properly find the drain current.

3.4.2 Interface Trap Effects

Trapping is a major issue in the realization of 2-D TMD devices. It is very important to include them to any compact model, otherwise the model can predict unrealistic high drain currents. The interface trap states occupied by electrons are as follows,

$$N_{trap} = \sum_i \frac{D_{trap,i}}{1 + e^{\frac{V - \varphi + E_{it}}{v}}} \tag{3.37}$$

Here, $D_{trap,i}$ and E_{it} are trap density and trap energy level calculated at ith subband. In order to incorporate this trap equation we need to modify carrier density function and subtract trap density for mobile carrier density.

Chapter 4

Results and Discussions

In this chapter, we present the validation of our model and its application in conducting a comprehensive study of the 2-D TMD channel MOSFET. Our model is validated against established numerical models and experimental results.

4.1 Validation of the Subthreshold Model

In order to verify the subthreshold model, transfer characteristics and output characteristics are calculated using the model and put into test against numerical simulations for both SOI and DG type structures. We have initially used MoS_2 as the channel material due to its promising features and applications in semiconductor industry. The device and physical parameters of the FET are $m=0.48m_0$, $\mu=300$ cm^2/Vs, $\varepsilon_{ch}=4.8\varepsilon_{ch}$, and $T_{ch}=0.65$ nm. Here m_0 is electron rest mass and ε_0 is vacuum permittivity. In later part of the work, we have used different channel materials and their properties will be noted when used. Channel length has been varied from 10 nm to 50 nm. 2nm thick HfO_2 and SiO_2 serve as the top and bottom gate oxides respectively. For SOI structure, bottom gate oxide is much thicker (90 nm).

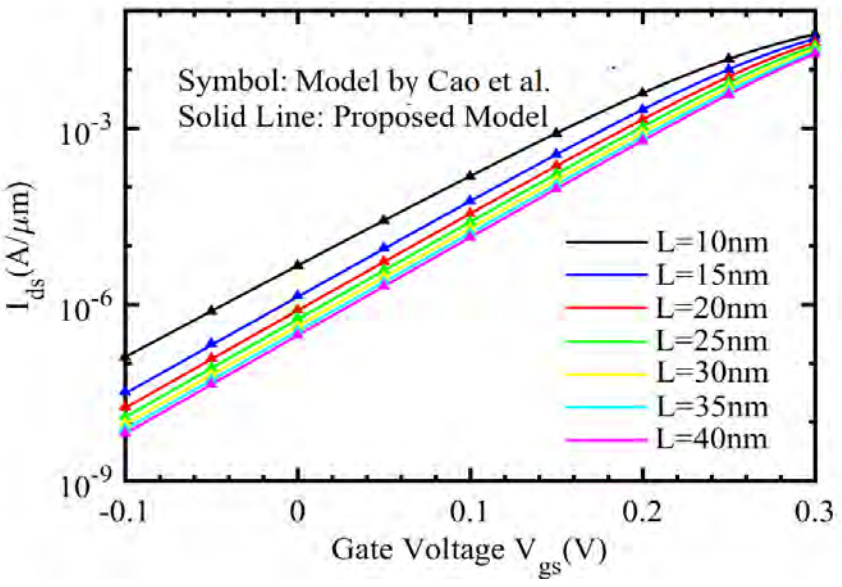

Figure 4.1: I_{ds} vs. V_{gs} in subthreshold for 2D TMD channel MOSFET. Vds=0.5 V.

Figure 4.1 and 4.2 shows that our model is in good agreement with previously established numerical models for long channel devices. But in case of short channel devices, the renowned model proposed by Cao et al. deviates from actual value. This stems from an assumption during the establishment of the differential system in the beginning that the electric field in the oxides is along the vertical direction. In fact, electric field in the top and bottom oxides also has lateral component similar to that considered in the channel. The preassumption that electric field in the gate dielectric is vertical to the channel, is only valid when the channel is much thicker than the gate dielectric.

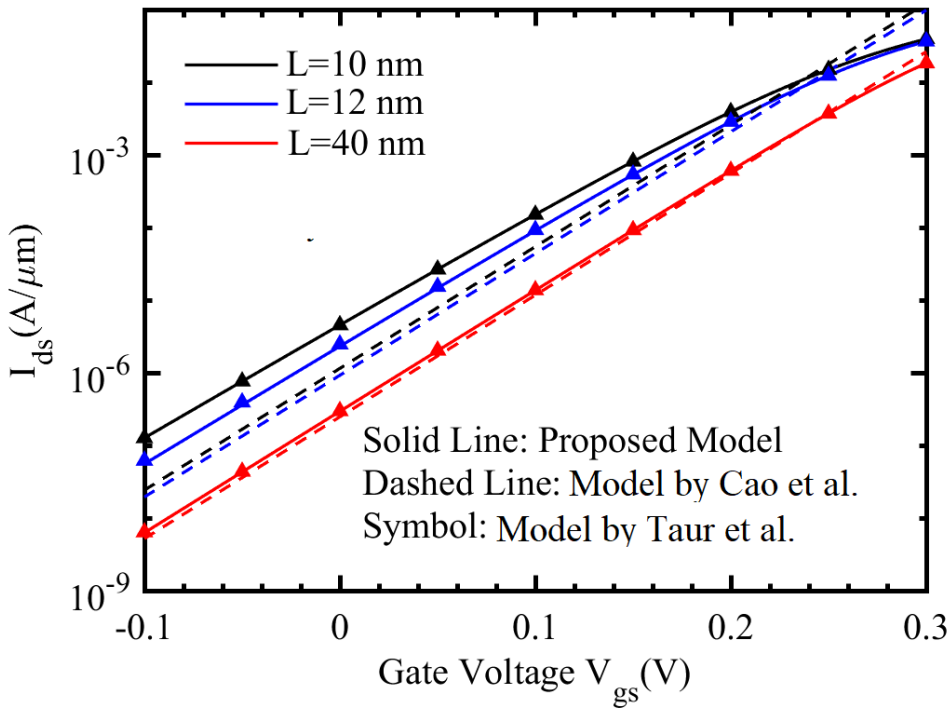

Figure 4.2: Comparison of our subthreshold model with models proposed in [5] and [6]. Our model is in perfect agreement with that of Taur et al. for both short and long channel devices. On the other hand, the model proposed by Cao et al. produces erroneous results for sub-30 nm devices. Subthreshold profile of the 10 nm device is extracted from long channel model in [5] using (11). Then it is used to model transfer characteristics for the 12 nm device. Bias was kept constant at Vds=0.5 V.

Taur et al. have proposed a short channel model that can correctly produce device behavior in channel length well below 30 nm. However, their model has assumed a constant scale

length which is exactly double of gate oxide thickness. This constant value of scale length fails to consider other important factors like permittivity of channel and dielectric material, channel thickness, thus it fails to incorporate the effect of different oxide materials. Our analytical solution of scale length accounts for these device and physical parameters and is verified against numerical solution of Equation (2.2) for different oxide materials. It should be noted that the scale length exponentially decays for oxides with higher dielectric constant. This makes the deviation in Taur model less prominent in high-K materials. Since the scale length is a key parameter in determining the subthreshold current, lower accuracy in determining this will eventually lead to erroneous results.

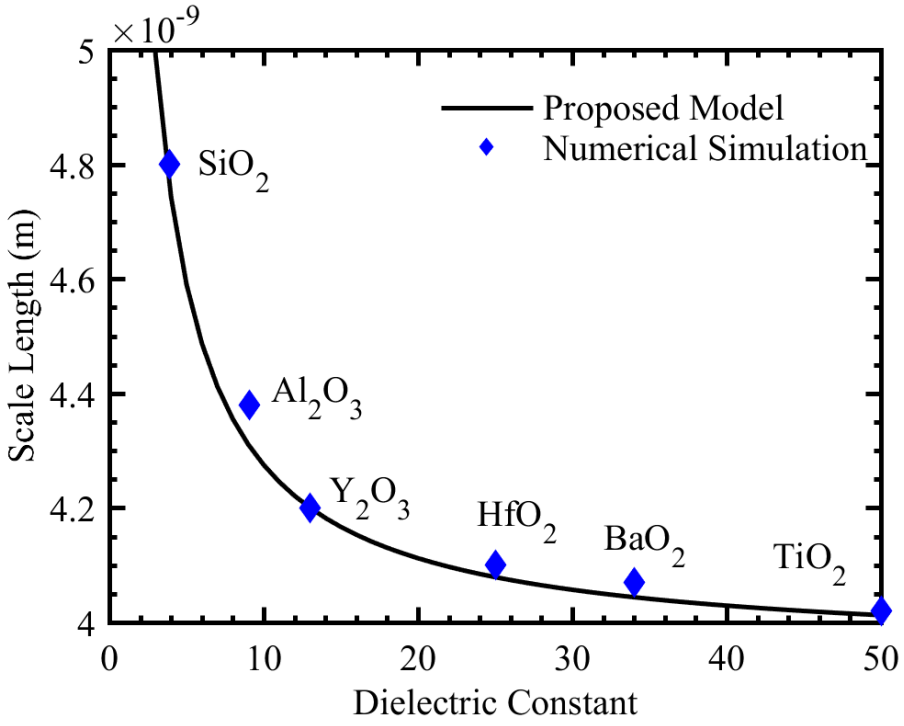

Figure 4.3: Variation of scale length with the permittivity of oxide materials for T_{ox}= 2 nm. Taur et al. proposed a constant scale length of $2T_{ox}$ in all cases.

It should be noted that our subthreshold model is valid for $V_{GS} < \varphi_m - \chi$ and L >10 nm. For higher gate voltages, velocity saturation model needs to be employed. On the other hand, when channel length is scaled down below 10 nm, the approximation in the calculation of subthreshold current yields erroneous results. For L >10 nm, the constituents of the right hand side of Equation (2.11) produces a plateau-shaped distribution where the two halves of normal distribution have a rectangle in between. The width of this rectangle

varies linearly with channel length. However, for L <10 nm the rectangle vanishes and a Gaussian curve of lower magnitude is formed. Figure 4.4 shows the Gaussian for sub-10 nm devices and the plateau shape for other channel lengths. The exponential functions are equally distant from each other since their channel lengths are equally distributed. This linear relation with channel length works as the basis of our analytical model, as it allows us to calculate the integral without involving numerical calculations.

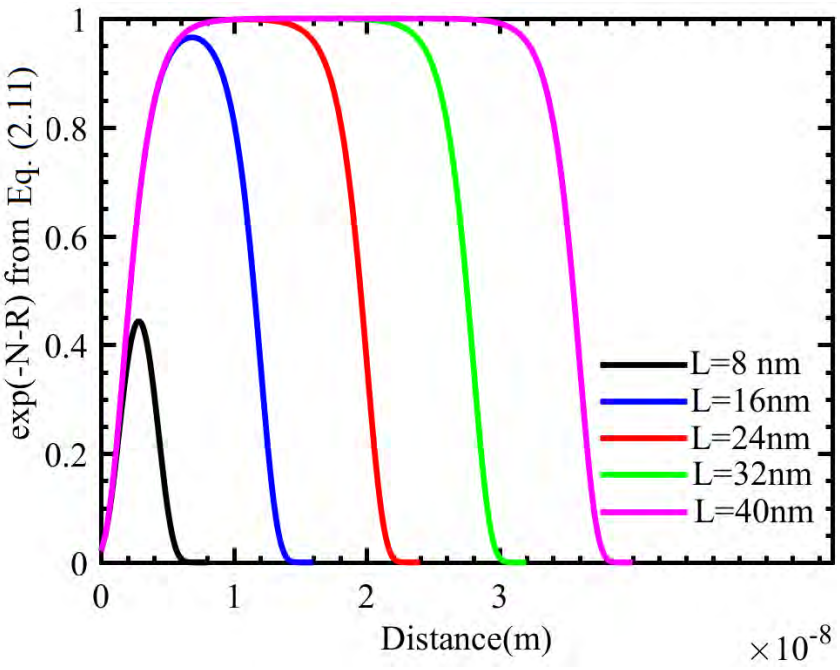

Figure 4.4: Variation of exp(-N-R) from Equation (2.11) with channel length in constant bias condition (V_{gs}=0.1V and V_{ds}=0.5V). In long channel devices, the width of the plateaus uniformly varies with channel length, while the magnitude remains same. In lower channel lengths the plateau shape is transformed into a Gaussian with lower magnitude.

One of the key features that distinguishes 2-D TMD channel MOSFETs from other transistors is its low subthreshold swing i.e. the inverse of the derivative of the subthreshold slope. Figure 4.5 demonstrates the subthreshold swing for TMD transistors. For long channel devices, SS is very close to its theoretical limit of 60 mv/dec. Although SS is considerably low for these long channel devices, it exponentially increases as channel One of the key features that distinguishes 2-D TMD channel MOSFETs from other transistors is its low subthreshold swing i.e. the inverse of the derivative of the subthreshold slope. Figure 4.5 demonstrates the subthreshold swing for TMD transistors. For long channel devices, SS is very close to its theoretical limit of 60 mv/dec. Although SS is considerably

low for these long channel devices, it exponentially increases as channel length comes below 15 nm. The model proposed by Cao et al. underestimates this variation of SS.

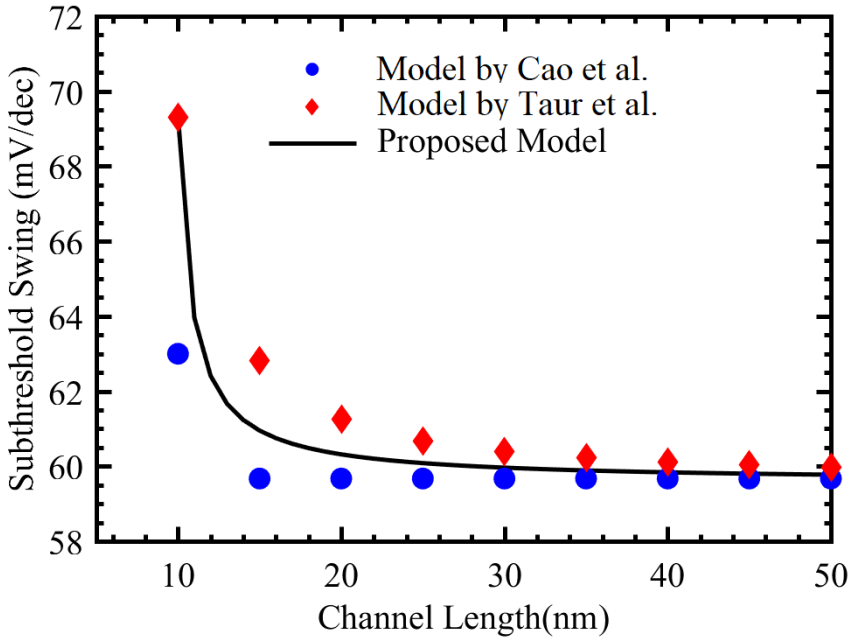

Figure 4.5: Variation of subthreshold swing with channel length.

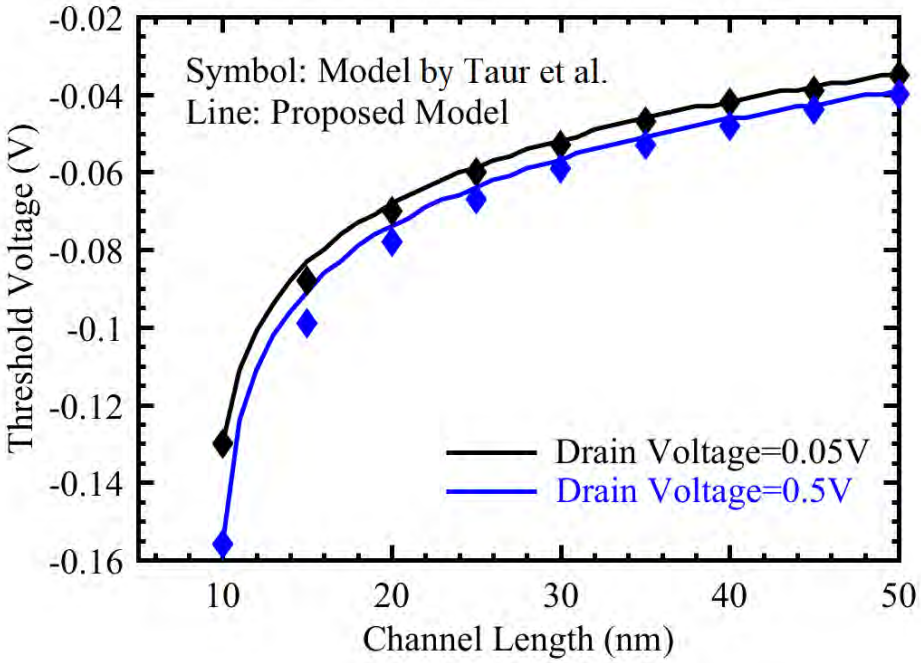

Figure 4.6: Threshold voltage roll-off calculated from our model and the model proposed by Taur et al.

The V_t roll-off curve in figure 4.6 is obtained by taking a constant current value cut through the subthreshold transfer characteristics curve. It is apparent that the roll-off problem starts to appear in a channel length below 15 nm. Above this length, the little variation in threshold voltage is ignorable. However, this roll-off problem becomes very prominent for low drain voltage operation.

4.2 Validation of the All Region Compact Model

The proposed compact model is validated against numerically simulated results. The compact model shows excellent match of surface potential both at the source side (φ_s) and the drain side (φ_d) against numerical simulation data with respect to applied gate voltage and drain bias. The proposed drain current model is then compared to a long channel device. The devices in Figure 4.7 has top oxide thickness of 2 nm. HfO_2 is used as the top dielectric. Bottom oxide has thickness of 2 nm for DG MOSFET and a long thickness of 90 nm for the SOI structure. In both cases, SiO_2 has been used as the bottom oxide material. Both figures demonstrate excellent agreement with simulation data. Non ideal effects like velocity saturation has not been considered in preparing figure 4.8. Same device topology was investigated by Cao et al. as well.

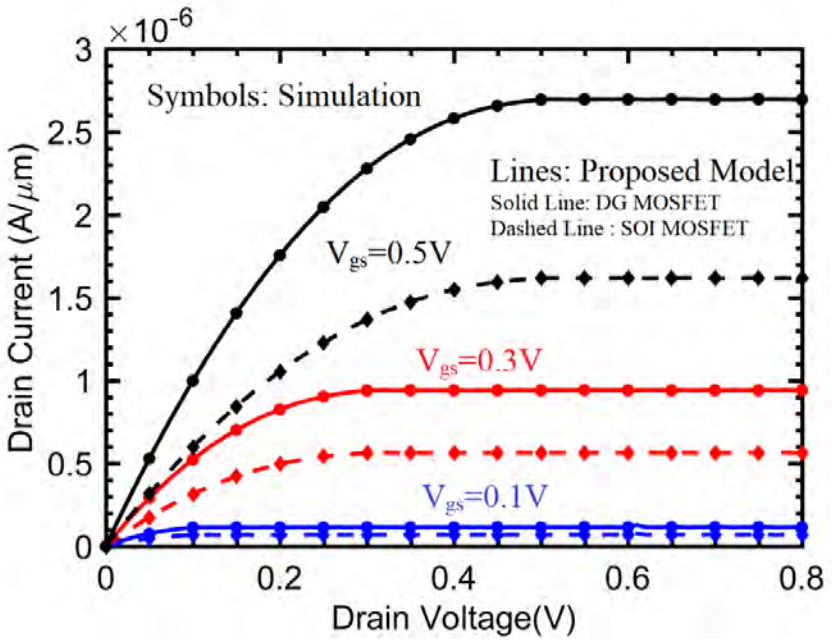

Figure 4.7: Output characteristics of an ideal 2D MOSFET in DG and SOI modes.

A real test of any realistic model is to quantitatively fit experimental results. Therefore, we validated our results with experimentally reported TMD materials-based nFET and pFET devices. We have found that the trap states play a very significant role in determining device performance in these devices. The physical parameters used in model verification are given in table 4.1.

Table 4.1: Physical Properties of TMD Materials

Material	Bandgap (eV)	Effective Mass $(\frac{m_n}{m_0} / \frac{m_h}{m_0})$	Dielectric Constant	Mobility (cm^2/Vs)
MoS_2	1.8	0.56/0.64	4.8	200
$MoTe_2$	1.10	0.64/0.78	8.0	9.5
WSe_2	1.62	0.35/0.46	4.5	10

The MoS_2-based nFET reported by Sachid et al. for a device with 2 μm channel length, 20 nm thick ZrO_2 front gate oxide, and 260 nm thick SiO_2 back oxide, is verified with the model and is shown in Figure 4.8 [41]. The transfer and output characteristics of mechanically exfoliated WSe_2 nFET with L_{ch} = 6.4μm, t_{tox} = 17.5 nm (ZrO_2), and t_{box} = 270 nm (SiO_2) are used to compare with the model as well in Figure 4.9 [42]. In addition to the MoS_2 and WSe_2 nFETs, experimentally reported 1 μm channel length $MoTe_2$ nFET is also used to validate the model behavior (see Figure 4.10), where t_{tox} is 1 nm with dielectric value of 5 and bottom oxide is 285 nm thick SiO_2 [43]. In all the three nFET devices used in validation, the model accurately fits the experimental data for the transfer as well as the output characteristics. It should be noted that the model matched experimental results only after incorporating trap density in the drain current. This demonstrates the necessity of using interface trap models in the compact model design. All the experimental data are available for SOI structure. Back gate voltage V_{bg} =0 in all cases.

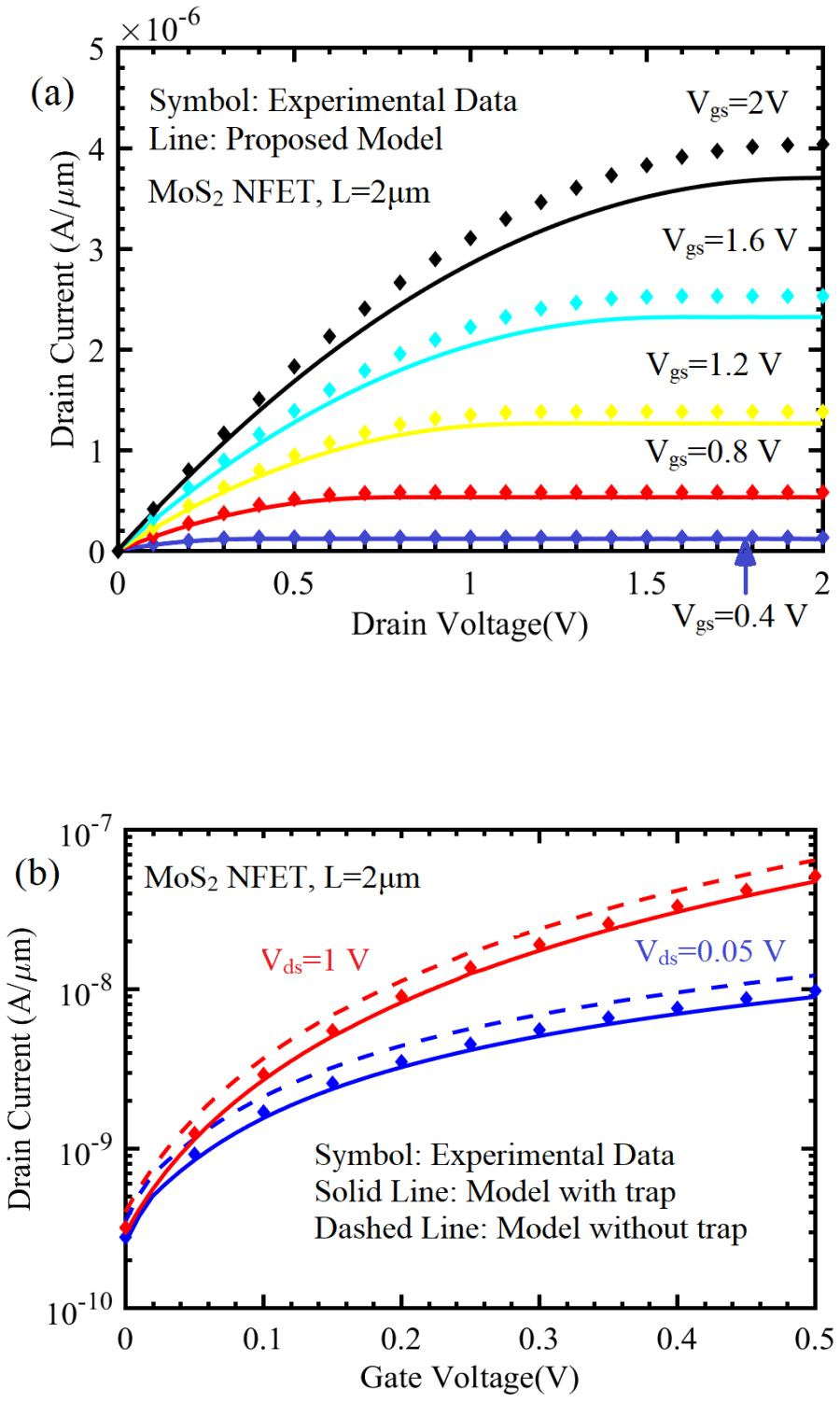

Figure 4.8: Drain current model behavior against the data of 2.0 μm long channel MoS_2 nFET experimental device reported by Sachid et al. (a) Output characteristics for V_{gs}= 0.4V to V_{gs} =2 V .(b) Transfer characteristics for V_{ds}=0.05 V(blue) and V_{ds}= 1 V(red).

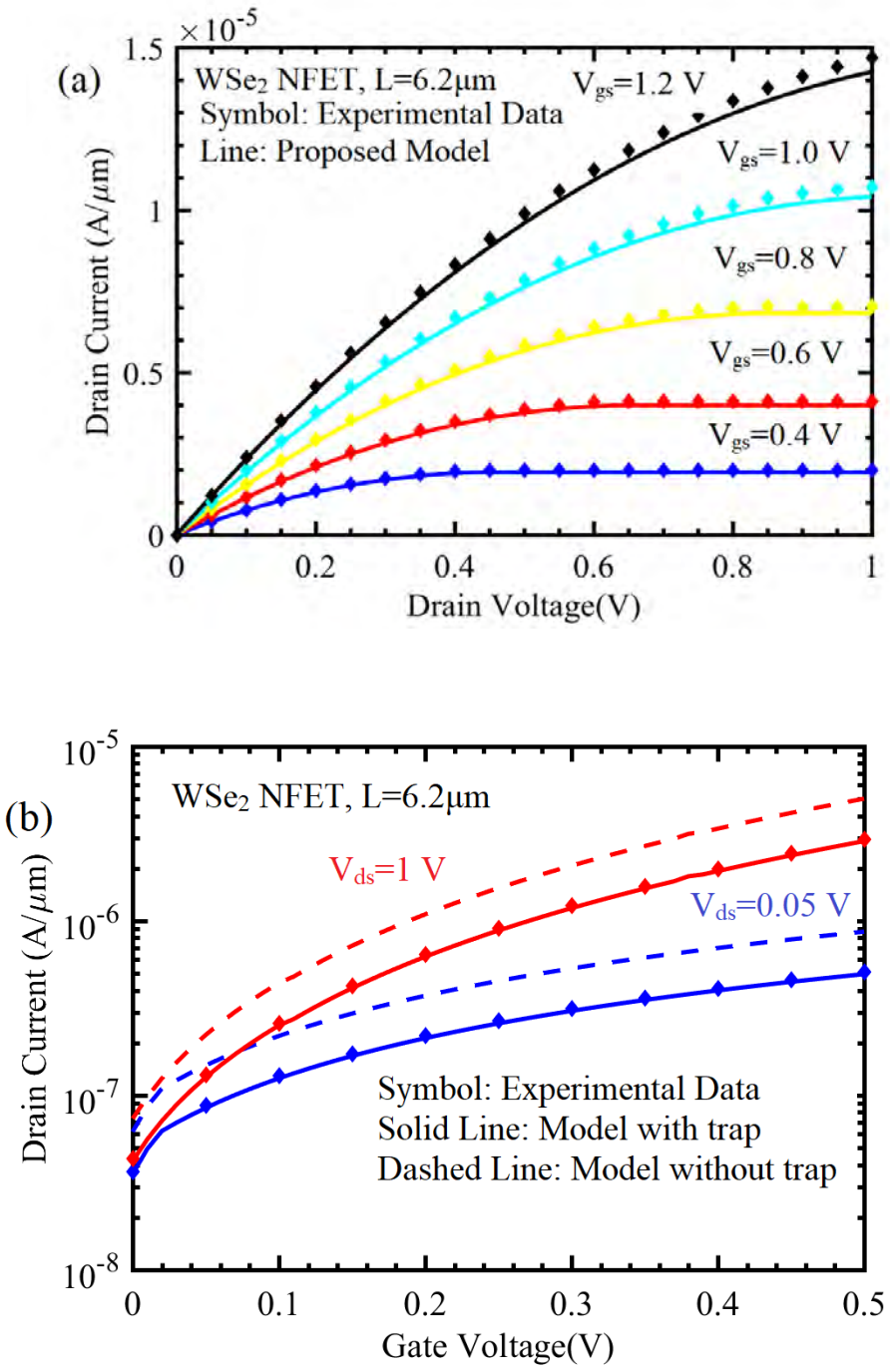

Figure 4.9: Drain current model behavior against the data of 6.2 μm long channel WSe_2 nFET experimental device reported by Fang et al. (a) Output characteristics for V_{gs}=0.4 V to 1.2 V (b) Transfer characteristics for V_{ds}=0.05 V(blue) and V_{ds}= 1 V(red)

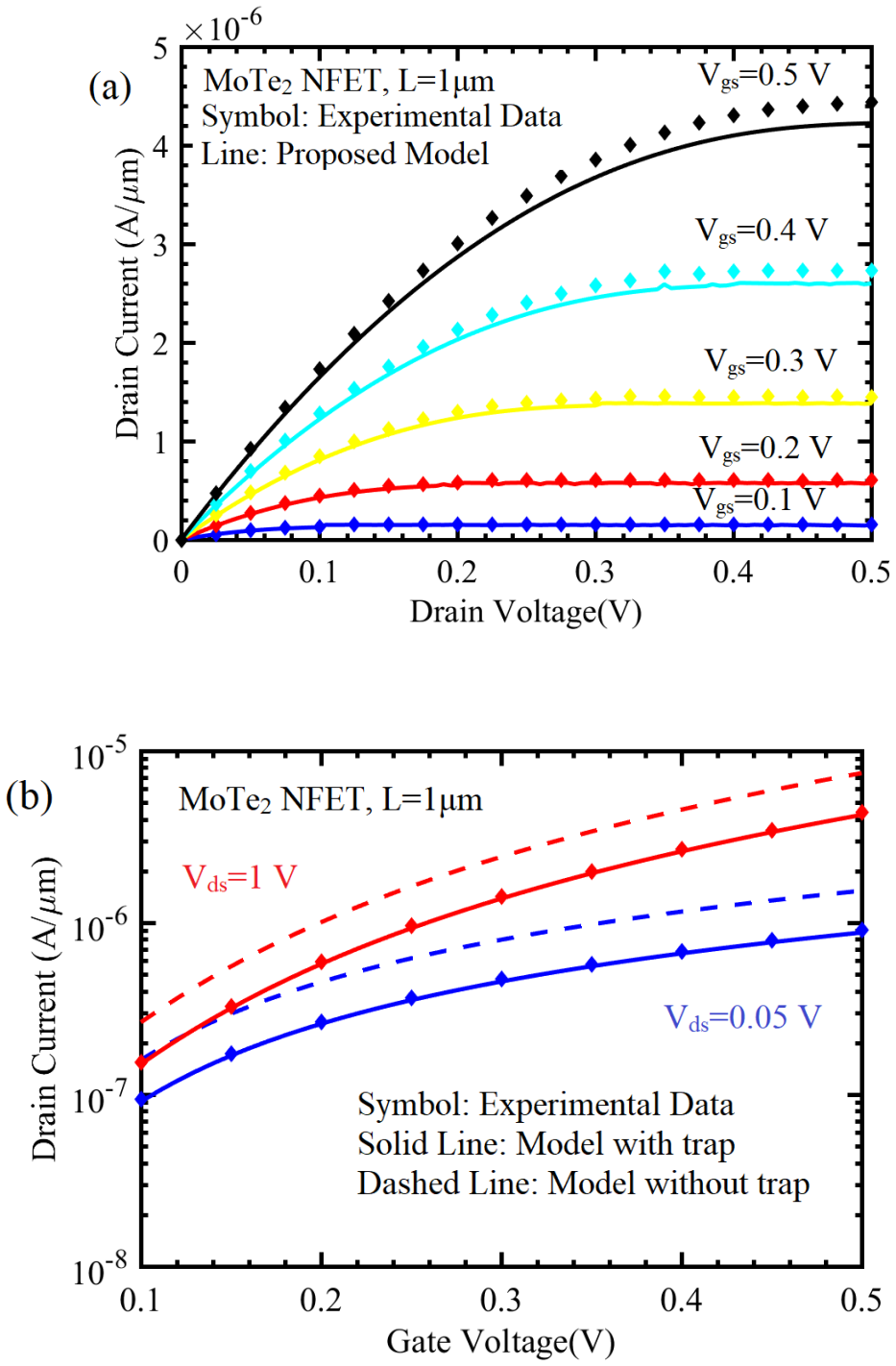

Figure 4.10: Drain current model behavior against the data of 1.0 μm long channel $MoTe_2$ nFET experimental device reported by Xu et al. (a) Output characteristics for V_{gs}=0.1 to V_{gs}=0.5 V (b) Transfer characteristics for V_{ds}=0.05 V(blue) and V_{ds}= 1 V(red)

The dashed line in the transfer characteristics exhibits the impact of traps on the device characteristics (threshold voltage, subthreshold slope, and ON current) and highlights the importance of including the trap effects in drain current. It should be noted that while mobility degradation affects the ON current, it does not alter the threshold voltage. However, traps have a direct and significant effect on threshold voltage. This increase in the threshold voltage also leads to reduction in the drain current with increasing trap states density. In addition, trap states also contribute to mobility degradation, on account of increased scattering. Thus, any realistic model should include the impact of the trap states on the threshold voltage and mobility. The output characteristics deviation from the long channel square law behavior specify the presence of the velocity saturation effect.

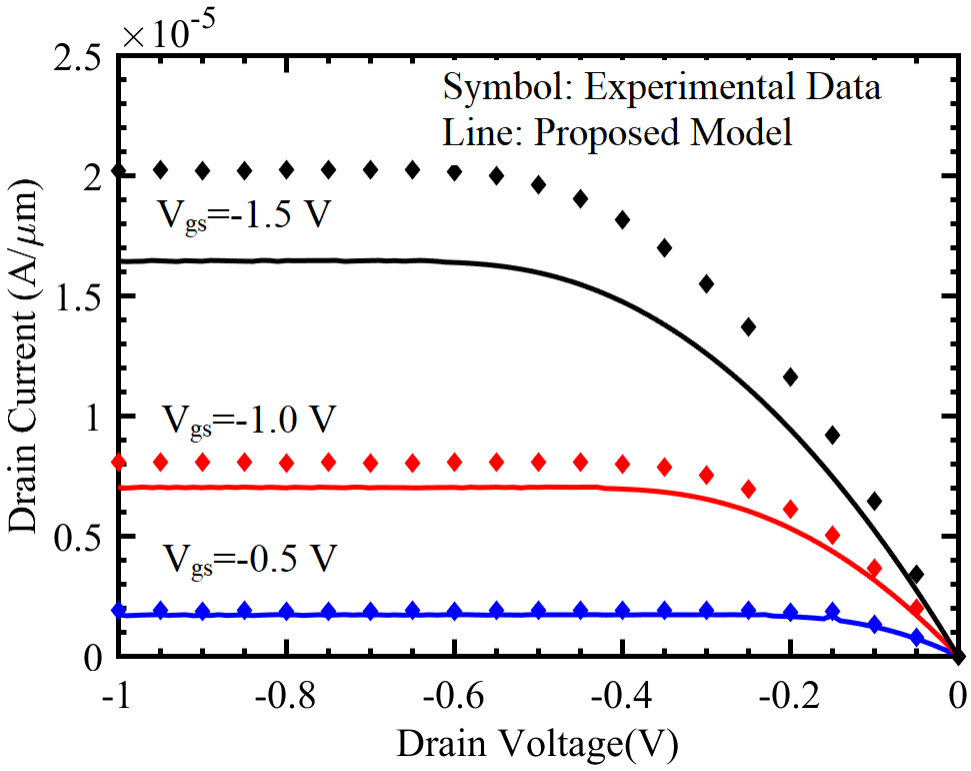

Figure 4.11: Drain current model behavior against the data of 6.2 μm long channel WSe_2 pFET experimental device reported by Sachid et al. Output characteristics for V_{gs}=-.5 V to -1.5 V.

The developed model for the p-type FET is validated against the experimental data of WSe_2-based long channel (L_g = 9.4 μm) top-gated pFET at Vbg = 0.0 V, as shown in Figure 4.11 [41]. The model efficiently captures the impact of the trap states on the threshold and in the drain current. The model also shows a good match for the output characteristics for the multiple values of the applied front gate voltage.

Chapter 5

Conclusion

This chapter summarizes the entire work and the limitations of our model. It also proposes some future developments that will help us evaluate the prospects of TMD channel MOSFETs in the post-Silicon era.

5.1 Summary

The compact analytical model developed in this work can play a significant role in ongoing research on 2-D TMD channel FETs. It will pave the way for a better understanding of these devices. Present models mostly concentrate on long channel devices and often include cumbersome numerical calculation. A complete analytical model that can specifically replicate the properties of short channel devices will definitely help the researchers. This urgency to have a robust, yet less complex model has motivated us in developing our model. We have first established a subthreshold model from the scale length equation. Since our model is primarily established on the concept of scale length, it is important to be able to calculate scale length with minimum room for error. This is why, we at first derived a cubic equation for scale length and later used that length in our subthreshold current equation.

We also deployed a new mathematical technique to calculate the integral of surface potential. This technique enables us to formulate a linear relation between channel length and the integral in the denominator of drift-diffusion equation in subthreshold. Previous models used numerical integration in this step.

Finally we derived an all-region model for drain current from surface potential. The results of our model are matched with reported experimental results. However, most experimental results are available for very long channel devices (L=1-20 μm). We have verified our model with results from reported long channel devices. For short channel devices numerically calculated results are used for the verification of our model. Our model properly predicts device performance for channel lengths as small as 10 nm. At a lower

length quantum mechanical effects play a prominent role and demands more careful handling.

5.2 Limitations and Possible Future Developments

- Our subthreshold model fails for channel length less than 10 nm. In those lengths, the plateu shape of the exponential of potential function does not hold anymore. Rather a Gaussian shape is formed that requires a different approach to have an analytical solution. Both these approaches can be merged together to develop a rigorous model in the subthreshold region.
- We have approximated a linear relation between mobile carrier density and potential, which simplifies the model in a great deal. But as a trade-off, the model fails to produce correct result in ultrashort length devices.
- The model can better predict device performance if nonidealities can be incorporated properly. Although we implemented trap models and velocity saturation models, both were modified from that of Si MOSFET. By developing proper mobility degradation models for 2D TMD channel devices, we can expect better agreement among the model and experimental results.
- The quasi Fermi level is assumed to be linear in the derived analytical model. For higher drain voltage assuming a parabolic quasi Fermi level with respect to the channel dimension can provide better estimation of charge carriers at those voltages, although the computational complexity will increase greatly in that case.
- This compact model can be further developed to make circuit models for 2D TMD devices. These models would facilitate EDA tools.

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