DESIGN OF NON-VOLATILE QUATERNARY MEMORY CELL USING MEMRISTOR-MOS HYBRID STRUCTURE

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MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by

Baishakhi Rani Biswas

Student No.: 1015062219

Department of Electrical and Electronic Engineering

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

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The thesis titled **"DESIGN OF NON-VOLATILE QUATERNARY MEMORY CELL USING MEMRISTOR-MOS HYBRID STRUCTURE"** submitted by Baishakhi Rani Biswas, Student No. P1015062219, session October, 2015, has been accepted as satisfactory in partial fulfillment of the requirement for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on September 29, 2018.

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DECLARATION

I hereby declare that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

Baishakhi Rani Biswas
September 2018

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At first I would like to thank the Almighty who enabled me to complete my thesis successfully and effectively.

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Finally it was a great opportunity for me to get introduced to memristor which is a very promising device and designing a memory system using memristors was really a great experience. I have tried my best to represent this thesis dissertation as appropriate as possible.

Baishakhi Rani Biswas

September, 2018

ABSTRACT

Memristor is a newly fabricated device which is becoming very popular among the researchers for its non-volatility, nanometer size and good switching behavior. In this work-memristor-MOS hybrid architecture based quaternary memory array design with complete read write technique has been developed. Each individual cell of the large memory array system contains only one memristor and a cell selection transistor and is able to store two bits of memory in the single cell. The proposed writing technique for this design is data erasing based which reduces circuit complexity by avoiding feedback read-based writing technique. The write circuit of the proposed design consists of a simple transmission gate and is common for the whole memory array. As a single cell stores two bits of data or in other words 4 different states (00, 01, 10, 11), the writing time is larger than conventional memory circuits. The read mechanism for this design is simple voltage division based and the read circuit has only a memristor and read enabling transistor. A complete 16×16 quaternary memory array with necessary peripheral read-write circuit has been simulated in LTSPICE for the verification of the proposed design. Further analysis has been done to prove that the proposed design shows superiority in terms of compactness, energy consumption, acceptable noise margin and simplicity in operation.

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1. INTRODUCTION

1.1 Introduction

In computing system, memory refers to the computer's hardware devices used to store information for computer. Typically computer data and machine code currently being used are stored in memory storages called RAM (Random Access Memory) which operates at a high speed regardless of the physical location of used data or code. RAMs are normally associated with volatile types of memory and usually of two types-SRAM and DRAM. Firstly, Dynamic random-access memory (DRAM) stores each bit of data in a separate tiny capacitor within an integrated circuit. DRAM requires periodic refreshments of data to prevent capacitor's charge leaking. Secondly, Static random access memory (SRAM or static RAM) is type of memory that uses bi-stable latching circuitry (Flip-flop) to store each bit. It doesn't require data refreshment but is volatile in the sense that the data is eventually lost when the circuit isn't powered. SRAM memory cell is comprised of 4 to 6 transistors unlike a DRAM memory cell, which is comprised of 1 transistor and 1 Capacitor. Though DRAM memory requires less area but SRAM is five times faster than the DRAM. Necessity of refreshing circuit is another disadvantage of DRAM. Apart from this two basic Random Access Memory, researchers have also developed some Non-volatile Random Access Memory (NVRAM) storages like Ferroelectric RAM (F-RAM), Magneto resistive RAM (MRAM), Flash memories etc. A newly found non-linear passive two terminal electric component known as memristor can also be used as an alternative to conventional memory devices like SRAM, DRAM and Flash memories. First theorized by Dr. Leon Chua in 1971 [1], memristor is a non-volatile and fast switching device which can not only be treated as a universal random access non-volatile memory (NVRAM), but also can perform in programmable analog ICs [2,3], basic arithmetic operations [4] and in modeling of neuromorphic and biological systems [5]. As the transistor-based CMOS memories scaling is approaching its physical limits in nanometer technologies, the hybrid CMOS/memristor structure is more reliable and practical for large scale memory. Apart from nanometer size, memristor based circuits are advantageous for low energy consumption and fast switching speed. Over the years many schemes [6-10] have been presented to use memristor as memory storing device where one cell contains one bit of data. The multi-valued memory achieved with memristors is a promising approach to enhance the memory density in simple structural designs. Effective and compact methods of reading and writing for multi-valued memories can significantly improve the performance of circuits. This thesis work focuses on developing a novel circuit structure for multivalued memristor-MOS hybrid architecture NVRAM to enhance the read/write speed, reduce power consumption and minimize area requirement.

1.2 Motivation of this Work

Neither DRAM nor SRAM have all the qualities to become fast, compact and cheaper memory system. Both of them are volatile and cannot retain data when power supply is lost. Use of flash memory may help us to a certain extent, but it has a limited number of read-write cycles it could sustain. This characteristic clearly is not suited for random access memory (RAM) because a huge number of read-write cycles occur on them regularly. Besides, flash memory consumes a great amount of power whereas DRAM and SRAM are low power devices. So to find an alternate way many researchers and scientist are working on NVRAMs like Fe-RAM, MRAM, PRAM etc. but neither of them was able to stay long. There was always a concern of dimension, speed and power consumption which left conventional volatile DRAM and SRAM technology a better choice. So there is a crucial need for inventing static memory system that will be as fast as SRAM, but will be non-volatile and less space demanding. If all these characteristics can be combined in a single memory design, then that memory will be perfectly suitable to be used as cache memory as well as flash memory for storing large amount of data. Hopefully researchers have found a new device called memristor which has opened new opportunities. In some memristor symposiums, it has been hypothesized that memristor in a crossbar structure can hold enormous amount of data in a small area. This device is very small, could be less than 10nm of length and can also be implemented with conventional CMOS technology which is called memristor-CMOS hybrid circuits. Again memristor-MOS hybrid structure based designs can further be used for storing multiple bits in a single cell. As multi-valued memory circuits have to deal with several memory states; so read-write techniques and noise margin are major design concerns there. Hence to obtain a practically implementable more efficient memory system, a multi-valued (quaternary) memristor based memory has been developed in this work along with the demonstration of complete peripheral circuits and read-write techniques.

1.3 Thesis Organization

This thesis describes the complete work with comparison to existing designs. The thesis paper has been organized in the following manner:

Chapter 2: Gives an idea of the memristor basics, existing memristor technology and the SPICE modeling of a memristor.

Chapter 3: Introduces different RAM circuits and memristor-MOS hybrid structure based memory designs. This chapter gives brief description to some recently proposed memristor based multi-valued memory schemes.

Chapter 4: A 16x16 memory array is designed with complete read write circuits where one cell consists of one memristor and a single transistor. The writing technique is data erasing based in proposed design and the read mechanism is simple voltage division based. All the simulation results have been shown to validate the designed memory array .

Chapter 5: In this chapter, an A/D converter is designed and simulated to convert the output voltage of the memory array into binary states.

Chapter 6: The performance of this circuit is discussed in terms of energy requirement, read-write time, area requirement, noise margin and the proposed scheme is compared to existing memory circuits.

Chapter 7: Summarizes the outcome of the proposed non-volatile memory array and discusses the future improvements or works to be done on this circuit.

2. INTRODUCTION TO MEMRISTOR

2.1 Memristor: A Memory Element

From the circuit point of view, there exists three basic circuit elements: A resistor (R), a capacitor (C) and an inductor (L). It is assumed that the real-world circuits can be modeled using only these elements with an ideal voltage source. The mentioned three basic two-terminal circuit elements are defined in terms of a relationship between two of the four fundamental circuit variables which are the current (i), the voltage (v), the charge (q) and the flux-linkage (Φ).The differential equations that characterize the basic elements provide three relationships out of the six possible relationships between the four fundamental elements.

$$Resistance, R = \frac{dv}{di} \qquad (2.1)$$

$$Capacitance, C = \frac{dq}{dv} \qquad (2.2)$$

$$Inductance, L = \frac{d\Phi}{di} \qquad (2.3)$$

The definition of current, i= $\frac{dq}{dt}$ and the Lenz's law, v =$\frac{d\Phi}{dt}$, give two more relations between the four constituents. These five relations are shown in Figure 2.1. So the only relationship that is missing is the relationship between q(t) and φ(t).

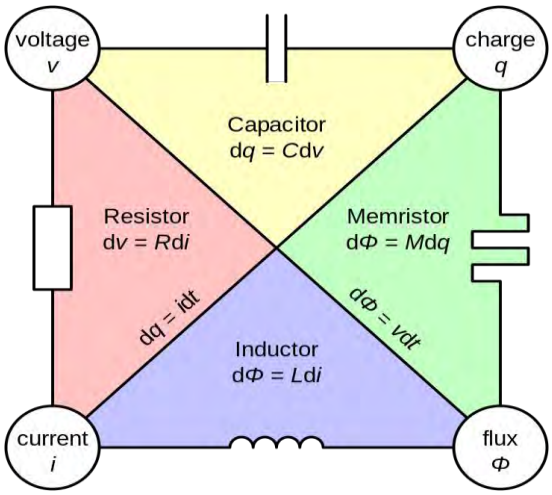


Figure 2.1: Relationships between the four fundamental circuit variables [1]

To find the missing case, Dr. Leon Chua postulated that a new ideal element defined by the single-valued relationship dφ = Mdq must exist to relate between q(t) and φ(t) [1]. He called this element memristor M, a short for memory-resistor. Thus a new two terminal basic circuit element was found apart from the three fundamental circuit elements. The memristance of the memristor is charge controlled (flux controlled) and the voltage across it is given by [1]:

$$v(t) = M(q(t)i(t)) \qquad (2.4)$$

$$M(q) = \frac{d\Phi(q)}{dq} \qquad (2.5)$$

Substituting the flux as the time integral of the voltage, and charge as the time integral of current, the more convenient forms are:

$$M(\big(q(t)\big) = \frac{d\Phi(q)/dt}{dq/dt} = \frac{V(t)}{I(t)} \qquad (2.6)$$

Thus M(q) has the unit of resistance, it is also called the incremental memristance. It can be inferred that memristance is charge-dependent resistance. The most significant feature of a memristor is its non-volatility: it retains its resistance after voltage across it is turned off. The memristor is static if no current is applied. If I(t) = 0, we find V(t) = 0 and M(t) is constant. This is the essence of the memory effect.

Though it was first postulated fifty years ago, only recently researchers have been able to fabricate practical memristor. This is due to the fact that memristance arises in nanoscale systems. HP labs first realized the memristor [11] which consisted of a thin film of thickness D (shown in Figure 2.2) with one layer of insulating TiO_2 and another layer of oxygen deficient TiO_{2-x} each sandwiched between platinum electrodes. The doped layer of TiO_{2-x} has significantly lower resistance compared to the undoped layer of TiO_2. Applying a voltage across a memristor causes the oxygen deficiencies in the TiO_{2-x} layer to migrate, and this changes the thickness of the oxygen deficient layer as well as the resistance of the memristor device.

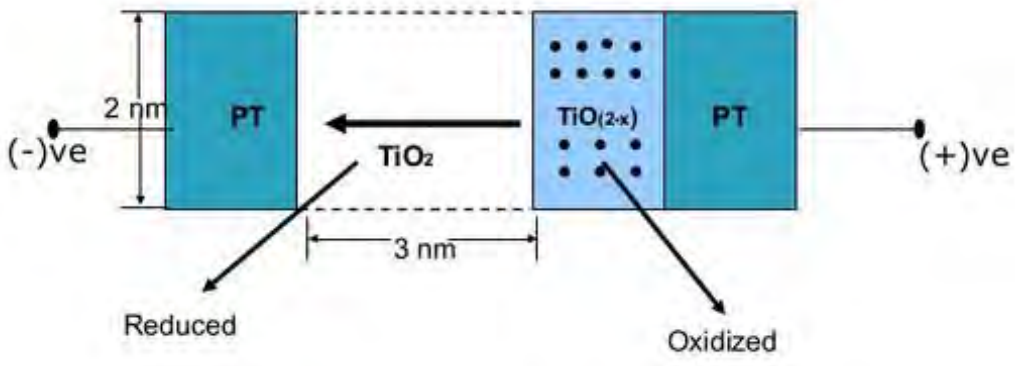


Figure 2.2: A single memristor [11]

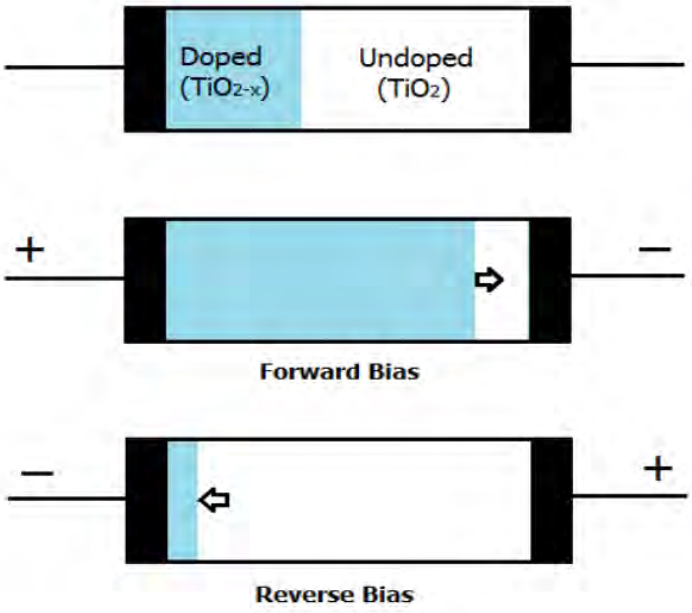


Figure 2.3: Function of a memristor [11]

The operation of the memristor has been shown in Figure 2.3. The resistance of the memristor depends on the amount of charge flown through it. The memristor is turned ON (resistance decreased) by channeling current through the memristor with a forward bias that displaces oxygen vacancies (major charge carrier) drifting them into bulk layer line-up to create a conducting channel with lower resistivity than the bulk layer. This will convert the high resistance bulk into low resistance. On the other hand, the memristor is turned OFF (resistance increased) by flowing current in the opposite direction with a reverse bias. The movement of oxygen vacancies in the opposite direction would cause disruption in the conduction channel converting the bulk layer again into a high resistance substance. Thus memristance can be altered between high and low by using alternate current direction, hence alternate voltage direction. Since the oxygen vacancies have a low mobility, they tend to stay in the same position after the voltage source is removed [11]. This phenomenon shows that the memristor can be used as non-volatile memory device where the resistance of a memristor is used to store information.

2.2 Memristor Modeling:

For memristor based circuits and Systems, it is very important to have a memristor model that can characterize the device properly. As we know, all electric devices can be modeled by basic ideal components. Researchers have also tried to describe memristor as combination of basic circuit components and derived Spice Model of memristor to be used in analysis of memristor based systems.

In 2008, HP Labs [11] published results for their previously mentioned Titanium based memristor device and modeled it according to equations (2.7) through (2.9). They considered the memristor device of thickness D and the thickness of the oxygen deficient titanium dioxide layer (TiO_{2-x}) defined a state variable w(t). They considered R_{OFF} and R_{ON} are the maximum and minimum possible resistances of the device respectively. Specifically, the region with high concentration of dopants (oxygen deficient titanium dioxide) having low resistance R_{ON}, and the remainder has a low dopant concentration and much higher resistance R_{OFF}. The memristance value will depend on the ratio between the state variable w(t) and the total thickness D.

$$V(t) = \left[R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right] I(t) \qquad (2.7)$$

$$v_D = \frac{dw}{dt} = \frac{\mu_D R_{ON}}{D} I(t) \qquad (2.8)$$

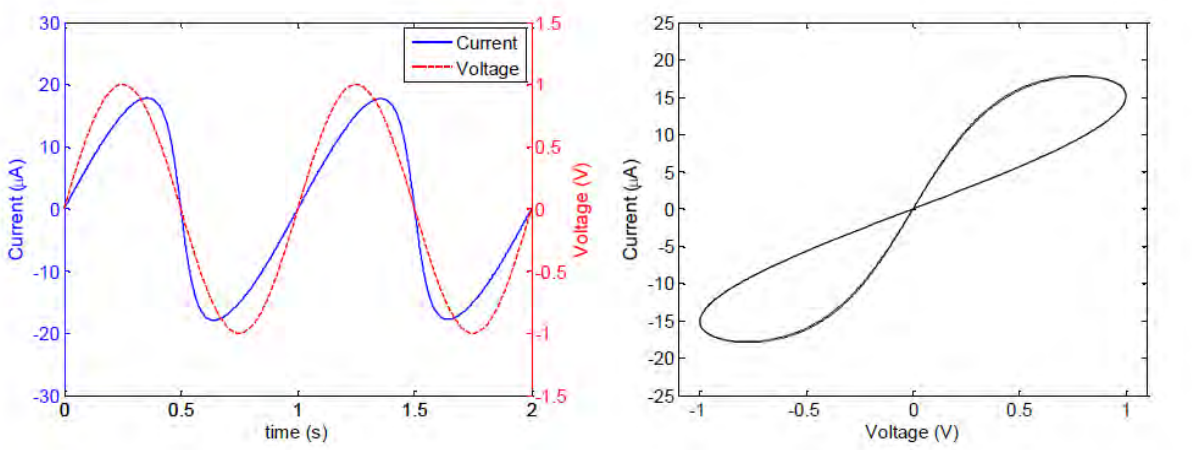
$$w(t) = \frac{\mu_D R_{ON}}{D} q(t) \qquad (2.9)$$

Here, V(t) is the applied voltage across the memristor and I(t) is the value of the memristor current. As the value of $w(t)$ increases, it can be seen that the overall device resistance lowers. Inserting (2.9) into (2.7), the memristance system can be characterized by:

$$M(q) = R_{OFF}\left(1 - \frac{\mu_D R_{ON}}{D^2}\right) q(t) \qquad (2.10)$$

For deriving equation (2.10), It has been assumed that $R_{OFF} >> R_{ON}$. The memristance property of a device is dependent on the factor $1/D^2$, and that's why the memristance property becomes significant in nanometer scale.

Figure 2.4 shows the simulation result for the model described by HP lab [11]. A simple sinusoid is applied to the memristor and the current-voltage wave shapes with respect to time have been shown in Fig 2.4(a). For a single voltage loop, the I-V curve of the memristor has been developed in MATLAB. The I-V curve displays a pinched hysteresis loop that is one of the significant characteristic of memristors. The hysteresis shows that the conductivity in a memristor is not only related to the voltage applied, but also to the previous value of the state variable $w(t)$. This hysteresis loop reflects the memory retaining property of the memristor.



(a) (b)

Figure 2.4: Simulation results for the HP Labs memristor with a sinusoidal input [11]. In this simulation: R_{ON}=10kΩ, R_{OFF}=100kΩ, μ_D=10^{-14} $m^2s^{-1}V^{-1}$, D=27nm, x_0=0.1D, and $V(t)$ = $\sin(2\pi t)$.

2.3 Memristor Spice Model

In the analysis of complex circuits having memristor requires reliable simulation tools that are easy to implement and efficient enough for predicting the output behavior of the total system. The SPICE (Simulation Program with Integrated Circuit Emphasis) environment is a general-purpose simulator that is used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior. Simulation using SPICE helps to model any device and also enables the model to be used in large systems and give an overview of the circuit characteristics that is close to the actual. So, before manufacturing an integrated circuit the best practice is to simulate it using SPICE simulators to verify its' operation. Till now a lot of modifications [12-15] to the initial memristor equations have been proposed and some SPICE models have also been developed for analyzing and simulating memristor based systems. In this work, a SPICE model of bipolar memristive system with threshold [16] has been used.

This model [16] was developed by Biolek et. el. and it provides a realistic description of bipolar memristive device by taking into account boundary values of memristance and threshold type switching behavior. In this model, the memristance is considered as an internal state variable defining device state x≡R and the memristance change when the absolute value of voltage across it is greater than a certain threshold voltage V_t. The device state can be defined by the following equations [16]:

$$I = x^{-1}V_M \qquad (2.11)$$

$$\frac{dx}{dt} = f(V_M)W(x, V_M) \qquad (2.12)$$

$$f(V_M) = \beta(V_M - 0.5(|V_M + V_t| - |V_M - V_t|) \qquad (2.13)$$

$$W(x, V_M) = \theta(V_M)\theta(R_{OFF} - x) + \theta(-V_M)\theta(x - R_{ON}) \qquad (2.14)$$

Here θ(.) is the step function and β is a positive constant characterizing the rate of memristance change when $V_M > V_t$ is the threshold voltage, and R_{ON} and R_{OFF} are limiting values of the memristance. The role of the θ(.) function is to limit the memristance value between the boundaries. The sketch of the function f(V_M) is shown in Figure 2.5 and this helps to understand the voltage threshold effect [16].

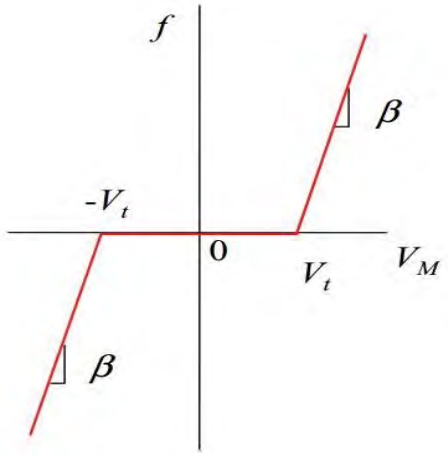


Figure 2.5: Sketch of the function f(V_M) modeling the voltage threshold property [16].

Based on above equations, Biolek et. el. developed a SPICE model which is presented in Figure 2.6.

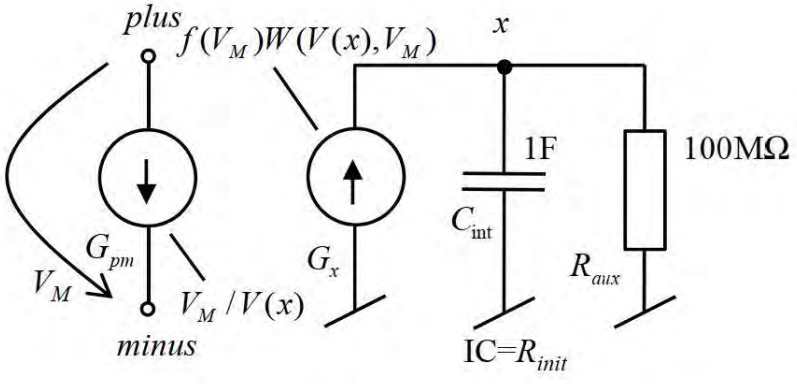


Figure 2.6: SPICE model of the memristive device with threshold [16].

In this SPICE model, the derivative of the memristance(x) according to Eq. 2.12 is modeled by the current of the voltage controlled source G_x, and its integral or the memristance (in ohms) is equal to the voltage of the node x(in volts). According to Eq. 2.11, the memristive port is modeled by the current source G_{pm}. Its current is computed as a ratio of the terminal voltage and the memristance. Eq. 2.13 and 2.14 contain discontinuous function (step) and function with discontinuous derivatives (absolute value). It can be a source of serious convergence problems, especially for applications utilizing large-scale models. To avoid this convergence problem, Biolek et. el. [16] proposed smoothed function on sigmoid modeling of the step function according to the formula:

$$\theta_s(x) = \frac{1}{1+e^{-x/b}} \qquad (2.15)$$

where b is a smoothing parameter and the smoothed function of the absolute value function can be expressed by [16]:

$$abs_s(x) = x([(x) - \theta_s(-x)] \qquad (2.16)$$

By adjusting the b parameter, a proper tradeoff between the accuracy and reliability can be found when a convergence problem appears.
According to these equations a SPICE code was developed [16].

```
**** Bipolar memristive system with threshold R2 ****
*D. Biolek, M. Di Ventra, Y. V. Pershin*
*Reliable SPICE Simulations of Memristors, Memcapacitors and Meminductors, 2013*
*Code for PSpice and LTspice; tested with Cadence PSpice v. 16.3 and LTspice v. 4*
**********************************************************************
.subcktmemR_TH plus minus PARAMS:
+ Ron=1K Roff=25K Rinit=5K beta=1E13 Vt=1.5
*model of memristive port
Gpm plus minus value={V(plus,minus)/V(x)}
*end of the model of memristive port
*integrator model
Gx 0 x value={fs(V(plus,minus),b1)*ws(v(x),V(plus,minus),b1,b2)*1p}
Raux x 0 1T
Cx x 0 1p IC={Rinit}
*smoothed functions
.param b1=10u b2=10u
.funcstps(x,b)={1/(1+exp(-x/b))}
.funcabss(x,b)={x*(stps(x,b)-stps(-x,b))}
.func fs(v,b)={beta*(v-0.5*(abss(v+Vt,b)-abss(v-Vt,b)))}
.func ws(x,v,b1,b2)={stps(v,b1)*stps(1-x/Roff,b2)+stps(-v,b1)*stps(x/Ron-1,b2)}
.ends memR_TH
```

To analyze the characteristics of this model, a memristor using SPICE model of bipolar memristive system with threshold was simulated by a simple voltage source according to Figure 2.7.

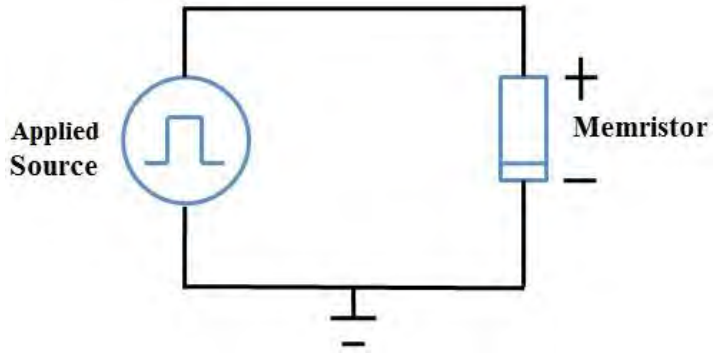


Figure 2.7: A memristor device driven by a voltage source

The response of the memristor for a sinusoidal voltage and the corresponding I-V curve is shown in Figure 2.8 and 2.9 respectively.

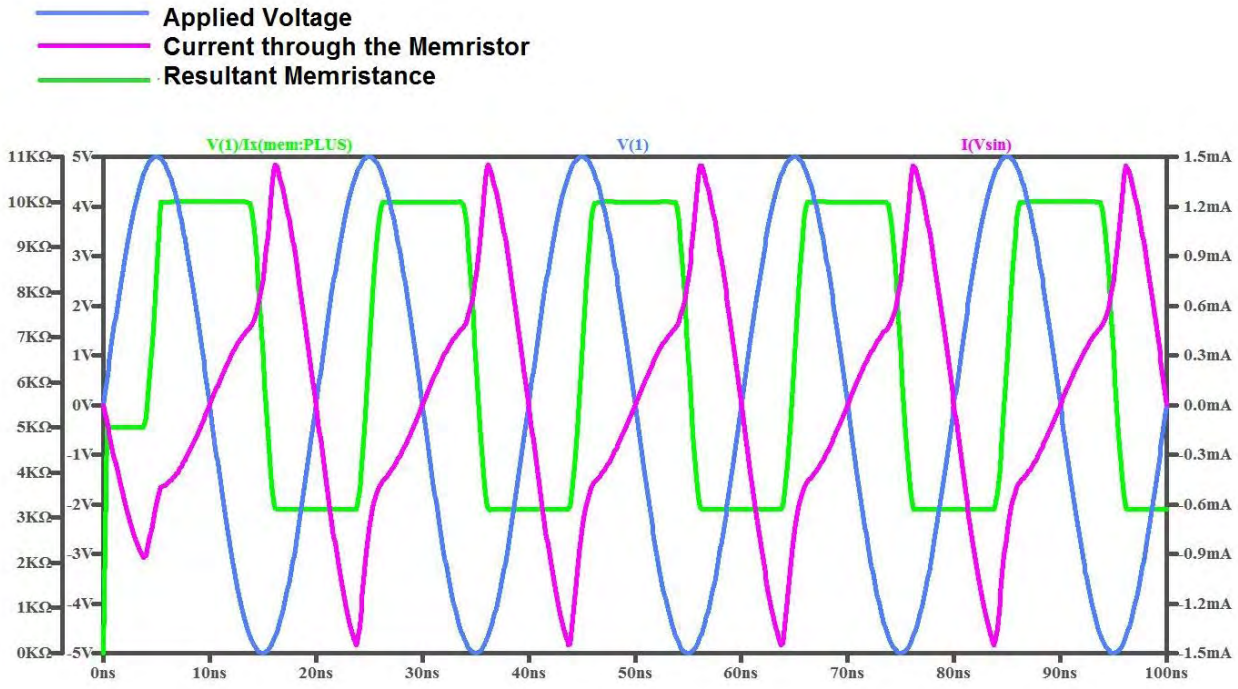


Figure 2.8: Simulation result for a memristor device having R_{ON}=1KΩ, R_{OFF}=10KΩ, β=10^{13} and threshold voltage of 4.6 V driven by a sinusoidal voltage source.

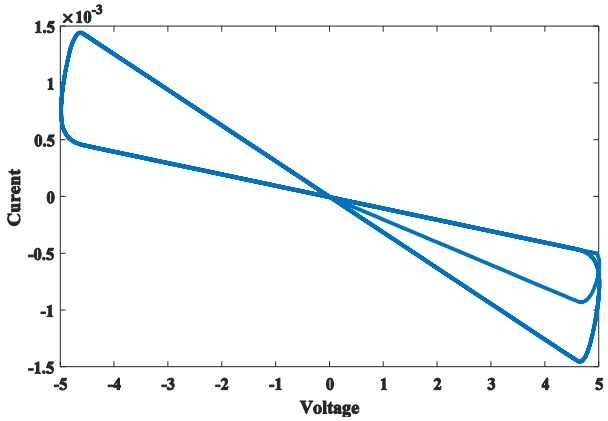


Figure 2.9: I-V curve of the memristor described in Figure 2.8

The memristor SPICE model used in this thesis work, have the parameters R_{ON}=1KΩ, R_{OFF}=25KΩ, β=10^{13} and threshold voltage of 1.5V. To further investigate, the voltage threshold property of this model, the memristor device driven by a pulse voltage source has been simulated in LTSPICE and the simulation result is shown in Figure 2.10.

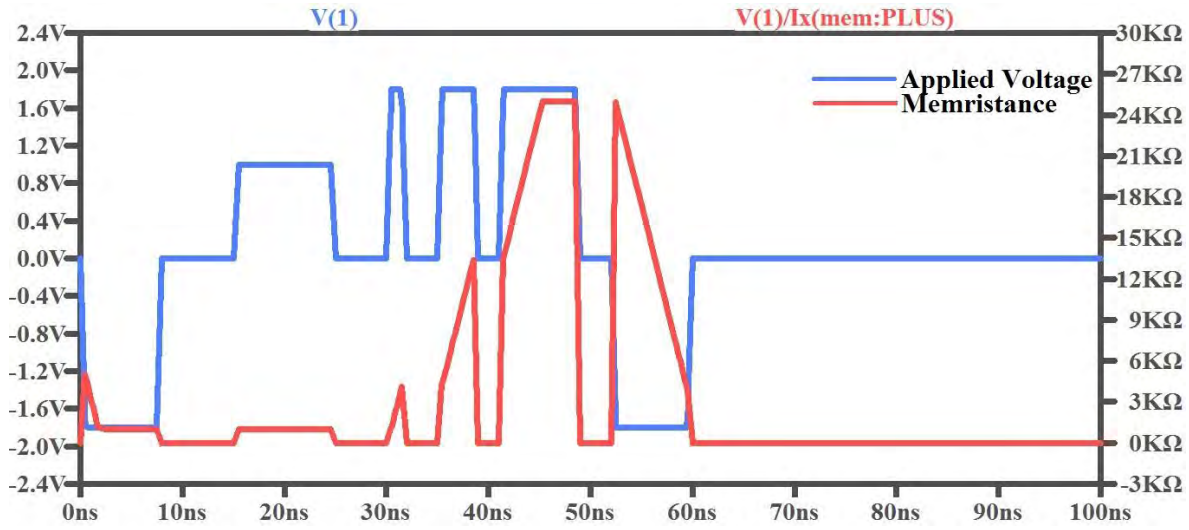


Figure 2.10: Simulation result for a memristor device having R_{ON}=1KΩ, R_{OFF}=25KΩ, β=10^{13} and threshold voltage of 1.5V driven by a pulse voltage source.

It is observed from the output waveforms that when a forward voltage is applied, the memristance increases only when the value of applied voltage is greater than threshold voltage. If the memristance reaches boundary value R_{OFF}, the memristance becomes fixed and doesn't change after applying more voltage. The value of the memristance depends on the previous states also. The most significant thing to observe from the simulation is that the memristance doesn't change when the voltage source is turned off or in other words the memristor can retain its previous memristance. Similarly, in the reverse bias condition, the memristance decreases if the value of applied voltage is greater than threshold.

3. MEMORY CELL BASIC

Memory cells are integral part of computing system for storing data and program instructions. A major portion of the silicon area of existing digital designs is dedicated to memory cells. More than half of the transistors in today's high-performance microprocessors are devoted to cache memories and this ratio is expected to further increase.

3.1 Types of Memory Cell

Memory cells are of different types and formats. Each of them have certain advantages and disadvantages over one another. The type of memory that is preferable for a given application is dependent on the required memory size, the time it takes to access the stored data, access patterns, required energy and the system requirement. Depending on the way of data access, the classification of memory cells is given in the following chart:

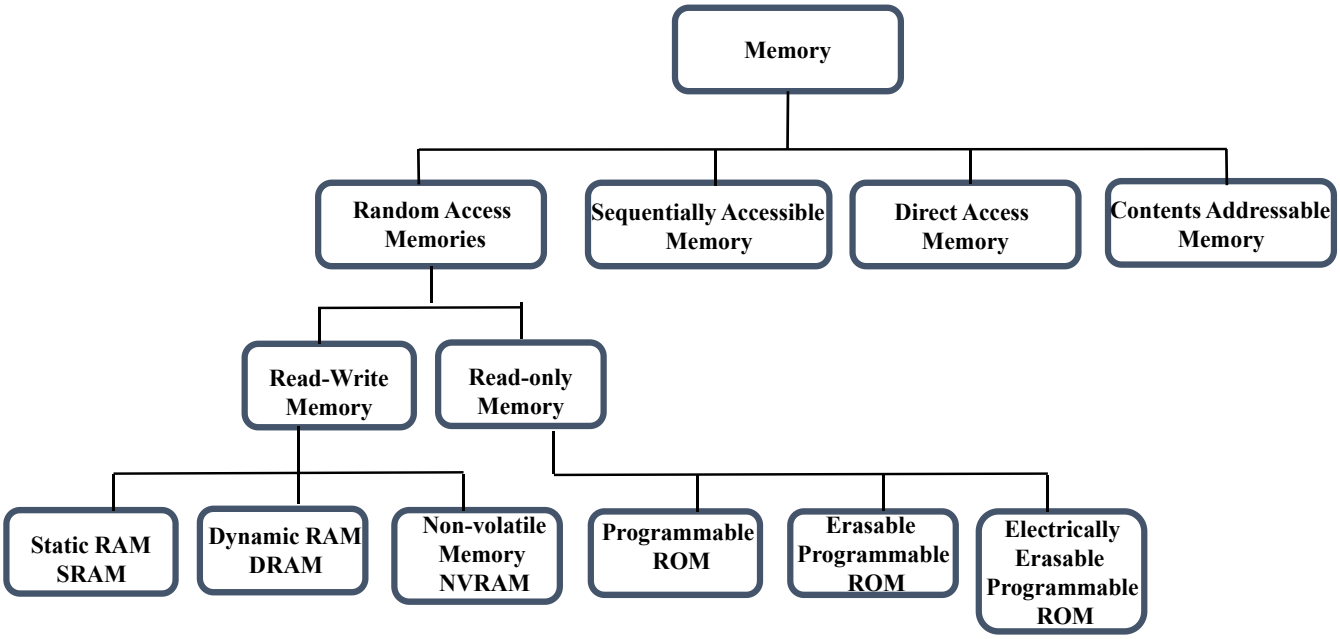


Figure 3.1: Classification of Memory Cells

This thesis work aims at designing a non-volatile memory (NVRAM) that is basically a random access type read-write memory. For random access memories, the access time to any piece of data is independent to the physical location of the data. NVRAM is used as the replacement for other read-write memories like SRAM and DRAM. So it is necessary to learn about different types of random access read-write memories and their advantages and disadvantages.

3.2 SRAM

SRAM is a one bit memory cell that uses bi-stable latches for data storage and there is no need for periodically refresh memory contents. In Figure 3.2, a conventional SRAM cell is shown where a single cell consists of six transistors. Each bit in an SRAM is stored on four transistors (M1, M2, M3 and M4) that form two cross-coupled inverters. Two additional access transistors serve to control the access to a storage cell during read and write operations. SRAM is commonly used in cache memory of the computing system.

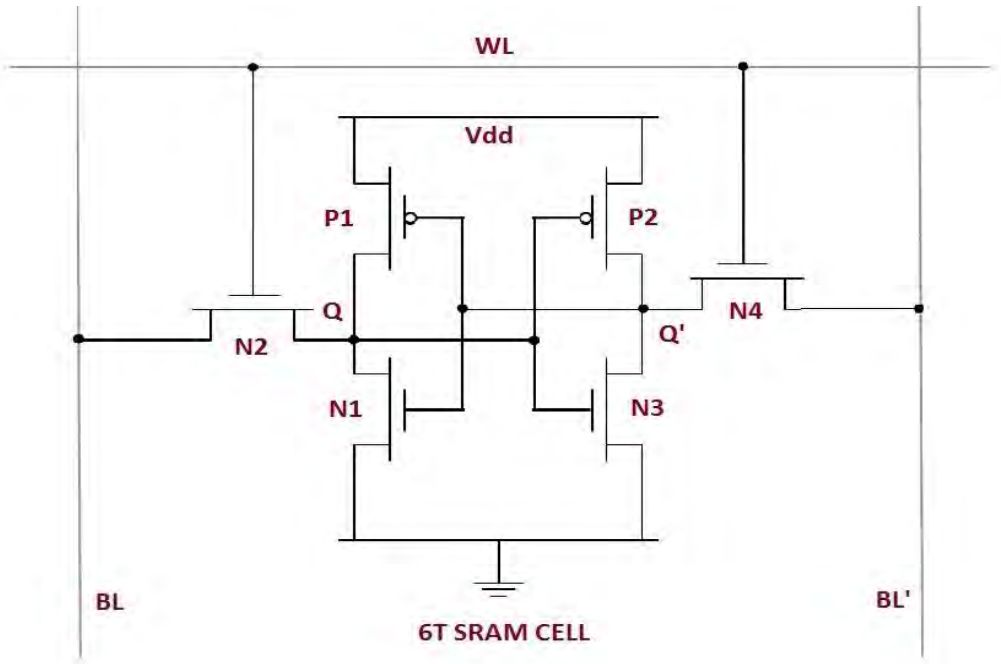


Figure 3.2: A conventional 6T SRAM cell

Advantages:

1. The operation of SRAM is very fast and noise immune.
2. SRAM circuits are less power hungry as standby current is minimum
3. Periodic data refreshment is not needed

Disadvantages:

1. SRAM cell size is large (six transistors per cell) and so it's expensive.
2. The data in the SRAM cell is lost in absence of power supply.

3.3 DRAM

Each one-bit memory cell uses a capacitor for data storage. Since capacitors leak, there is a need to refresh the contents of memory periodically. In modern computer and graphics card DRAM is used as the main memory. Figure 3.3 shows a basic DRAM cell. During both read and write operation of the cell, the transistor is needed to be enabled by providing high voltage on the line SEL. The bit of data desired to be written is given at the IN/OUT line. During reading of the data, the output data is available on the same line.

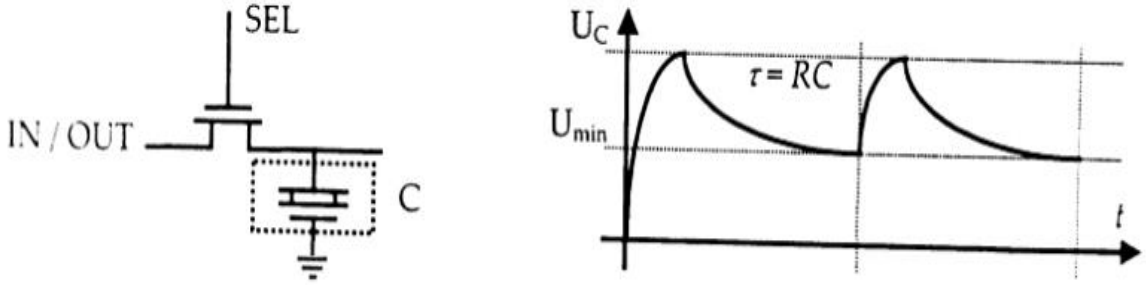


Figure 3.3: A conventional DRAM cell

Advantages:

1. DRAM cell is less expensive that SRAM.
2. The area requirement for DRAM is very low as the transistors and capacitors used are extremely small; billions can fit on a single memory chip.

Disadvantages:

1. Periodic data refreshment required
2. DRAM is slower in operation
3. The data in the DRAM cell also vanishes in absence of power supply.
4. Due to the dynamic nature of its memory cells, DRAM consumes relatively large amounts of power, with different ways for managing the power consumption.

3.4 NVRAM

Non-volatile random access memories retain their data information even after the power supply is lost. Presently the most known NVRAM is flash memory. The major drawback of flash memory is that it requires to be written in larger blocks than many computer can automatically address. Flash memory has limited longevity and performance limitations in matching response time. As such researchers are trying to find new technologies to replace flash memories and offer the performance of SRAM with the non-volatility of flash. Some recent approaches of NVRAM are listed below:

1. Ferroelectric RAM (FeRAM)
2. Magneto resistive RAM (MRAM)
3. Phase-change RAM (PRAM)
4. Millipede memory
5. Nano-RAM based carbon nanotube memory
6. Silicon-oxide-nitride-oxide silicon (SONOS) memory
7. Memristor based non-volatile memories

As this work is based on memristor based non-volatile memory, some previous works in this field will be discussed in this section. A lot of single bit storing memristor memories has been proposed till now. Sakode et. el. [17] proposed a novel 1 transistor based memory cell.

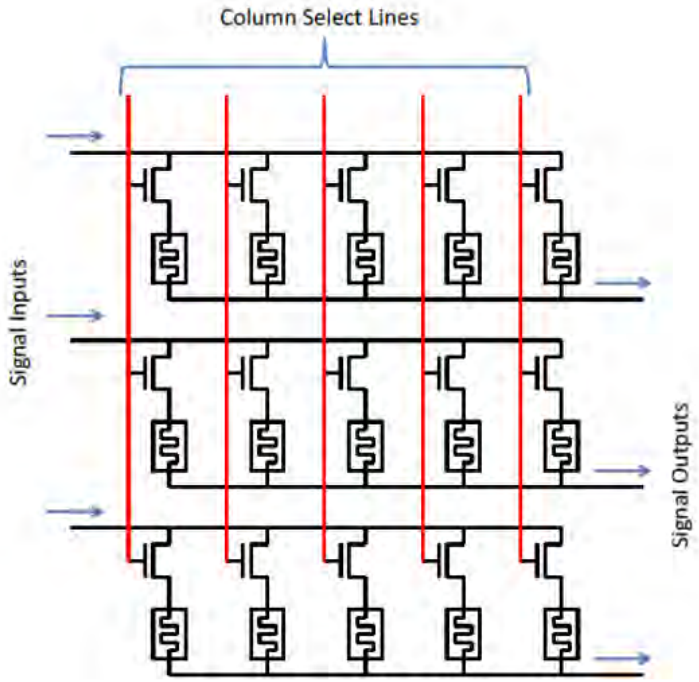
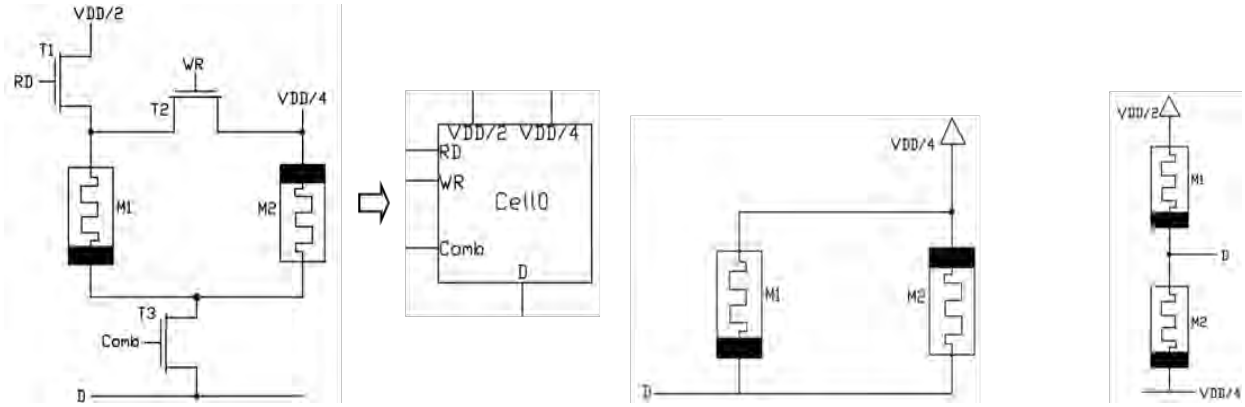


Figure 3.4: 1 transistor 1 memristor based memory cell [17]

This work can be extended for multivalued logic and this theis work not only uses this basic structure but also clearly describes the operation of the whole circuit with other peripheral circuits needed. Among other topologies, a 3T-2M SRAM [18] is mentionable.



(a) (b) (c)

Figure 3.5: A 3T-2M memory cell [18]

For this cell, two memristors are used as memory element. The arrangement is in such a way that during write cycle, they are connected in parallel but in opposite polarity [Figure 3.5 (b)] and during read cycle, they are connected in series [Figure 3.5 (c)]. These connections are established by two NMOS pass transistors T1 and T2. A third transistor T3 is used to isolate a cell from other cells of the memory array during read and write operations.

Some multivalued memristor based logic circuits has also been proposed [19-22]. Rabbani et. el. [21] proposed a complete circuitry (shown in Figure 3.6) where a single memristor device can be used to save multilevel (ternary here) data as the storage element in Resistive (ReRAM).

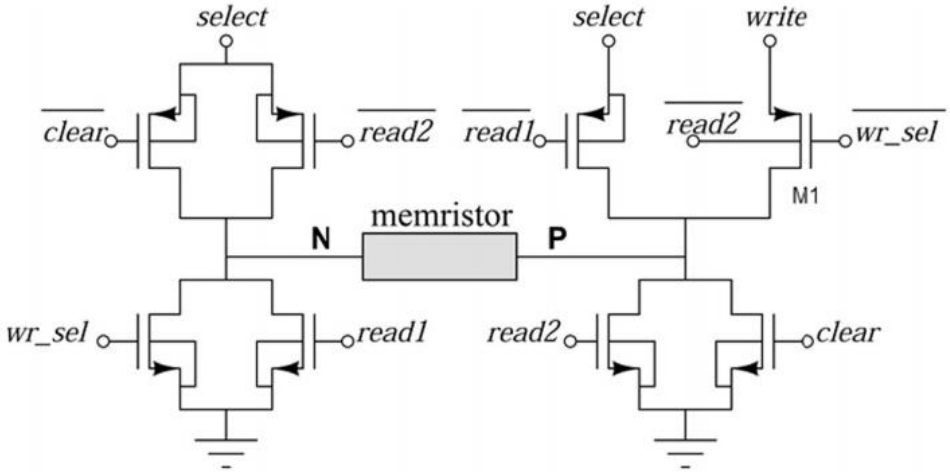


Figure 3.6: Memristor based multilevel circuit proposed by Rabbani et. el. [19]

4. MEMRISTOR BASED QUATERNARY MEMORY CELL

Memristor based circuit can be considered as an alternative SRAM memory cell as they don't need periodic refreshment of data and have the added advantage of retaining data after the power supply is lost. In memristor based NVRAM circuits, power supply is only needed during the writing and reading operation of the memory cell. In this chapter, the proposed memristor-MOS hybrid architecture quaternary memory cell has been discussed with complete peripheral circuit. The writing technique of this memory cell is data erasing based and reading technique is voltage division based. A basic cell uses one memristor and a single transistor. The proposed operation methodology enables the cell to store two bits of data in a single cell and that's why the proposed cell is called a quaternary memory cell. No feedback operation is used for this proposed design. This topology makes the circuit design very compact and simple.

4.1 Basic Quaternary Memory System Design

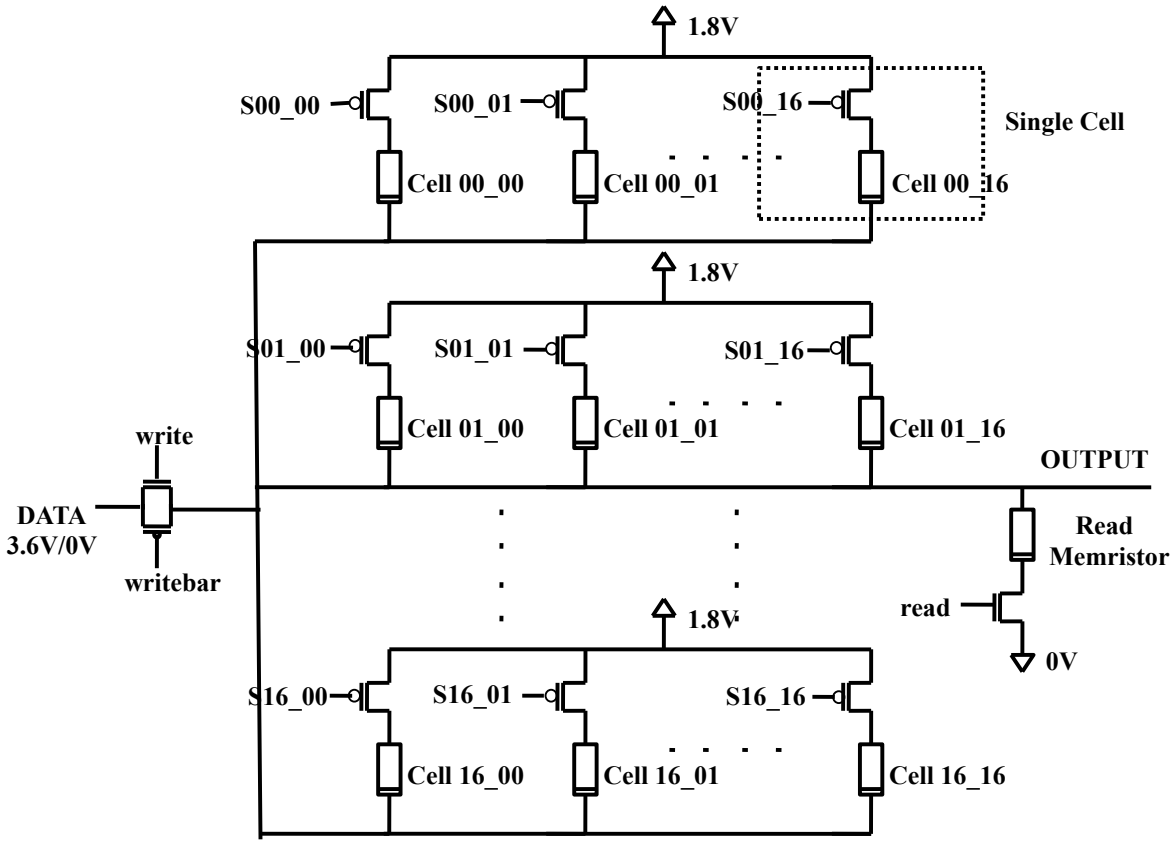


Figure 4.1: Proposed memristor based quaternary memory system

A basic cell used in this work comprises of a single memristor and a transistor used to select that cell memristor. For simulating the memory system, SPICE model of memristor proposed by Biolek. et. el. [16] is used and the ON Resistance, OFF Resistance and the threshold voltage are taken 1kΩ, 25KΩ and 1.5V respectively. Figure 4.1 shows a complete 16×16 quaternary memristor based memory array system. The write circuit is common to the whole memory array. Current can be flowed in both direction of the memory cell depending on the applied voltage. The data erasing technique based writing system can be implemented only by a transmission gate in the writing circuit. Two different type of voltages (reason is explained in the next section) is passed during the writing cycle and all the voltage are unidirectional for this design. As the memory cell stores two bits of data, the cell actually have to save four different combinations (00, 01, 10, and 11) of these two bits. The operation methodology for writing this four different state is very crucial in this design as there must be significant difference in any characteristics between the states by which the stored data can be detected. The read circuit is also common for the whole memory array and the reading technique is simple voltage division based. In the reading circuitry part, a single memristor does the whole work. There is a transistor in this part which is selected during reading a particular memory cell. Another important design consideration is noise margin between the states during reading and it must have a large enough value for practical data detection. The read memristor actually works as a fixed Resistor and the memristance of both the cell memristor and read memristor shouldn't change during the read operation to avoid data refreshing after reading.

To clearly investigate the operation of the proposed design at first consider a single cell is connected to the write and read circuit as shown in Figure 4.2 and the read-write technique is described in the next sections.

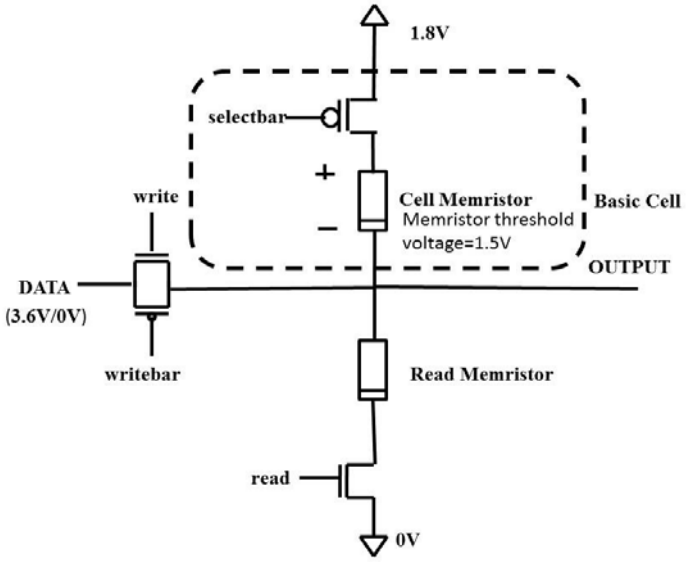


Figure 4.2: A single memristor cell with peripheral circuit

4.2 Write Methodology

As the quaternary memory Cell has to store four different states (00, 01, 10, 11), the write operation is comparatively complex and lengthy for this memory circuit. At the beginning of each write cycle, the particular cell is selected by enabling the transistor of that cell and the cell memristor is turned completely on by passing the DATA value of 3.6V for 9ns. This causes current flow in the opposite direction of the memristor and the memristance decreases to its lowest value (1kΩ). After that, the DATA value of 0V is passed for different time durations (depends on the type of the state to be written in the cell) causing the current flow in forward direction and the resistance of memristor will rise depending on the mentioned time duration. The methods to write four different states in a particular cell of the array is demonstrated below and the circuit operation for writing a sample State 01 has been shown in Figure 4.3. The circuit operation for other states is almost same except for the pass time of 0V.

4.2.1 Write 00

To write the state 00, 3.6V is applied as the DATA value for 9ns by enabling the transistor of a particular cell. A negative voltage of 1.8V appears at the memristor causing current flow in backward direction. As the applied voltage is greater than the threshold voltage, the memristance becomes 999.86Ω which is named ground state in this thesis work. This 9ns pulse actually works as a data erasing period for the cell. No forward current is flown through the cell memristor during writing 00.

4.2.2 Write 01

To write the state 01, 3.6V is applied as the DATA value for 9ns and after that 0V DATA is passed for 2ns. The first pulse forces the memristor to ground state and the second pulse causes current flow in forward direction which increases the resistance value to 4.315 KΩ.

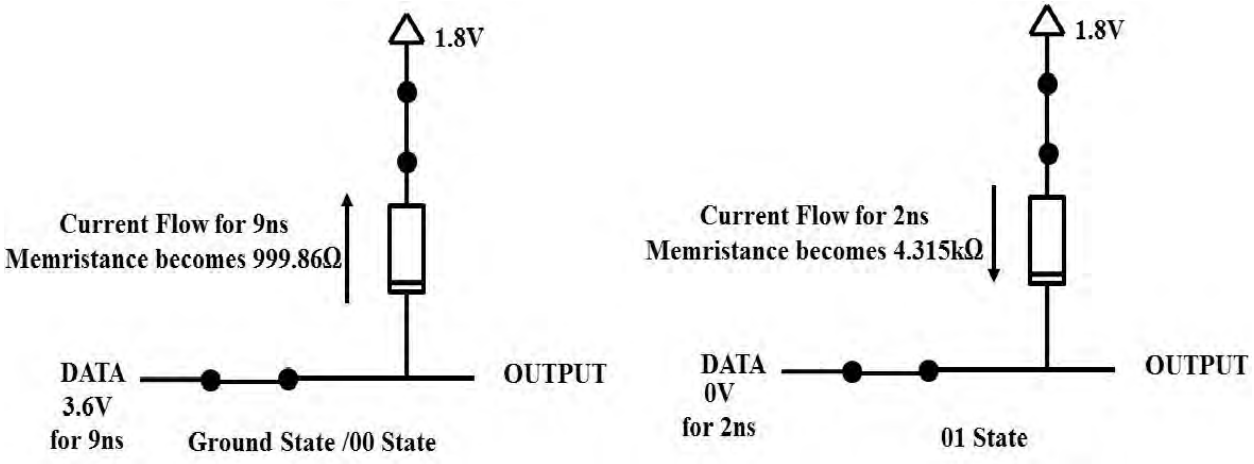


Figure 4.3: Writing Scheme for the State 01

4.2.3 Write 10

For this state, 3.6V is applied as usual for data erasing and then 0V is applied for 4ns. After the operation, the memristance becomes 10.017 KΩ.

4.2.4 Write 11

In this case, 3.6V is applied as the DATA value for 9ns followed by a 0V for 8ns. The resistance value becomes 21.663 KΩ when 11 is written in the cell.

A flowchart showing the writing methodology for all the four states has been shown in Figure 4.4. Thus after four different writing techniques, the memristances are significantly different in each state. Forcing the memristor to ground state is necessary in every write cycle because the cell needs to be erased before writing a new value in it. The maximum memristance value that the cell may require to erase is 21.663 KΩ. That's why a long pulse of 9ns is applied during erasing the memory of a cell. By following this approach proposed in this thesis work, feedback reading operation before writing can be avoided and the circuit design becomes very simple and compact.

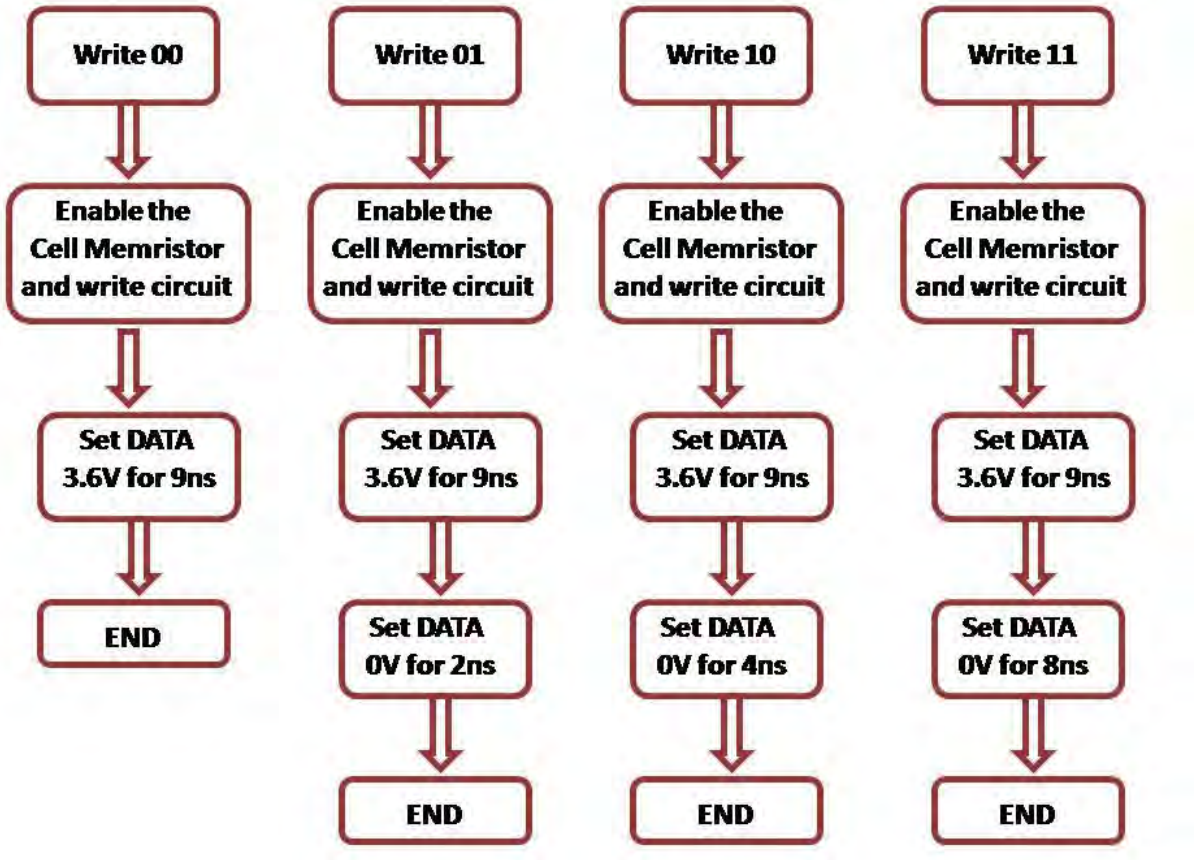


Figure 4.4: Flowchart for all the writing states of proposed quaternary memory cell

4.3 Read Methodology

The read operation for the quaternary memory cell is very simple and fast. In this case, the DATA line is disabled and the read transistor is selected. The cell required to be read is selected by enabling the cell transistor. The memristor used in the read circuit has a large threshold voltage which actually behaves like a fixed resistor. The memristance value of the read circuit has been chosen as 10 KΩ and it will not change after several read operations as the applied voltage through it is less than its threshold. The read cycle takes only **3 ns** and the circuit works on simple voltage division law. During reading, the voltage that appears at the cell memristor is also lower than its threshold voltage. So, cell data isn't corrupted during reading and the memristance is retained after several read cycles. As the memristances were different for four different states (00, 01, 10, 11), so the read voltages at the OUTPUT node of the circuit will also be significantly different from each other. So, the state of the cell can be determined by these read voltages. If a 2 bit Analog to Digital converter is placed after the OUTPUT node, then the read voltage can also be converted into binary outputs. The circuit operation during reading is shown in Figure 4.5.

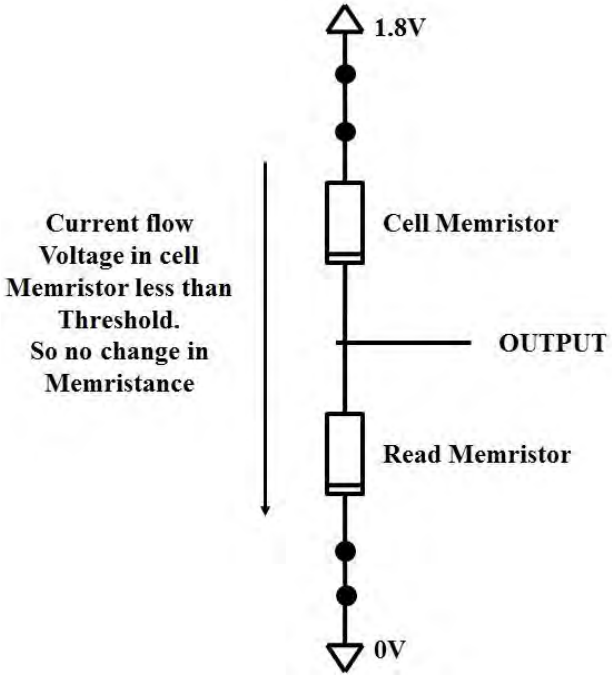


Figure 4.5: Circuit operation during reading in the proposed quaternary memory cell

4.4 Design Consideration: Generating the 3.6V Power Supply

For the proposed design in this thesis work, 3.6V is needed to be applied during the write cycle. This voltage is passed through only the transmission gate of the write cycle. For generating this voltage a switched capacitor dc-dc converter can be used [23]. The circuit design proposed in [23] can be configured for boost operation as shown in Figure 4.6.

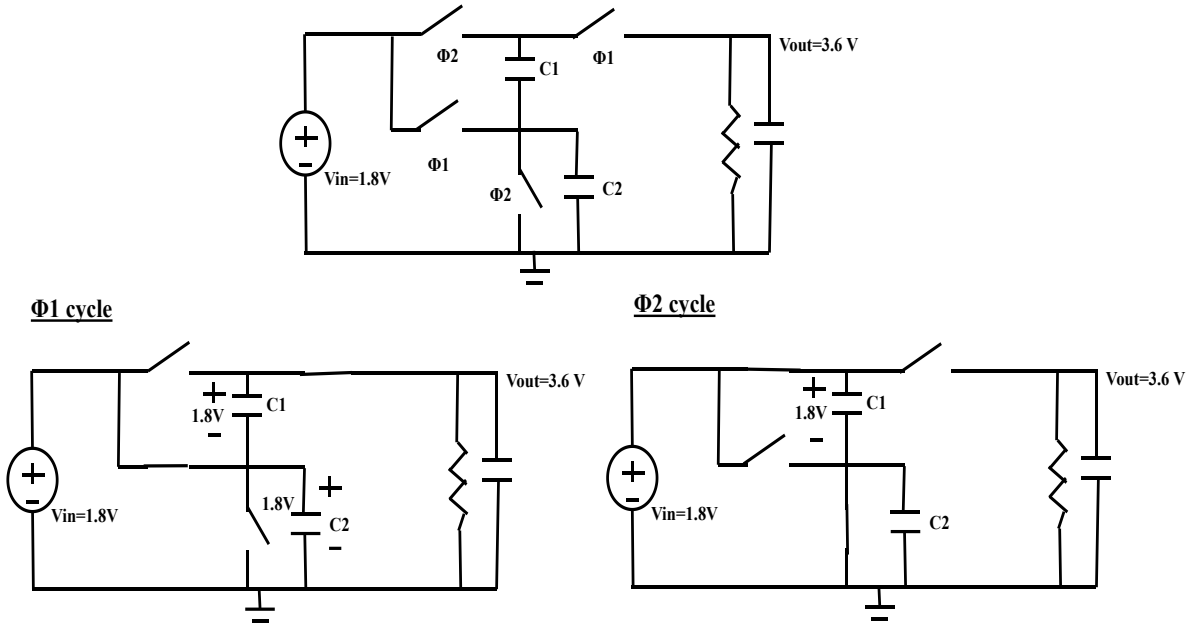


Figure 4.6: Circuit operation of switched converter based boost dc-dc converter

In the above circuit two fast clock cycles Φ1 and Φ2 are used each of 50% duty cycle. In Φ2 cycle, capacitor charges up to the input voltage 1.8V. In the next Φ1 cycle, the capacitor C2 charges up to 1.8V and both the capacitor voltages sums up to 3.6V and appears at the output. During Φ2 cycle, the output capacitor maintains the output voltage 3.6V (falls slightly) due to large capacitance value.

4.5 Simulation Results

A particular cell of the memory circuit is operated according to the mentioned read-write cycles. In Figure 4.7-4.10, the mentioned four different states are written in a cell. In each case, the cell is read during 21-23 ns when the OUTPUT line (shown in blue line) has different read voltages depending on the data written in the cell.

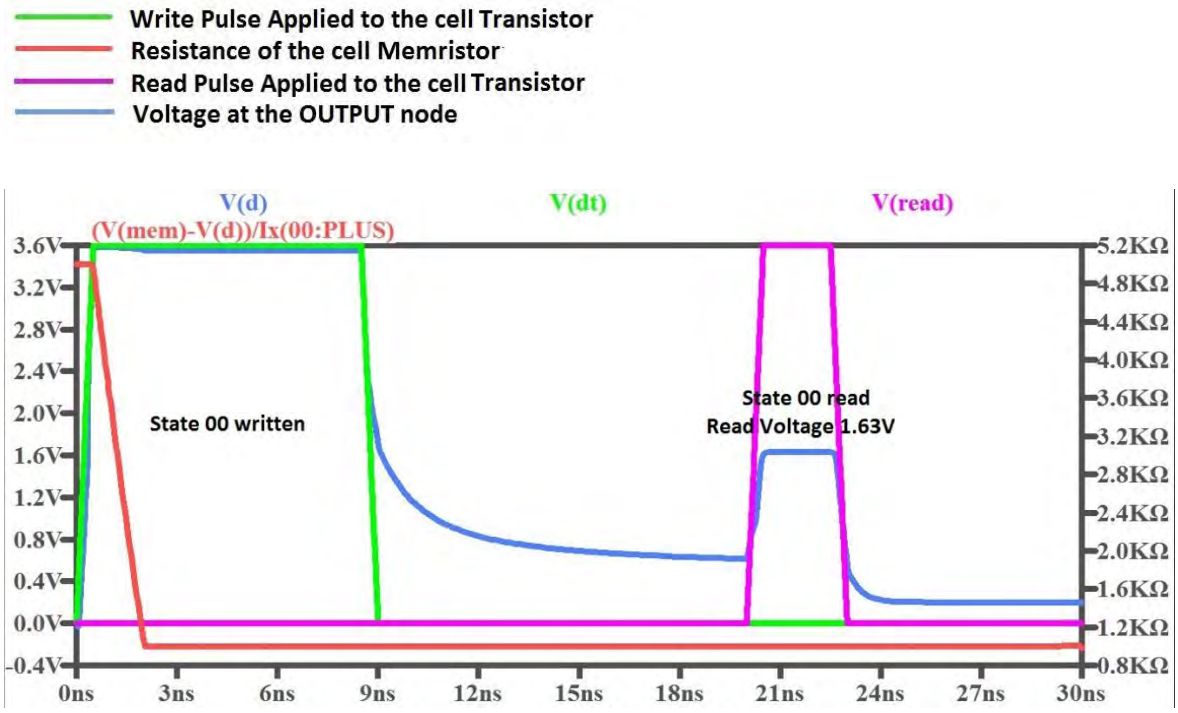


Figure 4.7: Read Write cycle and output wave forms during the state 00 in the cell

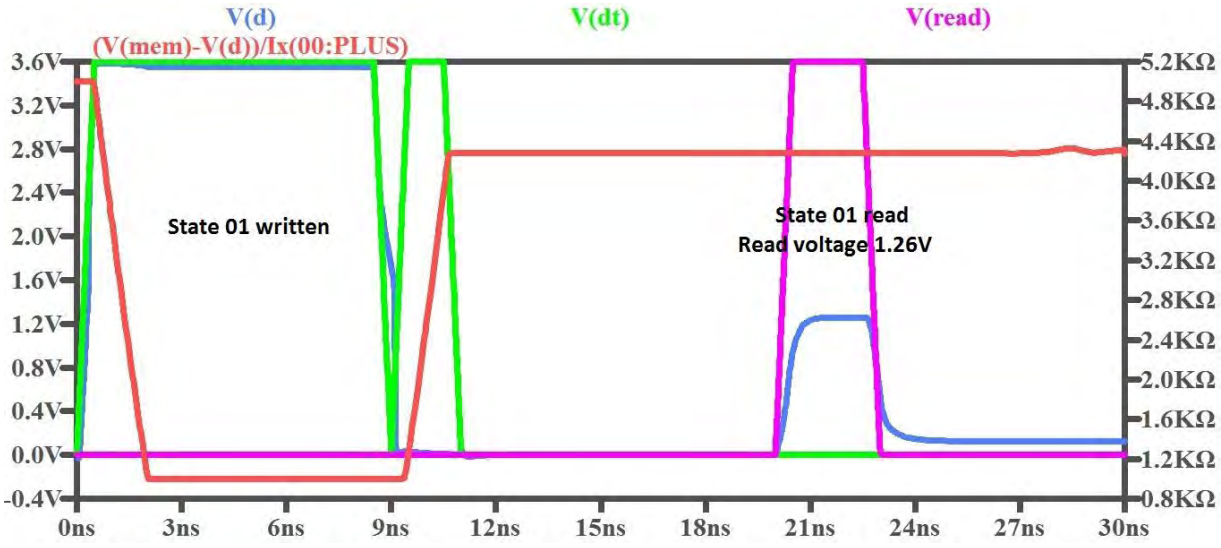


Figure 4.8: Read Write cycle and output wave forms during the state 01 in the cell

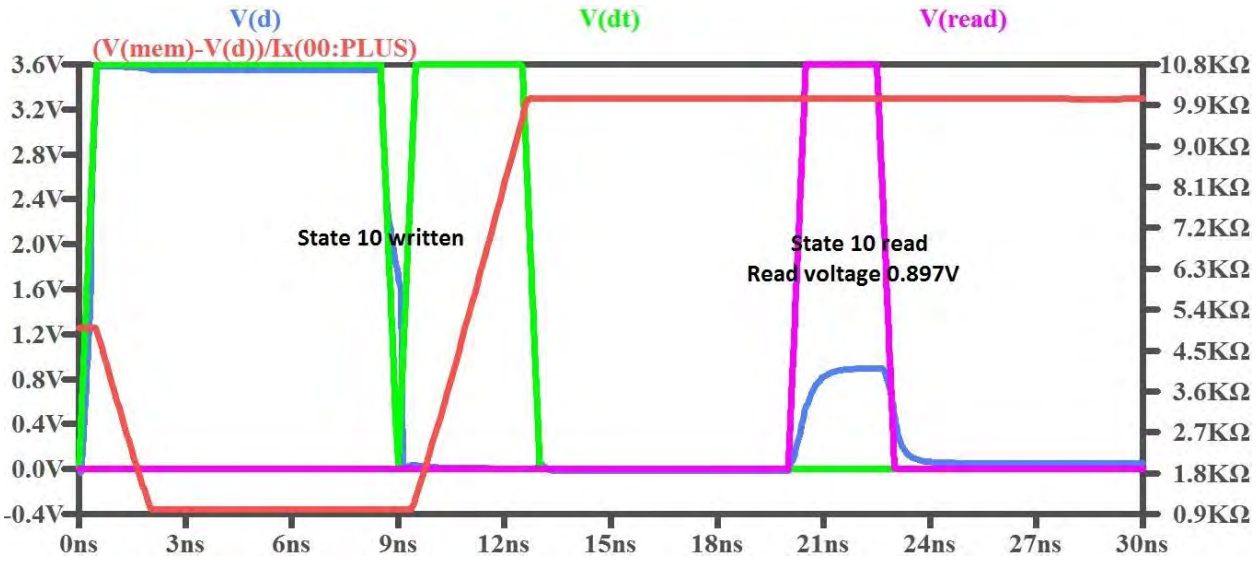


Figure 4.9: Read Write cycle and output wave forms during the state 10 in the cell

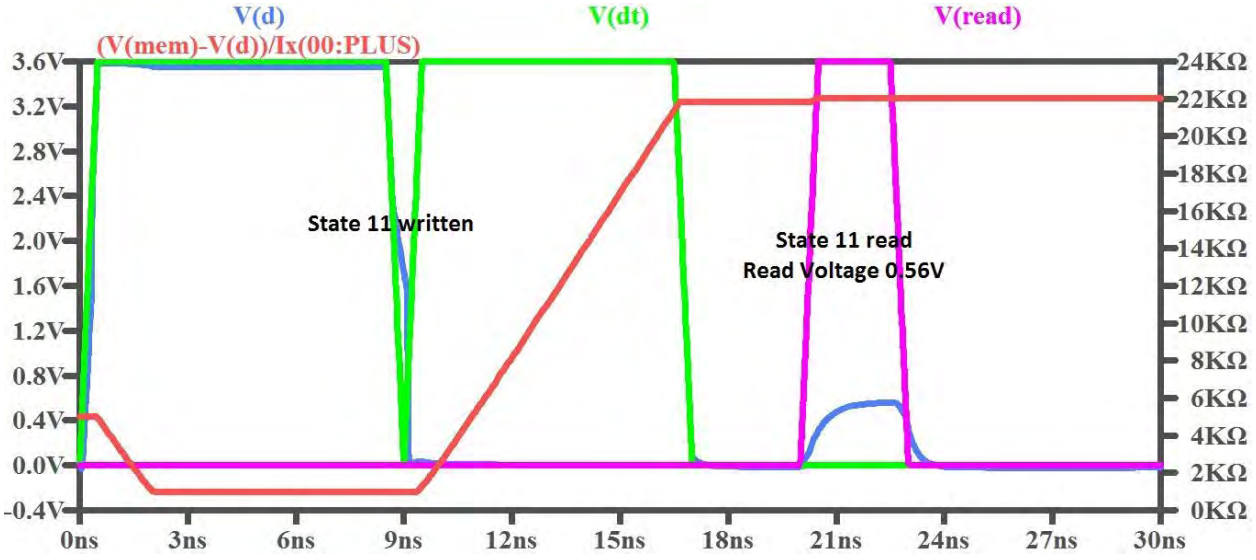


Figure 4.10: Read Write cycle and output wave forms during the state 11 in the cell

To further verify the operation of the design, 11 is written in a cell with mentioned writing technique and after that 00 is written in the same cell. For writing 00, the cell needs to erase its previous memristance that was 21.663 KΩ (maximum case). After applying 9ns pulse this memory is completely erased and the cell memristor comes to 00 state. Then the cell is read twice and the read voltages are got as expected. So the cell can successfully write any memory state in it regardless of its previous memory state and retains its memory after successive read operation. The simulation results have been shown in Figure 4.11 of this thesis work.

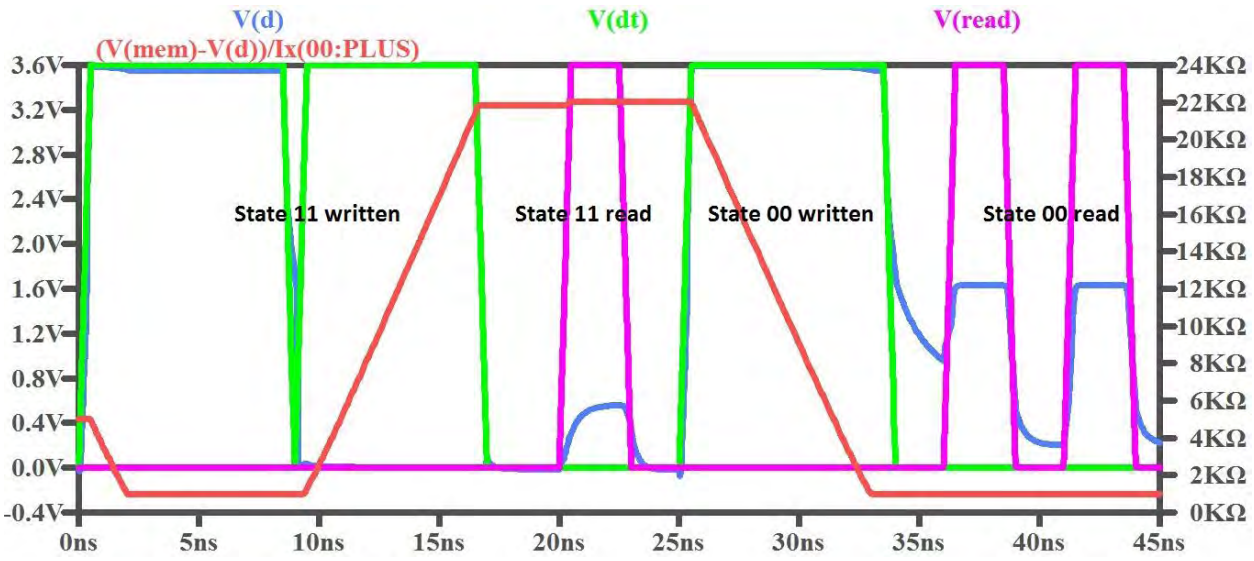


Figure 4.11: Read Write cycle and output wave forms during the state 11 followed by state 01

TABLE 4.1 summarizes the writing techniques for different memory states and output voltages after reading the corresponding states for the proposed quaternary memory circuit. The maximum write time is needed for the state 11 (17 ns) and the minimum write time is needed for the state 00 (9 ns). It can be seen from the table that the noise margin between the read voltages of consequent states is greater than 0.3V (the minimum case occurs between state 10 and state 11 which is 0.337V) which makes it possible to detect the DATA stored in the cell. Sense Amplifiers available these days can easily detect these voltage variations to identify the cell state accurately.

TABLE 4.1: Writing Mechanism for proposed design and corresponding read voltages

State to be written	Writing Technique	memristance after writing	OUTPUT Voltage after reading
00	Set DATA 3.6V for 9ns	999.86Ω	1.63V
01	Set DATA 3.6V for 9ns followed by 0V for 2ns	4.135 kΩ	1.26V
10	Set DATA 3.6V for 9ns followed by 0V for 4ns	10.017 kΩ	0.897V
11	Set DATA 3.6V for 9ns followed by 0V for 8ns	21.663 kΩ	0.56V

The whole 16×16 array system was simulated according to the operations described in TABLE 4.2. The simulation results are sown in Figure 4.11. The results are as expected with some additional delay introduced due to large array structure.

TABLE 4.2: Description of operating cycles in quaternary memory array

Time	Operation	Result
0-9 ns	State 00 written in the memory cell of fifth row and eighth column	State written successfully
17-20 ns	The memory cell of fifth row and eighth column is read	Read voltage 1.63V
25-38 ns	State 10 written in the memory cell of zeroth row and first column	State written successfully
41-44 ns	The memory cell of fifth row and eighth column is read	Read voltage 1.63V
46-49 ns	The memory cell of zeroth row and first column is read	Read voltage 0.877 V

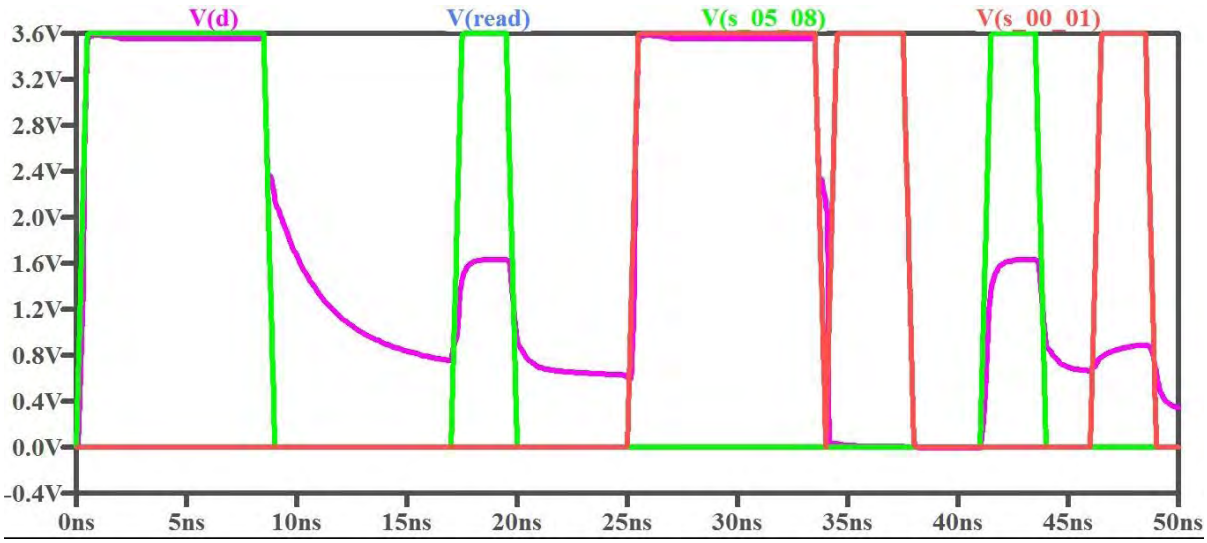


Figure 4.11: Simulation result for the memory array according to the operation described in TABLE 4.2

5. DESIGN OF THE A/D CONVERTER

5.1 Basics of the A/D Converter

As shown earlier, the output voltages for the proposed memory array are different voltage levels for different memory states. To convert these voltages to binary states an additional A/D converter has been designed in this work. The circuit diagram for the 4 to 2 A/D converter is shown below:

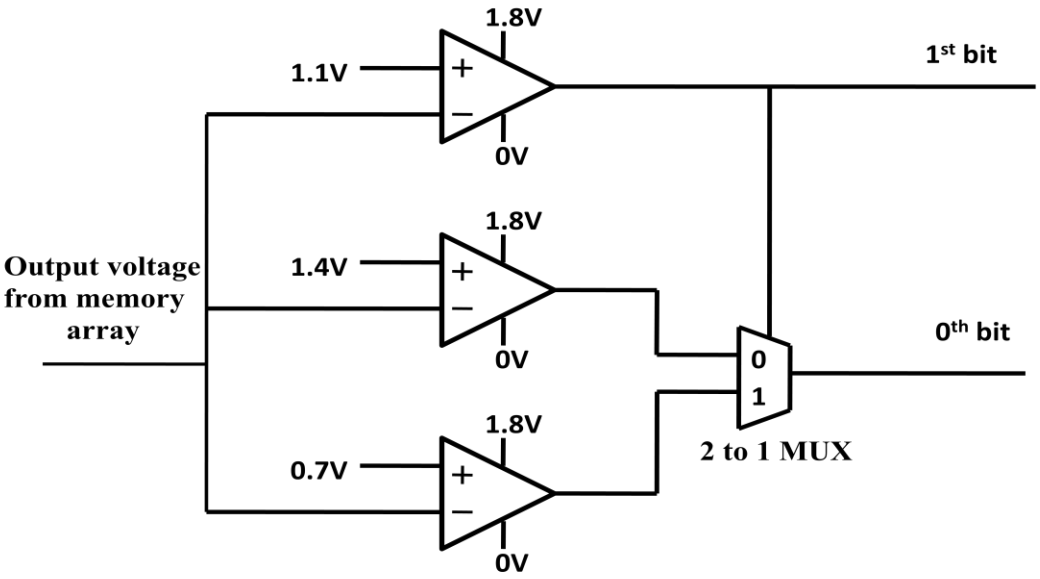


Figure 5.1: A/D converter structure

In this design three voltage converters have been used. A comparator is a device that compares two voltages or currents and switches its output to indicate which is larger. It compares the voltages at the + and – inputs. If the + input is at a higher voltage than the – input the comparator output will be high. If the – input is at a higher voltage than the + input the comparator output will be low.

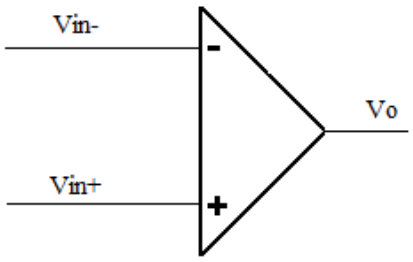


Figure 5.2: A simple voltage comparator

5.2 Comparator Design Specifications

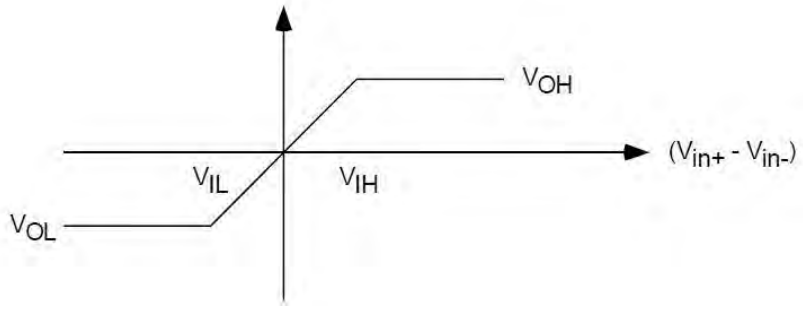


Figure 5.3: Comparator design specification

The output of a comparator is defined as:

$$V_o = \begin{cases} V_{OH} if (V_{in+} - V_{in-}) > V_{IH} \\ A_V (V_{in+} - V_{in-}) if V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} if (V_{in+} - V_{in-}) < V_{IL} \end{cases} \qquad (5.1)$$

In this work, The comparator used in our circuit was a two stage CMOS comparator with PMOS input drivers. The comparator circuit is shown in Figure 5.4:

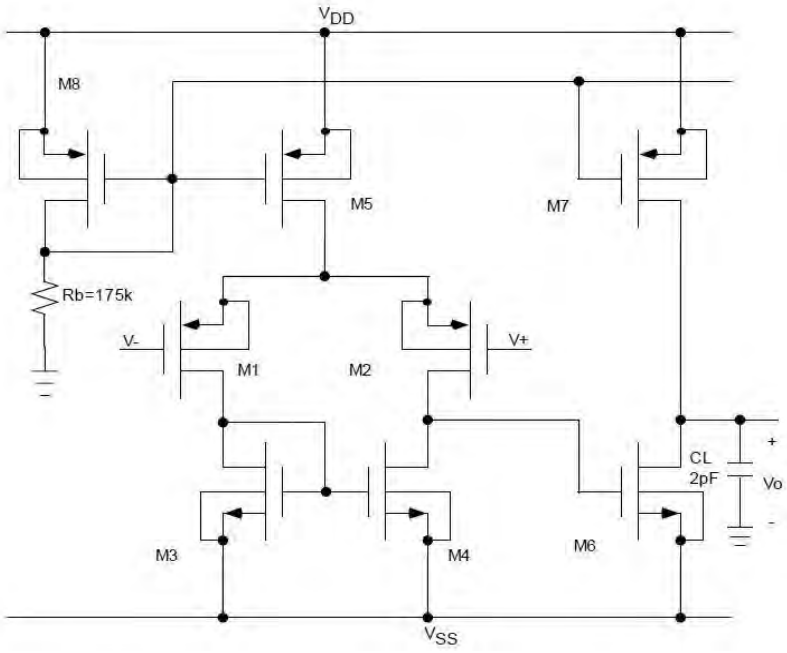


Figure 5.4: CMOS comparator with PMOS input drivers.

5.3 Output Characteristics of the A/D Converter

The output characteristics of the A/D converter designed for this work are shown in Figure 5.5-5.8. The response time of the A/D converter is longer than the earlier mentioned read time for the memory system. So for this part, the read time is taken to be 8ns. But as this is the response time of the peripheral circuit, the read time for proposed quaternary memory cell will still be considered as 3ns for the next chapters. More advanced A/D converters will have a faster response time and will have no effect on overall read time.

5.3.1 Simulation output when 00 is read

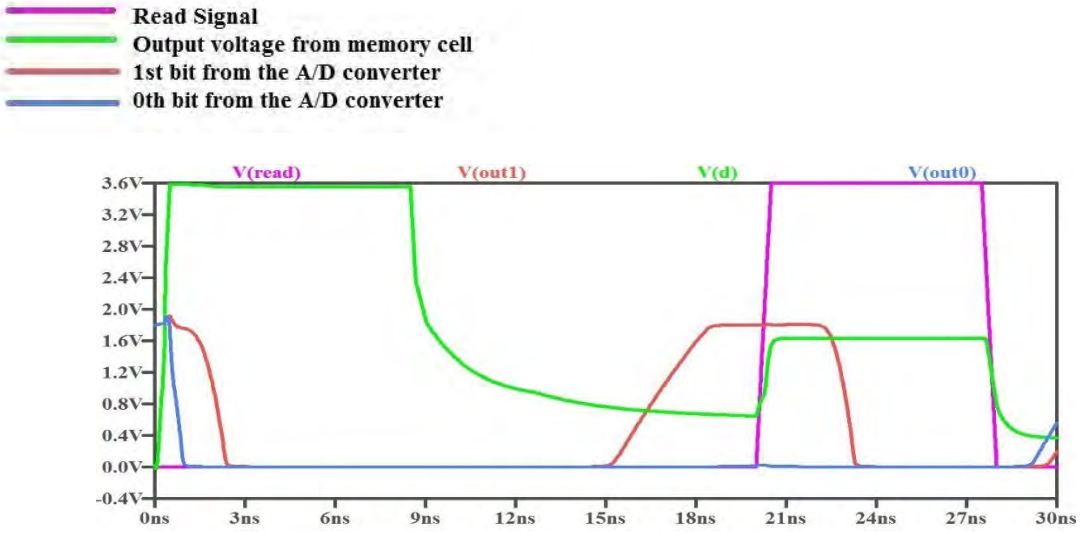


Figure 5.5: Output of the A/D converter after reading 00

5.3.2 Simulation output when 01 is read

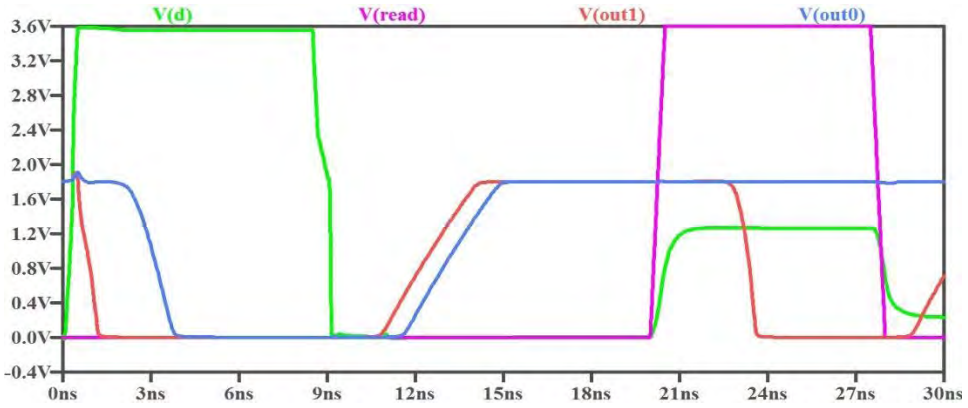


Figure 5.6: Output of the A/D converter after reading 01

5.3.3 Simulation output when 10 is read

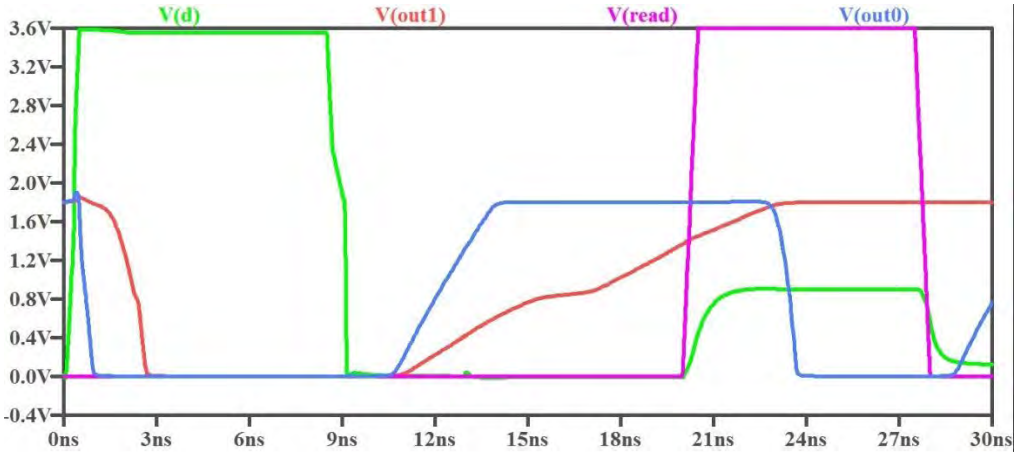


Figure 5.7: Output of the A/D converter after reading 10

5.3.4 Simulation output when 11 is read

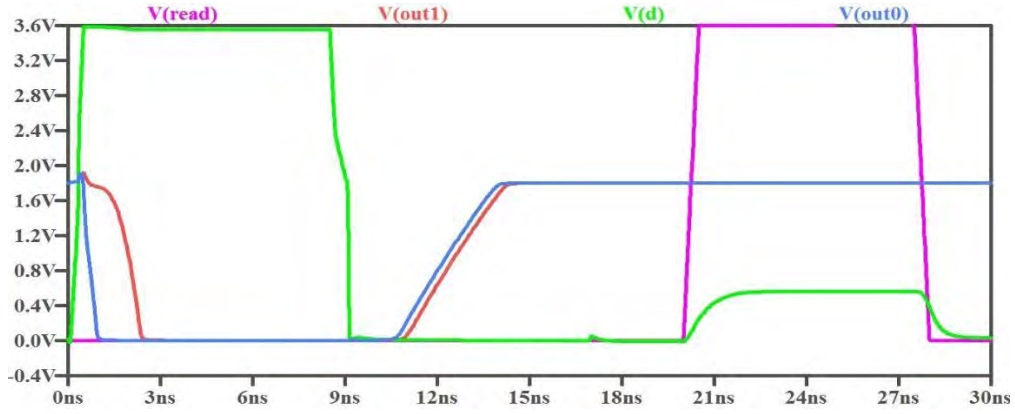


Figure 5.8: Output of the A/D converter after reading 11

6. PERFORMANCE EVALUATION

In this chapter, the performance of the proposed quaternary memory cell is evaluated in terms of energy consumption, area requirement and noise margin between the read voltages. The proposed cell is also compared to other existing memory systems to validate its superiority over others.

6.1 Performance Evaluation in Terms of Energy Consumption

Memristor based circuits are highly energy efficient due to their non-volatile nature. They consumes energy only during the operating cycles. At other times, they retain their memory state without any external power supply. On top of this, memristor based hybrid circuits consumes very low energy even for read-write cycles.

In calculating required energy in the proposed hybrid cell two factors play key roles. The first one is the characteristic of the memristor (the ON and OFF memristance and switching interval between these two states). Another factor is the circuital arrangement within the cell. However the first factor will vary with material composition and processing & fabrication technology. Another important comparable factor can be switching time (time for a memristor to completely switch logic state). This also contributes to the energy consumption factor as small switching time means power is being consumed for small period and this switching speed is proportional to the effective magnitude of potential difference across the memristor. The technique for energy calculation for writing and reading different states in the cell is described below:

6.1.1 Calculating energy for writing in a particular cell:

The circuit condition during writing the state 00 in a particular cell is shown in Figure 6.1. In this case the energy consumption occurs at the memristor and the select transistor of that particular cell. The peripheral transmission gate of the write circuit also consumes some energy which occurs due to the switching of the transmission gate. To calculate the total energy consumption for the writing period, individual energy consumptions at the transmission gate, memristor and cell selection transistor are summed up. For writing 00 in a particular cell the writing period is 9ns and lower than all other states. So the energy consumption is also lowest for this state.

For calculating the energy consumption by a single element in the circuit, the voltage and current data with respect to time is acquired from LTSPICE simulation. Later, this data is used in MATLAB to derive the power curve and energy consumption is calculated by integrating the power curve for the specific write period.

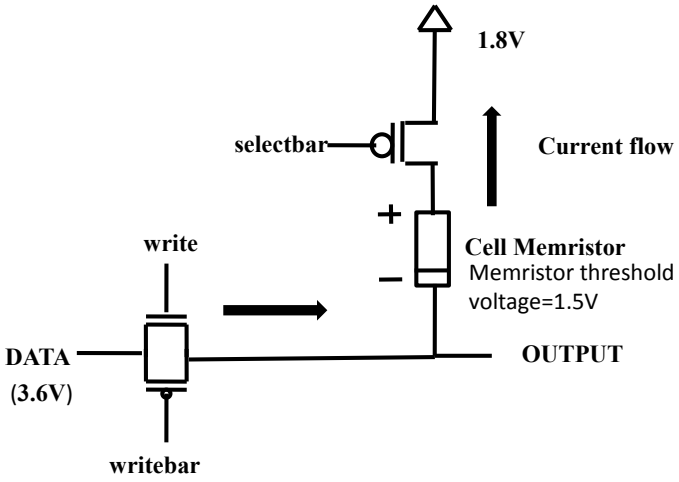


Figure 6.1: Circuit operation during writing 00 in the circuit

i. Energy consumption in transmission gate: The energy consumption in the transmission gate of the write circuit is basically switching loss. The overall loss is very low as compared to the energy consumption in the cell memristor. The area under the power curve (shown in Figure 6.3) is the measurement of the energy consumption and in the case of 00 state, 0.99744 pJ energy is consumed by the transmission gate.

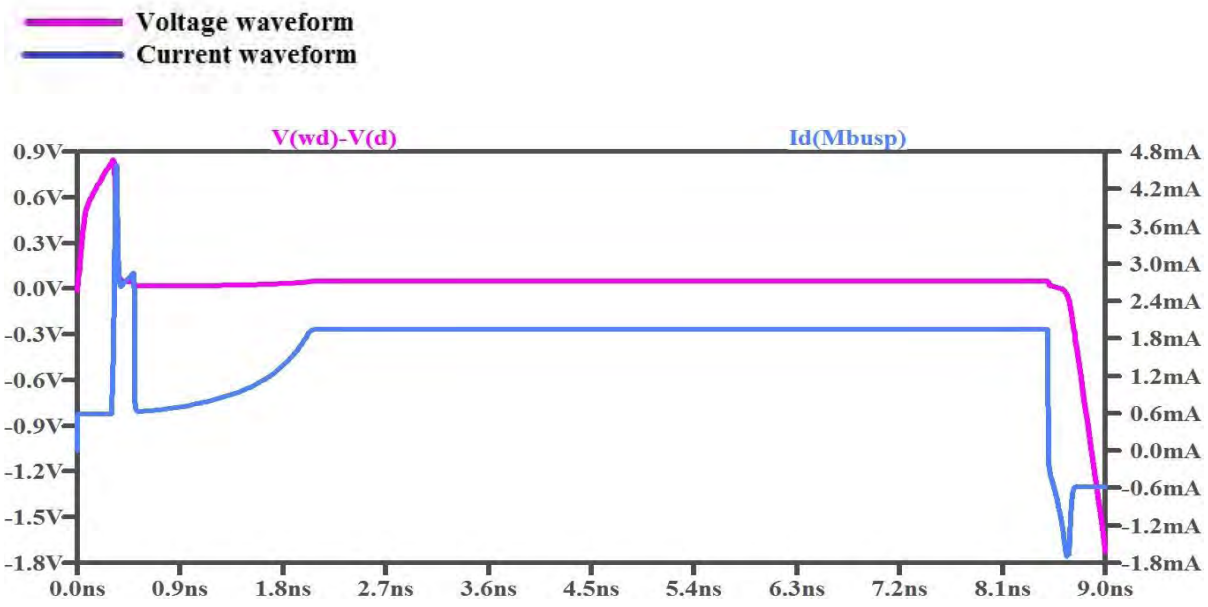


Figure 6.2: Voltage and current waveforms through the transmission gate during write "00"

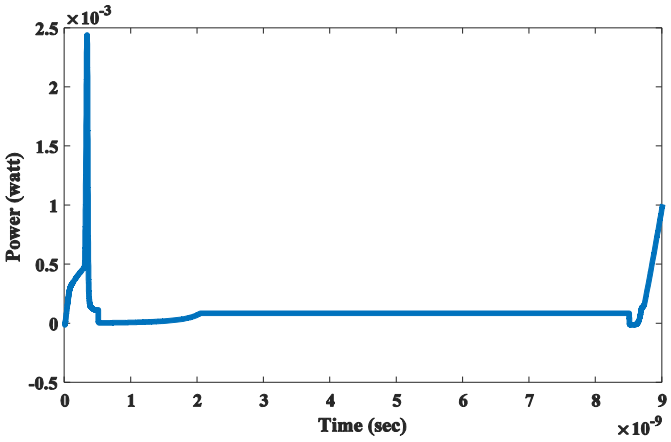


Figure 6.3: Power curve across the transmission gate while writing "00"

ii. Energy consumption in cell memristor: The major energy loss in writing any state to a particular cell of the memory array is the conduction loss through the cell memristor. During write cycle, the cell memristor changes its state according to the applied pulse. By integrating the power curve of the cell memristor for the whole writing period, the energy loss is measured to be 21.084 pJ.

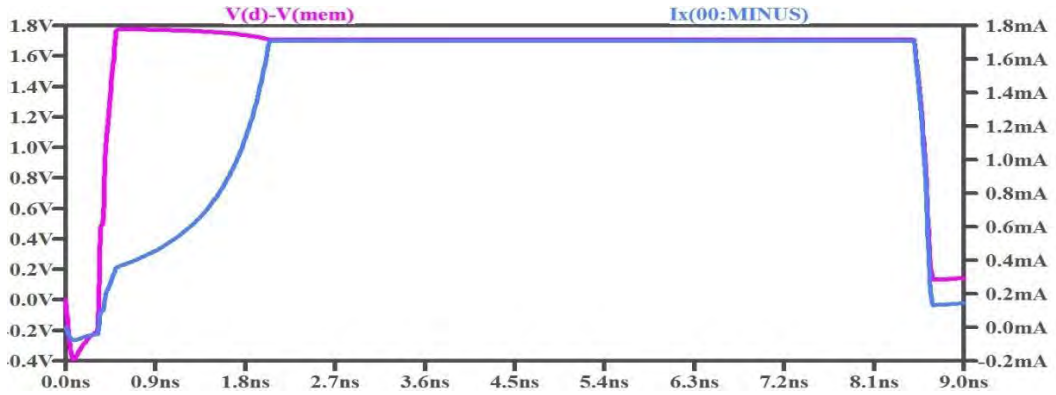


Figure 6.4: Voltage and current waveforms through the cell memristor during writing "00"

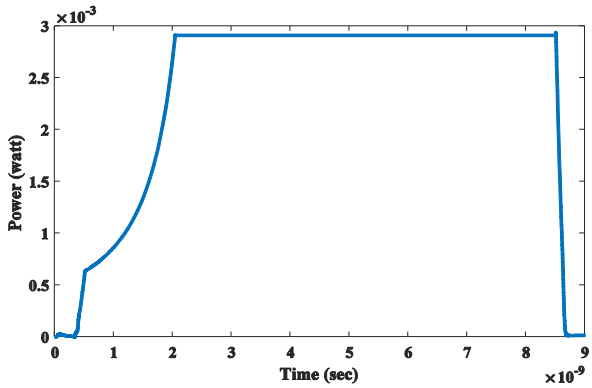


Figure 6.5: Power curve across the cell memristor while writing "00"

iii. Energy consumption in select transistor: The energy consumed (0.62326 pJ) in the cell selection transistor is again mostly switching loss and negligible.

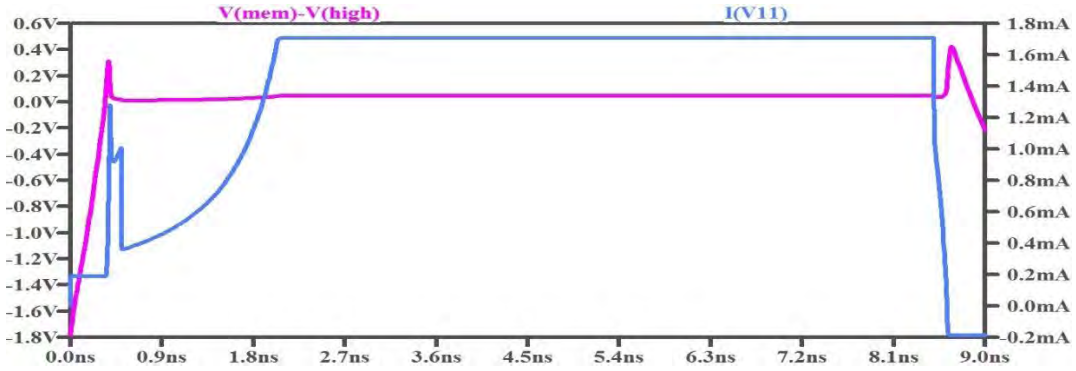


Figure 6.6: Voltage and current waveforms through the cell selection transistor during writing "00"

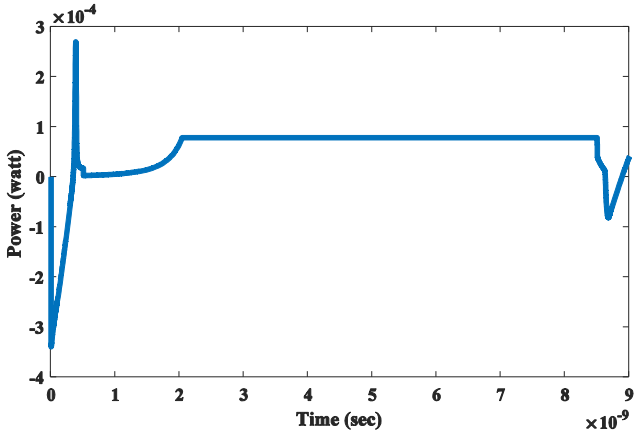


Figure 6.7: Power curve across the cell selection transistor while writing "00"

In a similar manner, the power curves and corresponding energy losses are derived for writing the remaining states (01, 10, and 11). All the power curves across the transmission gate, cell memristor and cell selection transistor have been shown in Figure 6.8 to Figure 6.16. Although for the state 00, the writing period was 9ns, but for the states 01, 10 and 11 the writing periods are longer (11ns for 01, 13ns for 10 and 17ns for 11 state). As the writing operations have already been discussed in this cases, the cell memristor changes its state twice for these states and so the energy consumption is also greater. The state 11 needs highest writing time, so the energy consumption for writing this state in the cell is also maximum (26.8799 pJ). Table 6.1 summarizes all the energy consumptions in individual elements during writing period and overall energy loss. It is again mentionable that, this losses will slightly vary depending on the previous state of the cell. The first 9ns pulse of every state is the memory erasing period and energy consumption of this period will depend on the state which is being erased.

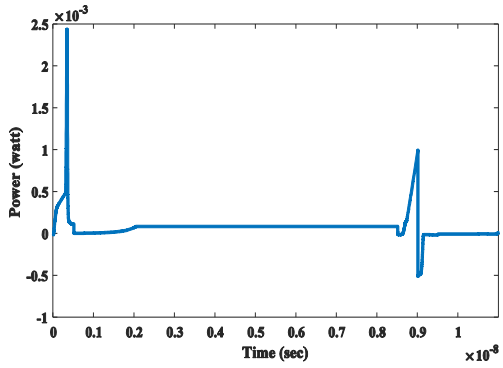


Figure 6.8: Power curve across the transmission gate while writing "01"

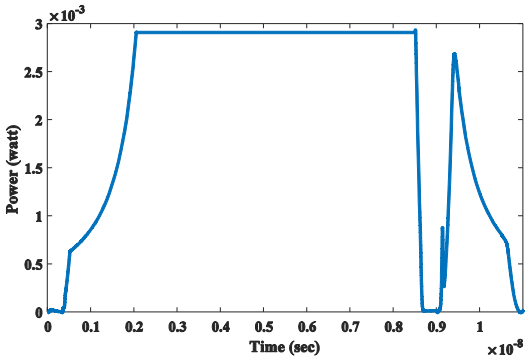


Figure 6.9: Power curve across the memristor while writing "01"

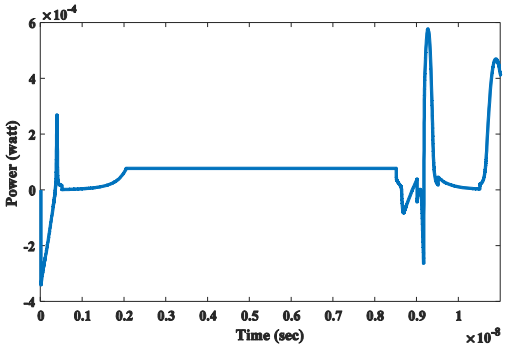


Figure 6.10: Power curve across the selection transistor while writing "01"

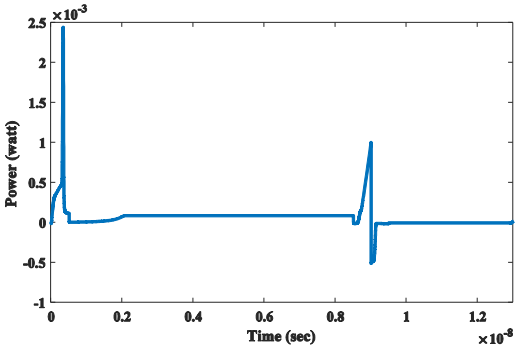


Figure 6.11: Power curve across the transmission gate while writing "10"

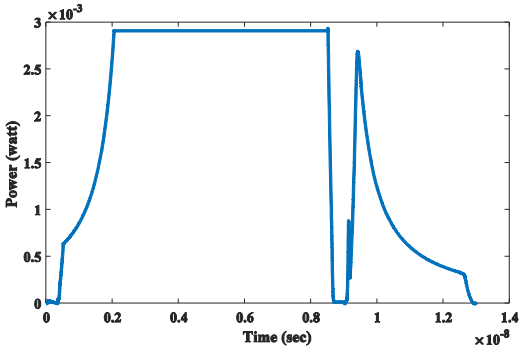


Figure 6.12: Power curve across the memristor while writing "10"

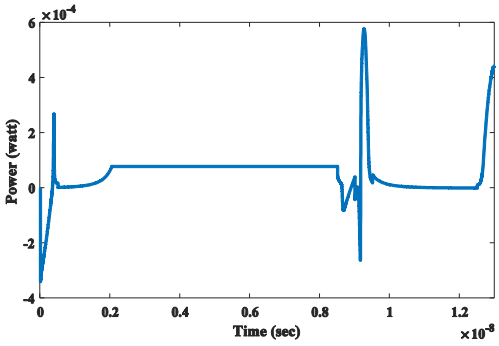


Figure 6.13: Power curve across the selection transistor while writing "10"

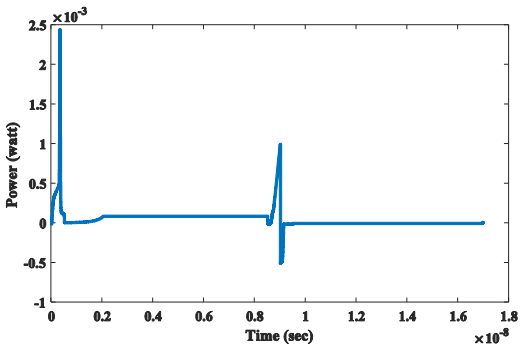


Figure 6.14: Power curve across the transmission gate while writing "11"

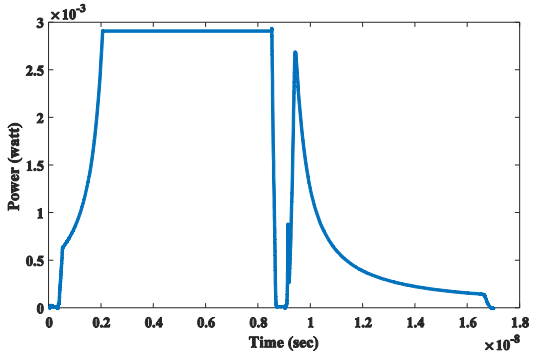


Figure 6.15: Power curve across the memristor while writing "11"

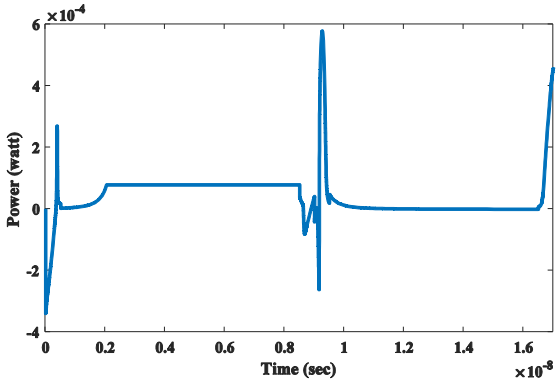


Figure 6.16: Power curve across the selection transistor while writing "11"

From Table 6.1, it is found that the proposed memristor-MOS hybrid structure is very energy efficient as it's consumes very low energy in writing two bits at a time. This is one of the reasons that the memristor-MOS hybrid structures are gaining popularity in recent times.

TABLE 6.1: Energy consumptions during writing different states in the memory cell

State to be written in the cell	Energy consumed by the Cell memristor	Energy consumed by the cell Selection transistor	Energy consumed by the transmission gate	Total energy consumption
00	21.084 pJ	0.62326 pJ	0.99744 pJ	22.7047 pJ
01	23.217 pJ	0.89531 pJ	1.0542 pJ	25.1665 pJ
10	24.130 pJ	0.87081 pJ	1.0538 pJ	26.0546 pJ
11	24.966 pJ	0.86027 pJ	1.0537 pJ	26.8799 pJ

6.1.2 Calculating energy for reading a particular cell:

The circuit arrangement during reading the memory cell has been shown in Figure 6.17. In this case, four individual elements that are the cell selection transistor, cell memristor, the read memristor and the read enabling transistor consume energy. A single voltage source 1.8V is active this time and the power curve of this source can be used to determine the overall read cycle energy consumption.

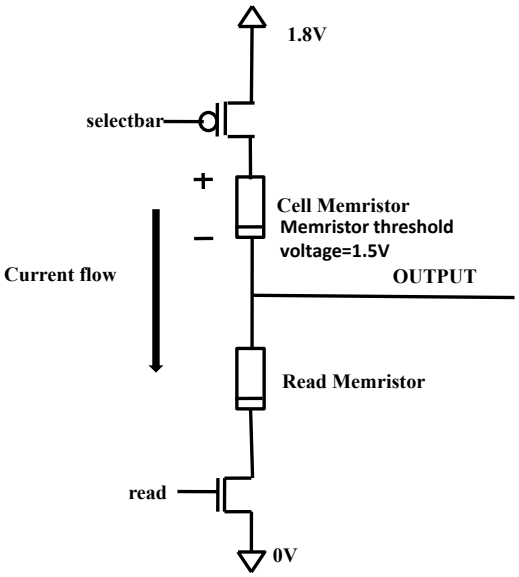


Figure 6.17: Circuit operation during reading the memory cell

The power curves during the read cycle for different states have been shown in Figure 6.18-Figure 6.21 and Table 6.2 summarizes the energy consumptions during the read cycle. The duration of the read cycle is only 3ns and the energy consumption during reading the memory cell is also very low. It is notable that as memristance of the cell is highest when the cell state is 11, so the current during this state is minimum during this state. As a result, state 11 requires minimum energy when it is read. The overall read energies for all the states are very low and the circuit structure again proves to be very energy efficient.

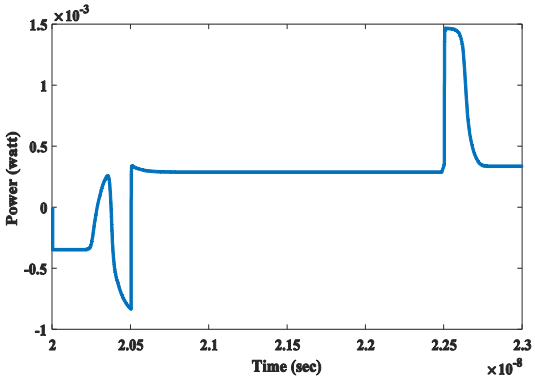


Figure 6.18: Power curve across the source while reading "00"

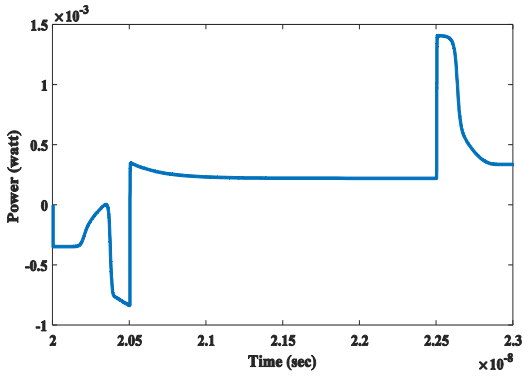


Figure 6.19: Power curve across the source while reading "01"

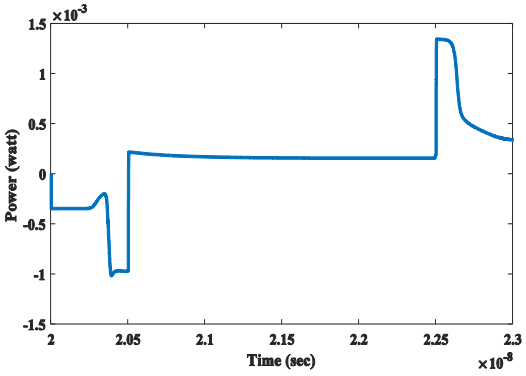


Figure 6.20: Power curve across the source while reading "10"

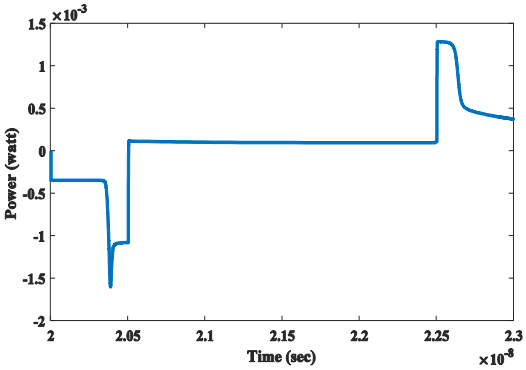


Figure 6.21: Power curve across the source while reading "11"

TABLE 6.2: Energy consumptions during reading different states in the memory cell

State to be read in the cell	Total energy consumption during read cycle
00	1.1103 pJ
01	0.99882 pJ
10	0.92429 pJ
11	0.82395 pJ

6.1.3 Comparison with other existing memory systems in terms of energy

Different memory circuits operate at different speeds and operating voltages. Again, the memristor based system use different memristor SPICE models and the device parameters also vary depending on the material composition of the memristive device. So it's very difficult to compare between them. A comparative study of the write energy consumption of some memory systems has been shown in TABLE 6.3. The read cycle energy for the proposed memory cell is even lower. Although DRAM consumes lower energy during read-write cycles, but they need periodic refreshment and they also consume static energy due to their volatile nature. So, the proposed memristor based quaternary memory cell is proved to be more energy efficient than the existing memory systems.

TABLE 6.3: Comparison of average write energy consumption for some memory systems

Memory Structure	Average write energy consumption
Proposed cell	25.2014 pJ (quaternary cell)
1T2M [20]	24.41 pJ (quaternary cell)
6T SRAM [24]	21.575 pJ (for single bit); apart from this energy, static energy is consumed in conventional SRAMs.

6.2 Performance Evaluation in Terms of Area Requirement

The proposed memristor-MOS hybrid architecture based quaternary memory cell has the superiority of having very low space requirement. All memristor based circuits has this advantage of being compact and less area consuming. The length of a memristor can be approximated to be 0.003μm and so the area is 0.00009 μm^2 which is negligible compared to the area requirement of the transistors. The proposed quaternary memory cell can be considered to be equal to the size of a single transistor which stores two bits of data. So, the data density per area is very high for this design. The peripheral read-write circuit is also very compact. On the other hand, the conventional SRAM has six transistors in the single cell and space requirement is large. The area requirement of the proposed design is comparable to DRAM but performance wise it's equivalent to the SRAM.

6.3 Performance Evaluation in Terms of Noise Margin

For the proposed quaternary memory design the output voltages during the different memory states are significantly different from each other which makes it possible to detect the data states. As the read circuit is simple voltage division based the voltage levels during reading

will depend on the operating voltage of the total system. The read voltages of some existing quaternary memory systems are discussed in TABLE 6.4.

TABLE 6.4: Comparison of read voltages in quaternary memory systems

Memory Structure	Noise margin between the read voltages
Proposed cell	The read voltages for the states 00, 01, 10 and 11 are 1.63V, 1.26V, 0.897V and 0.56V respectively. All states have minimum 0.3V difference between them.
H-bridged memristor [20]	For this design, the read mechanism is voltage division based and similar to the proposed design. The read voltages are 0.32V, 0.525V, 0.95V and 1.2V. The noise margins are feasible for this design too.
1T2M [21]	All the read voltages are below 0.25V for this design. Again the difference between the read voltages between the state 01 and 10 is less than 0.06V which may cause large error probability in data detection for the system.

6.4 Performance Evaluation in Terms of Read-Write Cycle Time:

One shortcoming of the proposed memory cell is that due to the data erasing writing technique based design, some extra time is needed for this data erasing period. The average data writing period for the proposed design is 12.5 ns and the read time is 3 ns. The response time of the memristor will depend on the SPICE model used and device parameters. Read-write cycle time for the whole memory array will automatically decrease if a memristor of faster response time is used.

7. CONCLUSION AND FUTURE WORK

In this chapter the outcome of the proposed memristor-MOS hybrid structure based quaternary memory cell and the future improvements or work opportunities on this circuit will be discussed.

7.1 Conclusion

The proposed memory cell structure in this thesis work can be addressed as data erasing writing technique based 1T1M quaternary memory array. This approach is a very promising circuit design for its high data density and simple structure. This technique is also suitable for logics with more levels. In this work, a memristor model that is closely matched to the practical fabricated memristor has been chosen and a 16x16 memory array has been designed using that memristor model. The additional read-write circuit and operation principle has been developed and described thoroughly. At first, a single cell was operated and then the whole memory array was operated according to proposed read-write mechanism. The output for the proposed circuit is different voltage levels for different memory states (00, 01, 10, and 11). An additional A/D converter has been designed in this work to convert the main output into binary logic.

In the next stage of this work, the performance of the proposed memory cell was evaluated in terms of switching energy, speed and device area. However, in these types of transistor comprising hybrid cell the size of transistor becomes crucial in the end. This is compensated by the lower power consumption and less read error probability. In the arena of memristor-transistor hybrid memory cell design technique the proposed cell can offer a greater flexibility. The longer write time for the proposed design can be justified by simple circuitry needed. Again, if memristor with higher switching speed (indicated by β in the used SPICE design) is used, then this time can be further reduced making this design very efficient and unsophisticated one.

7.2 Future Works

The proposed memory cell was simulated using TSMC 180nm technology library. But currently in the market more scaled technologies are available. Most of them have similar physical structure, hence are assumed to work satisfactorily if used in the proposed circuit and should also provide improved performance. But the latest 22nm technology has very different structure with 3-D Tri-Gate transistor. It will be a challenge to integrate memristor with this technology and exploit the advantages. New peripheral control circuitry may have to be introduced for this purpose. This can be another scope for research.

In this thesis work, the latest model of memristor has been used. There is a scope for improving the device characteristic working on device level so that the response of the simulated model gets more close to the ideal characteristics.

Again, the A/D converter used in this work has slow response time. More advanced design of A/D converter will ensure faster response and give accurate output result.

Lastly, the proposed quaternary memory cell has slightly different data pin combination than conventional 6-T SRAM cell where both complementary forms of data are needed. But this cell needs only non-inverted data. It might be possible to build a different data-bus and selector circuitry which could be more efficient for this cell combination.

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