SECTION - A

There are **FOUR** questions in this section. Answer any **THREE**.
All the symbols have their usual meanings unless explicitly mentioned.

1.  
   (a) Why are we interested in frequency domain representations of signals? How do we obtain frequency spectrum of a signal from its time domain representation? Write the corresponding formula. What is the difference between frequency spectrum of a periodic signal and frequency spectrum of an aperiodic signal? Explain graphically using the examples of a rectangular pulse and a periodic rectangular pulse train. Does being periodic or aperiodic have any effect on the bandwidth of a signal? Explain using the same examples, i.e., a rectangular pulse and a pulse train of the same pulse duration, $t$. 

   $$(4+3+6+5)$$

(b) Let $G(f)$ denotes the Fourier transform of the rectangular pulse $g(t)$ in Figure (a) below. Now, using properties of Fourier transform, express the Fourier transform of the triangular pulse $h(t)$ in Figure (b) in terms of $G(f)$. Show all steps of calculation.

   $$(10)$$

(c) Write the transfer function of an ideal low-pass filter. From the transfer function, derive the impulse response, in time domain, of the ideal low-pass filter.

   $$(2+5)$$

2.  
   (a) What is power-bandwidth trade-off? Demonstrate power-bandwidth trade-off with an example.

   $$(4+6)$$

(b) Show the Signal-to-Noise Ratio (SNR) of a uniformly spaced quantizer is proportional to input signal power. Assume all values in the amplitude range of the quantizer are equally likely.

   $$(10)$$

Contd .......... P/2
(c) A PCM system implements \( \mu \)-law companding where \( \mu = 255 \). Total number of levels in the quantizer is \( L = 256 \). Now, for each of the following sample values: \(-2.4, 0.6 \) and \( 5 \), what will be the value received after expansion. The \( \mu \)-law (for positive amplitude) is given by:

\[
y = \frac{1}{\ln(1+\mu)} \ln \left( 1 + \frac{\mu m}{m_p} \right), \quad 0 \leq \frac{m}{m_p} \leq 1
\]

Assume \( m_p = 5 \). Show detailed calculation steps.

3. (a) Draw a block diagram of the transmitter of a DPCM (Differential Pulse Code Modulation) system. Delta Modulation (DM) system is a special case of DPCM. What are the special features of a DM system with respect to a general DPCM system? What is the advantage of using a DM system? (5+3+3)

(b) Given a sequence of samples \( \{g_0, g_1, \ldots, g_{N-1}\} \) of an analog signal \( g(t) \), the Discrete Fourier transform (DFT) of the sequence is defined as:

\[
G_k = \sum_{n=0}^{N-1} g_n e^{-j \frac{2\pi kn}{N}}, \quad k = 0, 1, \ldots, N-1
\]

Here the sequence \( \{G_0, G_1, \ldots, G_{N-1}\} \) is called the transform sequence.

Now formulate a decimation-in-frequency FFT (Fast Fourier Transform) algorithm to efficiently compute the DFT of a finite data sequence. Draw the complete signal-flow graph corresponding to the computation of an 8-point DFT (i.e., \( N = 8 \)) using your algorithm. If in-place computation is used for space efficiency in such an algorithm, then the samples of the transform sequence \( G_k \) are stored in a bit-reversed order. Explain using the signal-flow graph drawn, what bit-reversed order means. (10+8+6)

4. (a) Describe two causes of asynchronicity among incoming channels of a TDM (Time Division Multiplexing) multiplexer. Describe how this problem of asynchronicity is resolved in a TDM system. (6+9)

(b) What is 'Digital Line Coding' technique? Describe six desirable characteristics of a line coding technique. For each of the characteristics, give examples: names and encoding rules of two line coding schemes such that one is better than the other with respect to that characteristic. Justify your examples with proper explanation. (2+18)
SECTION – B

There are FOUR questions in this section. Answer any THREE.

5. (a) Mention the transmission bandwidths required for DSB, QAM and SSB modulation techniques. \( (3+5+5+5=23) \)
   For a base signal \( m(t) = \cos 100t \times \cos 200t \)
   (i) Draw the spectrum of \( m(t) \).
   (ii) Draw the spectrum of DSB-SC for \( 2m(t)\cos 100t \).
   (iii) Draw the spectrum of DSB+C for \( 2(1 + m(t))\cos 1000t \).
   (iv) Draw the spectrum of LSB-SC from the figure you draw for Question (ii).
   (b) How does the value of RC affect Envelope Detection in DSB-WC? Mention the condition imposed on the value of RC. \( (8+4=12) \)

6. (a) Define Tone. What do you mean by Tone Modulation? \( (3) \)
   (b) Draw a detailed block diagram for SSB Modulation (Upper Side band only). \( (15) \)
   (c) Write the modulation equations for Frequency Modulation and Phase Modulation. Which one is better in practice? Draw the block diagrams for converting a Frequency Modulator into a Phase Modulator and vice versa. \( (8+2+7=17) \)

7. (a) Define PSK and DPSK. What is the difference between the two? \( (6+2=8) \)
   (b) For Vestigial Sideband Modulation, derive the following equation for an equalizer filter: \( H_o(f) = \frac{1}{H_i(f + f_c) + H_i(f - f_c)} \) (for an input filter \( H_i(f) \), and carrier frequency \( f_c \)). Draw the figures necessary for derivation. \( (27) \)

8. (a) Draw a detailed block diagram for a Nonlinear DSB-SC Modulator. \( (15) \)
   (b) Mention the bandwidth requirements for NBFM and WBFM. Draw the block diagram for constructing an NBFM Modulator using a DSB-SC Modulator. \( (5+15=20) \)
1. (a) A system comprising a microprocessor 8086 or 8088, a peripheral device, and a clock generator needs to be designed in such a way that the clock generator feeds both the microprocessor and the peripheral device with 5 MHz clock signals. To ensure it, a hardware designer presents the following design where he applies 15 MHz crystal in between X1 and X2, and another 30 MHz signal to EFI to feed necessary clock signals to both the microprocessor and the peripheral device (not shown in the figure).

Now, you need to answer the following (with other necessary diagrams)-

(i) Does the microprocessor get the intended clock signal? If so, then you need to explain how it is getting the clock signal from corresponding input to the clock generator to the clock input of the microprocessor. If not, then you need to explain why the two clock inputs to the clock generator are not enough or appropriate in supplying the intended clock signal to the microprocessor.

(ii) Does the peripheral device get the intended clock signal? If so, then you need to explain how it is getting the clock signal from corresponding input to the clock generator to the clock input of the peripheral device. If not, then you need to explain why the two clock inputs to the clock generator are not enough or appropriate in supplying the intended clock signal to the peripheral device.

Figure for Question 1(a)
CSE 315

Contd … Q. No. 1

(b) The following circuit is intended for a buffered system of 8086, where all address, control, and data buses are fully buffered. Do you think that the circuit is enough or appropriate for the purpose of fully buffered system of 8086? If so, then explain how it serves the purpose. If not, then present necessary correction(s) or enhancement(s) needed to be made in the circuit.

![Circuit Diagram](image)

Figure for Question 1(b)

2. (a) “The following circuit interrupts the microcontroller with NMI in case there happens any single-bit, 2-bit or multi-bit error” – validate or invalidate the statement with necessary elaboration and/or figure(s).
(b) Design separate Bank Write Strobes (for example, WR0, WR1, etc., all in low-enable) for 8086 and 80486. (15)

3. (a) 82C55 can operate in three different modes of operations. Timing diagram of one of the modes is given below: (5+15=20)

   Figure for Question 3(a)

Now, you need to answer the following:

(i) Which mode of operation is related to the above timing diagram? What can be its possible application?
CSE 315

Contd ... Q. No. 3(a)

(ii) What are the input and output signals (to 82C55) in the figure? How do the input signals control the output signal? You need to show it through pointing an arrow from a change in input signal to corresponding change in output signal for all cases.

(b) The following DRAM circuit needs to be refreshed one row at a time. The whole DRAM needs to be refreshed in 4 ms. In case of connecting it with a microprocessor having a clock rate of 5 MHz with 800 ns for a read or write operation, what will be the percentage (%) of loss in computer time due to the refreshing task? Show necessary calculations as needed.

![Figure for Question 3(b)](image)

4. (a) How can you do the following to a microprocessor?

(i) Apply always a fixed interrupt vector type number (for example FFH),
(ii) Place a fixed interrupt vector type number (for example 80H) only when it is required and have high-impedance state when it is not required, and
(iii) Expand the number of applicable interrupt vector type numbers.

(b) How can you generate necessary DMA control signals for 8086 or 8088? Elaborate with necessary figure(s).

SECTION – B

There are FOUR questions in this Section. Answer any THREE questions.
Find the Pin Configuration of ATmega32 MCU and its different register configurations at the end of the questions. If configuration for any of the required register is missing, just assume a configuration and clearly show the assumed configuration. If you believe any control word/bit configuration is missing in the question paper, just assume a pattern of your choice and clearly mention your assumption.

5. (a) Write a simple C program for ATmega16/32 to take an 8-bit input from Port A every second and output that to Port B.

(b) What is wrong with the following push button connection? Describe two different ways to tackle the problem in ATmega16/32.
CSE 315

Contd ... Q. No. 5(b)

Figure: Push button connection for question 5(b)

(c) How can you enable nested interrupts in ATmega16/32?

6. (a) Suppose two active high push switches A and B are connected to INT0 and INT2 pin of an ATmega32 MCU, respectively. Also, eight active high LEDs (LED0 – LED7) are connected to PA0 – PA7. Write a C code using external interrupt to implement a ring counter, which counts up upon pressing the switch A and counts down upon pressing the switch B. Use 0 for don’t care bits. The three external interrupt vector names are INTO_vect, INT1_vect, and INT2_vect.

The codes for external interrupt events of INT0 and INT1 are as following:

<table>
<thead>
<tr>
<th>Code</th>
<th>Interrupt Triggering Events</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Low Level</td>
</tr>
<tr>
<td>01</td>
<td>Any Logical Change</td>
</tr>
<tr>
<td>10</td>
<td>Falling Edge</td>
</tr>
<tr>
<td>11</td>
<td>Rising Edge</td>
</tr>
</tbody>
</table>

The codes for external interrupt events of external INT2:

<table>
<thead>
<tr>
<th>Code</th>
<th>Interrupt Triggering Events</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Falling Edge</td>
</tr>
<tr>
<td>1</td>
<td>Rising Edge</td>
</tr>
</tbody>
</table>

(b) What is the difference between Phase Correct and Fast PWM modes? Explain with appropriate examples and figures as needed.

(c) Write a program to write the characters ‘a’ to ‘z’ in the first 26 bytes of EEPROM.

7. (a) Consider, you are continuously receiving data from a PC using UART in polling approach. The connection details are: Baud rate:9600 bps, no parity (code: 0x0), 1 stop bit (code: 0x0), 8 data bits (code: 0x3), and asynchronous communication (code: 0x0). Assume a clock speed of 8MHz. Write a C code that continuously receives a word from the PC, writes that word to PORTA, and sleeps for 1 second and repeats. Clearly specify the initialization of different registers and necessary calculations of their values.
CSE 315

Contd ... Q. No. 7

(b) Consider you have configured the ATmega32 ADC with a reference voltage of 4V and left justified the result. Show the calculation to find out the step size in volts when:

(i) You are only reading ADCH
(ii) You are reading both ADCL and ADCH

(c) Describe with example(s) the necessity and application of using “volatile” variables in a C program in the context of ATmega16/32 interrupts.

8. (a) You need to write a C code for an ATmega32/16 based system to control temperature of a medicine storage facility. The facility requires the room temperature to be within 4-10 degree Celsius. If the temperature falls below the range, it should be increased by turning on the heater and when the temperature exceeds the range, the room needs to be cooled down by turning on the air cooler. Both the heater and air cooler stay off while temperature is within the desired range. A temperature sensor is used to measure the temperature of the room.

The output voltage of the temperature sensor is linearly proportional to the temperature and produces an output of 0V to 5.0 V for 0 degree to 20 degree Celsius linearly. Assume that you are using polling mode, reference voltage of 5 V (code: 0x1) and a prescalar of 2 (code:0x1). The sensor is connected to the pin ADC0 (code:0x0). You can turn on the heater and air cooler by writing a logic 1 to PB0 and PB1, respectively. Each time you turn on the heater or the air cooler, wait for 20 seconds before taking a new reading from temperature sensor.

(b) Determine the values of TOP and OCR1 (The value of OCR1 at which compare match occurs) to create a 1 KHz signal with 40% duty cycle using Fast PWM modes. The system clock frequency is 1 MHz an prescalar is 8.

(c) Write a C function unsigned int UART_receive () for ATmega16/32 that can receive data (character size 9 bits) sent through UART. If there is a frame or parity error, return -1.
Figure 2: ATmega 32 MCU pinout (for Section B)

Table 2: List of registers (for Section B)
L-3/T-1/CSE

Date: 17/09/2018

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1  B. Sc. Engineering Examinations 2017-2018

Sub: CSE 309 (Compiler)

Full Marks: 210  Time: 3 Hours

The figures in the margin indicate full marks

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are FOUR questions in this section. Answer any THREE.

1. (a) Explain, with necessary examples, the tasks performed by a preprocessor in compilation.

(b) In a certain programming language, the decimal numbers are like, 123.456E ± 789. Here, decimal part and exponent part are optional. Furthermore, the plus or minus in the exponent is optional. In formulating regular definitions for these numbers, some one came up with the following:

   \[ \text{number } \rightarrow [0-9] [0-9]^[0-9][0-9]^[0-9]^(E+\text{-}\text{[0-9]}^\text{*}) \]

   The above definition has got a number of flaws in it. Point out these flaws with necessary explanations.

(c) Explain "panic mode" in lexical analysis. What could be the side effects of panic mode?

   (10)

   (15)

   (10)

2. (a) In lexical analysis, the analyzer often has to look one or more characters beyond the next lexeme before it can be sure it has the right lexeme.

A programming language has got the following tokens:

<table>
<thead>
<tr>
<th>Token</th>
<th>Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>Identifiers</td>
<td>Starts with _ or letter followed by _ or letter or digit as many times as we want</td>
</tr>
<tr>
<td>IF</td>
<td>if</td>
</tr>
<tr>
<td>THEN</td>
<td>then</td>
</tr>
<tr>
<td>ELSE</td>
<td>else</td>
</tr>
<tr>
<td>ROR</td>
<td>&gt;&gt;</td>
</tr>
<tr>
<td>ROL</td>
<td>&lt;&lt;</td>
</tr>
<tr>
<td>PLUS</td>
<td>+</td>
</tr>
<tr>
<td>INC</td>
<td>++</td>
</tr>
<tr>
<td>TINC</td>
<td>+++</td>
</tr>
<tr>
<td>GT</td>
<td>&gt;</td>
</tr>
<tr>
<td>GE</td>
<td>&gt;=</td>
</tr>
</tbody>
</table>

Explain which of the above tokens require reading extra characters and which do not.

(12)

Contd ........ P/2
(b) What would have happened if instead of buffer pairs in lexical analysis, we decided to use a single buffer keeping the pointers same as those in buffer pair? Provide necessary diagram. Can the scenario be changed by using sentinels? Explain.

(c) The reserved words in programming languages look like identifiers and these require special measures so that these are not confused with identifiers. Describe these special measures.

3. (a) Enumerate the principles that are adopted in Lex for conflict resolution when several prefixes of the input match one or more patterns.

(b) Construct procedure based recursive-descent parser for the grammar given below:

\[ S \rightarrow Aa | bBb | c \]
\[ A \rightarrow aa | dd \]
\[ B \rightarrow b | eBe | e \]

Now, parse the string bebebe using the constructed parser and show how this parser actually implements a top-down parsing.

(c) Explain why left-recursive grammars with production rules like \( S \rightarrow Sa \) are not suitable for recursive-descent parser. In light of your answer, what do you think will happen in case of production rules like \( S \rightarrow aSa \)?

(d) Left factor the following grammar:

\[ S \rightarrow abA | abcS \]
\[ A \rightarrow aa | \varepsilon \]

In terms of the \( k \) in LL(\( k \)), what is the value of \( k \) for the above grammar?

4. (a) Compute the FIRST and FOLLOW sets for the nonterminals of the following grammar and use them to construct a parsing table of a top-down predictive parser for this grammar.

\[ S \rightarrow (A) | a \]
\[ A \rightarrow SB \]
\[ B \rightarrow +SB | \varepsilon \]

(b) Eliminate left-recursion from the following grammar:

\[ S \rightarrow Sc | Ta | b \]
\[ T \rightarrow Tc | Sd | Ub | d \]
\[ U \rightarrow Ua |Td | Sb | b \]

(c) Among other reasons, a grammar can not be LL(1), if, whenever \( A \rightarrow \alpha | \beta \) are two distinct productions of \( G \), the following condition does not hold:

"If \( \beta \Rightarrow \varepsilon \), then \( \alpha \) does not derive any string beginning with a terminal in FOLLOW(\( A \)). Likewise, for \( \alpha \Rightarrow \varepsilon , \beta \) does not derive any string beginning with a terminal in FOLLOW(\( A \))". Why? Explain with necessary examples.
CSE 309

SECTION – B

There are FOUR questions in this section. Answer any THREE.

5. (a) Look at the following, Syntax Directed Definition (SDD).

<table>
<thead>
<tr>
<th>PRODUCTION</th>
<th>SEMANTIC RULES</th>
</tr>
</thead>
</table>
| 1) $T \rightarrow FT'$ | $T'.\text{inn}=F\text{.real}$  
| | $T'.\text{real}=T'.\text{sym}$  
| 2) $T' \rightarrow \ast FT'$ | $T'.\text{inn}=T'.\text{inn} \times F\text{.real}$  
| | $T'.\text{sym}=T'.\text{sym}$  
| 3) $T' \rightarrow \epsilon$ | $T'.\text{inn}=T'.\text{sym}$  
| 4) $F \rightarrow \text{digit}$ | $F\text{.real}=\text{digit}.\text{real}$

This SDD can evaluate the value of an expression in the attribute val. However, it cannot handle addition/subtractions. For example, the given SDD will successfully handle the expression "2*3*4" but fail for the expression "2+3*4". Extend the SDD so that it is capable of handling addition/subtraction operators (+ and −) and consequently, is able to evaluate expressions with arbitrary number of addition, subtraction and multiplication operators.

(b) For the input string "2+3*4+5", draw the annotated parse tree with the SDD that you have just written in question 5(a).

(c) Write down the semantic rules for the productions below so that equivalent short circuit code is generated correctly.

(i) $S \rightarrow \text{if } (B) S_1 \text{ else } S_2$

(ii) $B \rightarrow B_1 \& \& B_2$

Assume that jumping labels are managed using inherited attributes $B\text{.true}$, $B\text{.false}$ and $S\text{.next}$; where $B$ is a Boolean expression and $S$ is a statement.

6. (a) Notice the following SDD.

<table>
<thead>
<tr>
<th>PRODUCTION</th>
<th>SEMANTIC RULES</th>
</tr>
</thead>
</table>
| $S \rightarrow \text{Id} \cdot E$ | $S\text{.code} = E\text{.code}$  
| | $\text{gen(toplevel.id.lexeme) }\leftarrow' E\text{.addr}$  
| $E \rightarrow E_1 + E_2$ | $E\text{.addr} = \text{new Temp}()$  
| | $E\text{.code} = E_1\text{.code} || E_2\text{.code}$  
| | $\text{gen(E.addr }= E_1\text{.addr }+ E_2\text{.addr) }$  
| $\mid - E_1$ | $E\text{.addr} = \text{new Temp}()$  
| | $E\text{.code} = E_1\text{.code}$  
| | $\text{gen(E.addr }= E_1\text{.addr) }$  
| $\mid ( E_1 )$ | $E\text{.addr} = E_1\text{.addr}$  
| | $E\text{.code} = E_1\text{.code}$  
| $\mid \text{id}$ | $E\text{.addr} = \text{toplevel.id.lexeme}$  
| | $E\text{.code} = "$$

Contd …….. P/4
This is used for generating machine code to an arithmetic expression. Now, for the following expression, draw the annotated parse tree. Annotate each internal node.

\[ a = -(b) + c; \]

Finally, write the code that has been generated by SDD separately.

(b) Notice the following activation tree.

When \( q(3,3) \) is being run by the processor,

(i) What are the live activations?

(ii) What activations have already been processed?

(c) Determine liveliness and next-use information for the following basic block.

\[ r = a + b \]
\[ u = a \cdot c \]
\[ v = t + u \]
\[ s = d \]
\[ d = v + u \]

7. (a) Convert the following code into flow graph:

1) \( i = 1 \)
2) \( j = 1 \)
3) \( t1 = 10 \cdot i \)
4) \( t2 = t1 + j \)
5) \( t3 = 8 + t2 \)
6) \( t4 = t3 - 88 \)
7) \( s[t4] = 0.0 \)
8) \( j = j + 1 \)
9) if \( j <= 10 \) goto (3)
10) \( i = i + 1 \)
11) if \( i <= 10 \) goto (2)
12) \( i = 1 \)
13) \( t5 = i - 1 \)
14) \( t6 = 88 \cdot t5 \)
15) \( s[t6] = 1.0 \)
16) \( i = i + 1 \)
17) if \( i <= 10 \) goto (13)
(b) Give examples of—

(i) Copy propagation

(ii) Code motion

(c) What is the output of the following code? Justify with a proper data structure.

```java
public class Base {
    public int publicBaseInt = 1;
    protected int baseInt = 2;
}

public class Derived extends Base {
    public int derivedInt = 3;
    public int publicBaseInt = 4;
    public void doSomething() {
        System.out.println(publicBaseInt);
        System.out.println(baseInt);
        System.out.println(derivedInt);
        int publicBaseInt = 6;
        System.out.println(publicBaseInt);
    }
}
```

8. (a) What is the output of the following code segment if—

(i) The program names are handled in compilation time?

(ii) The program names are handled in runtime?

```java
int x = 137;
int y = 42;
void Function1() {
    Print(x + y);
}

void Function2() {
    int x = 0;
    Function1();
}

void Function3() {
    int y = 0;
    Function2();
}

Function1();
Function2();
Function3();
```

(b) What is the one-core problem of the garbage collection method reference counting? Give an example.

(c) For the stop-and-copy generational garbage collectors, we cannot simply take bitwise copies of objects. Explain the reason. Also, explain how this issue is handled using necessary figures.
1. (a) Consider the following C code:
\[ A = B + C; \quad D = A + E; \]
All the above are memory instructions. The base address is in register t0 and the offsets are A (0), B (4), C (8), D (12), E (16). How many cycles are required to execute the above? Can you reduce the number of cycles using code scheduling? If yes, what will be resulting number of cycles? Show each step.

(b) Consider the following set of instructions:
\[ \text{add}, \ lw, \ beq \]
Draw the complete single cycle data path (not pipelined) and control that can execute the above set of instructions.

(c) Consider the following information for load word (lw) instruction:

<table>
<thead>
<tr>
<th>Instr.</th>
<th>Instruction Fetch</th>
<th>Register read</th>
<th>ALU op</th>
<th>Memory access</th>
<th>Register write</th>
</tr>
</thead>
<tbody>
<tr>
<td>lw</td>
<td>200 ps</td>
<td>100 ps</td>
<td>100 ps</td>
<td>200 ps</td>
<td>100 ps</td>
</tr>
</tbody>
</table>

Consider the following program:
\[ \text{lw} \, $1, \, 100($0) \]
\[ \text{lw} \, $2, \, 200($0) \]
\[ \text{lw} \, $3, \, 300($0) \]
What is the speedup for the pipelined datapath over the single cycle datapath for this program? What will be the speedup if we add 3,000,000 more load word (lw) instructions?

(d) "Even with a perfect branch predictor, l-cycle penalty for a taken branch". Why is that? How to solve this?

2. (a) Briefly explain double data hazard with example. How MIPS detect hazard due to the use of load instruction and how MIPS stall the pipeline?

(b) Design a complete forwarding unit with necessary equations for MIPS considering double data hazard. Draw the complete forwarding unit using the provided figure below.

Contd .......... P/2
(c) Give the MIPS codes for each of the following cases of data hazard for branches:

(i) Needs one cycle stall to resolve
(ii) Needs two cycle stalls to resolve

(d) Consider the following code:

outer:

// some code

inner:

// some code
beq $t0, $zero, inner
// some code
beq $t1, $zero, outer

What is the problem with the above code if we use 1 bit branch predictor? How can you solve that?

3. (a) What are the three sources of cache misses? The specification of an ideal disk is as follows:

sector size: 1 MB, rotational latency: 10000 rpm, average seek time: 5 ms, transfer rate: 100 MB/s, and controller overhead: 0.5 ms. What is the average read time for the disk? If the average seek time can be reduced to 2 ms, then how much improvement can be possible on average read time?
CSE 305

Contd... Q. No. 3

(b) What is meant by spatial and temporal locality? Briefly explain write-through and write-back scheme for cache. How do write-through and write-back schemes handle write-miss?

(c) Briefly explain how page table works with respect to virtual address, physical address, main memory and disk.

(d) Assume the miss rate of an instruction cache is 3%, the miss rate of the data cache is 5%, and the frequency of all loads and stores is 40%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 200 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Also, determine the amount of execution time spent on memory stalls.

4.

(a) Suppose we have a processor with a base CPI of 1.0, assuming all references hit in the primary cache and a clock rate of 4 GHz. Assume a main memory that has an access time of 200 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 4%. How much faster will the processor be if we add a second level cache that has a 10 ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 1%? How much faster will the processor be if we add a third level cache that has a 40 ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 0.5%?

(b) Assume there are three small caches, each consisting of four one-word blocks and uses LRU replacement policy. One cache is fully associative, the second is two-way set-associative, and the third is direct-mapped. Find the number of misses for each cache organization, given the following sequence of block addresses:

- 1, 3, 5, 1, 3, 1, 3, 5, 3, 1, 5, 3

(c) What is meant by TLB? Why TLB is necessary in a virtual memory system?

(d) Explain (with flow chart) the interaction between TLB and data cache for only write operation.

SECTION – B

There are FOUR questions in this section. Answer any THREE.

5.

(a) Suppose there are three classes of instructions A, B and C in a particular instruction set architecture with CPIs 1.2, 2 and 2.5, respectively. The number of instructions from each class in two separate programs P1 and P2 are as follows:

- P1: 4A, 5B, 3C
- P2: 3A, 4B, 5C

Find the CPI and the execution time for each program.
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Contd... Q. No. 5(a)

<table>
<thead>
<tr>
<th>Programs</th>
<th>Instruction Classes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
</tr>
<tr>
<td>P1</td>
<td>40</td>
</tr>
<tr>
<td>P2</td>
<td>12</td>
</tr>
</tbody>
</table>

(i) Which program will execute faster and by how much?

(ii) By how much should we improve the CPI of Instruction Class B to make P1 execute two times faster? Explain your finding.

(b) Consider a half precision floating point representation system where each floating point is represented by 16 bits in which the exponent is 4 bits long. Now convert the two floating points \(0.75_{10}\) and \(1.25_{10}\) into the mentioned representation system and then demonstrate the addition of them step by step along with the values of exponent and fraction fields at every step.

(c) Determine the decimal value of the floating point represented by the hexadecimal value \((7F80 0005)_{\text{hex}}\) according to IEEE 754 single precision floating point format.

6. (a) Design an ALU with three selection variables \(S_2, S_1\) and \(S_0\) that performs the following operations on two 4-bit inputs (A and B):

<table>
<thead>
<tr>
<th>(S_2)</th>
<th>(S_1)</th>
<th>(S_0)</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Addition</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Transfer A</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Decrement A</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Add 1's complement of B to A</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>XOR</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>AND</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>NOT</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>OR</td>
</tr>
</tbody>
</table>

Draw the logic diagram of one typical stage of your designed ALU.

(b) For each arithmetic operation listed in question 6(a), find out the conditions under which the output carry will be equal to 1.
7. (a) The following C code segment can sort an array of integers in ascending order. Write down the equivalent MIPS assembly code for it. Assume appropriate registers for the variables.

```c
void swap(int v[], int k)
{
    int temp;
    temp = v[k];
    v[k] = v[k+1];
    v[k+1] = temp;
}

void sort (int v[], int n)
{
    int i, j;
    for (i = 0; i < n; i += 1) {
        for (j = i - 1; j >= 0 && v[j] > v[j + 1]; j --) {
            swap(v, j);
        }
    }
}
```

(b) Suppose you are required to jump to the instruction at address (4000 0001)_{hex}. Write down the MIPS assembly code for this task.

8. (a) Suppose you have a 4-bit ALU and you are required to perform a division operation, where the dividend is 11010101 and the divisor is 1011. Show the division process step by step along with value of each relevant register at every step.

(b) Write down the equivalent MIPS assembly code for the following function, written in C programming language. Assume appropriate registers for the variables.

```c
float convert (float cels)
{
    float fahr = (9.0 * cels) / 5.0;
    fahr = fahr + 32.0;
    return fahr;
}
```

(c) How many instruction formats are there in MIPS? Write down the name of each instruction format along with the length of each field in it.

---
1. (a) There are several options of ERP implementation for organization which has 250 users. These are described as follows:

*SAP Customization:*
ERP for any organization can be implemented by customizing modules of SAP. The cost for per user licensing fee of the SAP is USD 2000.00. It might require complex customization with the effort of 30 Man Month by the highly experienced SAP consultants and programmers. It might require easy customization with the effort of 20 Man Month by the moderately experienced SAP consultants and programmers. The probability of requiring complex customization would be half of the probability of requiring easy customization. The cost of Man Month for highly and moderately experienced SAP consultants or programmers are USD 20000.00 and USD 10000.00 respectively.

*Customized ERP Development by own development team:*
It might require 5 analysts, 20 developers, 19 testers and 5 system engineers to develop and implement ERP in 20 months. The estimated monthly salary of analyst, developer, tester and system engineer are USD 4000.00, USD 3000.00, USD 2500.00 and USD 3500.00 respectively. There is a 60% chance to reuse the previously developed components to reduce the development time by 6 months.

*Customized ERP Development through outsourcing:*
The cost ERP developed by the vendor id USD 400000.00. It might require 2 analysts, 2 developers, 5 testers and 2 system engineers to supervise and monitor ERP development for 8 months. The estimated monthly salary of analyst, developer, tester and system engineer are USD 5000.00, USD 2500.00, USD 2500.00 and USD 3500.00 respectively.

Analyze all the options mentioned above and find the optimal decision.

(b) Discuss the pricing decisions in the following situations with proper reasoning:

(i) The software development company is trying to get a contract for automation of an organization where the maximum job duration of the employees in the client’s organization is 2 years.

(ii) The software development company is in the process of getting a new contract which will continue for the next 5 years.
(iii) The software development company has just started.
(iv) The new VAT rule may require new software and a multinational company wants to develop that software by the software development company.
(c) What is algorithmic cost model? What are the factors of accuracy in software cost estimation?
(d) After requirement analysis, the experienced system analyst estimated that the size of the code for a training simulator for fertilizer factory might be 230 KLOC. The software development company is a 5 year old company with CMMI level 3. The top management is committed to do formal risk management for smooth software development. Estimate the effort in person month, development time and team size using COCOMO 2 model.

2. (a) What are the problems of waterfall model? Describe how other models solve the problem.
(b) Consider a software development of a government organization which is using the paper based system by the employees for the last 40 years. The average age of the employees is more than 50 years. Describe how prototyping helps writing SRS in this situation. Show all the phases of prototyping with respect to this development scenario.
(c) Why is refactoring important in agile development? Give some example of refactoring in software development life cycle.
(d) “A pair of programmers working together is more efficient than two programmers working separately” – Justify.
(e) Write down a typical scrum meeting minutes (description of the meeting) for the software development of a digital research library.

3. (a) What do you mean by configuration in Software Configuration Management? What are the activities of Software Configuration Management? Explain with brief description.
(b) Explain baseline, codeline and mainline with proper examples.
(c) Consider a university records management system. The university will allow the students of any department to take audit courses from other departments. In this case the grades will not be reflected in the cumulative grade point average. Show the content of the change request form after approving the change.
(d) Why is merging required after branching of the codelines. Explain with necessary figures after defining branching and merging.
(e) Explain how the source code checksum helps minimize recompilation in system building.
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4. (a) How can you define software architecture? Show the architecture of a residential student hall management system with the following features:
   (i) Seat allocation, change and cancellation
   (ii) Food charge receiving through credit card and bank payment with automatic interfacing
   (iii) Issuing and returning books from hall library
   (iv) Clearance certificate issuing
   (v) Loan issue and repayment of the loan.
(b) Represent a library management system using layered architectural pattern and client-server architectural pattern with necessary justifications.
(c) A software development schedule is fixed from Oct 2018 to March 2019 in an offshore development center in the Gulshan area of Dhaka city. The top management is thinking of health risks of the software development team during the development period. Identify, analyze and plan mitigation strategies for health related risks in the above mentioned context.
(d) “Increasing reliability does not necessarily mean increasing safety” – Justify mentioning two different scenarios of using software.

   SECTION-B
   There are FOUR questions in this section. Answer any THREE questions.

5. (a) Ward is division of a hospital or a suite of rooms shared by patients who need a similar kind of care. In a hospital, there are a number of wards, each of which may be empty or have one or more patients. Each ward has a unique name. Wards are differentiated by gender of its patients, i.e. male wards and female wards. A ward can only have patients of the gender admitted to it. Every ward has a fixed capacity, which is the maximum number of patients that can be on it at one time (i.e. the capacity is the number of beds in the ward). Different wards may have different capacities. The doctors in the hospital are organized into teams. Each team has a unique name or code (e.g. Orthopaedics or Pediatrics) and is headed by a consultant doctor or attending physician. Consultant doctor or attending physician is the senior doctor who has completed all of his or her specialist training, residency and practices medicine in a clinic or hospital, in the specialty learned during residency. She or he can supervise fellows, residents, and medical students. The rest of the team members are all junior doctors. Each doctor could be a member of no more than one team. Everyday each consultant doctor visits the patients admitted under him/her. During this visit, she/he prescribes treatment or modifies previous prescription. When a patient is ready to released, s/he advises the release. Design a Class diagram to implement the scenario described above.

Contd .......... P/4
(b) What do you understand by the usability of software application? How is it measured? Discuss two dimensions of usability with example. (12)

(c) What indirect benefits are offered by Code Review practice in a software development company? Discuss in brief with examples. (9)

6. (a) In the food shop at Lalbagh many BUET students visit to have dinners. There, they have option to choose different types of set-meals. Each has a main item like rice or bread. Along with rice, gravy curries are added. For bread, chicken or beef kebabs are there. Drinks/ juices need to be ordered additionally out of the set-meal if the customer desires to have. Along with the meal, the bill is served and need to be paid before the start of consumption. Draw a class diagram to present appropriate design pattern and write necessary codes so that your code fulfills all the requirements. (7+15)

(b) What do you understand by “Parameterization” in the context of software design? Design a user interface to parameterize the price of product that may vary for different brands, sizes, etc. for a point-of-sales software. (3+10)

7. (a) The requirement specification of a web-based software application stated that maximum 100 users may access simultaneously. After deployment, the application failed to response properly when 90 users accessed at a time. It was recovered later and then on a certain occasion 150 users tried to access and again it crashed. Which two software testing methods could prevent those two failures respectively? (6)

(b) “Uber” and “Pathao” are the popular car based ride sharing applications. They calculate cost based on number of passengers and distance using the following formula:

\[
\text{Uber:} \quad \text{Cost} = n \times d \times 18 \times \text{time\_factor}; \quad \text{where} \ n = \text{number of passengers} \ \text{and} \ d = \text{distance}
\]

- if it is extremely peak hour, then \( \text{time\_factor} = 1.8 \)
- if it is moderately peak hour, then \( \text{time\_factor} = 1.2 \)
- if it is off peak hour, then \( \text{time\_factor} = 0.9 \)

\[
\text{Pathao:} \quad \text{Cost} = n \times d \times 20 \times \text{time\_factor};
\]

- if it is extremely peak hour, then \( \text{time\_factor} = 1.5 \)
- if it is moderately peak hour, then \( \text{time\_factor} = 1.15 \)
- if it is off peak hour, then \( \text{time\_factor} = 0.9 \)

“Uber Moto” and “Pathao Moto” are the popular bike based ride sharing app. They calculate cost based on the distance to destination using of following formula:

\[
\text{Uber:} \quad \text{Cost} = 25 + d \times 12
\]
\[
\text{Pathao:} \quad \text{Cost} = 30 + d \times 11
\]

Contd .......... P/5
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Contd... Q. No. 7(b)

The user will input the destination distance, number of passengers and an input t. (t = 1, 2, 3 for extremely peak, moderately peak and off peak hour respectively.) You need to output the cost for each app. Draw a class diagram to present appropriate design pattern and write necessary codes so that your code fulfils all the requirements.
(c) What is tight cohesion and loose coupling? How does it influence software design? (8)

8. (a) What are the advantages and disadvantages of black-box testing? Discuss performance and regression testing in brief. (4+8)
(b) Assume that there is a blog and users register to that blog for update. When a new article is posted in the blog, it will send update to the registered users saying a new article is posted. Then the user will access the blog and read the new article posted. Draw a class diagram to present appropriate design pattern and write necessary codes so that your code fulfils all the requirements. (5+12)
(c) Show example diagrams of real-world scenario to present Aggregation and Composition in the context of Class Diagram. (6)