L-3/T-1/CSE **Date : 14/01/2017**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2015-2016

Sub : **CSE 307** (Software Engineering and Information System Design)

Full Marks : 280 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. A library keeps records of current loans of books to borrowers. Each borrower is identified by borrower number and each copy of a book by an accession number. The information held about books is the title, author's name/s, publisher's name, publication date, international standard book number (ISBN - a unique book identifier), purchase price, classification (reference or fiction), and number of pages. A given book may be written by a number of different authors. A book may cover a number of different subjects. When a member of the library issues a borrow request, s/he is granted it if the book is available and his/her personal borrowing restriction is not violated. Each member has a restriction of maximum number of books to be allowed to borrow at a time depending on the type of membership, e.g., student/teacher. When a book is borrowed, the return date is automatically recorded based on the current date and the borrower's classification. Other borrowers, pending their return, may reserve books out on loan. Borrowers who hold overdue books or who have reached their loan limit, are flagged to prevent further borrowings. **(15+18+13⅔)**

   (i) Design a **Class** diagram to implement Library system described above.

   (ii) Design **Collaboration** diagram for the book borrowing scenario.

   (iii) Draw a **State** Diagram for an Object of Book class showing the associated actions.

2. (a) Suppose we are designing an Accounting Software. We have a class named **Account** to represent the accounting heads in the chart of accounts. In each transaction one account is debited and at the same time another account is credited. There are classes called **Debtor** and **Creditor** which stores the information which account is debited and which account is credited. An account may have children. The account that does not have any child is called leaf account. An account that has any transaction associated with it cannot be deleted. Also an account which has child cannot be deleted. **(18)**

   Draw the sequence diagram of an account deletion use case where the user is first presented with a list of accounts and user can select one to delete. If the deletion is successful the user will be notified and if it is not possible then the user will be shown a message saying why it is not possible.

   (b) Discuss *white-box* testing in brief. What are the advantages and disadvantages of white-box testing? **(12⅔)**

   (c) Discuss how *confidentially*, *integrity* and *non-repudiation* are implemented for software applications. **(16)**

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3. (a) The requirement specification of a web-based software application stated that maximum 100 users may access simultaneously. After deployment the application failed to response properly when 90 users accessed at a time. It was recovered later and then on a certain occasion 150 users tried to access and again it crashed. Which two software testing methods could prevent those two failures respectively? **(8)**

   (b) Discuss MVC architecture with advantages and disadvantages. What indirect benefits are offered by Code Review practice in a software development company? **(12+10 2/3)**

   (c) If a student gets mark less than 50, s/he gets F grade. For 51-60 s/he gets C, for 61-70 gets B, and for marks obtained more than 70 he received grade A. Mark less than 0 is invalid. Write a java method to implement JUnit testing that will take mark as input and test the program that computes grade with the rule discussed above. Check for all boundary values as well as invalid input. **(16)**

4. (a) A news agency gathers new and publishes them to different subscribers. You need to create a framework for an agency to be able to inform immediately, when event occurs, its subscribers about the event. The subscribers can receive the news in different ways: Emails, SMS, etc. The solution need to be extensively enough to support new types of subscribers (may be new communication technologies will appear). What will be the appropriate design pattern to implement this scenario? Draw the diagram and write Java code to implement the solution. **(20)**

   (b) Briefly discuss eight common bad practices found in software development from the security viewpoint. **(12)**

   (c) What should you keep in mind to avoid merge conflict in version controlling systems? What are the advantages of distributed version control system? **(14 2/3)**

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) What are different layers in software architecture? Briefly explain. **(10)**

   (b) In terms of use-case modeling, define the "extends" relationship with example. **(10)**

   (c) Distinguish between thin client and fat client. **(6 2/3)**

   (d) The Pizza Ordering System: **(20)**

   The Pizza Ordering System allows the user of a web browser to order pizza for home delivery. To place an order, a shopper searches to find items to purchase, adds items one at a time to a shopping cart, and possibly searches again for more items. When all items have been chosen, the shopper provides a delivery address. If not paying with cash, the shopper also provides credit card information. The system has an option for shoppers to register with the pizza shop. They can then save their name and address information, so that they do not have to enter this information every time that they place an order. Develop a use case diagram, for the Pizza Ordering System. The system should allow a user to register and log in, and PaybyCredit, which requires credit card payments.

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6. (a) What is payback analysis? Explain briefly how it works. **(10 2/3)**

(b) Distinguish between distributed and centralized architecture. What are the disadvantages of distributed architecture? **(12)**

(c) Consider the following problem description: **(20)**

A major penal centre (PC) has been built outside the town of Dhaka for keeping prisoners convicted of only one offense of white collar crimes. The prison facility has a constant flow of prisoners into and out of the prison. They are also moving prisoners within the prison based on their good behaviour. On a day to day basis, approximately 136 prisoner changes take place. The changes are processed in the prison control centre office by Control Centre Officer (CCO). Each day, the new prisoner processing division receives the new prisoners, conducts a physical examination, assigns the prisoners to living quarters and sends the information file on the new prisoners to CCO's office. CCO adds information on the new prisoner to a prisoner information database kept on the PC. CCO also updates the prisoner locator log which keeps records of where each prisoner resides. Finally, CCO files the actual folder away in an enormous storehouse of file cabinets which contain information on all prisoners who have ever stayed at Dhaka prison. If a new prisoner is found to have been a previous occupant of Dhaka prison, CCO consolidates both files. As prisoners stay at Dhaka prison, the officials review their behaviour record. Good behaviour or closeness to release time warrant an upgrade in accommodations, usually to minimum security housing. Movement of prisoners to new quarters is done on a weekly basis. Orders are issued to move the prisoners and the move information is sent to CCO. CCO makes these changes in the prisoner locator log and the prisoner information database. CCO also pulls the prisoners long term file and notes good behaviour commendations. A release review and parole board reviews prisoner records on a daily basis and generates a set of prisoners to be released either into the custody of a parole officer or without any restrictions. They notify the prisoner and send an update of the release to CCO's office. CCO removes the prisoner from the prisoner information database and prisoner locator log and update the long-term file of the prisoner to reflect the release.

Draw a data flow diagram for describing the functional requirements of the above system.

(d) What is discovery prototyping? **(4)**

7. (a) What is software validation? Describe the software testing phases with necessary diagram. **(10)**

(b) Discuss about the phase of classic life-cycle model. Write down the advantages of the model. **(10)**

(c) Draw the activity diagram of project planning process. **(10)**

(d) Describe the difference between plan-driven and agile approaches with a diagram. What are the advantages and drawbacks of agile approaches? **(16 2/3)**

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8. (a) The following table sets out a number of tasks of a project, their durations and dependencies. How many days are required to complete the project? Draw a bar chart showing the project schedule. **(16 2/3)**

Task	Duration (days)	Dependencies
T1	10	
T2	15	T1
T3	10	
T4	20	T2, T3
T5	15	
T6	10	T3, T5
T7	20	T3
T8	25	T6
T9	15	T4
T10	5	T5, T9
T11	10	T1, T3, T9
T12	20	T11

(b) Suppose you have got a project to develop a fully functional system within a very short time period. Which process model will you choose to complete such a project? Illustrate the model. What are the factors that may influence you to reject the project offer? **(15)**

(c) Briefly discuss about the risk management process with necessary diagram. Write down the potential indicators for each of the following risk type: **(9+6=15)**

(i) People

(ii) Organizational

(iii) Estimation

L-3/T-1/CSE **Date : 18/01/2017**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2015-2016

Sub : **CSE 305** (Computer Architecture)

Full Marks : 210 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) Consider three different processors P1, P2 and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. **(10)**

(i) Which processor has the highest performance expressed in instructions per second?

(ii) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

(iii) We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

(b) The following table shows the numbers of instructions for a program. **(10)**

Arithmetic	Store	Load	Branch
500	50	100	50

The following table shows the number of cycles taken by each instruction.

Arithmetic	Store	Load	Branch
1	5	5	2

(i) What is the execution time of the program in a 4 GHz processor?

(ii) What is the CPI of the program?

(iii) If the number of load instructions can be reduced by half, what is the speed-up and CPI?

(c) Assume for arithmetic, load/store, and branch instructions, a processor has CPIs of 1, 12, and 5, respectively. Also, assume that on a single processor a program requires the execution of 2.56 billion arithmetic instructions, 1.28 billion load/store instructions, and 256 million branch instructions. Assume that each processor has a 2 GHz clock frequency. Assume that, as the program is parallelized to run over multiple cores, the number of arithmetic and load/store instructions per processor is divided by $0.7 \times p$ (where p is the number of processors) but the number of branch instructions per processor remains the same. (1 billion = 10^9, 1 million = 10^6). **(15)**

(i) Find the total execution time for this program on 1, 2, and 4 processors, and show the relative speedup of the 2, and 4 processors compared to the single processor.

(i) If the CPI of the arithmetic instructions was doubled, what would the impact be on the execution time of the program on 1, 2, and 4 processors?

(iii) How much should the CPI of load/store instructions be reduced for a single processor to match the performance of 4 processors using the original CPI values?

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2. (a) Consider the following information for two different computers. **(5)**

Computer	Number of Instructions	Clock Rate	CPI
A	10 Billion	4 GHz	1
B	8 Billion	4 GHz	1.1

(i) Which has the highest MIPS rating?

(ii) Which is faster?

(b) Consider the following information for load word (lw) instruction **(5)**

Instr.	Instruction Fetch	Register read	ALU op	Memory access	Register write
lw	200 ps	100 ps	200 ps	200 ps	100 ps

Consider the following program:

lw $1, 100($0)
lw $2, 200($0)
lw $3, 300($0)

What is the speedup for the pipelined dadapath over the single cycle datapath for this program? What will be the speedup if we add 2,000, 000 more load word (lw) instructions?

(c) Draw the complete MIPS pipelined datapath and control for load (lw) instruction with pipelined registers. **(10)**

(d) Consider the following C code **(10)**

A = B + C; D = A + E;

All the above are memory instructions. The base address is in register t0 and the offset are A(0), B(4), C(8), D(12), E(16). How many cycles are required to execute the above? Can you reduce the number of cycles using code scheduling? If yes, what will be the resulting number of cycles? Show each step.

(e) "Even with a perfect branch predictor, 1-cycle penalty for a taken branch". Why is that? How to solve this? **(5)**

3. (a) What do you mean by double data hazard? Write down the equations to detect forwarding in MIPS considering double data hazard? How MIPS detect hazard due to the use of load instruction? **(10)**

(b) Briefly explain write-through and write-back scheme for cache? How does write-though and write-back schemes handle write-miss? **(10)**

(c) Briefly explain how page table works with respect to virtual address, physical address, main memory and disk. **(5)**

(d) Though both TLB and data cache are cache memory, how are they different from each other? Explain with flow chart the interaction between TLB and data cache for both read and write operation. **(10)**

Contd P/3

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4. (a) Assume the miss rate of an instruction cache is 3% and the miss rate of the data cache is 5%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 40%. What is the amount of execution time spent on memory stalls? **(5)**

(b) For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache. **(10)**

Tag	Index	Offset
31–10	9–5	4–0

What is the cache block size (in words) and how many entries does the cache have? Starting from power on, the following byte-addressed cache references are recorded.

0, 4, 16, 132, 232, 160, 1024, 30, 140, 3100, 180, 2180

How many blocks are replaced and what is the hit ratio?

(c) Assume there are three small caches, each consisting if four one-word blocks and uses LRU replacement policy. One cache is fully associative, a second is two-way set-associative, and the third is direct-mapped. Find the number of misses for each cache organization given the following two independent sequences of block addresses: **(15)**

0, 2, 4, 8, 10, 12, 14, 16, 0

1, 3, 5, 1, 3, 1, 3, 5, 3

(d) Suppose we have a processor with a base CPI of 1.0, assuming all references hit in the primary cache, and a clock rate of 4 GHz. Assume a main memory access time of 100 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 3%. How much faster will the processor be if we add a secondary cache that has a 5 ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 1%. **(5)**

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE.**

5. (a) Produce the compiled MIPS code for the following C function. Assume that addresses of dest, source in `$a0`, and `$a1`. Use a minimal number of MIPS assembly instructions. **(25)**

```
void rstrcopy (char *dest, char *source)
{
     if (*source)
     {
          *dest++=*source++;
          rcopy (dest, source);
     }
     else
          *dest='\0';
}
```

Contd P/4

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Contd ... Q. No. 5

(b) What is the MIPS assembly code to load this 32-bit constant into register $s0? **(6)**

0001 0000 0011 1101 0000 1001 0000 0000

(c) What do you understand by *pseudoinstructions*? Give two examples of *pseudoinstructions* that MIPS assembler accepts. **(4)**

6. (a) What are the steps of floating point addition? Describe with an example. **(12)**

(b) What are the different addressing modes of MIPS? Describe and illustrate the calculation process for each addressing mode. **(15)**

(c) What is data race? What instructions are available in MIPS to address this issue? How these instructions work? **(8)**

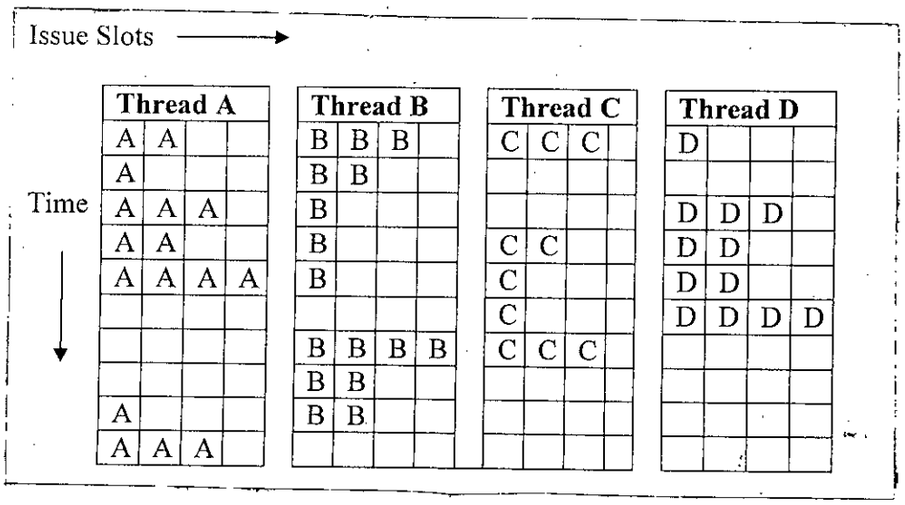
7. (a) Assume that you have four different threads. Show how the four threads could be combined to execute on the processor more efficiently using following three multithreading options: **(15)**

(i) A superscalar with coarse-grained multithreading

(ii) A superscalar with fine-grained multithreading

(iii) A superscalar with simultaneous multithreading

How the four threads would execute independently on a superscalar without any multithreading support is given below.



(b) Find the maximum number of processors each having clock rate i with cache memories that a bus with Bandwidth B can support. **(10)**

(c) What is the use of *Bias* in floating point representation? Give the encoding of floating point `infinity`. **(10)**

Contd P/5

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8. (a) What are the different methods to maintain coherence among all caches and global memory in a shared memory system? Describe briefly. **(10)**

(b) Suppose we want to sum 64,000 numbers on a shared memory multiprocessor computer with uniform memory access time. Let's assume we have 64 (i) UMA processors, (ii) message passing processors. Write the corresponding C code. **(20)**

(a) for each processor to sum their subset of numbers

(b) to add the partial sums

(c) Draw the organization of a message passing multiprocessor. **(5)**

L-4/T-2/CSE **Date : 29/01/2017**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-4/T-2 B. Sc. Engineering Examinations 2014-2015

Sub : **CSE 311** (Data Communication)

Full Marks: 210 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

Give your answer to the point avoiding unnecessary writings.

Try to draw as many figures as possible and explain with block diagrams.

1. (a) Briefly explain the steps required for "Echo Cancellation"? Explain how "Inter-Symbol Interference (ISI)" can occur? **(7+6)**

   (b) Briefly explain the procedure of 4B/5B encoding scheme and intentions behind it. **(10)**

   (c) Show with necessary figures how 4-bit information is passed at a time with 16-QAM (Quadrature Amplitude Modulation). **(6)**

   (d) For a baseband signal of $m(t) = \cos 100t + \cos 400t$ **(6)**

   (i) Draw basic spectrum of $m(t)$

   (ii) Draw spectrum of the modulated signal using Double Side Band with Carrier (DSB+C), where the carrier signal is $2(1+m(t))\cos 1000t$. **(6)**

2. (a) Draw digital signals of the corresponding binary sequence of 1011001 for the following line encoding schemes, **(9+6)**

   (i) Pseudo-Ternary

   (ii) Differential Manchester

   (iii) Multi-transition (MLT)-3

   Summarize each of these in terms of Bandwidth, Baseline wandering, and DC component issues.

   (b) Explain the incoherent demodulation procedure of FM and FSK. Explain how modulations of Phase Shift Keying (PSK) and Quadratic Amplitude Modulation (QAM) relate to each other? **(5+3)**

   (c) Explain how offset QPSK (Quadrature Phase Shift keying) reduces maximum phase shift from π to $\frac{\pi}{2}$ without reducing bit rate. Explain how phase continuation is maintained during MSK (Minimum shift keying). **(6+6)**

Contd P/2

CSE 311

3. (a) Show that, for a real time $f(t)$, the signal $f_{USB}(t) = f(t)\cos\omega_c t - f_h(t)\sin\omega_c t$ represents an upper sideband SSB-SC signal, where $f_h(t)$ represents Hilbert Transform of $f(t)$ and ω_c is the carrier frequency in rad/sec. **(13)**

(b) What is orthogonal signal? Explain the motivations behind making each m-FSK signals orthogonal to each other? Show that the minimum frequency difference to make signal orthogonal is, $\delta_f = \frac{1}{2T_b} Hz$. **(2+4+6)**

(c)What was the fallacy behind the estimation of the bandwidth of Frequency Modulation (FM)? Show that the bandwidth requirement of Wide Band Frequency Modulation (WBFM) is $\approx 2(\Delta f + 2B)\,Hz$, where Δf refers to peak frequency deviation. **(4+6)**

4. (a) Explain with diagram how Phase Locked Loop (PLL) maintains Phase and Frequency synchronization between source and generated carrier signals. **(15)**

(b) For a Vestigial Side Band (VSB) modulation with suppressed carrier, derive following relation between input and output filter, $H_o = \frac{1}{H_i(\omega+\omega_c) + H_i(\omega-\omega_c)}$. **(8)**

(c) Explain with necessary figures and diagrams, the modulation and demodulation techniques of On Off Keying (OOK), Frequency Shift Keying (FSK), and Differential Phase Shift Keying (DPSK). **(4+4+4)**

SECTION-B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) There are two principal forms of digital switching in communication networks, **(10)**
   (i) Circuit switching
   (ii) Packet switching

Big website companies like Facebook and Google store their data in data centers where thousands of computers act together as a single server. Also, they establish multiple data centers in geographically distance locations. That means when you load your Facebook home page, it may be the case that the picture of Aashik Salam, one of your computer science teachers, was downloaded from the Facebook data center at Singapore and the picture of Himel Sen, another of your computer science teachers, was downloaded from the data center at California. However, it is not just the case that only clients communicate with the data center servers, data centers communicate with each other a lot as well. What form of digital switching do these data centers use to communicate with each other?

(b) State and prove the dilation property of the Fourier transform. **(5+5)**

(c) If the Fourier Transform of the signal $g(t)$ is $G(f)$, then determine the Fourier Transform of the signal, $\sin^2(2\pi f_c t)g(t)$. **(10)**

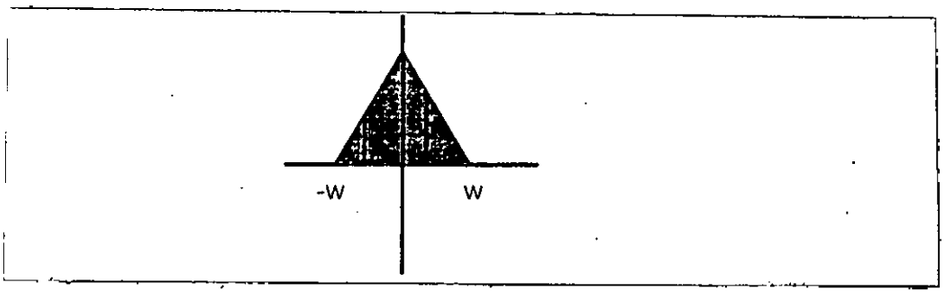
(d) Derive the Fourier Transform of the Dirac Delta Function. **(5)**

Contd P/3

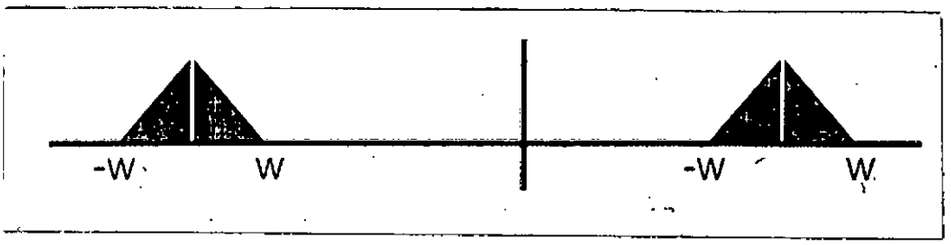
CSE 311

6. (a) Determine the bandwidth of the following two signals. The frequency domain representation of the signals are drawn as follows. Also tell what will be the bandwidth if the diagrams drawn are for time domain representation. **(3+3+4)**

(i) Signal One

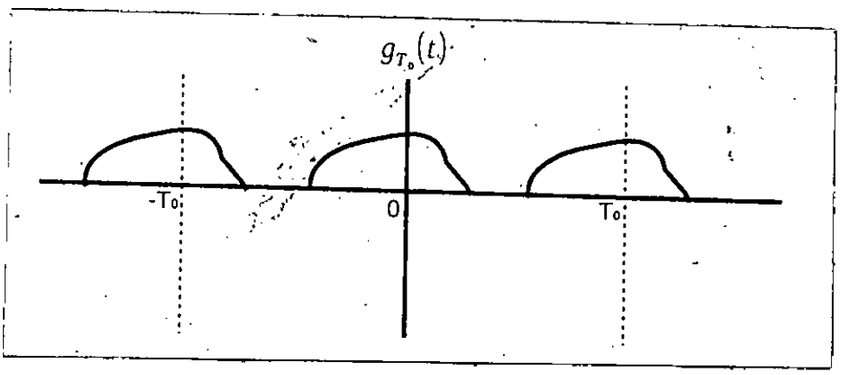


(ii) Signal Two



(b) Derivation of the Fourier Transform of periodic signals are given below. Read the derivation given below and write answer the questions: **(20)**

Let $g_{T_o(t)}$ be a periodic signal with period T_o. The diagram and the definition of $g_{T_o(t)}$ regarding complex exponential Fourier Series are given below,



$$g_{T_o}(t) = \sum_{n=-\infty}^{\infty} c_n \exp(j2\pi n f_0 t) \quad \cdots\cdots (1)$$

where c_n is defined as

$$c_n = \frac{1}{T_0} \int_{-\frac{T_0}{2}}^{\frac{T_0}{2}} g_{T_0}(t) \exp(-j2\pi n f_0 t)\, dt \quad \cdots\cdots (2)$$

Now, a pulse like function $g(t)$ is defined in terms of $g_{T_0}(t)$ as,

$$g(t) = \begin{cases} g_{T_0}(t) & ; -\frac{T_0}{2} \le t \le \frac{T_0}{2} \\ 0 & ; \text{elsewhere} \end{cases} \quad \cdots\cdots (3)$$

Contd P/4

CSE 311

Contd... Q. No. 6(b)

(i) **Why do we need to introduce this new function $g(t)$?** [Given: the Fourier Transform of $g(t)$ if $G(f)$]

(ii) **Also, Draw the time domain diagram of $g(t)$.**

Now c_n can be written as: $c_n = f_0 G(n f_0)$ ..... (4)

(iii) **How can c_n be equal to $f_0 G(n f_0)$?**

Now $g_{T_0}(t)$ can be expressed as:

$$g_{T_0}(t) = \sum_{n=-\infty}^{\infty} f_0 G(nf_0) \exp(j2\pi n f_0 t) \quad \cdots\cdots (5)$$

and the Fourier Transform of $g_{T_0}(t)$ would be,

$$F\left[g_{T_0}(t)\right] = \sum_{n=-\infty}^{\infty} f_0 G(nf_0) F[\exp(j2\pi n f_0 t)] \quad \cdots\cdots (6)$$

(iv) **Why is Fourier Transform only applied to $\exp(j2\pi n f_0 t)$?**

Why is Fourier Transform not applied to the part $f_0 G(nf_0)$?

From this definition we can conclude,

$$F\left[g_{T_0}(t)\right] = f_0 \sum_{n=-\infty}^{\infty} G(nf_0)\delta(f - nf_0) \quad \cdots\cdots (7)$$

(v) **How can we deduce Eq. 7 from Eq. 6?**

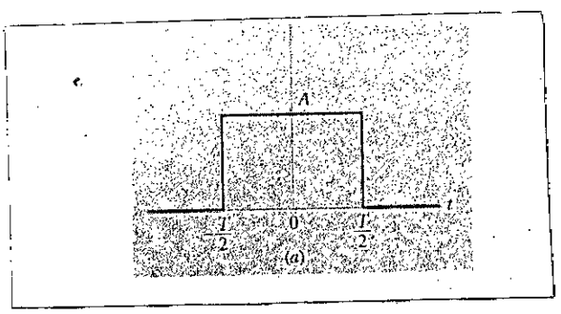
(c) Why is non-uniform quantization needed? What are the problems in case of uniform quantization? **(5)**

7. (a) Write short notes on- **(5+5)**

(i) Linear System

(ii) Time Invariant System

(b) Draw the response of the ideal low-pass filter if the following pulse was given as input. From these two diagrams, explain why this filter is called "ideal" rather than "real"? **(10)**

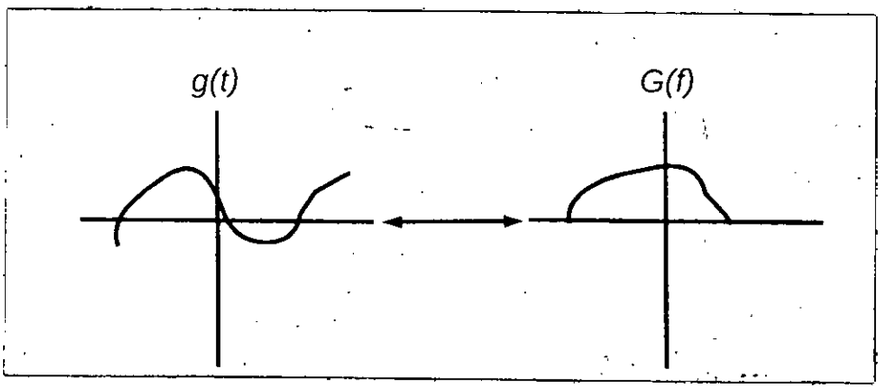


(c) Deduce the recurrence relationship for the Fast Fourier Transform. **(15)**

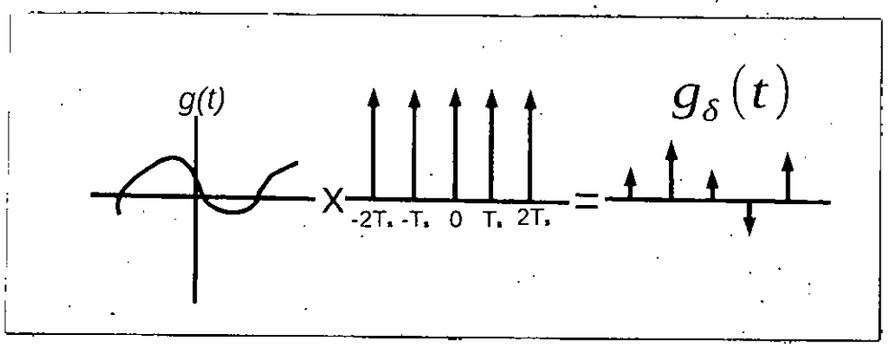
Contd P/5

CSE 311

8. (a) Suppose a Fourier Transform pair signal is given as follows: **(6+3+6)**



The signal is sampled as described in the following figure,



The sampled signal is described as,

$$g_\delta(t) = g(t)\sum_{n=-\infty}^{\infty}\delta(t-nT_s) = \sum_{n=-\infty}^{\infty} g(nT_s)\delta(t-nT_s)$$

Find the Fourier Transform of $g_\delta(t)$. Also draw the diagram of $G_\delta(f)$. From the diagram, explain the sampling theorem.

(b) Draw the block diagram of the regenerative repeater component of Pulse code modulation. Also explain how each of the sub-components work in the regenerative repeater. **(10)**

(c) What are the two types of error in case of delta modulation? Illustrate each of them with figures. Also, describe how these two type of errors can be overcome. **(10)**

L-3/T-1/CSE **Date : 04/02/2017**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2015-2016

Sub : **CSE 303** (Database)

Full Marks: 210 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) A distributed database system consisting of five sites is shown in Figure 1. A transaction, T_1 (Figure 2) has been initiated from site S_1. Data item A is fragmented and stored in sites S_2 and S_4. Data item B is fragmented and stored in sites S_2, S_3 and S_5. Accordingly, any update (write) operation need to be performed to all related sites. **(20)**

   (i) Show all the messages e.g. <Prepare T_1> etc. passing between S_1 (transaction initiator) and the related other sites (S_2, S_3, S_4 and S_5) for phase 1 and phase 2 to COMMIT the transaction T_1 using the two-phase commit protocol.

   (ii) Show all the message passing similar to 1(a)(i) for phase 1 and phase 2 to abort the transaction T_1 because of sending < Abort T_1 > message from S_5 to S_1.

   (b) Figure 3 shows the fixed length record file structure for customer relation. Show the file structure after deletion of records with customer ids C004 and C007 for different file deletion methods. Compare the advantages and disadvantages among different deletion methods as per above. **(15)**

2. (a) Find the equivalent serial schedule for the concurrent schedule shown in Figure 4 by swapping of non-conflicting instructions. **(15)**

   (b) Verify the serial schedule created in 2(a) with the serial schedule created by using precedence graph. **(5)**

   (c) Create lock table for the list of data items and the corresponding locking status of different transactions as given in Figure 5. **(15)**

3. (a) A set of transactions along with their time stamp values and instructions is given in Figure 6(b). The timestamp values of data item A is given in Figure 6(a). Find the status (roll back or executed) of each transaction and the corresponding timestamp values of data item A using the timestamp-based protocol. **(15)**

   (b) Explain Thomas write rule with an example. **(5)**

Contd P/2

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Contd... Q. No. 3

(c) (i) The initial account balance of A_1, A_2 and A_3 are 1000, 2000 and 3000 respectively. Write log records for the transactions given in Figure 7. **(15)**

(ii) Show the log-based recovery if a failure occurs after write (A_3).

(iii) Show the recovery if a failure occurs after write (A_2).

4. (a) Construct the dynamic hash index structure on balance for the relation given in Figure 3. The binary representation of the most significant digit of balance is the hash code on balance. You have to insert records in descending order of balance. **(20)**

(b) (i) Show the final B+ tree index structure for the search key values 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24 with 4 leaf nodes and n = 4. You do not need to create this index in step by step. **(10)**

(ii) Show the index structure after insertion of 15.

(c) Write short note on bitmap indexing. **(5)**

SECTION-B

There are **FOUR** questions in this section. Answer any **THREE**.

Please read carefully, some questions might have additional restrictions.

5. (a) Consider the following relational database schema: **(7×4=28)**

Product (maker, model, type)

PC (model, speed, ram, hd, price)

Laptop (model, speed, ram, hd, screen, price)

Printer (model, color, type, price)

The Product relation gives the manufacturer, model number and type (PC, laptop, or printer) of various products. We assume for convenience that model numbers are unique over all manufacturers and product types; that assumption is not realistic, and a real database would include a code for the manufacturer as part of the model number. The PC relation gives for each model number that is a PC the speed (of the processor, in gigahertz), the amount of RAM (in megabytes), the size of the hard disk (in gigabytes), and the price. The Laptop relation is similar, except that the screen size (in inches) is also included. The Printer relation records for each printer model whether the printer produces color output ('T', if so; 'F' otherwise), the process type (laser or ink-jet, typically), and the price. Write the following SQL queries:

(i) Find those manufacturers that sell Laptops, but not PCs or Printers.

(ii) Find those hard disk sizes that occur in two or more PCs.

(iii) Find those pairs of PC models that have both the same speed and RAM. A pair should be listed only once.

(iv) 'Find the manufacturers of PCs with at least three different speeds.

(v) Find the makers who produce only one type of product.

Contd P/3

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Contd... Q. No. 5(a)

(vi) Find the maker(s) of the cheapest color printer(s).

(vii) Find the PC model with maximum processing speed **without** using any aggregate function.

(b) Consider three tables T1, T2 and T3. Each table has only one column which contains only integers. Suppose the content of the three tables are as follows: **(2+2+3=7)**

T1: 1, 2, 2, 2, 3, 4, 4

T2: 2, 3, 4, 4, 4, 5

T3: 2, 2, 3, 3, 4, 4, 5, 5

Show the values of the following SQL queries:

(i) SELECT * FROM T1 **UNION** SELECT * FROM T2

(ii) SELECT * FROM T1 **MINUS** SELECT * FROM T3

(iii) (SELECT * FROM T1 **UNION ALL** SELECT * FROM T2) **INTERSECT ALL** (SELECT * FROM T3)

6. (a) Consider a relation R(A, B, C, D) and FD's AB→C, BC→D, CD→A, and AD→B. **(12)**

(i) What are all nontrivial FD's that follow from the given FD's? You should restrict yourself to FD's with single attributes on the right side.

(ii) What are all the keys of R?

(iii) What are all the superkeys for R that are not the keys?

(b) Prove that any two-attribute relation is in BCNF. **(7)**

(c) For the relation schema R(A, B, C, D, E) with FD's AB→C, DE→C, and B→D do the following: **(10)**

(i) Indicate all the BCNF violations.

(ii) Decompose the relations, as necessary, into the collections of relations that are in BCNF.

(d) Suppose R is a relation with attributes A1, A2, A3, ..., An. As a function of n, find out how many superkeys R has, if the only keys are {A1} and {A2, A3}. **(6)**

7. (a) Consider the following relational database schema designed for a university database: **(4×4=16)**

Department (<u>name</u>, headID, yearOfEastablishment)

Employee (<u>id</u>, name, address, designation, salary, gender)

(i) Suppose we want to enforce the rule that says "Departmental head must be an employee of the university". Show two ways to implement the above rule: one using a check constraint and the other **without** using any check constraint.

(ii) Write a check constraint to make sure that *no two departments have the same person as Head.*

(iii) Write an assertion to check the rule: *if the Head of the Department's gender is male then his name must not begin with 'Ms'.*

(iv) Write an assertion to check the rule: *the CSE Departmental head's salary must not be less than 1,50,000 Taka.*

Contd P/4

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Contd... Q. No. 7

(b) (i) Consider the following DDL: **(4+4=8)**

```
CREATE TABLE MyTable(
    .....
    gender CHAR(1) NOT NULL,
    .....
    );
```

Replace the above NOT NULL constraint using a CHECK constraint.

(ii) Consider the following DDL:

```
CREATE TABLE MyTable(
    .....
    headID INT UNIQUE,
    .....
    );
```

Replace the above UNIQUE constraint using a CHECK constraint.

(c) What are the three different policies for UPDATE and DELETE that you can mention for maintaining referential integrity? Among these which one is more suitable for UPDATE and which one is more suitable for DELETE? Why? **(6)**

(d) Suppose we want to create a copy of a table R including the schema. Show the DDL to perform such operation. What will be the DDL if we just want to copy the schema and not the tuples of the table R? **(5)**

8. (a) East West Property Development is a construction company of Bashundhara group with over 1000 employees. A customer can hire the company for more than one project, and employees sometimes work on more than one project at a time. Equipment is assigned to only one project. Draw an E-R diagram for this company indicating cardinality. **(7)**

(b) A university has a large number of courses. Each course may have one or more different courses as prerequisites, or may have no prerequisites. Similarly a particular course may be prerequisite of any number of courses or may not be prerequisite of any other courses. Sketch an E-R diagram that includes COURSE as the single entity, including cardinality. Each course has a course number and title. Convert the E-R diagram into relation schema. **(7)**

Contd P/5

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Contd... Q. No. 8

(c) Convert the following E-R diagram into Relation schema: **(6)**

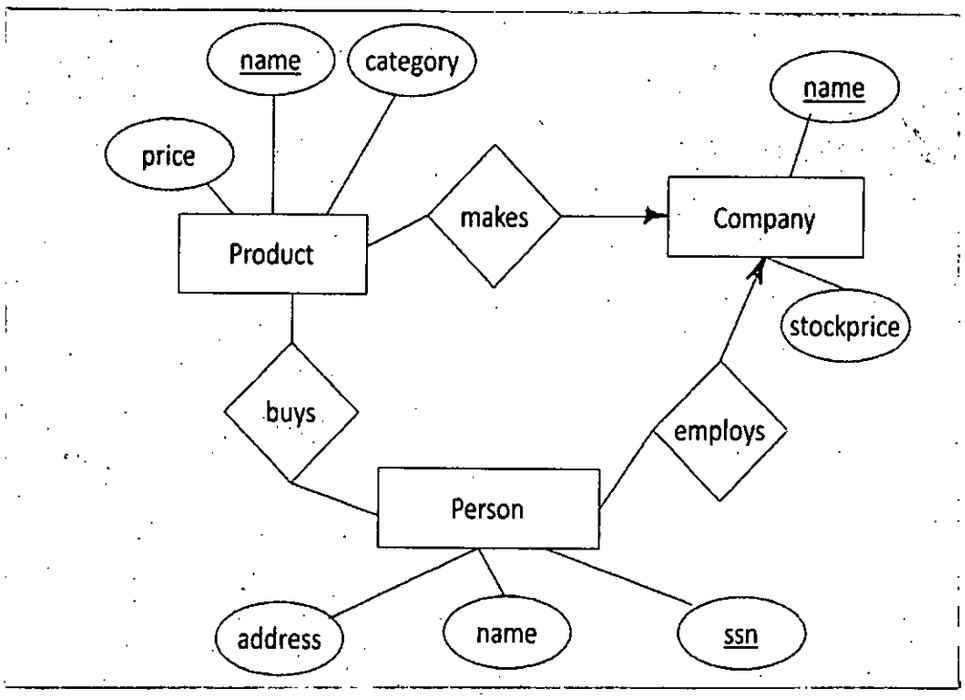

Figure 8: E-R diagram for question 8(c)

(d) Consider a database with the following schema **(4+4+4+3=15)**

Route: flight number (FN), departure city (DC), arrival city (AC), distance in miles (DI), scheduled department time (SD), Scheduled arrival time (Sa), plane model (PM).

Flight: flight number (FN), date (DT), number of passengers (NP), actual department time (AD), actual arrival time (AA).

Plane: plane model (PM), capacity (CA), type (TP).

A snapshot of the database is shown in Figure 9. Translate the following queries into relational algebra:

(i) Which flights have at least 50 passengers on board arrived more than 30 minutes late?

(ii) What are the departure and arrival cities of all flights on October 10th that were completely full?

(iii) What are the plane types that travel between BOSTON (BOS) and FRANCISCO (SFO)?

(iv) Which flights departed late but arrived without any delay?

Contd P/6

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Contd... Q. No. 8(d)

ROUTE

flight number (FN)	from city (FC)	to city (TC)	distance in miles (DI)	scheduled departure time (SD)	scheduled arrival time (SA)	plane (PM)
1384	ROC	BOS	325	0650	0810	F101
1205	BOS	ROC	325	1730	1900	F101
110	BOS	LAX	3250	0900	1040	L1011
398	LAX	SFO	240	1120	1210	757
124	SFO	BOS	3180	1400	2310	L1011
448	BOS	DCA	340	0700	0830	737
540	DCA	BOS	340	1900	2030	737

FLIGHT

flight number (FN)	date (DT)	number of passengers (NP)	actual departure time (AD)	actual arrival time (AA)
1384	2000-10-09	40	0650	0800
1384	2000-10-10	12	0730	0842
1384	2000-10-11	30	0700	0815
1205	2000-10-09	42	1735	1900
1205	2000-10-10	8	1730	1855
1205	2000-10-11	20	1810	1932
110	2000-10-10	403	0940	1115
110	2000-10-11	365	0905	1035
398	2000-10-09	148	1150	1220
398	2000-10-10	95	1125	1210
124	2000-10-09	150	1500	2350
124	2000-10-10	414	1410	2310

PLANE

model (PM)	capacity (CA)	type (TP)
737	120	jet
747	460	jet
757	200	jet
L1011	440	jet
F101	45	prop

Figure 9: A sample snapshot of database for question 8(d)

P.T.O

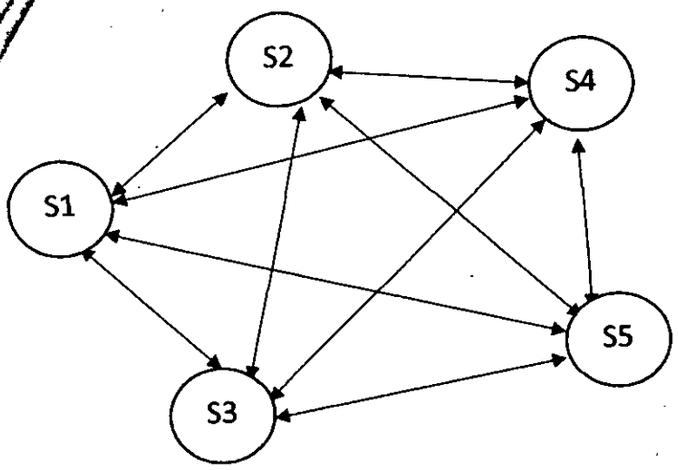

Figure 1: Distributed Database System consisting of five sites

T1	Data replication
READ (A)	Data item **A** is fragmented to S2, S4
READ (B)	Data item **B** is fragmented to S2, S3, S5
WRITE (A)	
WRITE (B)	
COMMIT	

Figure 2: A transaction T1 initiated from S1 of Figure 1.

	Customer Id	Name	street	City	Balance
record 0	C0001	N1	North	Dhaka	1000
record 1	C0002	N2	North	Dhaka	2000
record 2	C0003	N3	North	Dhaka	3000
record 3	C0004	N4	North	Dhaka	4000
record 4	C0005	N5	North	Dhaka	5000
record 5	C0006	N6	South	Dhaka	6000
record 6	C0007	N7	South	Dhaka	7000
record 7	C0008	N8	South	Dhaka	8000
record 8	C0009	N9	South	Dhaka	9000
record 9	C0010	N10	South	Dhaka	10000

Figure 3: File containing *Customer* relation records

P.T.O

T1	T2	T3	T4
READ(A)			
	READ (C)		
READ(B)			
	WRITE (C)		
		READ(C)	
		WRITE (C)	
			READ(B)
			READ(A)
			READ(D)
WRITE (A)			
			WRITE (D)
READ(B)			
		READ(B)	

Figure 4: Concurrent schedule of four transactions

Data item	Hash Value	Transactions obtained lock	Transactions waiting for lock
A	5	T1, T5	T2
S	3	T1, T2	
D	5		T3
F	2	T2	T5
G	2	T2, T3, T4	T1
H	5	T4	

Figure 5: List of data items, corresponding hash values and transactions obtained lock and waiting for lock.

P.T.O

Data Item time stamp	Time stamp value
W-timestamp (A)	10
R-timestamp (A)	20

(a)

Transaction	Timestamp	Instruction
T1	5	READ (A)
T2	15	READ (A)
T3	25	WRITE (A)
T4	12	WRITE (A)

(b)

Figure 6: (a) Timestamp values of data item A
(b) Timestamp values of transactions

T20	T21
READ (A1) A1=A1+100 WRITE (A1) READ (A3) A3 = A3 - 100 WRITE (A3) COMMIT	
	READ (A2) A2 = A2+ 0.1*A2 WRITE (A2) COMMIT

Figure 7: Two serial transactions