Analytical Model and Performance Analysis of Graded Channel Dual Material Double Gate Junctionless Field Effect Transistor with High-k Spacer

by

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CERTIFICATE OF APPROVAL

The thesis titled ***"Analytical Model and Performance Analysis of Graded Channel Dual Material Double Gate Junctionless Field Effect Transistor with High-k Spacer"*** submitted by Raisa Fabiha, Student ID: 0417062212, Session: April 2017 has been accepted as satisfactory in partial fulfillment of the requirements for the degree of ***Master of Science in Electrical and Electronic Engineering*** on 20 July, 2019.

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To My Beloved Parents

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LIST OF ABBREVIATIONS

ITRS	International Technology Roadmap of Semiconductors
CMOS	Complementary Metal-Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Semiconductor
BJT	Bipolar Junction Transistor
IEDM	International Electron Device Meeting
SIA	Semiconductor Industry Association
SRAM	Static Random Access Memory
DRAM	Dynamic Random Access Memory
IRDS	International Roadmap for Devices and Systems
EUV	Extreme Ultraviolet
FDSOI	Fully Depleted Silicon-on-Insulator
LGAA	Lateral Gate-All-Around
VGAA	Vertical Gate-All-Around
M3D	Monolithic-3D
FinFET	Fin Shaped Field Effect Transistor
EPI	Epitaxial wafer
MPU	Microprocessor Unit
SoC	System on Chip
NW	Nanowire
SRB	Strain-Relaxation-Buffer
QW	Quantum Well
SBH	Schottky Barrier Height
WAC	Wrap-Around-Contact
DD	Drift-Diffusion
TFET	Tunneling Field Effect Transistor
JLFET	Junctionless Field Effect Transistor
NCMOS	Negative capacitance MOSFET
SCE	Short Channel Effect

PHEMT	Pseudomorphic High Electron Mobility Transistor
HEMT	High Electron Mobility Transistor
MHEMT	Metamorphic High Electron Mobility Transistor
HBT	Heterojunction Bipolar Transistor
RF	Radio Frequency
AMS	Analog/Mixed Signal
MESFET	Metal-Semiconductor Field Effect Transistor
GMR	Giant Magneto Resistance
MTJ	Magnetic Tunnel Junction
FTJ	Ferroelectric Tunnel Junction
GC-DM-DG-JLFET-SP	Graded Channel Dual Material Double Gate Junctionless Field Effect Transistor with High-k Spacer
UC-DM-DG-JLFET-SP	Uniform Channel Dual Material Double Gate Junctionless Field Effect Transistor with High-k Spacer
ZTC	Zero Temperature Coefficient
SS	Subthreshold Swing
DIBL	Drain Induced Barrier Lowering
QME	Quantum Mechanical Effect

LIST OF SYMBOLS

κ	Scaling factor (constant field scaling)
V_{dd}	Power supply
t_{ox}	Oxide thickness
x_j	Junction depth
N_a	Doping concentration
α	Scaling factor (generalized scaling)
I_{on}	On current
I_{off}	Off current
V_{FB}	Flat-band voltage
V_{TH}	Threshold voltage
V_T	Thermal voltage
V_G	Gate voltage
n	Peak electron concentration
N_D	Doping concentration
V_{DS}	Drain to source voltage
g_m	Transconductance
I_{ds}	Drain current
V_{EA}	Early voltage
A_{V0}	Intrinsic gain
N_{gd}	Doping concentration of the channel area under metal 2
N_d	Doping concentration of the source, drain and channel area under metal 1
L	Channel length
L_s	Length of each spacer
t_{si}	Channel thickness
t_g	Gate thickness
t_{ox1}	Top gate oxide thickness
t_{ox2}	Bottom gate oxide thickness

V_1	Voltage applied to source
V_{gs1}	Voltage applied to top gate (metal 1)
V_{gs2}	Voltage applied to bottom gate (metal 1)
V_{gs3}	Voltage applied to top gate (metal 2)
V_{gs4}	Voltage applied to bottom gate (metal 2)
$\psi_i(x, y)$	2-D source potential in source and drain region
q	Elementary charge
ϵ_{si}	Dielectric constant for silicon
ϵ_{ox1}	Permittivity of top gate oxide (metal 1)
ϵ_{ox2}	Permittivity of bottom gate oxide (metal 1)
ϕ_{ms1}	Work function difference between metal 1 and silicon of top gate electrode
ϕ_{ms2}	Work function difference between metal 1 and silicon of bottom gate electrode
$\phi_1(x, y)$	2-D potential in the channel region under metal 1
V'_{gs1}	Effective top gate bias
V'_{gs2}	Effective bottom gate bias
V_{fb1}	Flat-band voltage of top gate electrode
V_{fb2}	Flat-band voltage of bottom gate electrode
ϕ_s	Work function of silicon
χ_s	Electron affinity
E_g	Bandgap energy
n_i	Intrinsic carrier concentration
C_{ox1}	Capacitance of top gate oxide (metal 1)
C_{ox2}	Capacitance of bottom gate oxide (metal 1)
C_{si}	Capacitance of silicon body
ϕ_{m1}	Work function of metal 1
ϕ_{m2}	Work function of metal 2
ϵ	Dielectric constant of high-k spacer
$\psi_{c1}(x, y)$	2-D potential in source region

$\phi_2(x,y)$	2-D potential in the channel region under metal 2
$\psi_{c2}(x,y)$	2-D potential in drain region
V_{gs}	Gate bias
G_D	Drain output conductance

ABSTRACT

The continuous downscaling of chip size and dimension have led to the innovation of newer, cheaper and more efficient transistors since its first invention in 1947. As predicted by More Moore scaling, the transistor's gate length will be reduced to 5 nm by 2024 and new device structures other than conventional MOSFET and finFET need to be introduced to improve the short channel characteristics and device performance. The researchers have suggested various emerging and potential device structures like tunnel field effect transistor (TFET), junctionless field effect transistor (JLFET), spin field effect transistor (spin-FET), negative capacitance metal oxide semiconductor (NCMOS) etc. In this thesis, the presented work is dedicated to JLFET. In recent years, many research papers and publications have already been done on diverse structures of both symmetric and asymmetric JLFET such as, nanowire, double gate, dual material, stack-oxide, graded channel, inclusion of high-k and dual-k spacer etc. In this thesis, a two-dimensional analytical model for graded channel dual material double gate JLFET with high-k spacer (GC-DM-DG-JLFET-SP) has been proposed by solving two-dimensional Poisson's equation, assuming cubic potential distribution across the channel and considering fringing field effect in spacer region. Though previously, simulation-based performance analysis on similar device has been done, no publication has been reported yet on the development of its two-dimensional analytical model. The derived analytical model of surface potential has later been verified with the published simulated result. After the verification, surface potential, drain current, different short channel characteristics like drain induced barrier lowering (DIBL) and subthreshold swing (SS) and different performance parameters and figure of merits like on/off current ratio, transconductance (g_m), transconductance generation factor (g_m/I_{ds}), drain output conductance (G_D), intrinsic gain (A_{V0}) and early voltage (V_{EA}) of GC-DM-DG-JLFET-SP have been compared with those of uniform channel dual material double gate junctionless field effect transistor with high-k spacer (UC-DM-DG-JLFET-SP). The presented device GC-DM-DG-JLFET-SP shows higher on/off current ratio, better suppression of DIBL and SS and improved G_D while causing degradation of g_m and V_{EA} and very slight degradation of A_{V0}. All performance analysis and comparisons have been done using MATLAB and calculations of performance parameters have been done numerically using the developed two-dimensional analytical model of potential distribution to avoid mathematical complexity.

Chapter 1

INTRODUCTION

The transistors are the basic building blocks of all modern electronic devices. The advancement of science and technology has brought tremendous and revolutionary change in semiconductor industry. This chapter elaborates on the evolution of transistor in last 70 years since its first invention, various approaches taken to meet its growing market demand and possible future prospects to continue the current trend. The last section describes the objective and motivation of this thesis work and also presents literature review in brief.

1.1 ITRS and Current Trends in CMOS Scaling

Following the invention of the first transistor in 1947, semiconductor electronics faced some reliability challenges during 1950s. Undertaking different approaches to reliable circuit miniaturization and device integration in the late 1950s and early 1960s paved way to an emerging dominant design "the integrated circuit". To convince the commercial electronics users of the maturity and cost-effectiveness of integrated circuit technology, Gordon Moore, then R&D Director at Fairchild, mentioned of "cramming more components onto integrated circuits" [1]. Moore's assumption of the number of components per chip doubling every 18 months became known as "Moore's law". Soon, the use of metal oxide semiconductor field effect transistor (MOSFET) replaced the previously used bipolar junction transistor (BJT) because of its advantages in miniaturization, circuit density and manufacturing cost. Thus, the MOS integrated circuits rapidly captured market share through the 1970s.

In the 1970s, IBM corporate researcher, Robert H. Dennard, presented his research work on the scaling of the MOSFET devices at the International Electron Device Meeting (IEDM) in 1972 [2] and published a comprehensive paper on the scaling of the MOS transistor in 1974 [3]. He posited physical dimension, voltage and doping concentration as parameters for scaling and identified challenges of minimum gate oxide thickness, interconnect resistance and non-scaling of the subthreshold slope that arose with continued scaling. "Dennard scaling", named after his name, dominated the semiconductor research and manufacture for the next three decades. The scaling process is performed by three design parameters of a transistor by the

same scaling factor, κ. The scaled down device will have a reduced voltage (V_{dd}/κ), vertical (t_{ox}/κ and x_j/κ) and horizontal (L/κ) dimension and an increased doping concentration (κN_a) which is illustrated in Figure 1.1. Despite the change in those parameters, the intensity of the electric field remains virtually unchanged. For this reason, this scaling method is also known as "constant field scaling".

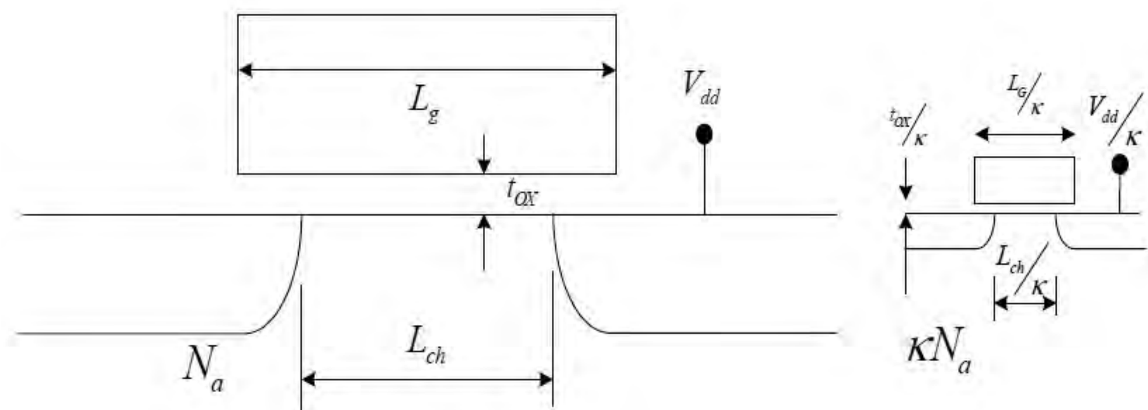


Figure 1.1: Miniaturization of MOSFET according to constant field scaling [3]

For sub-micron devices, two-dimensional short channel effects and drain induced barrier lowering become important factors, the electric field changes significantly and constant field scaling becomes invalid. Brews et al. [4] and Baccarani et al. [5] introduced generalized scaling theory for such devices. Brews et al. considered only the scaling of channel length. It was assumed that channel length could be reduced until a 10% increase in drain current is obtained while the subthreshold characteristics can be maintained [4]. Baccarani et al. concentrated on the scaling of supply voltage and doping concentration. They suggested that these two parameters should be scaled with different scaling factor and for this, they introduced a new scaling constant, α. Based on their theory, the potential will be scaled by α/κ and the electric field by α. The major limitation of the generalized scaling rule is that power density increases by α^2 in deep sub-100 nm scaled devices while the total area scales as $1/\kappa^2$ and the power dissipation per circuit scales as α^2/κ^2, that is, the size of the area scales down faster than the power dissipation [6].

Table 1.1 shows the changes in device dimensions and circuit parameters as a result of both the constant field and generalized scaling rules.

Table 1.1: Summary of the constant field scaling and the generalized scaling rules [3]

Scaled parameters	Constant field scaling	Generalized scaling
Physical dimension (t_{ox}, L, W, x_j)	$1/\kappa$	$1/\kappa$
Doping concentration (N_a, N_d)	κ	$\alpha\kappa$
Power supply (V_{dd})	$1/\kappa$	α/κ
Electric field (E)	1	α
Capacitance (C)	$1/\kappa$	$1/\kappa$
Inversion charge density (Q)	1	α
Circuit delay time ($\tau = CV/I$)	$1/\kappa$	$1/\kappa$
Power dissipation (P)	$1/\kappa^2$	α^2/κ^2
Power density (P/A)	1	α^2
Circuit density	κ^2	κ^2
Chip area (A)	$1/\kappa^2$	$1/\kappa^2$
Current (I)	$1/\kappa$	$1/\kappa$

The organization of the US semiconductor industry, the Semiconductor Industry Association (SIA), launched its first roadmap in 1992. The International Technology Roadmap of Semiconductors (ITRS) is a guiding reference for advanced semiconductor device research and manufacturing purposes. The ITRS has three major contributions [7]:

i. Providing the industry with a common basis for planning through its projections of key technology characteristics and requirements
ii. Assessing critical challenges and potential gaps in capabilities, so that these challenges and gaps may be addressed
iii. Recognizing the existence of interim solutions for the medium-term challenges and limitations

By the late 1990s and early 2000s, the industry began to reckon with many limitations. 1998 ITRS cited three challenges as “roadblocks” with “no known solutions” – dopant clustering, electron tunneling through the gate oxide and dopant distribution [8]. For sub-100 nm devices, Dennard scaling failed to provide the benefits as devices became limited by materials’ shortcomings. As a potential solution to overcome this situation, the industry came up with the

concept of "equivalent scaling" which addressed electron mobility and quantum mechanical effects. In the late 2000s, the ITRS adopted a three-trajectory typology [9]:

i. **More Moore:** Continuing the historical trajectory of performance improvements with continued CMOS evolution (for example, implementation of new device geometries – gate all around transistors and nanowires, integration of new materials for the transistor channel and interconnects and a possible switch to tunnel FETs)
ii. **More-than-Moore:** Heterogeneous functionality integration into the CMOS platform (for example, functional diversification of semiconductor-based devices like sensors, radio-frequency circuits or micro-electromechanical devices)
iii. **Beyond CMOS:** Everything from a new computing element to entirely new computing architectures that are initially CMOS-compatible (for example, emerging research devices)

The ITRS has been under pressure since 2010 because of its "one-dimensional" exponential-growth philosophy. Table 1.2 shows the 2013 edition of ITRS [10]. This ITRS postulated minimum metal half-pitch scaling progress with math formulas that have no correlation with scientific publication and used standard lists of challenges in reaching the scaling projections. In 2013-14, the functional chip products settled at 14 nm for SRAM and Flash, 20 nm for DRAM and 24 nm for processors. The data presented in Table 1.2, 5 nm in 2028 with less than one doping atom in the transistor channel and no large-scale lithography in sight for < 7 nm, are hardly feasible. Intel's 2017 manufacturing day presentation showed lower overall performance characteristics for 10 nm node to be released in 2018 than for 14 nm+ and 14 nm++ nodes released in 2016 and 2017 respectively [9]. So, the performance improvements after 2018 will actually lag the historical trend [11]. As of 2017, the ITRS is no longer updated [12]. Its successor is International Roadmap for Devices and Systems (IRDS).

Table 1.2: Master plan of critical parameters, 2013 edition [10]

Year	2015	2020	2025	2028
Node (nm)	10	4	1.8	?
Logic ½ pitch (nm)	32	20	10	7
2D flash ½ pitch (nm)	15	10	8	8
DRAM ½ pitch (nm)	24	15.5	10	7.7
FinFET ½ pitch (nm)	24	13.5	7.5	5.3
Fin width (nm)	7.2	6.3	5.4	5.0
6T SRAM cell area (nm^2)	6×10^4	2×10^4	6×10^3	3×10^3
NAND flash (b/chip)	128/256 Gb	512 Gb/1T	2T/4T	4T/8T
Flash layers	16-32	40-76	96-192	192-384
DRAM (Gb/chip)	8	24	32	32
Wafer diameter (nm)	300	450	450	450
V_{DD} (V)	0.83	0.75	0.68	0.64
CV/I (ps)	0.65	0.5	0.4	0.3

1.2 Challenges of CMOS Scaling

According to International Roadmap for Devices and Systems (IRDS), "Die cost reduction has been enabled so far by concurrent scaling of poly pitch, metal pitch and cell height scaling. This (will likely) continue until 2024 [13]." It is also projected that physical channel length would saturate around 12 nm due to worsening electrostatics and contacted poly pitch would saturate at 24 nm. The challenges that are faced in conventional scaling of the devices are [14-16]:

i. Transistor leakage current and interconnect delay across a chip have continued to worsen.
ii. Commercially available transistors are close to the physical limits for subthreshold slope.
iii. Leakage power has become a substantial portion of the total power consumption which has limited the benefits of further scaling.

iv. The increasing complexity of designing leading-edge chips and delays in integrating EUV lithography have caused slowing of improvements and also increased cost per transistor.

Table 1.3 shows chips approach and physical size challenges (marked in yellow) starting in 2021. This shows the technology capability. On top of pitch scaling, there are other elements such as cell height, vertical integration, fin depopulation etc. which define the target area scaling.

Table 1.3: Device architecture and ground rules roadmap for logic device technologies [17]

Year of Production	**2015**	**2017**	**2019**	**2021**	**2024**	**2027**	**2030**
Logic industry "Node Range" labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET, FDSOI	finFET, FDSOI	finFET, LGAA	finFET, LGAA, VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
Logic device ground rules							
MPU/SoC metal ½ pitch (nm)	28	18	12	**10**	**6**	**6**	**6**
MPU/SoC metal ½ pitch (nm)	28	18	12	**10**	**6**	**6**	**6**
Contacted poly half pitch (nm)	35	24	21	**16**	**12**	**12**	**12**
L_g: Physical gate length for HP logic (nm)	24	18	14	**10**	**10**	**10**	**10**
L_g: Physical gate length for LP logic (nm)	26	20	16	**12**	**12**	**12**	**12**
Channel overlap ratio – two sided	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Spacer width (nm)	12	8	6	**5**	**4**	**4**	**4**
Contact CD (nm) – finFET, LGAA	22	14	16	**12**	**11**	**11**	**11**
Device architecture key ground rules							
FinFET fin half-pitch (new) – 0.75 or 1.0 M0/M1 (nm)	21	18	12				
FinFET fin width (nm)	8	6	6				
FinFET fin height (nm)	42	42	42				
Footprint drive efficiency – FinFET	2.19	2.50	3.75				

Year of Production	2015	2017	2019	2021	2024	2027	2030
Lateral GAA lateral half-pitch (nm)			12	10			
Lateral GAA vertical half-pitch (nm)			12	9			
Lateral GAA diameter (nm)			6	6			
Footprint drive efficiency – lateral GAA, 3x NWs stacked			2.4	2.8			
Vertical GAA lateral half-pitch (nm)				10	**6**	**6**	**6**
Vertical GAA diameter (nm)				6	**5**	**5**	**5**
Footprint drive efficiency – vertical GAA, 3x NWs stacked				2.8	**3.9**	**3.9**	**3.9**
Device effective width (nm)	92	90	56.5	56.5	**56.5**	**56.5**	**56.5**
Device lateral half-pitch (nm)	21	18	12	10	**6**	**6**	**6**
Device width or diameter (nm)	8	6	6	6	**5**	**5**	**5**

1.3 Various Approaches of CMOS Scaling

According to “More Moore” topology, to overcome the challenges of performance and power consumption, new device geometries and new materials for transistor channel and interconnects can be introduced to continue the industry’s historical trend of shrinking devices and chips. As projected by IRDS, FinFETs will dominate and sustain in the industry until 2021 for high performance logic applications. After that, a potential transition to gate-all-around (GAA) and vertical nanowire transistors will be required since it will not be possible to scale down the gate length and fin width of FinFETs anymore.

Table 1.4 shows that new materials will be needed to improve performance and for lower power consumption as chip size scales down in future.

Table 1.4: Device roadmap enabling More Moore scaling [17]

Year of Production	**2015**	**2017**	**2019**	**2021**	**2024**	**2027**	**2030**
Logic industry "Node Range" labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET, FDSOI	finFET, FDSOI	finFET, LGAA	finFET, LGAA, VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
Device architecture and modules							
Starting substrate	Si, SOI	Si, SOI	Si, SOI, SRB, QW	Si, SOI, SRB, QW	Si, SOI, SRB, QW	Si, SOI, SRB, QW	Si, SOI, SRB, QW
N-channel	Si	s Si	s Si, Ge	s Si, s Ge, III-V	s Si, s Ge, III-V	s Si, s Ge, III-V	s Si, s Ge, III-V
P-channel	Si	Si, SiGe	Si, SiGe	Si, SiGe	Ge	Ge	Ge
Channel formation	Etch	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI
Contact material	Silicide	Low-SBH	Low-SBH	Low-SBH	Low-SBH	Low-SBH	Low-SBH
Contact integration	EPI	EPI	EPI,WAC	WAC	WAC	WAC	WAC
Device performance boosters							
Main performance booster	SCE, Fin height, V_t	SCE, Fin height, V_t	Parasitics, fin height	Parasitics, fin height	Low V_{dd}, 3D	Low V_{dd}, 3D	Low V_{dd}, 3D
Scaling focus	Perf	Power	Power	Power	Function	Function	Function
Channel strain	Yes	Yes	Yes	Yes	Yes	Yes	Yes
S/D strain	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Transport scheme	DD	Quasi Ballistic	Quasi Ballistic	Ballistic	Ballistic TFET, JLFET, NCMOS	Ballistic TFET, JLFET, NCMOS	Ballistic TFET, JLFET, NCMOS, Spin

1.3.1 Process Integration, Devices and Structures

New and emerging technologies for process integration, devices and structures will be adopted by semiconductor industry as suggested by experts.

i. **Multi-gate transistors:** The scaling of planar transistors has become more difficult due to degradation of electrostatics and short channel effects. The multiple number of gates surrounding the channel allows to suppress the off-state current, enhance on-state current and thus improving on/off current ratio. It also results in lower power consumption in subthreshold region and enhances the device performance [18]. Figure 1.2 shows various types of multi-gate transistors [19].

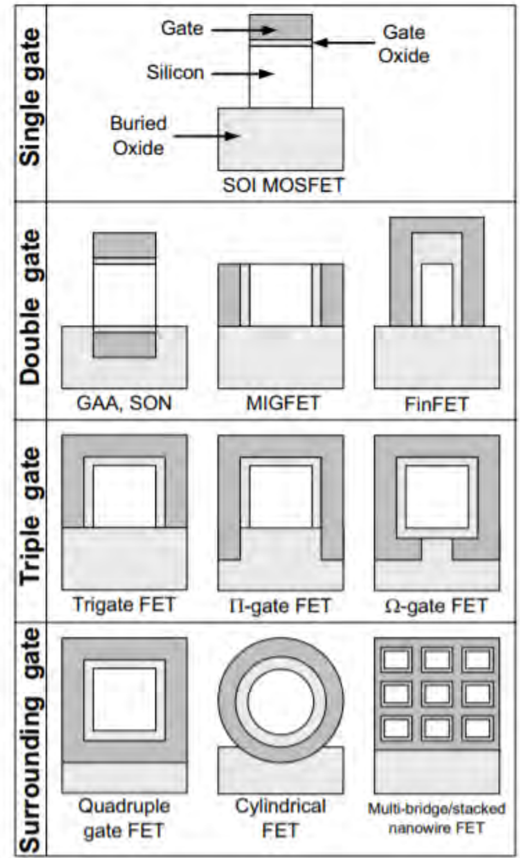


Figure 1.2: Various multi-gate transistors [19]

ii. **Gate insulators with high dielectric constant:** With the continued scaling of chip size, the thickness of the oxide layer is shrunk to maintain adequate capacitance. But it leads to electrical leakage and excess heat. To solve this problem, Intel introduced high-k oxide as the replacement of conventional silicon dioxide along with metal gate

electrode (as shown in Figure 1.3) for 45-nm transistor because high-k oxide such as hafnium oxide is not compatible with silicon gate [20].

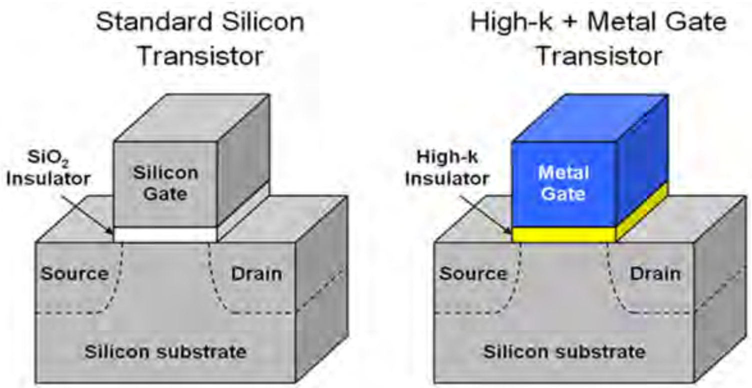


Figure 1.3: Incorporation of high-k insulator in oxide layer [20]

iii. **III-V materials for transistor channels:** The III-V compound semiconductors are obtained by combining group III materials (Al, Ga, In) with group V materials (N, P, As, Sb). Gallium arsenide (GaAs), gallium nitride (GaN), indium phosphide (InP), zinc selenide (ZnSe) and silicon carbide (SiC) are some typical III-V materials used as transistor channels. Inclusion of III-V material in transistor channel offers following advantages [21]:

   a. It provides with higher carrier mobility and intensive heat owing capacity and lowers noise induced device degradation.
   b. It has ultrahigh speed switching capability at very low supply voltage.
   c. It is very promising in the applications of process and integration development such as gate stack, low resistance contact, self-aligned process etc.

1.3.2 Interconnects

The goal for interconnects on-chip is Tb's per second at the energy level of fJ/b [10]. As noted in 2013 edition of ITRS, the energy levelled off at ~1 pJ/b and air gaps in NAND flash was introduced. The 3D integration is also suggested as a potential solution regarding through-silicon vias [10].

1.3.3 Radio Frequency and Analog/Mixed-Signal Technologies

Recognizing wireless application as a new system driver, ITRS formed Radio Frequency and Analog/Mixed Signal Wireless Technology Working Group (RF and AMS TWG) in 2003. Figure 1.4 shows that Si and SiGe dominate below 10 GHz and III-V compound semiconductors GaAs PHEMT, InP HEMT, GaAs MHEMT, GaN HEMT, InP HBT and SiGe HBT dominate above 10 GHz technology. In coming years, instead of this prevailing trend, the future boundaries will be dominated by noise, output power, power added efficiency, linearity and cost [22]. The 2005 RF and AMS chapter focused on CMOS, bipolar, passive and power amplifiers for 0.8 to 10 GHz applications and mm-wave for 10 to 100 GHz applications [23].

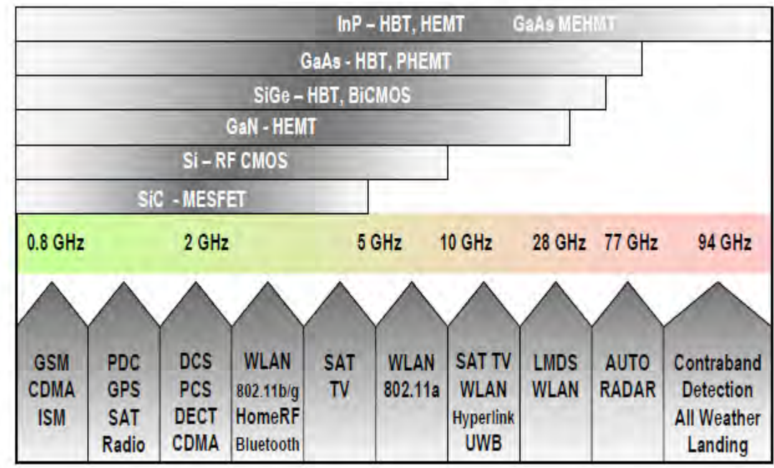


Figure 1.4: Wireless communication application spectrum [22]

1.3.4 New and Emerging Devices

Following the concept of More Moore, the future semiconductor industry might switch to new device structures like tunnel field effect transistor (TFET), junctionless field effect transistor (JLFET), high electron mobility transistor (HEMT), metal-semiconductor field effect transistor (MESFET), MoS_2 transistor, spintronics etc. for continuing further downscaling of chip size and dimension.

i. **Tunnel field effect transistor (TFET):** TFET is a p-i-n diode which functions as a transistor when operated in reverse bias condition. Its output current depends on band-to-band tunneling which is responsible for switching mechanism. Though TFET suffers from ambipolar behavior, lower on-state current and poor RF performance, it provides

lower off-state current and subthreshold swing of less than 60 mV/decade [24]. To improve its switching capabilities and performance, various new TFET structures such as double gate TFET, dielectric pocket TFET, dual material gate charge-plasma based TFET, hetero gate dielectric TFET, source pocket TFET and multi-fin TFET have been proposed. TFET has proved to be very promising as an energy efficient switch. A simple TFET structure is shown in Figure 1.5 [25].

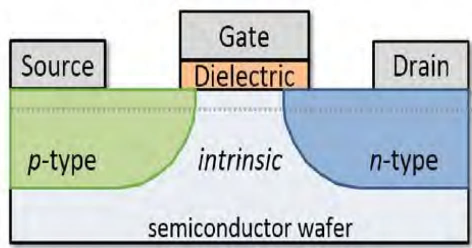


Figure 1.5: Structure of TFET [25]

ii. **Junctionless field effect transistor (JLFET):** As the transistor lengths are scaled down to 10 nm, it becomes challenging to form p-n junction because of extremely high doping concentration, low thermal budget processing and flash annealing technique [26]. To overcome this challenge, a new device structure was proposed based on Lilienfield's first transistor architecture [27] which is called junctionless transistor which is shown in Figure 1.6 [28]. It is a simple resistor with no p-n junction and same doping concentration in the source, channel and drain. During on-state, it has large current due to high doping concentration and during off-state, it becomes fully depleted to ensure fully off device. Studies on different structures of JLFET such as bulk planar, double gate, silicon-on-insulator, stack oxide have been conducted.

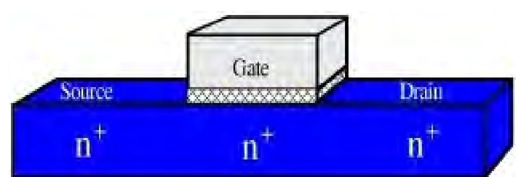


Figure 1.6: Structure of JLFET [28]

iii. **High electron mobility transistor (HEMT):** High transconductance is necessary for fast switching and large signal to noise ratio and depends on current conduction and drift of the majority carrier. So, carrier mobility is a key concern for designing

amplifiers and switching devices which led the invention of high electron mobility transistor (HEMT). HEMTs are essentially heterojunctions having dissimilar bandgaps. The wide band element is doped with donor atoms and has excess electrons in conduction band which diffuse to the adjacent narrow band material's conduction band with lower energy and are pushed back to wide band element's conduction band due to electric field. This process continues until electron diffusion and electron drift balance each other. The fact that the charge carriers are majority carriers yields high switching speeds and the fact that the low band gap semiconductor is undoped means that there are no donor atoms to cause scattering and thus yields high mobility [29]. In recent years, larger band gap and higher breakdown voltage are given priority to high carrier mobility for future use in the high temperature and high power applications [30]. The studies on GaN have also been done for LED and laser applications [31] and its HEMT structure is shown in Figure 1.7.

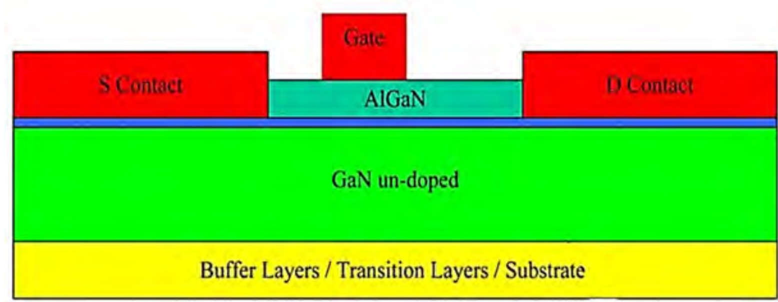


Figure 1.7: Structure of HEMT [32]

iv. **Spintronics:** As the future gate length becomes 5 nm, off current leakage will be too high and spintronics will emerge as a potential solution as indicated by Table 1.4 [17]. Spintronics exploits the influence of electron spin on the electrical conduction. Spin is a pseudo vector quantity which has a fixed magnitude of $h/4\pi$ with a variable polarization. In this case, switching is accomplished by flipping the polarization of spin without any change in flow of current which results in significant energy saving. Spin valve, giant magneto resistance (GMR), magnetic tunnel junction (MTJ), ferroelectric tunnel junction (FTJ), spin-FET and spin MOSFET are some of the active and passive low power spintronics technologies [33]. Organic spintronics is another area of research which has great potential since the organic materials are cheap, light weight, chemically interactive and mechanically flexible and the incorporation of the concept of spintronics allows the non-volatility in device [34, 35].

1.4 Objective and Motivation of the Present Work

More Moore topology focuses on “equivalent scaling” of transistors to solve the problems accrued from continued scaling of chip size and dimension. Extensive researches are going on to invent new device structure and to integrate new materials for the transistor channel and interconnects. According to Table 1.4, tunnel field effect transistor (TFET), junctionless field effect transistor (JLFET) and negative capacitance (NC) MOSFET will occupy the semiconductor industry after 2024. In this thesis, the main focus has been drawn to JLFET.

JLFET was first invented by Tyndall National Institute in Cork, Ireland [36]. This transistor has no p-n junction, thus avoiding the complexity arose during the formation of ultrashallow junction in the case of submicron devices. Instead, it uses a control gate around a silicon nanowire to carry the current and the current flow is controlled by “electrical squeezing effect.” JLFET also offers lower leakage current, high I_{on}/I_{off} ratio and less subthreshold slope [37]. Despite its nature of better scalability and lower thermal budget, JLFETs suffer from lesser drain current, lesser transconductance and subthreshold leakage [38-40]. The Tyndall team led by Jean-Pierre Colinge was also able to fabricate this transistor with only a few dozen atoms in diameter using electron-beam lithography technique.

In recent years, various junctionless architectures like bulk planar, SOI, double gate, tunnel, gate all around, stack-oxide, dual material and graded channel have been reported to improve its performance [40-53]. Double gate architecture has been commenced to increase the gate controllability over the channel region [37, 43]. Dual material gate structure has been introduced for improved carrier transport efficiency, transconductance and drain output resistance [48]. Graded doping concentration and incorporation of high-k spacer improves the off-state current and thus suppresses the subthreshold leakage significantly [40, 48-50]. Combining these multiple structures, many models such as double gate JLFET with high-k spacer, dual material double gate with high-k spacer, graded-doping channel double gate JLFET, graded channel dopingless JLFET with dual-k spacer and graded channel dual material double gate JLFET have also been developed and simulated for enhanced analog/RF performances [37, 48, 50-52].

In this thesis work, performance of graded channel dual material double gate junctionless field effect transistor with high-k spacer (GC-DM-DG-JLFET-SP) has been analyzed. The objectives of this thesis work are:

i. To develop a two-dimensional analytical model for GC-DM-DG-JLFET-SP
ii. To verify our derived model with the model presented in the paper written by V. Pathak and G. Saini [52]
iii. To simulate the device and observe its drain current versus gate voltage characteristic, short channel effects and analog/RF performance
iv. To compare the performance of the device with that of uniform channel dual material double gate junctionless field effect transistor with high-k spacer (UC-DM-DG-JLFET-SP)

In order to formulate analytical model, two-dimensional Poisson's equation will be solved in the channel region using cubic approximation with appropriate boundary conditions. Drain current versus gate voltage characteristics and various parameters defining the short channel and analog/RF performances are numerically calculated using MATLAB to avoid extensive mathematical complexity arising from potential model. Finally, all these performance parameters of GC-DM-DG-JLFET-SP will be compared with those of UC-DM-DG-JLFET-SP.

Chapter 2

THEORY OF JUNCTIONLESS TRANSISTOR

Junctionless transistor, also called gated resistor, has no junction and no doping concentration gradient. Beside overcoming the limitation of fabrication, junctionless transistor ensures better gate controllability, larger current drive and better immunity against short channel effects. This chapter is devoted to the theoretical background and operational principle of junctionless transistor.

2.1 Simplified Fabrication Process

Due to scaling down of CMOS technology node, the devices are becoming smaller, faster and cheaper offering increased number of functionalities. But with the decreasing of feature size, channel length is getting smaller and the distance between source and drain is also getting reduced which results in loss of gate controllability over channel and increase in leakage current. Moreover, the formation of ultrashallow junction has become extremely challenging because of laws of diffusion and statistical nature of the distribution of the doping atoms in the semiconductor [53]. To achieve shallow junction, extremely low energies are required which causes low extraction current and longer implantation time. Light ions with lower energy also cause buried damage which leaves defects. Channeling also occurs during fabrication which affects final junction depth [54].

On the contrary, fabrication process of junctionless transistor avoids the formation of shallow junction. Two key features of fabricating junctionless transistor are [53]:

i. The formation of thin and narrow semiconductor such that it allows full depletion of carriers when the device is turned off
ii. The heavy and uniform doping of semiconductor throughout the device which allows a decent current flow when the device is turned on

These two features ensure improved off-state current in subthreshold regime and thus increasing on/off current ratio which is an important figure of merit of a device.

2.2 Conduction Mechanism

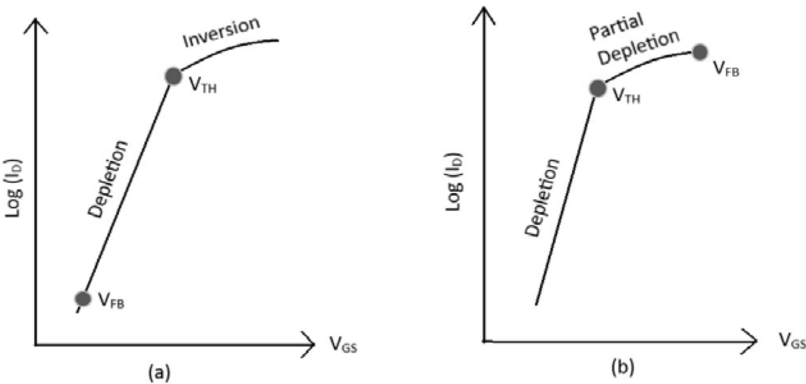


Figure 2.1: Drain current (log scale) as a function of gate voltage in (a) inversion-mode MOSFET and (b) junctionless transistor [53]

Figure 2.1 shows drain current vs. gate voltage characteristic curves for inversion-mode MOSFET (N^+PN^+) and junctionless transistor ($N^+N^+N^+$). For inversion-mode MOSFET, below flatband voltage, V_{FB}, the body is p-type neutral and the device is in off-state. As the gate voltage is increased, the holes are pushed away from oxide-semiconductor interface and a negative space charge region or depletion region is created. Thus, above flatband voltage and below threshold voltage, V_{TH}, the body is fully or partially depleted and the device is off. Above threshold voltage, more negative charges are accumulated, an n-type layer is formed, a channel is created between source and drain and the device becomes turned on. Figure 2.2 illustrates these different states.

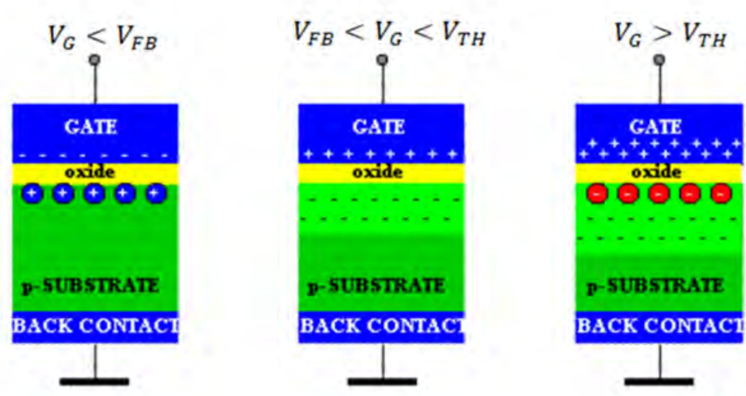


Figure 2.2: Different states of conduction of inversion-mode MOSFET for accumulation ($V_G < V_{FB}$), depletion ($V_{FB} < V_G < V_{TH}$) and inversion ($V_G > V_{TH}$) [55]

For junctionless transistor, the device is fully depleted below threshold voltage, V_{TH}. As gate voltage is increased, the electron concentration in the channel increases. At threshold voltage, peak electron concentration, n, becomes equal to the doping concentration, N_D. Above threshold voltage, the diameter of this region, where $n = N_D$, increases as the gate voltage increases. At flatband voltage, V_{FB}, the entire cross section of the device becomes neutral. Thus, junctionless transistor follows volume conduction mechanism whereas inversion-mode MOSFET follows surface conduction mechanism. Above flatband voltage, charge carriers are accumulated under oxide-semiconductor interface which is not desirable because it causes surface roughness scattering and also reduces the mobility of the carriers and hence the maximum output current. The electron concentration contour plots for these different states are shown in Figure 2.3.

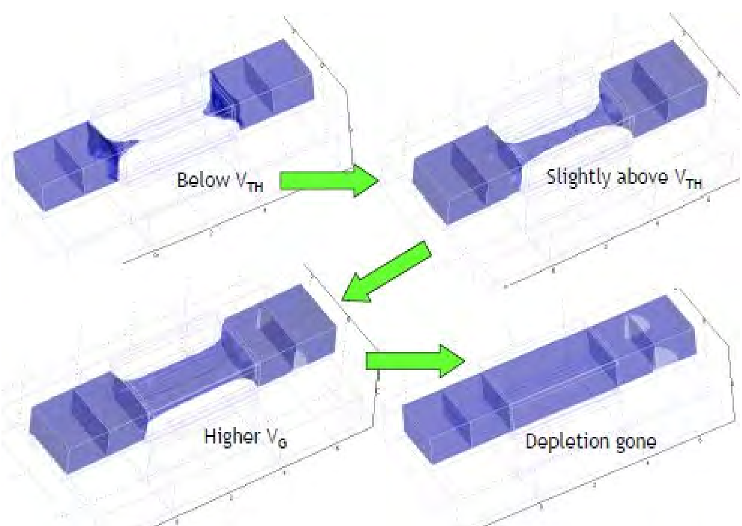


Figure 2.3: Electron concentration contour plots in an n-type junctionless transistor (V_{DS} = 50 mV) for $V_G < V_{TH}$, $V_G = V_{TH}$, $V_G > V_{TH}$ and $V_G = V_{FB} >> V_{TH}$ [56]

2.3 Temperature Dependence and Mobility

In inversion-mode MOSFET, the threshold voltage decreases and the drain current increases with the increase in temperature. But at the same time, due to the effect of phonon scattering, mobility decreases which tends to decrease drain current [57, 58]. As a result, a gate bias point called "zero temperature coefficient (ZTC)" exists at which these multiple effects compensate

one another [59]. In contrast, the mobility of junctionless transistor is relatively insensitive to phonon scattering [53]. So, current increases in monotonous manner with the increase in temperature.

The electron mobility depends on two factors: electric field and doping concentration. In inversion-mode MOSFET, vertical electric field increases with the decrease in effective oxide thickness and hence, mobility decreases [60]. But in junctionless transistor, the channel is formed in the center of the device and the electric field perpendicular to the current flow is very small. So, mobility is not expected to decrease as the effective oxide thickness decreases [61]. Another factor on which mobility depends is doping concentration. It is observed from Figure 2.4 that the mobility drops from 1400 cm^2/Vs in lightly doped silicon to 80 cm^2/Vs for $N_D = 10^{19}$ cm^{-3} and it does not significantly degrade any further as the doping concentration is increased beyond 10^{19} cm^{-3} [62].

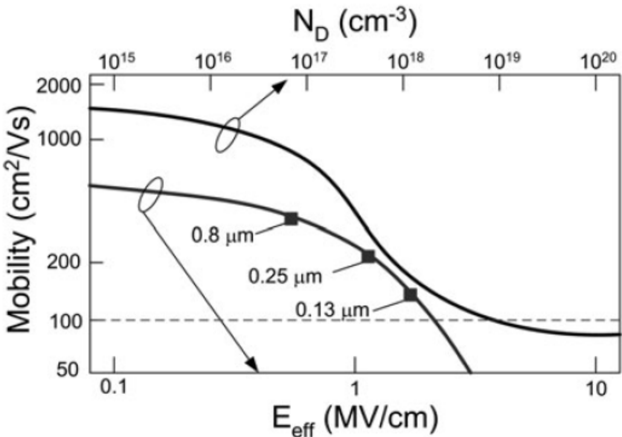


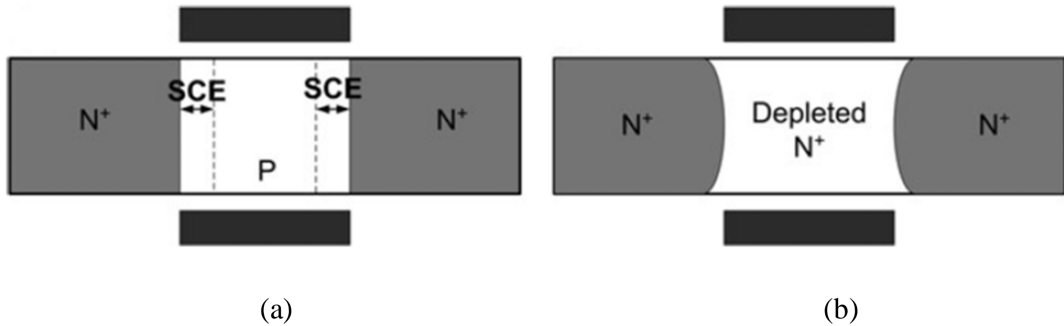
Figure 2.4: Electron mobility in silicon as a function of donor doping atom concentration and as a function of electric field in the channel [62]

2.4 Device Performance

The device performance is determined by its short channel characteristics and analog performances. For very short channel devices, junctionless transistor exhibits improved short channel characteristics, analog performances and also reduces source to drain direct tunneling in comparison with inversion-mode MOSFET due to better electrostatic integrity and gate controllability of channel.

2.4.1 Short Channel Characteristics

The distance between source and drain is called physical gate length. The effective gate length is, in general, equal to the physical gate length. The statistical distribution of doping impurities causes the variation of effective gate length from device to device [63]. This variation is also corelated to ion implantation and diffusion process. In inversion-mode MOSFET, dopants from drain and source can scatter in the channel region and thus the effective gate length decreases which causes short channel effects. In junctionless transistor, there is no gradient of doping concentration between source, channel and drain and thus no dopant diffusion from drain and source occurs. Moreover, the electrostatic squeezing effect causes the distance between non-depleted source and drain to be larger than the physical gate length [64]. Thus, short channel effects improve in junctionless transistor. These two phenomena are illustrated in Figure 2.5.



(a) (b)

Figure 2.5: Illustration of effective gate length in (a) inversion-mode MOSFET and (b) junctionless transistor [53]

The decrease of threshold voltage with decreased channel length is called “threshold voltage roll-off” which is an important short channel effect for any device. It has been observed that threshold voltage of a junctionless transistor is more sensitive to channel doping and silicon film width and less sensitive to channel length variation compared to those of inversion-mode MOSFET [28, 65, 66].

Another important measure of device performance is on/off current ratio. Since junctionless transistor is a heavily doped device and channel resistivity decreases with increased amount of doping, it ensures larger current drive in on-state compared to inversion-mode MOSFET. Again, this device becomes fully depleted in off-state. Thus on/off current ratio improves in the case of junctionless transistor.

2.4.2 Analog Performances

With the scaling down of device dimension, the short channel effect tends to degrade the analog performances. The figure of merits for analog performance are transconductance (g_m), early voltage (V_{EA}), transconductance to current ratio (g_m/I_{ds}) and intrinsic current gain (A_{V0}). It is observed that junctionless transistor shows smaller g_m/I_{ds}, larger V_{EA} and larger A_{V0} [38]. Among these, g_m/I_{ds} and V_{EA} indicate the efficiency of device to convert dc power into ac frequency. Since junctionless transistor has larger current drive, it shows smaller g_m/I_{ds} compared to inversion-mode MOSFET. On the other hand, V_{EA} depends on fin width and an increase in width increases device characteristic length which reduces V_{EA}.

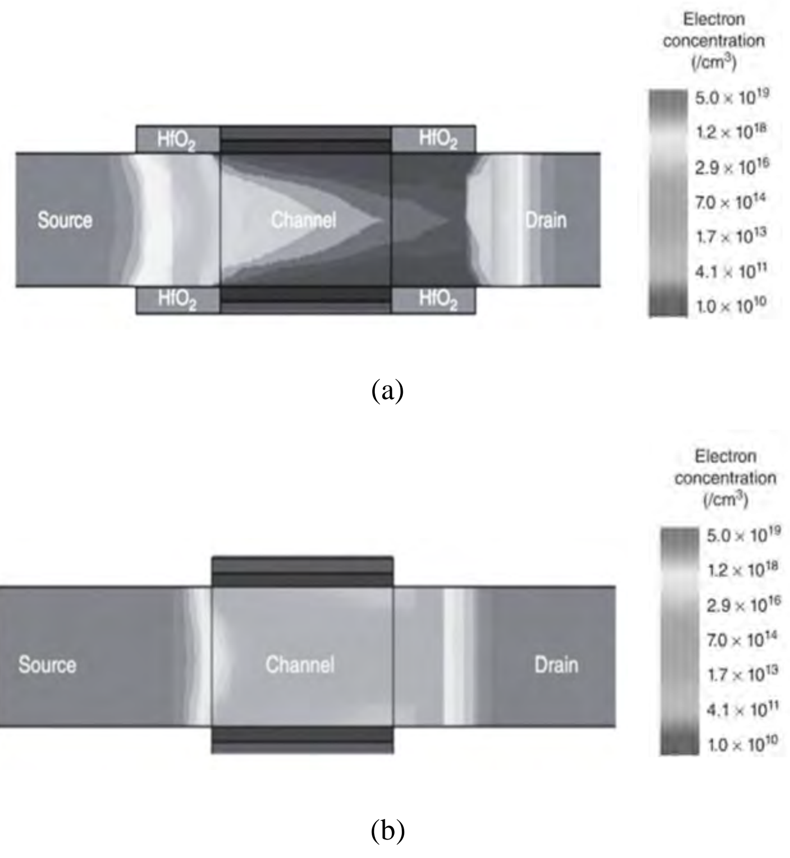
2.5 Key Features of Graded Channel Dual Material Double Gate Structure with High-k Spacer

Various gate engineering technologies have been proposed to improve performance of junctionless transistors. Double gate engineering technique is introduced for suppressing short channel effects by device geometry and a thin silicon channel leading to tight coupling of gate potential with channel potential [43, 67, 68]. These features provide some advantages including a shorter allowable channel length compared to bulk FET, a sharper subthreshold swing (60 mV/dec compared to >80 mV/dec for bulk FET) and better carrier transport as the channel doping is reduced. The dual material gate structure offers improved carrier transport efficiency, transconductance and the drain output resistance compared to single material gate devices [69-71]. Carrier transport efficiency depends on average electron transport velocity and electric field distribution along the channel [69]. The electrons move relatively faster near drain region than source region [72]. By adjusting metal work functions and channel potential, electric field distribution can be controlled. Dual material double gate structure reduces the peak electric field near the drain end, increases the drain breakdown voltage, improves the transconductance and reduces the drain conductance and desired threshold voltage roll-off for shorter channel lengths [73, 74].

The inclusion of channel engineering such as graded channel in the conventional junctionless transistor offers better short channel characteristics and analog performances [49, 51]. In graded channel, a reduced doping concentration gives rise to a decrease in the conductivity of the channel which further increases the resistivity of the path and lowers the off-state current

[52]. Thus, graded channel doping ensures better on/off current ratio without much affecting the on-state current.

The high-k spacer adjacent to the gate increases the fringing field through the spacer which leads to larger accumulation of electrons under the spacer resulting in a lower parasitic series resistance and a higher current driving capability [75]. It reduces leakage current, enhances electrostatic integrity, facilitates the depletion of the channel in off-state and thus effective channel length increases which is depicted in Figure 2.6 [75, 76]. It results in significant suppression of short channel effects and higher on/off current ratio. However, fringing fields through the spacer increase the outer fringe capacitance which leads to an enlarged gate capacitance and higher intrinsic delay [77]. So, dielectric constant of the spacer should be carefully chosen to get lower intrinsic delay but higher on/off current ratio.



(a)

(b)

Figure 2.6: Electron concentration contour plot of JLFET in off-state with (a) HfO_2 spacer and (b) air spacer [75]

Chapter 3

ANALYTICAL MODEL DEVELOPMENT

Development of analytical model helps to analyze, explain and predict the device performance in more reliable approach. This chapter introduces the 2-D device structure of graded channel dual material double gate junctionless transistor with high-k spacer (GC-DM-DG-JLFET-SP) and also provides with detailed mathematical derivation of potential distribution across the device using 2-D Poisson's equation, conformal mapping technique, 1-D capacitance model and associated boundary conditions.

3.1 Device Structure

The cross-sectional view of an n-type graded channel dual material double gate junctionless transistor with high-k spacer (GC-DM-DG-JLFET-SP) is shown in Figure 3.1.

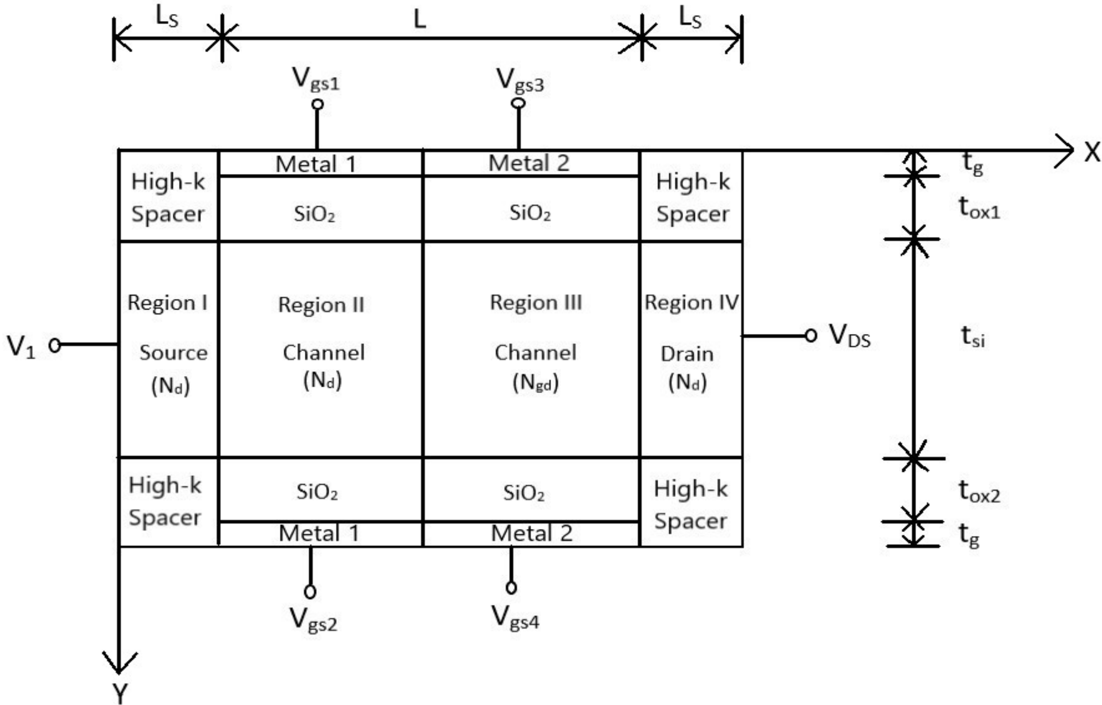


Figure 3.1: Cross-sectional view of a GC-DM-DG-JLFET-SP

In Figure 3.1, X axis indicates the source to drain direction and Y axis indicates the top to bottom direction. The source, silicon channel and drain are heavily doped with n-type impurity. Since the device is graded channel device, the doping concentration is not uniform throughout the channel. For the device in Figure 3.1, the doping concentration of the channel area under metal 2, N_{gd}, is higher than the doping concentration of the source, drain and channel area under metal 1, N_d. L is the channel length and L_S is the length of each spacer area. The thickness of the silicon channel and metal gate are indicated by t_{si} and t_g respectively. The top and bottom gate oxide thickness are denoted by t_{ox1} and t_{ox2} respectively. The voltage V_1, V_{DS}, V_{gs1}, V_{gs2}, V_{gs3} and V_{gs4} are applied to source, drain, top gate (metal 1), bottom gate (metal 1), top gate (metal 2) and bottom gate (metal 2) respectively.

3.2 Electrostatic Potential Modeling

In order to develop analytical model for symmetric graded channel dual material double gate junctionless transistor, the device is divided into four regions. Since region I (source) and region IV (drain) experience fringing field effect from the gate, conformal mapping technique along with 2-D Poisson's equation are used to determine the potential distribution in these regions. To derive the potential model for Region II and III, 2-D Poisson's equation and 1-D capacitance model are used. Finally, appropriate boundary conditions are used to develop the overall potential distribution for the device.

3.2.1 Potential distribution in source region (Region I)

2-D Poisson's equation is written as,

$$\frac{\delta^2\psi_i(x,y)}{\delta x^2}+\frac{\delta^2\psi_i(x,y)}{\delta y^2}=-\frac{qN_d}{\epsilon_{si}} \quad \left.\right\} \begin{array}{l} 0\le x\le L_s, \\ 0\le y\le t_{si} \end{array} \tag{3.1}$$

Here, $\psi_i(x,y)$ is the 2-D source potential, q is the elementary charge, N_d is the doping concentration in source region and ϵ_{si} is the dielectric constant for silicon.

Parabolic potential distribution is assumed along the horizontal direction inside Region I as,

$$\psi_i(x,y) = \psi_{si}(x) + a_{i1}(x)y + a_{i2}(x)y^2 \tag{3.2}$$

Since the device is symmetric, the potential at the upper and lower surface are equal.

$$\psi_i(x, 0) = \psi_i(x, t_{si}) \tag{3.3}$$

Here, t_{si} is the thickness of silicon substrate of the device.

By setting $y = 0$, equation (3.2) can be written as,

$$\psi_i(x, 0) = \psi_{si}(x) \tag{3.4}$$

From equation (3.2), (3.3) and (3.4),

$$a_{i2}(x) = -\frac{a_{i1}(x)}{t_{si}} \tag{3.5}$$

So, equation (3.2) can be written as,

$$\psi_i(x, y) = \psi_{si}(x) + a_{i1}(x)y - \frac{a_{i1}(x)}{t_{si}}y^2 \tag{3.6}$$

Now, solving equation (3.1) and using equation (3.2) and (3.5),

$$\frac{\delta^2\psi_{si}(x)}{\delta x^2} - \frac{2a_{i1}(x)}{t_{si}} = -\frac{qN_d}{\epsilon_{si}} \tag{3.7}$$

To illustrate fringing field effect in this region, the conformal mapping technique is used as shown in Figure 3.2 and the following transfer function is considered [37],

$$-y + j\eta(L_s - x) = t_{ox}\sin(u + jv) \tag{3.8}$$

Here,

$$\eta = \frac{t_{ox}}{L_s}\sinh\left(cosh^{-1}\frac{t_{ox} + t_g}{t_{ox}}\right), \tag{3.9}$$

t_{ox} = oxide thickness (for symmetric device, top and bottom gate oxide thickness are equal, so, $t_{ox1} = t_{ox2} = t_{ox}$)

and t_g = gate thickness

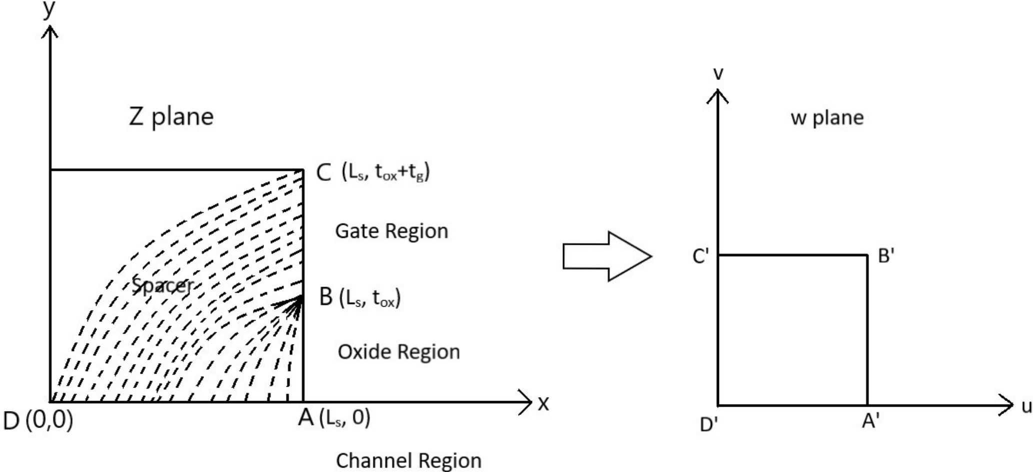


Figure 3.2: Conformal mapping transformation of region I (CB: Gate left edge, AD: Si-oxide interface, AB: Gate oxide) [37]

We know that,

$$\sin(u + jv) = \sin u \cosh v + j \cos u \sinh v \tag{3.10}$$

Replacing $\sin(u + jv)$ from equation (3.10) into equation (3.8) and separating the real and imaginary part,

$$y = -t_{ox} \sin u \cosh v \tag{3.11}$$

$$x = L_s - \frac{t_{ox}}{\eta} \cos u \sinh v \tag{3.12}$$

The electrical displacement in u-v coordinate system is,

$$E \Big|_{u=0} = \frac{\delta \psi_i(u, v)}{\delta u}\Big|_{u=0} \tag{3.13}$$

and

$$\frac{\delta \psi_i(u, v)}{\delta u}\Big|_{u=0} = \frac{\epsilon_{ox}}{\epsilon_{si}} . \frac{\psi_{si}(v) - V_{gs1} + \phi_{ms1}}{\frac{m\pi}{2}} \tag{3.14}$$

where, ϵ_{ox} is the permittivity of the gate oxide (for symmetric device, permittivity of top and bottom gate oxide are equal, so, $\epsilon_{ox1} = \epsilon_{ox2} = \epsilon_{ox}$) and m is such that $\sin(m\pi/2) = 1$

Now,

$$\frac{d^2\psi_{si}(x)}{dx^2} = \frac{d^2\psi_{si}(v)}{dv^2}.\left(\frac{dv}{dx}\right)^2 + \frac{d\psi_{si}(v)}{dv}.\frac{d^2v}{dx^2} \tag{3.15}$$

and

$$a_{i1}(x) = \frac{d\psi_{si}(u,v)}{du}\bigg|_{u\,=\,0} \times \frac{du}{dy}\bigg|_{y\,=\,0} \tag{3.16}$$

Differentiating equation (3.11) and setting $u = 0$,

$$\frac{du}{dy}\bigg|_{u\,=\,0} = -\frac{1}{t_{ox}\cosh v} \tag{3.17}$$

So, from equation (3.16),

$$a_{i1}(x) = \frac{\epsilon_{ox}}{\epsilon_{si}}.\frac{\psi_{si}(v) - V_{gs1} + \phi_{ms1}}{\frac{m\pi}{2}} \times \left(-\frac{1}{t_{ox}\cosh v}\right) \tag{3.18}$$

Substituting $a_{i1}(x)$ from equation (3.18) and using equation (3.15), equation (3.7) can be written as,

$$\frac{d^2\psi_{si}(v)}{dv^2}.\left(\frac{dv}{dx}\right)^2 + \frac{d\psi_{si}(v)}{dv}.\frac{d^2v}{dx^2} + \frac{2}{t_{si}}.\frac{1}{t_{ox}\cosh v}.\frac{\epsilon_{ox}}{\epsilon_{si}}.\frac{\psi_{si}(v) - V_{gs1} + \phi_{ms1}}{\frac{m\pi}{2}} = -\frac{qN_d}{\epsilon_{si}} \tag{3.19}$$

Similarly, differentiating equation (3.12),

$$\frac{dv}{dx}\bigg|_{u\,=\,0} = -\frac{\eta}{t_{ox}}.\frac{1}{\cosh v} \tag{3.20}$$

Squaring both sides of equation (3.20),

$$\left(\frac{dv}{dx}\right)^2 = \frac{\eta^2}{t_{ox}^2\,cosh^2 v} \tag{3.21}$$

Further differentiating equation (3.20),

$$\frac{d^2v}{dx^2} = -\frac{\eta^2 \sinh v}{t_{ox}^2\,cosh^3 v} \tag{3.22}$$

Again,

$$\frac{2}{t_{si}}\cdot\frac{1}{t_{ox}\cosh v}\cdot\frac{\epsilon_{ox}}{\epsilon_{si}}\cdot\frac{\psi_{si}(v)-V_{gs1}+\phi_{ms1}}{\frac{m\pi}{2}}=\frac{4\epsilon_{ox}\left[\psi_{si}(v)-V_{gs1}+\phi_{ms1}\right]}{t_{si}t_{ox}\epsilon_{si}m\pi\cosh v} \tag{3.23}$$

Using equation (3.21), (3.22) and (3.23), equation (3.19) is written as,

$$\frac{\eta^2}{t_{ox}^2\, cosh^2 v}\cdot\frac{d^2\psi_{si}(v)}{dv^2}-\frac{\eta^2\sinh v}{t_{ox}^2\, cosh^3 v}\cdot\frac{d\psi_{si}(v)}{dv}+\frac{4\epsilon_{ox}\left[\psi_{si}(v)-V_{gs1}+\phi_{ms1}\right]}{t_{si}t_{ox}\epsilon_{si}m\pi\cosh v} = -\frac{qN_d}{\epsilon_{si}} \tag{3.24}$$

Multiplying both sides of equation (3.24) by $\left(\frac{t_{ox}}{\eta}\right)^2$,

$$\frac{1}{cosh^2 v}\cdot\frac{d^2\psi_{si}(v)}{dv^2}-\frac{\sinh v}{cosh^3 v}\cdot\frac{d\psi_{si}(v)}{dv}+\frac{t_{ox}^2}{\eta^2}\cdot\frac{4\epsilon_{ox}\left[\psi_{si}(v)-V_{gs1}+\phi_{ms1}\right]}{t_{si}t_{ox}\epsilon_{si}m\pi\cosh v} = \frac{t_{ox}^2}{\eta^2}\left(-\frac{qN_d}{\epsilon_{si}}\right) \tag{3.25}$$

Let,

$$\alpha = \frac{4\epsilon_{ox}t_{ox}^2}{m\pi\ \epsilon_{si}t_{ox}t_{si}\eta^2} \tag{3.26}$$

So, from equation (3.25),

$$\frac{1}{cosh^2 v}\cdot\frac{d^2\psi_{si}(v)}{dv^2}-\frac{\sinh v}{cosh^3 v}\cdot\frac{d\psi_{si}(v)}{dv}+\frac{\alpha}{\cosh v}\left[\psi_{si}(v)-V_{gs1}+\phi_{ms1}\right] = \frac{t_{ox}^2}{\eta^2}\left(-\frac{qN_d}{\epsilon_{si}}\right) \tag{3.27}$$

Simplifying equation (3.27),

$$\frac{1}{cosh^2 v}\cdot\frac{d^2\psi_{si}(v)}{dv^2}+\alpha.\frac{\psi_{si}(v)}{\cosh v}=\alpha.\frac{V_{gs1}-\phi_{ms1}}{\cosh v}-\left(\frac{t_{ox}}{\eta}\right)^2.\frac{qN_d}{\epsilon_{si}} \tag{3.28}$$

Let,

$$t = \sinh v \tag{3.29}$$

and

$$\cosh v = \sqrt{1+t^2} \tag{3.30}$$

Now, equation (3.28) can be written as,

$$\frac{1}{1+t^2}.\frac{d^2\psi_{si}(t)}{dt^2}+\alpha.\frac{\psi_{si}(t)}{\sqrt{1+t^2}}=\alpha.\frac{V_{gs1}-\phi_{ms1}}{\sqrt{1+t^2}}-\left(\frac{t_{ox}}{\eta}\right)^2.\frac{qN_d}{\epsilon_{si}} \quad (3.31)$$

Using Taylor Series approximation and solving $\psi_{si}(t)$, the potential distribution in Region I is written as,

$$\psi_{si}(t)=A_1\left(1-\frac{\alpha}{2}t^2\right)+B_1\left(t-\frac{\alpha}{6}t^3\right)+V_{gs1}-\phi_{ms1}-\frac{qN_dt_{ox}^2}{\alpha\epsilon_{si}\eta^2}\sqrt{1+t^2} \quad (3.32)$$

where, the coefficients A_1 and B_1 are solved using appropriate boundary conditions and

$$t=\eta.\frac{L_s-x}{t_{ox}} \quad (3.33)$$

3.2.2 Potential distribution in channel under metal 1 (Region II)

2-D Poisson's equation for n-channel GC-DM-DG-JLFET-SP can be expressed as,

$$\left.\frac{\delta^2\phi_1(x,y)}{\delta x^2}+\frac{\delta^2\phi_1(x,y)}{\delta y^2}=-\frac{qN_d}{\epsilon_{si}}\quad\right\}\begin{array}{l}L_s\le x\le(L_s+(L/2)),\\0\le y\le t_{si}\end{array} \quad (3.34)$$

Here, $\phi_1(x,y)$ is the 2-D potential in the channel region under metal 1, q is the elementary charge, N_d is the doping concentration in this region and ϵ_{si} is the dielectric constant for silicon.

Assuming parabolic potential distribution,

$$\phi_1(x,y)=c_0(x)+c_1(x)y+c_2(x)y^2 \quad (3.35)$$

Boundary conditions at the top/bottom gate oxide and silicon channel interface are given by,

$$\phi_1(x,y)\Big|_{y=0}=\phi_{s1}(x) \quad (3.36)$$

$$\phi_1(x,y)\Big|_{y=t_{si}}=\phi_{s2}(x) \quad (3.37)$$

According to Gauss's law, the electrical flux between the silicon channel and gate oxide must be continuous. The electric fields at the top/bottom gate oxide and channel interface are given as,

$$\left.\frac{\delta\phi_1(x,y)}{\delta y}\right|_{y\,=\,0} = \frac{\epsilon_{ox1}}{\epsilon_{si}}.\frac{\phi_{s1}(x) - V'_{gs1}}{t_{ox1}} \tag{3.38}$$

$$\left.\frac{\delta\phi_1(x,y)}{\delta y}\right|_{y\,=\,t_{si}} = \frac{\epsilon_{ox2}}{\epsilon_{si}}.\frac{V'_{gs2} - \phi_{s2}(x)}{t_{ox2}} \tag{3.39}$$

Here, ϵ_{ox1} and ϵ_{ox2} are the permittivity of the top and bottom gate oxide respectively. Since the device is considered symmetric, $\epsilon_{ox1} = \epsilon_{ox2} = \epsilon_{ox}$. The effective top and bottom gate biases are $V'_{gs1} = V_{gs1} - V_{fb1}$ and $V'_{gs2} = V_{gs2} - V_{fb2}$ respectively. The flat band voltages are written as $V_{fb1} = \phi_{m1} - \phi_s$ and $V_{fb2} = \phi_{m2} - \phi_s$ where ϕ_{m1} and ϕ_{m2} are the work functions of the top and bottom gate electrodes respectively and ϕ_s is the work function of silicon which can be written as,

$$\phi_s = \chi_s + \frac{E_g}{2q} - V_T \ln\left(\frac{N_d}{n_i}\right) \tag{3.40}$$

where V_T is the thermal voltage, χ_s is the electron affinity, E_g is the bandgap energy and n_i is the intrinsic carrier concentration of silicon.

Now, setting $y = 0$ in equation (3.35) and using equation (3.36),

$$c_0(x) = \phi_{s1}(x) \tag{3.41}$$

Differentiating equation (3.35) with respect to y and setting $y = 0$,

$$\left.\frac{\delta\phi_1(x,y)}{\delta y}\right|_{y\,=\,0} = c_1(x) \tag{3.42}$$

Equation (3.42) can be further implied as,

$$c_1(x) = \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}\left[\phi_{s1}(x) - V'_{gs1}\right] \tag{3.43}$$

Similarly, setting $y = t_{si}$ and using equation (3.37),

$$c_2(x) = \frac{1}{t_{si}^2}\left[\phi_{s2}(x) - \phi_{s1}(x)\right] - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}\left[\phi_{s1}(x) - V'_{gs1}\right] \tag{3.44}$$

Replacing $c_0(x)$, $c_1(x)$ and $c_2(x)$ in equation (3.35),

$$\phi_1(x,y) = \phi_{s1}(x) + \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}\left[\phi_{s1}(x) - V'_{gs1}\right]y$$
$$+\left\{\frac{1}{t_{si}^2}\left[\phi_{s2}(x) - \phi_{s1}(x)\right] - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}\left[\phi_{s1}(x) - V'_{gs1}\right]\right\}y^2 \quad (3.45)$$

To find a solution of potential distribution in the channel region from 2-D Poisson's equation, first it has to be converted into 1-D differential equation [78]. For the 1-D capacitance model, the device is assumed to have capacitances shown in Figure 3.3. The capacitances C_{ox1} and C_{ox2} are for top and bottom oxide layer respectively. Since the device is assumed symmetric, they are both equal. Capacitance C_{si} is for silicon body.

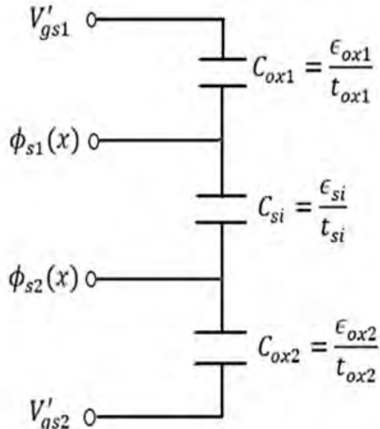


Figure 3.3: Capacitance model for Region II of GC-DM-DG-JLFET-SP

We know that,

$$Q = CV \quad (3.46)$$

Since C_{ox1}, C_{si} and C_{ox2} are in series,

$$Q = \frac{C_{ox1}C_{si}C_{ox2}}{C_{ox1}C_{si} + C_{ox1}C_{ox2} + C_{si}C_{ox2}}\left(V'_{gs1} - V'_{gs2}\right) \quad (3.47)$$

Again,

$$Q = \left[\phi_{s1}(x) - \phi_{s2}(x)\right]C_{si} \quad (3.48)$$

Solving equation (3.48),

$$\phi_{s2}(x) = \phi_{s1}(x) - \frac{C_{ox1}C_{ox2}}{C_{ox1}C_{si} + C_{ox1}C_{ox2} + C_{si}C_{ox2}}\left(V'_{gs1} - V'_{gs2}\right) \quad (3.49)$$

Substituting $\phi_{s2}(x)$ from equation (3.49) into equation (3.45),

$$\phi_1(x,y) = \phi_{s1}(x) + \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}\left[\phi_{s1}(x) - V'_{gs1}\right] y + \left\{\frac{1}{t_{si}^2}\left[\phi_{s2}(x) - \phi_{s1}(x)\right] - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}\left[\phi_{s1}(x) - V'_{gs1}\right]\right\} y^2 \tag{3.50}$$

From equation (3.50), $\phi_{s1}(x)$ can be found as,

$$\phi_{s1}(x) = \frac{\phi_1(x,y) + \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.V'_{gs1}.y - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}.V'_{gs1}.y^2 + \frac{1}{t_{si}^2}.\frac{\epsilon_{ox1}\epsilon_{ox2}t_{si}\left(V'_{gs1} - V'_{gs2}\right)}{\epsilon_{ox1}\epsilon_{si}t_{ox2} + \epsilon_{ox1}\epsilon_{ox2}t_{si} + \epsilon_{si}\epsilon_{ox2}t_{ox1}}.y^2}{1 + \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.y - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}.y^2} \tag{3.51}$$

The 1-D potential line along the source to drain direction at an arbitrary path $y = Y$ in the channel region is defined as [78],

$$\phi_{Y1}(x) = \phi_1(x,y)\Big|_{y = Y} \tag{3.52}$$

Finally, the 2-D potential function in term of $\phi_{Y1}(x)$ can be found as,

$$\begin{aligned}\phi_1(x,y) = \Bigg[\Bigg\{&\phi_{Y1}(x) + \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.V'_{gs1}.Y \\ &+ \left(\frac{1}{t_{si}^2}.\frac{\epsilon_{ox1}\epsilon_{ox2}t_{si}\left(V'_{gs1} - V'_{gs2}\right)}{\epsilon_{ox1}\epsilon_{si}t_{ox2} + \epsilon_{ox1}\epsilon_{ox2}t_{si} + \epsilon_{si}\epsilon_{ox2}t_{ox1}} - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}.V'_{gs1}\right)Y^2\Bigg\} \\ &\times \frac{1 + \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.y - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}.y^2}{1 + \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.Y - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}.Y^2}\Bigg] - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.V'_{gs1}.y \\ &- \left[\frac{1}{t_{si}^2}.\frac{\epsilon_{ox1}\epsilon_{ox2}t_{si}\left(V'_{gs1} - V'_{gs2}\right)}{\epsilon_{ox1}\epsilon_{si}t_{ox2} + \epsilon_{ox1}\epsilon_{ox2}t_{si} + \epsilon_{si}\epsilon_{ox2}t_{ox1}} - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}.V'_{gs1}\right]y^2\end{aligned} \tag{3.53}$$

Recalling 2-D Poisson's equation from (3.34),

$$\frac{\delta^2\phi_{Y1}(x)}{\delta x^2} + \frac{\delta^2\phi_{Y1}(x)}{\delta y^2} + \frac{qN_d}{\epsilon_{si}} = 0 \tag{3.54}$$

Now, substituting (3.53) in equation (3.54), 2-D Poisson's equation can be reduced to a simple 1-D second order non-homogeneous differential equation for the potential distribution at $y = Y$,

$$\frac{\delta^2\phi_{Y1}(x)}{\delta x^2} + \left\{ \frac{\phi_{Y1}(x) + \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.V'_{gs1}.Y + \left[\frac{1}{t_{si}^2}.\frac{\epsilon_{ox1}\epsilon_{ox2}t_{si}\left(V'_{gs1} - V'_{gs2}\right)}{\epsilon_{ox1}\epsilon_{si}t_{ox2} + \epsilon_{ox1}\epsilon_{ox2}t_{si} + \epsilon_{si}\epsilon_{ox2}t_{ox1}} - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}.V'_{gs1} \right] Y^2}{1 + \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.Y - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}.Y^2} \times \left(-\frac{2\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}\right) \right\} - 2\left[\frac{1}{t_{si}^2}.\frac{\epsilon_{ox1}\epsilon_{ox2}t_{si}\left(V'_{gs1} - V'_{gs2}\right)}{\epsilon_{ox1}\epsilon_{si}t_{ox2} + \epsilon_{ox1}\epsilon_{ox2}t_{si} + \epsilon_{si}\epsilon_{ox2}t_{ox1}} - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}.V'_{gs1}\right] + \frac{qN_d}{\epsilon_{si}} = 0 \tag{3.55}$$

Equation (3.55) can be written as,

$$\frac{\delta^2\phi_{Y1}(x)}{\delta x^2} - \frac{1}{\lambda_{Y1}^2}\{\phi_{Y1}(x) - \gamma_{Y1}\} = 0 \tag{3.56}$$

where,

$$\gamma_{Y1} = \alpha_{Y1} + \beta_{Y1}\lambda_{Y1}^2 \tag{3.57}$$

Replacing γ_{Y1} from equation (3.57) in (3.56),

$$\frac{\delta^2\phi_{Y1}(x)}{\delta x^2} - \frac{1}{\lambda_{Y1}^2}\{\phi_{Y1}(x) - \alpha_{Y1} - \beta_{Y1}\lambda_{Y1}^2\} = 0 \tag{3.58}$$

Comparing equation (3.58) to (3.55),

$$\lambda_{Y1} = \sqrt{\frac{1 + \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.Y - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}.Y^2}{\frac{2\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}}} \tag{3.59}$$

$$\alpha_{Y1} = -\frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.V'_{gs1}.Y - \left[\frac{1}{t_{si}^2}.\frac{\epsilon_{ox1}\epsilon_{ox2}t_{si}\left(V'_{gs1} - V'_{gs2}\right)}{\epsilon_{ox1}\epsilon_{si}t_{ox2} + \epsilon_{si}\epsilon_{ox2}t_{ox1} + \epsilon_{ox1}\epsilon_{ox2}t_{si}} - \frac{\epsilon_{ox1}V'_{gs1}}{\epsilon_{si}t_{ox1}t_{si}}\right]Y^2 \tag{3.60}$$

$$\beta_{Y1} = \frac{2\epsilon_{ox1}V'_{gs1}}{\epsilon_{si}t_{ox1}t_{si}} - \frac{2}{t_{si}^2}.\frac{\epsilon_{ox1}\epsilon_{ox2}t_{si}\left(V'_{gs1} - V'_{gs2}\right)}{\epsilon_{ox1}\epsilon_{si}t_{ox2} + \epsilon_{si}\epsilon_{ox2}t_{ox1} + \epsilon_{ox1}\epsilon_{ox2}t_{si}} + \frac{qN_d}{\epsilon_{si}} \quad (3.61)$$

Finally, solving for the general solution of ordinary differential equation (3.58), the equation for surface potential for Region II of GC-DM-DG-JLFET-SP is obtained as,

$$\phi_{Y1}(x) = A_{Y1}e^{x/\lambda_{Y1}} + B_{Y1}e^{-x/\lambda_{Y1}} + \gamma_{Y1} \quad (3.62)$$

where, the coefficients A_{Y1} and B_{Y1} are solved using appropriate boundary conditions.

3.2.3 Potential distribution in channel under metal 2 (Region III)

As similar as the derivation for Region II, the surface potential for Region III of GC-DM-DG-JLFET-SP can be expressed as,

$$\phi_{Y2}(x) = A_{Y2}e^{x/\lambda_{Y2}} + B_{Y2}e^{-x/\lambda_{Y2}} + \gamma_{Y2} \quad (3.63)$$

where, the coefficients A_{Y2} and B_{Y2} are solved using appropriate boundary conditions and

$$\lambda_{Y2} = \sqrt{\frac{1 + \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.Y - \frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}.Y^2}{\frac{2\epsilon_{ox1}}{\epsilon_{si}t_{ox1}t_{si}}}} \quad (3.64)$$

$$\gamma_{Y2} = \alpha_{Y2} + \beta_{Y2}\lambda_{Y2}^2 \quad (3.65)$$

$$\alpha_{Y2} = -\frac{\epsilon_{ox1}}{\epsilon_{si}t_{ox1}}.V'_{gs3}.Y - \left[\frac{1}{t_{si}^2}.\frac{\epsilon_{ox1}\epsilon_{ox2}t_{si}\left(V'_{gs3} - V'_{gs4}\right)}{\epsilon_{ox1}\epsilon_{si}t_{ox2} + \epsilon_{si}\epsilon_{ox2}t_{ox1} + \epsilon_{ox1}\epsilon_{ox2}t_{si}} - \frac{\epsilon_{ox1}V'_{gs3}}{\epsilon_{si}t_{ox1}t_{si}}\right]Y^2 \quad (3.66)$$

$$\beta_{Y2} = \frac{2\epsilon_{ox1}V'_{gs3}}{\epsilon_{si}t_{ox1}t_{si}} - \frac{2}{t_{si}^2}.\frac{\epsilon_{ox1}\epsilon_{ox2}t_{si}\left(V'_{gs3} - V'_{gs4}\right)}{\epsilon_{ox1}\epsilon_{si}t_{ox2} + \epsilon_{si}\epsilon_{ox2}t_{ox1} + \epsilon_{ox1}\epsilon_{ox2}t_{si}} + \frac{qN_{gd}}{\epsilon_{si}} \quad (3.67)$$

3.2.4 Potential distribution in drain region (Region IV)

The potential distribution for Region IV can be derived following the steps done for Region I of GC-DM-DG-JLFET-SP,

$$\psi_{si}(t) = A_2\left(1 - \frac{\alpha}{2}t^2\right) + B_2\left(t - \frac{\alpha}{6}t^3\right) + V_{gs3} - \phi_{ms3} - \frac{qN_d t_{ox}^2}{\alpha\epsilon_{si}\eta^2}\sqrt{1 + t^2} \quad (3.68)$$

where, the coefficients A_2 and B_2 are solved using appropriate boundary conditions and

$$t = \eta . \frac{x - L_s - L}{t_{ox}} \tag{3.69}$$

3.2.5 Solving boundary conditions

The coefficients in equation (3.32), (3.62), (3.63) and (3.68) can be formulated using appropriate boundary conditions. For our device, eight boundary conditions can be found:

1. The potential at the source side,

$$\psi_{c1}(x) \Big|_{x\,=\,0} = V_1 \tag{3.70}$$

2. The potential at the interface of source (Region I) and channel under metal 1 (Region II) is continuous.

$$\psi_{c1}(x) \Big|_{x\,=\,L_s} = \phi_1(x, y) \Big|_{x\,=\,L_s,\, y\,=\,Y} \tag{3.71}$$

3. The electric field at the interface of source (Region I) and channel under metal 1 (Region II) is continuous.

$$\frac{d\psi_{c1}(x)}{dx} \Bigg|_{x\,=\,L_s} = \frac{d\phi_1(x, y)}{dx} \Bigg|_{x\,=\,L_s,\, y\,=\,Y} \tag{3.72}$$

4. The potential at the interface of channel under metal I (Region II) and channel under metal 2 (Region III) is continuous.

$$\phi_{Y1}(x) \Big|_{x\,=\,L_s\,+\,(L/2)} = \phi_{Y2}(x) \Big|_{x\,=\,L_s\,+\,(L/2)} \tag{3.73}$$

5. The electric field at the interface of channel under metal I (Region II) and channel under metal 2 (Region III) is continuous.

$$\frac{d\phi_{Y1}(x)}{dx} \Bigg|_{x\,=\,L_s\,+\,(L/2)} = \frac{d\phi_{Y2}(x)}{dx} \Bigg|_{x\,=\,L_s\,+\,(L/2)} \tag{3.74}$$

6. The potential at the interface of channel under metal II (Region III) and drain (Region IV) is continuous.

$$\phi_{Y2}(x) \Big|_{x\,=\,L_s\,+\,L} = \psi_{c2}(x) \Big|_{x\,=\,L_s\,+\,L} \tag{3.75}$$

7. The electric field at the interface of channel under metal II (Region III) and drain (Region IV) is continuous.

$$\left.\frac{d\psi_{c2}(x)}{dx}\right|_{x\,=\,L_s\,+\,L} = \left.\frac{d\phi_{Y2}(x)}{dx}\right|_{x\,=\,L_s\,+\,L} \tag{3.76}$$

8. The potential at the drain side,

$$\left.\psi_{c2}(x)\right|_{x\,=\,L\,+\,2L_s} = V_{ds} + V_1 \tag{3.77}$$

Solving the above eight boundary conditions, the coefficients A_1, B_1, A_{Y1}, B_{Y1}, A_{Y2}, B_{Y2}, A_2 and B_2 in equations (3.32), (3.62), (3.63) and (3.68) are derived as follows,

$$A_1 = \frac{V_1 - B_1 Q - R}{P} \tag{3.78}$$

$$B_1 = \frac{\frac{t_{ox}}{\eta\lambda_{Y1}}\left[A_{Y1}e^{L_s/\lambda_{Y1}} - B_{Y1}e^{-L_s/\lambda_{Y1}}\right]}{\frac{\epsilon_{ox}}{\epsilon_{si}}\cdot\frac{Y - \frac{1}{t_{si}}.Y^2}{\frac{m\pi}{2}.t_{ox}} - 1} \tag{3.79}$$

$$A_{Y1} = \frac{V_1 - R - \frac{\gamma_{Y1}P}{S} + \frac{TP}{S} - B_{Y1}\left(\frac{P}{S} - \frac{t_{ox}Q}{\eta\lambda_{Y1}J}\right)e^{-L_s/\lambda_{Y1}}}{\frac{P}{S} + \frac{t_{ox}Q}{\eta\lambda_{Y1}J}} \times e^{-L_s/\lambda_{Y1}} \tag{3.80}$$

$$B_{Y1} = \frac{E - \lambda_{Y1}\left(\frac{P}{S} + \frac{t_{ox}Q}{\eta\lambda_{Y1}J}\right)\left[\frac{A_{Y2}}{\lambda_{Y2}}e^{(L_s+L_1)/\lambda_{Y2}} - \frac{B_{Y2}}{\lambda_{Y2}}e^{-(L_s+L_1)/\lambda_{Y2}}\right]e^{-L_1/\lambda_{Y1}}}{D} \tag{3.81}$$

$$A_{Y2} = \frac{Q_1 + B_{Y2}R_1}{P_1} \tag{3.82}$$

$$B_{Y2} = \frac{B_2P_2 - Q_1}{R_1 - Q_2} \tag{3.83}$$

$$A_2 = \frac{V_1 + V_{ds} - \frac{R_3G}{P_3} - H - I}{F + \frac{Q_3G}{P_3}} \tag{3.84}$$

$$B_2 = \frac{A_2Q_3 + R_3}{P_3} \tag{3.85}$$

where,

$$L_1 = \frac{L}{2} \tag{3.86}$$

$$P = \left(1 - \frac{\alpha}{2} t_0^2\right)\left(1 - \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} \cdot t_{ox}\sqrt{1 + t_0^2}}\right) \tag{3.87}$$

$$Q = \left(t_0 - \frac{\alpha}{6} t_0^3\right)\left(1 - \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} \cdot t_{ox}\sqrt{1 + t_0^2}}\right) \tag{3.88}$$

$$R = \left(V_{gs1} - \phi_{ms1} - \frac{qN_d t_{ox}^2}{\alpha \epsilon_{si} \eta^2} \sqrt{1 + t_0^2}\right)\left(1 - \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} \cdot t_{ox}\sqrt{1 + t_0^2}}\right) + \left(\frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{V_{gs1} - \phi_{ms1}}{\frac{m\pi}{2}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{t_{ox}\sqrt{1 + t_0^2}}\right) \tag{3.89}$$

$$t_0 = \frac{\eta L_s}{t_{ox}} \tag{3.90}$$

$$S = 1 - \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} \cdot t_{ox}} \tag{3.91}$$

$$T = \left(V_{gs1} - \phi_{ms1} - \frac{qN_d t_{ox}^2}{\alpha \epsilon_{si} \eta^2}\right)\left(1 - \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} \cdot t_{ox}}\right) + \left(\frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{V_{gs1} - \phi_{ms1}}{\frac{m\pi}{2}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{t_{ox}}\right) \tag{3.92}$$

$$F = \left(1 - \frac{\alpha}{2} t_1^2\right)\left(1 - \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} \cdot t_{ox}\sqrt{1 + t_1^2}}\right) \tag{3.93}$$

$$G = \left(t_1 - \frac{\alpha}{6} t_1^3\right)\left(1 - \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} \cdot t_{ox}\sqrt{1 + t_1^2}}\right) \tag{3.94}$$

$$H = \left(V_{gs3} - \phi_{ms3} - \frac{qN_d t_{ox}^2}{\alpha \epsilon_{si} \eta^2} \sqrt{1 + t_1^2}\right)\left(1 - \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} \cdot t_{ox}\sqrt{1 + t_1^2}}\right) \tag{3.95}$$

$$I = \frac{\left(V_{gs3} - \phi_{ms3}\right)\left(Y - \frac{1}{t_{si}} Y^2\right)}{\frac{m\pi}{2} \cdot t_{ox}\sqrt{1 + t_1^2}} \tag{3.96}$$

$$t_1 = \eta \frac{L + 2L_s - L_s - L}{t_{ox}} = \frac{\eta L_s}{t_{ox}} \tag{3.97}$$

$$J = \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} . t_{ox}} - 1 \tag{3.98}$$

$$D = \left(\frac{P}{S} - \frac{t_{ox} Q}{\eta \lambda_{Y1} J}\right) e^{-L_s/\lambda_{Y1}} + \left(\frac{P}{S} + \frac{t_{ox} Q}{\eta \lambda_{Y1} J}\right) e^{-(L_s + 2L_1)/\lambda_{Y1}} \tag{3.99}$$

$$E = V_1 - R - \frac{\gamma_{Y1} P}{S} + \frac{TP}{S} \tag{3.100}$$

$$P_1 = \frac{D}{2}\left(1 - \frac{\lambda_{Y1}}{\lambda_{Y2}}\right) e^{(L_s + L_1)\left(\frac{1}{\lambda_{Y2}} - \frac{1}{\lambda_{Y1}}\right)} e^{2(L_s + L_1)/\lambda_{Y1}} + \frac{\lambda_{Y1}}{\lambda_{Y2}}\left(\frac{P}{S} + \frac{t_{ox} Q}{\eta \lambda_{Y1} J}\right) e^{(L_s + L_1)/\lambda_{Y2}} e^{-L_1/\lambda_{Y1}} \tag{3.101}$$

$$Q_1 = E - \frac{D}{2}(\gamma_{Y2} - \gamma_{Y1}) e^{-(L_s + L_1)/\lambda_{Y1}} e^{2(L_s + L_1)/\lambda_{Y1}} \tag{3.102}$$

$$R_1 = \frac{\lambda_{Y1}}{\lambda_{Y2}}\left(\frac{P}{S} + \frac{t_{ox} Q}{\eta \lambda_{Y1} J}\right) e^{-(L_s + L_1)/\lambda_{Y2}} e^{-L_1/\lambda_{Y1}} - \frac{D}{2}\left(1 + \frac{\lambda_{Y1}}{\lambda_{Y2}}\right) e^{-(L_s + L_1)\left(\frac{1}{\lambda_{Y1}} + \frac{1}{\lambda_{Y2}}\right)} e^{2(L_s + L_1)/\lambda_{Y1}} \tag{3.103}$$

$$P_2 = \frac{\lambda_{Y2} P_1 \eta}{t_{ox}} \left(1 - \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} . t_{ox}}\right) e^{-(L_s + L)/\lambda_{Y2}} \tag{3.104}$$

$$Q_2 = P_1 e^{-2(L_s + L)/\lambda_{Y2}} \tag{3.105}$$

$$P_3 = P_2 \left\{\left(\frac{1}{\lambda_{Y2}} e^{-(L_s + L)/\lambda_{Y2}}\right) \lambda_{Y2} + e^{-(L_s + L)/\lambda_{Y2}}\right\} + \left[\left\{\frac{\eta}{t_{ox}} \left(1 - \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} . t_{ox}}\right)\right\} \lambda_{Y2} (R_1 - Q_2)\right] \tag{3.106}$$

$$Q_3 = \left(1 - \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} . t_{ox}}\right) (R_1 - Q_2) \tag{3.107}$$

$$R_3 = \left\{\left(V_{gs3} - \phi_{ms3} - \frac{qN_d t_{ox}^2}{\alpha \epsilon_{si} \eta^2}\right)\left(1 - \frac{\epsilon_{ox}}{\epsilon_{si}} . \frac{Y - \frac{1}{t_{si}} Y^2}{\frac{m\pi}{2} . t_{ox}}\right) + \left(\frac{\epsilon_{ox}}{\epsilon_{si}} . \frac{V_{gs3} - \phi_{ms3}}{\frac{m\pi}{2}} . \frac{Y - \frac{1}{t_{si}} Y^2}{t_{ox}}\right) - \gamma_{Y2}\right\}(R_1 - Q_2) + Q_1 \left\{\left(\frac{1}{\lambda_{Y2}} e^{-(L_s + L)/\lambda_{Y2}}\right)\lambda_{Y2} + e^{-(L_s + L)/\lambda_{Y2}}\right\} \quad (3.108)$$

Chapter 4

SIMULATION RESULTS

This chapter presents the simulations and results of model verification and comparison of performance between graded channel dual material double gate junctionless field effect transistor with high-k spacer (GC-DM-DG-JLFET-SP) and uniform channel dual material double gate junctionless field effect transistor with high-k spacer (UC-DM-DG-JLFET-SP). After deriving the analytical model for surface potential of GC-DM-DG-JLFET-SP, this model will be verified with the simulation done by V. Pathak and G. Saini [52]. Then the short channel characteristics and analog performances of this device will be compared with those of UC-DM-DG-JLFET-SP. All simulations will be performed by MATLAB.

Table 4.1: Various device parameters used for simulations [52]

Parameter Description	GC-DM-DG-JLFET-SP	UC-DM-DG-JLFET-SP
Gate length (L)	60 nm	60 nm
Spacer length (L_S)	10 nm	10 nm
Channel thickness (t_{si})	10 nm	10 nm
Thickness of top gate oxide layer (t_{ox1})	2 nm	2 nm
Thickness of bottom gate oxide layer (t_{ox2})	2 nm	2 nm
Doping type	n	n
Doping in source, channel under metal 1 and drain (N_d)	2×10^{19} cm^{-3}	2.5×10^{19} cm^{-3}
Doping in channel under metal 2 (N_{gd})	2.5×10^{19} cm^{-3}	2.5×10^{19} cm^{-3}
Work function of gate electrode (ϕ_{m1})	5.535	5.577
Work function of gate electrode (ϕ_{m2})	4.8	5.5
Work function of Si (ϕ_{si})	4.184	4.184
Dielectric constant of Si (ϵ_{si})	11.7	11.7
Dielectric constant of SiO_2 (ϵ_{ox})	3.9	3.9
Dielectric constant of high-k spacer (ϵ)	20	20

4.1 Model Verification

The 2-D analytical model for surface potential of GC-DM-DG-JLFET-SP formulated in previous chapter has been verified by comparing its plot with the simulation done by V. Pathak and G. Saini [52]. For model verification, the same process parameters have been used as in [52] and are shown in Table 4.1. The simulations have been performed using MATLAB and are shown in Figure 4.1. It shows that there is a slight discrepancy between these two plots but the curve plotted using the derived analytical model has followed the nature of the curve obtained from [52]. For both simulations, source voltage, V_1, is 0.5 V and the drain side voltage, V_{ds}, is 1 V.

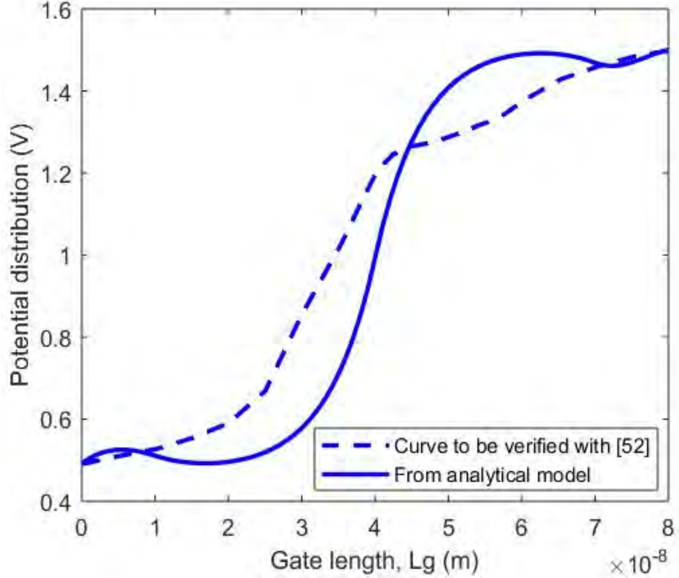


Figure 4.1: Verification of analytical model of GC-DM-DG-JLFET-SP at V_{gs} = 0.5 V

4.2 Surface Potential

The surface potential has been calculated for GC-DM-DG-JLFET-SP considering uniform doping concentration, N_d = 2×10^{19} cm^{-3}, in source, drain and channel region under metal 1 and higher doping concentration, N_{gd} = 2.5×10^{19} cm^{-3}, in channel region under metal 2. The potential distribution for UC-DM-DG-JLFET-SP has been calculated using the uniform doping concentration, N_d = 2.5×10^{19} cm^{-3}, across the source, drain and whole channel region. The metal work functions of dual material gates are used as same as in [52] and are also mentioned in Table 4.1. The work function used for metal 1 is chosen to be higher than work function of

metal 2 which introduces a step function in the potential distribution along the channel, enhances the electric field distribution at the source side to increase the velocity of the electrons and prevents any change in the drain bias to affect the channel region under metal 1 [79]. Hafnium oxide (HfO_2) has been used as high-k spacer in both devices and hence, same dielectric constant, $\epsilon = 20$, has been used.

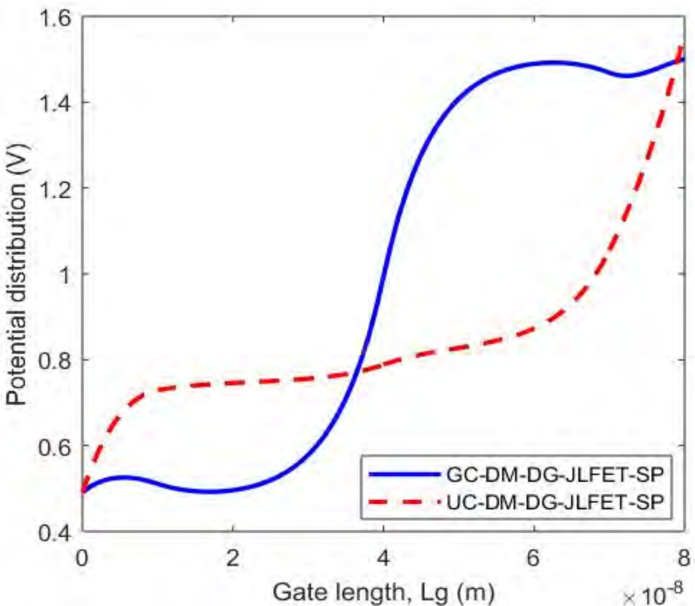


Figure 4.2: Comparison of surface potential between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP at $V_{gs} = 0.5$ V

Figure 4.2 compares the surface potential of GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP. The plot for surface potential of UC-DM-DG-JLFET-SP appears to be flatter than that of GC-DM-DG-JLFET-SP because the difference between work functions of metal 1 and metal 2 used for UC-DM-DG-JLFET-SP is much smaller than that used for GC-DM-DG-JLFET-SP. It can be observed that the potential distribution of UC-DM-DG-JLFET-SP in region I (0 to 10 nm) and region II (10 to 40 nm) is higher than that of GC-DM-DG-JLFET-SP because of the higher doping concentration of UC-DM-DG-JLFET-SP. The potential profile of GC-DM-DG-JLFET-SP rises more sharply than that of UC-DM-DG-JLFET-SP because of the variation in carrier concentration and velocity distribution across the channel. Due to abrupt change in doping concentration between region II (10 to 40 nm) and region III (40 to 70 nm), there is a critical difference in the electric field and the electrons experience stronger pull while travelling across the channel [52].

4.3 Drain Current versus Gate Voltage (I_{ds} versus V_{gs})

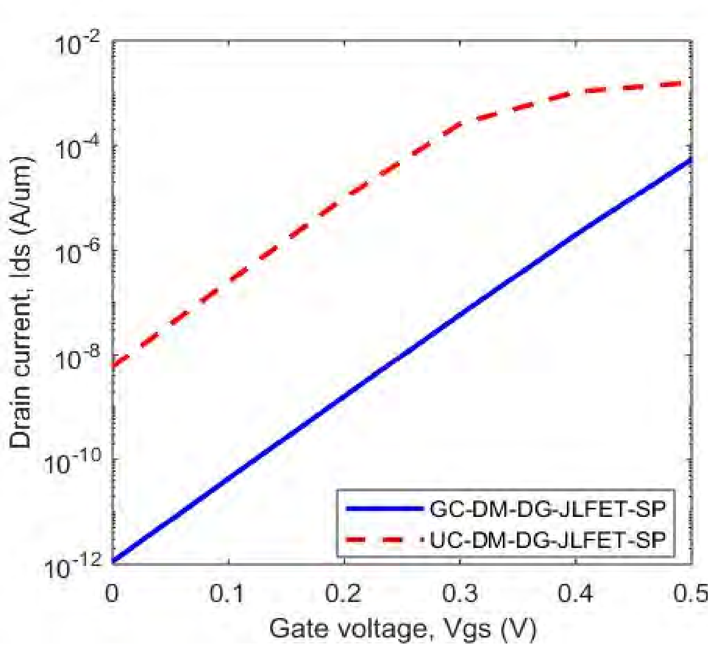


Figure 4.3: Comparison of drain current versus gate voltage between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP in subthreshold region for L_g = 80 nm at V_{ds} = 1 V

Drain current is calculated as [37],

$$I_{ds} = \frac{q\mu_n W V_T (1 - e^{-V_{ds}/V_T})}{\int_0^{L_S} \frac{dx}{\int_0^{t_{si}} n_i e^{\frac{\psi_{c1}(x,y)}{V_T}} dy} + \int_{L_S}^{L_S+L/2} \frac{dx}{\int_0^{t_{si}} n_i e^{\frac{\phi_1(x,y)}{V_T}} dy} + \int_{L_S+L/2}^{L_S+L} \frac{dx}{\int_0^{t_{si}} n_i e^{\frac{\phi_2(x,y)}{V_T}} dy} + \int_{L_S+L}^{2L_S+L} \frac{dx}{\int_0^{t_{si}} n_i e^{\frac{\psi_{c2}(x,y)}{V_T}} dy}} \tag{4.1}$$

Here, q is charge of electron, μ_n is effective mobility of silicon, W is the channel width, V_T is the thermal voltage and n_i is the intrinsic carrier concentration. The surface potentials $\psi_{c1}(x,y)$, $\phi_1(x,y)$, $\phi_2(x,y)$ and $\psi_{c2}(x,y)$ are calculated using our derived 2-D analytical model.

Figure 4.3 shows the comparison of drain current between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP in subthreshold region. The off-state current improves for GC-DM-DG-JLFET-SP because a reduced doping concentration gives rise to a decrease in the conductivity of the channel which further increases the resistivity of the path. From Figure 4.3, it can be

seen that off-state current decreases significantly for GC-DM-DG-JLFET-SP. When $V_{gs} = 0$ V, $I_{ds} = 1.129\times10^{-12}$ A/µm for GC-DM-DG-JLFET-SP and $I_{ds} = 5.887\times10^{-9}$ A/µm for UC-DM-DG-JLFET-SP.

4.4 I_{on}/I_{off} Ratio

I_{on}/I_{off} ratio is the figure of merit for having high performance (more I_{on}) and low leakage power (less I_{off}). Higher on/off current ratio is always expected for better performance of a device. I_{off} and I_{on} have been calculated from I_{ds} versus V_{gs} curve respectively at $V_{gs} = 0$ and $V_{gs} = V_{TH}$.

Since off-state current decreases significantly for GC-DM-DG-JLFET-SP, on/off current ratio is higher for graded channel device. Figure 4.4 shows that for gate length of 50 nm, $I_{on}/I_{off} = 2.01\times10^{7}$ for GC-DM-DG-JLFET-SP and $I_{on}/I_{off} = 5.77\times10^{3}$ for UC-DM-DG-JLFET-SP. So, on/off current ratio of graded channel device is 10^{3} times higher than that of uniformly doped channel device for $L_g = 50$ nm.

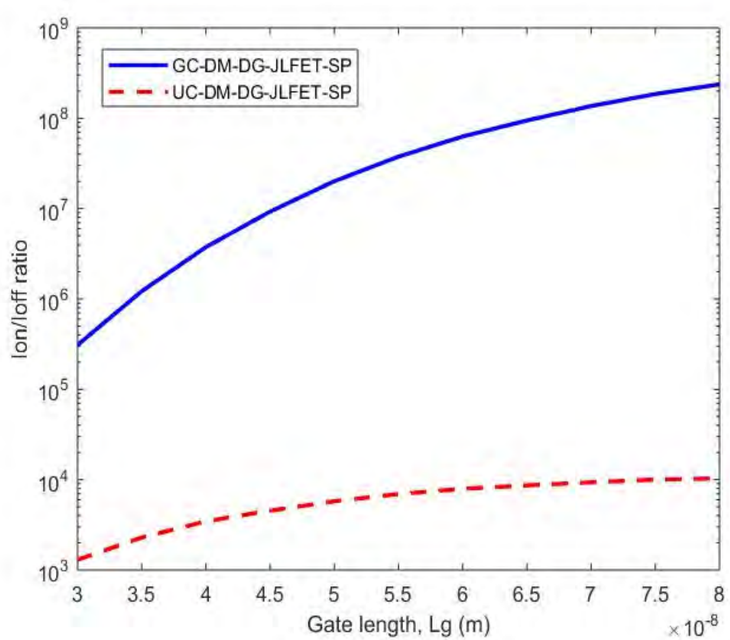


Figure 4.4: Comparison of I_{on}/I_{off} ratio between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP at $V_{ds} = 1$ V

4.5 Short Channel Characteristics

This section compares the short channel characteristics between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP. Here, two short channel effects – subthreshold swing and drain induced barrier lowering have been considered for analyzing the performance of the two devices.

4.5.1 Subthreshold Swing (SS)

Subthreshold swing is calculated from the following equation [43],

$$SS = \frac{\delta V_{gs}}{\delta log_{10}(I_{ds})} \tag{4.2}$$

Subthreshold swing is defined as the change in gate voltage which must be applied in order to create a one decade increase in the subthreshold current. It is expected that in order to have large change in the output current, low gate voltage should be applied. So, subthreshold swing should be smaller. Theoretical limit of subthreshold swing of a transistor is 60 mV/decade [80].

In order to take the device from OFF state to ON state, $SS = \frac{V_{TH}-0}{log_{10}(I_{on}-I_{off})}$. So, if I_{off} decreases, the denominator becomes greater and SS decreases. Since GC-DM-DG-JLFET-SP shows significantly smaller off-state current than UC-DM-DG-JLFET-SP, it has lower SS than the uniformly doped channel device.

Figure 4.5 shows that with the decrease in gate length, subthreshold swing degrades. For gate length of 50 nm, SS = 73.35 mV/dec for GC-DM-DG-JLFET-SP and SS = 78.99 mV/dec for UC-DM-DG-JLFET-SP. For gate length of 80 nm, SS = 65.04 V/dec for GC-DM-DG-JLFET-SP and SS = 72.72 mV/dec for UC-DM-DG-JLFET-SP. So, for graded channel device, SS is lower than that of uniformly doped channel device.

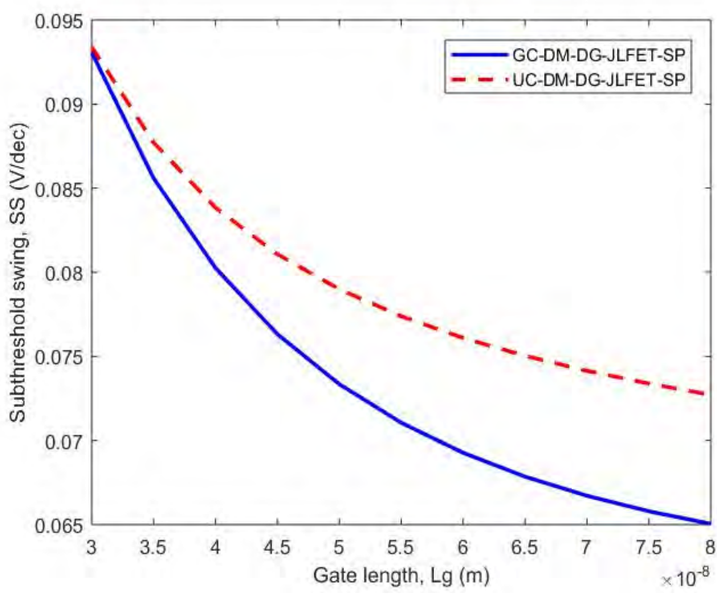


Figure 4.5: Comparison of subthreshold swing between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP at V_{ds} = 1 V

4.5.2 Drain Induced Barrier Lowering (DIBL)

Drain induced barrier lowering is referred to as a reduction of threshold voltage of the transistor at higher drain voltages. If a high drain voltage is applied, the height of potential barrier can decrease which results in increased drain current. DIBL is calculated using following equation [43]:

$$DIBL = \frac{\Delta V_{TH}}{\Delta V_{ds}} = \frac{V_{TH_L} - V_{TH_H}}{V_{ds_H} - V_{ds_L}} \tag{4.3}$$

Here, threshold voltage V_{TH_L} is calculated at V_{ds_L} = 0.1 V and V_{TH_H} is calculated at V_{ds_H} = 1 V. At higher drain voltage, potential barrier decreases, I_{off} increases and V_{TH} decreases too. As a result, DIBL increases. Since UC-DM-DG-JLFET-SP offers higher I_{off} than GC-DM-DG-JLFET-SP, uniformly doped channel device shows higher DIBL than graded channel device.

Figure 4.6 compares the DIBL between the two devices. At gate length of 40 nm, DIBL of graded channel device is 2.423 mV/V while DIBL of the uniformly doped device is 5.58 mV/V.

So, GC-DM-DG-JLFET-SP shows 3.157 mV/V less DIBL than UC-DM-DG-JLFET-SP at L_g = 40 nm.

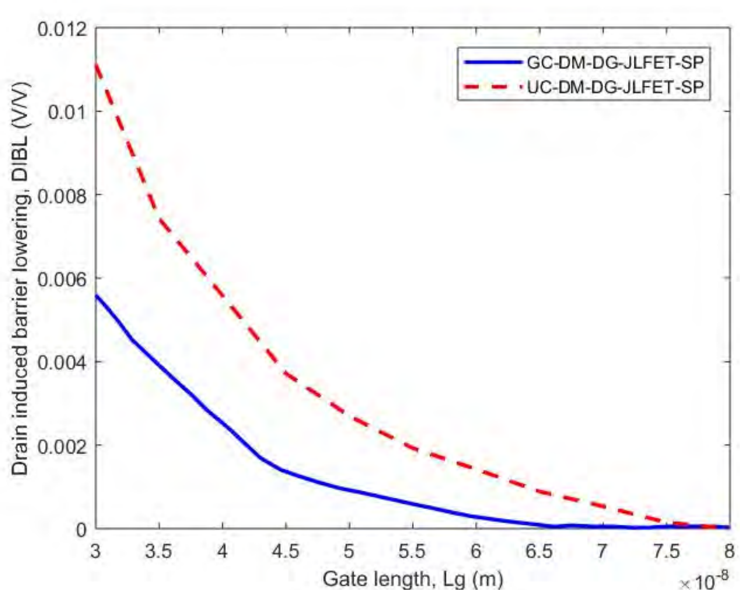


Figure 4.6: Comparison of drain induced barrier lowering between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP

4.6 Analog Performances

The key indicators for analog/RF performances of a device are transconductance, transconductance generation factor, drain output conductance, intrinsic gain and early voltage. This section analyzes and compares these figures of merit between the two devices.

4.6.1 Transconductance (g_m)

Transconductance can be defined as the effectiveness of a device to convert voltage into current. It can be calculated as [51],

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} \tag{4.4}$$

From equation (4.4), it can be depicted that transconductance is the slope of I_{ds} versus V_{gs} curve shown in Figure 4.7. Figure 4.8 (a) presents the verification of transconductance of GC-DM-DG-JLFET-SP for L_g = 50 nm and Figure 4.8 (b) shows the comparison of

transconductance between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP for L_g = 80 nm. It can be seen that GC-DM-DG-JLFET-SP exhibits lower transconductance than UC-DM-DG-JLFET-SP for V_{gs} < 0.9 V because drain current for UC-DM-DG-JLFET-SP increases more steeply than GC-DM-DG-JLFET-SP.

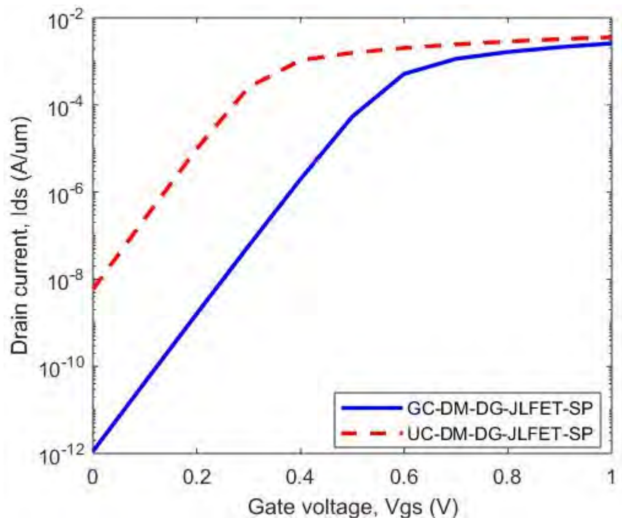


Figure 4.7: Comparison of drain current versus gate voltage between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP for L_g = 80 nm at V_{ds} = 1 V

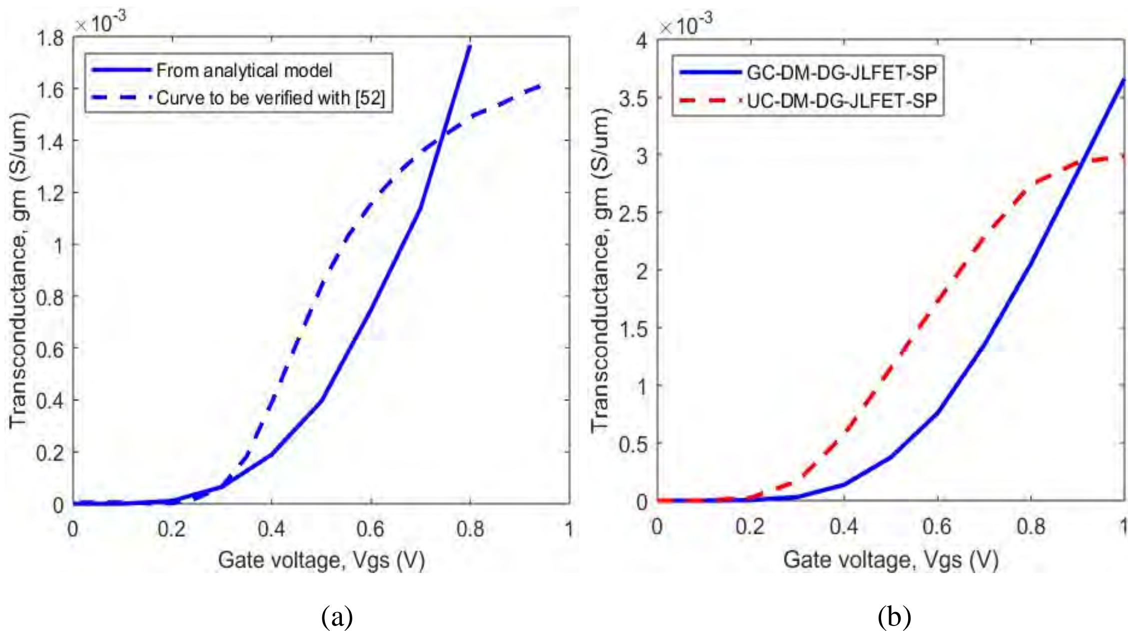


Figure 4.8: a) Verification of transconductance of GC-DM-DG-JLFET-SP for L_g = 50 nm and b) Comparison of transconductance between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP for L_g = 80 nm at V_{ds} = 1 V

From Figure 4.8 (b), it can be seen that at gate voltage of 0.6 V, transconductance of graded channel device is 0.7595 mS/μm whereas that of uniform channel device is 1.728 mS/μm. Again, at gate voltage of 1 V, transconductance of graded channel device is 3.657 mS/μm whereas that of uniform channel device is 2.987 mS/μm.

4.6.2 Transconductance Generation Factor (g_m/I_{ds})

Transconductance generation factor g_m/I_{ds} refers to how efficiently a transistor can translate dc power into ac frequency and gain performance [51]. Figure 4.9 (a) verifies g_m/I_{ds} of GC-DM-DG-JLFET-SP for L_g = 50 nm. From Figure 4.9 (b), it can be seen that the graded channel device of 80 nm gate length shows higher transconductance generation factor than uniform channel device for V_{gs} > 0.2 V since GC-DM-DG-JLFET-SP has lower drain current in spite of having lower g_m compared to UC-DM-DG-JLFET-SP. For V_{gs} > 0.8 V, this factor becomes close to zero because the drain current for both devices become saturated after applying a certain gate voltage. From Figure 4.9 (b), for L_g = 80 nm, when V_{gs} = 0.5 V, g_m/I_{ds} for graded channel device is 30.45 V^{-1} and uniform channel device is 2.883 V^{-1} and when V_{gs} = 0.8 V, g_m/I_{ds} for graded channel device is 2.928 V^{-1} and uniform channel device is 1.386 V^{-1}.

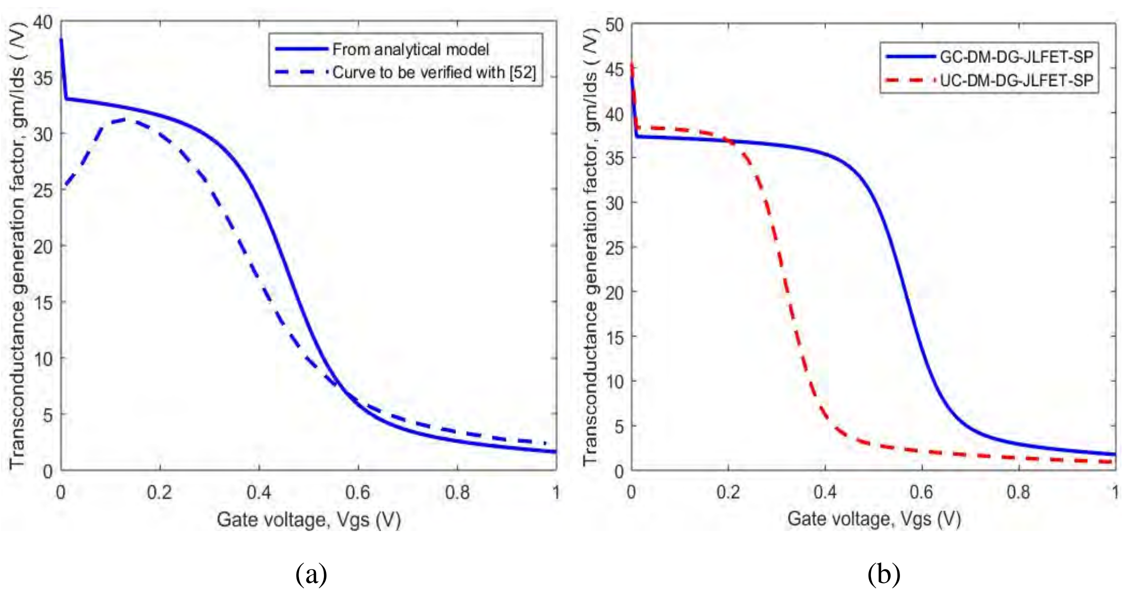


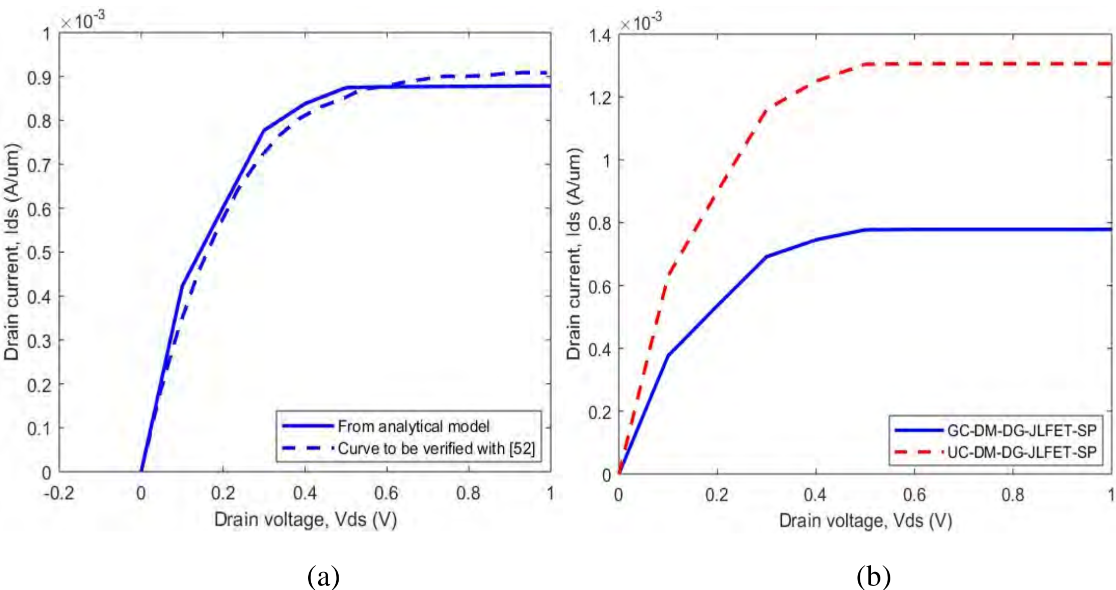
Figure 4.9: a) Verification of g_m/I_{ds} of GC-DM-DG-JLFET-SP for L_g = 50 nm and b) Comparison of g_m/I_{ds} between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP for L_g = 80 nm at V_{ds} = 1 V

4.6.3 Drain Output Conductance (G_D)

Drain output conductance is calculated as [51],

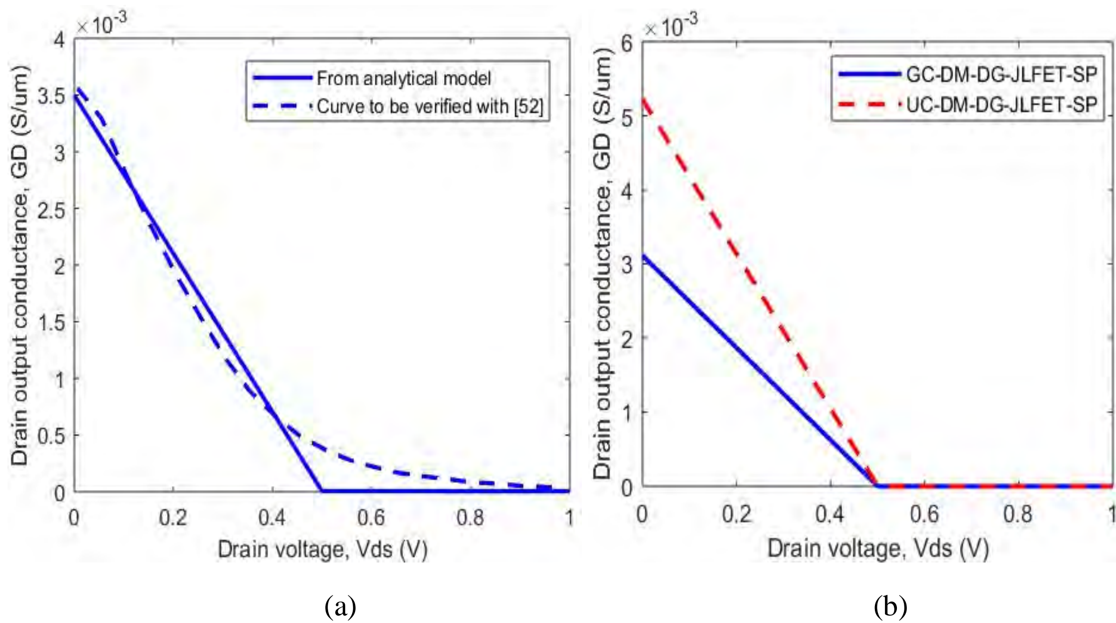
$$G_D = \frac{\delta I_{ds}}{\delta V_{ds}} \tag{4.5}$$

Drain output conductance is the slope of I_{ds} versus V_{ds} curve shown in Figure 4.10. Figure 4.10 (a) verifies the drain current versus drain voltage of graded channel device of L_g = 50 nm obtained using the analytical model by comparing it with the one presented in [52]. Figure 4.10 (b) compares the drain current versus drain voltage between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP for gate length of 80 nm. Figure 4.11 (a) verifies the drain output conductance of GC-DM-DG-JLFET-SP for 50 nm gate length. From Figure 4.11 (b), it can be observed that output current of UC-DM-DG-JLFET-SP increases in slightly steeper manner than GC-DM-DG-JLFET-SP for V_{ds} < 0.5 V and hence, it shows higher output conductance as shown in Figure 4.11 (b). For V_{ds} > 0.5 V, G_D for both devices becomes zero since drain current becomes constant as shown in Figure 4.10 (b). From Figure 4.11 (b), it can also be seen that at V_{ds} = 0.25 V, drain output conductance of GC-DM-DG-JLFET-SP is 1.557 mS/µm while that of UC-DM-DG-JLFET-SP is 2.611 mS/µm. As V_{ds} becomes greater than 0.5 V, I_{ds} becomes constant for both devices and as a result, G_D also becomes zero for both devices.



(a) (b)

Figure 4.10: a) Verification of drain current versus drain voltage of GC-DM-DG-JLFET-SP for L_g = 50 nm and b) Comparison of drain current versus drain voltage between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP for L_g = 80 nm



(a) (b)

Figure 4.11: a) Verification of drain output conductance of GC-DM-DG-JLFET-SP for L_g = 50 nm and b) Comparison of drain output conductance between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP for L_g = 80 nm

4.6.4 Intrinsic Gain (A_{V0})

Intrinsic gain of a device can be defined as [51],

$$A_{vo} = \frac{g_m}{G_D} \tag{4.6}$$

It can be depicted from Figure 4.12 that GC-DM-DG-JLFET-SP shows lower intrinsic gain compared to UC-DM-DG-JLFET-SP. At V_{ds} = 0.5 V, the value of intrinsic gain for graded channel device is 3.353×10^4 and that for uniform channel device is 4.027×10^4. As Figure 4.11 (b) shows that the value of G_D tends to very low and becomes zero for V_{ds} > 0.5 V, the value A_{V0} is too high for both devices which can be seen from Figure 4.12.

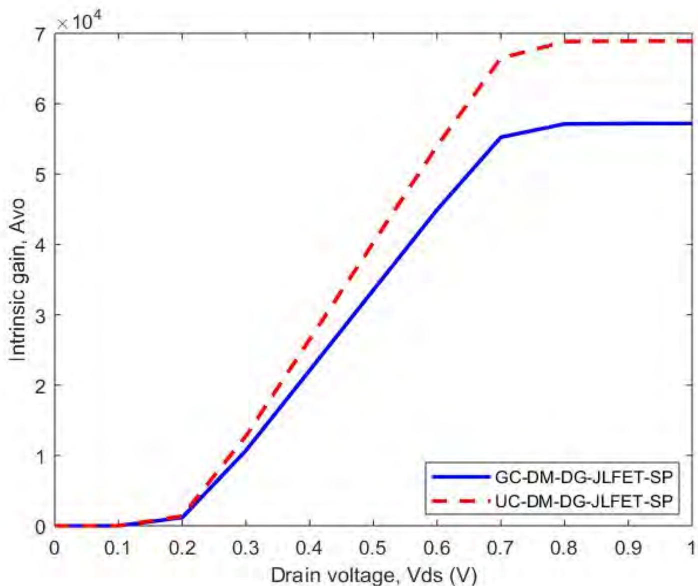


Figure 4.12: Comparison of intrinsic gain between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP for L_g = 80 nm at V_{gs} = 1 V

4.6.5 Early Voltage (V_{EA})

Early voltage is defined as [51],

$$V_{EA} = \frac{I_{ds}}{G_D} \tag{4.7}$$

Early voltage is the drain voltage at which I_{ds} versus V_{ds} curve intersects the negative V_{ds} axis and this can be achieved by extrapolating the I_{ds} versus V_{ds} curve in backward direction. The phenomenon of "early voltage" can be understood from Figure 4.10. Ideally, with the increase of V_{ds}, the drain current I_{ds} is expected to become constant. But as can be seen from Figure 4.10, the actual drain current slightly increases with the increase of V_{ds}. If we rewrite equation (4.7) as, $V_{EA} = \frac{I_{ds}}{\frac{\delta I_{ds}}{\delta V_{ds}}}$ or, $\frac{\delta V_{ds}}{V_{EA}} = \frac{\delta I_{ds}}{I_{ds}}$, so, $\frac{\delta V_{ds}}{V_{EA}}$ can be interpreted as the percent increase in drain current over its ideal value of constant drain current.

Figure 4.13 compares the early voltage between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP. As V_{ds} increases, graded channel device shows lower early voltage than uniformly

doped device. For V_{ds} = 0.7 V, the early voltage for graded channel device is 3.067×10^4 V and that for uniform channel device is 6.809×10^4 V.

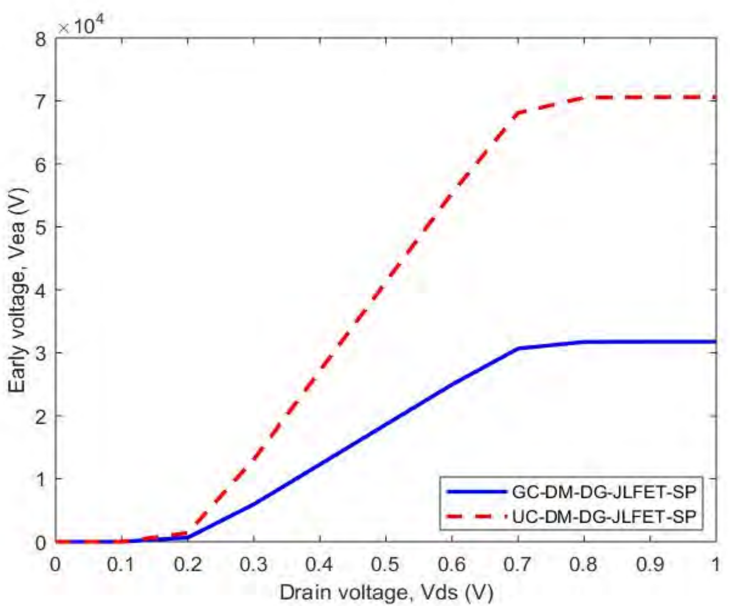


Figure 4.13: Comparison of early voltage between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP for L_g = 80 nm at V_{gs} = 1 V

Chapter 5

CONCLUSIONS AND SUGGESTIONS

This chapter draws conclusions by summarizing and discussing the results of this thesis work and provides with some suggestions which can be used for future researches.

5.1 Conclusions

In this thesis, a two-dimensional analytical model for graded channel dual material double gate junctionless field effect transistor with high-k spacer (GC-DM-DG-JLFET-SP) has been developed. The potential distribution under high-k spacer regions has been formulated by using conformal mapping technique to consider fringing field effect. The potential profile for channel region has been calculated by solving two-dimensional Poisson's equation and 1-D capacitance model. The derived model has been verified with the one developed by V. Pathak and G. Saini [52].

After verification, the developed analytical model of surface potential for GC-DM-DG-JLFET-SP has been used to calculate drain current, I_{ds}, using the appropriate formula. By using these two expressions of potential distribution and drain current, the on/off current ratio, two short channel effects – subthreshold swing (SS) and drain induced barrier lowering (DIBL) and parameters for analog performances – transconductance (g_m), transconductance generation factor (g_m/I_{ds}), drain output conductance (G_D), intrinsic gain (A_{V0}) and early voltage (V_{EA}) have been calculated later. These parameters have also been compared with those of uniform channel dual material double gate junctionless field effect transistor with high-k spacer (UC-DM-DG-JLFET-SP). It has been found that GC-DM-DG-JLFET-SP shows much lower off-state current and thus consumes lower power in subthreshold region than UC-DM-DG-JLFET-SP. Though graded channel device draws slightly lower on-state current than uniformly doped device, it has been observed that it shows 10^3 times higher on/off current ratio than uniformly doped device because of improvement in off-state current. When comparing short channel effects, GC-DM-DG-JLFET-SP shows lower DIBL and lower SS compared to UC-DM-DG-JLFET-SP. Again, when comparing the analog/RF performance curves between GC-DM-DG-JLFET-SP and UC-DM-DG-JLFET-SP, the graded channel device shows partially better g_m

(for higher gate voltage) and poorer g_m/I_{ds} due to less on-state current compared to uniform channel device. It also shows better G_D which leads to nominal degradation in intrinsic gain compared to the latter device.

So, considering the performance analysis done for two devices, it can be concluded that GC-DM-DG-JLFET-SP exhibits improved performance in off-state by suppressing subthreshold leakage and short channel characteristics. Though it shows poorer g_m, g_m/I_{ds} and V_{EA}, it has better drain output conductance and slightly lower intrinsic gain which is negligible. Thus, the graded channel device can be used for high frequency applications where subthreshold power consumption and short channel effects can be improved significantly while maintaining higher intrinsic gain.

5.2 Suggestions for Future Works

i. The derived model can be extended to analytically determine the threshold voltage, I_{ds}, DIBL, SS, g_m, g_m/I_{ds}, G_D, A_{V0} and V_{EA} which have been calculated numerically and using formulas in this thesis work.

ii. The presented thesis work which is done for symmetric device can be further modified by using asymmetric structure (different gate bias voltage and dissimilar material used for the gates).

iii. The performance analysis can be observed in more detail by varying doping concentration, oxide thickness, spacer width and dielectric material of spacer.

iv. Constant carrier mobility has been employed to calculate the drain current for our device. Field dependent mobility may be included for considering device transport characteristics.

v. The proposed model can be extended for III-V JLFETs.

vi. Incorporating Quantum Mechanical Effect (QME) in the channel region, a self-consistent analysis can be performed by developing Schrodinger-Poisson solver.

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