PHONON SCATTERED ELECTRON TRANSPORT CALCULATION OF JUNCTIONLESS NANOWIRE TRANSISTOR BY A COMPUTATIONALLY EFFICIENT ATOMISTIC APPROACH

A thesis submitted to the

Department of Electrical and Electronic Engineering (EEE)

of

Bangladesh University of Engineering and Technology (BUET)

In partial fulfillment of the requirement for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by

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BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY (BUET)

August 2019

The thesis titled "**PHONON SCATTERED ELECTRON TRANSPORT CALCULATION OF JUNCTIONLESS NANOWIRE TRANSISTOR BY A COMPUTATIONALLY EFFICIENT ATOMISTIC APPROACH**" submitted by Md. Samzid Bin Hafiz, Roll No.: 0417062204 P, Session: April 2017, has been accepted as satisfactory in partial fulfillment of the requirement for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on August 31, 2019.

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Declaration

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Dedicated to

My beloved parents

Acknowledgements

My heartiest gratitude is to my thesis supervisor, Prof. Dr. Quazi Deen Mohd Khosru, whose constant support and direction have made it possible for me to complete the research work. Starting from the time when I was introduced to research in my undergraduate up to now, he has always encouraged me to face new challenges in research and paved the way for overcoming the challenge. The experience and ideas that he has shared will guide me throughout my future research work as well. I am indebted to him for the freedom he provided while conducting my research work without which the period I have worked with him would not have been this much thrilling and enjoyable.

I also express my gratitude to Dr. Md. Shafiqul Islam, Head, Department of Electrical and Electronic Engineering (EEE), BUET, for endowing me with a perfect ambiance for continuing my research. My thankfulness also extends to EEE department for granting the required tools and guidance so that not only me, but also all students can thrive in their search for truth and knowledge.

I would like to thank the members of my thesis committee, Prof. Dr. Shafiqul Islam, Dr. Md Zunaid Baten and Prof. Dr. Md. Anwarul Abedin for their constructive suggestion on future improvement of my work.

Last, but not the least, I want to acknowledge the support, enthusiasm and love of my parents that has given me the mental strength to stick towards such a challenging research work.

Abstract

In this thesis, electronic transport characteristics of Junctionless Nanowire Transistor (JNT) in presence of phonon scattering has been studied. JNT is a novel electronic device, which has no distinct p-n junction and no doping concentration gradients in its structure. As the channel length of MOSFETs scales down, the formation of ultra-shallow source/drain junctions poses difficult fabrication challenge. The JNT overcomes this difficulty as it has no p-n junction. The device contains a doped Silicon channel region surrounded by two Poly gate structures on opposite directions, separated by an oxide layer on each side. As gate voltage is increased, the induced depletion region reduces, and as voltage exceeds threshold, the channel conductance commences. For voltage over flat-band, the device operation switches from depletion to accumulation mode. The current-voltage characteristics of the device closely resemble that of MOSFET. The device, free from doping gradient optimization constraints, can support further scaling down of the device structure than traditional FETs. The device also exhibits better non-ideal short channel and subthreshold characteristics, along with superior high temperature operations. Instead of conventional effective mass approach the quantum mechanical atomistic tight binding method has been used in this thesis. The effect of phonon scattering on electronic current has also been studied. In this thesis, the atomic scale calculations were performed in Python scripting via QuantumATK software. Electronic band structure, transmission spectrum and projected local density of states were observed. The phonon band structure, phonon density of states and phonon transmission spectrum were also observed. The elastic and inelastic component of current were analyzed. The inelastic current distribution due to various phonon modes was explained. Then the total current of the device with varying gate and drain voltage was calculated. The drain current vs gate voltage was evaluated by varying oxide thickness, channel thickness, channel length, doping concentration, and channel material crystal orientation. Finally, the simulation approach was verified by comparing with other results.

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Chapter 1

Introduction

1.1 Preface

The central component of semiconductor electronics is the integrated circuit (IC), which combines the basic elements of electronic circuits - such as transistors, diodes, capacitors, resistors and inductors - on one semiconductor substrate. The two most important elements of silicon electronics are transistors and memory devices. For logic applications MOSFETs are used. MOSFETs have been the major device for ICs over the past two decades. With technology advancement and the high scalability of the device structure, silicon MOSFET based very-large-scale integrated (VLSI) circuits have continually delivered performance gain and cost reduction to semiconductor chips for data processing and memory functions.

The invention of first transistor at Bell Laboratory (Shockley's group) in 1947 was followed by the integrated circuit era. The minimum critical feature size (physical gate length) of MOSFET has been successfully reduced by more than two orders of magnitude according to Moore's law until now and International Technology Roadmap of Semiconductors 2013 (ITRS) recently foresaw that the minimum feature size will still decrease from 20 nm in 2013 to around 8 nm in 2023 [1].

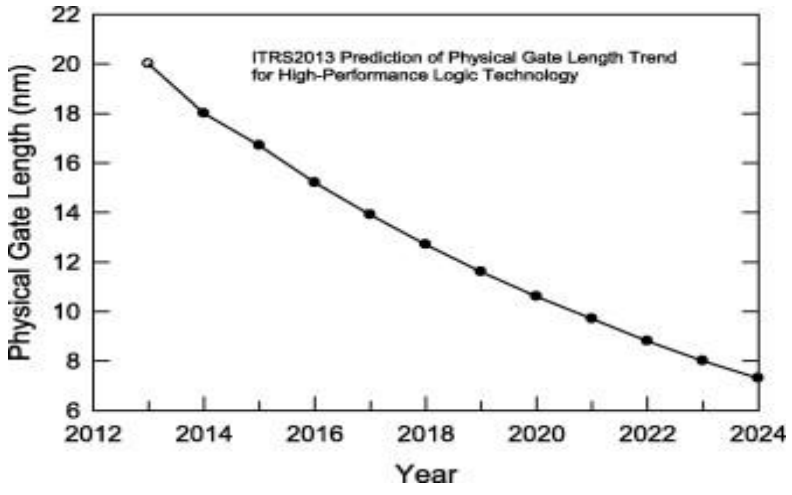

Figure 1.1: Scaling trend of high performance logic technologies with year [1]

However, as the feature size decreases, i.e. device is scaled further, short channel effects become highly significant. The Sources of short channel effects of MOSFET can be attributed to two distinct physical phenomena: channel electron drift characteristics limitations due to scaling and the alteration of the threshold voltage due to the shortened channel length. The five major short-channel effects include [2]: 1. Drain-Induced Barrier Lowering (DIBL), 2. Surface Scattering, 3. Velocity Saturation, 4. Impact Ionization, 5. Hot Electrons Effects.

Such non-ideal effects are detrimental to the proper gate control of MOSFETs. However, recent studies show that multi-gate nanowire structure can be used to improve gate control against short channel effects to the highest degree [3]. According to the term proposed by Yan et al. in 1992 [4] and improved by Suzuki et al. in 1993 [5], a device can be considered free of short-channel effects if the gate length is at least 6–10 times larger than the Natural Length (λ). In case of multi-gate nanowire structure, a term called Effective Number of Gates (n) can be introduced which also depends on threshold voltage and semiconductor film thickness, which in turn decreases the effective natural length of the device.

So, a multi-gated structure can be used for better gate control against short channel effects. For example, the novel device Multi-Gate-FET (MuGFET) shows significant improvement in DIBL [6]. The MuGFET also shows better high temperature performance for both long and short channel devices [7]. JNT, also known as Junctionless MuGFETs can also demonstrate similar properties.

The existing metal-oxide-semiconductor field-effect transistors are composed of pn junctions in the source-channel-drain path. The p-n junctions allow or block current through it according to the applied bias on the gate. Junctionless transistor (JLT), which does not have pn junction in the source-channel-drain path, has recently been reported by Colinge's group at Tyndall National Institute,University College Cork, Ireland [8] following the idea of the first transistor by Julius EdgarLilienfield in 1925 [9-10]. Lilienfield patented his work under the title "Device for controlling the electric current". It consists of a thin semiconductor film deposited in a thin insulator layer, itself deposited in a metal electrode (gate). Thus, it does not have a junction; rather it is a simple "resistor". It is also called "gated trans-resistor". In principle, current flows in the resistor in the same way that drain current flows from drain to source in a MOSFET. Junctionless transistor is basically an accumulation mode device with a very thin silicon thickness (~5-10 nm). The requirement of thin semiconductor layer is to have full depletion of carriers when the device

is turned off. Therefore, JLT offers good sub-threshold characteristics. However, a typical accumulation mode device is made in relatively thick silicon films (typically higher than 20 nm or so) and hence it exhibits worst short channel performances. However, one advantage of accumulation mode transistor is, drain current varies less with channel doping concentration. The other major difference of JLT with accumulation mode transistor is that in the former, accumulation of carriers happens at a higher threshold voltage than the later device. The junctionless transistor which is also called "gated resistor" or "nanowire pinch-off FET" is highly doped (typically ~8×1018 cm-3 to 8×1019 cm-3) to have an acceptable drain current. Commonly, a junctionless transistor has same doping concentration at source, channel and drain regions. Thus, the structure of a JLT is N+ – N+ – N+ for n-channel and P+ –P+ –P+ for p-channel in the source-channel-drain region. P+ and N+ polysilicon gates are used for n and p channel JLT respectively (N+/ P+ denote highly doped with N/P-type dopants respectively). However, non-uniform doping in JLT has also been reported; to obtain superior ON-state to OFF-state current ratio (ION /IOFF) compared to uniformly doped JLT [8].

JLTs have many advantages over conventional MOSFETs such as – better SCE performance (reduced drain induced barrier lowering (DIBL) and sub-threshold slope (SS) degradation) resulting better scalability, lesser sensitive to doping fluctuations and negative bias thermal instability, greatly simplified process flow and low thermal budgets after gate formation resulting in flexibility in the choice of materials for gate dielectric and gate metal etc. [6, 8, 11]. Because of uniform and homogeneous doping in the channel region, a JLT eliminates the subsequent annealing process and the device can be fabricated with shorter channel lengths. In addition, JLTs offer low standby power operation and low gate induced drain leakage [6, 12-13]. Also, lesser fabrication steps reduce process cost significantly compared to junction based devices of similar dimension [14]. JLTs exhibit lesser random telegraph-noise [15] and 1/f noise [16]. JLT has fully CMOS compatibility. With constant device dimensions scaling, the effective gate oxide thickness decreases. This increases vertical electric field according to Takagi et al.'s relation $\mu \approx E^{-0.3}$ [17-18]. The inversion carrier mobility in a conventional MOSFET is reduced because of vertical electric field. For example, when technology node changes from 0.8 μm to 0.13 μm, mobility decreases from 400 to 130 cm2/V. The vertical electric field in a JLT is much lower compared to junction based MOSFET and accumulation mode devices as discussed below. Therefore, mobility

in a JLT is not reduced much because of vertical electric field [19]. The conventional junction based device is normally an OFF device, as the drain junction is reverse biased. It prevents current flowing through the device. To turn the device on, an inverted channel is created by applying a gate bias. However, a JLT is normally an ON-device. The work-function difference between the gate electrode and silicon nanowire (~1.1 eV) shift the flat-band voltage and turns the threshold voltage into a positive value. In the ON-state, the device is in flat-band condition. Therefore, there is zero vertical electric field perpendicular to the current flow. Unlike in a junction based transistor where conduction mechanism is surface based; in a JLT, current basically flows through bulk conduction mechanism. The threshold voltage depends on doping, equivalent oxide thickness as well as on the width and thickness of the nanowires [20]. In a JLT, the OFF-state current is determined solely by the electrostatic control of the gate and not by the leakage current as is the case for junction based device. This makes JLT lesser sensitive to contamination [6]. Junctionless transistor is studied theoretically with single, double, triple and gate-all-around architectures; and fabricated with triple and gate-all-around architectures.

However, along with the many advantages that JLT offers as aforementioned, it has some disadvantages as well. One of the most important drawback of JLT is it suffer from lesser ON-state current (ID) and hence trans-conductance (Gm) compared to IM MOSFETs due to its inferior mobility (due to high doping concentration (ND) in channel region) [21]. Also, to have a highly doped uniform channel with such small thickness (~ 5–10 nm) is extremely challenging and expensive for non-planer kind of structure. The higher channel doping concentration to accomplish higher ON-state current makes threshold voltage variation with doping concentration as well as nanowire width [22-23].

The benefits of JNT offsets the shortcomings. Its fabrication simplicity along with less short channel effects make JNT one of the most potential device of 21st century.

1.2 Literature Review

The first junctionless transistor structure was designed and patented by J. Lilienfeld in 1925. He patented his so called "Lilienfeld Transistor" in USA under the name of “Device for controlling electric current" [9]. It was a Field-Effect-Transistor containing a thin semiconductor film deposited on a thin insulator layer, which was in turn deposited on a metal electrode. The device was basically a gated resistor. However, unlike traditional MOSFET or BJT structures, the device did not include any explicit p-n junction [24]. However, due to lack of proper processing technology and material fabrication constraints, up until 1950, the device did not see a working model to be constructed.

The multigate nanowire transistor idea was first pitched by Colinge et al. in 1995 [25]. They dubbed it as the Silicon-on-Insulator (SOI) Quantum Wire. They implemented the device structure on a so-called Quantum Wire. Seven parallel devices were connected for better Signal-to-Noise-Ratio (SNR) margin. Classical 3D DAVINCI simulation was utilized to determine I/V relations of seven nanowire devices in series. The study reported I/V relationship closely related to the MOSFET one, containing non-idealities due to irregularities in sub-band population time. It was also observed that better current density can be found for higher temperature at constant voltage. However, this was not in fact a junctionless device, but a precursor to nanowire structures.

The Junctionless device in question was also the result of studies performed by Colinge et al. in 2009. Along with Lee et al., they formulated the first model of a Tri-Gate JNT (TG-JNT) [6]. They proposed a device with Triple-Gate structure enclosing n type Si channel with no effective p-n junctions. The internal structure roughly contained an n-doped semiconductor channel connected with the gate via a thin oxide layer similar to a standard FET structure. Hence, no distinct p-n junction was present within the structure. ATLAS 3D simulations were performed to study device properties. Due to its junctionless structure, doping gradient problems were eradicated significantly. They also studied the non-ideal properties and compared it against MOSFET to find to be superior. The DIBL and subthreshold slope of JNT improves significantly compared to

traditional FETs. The study performed detailed analysis of JNT device properties and relative merits and demerits.

In 2010, a more detailed study was performed by Colinge et al [8]. SOI technology was used to construct the device. They coined the name Junctionless Nanowire Transistor (JNT) as well as Gated Resistor. The study determined the theoretical I/V relationships and found it to be comparable of that of a MOSFET. Moreover, the on-off current ratio was found to larger, and also the off current is under the detection limit. The non-ideal effects regarding subthreshold conditions are hence heavily reduced. The subthreshold slope was, in fact, found to be the best observed quantity up to that point for any device, which remains fixed for a wide temperature range. The authors also formulated 3D simulation of channel charge variation using simulator and the study also found the delay profile of JNT to be superior to MOSFET. However, due to channel core current flow away from the surface, observed channel mobility is significantly lowered compared to similar MOSFET devices.

Colinge et al. followed up their study in 2010 by studying a double-gate structure of JNT (DG-JNT) [26]. They studied device physics and SOI based structure. Quite significantly, the double-gate structure of JNT was first introduced in this study, rather than traditional triple gate structure. In this study a more in-depth analysis of device physics and internal operations were discussed. They also reviewed the variation of threshold voltage with variation of silicon width and thickness and found it to be inversely related. The use of undoped channels in thin SOI devices of multigate FETs has been shown to minimize threshold voltage variations caused by random impurity fluctuation effects. Subthreshold characteristics were also studied. But no atomistic study is done here.

Additionally, the feasibility of a Bulk Double-Gate Junctionless Transistor Device was discussed in the study under discussion [26]. For n channel device, a p type substrate was advised to use for bulk implementation for proper device isolation and fabrication. Hence the device is no longer junctionless in the strictest sense, although the current flow path still does not have to cross any junctions, and the device still exhibits every advantage of previously discussed structure. The

DIBL performance of the bulk JNT can be found to be similar to that of the SOI JNT. The subthreshold slope of the bulk JNT, on the other hand, is more degraded at short gate length than in the case of SOI devices.

In 2010, Lee et al. studied the effect of High Temperature on JNT [21]. It was observed that the use of the MuGFET structure can reduce the temperature dependence of the threshold voltage when narrow silicon fingers are used due to the reduction in the surface potential variation with the temperature. The study observed the fact that in JNT, no Zero Temperature Coefficient (ZTC) point exists, resulting in monotonic current increase. This phenomenon results in possible better JNT operation under high temperature constraints. However, the off-leakage current increases with temperature because of the increase of intrinsic carrier concentration, which increases both diffusion and generation currents. Here, DIBL at high temperature is dominated by Band-to-Band Tunneling (BBT), rather than Band-to-Defect Tunneling (BDT) as in the case of MOSFETs. Hence, the usual non-ideal effects at high temperature are less significant for GAA-JNT as well.

Colinge et al. studied the Electric field variation of JNT in 2010 [19]. The Effective Oxide Thickness (EOT) variation with scaling causes increase in the Vertical electric field of a transistor, resulting in high carrier scattering, and hence decreasing mobility. When the JNT device is turned on, it is in flat-band condition, and hence, there is zero electric field in the directions perpendicular to the current flow direction. As a result, transconductance decreases less rapidly with high voltage for JNT compared to FET.

Lee et al. also studied the subthreshold slope characteristics of JNT in 2010 and compared it against MOSFET [27]. The subthreshold slope of a device limits the on-off current ratio of a device, which has the theoretical minima at 60 mV/decade for MOSFETs. For simulation, ATLAS simulator was utilized. The simulation showed increased electron temperature but decreased ionization rate for similar slope, resulting in increased efficiency. Under subthreshold conditions, in case of JNT, the drain potential drop is found inside the drain electrode, outside of the region covered by the gate. Hence the entire channel region is pinched off, and bulk of the drain potential drop is found in the

drain, near the gate electrode. The region over which impact ionization takes place is found to be much larger in the junctionless devices than a MOSFET, reducing Drain to Source voltage considerably. However, TG-JNT structure can be used to find better characteristics.

In 2010, Ansari et al. reported a Si Nanowire GAA-JNT with 3 nm gate length and 1 nm wire diameter [29]. This study considered the GAA-JNT structure with 3.1 nm feature size, scaled down from 1 μm one from previous studies, and hence shifting device properties to complete Nanoscale range. They also implanted a very high doping density in the scale of $8x10^{20}$ atoms/cm^3. The simulation was performed via full quantum mechanical treatment using Density Functional Tight-Binding ($DFTB^+$) Method, parameters calculated via Density Functional Theory (DFT) over an 800-atom supercell. Mulliken Population Analysis was performed to calculate the localized charge density. The analysis shows adequate carrier density even under undoped channel conditions, which is unlikely for both similar scale MOSFET and larger JNT devices. However, de-localization would make the junctionless design more robust against dopant fluctuations. The observed I/V characteristics were in accordance with results obtained for larger feature size. Also, the positioning of the dopant in the wire cross section makes a difference in the band structure of the device, which results in steeper I/V relation at low bias. Even though atomistic calculations are done but there is no electron phonon coupling analysis.

In 2011, Su et al. proposed a novel junctionless structure with Polysilicon nanowire channel [32]. For the first time in the world, the authors experimentally investigated the feasibility of GAA polycrystalline silicon (poly-Si) nanowire transistors with junctionless configuration by utilizing only one heavily doped poly-Si layer to serve as source, channel, and drain regions in a GAA-JNT structure. The formation of cavities was carried out by carefully controlling the lateral etching of the Tetraethyl Orthosilicate (TEOS) oxide layer in dilute HF solution. High Resolution Transmission Electron Microscopic (HRTEM) Image was obtained to study the designed model. Better I/V characteristics than a MOSFET structure was observed for this model. A very high trans-conductance was also observed compared to the IM device. Channel resistance also decreases considerably, which increases with channel length for obvious reasons.

In 2011, Trevisoli et al. derived a mathematical model of threshold voltage of TG-JNT solving 2D Poisson's equations along with Schrödinger equation solutions, and observed its dependence on the nanowire width, height and doping concentration [33]. A 3D TCAD Numerical Analysis was performed for this purpose. Corner effects were also modeled, and temperature dependence was analyzed. A mathematical model was derived and used to simulate such device properties. Self-Consistent analysis was performed to obtain an analytical formula for Threshold voltage as a function of flat band voltage. A formula for gate oxide capacitance was also discussed. Also, Altermatt Model was used to measure variation of threshold voltage with temperature. Threshold voltage variation with temperature was found to be almost linearly decreasing, while the decrease was way steeper with doping concentration. However, the analytical equations used here aren't as accurate as quantum mechanical equation for short channel devices.

In 2011, Choi et al. studied the sensitivity of threshold voltage to nanowire width variation in case of Gate-All-Around Junctionless Transistors (GAA-JNT) [34]. A 2D ATLAS simulation was performed to determine the parameters. The simulated results suggested that the comprehensive analysis of the threshold voltage fluctuation caused by both the RDF and width variation is required. The performed ATLAS simulation was followed by observed I/V relationship analysis and variation of threshold voltage with dopant density and process variation. They found the threshold voltage to linearly decrease with increasing width and dopant density for JNT, unlike MOSFET, where the variation is a more complex function of both parameters. However, structural optimization is essential to eliminate constraints in the possible applications of junctionless transistors.

Duarte et al. performed drain current modeling analysis of Double Gate JNT in 2011 [36]. A depletion approximation was used to solve the Poisson equation in the channel in a similar manner performed in accumulation-mode transistors. Simplified Taylor Series expansion was utilized and higher order reduction approximation was performed. Ohm's law was used to model channel current profile. Then a 2D ATLAS simulation was performed via Lombardi Mobility Model, while Fermi–Dirac carrier statistics was also included. Resulting simulation, under narrow range of

convergence, had reasonable outcome. Here, their piecewise approach at current modeling, which, albeit simple, had serious convergence problems.

In 2011, Duarte et al. improved on their previous crude attempt at current modeling [37]. In this study, by extending the parabolic potential approximation above the subthreshold region and using Pao-Sah electrostatic assumptions, a 1-D continuous charge model was developed for a symmetric long-channel Double Gate JNT, considering the dopant and mobile carrier charges. Using self-consistent analysis Charge Model was defined and solved to obtain the charge distribution profile of the device channel. Drain Current Model was obtained by integrating the continuity equation via drift-diffusion analysis. Finally, 2D ATLAS simulation was performed using Lombardi Mobility Model, accounting for the temperature, doping, and field-dependence effects. The Fermi-Dirac carrier statistics, along with standard recombination models were also included. The study resulted in an improved analytical expression of channel current density. Even though the convergence problem is improved here, the simulations aren't based on Quantum mechanical approach.

The ballisticity of transport mechanism through JNT channel is studied by Akhavan et al. in 2011 [38]. This study shows that JNT exhibits lower degree of ballisticity in subthreshold and higher ballisticity above threshold compare to conventional inversion-mode transistors due to quantum mechanical effects. The lower degradation of the ballisticity above threshold region gives the JNT near-ballistic transport performance and hence a high current drive. On the other hand, lower ballisticity in subthreshold region helps reducing the off-current and improves the subthreshold slope. In the presence of optical phonons, the JNT shows improved performance through reduced phonon scattering above threshold and increased phonon scattering below threshold, which gives JNTs a higher on-off current ratio than conventional IM transistors. However the calculations aren't computationally efficient due to self-consistent Born approximation method for calculating electron phonon coupling.

The Low frequency noise profile in TG-JNT channel was studied by Jang et al. in 2011 [39]. Static and noise measurement were simultaneously performed in a dark box at room temperature. The carrier number fluctuations related to the conduction process were mainly found to be limited by

the bulk expecting Hooge Mobility Fluctuations. The trapping-release ratio of charge carriers was found to be related not only to the oxide-semiconductor interface but also to the depleted channel. The volume trap density was observed to be similar to Si-SiO_2 bulk transistors and remarkably lower than in high-*k* transistors. The relative contribution of the noise sources was observed as a diagnostic index the uniformity of the line width of the channel. Hence, the noise originating from the surface conduction could not be observable.

In 2012, Mariniello et al. studied the variation of gate capacitances of a TG-JNT with respect to various parameters in detail [40]. They derived a model for gate capacitance of JNT and a mathematical expression was also obtained. They observed the variation of gate capacitance with respect to applied Gate voltage for various device size and doping density constraints. They also studied the gate capacitance variation with the variations of such parameters, namely device width, thickness and doping concentration of the channel. The study shows a decrease in gate voltage requirement with increase of channel width, thickness and doping concentration, as expected. Also, such increase stretches the capacitance curves to the depletion region. A reduction in corner value of gate capacitance is also observed for increase in doping or channel dimensions. However the simulation results are only for long channel devices.

In 2012, Ansari et al. improved their study of subthreshold characteristics by incorporating atomic scale simulations [41]. The simulations predict that the junctionless transistor performs well near atomic limits, turning off with source-drain leakage. The calculations indicate that the dopant atoms are energetically more favorable on surface sites. However, by decreasing the doping concentration the effect of surface doping can be reduced. The basic operating principle of the junctionless Si NW is robust against dopant fluctuations on this length scale. Suppression analysis of the transmission near the Fermi level for higher gate voltages were performed, yielding a surprisingly good predicted subthreshold slope for transistors with a gate length of only 3 nm. But no electron phonon coupling effect was considered.

Very recently, Lou et al. (2012) proposed a novelization of JNT device, namely DualMaterial-Gate Junctionless Nanowire Transistor (DMG-JNT) [42]. The DMG-JNT structure combines the advantages of JNT and DMG structures. The structure has two distinct gates, namely Control Gate

and Screen Gate, with a GAA-JNT structure. The two gates have separate work functions. The two gates have equal physical dimensions and mounted side-byside, with equal feature size. The density gradient model applied was utilized to account for the quantum effects. The ON-state current seemingly improved, as well as transconductance. The potential distribution of a DMG-JNT could be observed to contain an abrupt change near the transition of the two gates, whereas that of the SMG-JNT increases monotonically from the source to the drain. The abrupt change is caused by the difference of gate work function of the DMG-JNT. The potential drop across the source/drain extensions in the DMG-JNT is larger than that in the SMG-JNT, which indicates that the channel ON-state resistance of the DMG-JNT is smaller than that of the SMG-JNT. Furthermore, The DMG structure is more effective in reducing the drain channel field, which in turn suppresses the short-channel effect and the hot-carrier effect in JNT. The saturation current is hence higher in DMG-JNT. The on-off current ratio also improves as DIBL decreases. Due to suppression of DIBL, higher cutoff frequency was also observed. The device hence has high potential in high frequency applications. Hence, Drift–diffusion based TCAD simulation without impact ionization was performed.

A more detailed study regarding analytical modeling of Double-Gate JNT was performed by Hwang et al in 2015 [55]. Regional analysis was performed in order to study device properties under different biasing modes. NEGF based self-consistent analysis was performed to obtain charge distribution and potential profile. Finally, a TCAD based simulation was performed in order to verify analytical assumptions and provide visual aids. Drain current, electric field, charge density, channel voltage and transconductance were compared against variation in gate voltage. However, the study mostly revolved around long channel devices.

In 2012, Chen et al. designed the drain current model of long channel JNTs using detailed mathematical analysis [43]. For analysis, they studied a dual-gate JNT structure. Regional approach was used to establish the relationships between surface potential and gate voltage by a separate consideration of the accumulation, partial depletion, and deep depletion conditions. With the derived surface potential model, the Pao-Sah Integral was analytically obtained, which led to a full-range drain current model. In particular, Lambert W-function was used to express the subthreshold current. The model was next validated via TCAD tool Sentaurus Device. Due to the

long-channel device, the Lombardi Mobility Model is employed, accounting for the dependence on the impurity concentration as well as the transverse and longitudinal electric field values. The simulated I/V relationship regarding both drain and gate voltage closely resembles the theoretical assumptions. The derived expressions account for the numerous advantages of JNT, namely, steeper subthreshold slope and DIBL, as well as higher on-off current ratio. It also shows a reduction in channel mobility. But the device calculations are only for long channel devices.

The study was modified for Short Channel JNT devices by Gnudi et al. in 2013 [44]. Here, an analytical solution for the potential was worked out that removes the limitations described above and provides potential distributions in the channel that compare favorably with TCAD simulation results, even for very short gate lengths. First Electrostatic Potential Model was used to find normalized electron wave function in the channel. A TCAD simulation was performed to observe the validity and feasibility of the model. The I/V relationship and energy band structure with coordinates were modeled for various channel size. The simulation found the agreement between theory and experiment to be very concrete. Also, Drift-diffusion analysis was utilized in order to perform Channel Current Analysis, which resulted in a compact model of current characteristics profile. Variations of Threshold voltage and subthreshold conditions with respect to the channel length were also studied. But the Drift-diffusion model isn't as accurate as quantum mechanical method.

There have been several developments of atomic-scale models along with nonequilibrium Green's function (NEGF) formalism. Simulation of junctionless Si nanowire transistors with 3 nm gate length based on DFT and NEGF assuming ballistic transport has recently been demonstrated [10]. Source-to-drain tunneling leakage current in nanowire transistor is investigated based on atomistic approach. However, these calculations ignore electron phonon interaction when calculating transport characteristics. But short channel JNTs also suffer from phonon assisted source-drain (S-D) quantum tunneling leakage current which is ignored in existing transport calculations. Source-to-drain quantum tunneling leakage current deteriorates the I_{ON}/I_{OFF} ratio and subthreshold swing in ultra-scaled devices. In short, atomistic quantum approaches with NEGF formalism considering electron phonon coupling for the transport calculation of short channel JNT has not been reported yet.

1.3 Objective of the Thesis

The aim of this research is to find out the electronic transport characteristics of GGA-JLT in presence of electron-phonon coupling as follows:

- To design a computationally efficient device algorithm using atomistic quantum approach with NEGF formalism incorporating electron phonon coupling.
- To investigate the short channel effects such as subthreshold slope (SS), threshold voltage roll-off, I_{ON}/I_{OFF} ratio, drain induced barrier lowering (DIBL) etc. in the short channel junctionless nanowire transistor.
- Study the effect of source to drain quantum tunneling leakage current in transport characteristics of JNT.

1.4 Organization of the Thesis

The works presented in this thesis has been organized as follows:

- In **Chapter 1 (**Introduction): I have presented introduction and motivations of my research work. I briefly discuss the device properties and its advantages over the traditional transistors. In Literature Review, I present the previous studies performed to get a better view on the state of the art. The Thesis Objectives are then stated.
- In **Chapter 2** (Device Structure and Operating Principle)**:** Firstly, I discuss the basic structure of a standard GAA-JNT device, its internal components and the materials used in its production in depth. I also present schematic model of the device for better understanding of its internal structure and operations. Then the basic operating principles of the device is discussed where I show the variations of energy band structures and carrier distributions with applied external voltage and how it affects the device operations and hence defines its characteristics. The usual fabrication strategies undertaken for the fabrication of the JNT is discussed. Although, no fabrication endeavor was executed throughout this study, standard practices are included for better perception. Then the major advantages observed for GAA-JNT over traditional MOSFET are discussed briefly. Elimination of Doping Gradient in JNT represents its better scaling potential. Reduction of

Short Channel Effects in JNT means it has improved non-ideal effects. Improved High-Temperature Operations and improved ON-OFF current ratio of JNT is then stated. The JNT has also improved Subthreshold Characteristics.

- In **Chapter 3** (Methodology): I discuss the methods required to obtain the device characteristics. The chapter is divided into three sections. The first section details the method used to describe the electronic structure of the systems investigated. In the second section the non-equilibrium Green's function (NEGF) method for quantum transport is introduced. In the third section calculation of the effect of lattice vibrations (phonons) on the electronic current is discussed.
- In **Chapter 4** (Simulator Implementation): I discuss the implementation of the methods discussed in chapter 3. The atomic scale calculations are done with QuantumATK software using Python scripting. At first the electronic structure of the device is calculated through atomistic approach. The semi-emperical tight binding Slater-Koster model is used. Then the effect of vibrations (phonons) on the electronic current is calculated using Inelastictransmissionspectrum module.
- In **Chapter 5** (Result and Discussion): The results of our simulations with detailed explanations are presented. Firstly, I summarize all the simulations performed in the course of this study. The electronic band-structure of the device is presented. Then the transmission spectrums of the device on three states: (OFF, Sub-threshold, ON) are discussed. Projected Local Density of States of JNT at three states are also discussed. Inelastic current distribution due to various phonon modes of the device on various states are then shown. Phonon band-structure, phonon transmission spectrum and phonon density of states are then demonstrated. Then I have shown the drain current vs gate voltage and drain current vs drain voltage curves with and without electron-phonon scattering. The drain current variation due to oxide thickness, channel thickness, channel length, doping and channel orientation are then discussed thoroughly. Finally, the benchmarking of the results is done by comparing with the results from another approach and the results from previous literature.
- In **Chapter 6** (Conclusion): I summarize the main results of the thesis and give an overall outlook. The future scope of this thesis is then presented.

Chapter 2

Device Structure and Operating Principle

2.1 About the Device

In this chapter the structure and operating principles of Junctionless Nanowire Transistor (JNT) will be discussed. JNT is a novel electronic device, which operates similarly as a traditional FET device despite containing no distinct p-n junction in its structure. Although introduced recently, Junctionless nanowire transistors (JLTs) recently gained much interest as a promising candidate device in the nanoscale transistor industry due to fabrication simplicity and its figure of merits over improved short-channel operation such as reduced threshold voltage (Vth) roll-off and drain induced barrier lowering (DIBL). The device mainly consists of a doped semiconductor channel, encapsulated by poly silicon gate from all directions (gate all around structure). Moreover, in contrast with the inversion-mode (IM) transistors, the majority carriers can carry the current, and an ultra-sharp p-n junction between silicon channel and source(S)/drain(D) is no more required because it consists of the constant doping concentration from S to D. As a result, the cost of device fabrication and the complexity of process can be much reduced compared to IM transistors.

2.2 Basic Structure of the Device

The Gate all around Junctionless Nanowire Field Effect Transistor (GAA-JLNWFET or GAA-JNT in short) device structure contains three major regions: the Channel, the Gate and the Insulator.

The channel is the conducting path of JNT device. For nanowire devices the channel usually is fabricated from highly doped p or n type semiconductor material. No distinct p-n junction is present in the channel region in the path of current flow. The device properties change polarity along with dopant material. That is, the applied voltage polarity for activation and direction of current flow switches side along with dopant polarity. For simplicity, the n-channel JNT can be compared with the NMOS structure, while p-channel JNT is to be compared against PMOS. Here, I confine my study within the scope of n-channel GAA-JNT devices.

In junctionless transistors doping density of channel, source and drain are kept same. There is no need for doping gradient between channel and source/drain. Thus, fabrication is much simpler than other junction nanowire transistors.

There are two terminals along two distinct edges of the channel: the Drain terminal (D) and the Source terminal (S), referring to the identically termed FET terminals. The terminals are completely identical and interchangeable, even during device operations like usual FET structures. In case of n-channel JNT, similar to FET notations, the terminal with higher voltage is referred to as the Drain terminal, and the lower one is termed as the Source. If terminal voltage is switched during operation, the terminal polarity switches sides as well. However, in case p-channel device, the lower voltage terminal is termed as the drain, and the higher one as source, in compliance with the PMOS notations. The channel current flows from drain to source for n-channel devices, and hence it is often termed as the Drain Current. For p-channel devices, the direction is reversed.

The channel can be prepared using almost any semiconductor available for fabrication. Su et al. even recently proposed a novel junctionless structure with Polysilicon nanowire channel [32]. However, due to the unique device structure and operating principles, the effective mobility is lowered for JNT devices compared to FET ones. Hence high mobility semiconductors should be preferred while designing a GAA-JNT channel structure. However, for cost and feasibility considerations, initial studies of the device have been constrained within Silicon based semiconductor channel structure. In our study we have chosen Silicon (Si) channel with Arsenic (As) doped n-type structure. We had [110] oriented Silicon wafer with transport direction in the [110] direction.

The Gate is the controlling element of the JNT device. The Gate Terminal (G) of the device together with the Drain and Source terminals, complete the three terminal structure of the transistor. Similar to its namesake, the Gate terminal of FETs, the gate of JNT perform similar functions [8]. That is, the gate acts as the switching regulator of the transistor. When and only when, a significant voltage is applied at the gate terminal, the device turns ON, and constant current flows through the channel. The limiting value is generally dubbed as the Threshold Voltage of the device. Also, in case of JNT, the Flat-Band Voltage acts as the Corner Voltage of the device.

In a GAA structure, the channel is covered from all four directions with the gate structure. The gates are placed along a plane perpendicular to current flow. I.e. if current flow is considered to be along Z axis, the gates are placed along XY plane. With the variation of gate voltage, the channel surface charge density along XY plane varies, turning the device ON or OFF or keeping in between. In our work we studied about cylindrical gate all around junctionless nanowire transistor (CGAA-JNT).

The multigate structure exhibits several improvements over traditional single gate structures. Recent studies show that multi-gate nanowire structure can be used to improve gate control against short channel effects to the highest degree [3]. A multi-gated structure can be used for better gate control against short channel effects. The GAA Structure provides best utilization of the advantages of multigate structure.

Various materials can be chosen for gate fabrication. Classic metal gate structure is still feasible, although current trend of Poly gates, i.e. p+ or n+ Polysilicon gates are better well suited for device fabrication. Here, I have considered a p+ Polysilicon gate structure for n-channel device.

In JNTs, an insulator layer separates the Gate structure from the channel. The insulator should have low conductivity for proper device operations. Also, for reducing lattice mismatch while fabrication, the device should have closely matched channel and insulator material. Almost universally, the Oxide or Nitride layer of the channel semiconductor is used as the insulator material. In accordance with the stated practice, an all around the channel structure for the thin layer of oxide is considered which is grown on the channel, separating it from the p+ Polysilicon Gate structures. I have considered Hafnium dioxide (HfO_2) and Silicon dioxide (SiO_2) for the oxide layer and investigate the performance of both the oxides in the current voltage characteristics.

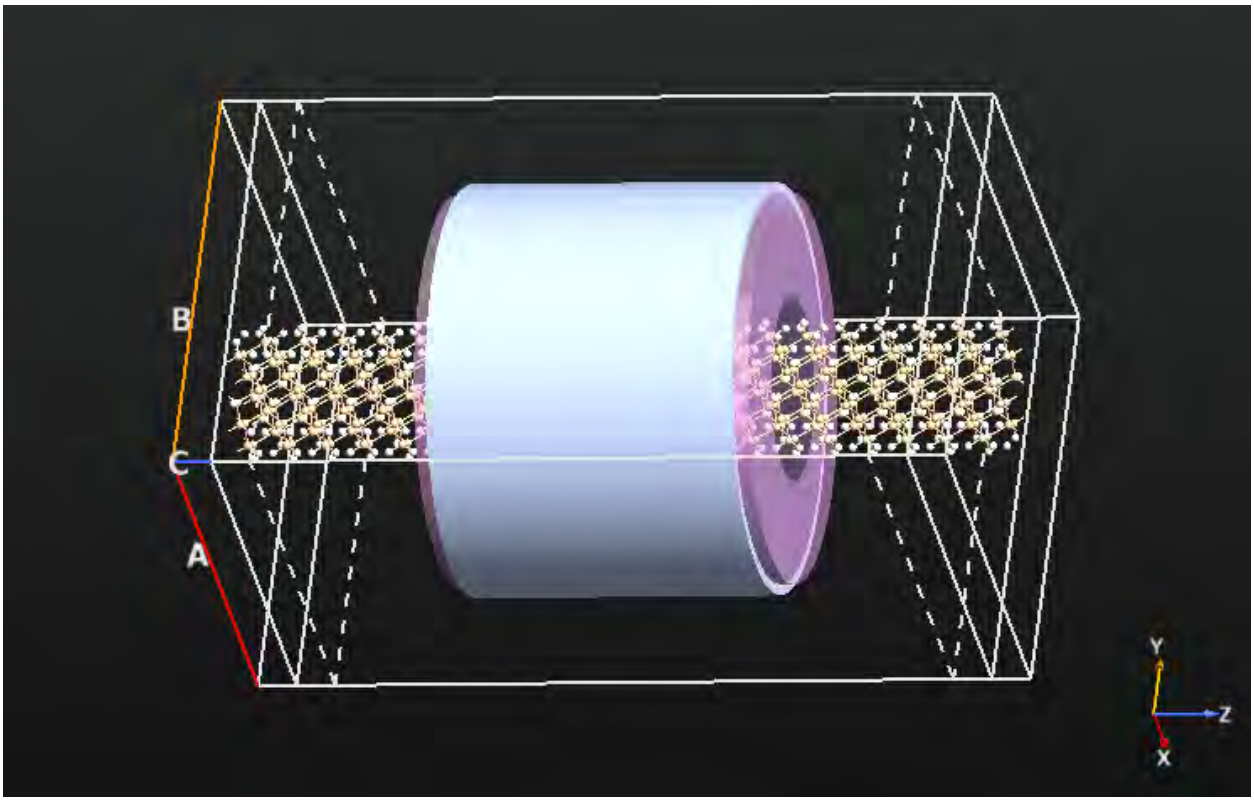

Figure 2.1: View of the Cylindrical Gate Junctionless Nanowire Transistor

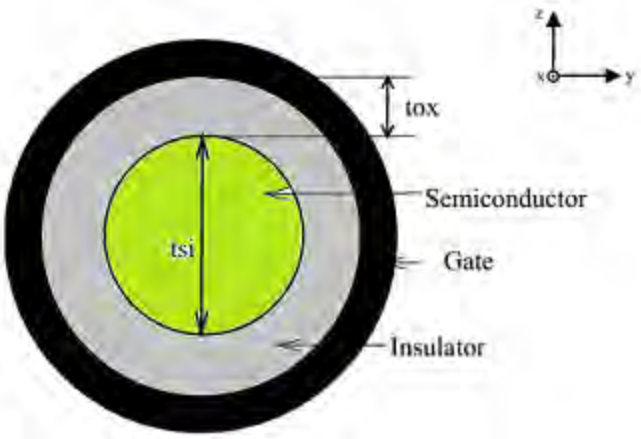

Figure 2.2: Cross Sectional view of the Cylindrical Gate Junctionless Nanowire Transistor

The Figure 2.1 is a simplified 3D model of the device under discussion. As it can be seen from the figure, the p_+ Poly gates enclose the device along XY plane, while the n-Si channel has Drain and Source terminals along Z axis, which acts as the direction of current flow. Oxide Layers separate

the Channel from the gates, barring gate current flow. Figure 2.2 shows the cross section of the device. Here, t_{ox} and t_{si} are gate oxide thickness and the silicon channel thickness respectively.

For experimental studies, usually nanoscale quantum wires are utilized for channel fabrication. In current dielectric technology, EOT is usually chosen as 1 nm. Standard feature size used for fabrication was 1 μm. However, recently, feature size up to 3 nm has been reported [29]. The standard doping density of n-channel region of the GAA-JNT device can be varied as well. Usually, as no high doped diffusion area has to be fabricated, the usual doping density of JNT is higher compared to standard FETs. The usual studies contain the doping density in the range of $2x10^{19}$ atoms/cm^3 to $1x10^{21}$ atoms/cm^3 [26].

2.3 Basic Operating Principles of the Device

The Gate-All-Around Junctionless Nanowire Transistors (GAA-JNT) has a quite different operating principle than the standard inversion or accumulation type FET devices. While the FET devices use gate voltages to attract or repulse carriers with a view to constructing an inversion layer in order to support a channel for current flow near the surface of the structure, the JNT devices, on the other hand, utilize its gate voltage to free its already present channel from the chokehold of junction Fermi level mismatch, as a channel near the core of the Quantum Wire structure [8].

The operation of the device can be best understood by observing its energy band diagram for varying gate voltage conditions. From the elementary knowledge of electronics, it is known that, when a junction is formed, the different materials present in the structure attempt to match their Electrochemical Potentials, also known as Fermi Levels along the same energy level. In case of a p-n junction, as seen in traditional electronic devices, the p-type material is doped using Group-III materials with electron deficiency. Hence the Fermi level resides closer to the valance band. On the other hand, the n-type material, doped with Group-V materials, has its Fermi level closer to the conduction band. The intrinsic level is hence along the center of the region. Now, when a junction is formed, the levels tend to match along the junction region, resulting in a slope in the

conduction band, valance band and intrinsic Fermi level of the materials along the area. The slope region, i.e. the Depletion or Space-Charge Region, is less n-type inside the n-region due to presence of static positive charge within it. The opposite is true for the p-region.

Now, in case of a Gate-Oxide-Semiconductor combination, as seen for both FETs and JNTs, the gate is usually a p^+ Polysilicon with very high doping density. Hence its Fermi level resides very close to the valance band. Although no direct junction is formed, the excess charges of gate and channel regions attract each other through the oxide layer, often with the aid of trapped oxide charges present in the layer, but no current can flow. Hence, a slope can be observed in the conduction and valance bands of the n doped channel region as space charge zone is formed.

A. Before Contact Formation: Figure 2.3 shows the energy band structure that would have been present along the previously defined X axis, in the device if no electrochemical equilibrium was supposed to be attained, i.e. under the assumption of no contact.

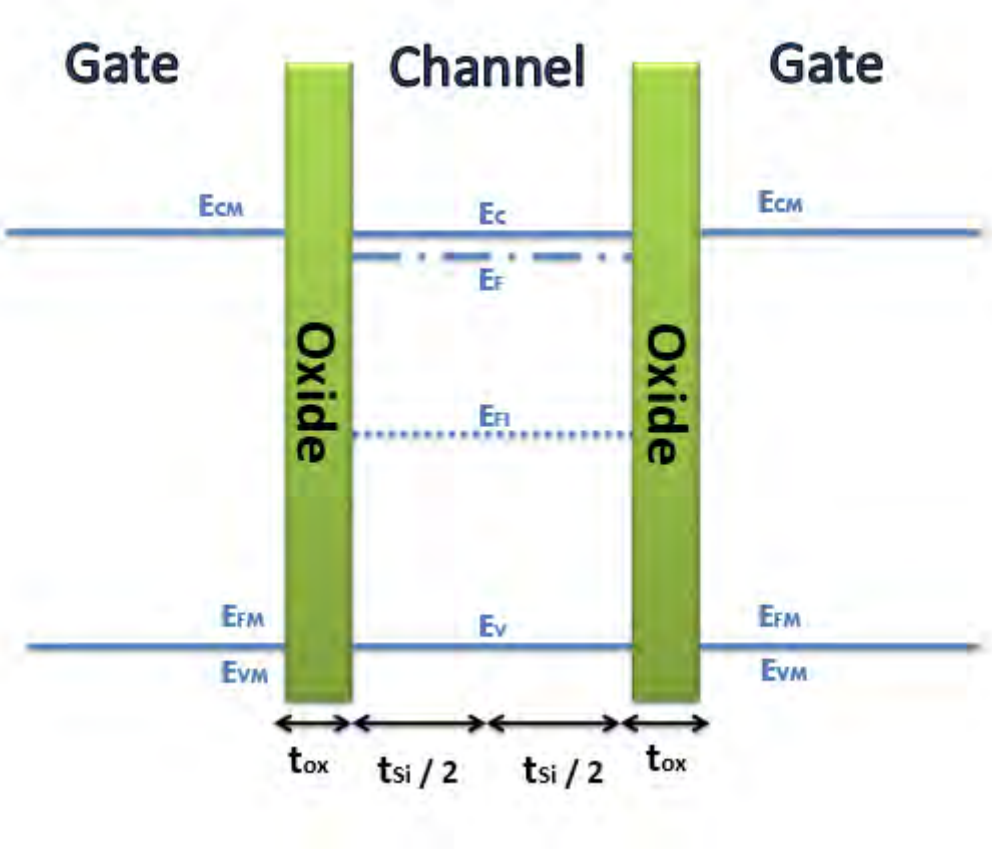

Figure 2.3: Energy Band Diagram of n-channel GAA-JNT before Junction Formation / after Flat Band Condition

The n-channel has its Fermi level near the conduction band, as an immense energy gap persists between the Fermi Levels of the channel and the gates. The Channel width is divided into two regions in the figure. Let's define the regions as the Left and Right halves of the channel [9].

B. Full Depletion Mode: Now, in reality, as the contact is formed, the Fermi levels would align, and space charge region would be produced. The trapped oxide charges in the insulator layer would also cause a slope in the conduction and valance bands of the oxide layers as well. Figure 2.4 shows the energy band conditions that would persist under the assumptions of no gate voltage.

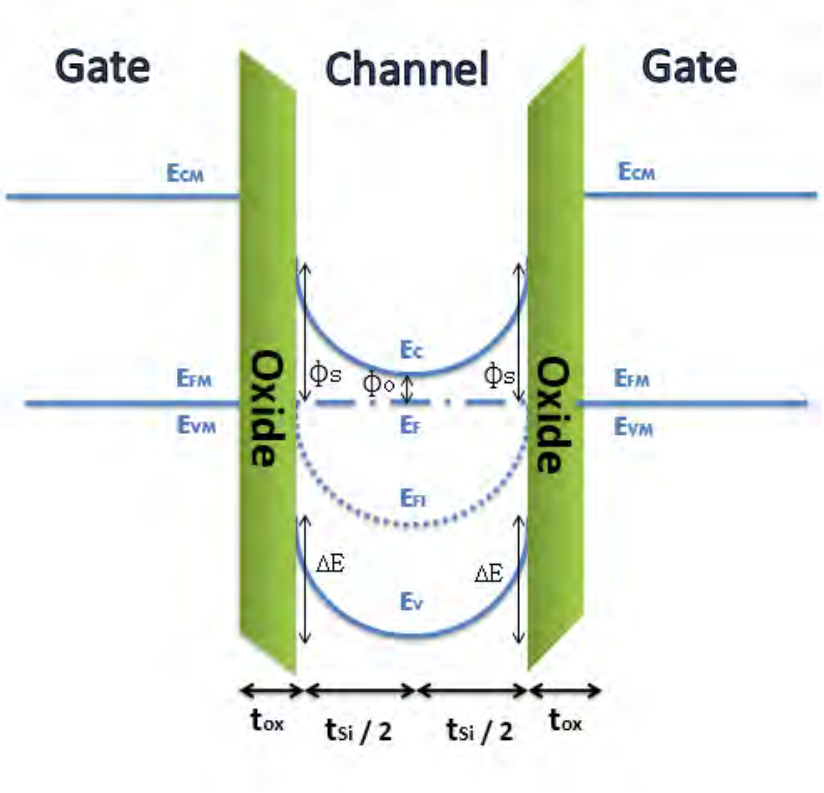

Figure 2.4: Energy Band Diagram of n-channel GAA-JNT in Full Depletion Mode

As it can be seen from the figure, the conduction and valance band bending occur by the amount of ΔE along the surface of the channel-oxide interface. So, potential varies from φ_o to φ_s along the X axis from the core of the channel to the surface regions. As a result, a space charge region persists almost throughout the channel cross-section. This is called the "Full Depletion Mode" of the device operations [55].

C. Partial Depletion Mode: When a gate voltage is applied, the band bending profile varies accordingly. The electrochemical potential decreases as positive electric potential is increased along a material axis. Hence, if a positive gate voltage is applied along the gate terminals, the gate Fermi levels V_{FM} would decrease, i.e. move toward the valance band. Moreover, since potential decreases with distance from source, the channel would experience an effective negative voltage in accordance with Kirchhoff's Voltage Law. Hence, the channel Fermi Level would tend to move upward nearer to the conduction band.

The reason of Fermi level matching in thermal equilibrium can be traced back to the propensity of material's maintaining equilibrium charge density throughout the surface. But, when a voltage is applied, the equilibrium condition no longer persists. Hence there would again be a mismatch of Fermi levels present in the device, resulting in straightening out of the conduction and valance bands.

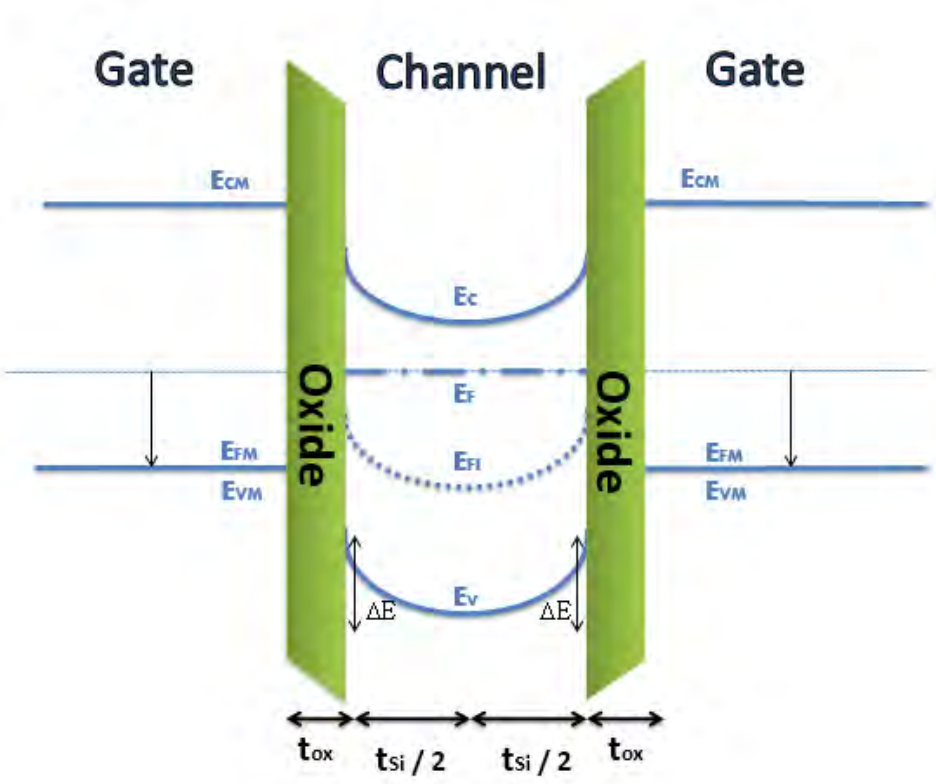

Figure 2.5: Energy Band Diagram of n-channel GAA-JNT in Partial Depletion Mode

Figure 2.5 Shows the band diagram under a positive gate voltage biasing condition. As the voltage increases, the Fermi levels drift apart, and ΔE reduces. Hence the band bending declines and so the depletion region width decreases with increasing gate voltage. This is named the “Partial Depletion Mode” of the device operations [55].

Now, let's review the device structure to delve into device operation. The channel from drain to source is the active region of the device, which is expected to allow ample current flow under proper gate biasing constraints. When the device has no input gate voltage present, the induced space charge region almost completely covers the channel region. It can be visualized as the gate choking the channel such that little to no current can flow.

Now, as gate voltage increases, the space charge region reduces in area, and moves further away from the center. Hence, current now has better potential of flowing than before. As said before, the chokehold of the gate on the channel lessens as current flow path cross section area increases. As a result, drain current flow initiates [26]. After a certain gate voltage is reached, current flow commences. A certain gate voltage can be marked as the "Threshold Voltage" of the device. Up to this point no current can flow through the channel, since sufficient mobile charge density cannot muster up for current flow. At the threshold, finally the current flow can begin.

D. Flat Band Condition: Space charge region diminishes at the “Flat-Band Voltage”, The depletion conditions die out as band structure straightens similar to the pre-connection status. Hence, At Flat-band, the band diagram closely resembles Before Contact Formation Condition in Figure 2.3, as conduction and valance band both are completely straightened.

E. Accumulation Mode: For voltages higher than the Flat Band voltage, band bending begins again, in the upward direction, since now accumulation layer of electron in CB (n-channel) is created near the channel surface, which increases surface current carrying capability. Now, current flow occurs due to the accumulation layer of charge present near the junction, similar to AM-MOSFET devices, as opposed to IM devices. Figure 2.6 shows the band diagram under a

positive (n-channel) gate voltage biasing condition for over the Flat Band Voltage limit. This is the Accumulation Mode of the device operations [46].

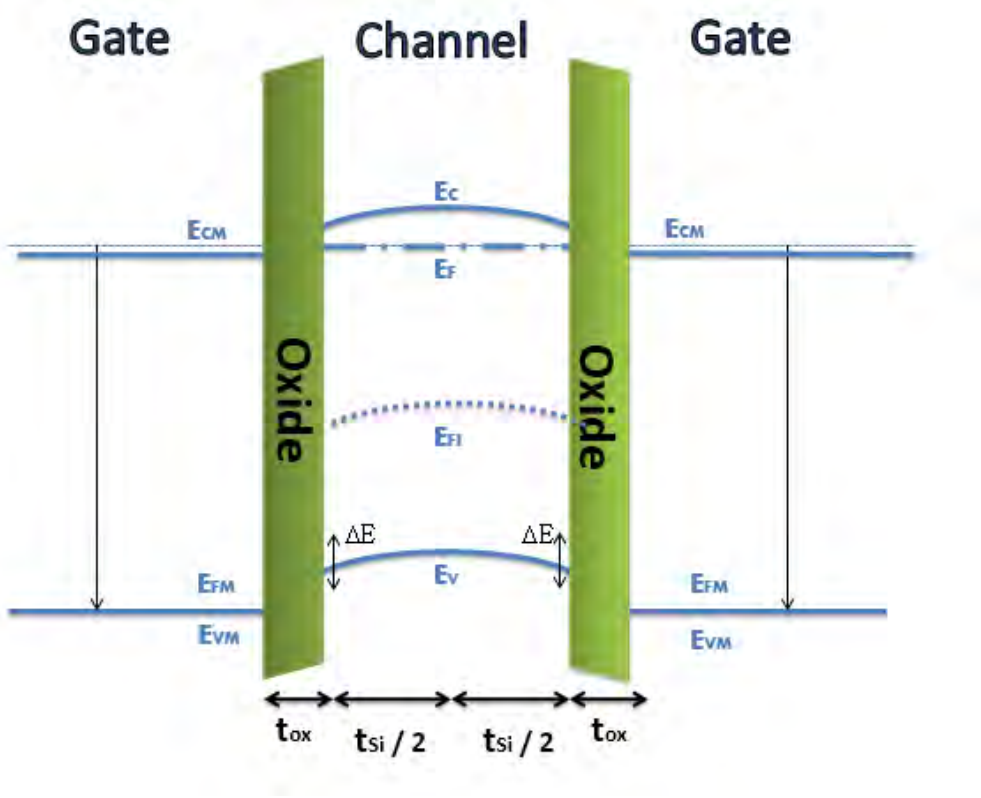

Figure 2.6: Energy Band Diagram of n-channel GAA-JNT in Accumulation Mode

So, to sum up, as gate biasing voltage increases, channel depletion region decreases. For voltages over threshold mobile charge density increases, and the device operates similar to an IM-FET. It continues up until flat-band is reached, when device enters accumulation mode, and operates as an AM-FET device.

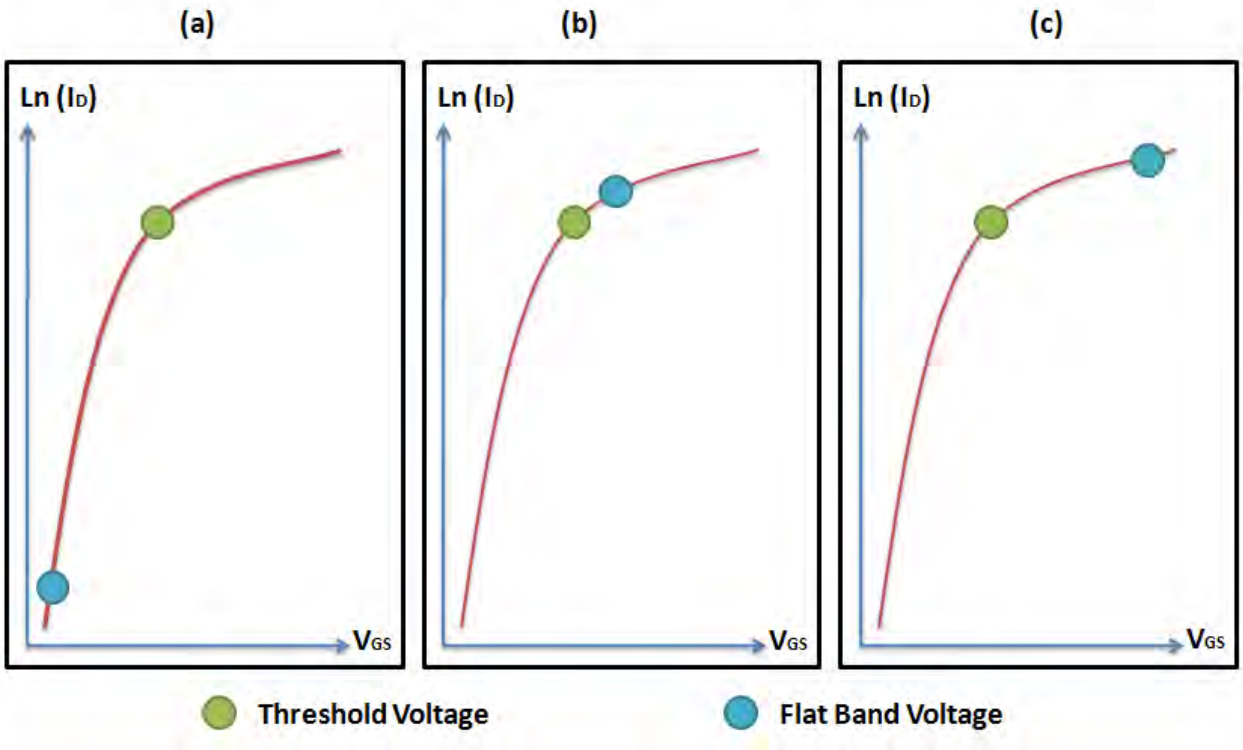

Figure 2.7: I/V Characteristic of n-channel (a) IM-FET (b) GAA-JNT (c) AM-FET showing relative positions of Threshold and Flat Band Voltage

Figure 2.7 shows standard I/V relations of GAA-JNT compared to inversion and accumulation type MOSFETs. In case of IM MOSFET devices, the band bending is miniscule, as flat-band lies close to zero voltage. On the other hand, for accumulation, flat band is very high. But, as we can clearly see, unlike MOSFET, the flat-band voltage is situated very close to threshold for JNT [26].

The Drain Voltage-Drain Current related I/V Relationship of the JNT device closely resembles MOSFET I/V relationship. For gate voltage higher than threshold, the drain current increases linearly with drain voltage, as channel current flow path can be considered as resistive. The largest contribution of such resistance comes from impurity scattering of carrier free electrons [8].

However, for sufficiently large input drain to source voltage, the channel charge density varies significantly from drain to source. At a certain high voltage the channel is pinched off, and incremental resistance is nullified. Hence, drain current remains constant for higher voltage constraints. This operation is hence same as FET characteristics.

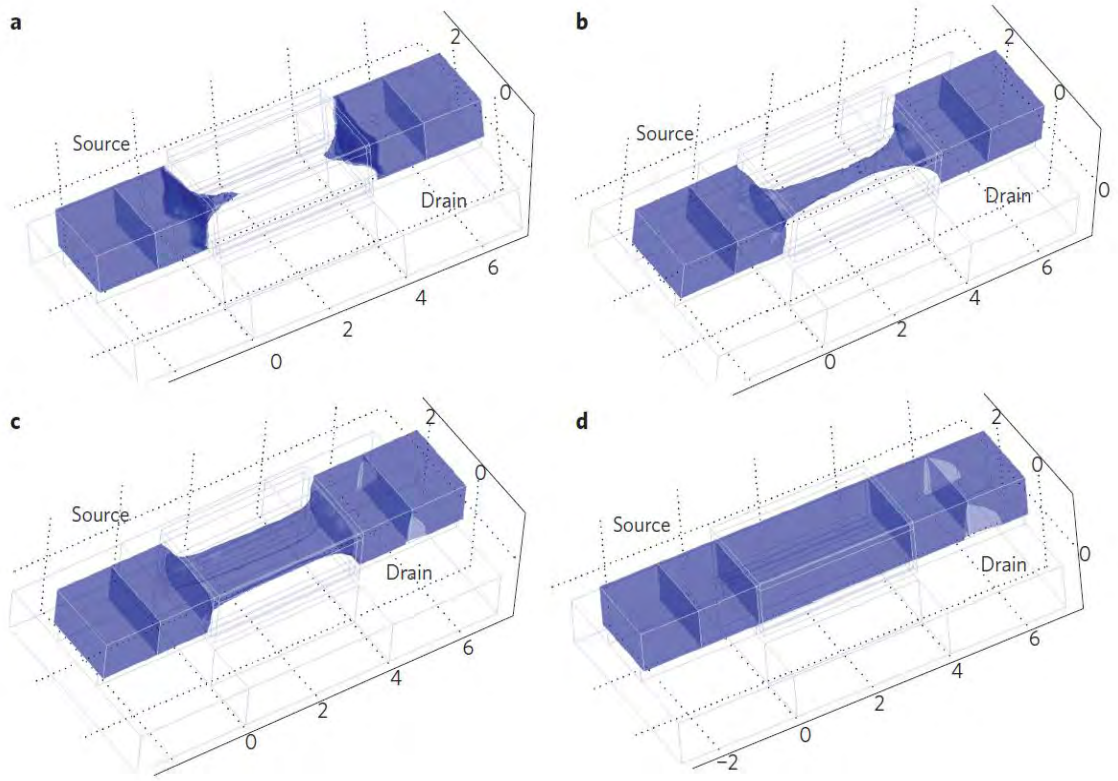

Figure 2.8: Electron concentration contour plots of n-channel JNT at (a) $V_G<V_{th}$ (b) $V_G=V_{th}$ (c) $V_G=V_{FB}$ (d) $V_G>V_{FB}$ Courtesy: Colinge et al [8]

Figure 2.8 Shows the 3D plot of channel charge density variation due to applied gate biasing voltage alteration [8].

2.4 Standard Fabrication Process of the Device

The Device fabrication procedures of Double Gate JNT are pretty elaborate and complex. The intricacies of fabrication are outside the scope of this study. However, for better conceptual comprehension, standard fabrication procedures undertaken previously are discussed here in a nutshell.

Usually, SOI (Silicon-on-insulator) technology is used to produce high-quality, single-crystal silicon films with a thickness of a few nanometers. Electron Beam Lithography and SOI wafers are used to produce Nanowires or Nanoribbons. Then ion implantation is used to yield uniform doping concentration. The gate is typically formed using amorphous Silicon deposition by dint of the Low Pressure Chemical Vapor Deposition (LPCVD) Reactor. Heavy doping and passive ambient annealing are then performed to turn the gate into Polycrystalline silicon. Then electrodes were patterned via Reactive-Ion Etch (RIE) Reactor. Next, a protective Silica isolation layer is deposited and contact holes are etched. Metallization process follows for better electrical contact formation. The gates are formed in a classic sandwich structure to craft a novel DG-JNT device.

In case of bulk JNT structure, usually, p-doped silicon is used as substrate for the n-doped Nanowire and the Polysilicon gate electrodes. So, a physical pn junction is present in the device. However, since career electrons need not overcome any pn junction while flowing, the device can still be considered to a junctionless nanowire transistor.

2.6 Advantages of the Device

Although introduced quite recently, the device called JNT has been the center of major study and analysis for its overwhelming potential of near future industrial fabrication and day-today applications in the electronics sector. If all goes well, the device even has the potential of dethroning MOSFET as the principal supply of transistors, which are the building blocks of modern electronic circuitry. Moreover, the potential of the device in device scaling can even overcome the predictions of Moore's Law. The major advantages of the device are explained in brief as follows.

2.6.1 Elimination of Doping Gradient

The junctionless nanowire transistor (JNT), unlike MOSFET or BJT, contains no distinct pn junctions in its channel region or any part of the current carrying path of the device. This is a significant departure from the FET based device characteristics, where a pnp or npn junction is a major element of device operations.

The junctions present in a FET based device results in several severe complications in fabrication process. With increasing scaling of the device size, the junctions in the device channel needs to be scaled as well. However, for proper and better device operations, it is expected that abrupt junction ending assumptions can hold up reasonably. To ensure that, very steep doping gradient must be maintained. Even in the deca-nanometer regime, abrupt ending of dopant concentration must be simulated as closely as possible, which results in extremely high doping density gradients near the junctions [8]. The doping gradient increases further with device scaling, which is increasing fast as predicted by Moore's law [1]. This problem is worsened by increased doping density in scaled Nanowire devices for ensuring enhanced properties.

For current fabrication technology, maintaining such intricate slope is proving more and more difficult. The diffusion characteristics and statistical nature of dopant and semiconductor prohibits the formation of ultra-shallow junctions with extremely high doping concentration gradients. This

constraint is holding up scaling industry all by itself. Most modern fabrication techniques use novel doping techniques and ultrafast annealing techniques, which must be constantly improved, making evolution increasingly difficult. Even, a tradeoff between device scale and quality is fast prevailing.

The JNT device, on the other hand, does not contain any explicit pn junctions. In fact, the channel present in the device is uniformly doped p or n type semiconductor with no doping gradient present whatsoever. Hence, the intricacies involved with doping gradient are of little to no consequence for the device at hand. Such freedom, makes it easier to design further scaled down transistors with reduced performance tradeoff.

2.6.2 Reduction of Short Channel Effects

Ideal FET based devices are supposed to perform as a simple switch, or at least a linear gates resistor, where the gate acts as a switching controller, turning ON or OFF the drain to source channel. However, in reality, several non-linear effects affect the device operations. Usually, enhanced device design techniques are used to reduce such complicacies to such an extent as possible, while device operations and characteristics are modeled via equations and diagrams, and appropriate approximations are made in order to simulate ideal device characteristics.

However, with further scaling of the device, several non-ideal factors are becoming more and more significant, which were considered trivial previously. Among them *Short-Channel Effects* is of major concern. The Sources of short channel effects of MOSFET can be attributed to two distinct physical phenomena: channel electron drift characteristics limitations due to scaling and the alteration of the threshold voltage due to the shortened channel length. The five major short-channel effects include [2]:

1. Drain-Induced Barrier Lowering (DIBL) and Punch Through

2. Surface Scattering

3. Velocity Saturation

4. Impact Ionization

5. Hot Electrons

Drain-induced barrier lowering (DIBL) is a short-channel effect referring originally to a reduction of threshold voltage of the transistor at higher drain voltages. In a classic planar field-effect transistor with a long channel, the bottleneck in channel formation occurs far enough from the drain contact that it is electrostatically shielded from the drain by the combination of the substrate and gate, and so classically the threshold voltage was independent of drain voltage. However, in short-channel devices this is no longer true, as the drain is close enough to gate the channel, and so a high drain voltage can open the bottleneck and turn on the transistor prematurely.

The surface scattering is often marked as universal mobility diminishing factor. The carriers, while moving along the channel while maintaining current flow, get scattered due to impurity and phonon based collisions. With increased field in short channel cases, higher scattering occurs, decreasing current flow.

In semiconductors, when a strong enough electric field is applied, the carrier velocity in the semiconductor reaches a maximum value, known as the Saturation Velocity. As the applied electric field increases from that point, the carrier velocity no longer increases because the carriers lose energy through increased levels of interaction with the lattice. Under this condition, a charge carrier cannot move any faster, having reached its saturation velocity, limiting net current flow in the FET. In short channel devices, the saturation velocity is lowered, and device current flow decreases.

Impact ionization is the process in a material by which one energetic charge carrier can lose energy by the creation of other charge carriers. An electron with enough kinetic energy can knock a bound electron out of its bound creating an electron-hole pair. For carriers to have sufficient kinetic

energy a sufficiently large electric field must be applied, in essence requiring a sufficiently large voltage but not necessarily a large current.

Hot carrier injection is a phenomenon in solid-state electronic devices where an electron gains sufficient kinetic energy to overcome a potential barrier necessary to break an interface state. Since the charge carriers can become trapped in the gate dielectric of a MOS transistor, the switching characteristics of the transistor can be permanently changed. Hot-carrier injection is one of the mechanisms that adversely affect the reliability of semiconductors of solid-state devices. Scaled short channel devices display increased injection.

Such non-ideal effects are detrimental to the proper gate control of MOSFETs. However, recent studies show that multi-gate nanowire structure can be used to improve gate control against short channel effects to the highest degree [3].

In case of multi-gate nanowire structure, a term called Effective Number of Gates (n) can be introduced which also depends on threshold voltage on silicon film thickness, which in turn decreases the effective natural length of the device.

A device can be considered free of short-channel effects if the gate length is at least 6-10 times larger than the Natural Length (λ). Hence multi-gate devices show drastically reduced short-channel effects. The GAA-JNT structure displays especially significant reductions in such effects. For example, highly improved DIBL constraints can be viewed for JNT devices [5].

2.6.3 Improved High-Temperature Operations

Traditional FET devices show aggravated device characteristics with increased temperature. In conventional MOSFET devices, the threshold voltage decreases with temperature, which in turn increases the drain current. However, carrier mobility decreases with increased temperature due to increased phonon scattering. The two variations counteract each other. At a certain temperature,

this two effects cancel out one another. The gate bias for which such effects counteract each other is denoted as the Temperature Coefficient (ZTC) point [21].

However, in case of JNT devices, the reduction of mobility is significantly less than traditional FET devices. Hence, there is no JNT, resulting in monotonic increase of current with temperature. The use of the MuGFET structure can further reduce the temperature dependence of the threshold voltage when narrow silicon wires are used due to the reduction in the surface potential variation with the temperature [47]. As a result, better I/V characteristics can be observed at high voltage and higher temperatures. Also, the usual non-ideal effects found for MOSFET at high temperature is less significant for GAA-JNT.

2.6.4 Improved Subthreshold Characteristics

The subthreshold conditions of a transistor are defined as the device characteristics and I/V relations observed for voltage under the threshold limit for the device. Under this condition, usual I/V relations of the device does not hold up. Gate leakage and other non-ideal factors prevail as significantly higher current can be observed for reduced bias voltage.

Such non-idealities constitute the OFF current of the device. The ON-OFF current ration of the device has a high significance as it marks device operation efficiency to some extent. The ratio can be improved by limiting the Subthreshold Slope of the device, i.e. rate of increase of OFF current, and hence reducing the OFF current considerably.

The subthreshold slope of a device limits the on-off current ratio of a device, which has the theoretical minima at 60 mV/decade for MOSFETs. However, that is no longer sufficient with increased device scaling along with gate voltage reduction. Positive feedback loop from increased current due to impact ionization can be used to limit the slope further down. However, multi-gated JNT structure can be used to find better characteristics [27]. The device displays increased electron temperature but decreased ionization rate for similar slope, resulting in increased slope efficiency.

At voltage under threshold, i.e. under subthreshold conditions, both JNT and MOSFET are turned off, and a high electric field is found at the drain junction of the MOSFET, which holds the bulk of the applied drain bias which peaks in the channel region. But In the junctionless device, the drain potential drop is found inside the drain electrode, outside of the region covered by the gate, since current blocking is caused by pure electrostatic pinch-off of the heavily doped nanowire structure. Hence the entire channel region is pinched off, and bulk of the drain potential drop is found in the drain, near the gate electrode. The region over which impact ionization takes place is found to be much larger in the junctionless devices than a MOSFET, reducing Drain to Source voltage considerably. Hence JNT can support an improved subthreshold slope.

Chapter 3

Methodology

This chapter describes the methods applied throughout this thesis and serves as a reference point for basic equations. The chapter is divided into three sections. The first section details the method used to describe the electronic structure of the systems investigated. In the second section the non-equilibrium Green's function (NEGF) method for quantum transport is introduced. In the third section calculation of the effect of lattice vibrations (phonons) on the electronic current will be discussed.

3.1 Electronic structure method

The majority of this thesis concerns the calculation of electronic transport of atomic scale systems under a variation of influences. In order to calculate electronic transport, one must first choose an appropriate model for the electrons. Here we introduce the semi empirical Slater-Koster tight binding method applied in this thesis.

The semi empirical method can model the electronic properties of devices using both self-consistent and non-self-consistent **tight-binding** models.

The non-self-consistent part of the tight-binding Hamiltonian is parameterized using a two-center approximation, i.e. the matrix elements only depend on the distance between two atoms and is independent of the position of the other atoms. In the Slater–Koster model, the distance-dependence of the matrix elements is given as a numerical function; this gives higher flexibility but also makes the fitting procedure more difficult.

For the self-consistent part of the calculation, the density matrix is calculated from the Hamiltonian using non-equilibrium Green's functions for device systems. The density matrix defines the real-

space electron density and consequently the Hartree potential can be obtained by solving the Poisson equation. The following describes the details of the mathematical formalism behind the implementation.

3.1.1 Non-self-consistent Hamiltonian

The Hamiltonian is expanded in a basis of local atomic orbitals (an LCAO expansion) in Eq. (3.1).

$$\phi_{nlm}(r) = R_{nl}(r)Y_{lm}(\hat{r}) \tag{3.1}$$

where Y_{lm} is a spherical harmonic and R_{nl} is a radial function. Typically, the atomic orbitals used in the LCAO expansion have a close resemblance to the atomic eigenfunctions.

3.1.2 Onsite terms

With this form of the basis set, the onsite elements are given by Eq. (3.2).

$$S_{ij}^{onsite} = \delta_{ij}$$

$$H_{ij}^{onsite} = E_i\delta_{ij} \tag{3.2}$$

where E_i is an adjustable parameter that is often close to the atomic eigenenergy.

3.1.3 Offsite Hamiltonian in the Slater–Koster model

The overlap matrix is given by pairwise integrals between the different basis functions. These integrals can be pre-calculated for all relevant distances and different orbital combinations, and stored in so-called Slater–Koster tables. The Slater–Koster table stores the distance-dependent parameters $s(d, Z1, Z2, l_1, l_2, m)$, where d is the distance, $Z1, Z2$ the element types, l_1, l_2 the angular momentum of the two orbitals, and the index $m \leq \min(l_1, l_2)$.

From the Slater–Koster tables, the overlap matrix elements are given by Eq. (3.3).

$$\boldsymbol{S_{ij}} = \sum_{m \leq \min(l_1, l_2)} \alpha_{l_i, m_i, l_j, m_j, m}(\hat{R}_{ij}) s(d_{ij}, Z_i, Z_j, l_i, l_j, m) \tag{3.3}$$

where α are the Slater–Koster expansion coefficients.

In the Slater–Koster model it is assumed that also the Hamiltonian has a pairwise form and a Slater–Koster table is generated for the Hamiltonian matrix elements. This table may be generated by calculating Hamiltonian matrix elements for a set of dimer distances or by simply fitting matrix elements to the band structure for different lattice constants.

3.1.4 Self-consistent Hamiltonian

In the self-consistent semi-empirical model, the electron density is computed using the tight-binding model as described above. The density gives rise to a Hartree potential V_H.The Hartree potential is defined as the electrostatic potential from the electron charge density and must be calculated from the Poisson equation of Eq. (3.4).

$$\nabla^2 V_H[n](\mathbf{r}) = -4\pi n(\mathbf{r}). \tag{3.4}$$

The Poisson equation is a second-order differential equation and a boundary condition is required in order to fix the solution. The system is enclosed in a bounding box, and the Hartree potential is defined on a regular grid inside the bounding box. Different boundary conditions can be imposed on the solution at the bounding box surface:

- DirichletBoundaryCondition: The Hartree potential is zero at the boundary.
- NeumannBoundaryCondition: The negative gradient of the Hartree potential, e.g. the electric field, is zero at the boundary.
- PeriodicBoundaryCondition: The potential has identical values on opposite faced boundaries.
- MultipoleBoundaryCondition: The potential at the boundary is determined by calculating the monopole, dipole and quadrupole moments of the charge distribution inside the box, and using these

moments to extrapolate the value of the electrostatic potential at the boundary of the box.

It is possible to include an electrostatic interaction with a continuum of metallic or dielectric material inside the bounding box. The continuum metals are handled by constraining the Hartree potential within the metallic region to a fixed value. Dielectric materials are handled by introducing a spatially dependent dielectric constant, $\boldsymbol{\epsilon}(\mathbf{r})$, where $\boldsymbol{\epsilon}(\mathbf{r}) = \boldsymbol{\epsilon_K}$, inside the dielectric material with dielectric constant $\boldsymbol{\epsilon_K}$, and $\boldsymbol{\epsilon}(\mathbf{r}) = \boldsymbol{\epsilon_0}$ outside the dielectric material.

The Hartree potential is included through an additional term in the Hamiltonian in Eq. (3.5).

$$H_{ij}^{SCF} = \frac{1}{2}\left(V_H(R_i) + V_H\left(R_j\right)\right) S_{ij}. \tag{3.5}$$

3.1.5 Electron density

The electron density is given by the occupied eigenfunctions in Eq. (3.6).

$$n(\mathbf{r}) = \sum_\alpha f_\alpha \, |\psi_\alpha(\mathbf{r})|^2, \tag{3.6}$$

where f_α is the occupation of the level denoted by α. For finite temperature calculation the occupations are determined by the Fermi-Dirac distribution $f_\alpha = \frac{1}{1+e^{(\epsilon_\alpha - \epsilon_F)/kT}}$ with ϵ_α being the energy of the eigenstate ψ_α, ϵ_F the Fermi level and T the electron temperature.

The eigenstates in the Slater orbital basis can be written by Eq. (3.7).

$$\psi_\alpha = \sum_i c_{\alpha i} \phi_i \, , \tag{3.7}$$

Where $c_{\alpha i}$ are the Slater–Koster expansion coefficients.

The total number of electrons, $N = \int_V n(\mathbf{r})d\mathbf{r}$, is given by Eq. (3.8).

$$N = \sum_{ij} D_{ij} S_{ij}, \tag{3.8}$$

where $D_{ij} = \sum_{\alpha} f_{\alpha} c_{\alpha i}^{*} c_{\alpha j}$ is the density matrix.

3.1.6 An approximate atom-based electron density

In practice, a simple approximation is used for the electron density. To this end, we introduce the Mulliken population in Eq. (3.9).

$$m_l = \sum_{i \in l} \sum_j D_{ij} S_{ij}\,, \tag{3.9}$$

for l shell of atom number μ, and write the total number of electrons as a sum of atomic contributions, $N = \sum_{\mu} \sum_{l \in \mu} m_l$. The radial dependence of each atomic-like density is represented by a Gaussian function, and the total induced charge in the system is approximated by Eq. (3.10).

$$\delta n(\mathbf{r}) = \sum_{\mu} \sum_{l \in \mu} \delta m_l \left(\frac{\alpha_l}{\pi}\right)^{\frac{3}{2}} e^{-\alpha_l |\mathbf{r}-\mathbf{R}_{\mu}|^2}\,, \tag{3.10}$$

where $\delta m_l = m_l - Z_{\mu}$ is the total charge for shell l of atom μ, i.e. the sum of the valence electron charge m_l and the ionic charge $-Z_{\mu}$.

To see the significance of the width α_l of the Gaussian orbital, consider the electrostatic potential from a single Gaussian density at position $\mathbf{R}_{\mu}$ in Eq. (3.11).

$$V_H(\mathbf{r}) = \left(m_l - Z_{\mu}\right) \frac{\mathrm{erf}\left(\sqrt{\alpha_l}|\mathbf{r}-\mathbf{R}_{\mu}|\right)}{|\mathbf{r}-\mathbf{R}_{\mu}|}. \tag{3.11}$$

The onsite value of the Hartree potential is $\boldsymbol{V_H}(\mathbf{R}_{\mu}) = \left(m_l - Z_{\mu}\right)U_l$, where $U_l = 2\sqrt{\frac{\alpha_l}{\pi}}$ is the onsite Hartree shift. U_l is used to determine the width α_l of the Gaussian using the above relation.

3.1.7 Onsite Hartree shift parameters

The shell-dependent onsite Hartree shift U_l can be obtained from an atomic calculation. U_l is related to the linear shift of the eigenenergy ε_l of shell l as function of the shell occupation q_l as shown in Eq. (3.12).

$$U_l = \frac{d\varepsilon_l}{dq_l}. \tag{3.12}$$

Thus, U_l can be obtained by performing atomic calculations with different values of q_l. It is recommended to use the same onsite Hartree shift parameter for the s- and p-shells of each atom.

3.1.8 Spin polarization

The inclusion of spin in the tight-binding Hamiltonian follows the scheme in [56]. The following spin dependent term from Eq. (3.13) is added to the Hamiltonian.

$$H_{ij}^{\sigma} = \pm\frac{1}{2}S_{ij}\left(dE_{l_i} + dE_{l_j}\right), \tag{3.13}$$

where the sign in the equation depends on the spin.

The spin splitting $\boldsymbol{dE_l}$ of shell $\boldsymbol{l}$ is calculated from the spin-dependent Mulliken populations $\boldsymbol{\mu_l}$ of each shell at the local site as shown in Eq. (3.14).

$$dE_l = \sum_{l'\in\mu_l} W_{ll'}(m_{l'\uparrow} - m_{l'\downarrow}). \tag{3.14}$$

3.1.9 Onsite spin-split parameters

The shell-dependent spin splitting strength $W_{ll'}$ can be obtained from a spin-polarized atomic calculation [56] as shown in Eq. (3.15).

$$W_{ll'} = \frac{1}{2}\left(\frac{d\varepsilon_{l'\uparrow}}{dm_{l'\uparrow}} - \frac{d\varepsilon_{l'\uparrow}}{dm_{l'\downarrow}}\right). \tag{3.15}$$

Since $W_{ll'}$ enters symmetrically in the Hamiltonian, it is convenient to symmetrize it by the Eq. (3.16).

$$\bar{W}_{ll'} = \frac{1}{2}(W_{ll'} + W_{l'l}) \,. \tag{3.16}$$

3.2 NEGF Formalism

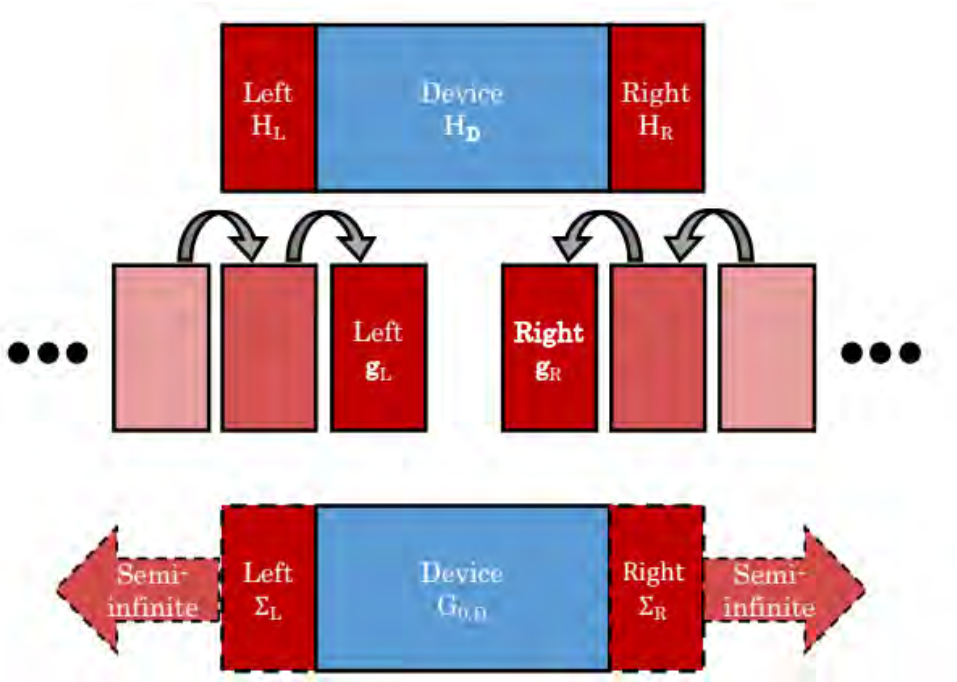

Figure 3.1: Sketch of the NEGF procedure. Top: First the system is partitioned into a central device (D) region and left (L) and right (R) electrode regions. Middle: The retarded surface Green's functions are calculated recursively from the left and right unit cells. Bottom: The self-energies of the left and right electrodes are connected to the device region through the expression Eq. (3.22) replacing the left and right region with semi-infinite leads.

The real-space representation of the Hamiltonian allows for the straightforward separation of the system into an interacting device region (D) and noninteracting left (L) and right (R) electrode regions (leads) as illustrated in Fig. 3.1.

The left and right regions are equilibrium systems with periodic boundary conditions, and the properties of these systems are obtained using a conventional electronic structure calculation. The challenge in calculating the properties of a device system lies in the calculation of the non-equilibrium electron distribution in the central region.

The electron density is given in terms of the electron density matrix. The density matrix can be divided into left and right contributions as shown in Eq. (3.17).

$$D = D^L + D^R \tag{3.17}$$

The left density matrix contribution is calculated using the NEGF method by Eq. (3.18) as [57].

$$D^L = \int \rho^L(\varepsilon)\ f\left(\frac{\varepsilon - \mu_L}{k_B T_L}\right) d\varepsilon, \tag{3.18}$$

Where

$$\rho^L(\varepsilon) \equiv \frac{1}{2\pi} G(\varepsilon)\Gamma^L(\varepsilon)G^\dagger(\varepsilon) \tag{3.19}$$

In Eq. (3.19) ρ^L is the spectral density matrix. Note that while there is a non-equilibrium electron distribution in the central region, the electron distribution in the electrode is described by a Fermi function f with an electron temperature T_L.

In this Eq. (3.19), G is the retarded Green's function.

$$\Gamma^L = \frac{1}{i}(\sum^L - (\sum^R)^\dagger) \tag{3.20}$$

In Eq. (3.20), Γ^L is the broadening function of the left electrode, given in terms of the left electrode self energy, $\sum^L$. A similar equation exists for the right density matrix contribution. The following section describes the calculation of G and Σ in more detail.

3.2.1 Retarded Green's function

The key quantity to calculate is the retarded Green's function matrix from Eq. (3.21).

$$G(\varepsilon) = \frac{1}{(\varepsilon + i\delta_+)S - H}, \tag{3.21}$$

Where δ_+ is an infinitesimal positive number. S and H are the overlap and Hamiltonian matrices, respectively, of the entire system.

The Green's function is only required for the central region and can be calculated from the Hamiltonian of the central region by adding the electrode self energies in Eq. (3.22).

$$\boldsymbol{G}(\varepsilon) = \left[(\varepsilon + i\delta_+)\boldsymbol{S} - \boldsymbol{H} - \boldsymbol{\Sigma}^{\boldsymbol{L}}(\varepsilon) - \boldsymbol{\Sigma}^{\boldsymbol{R}}(\varepsilon)\right]^{-1}. \tag{3.22}$$

Therefore, the calculation of the Green's function of the central region at a specific energy requires the inversion of the Hamiltonian matrix of the central region [58].

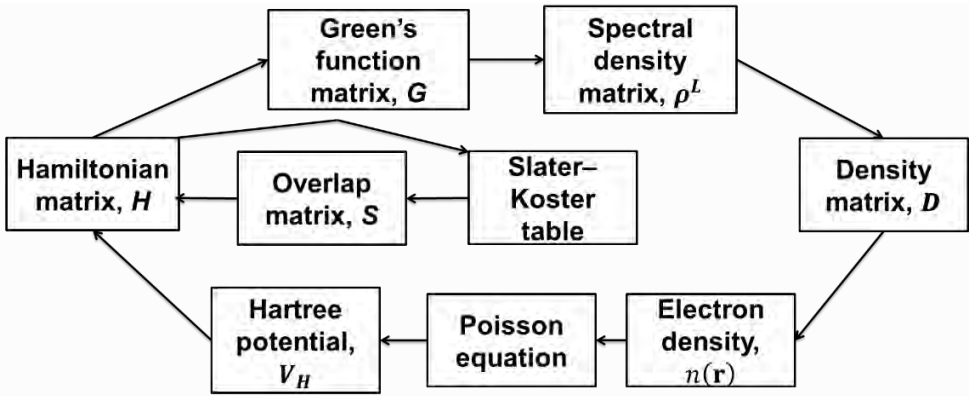

Figure 3.2: Flow diagram of electronic transport calculation using tight binding method

The overall procedure of electronic transport calculation using tight binding method is summarized in Fig. 3.2. The density matrix is calculated from the Hamiltonian matrix using non-

equilibrium Green's functions for device systems. The density matrix defines the real-space electron density and consequently the Hartree potential can be obtained by solving the Poisson equation. The Slater–Koster table is generated for the Hamiltonian matrix elements. From the Slater–Koster table, the Overlap matrix is determined. Then the self-consistent Hamiltonian matrix is determined from the Overlap matrix and Hartree potential.

3.2.2 Self energy

The self energy describe the effect of the electrode states on the electronic structure of the central region. The self energy can be calculated from the electrode Hamiltonian. RecursionSelfEnergy method which is an iterative scheme is used here for calculating the self energy [59].

3.2.3 Complex contour integration

The energy integral needed to obtain the density matrix within the NEGF framework is evaluated through a complex contour integration. It is divided into two parts; an integral over equilibrium states and an integral over non-equilibrium states.

The integral over the equilibrium states can be done using SemiCircleContour method which defines a semi-circular complex contour that gives high computational efficiency [57].

Lastly, one of two different contour methods must be chosen (usually just left at the default value):

- SingleContour uses a single contour for the calculation. This is appropriate for small biases, and is the fastest method.
- DoubleContour uses a double contour for the calculation. This gives best stability and must be used for high biases. The method can also handle if there are bound states inside the bias window.

3.2.4 Spill-in terms

In terms of the density matrix, D, the electron density of the central region is given by Eq. (3.23).

$$n(\boldsymbol{r}) = \sum_{ij} D_{ij}\, \phi_j(\boldsymbol{r}). \tag{3.23}$$

The Green's function of the central region gives the density matrix of the central region, D_{CC}, however, to calculate the density correctly close to the central cell boundaries the terms involving, $D_{LL}, D_{LC}, D_{CR}, D_{RR}$ are also needed. These terms are denoted spill-in terms which are required for both calculating the electron density $n(\boldsymbol{r})$ and the Hamiltonian integral. This gives additional stability and well-behaved convergence in the device algorithm [60].

3.2.5 Effective potential

Once the non-equilibrium density is obtained the next step in the self-consistent calculation is the calculation of the effective potential as the sum of the exchange-correlation and electrostatic Hartree potentials. The calculation of the exchange-correlation potential is straightforward since it is a local or semi-local function of the density. However, the calculation of the electrostatic Hartree potential requires some additional consideration for a device system. The following describes the calculation of the Hartree potential in more detail.

The starting point is the calculation of the self-consistent Hartree potential in the left and right electrodes. The Hartree potential of a bulk system is defined up to an arbitrary constant. However, in a device setup the Hartree potentials of the two electrodes are aligned through their chemical potentials (i.e. their Fermi levels), since these are related by the applied bias as in Eq. (3.24).

$$\mu_R - \mu_L = eV_b. \tag{3.24}$$

The Hartree potential of the central region is obtained by solving the Poisson equation, using the bulk-like Hartree potentials of the electrodes as boundary conditions at the interfaces between the electrodes and the central region. For solving the Poisson equation of a device system ParallelConjugateGradientSolver is used. It is an iterative solver based on the conjugate gradient method. It allows for different types of boundary conditions, implicit solvents, and the use of metallic and dielectric spatial regions to simulate gates.

3.2.6 Total energy and forces

A device system is an open system where charge can flow in and out of the central region from the left and right reservoirs. Since the particle number is not conserved it is necessary to use a grand canonical potential to describe the energetics of the system [61]:

$$\Omega[\mathrm{n}] = \varepsilon[n] - eN_L\,\mu_L - eN_R\,\mu_R, \tag{3.25}$$

Where $N_{L/R}$ is the number of electrons contributed to the central region from the left/right electrode.

Due to the screening approximation, the central region will be charge neutral, and therefore $N_L + N_R = N$, where N is the ionic charge in the central region. Thus, at no applied bias, we have $\mu_L = \mu_R$ and the particle terms in Ω will be constant when atoms are moved in the central region. However, at finite bias $\mu_L \neq \mu_R$, and the particle Ω terms in will be important.

The forces are given by Eq. (3.26).

$$\boldsymbol{F}_i = -\frac{\partial\Omega[\mathrm{n}]}{\partial \boldsymbol{R}_i}. \tag{3.26}$$

It can be shown that the calculation of this force is identical to the calculation of the equilibrium force. In the non-equilibrium case it is however required that the density and energy density matrix is calculated with the NEGF framework [57], [61], [62].

3.2.7 Transmission coefficient

When the self-consistent non-equilibrium density matrix has been obtained, it is possible to calculate various transport properties of the system. One of the most notable is the TransmissionSpectrum from which one can obtain the current and differential conductance.

The transmission coefficient may also be obtained from the retarded Green's function using Eq. (3.27).

$$T(\varepsilon) = G(\varepsilon)\Gamma^L(\varepsilon)G^\dagger(\varepsilon)\Gamma^R(\varepsilon). \tag{3.27}$$

3.2.8 Electrical current

To calculate the current one must first calculate a TransmissionSpectrum, and then from this extract the electrical current. This approach has the advantage that once the TransmissionSpectrum is calculated, it is fast to calculate the current for different electrode temperatures [60].

3.2.9 Interacting current

One property that I will extract several times throughout this thesis is the electronic current since it is the observable most relevant for electronic applications. The current flowing into lead α including interactions in the device region is given by the Meir-Wingreen equation [63, 64]:

$$I_\alpha = \frac{G_o}{e}\int_{-\infty}^{\infty} d\varepsilon\, T_\alpha\,,$$

$$T_\alpha = \mathrm{Tr}\{\boldsymbol{\Sigma}_\alpha^{<}(\varepsilon)G_D^{>}(\varepsilon) - \boldsymbol{\Sigma}_\alpha^{>}(\varepsilon)G_D^{<}(\varepsilon)\}, \tag{3.28}$$

where $G_o = \frac{2e^2}{h}$is the conductance quantum, $G_D^{\gtrless}(\varepsilon)$ is the lesser/greater device Green's function including interactions in the device region and $\boldsymbol{\Sigma}_\alpha^{\gtrless}(\varepsilon)$ is the lesser/greater self-energy of lead α giving the rate of electrons/holes coming from the lead into the device region. The lesser and greater self-energies are given by Eq. (3.29).

$$\boldsymbol{\Sigma}_\alpha^{<} = i\Gamma_\alpha f_\alpha\,, \qquad \boldsymbol{\Sigma}_\alpha^{>} = i\Gamma_\alpha(1-f_\alpha), \tag{3.29}$$

Where $f_\alpha = 1/(e^{(\varepsilon-\mu_\alpha)/k_BT}+1)$ is the Fermi Dirac distribution function with chemical potential μ_α and $\boldsymbol{\Gamma}_\alpha$ is the broadening of device states due to the coupling with the semi-infinite states of lead α. We can express the broadening in terms of the lead self-energies as in Eq. (3.30).

$$\boldsymbol{\Gamma}_\alpha = i(\boldsymbol{\Sigma}_\alpha - \boldsymbol{\Sigma}_\alpha^\dagger). \tag{3.30}$$

The lesser and greater Green's function are given by the steady state Keldysh equations [64–67]:

$$\boldsymbol{G}_D^{\gtrless}(\varepsilon) = \boldsymbol{G}_D \left[\sum_\alpha \boldsymbol{\Sigma}_\alpha^{\gtrless} + \boldsymbol{\Sigma}_{int}^{\gtrless}\right] \boldsymbol{G}_D^\dagger, \tag{3.31}$$

and the full retarded Green's function $\boldsymbol{G}_D$ is given by Dysons equation [64–67]:

$$\boldsymbol{G}_D = \boldsymbol{G}_{0,D} + \boldsymbol{G}_{0,D}\boldsymbol{\Sigma}_{int}\boldsymbol{G}_D, \tag{3.32}$$

where we have introduced the lesser/greater $\boldsymbol{\Sigma}_{int}^{\gtrless}$ and retarded $\boldsymbol{\Sigma}_{int}$ interaction self-energies, accounting explicitly for additional interactions that occur inside the device region. In this thesis we will calculate the current due to electron-phonon coupling which will be described in the following section.

3.2.10 Noninteracting current

We can consider a non-interacting device region by setting $\boldsymbol{\Sigma}_{int} = \boldsymbol{\Sigma}_{int}^{\gtrless} = 0$, and after some rewriting, we recover from Eq. (3.28) the well known Landauer-Büttiker formula:

$$I_0 = \frac{G_0}{e}\int_{-\infty}^{\infty} d\varepsilon\, T_0(\varepsilon)[f_L(\varepsilon) - f_R(\varepsilon)]$$

$$T_0 = \mathrm{Tr}\{\boldsymbol{\Gamma}_L \boldsymbol{G}_{0,D} \boldsymbol{\Gamma}_R \boldsymbol{G}_{0,D}^\dagger\} \tag{3.33}$$

giving the non-interacting current.

3.3 Electron-phonon coupling

The interaction between the current carrying charges and the vibrations of the lattice at finite temperature is known as electron-phonon coupling (EPC). In this section we will introduce a robust approach used to include electron-phonon coupling.

3.3.1 Calculating phonons

To obtain the eigenvectors $\boldsymbol{e}_\lambda$ and frequencies Ω_λ of the phonon modes λ we use the frozen phonon method [68–70]. The dynamical matrix is given by Eq. (3.34).

$$\boldsymbol{D}_{i\mu,j\nu} = \frac{1}{\sqrt{M_i M_j}} \boldsymbol{K}_{i\mu,j\nu}, \tag{3.34}$$

Where M_i are the atomic masses of the ions in the system and $\boldsymbol{K}_{i\mu,j\nu}$ is the Hessian matrix obtained by displacing each atom i away from its relaxed position along direction μ and evaluating the force F on the atom j in direction ν. Using finite difference $\boldsymbol{K}$ is obtained from Eq. (3.35).

$$\boldsymbol{K}_{i\mu,j\nu} = \frac{\partial^2 E}{\partial r_{i,\mu} \partial r_{j,\nu}} = \frac{F_{j,\nu}(\Delta_{i,\mu}) - F_{j,\nu}(-\Delta_{i,\mu})}{2\Delta_{i,\mu}} \tag{3.35}$$

where Δ is a small displacement. The phonon frequencies Ω_λ and eigenvectors $\boldsymbol{e}_\lambda$ are then obtained from the dynamical matrix by solving the Eq. (3.36).

$$\boldsymbol{D}\boldsymbol{e}_\lambda = \Omega_\lambda^2 \boldsymbol{e}_\lambda \tag{3.36}$$

The electron-phonon coupling matrix for a given phonon mode, λ , is obtained from Eq. (3.37).

$$\boldsymbol{M}_\lambda = \sum_{I\nu} \left\langle \phi_i \middle| \frac{\partial \mathbf{H}}{\partial r_{I\nu}} \middle| \phi_j \right\rangle \boldsymbol{e}_{\lambda,I\nu} \sqrt{\frac{\hbar}{2M_I \Omega_\lambda}} \tag{3.37}$$

where the sum runs over atom indices I and Cartesian directions $\nu = (x, y, z)$.

The force *F* can be evaluated directly from DFT or, when applicable, using classical inter-atomic potentials. The classical force field calculation is much more computationally efficient than DFT calculation. Both approaches give approximately same values.

In practice, when calculating the Hessian matrix, the dynamical part of the system is repeated a few times along periodic directions before performing the displacements of atoms.

3.3.2 Lowest Order Expansion

One way to derive an expression for the current due to EPC in the device region, is to start from the Meir-Wingreen equation Eq. (3.28) introducing a phonon self-energy $\boldsymbol{\Sigma}_{ph}$ as the interaction self-energy. Assuming free uncoupled phonons one can derive the Eq. (3.38) for the phonon self-energies.

$$\boldsymbol{\Sigma}_{ph}^{\gtrless}(\varepsilon) = \sum_{\lambda} i \int_{-\infty}^{\infty} \frac{d\Omega_{\lambda}}{2\pi} \boldsymbol{M}_{\lambda} D_0^{\gtrless}(\Omega_{\lambda}) \lambda \boldsymbol{G}_D^{\gtrless}(\varepsilon - \Omega_{\lambda}) \boldsymbol{M}_{\lambda}$$

$$\boldsymbol{\Sigma}_{ph} = \frac{1}{2}\left(\boldsymbol{\Sigma}_{ph}^{>} - \boldsymbol{\Sigma}_{ph}^{<}\right) - \frac{i}{2}\mathcal{H}\left(\boldsymbol{\Sigma}_{ph}^{>} - \boldsymbol{\Sigma}_{ph}^{<}\right) \tag{3.38}$$

where $\boldsymbol{D}_0^{\gtrless}$ are the free greater/lesser bosonic phonon Green's functions, $\boldsymbol{M}_{\lambda}$ is the electron-phonon coupling matrix and $\boldsymbol{\mathcal{H}}$ is the Hilbert transform. This is known as the self-consistent Born approximation (**SCBA**). These equations along Keldysh and Dyson equations can be solved iteratively to evaluate the current including EPC. However, the computational time needed for this evaluation means it is only a viable approach for systems containing a handful of atoms. However, for systems where the *e*-ph coupling is weak and the density of states DOS varies slowly with energy, the SCBA current expression can be expanded to lowest (second) order in $\boldsymbol{M}_{\lambda}$ arriving at the Lowest Order Expansion (LOE) current expression.

The main computational burden of the SCBA originates from the numerical integration over energy needed in the evaluation of the current expression (31). The LOE approximation assumes that the **retarded and advanced** single-particle Green's functions ($\boldsymbol{G}_{0,D}$,$\boldsymbol{G}_{0,D}^{\dagger}$) and lead self-

energies ($\boldsymbol{\Sigma}_{\alpha}$, $\boldsymbol{\Sigma}_{\alpha}^{\dagger}$) are energy independent. We can then expand the current expression to the lowest (second) order in *e*-ph couplings $\boldsymbol{M}_{\lambda}$ and perform the energy integrations analytically. These integrals consist of products of Fermi-Dirac functions and their Hilbert transforms. The LOE thus retains the Pauli exclusion principle for fermionic particles, which is necessary to model the blocking of phonon emission processes at low bias.

The LOE approximation allows us to write the current through the device as Eq. (3.39).

$$I(V) = I_e + I_i \tag{3.39}$$

Where I_e= elastic current and I_i =inelastic current

$$I_e = \frac{G_0}{e}\int_{-\infty}^{\infty} d\varepsilon\{f_L(\varepsilon) - f_R(\varepsilon)\}\{Tr\big[G_{0,D}\boldsymbol{\Gamma}_L G_{0,D}^{\dagger}\boldsymbol{\Gamma}_R\big](\varepsilon) + 2ReTr\big[G_{0,D}\boldsymbol{\Sigma}_{ph}G_{0,D}\boldsymbol{\Gamma}_L G_{0,D}^{\dagger}\boldsymbol{\Gamma}_R\big](\varepsilon)\}$$

$$I_i = \sum_{\lambda}\big[I_{\lambda}^{sym}(V,T)T_{\lambda}^{sym}(\varepsilon_F) + I_{\lambda}^{asym}(V,T)T_{\lambda}^{asym}(\varepsilon_F)\big] \tag{3.40}$$

Where ε_F is the fermi energy and the rest of the new symbols are defined as follows: In either approximation, the universal current functions appear in the same form in Eq. (3.41).

$$I_{\lambda}^{sym}(V,T) = \frac{G_0}{2e}\sum_{\sigma=\pm}\sigma(\hbar\omega_{\lambda} + \sigma eV)\ \left(\coth\frac{\hbar\omega_{\lambda}}{2k_BT} - \coth\frac{\hbar\omega_{\lambda} + \sigma eV}{2k_BT}\right)$$

$$I_{\lambda}^{asym}(V,T) = \tfrac{G_0}{2e}\textstyle\int_{-\infty}^{\infty} d\varepsilon[n_F(\varepsilon - eV) - n_F(\varepsilon)]\,.\,\mathcal{H}_{\varepsilon'}[n_F(\varepsilon' - eV) - n_F(\varepsilon' + eV)](\varepsilon) \tag{3.41}$$

Where $G_o = \frac{2e^2}{h}$is the conductance quantum, $n_F(.)$ is the Fermi-Dirac distribution function, and $\mathcal{H}_{\varepsilon'}[.](\varepsilon)$ means the Hilbert transform. In extended LOE (XLOE), the transmission functions are given by Eq. (3.42).

$$T_{\lambda}^{sym}(\varepsilon) = \mathrm{Tr}\big[M_{\lambda}\tilde{A}_L(\mu_L)M_{\lambda}A_R(\mu_R)\big] + \mathrm{Im}\,B_{\lambda}(\varepsilon),$$

$$T_{\lambda}^{asym}(\varepsilon) = 2\mathrm{Re}\,B_{\lambda}(\varepsilon), \tag{3.42}$$

With

$$\mu_L = \varepsilon,$$

$$\mu_R = \varepsilon \pm \hbar\omega_\lambda,$$

$$\tilde{A}_L(\varepsilon) = G_{0,D}(\varepsilon)\mathbf{\Gamma}_L(\varepsilon)G_{0,D}^{\dagger}(\varepsilon), \tag{3.43}$$

and

$$B_\lambda(\varepsilon) = Tr\left[M_\lambda A_R(\mu_L)\Gamma_L(\mu_L)G_{0,D}(\mu_L)M_\lambda A_R(\mu_R) - M_\lambda G_{0,D}^{\dagger}(\mu_R)\Gamma_L(\mu_R)A_R(\mu_R)M_\lambda A_L(\mu_L)\right]. \tag{3.44}$$

This XLOE expression of the transmission functions reduces to the LOE expression by setting $\mu_L = \mu_R = \varepsilon$. In the above equations, all the Greens function are non-interacting, i.e. they do not include the electron-phonon self-energies. Importantly, in the expression of the current, the Green's function, the self-energies, and the spectral functions in the transmission functions are evaluated at two different energies $\varepsilon_F \pm \hbar\omega_\lambda$ in XLOE, whereas they are all evaluated at the same energy ε_F in LOE. [71]. This means that many more calculations are needed for the XLOE calculations rather than LOE which therefore takes more time.

The LOE is originally developed for studying molecular junctions where a molecule is placed between metallic electrodes. If there are no molecular states close to the Fermi energy, the LOE will be sufficient to use. However, if there are states close to the Fermi energy, the XLOE will be a more correct description as it allows some variation of the density of states. XLOE should be used if transport occurs close to semi-conductor band edges.

Here we simply state the current equations, while the rigorous derivation of these equations can be found elsewhere [71-73].

The electron-phonon coupling matrix $\boldsymbol{M}_\lambda$ is to lowest order given by the Hamiltonian derivative with respect to coordinate position $\mathbf{\nabla_r H}$ [71-73]. In the harmonic approximation $\mathbf{\nabla_r H}$ can be calculated from finite difference as in Sec. 3.3.1 and the electron-phonon coupling is given by Eq. (3.45).

$$\boldsymbol{M}_\lambda = \sum_{Iv} \left\langle \phi_i \middle| \frac{\partial \mathbf{H}}{\partial r_{Iv}} \middle| \phi_j \right\rangle \boldsymbol{e}_{\lambda,Iv} \sqrt{\frac{\hbar}{2M_I\Omega_\lambda}} \tag{3.45}$$

The dynamical matrix, **D**, and Hamiltonian derivative, $\nabla_r \mathbf{H}$ in particular, are computationally demanding to calculate from atomistic approach, and are often out of reach for systems with large device regions. In repeated two-probe systems the device region is simply a repetition of the electrode unit-cell along the transport direction and as such **D** and $\nabla_r \mathbf{H}$ can be obtained from the electrode unit-cell, reducing the calculation time drastically [73].

In calculating the inelastic current we formally have a sum over all the phonon modes. In order to reduce the computational burden, we perform a summation of the phonon modes in energy intervals to form new effective phonon modes. We typically use intervals of 10 meV length, i.e [0, 0.01]eV, [0.01, 0.02]eV, etc. Similar approximations are commonly used in other codes [74]. The sum over modes is thus replaced by a sum over phonon energy intervals using the redefined phonon modes. Otherwise the formulas remain the same.

Chapter 4

Simulator Implementation

The atomic scale calculations in this thesis are can be divided into two parts. Firstly the electronic structure of the JNT device is calculated using semi-empirical tight binding method combined with nonequilibrium Green's functions (NEGF). Then the effect of lattice vibrations (phonons) on the electronic current is calculated. These calculations are carried out using QuantumATK software [75]. QuantumATK is a highly customized software with enriched material database and library functions and modules where one can implement atomistic calculations using **Python** scripting.

The semi-empirical tight binding method can be implemented through the ATK-SE calculator based on Slater–Koster model. One very important feature of ATK-SE is that it is possible to manually define custom Slater-Koster parameters, e.g. found in scientific literature. There are two primary ingredients in a Slater-Koster (SK) model for electronic structure calculations:

1. The values of the onsite matrix elements for each element (or atom types) in the model.
2. The values of the offsite (hopping) matrix elements for each pair of atom types in the model, and how these depend on the distance between the atoms.

4.1 Nearest-neighbor model for silicon with dummy hydrogen atoms:

We will use the Boykin-type $sp^3d^5s^*$ model by Zheng *et al.* [76], which is a commonly used Slater-Koster parametrization for studying Si nanowire transistor. The model extends an earlier parametrization of Si and Ge [77], which in turn builds on the original $sp^3d^5s^*$ models by Jancu *et al.* [78].

The first step is to define the SK model for Si according to Ref. [77], then the hydrogen matrix elements will be added to the model in a second step according to Ref. [76]. These are used to remove spurious electronic states due to dangling Si surface bonds, so they basically constitute a numerical trick.

4.1.1 Onsite matrix element

First, consider the onsite matrix element. Here you need to specify the angular momenta, number of valence electrons, ionization potentials and spin-orbit split of the basis orbitals. The onsite Hartree shift and spin split are taken from built-in databases in QuantumATK. The ionization potentials and spin-orbit split can be taken directly from Ref. [77]. There are four types of valence orbitals (3s, 3p, 3d, and an excited s-type orbital, commonly denoted s^* in literature). The onsite Hartree shifts can be extracted from a built-in database; for the unoccupied orbitals 3d and s^* will use the values from the occupied valence orbitals. The spin splits are also obtained from a built-in database. The onsite matrix elements for each element in the basis set are specified as instances of the SlaterKosterOnsiteParameters ATKPython class. For the present silicon SK model, we use the variable onsite for an instance of this class.

4.1.2 Offsite matrix elements

A Slater-Koster model is in general not based on the concept of neighbors – the offsite (hopping) matrix elements are instead defined in a range of distances around each atom, possibly using a scaling function to specify the distance-dependence of the Hamiltonian matrix element. A cut-off distance should also be specified, above which atoms do not interact (the matrix element is set to zero beyond this distance). The hopping matrix elements are therefore tabulated in an interval around the silicon nearest-neighbor distance, using values from Ref. [77].

4.1.3 Defining the full Slater-Koster table

In QuantumATK, the Slater-Koster basis set should be implemented as an instance of the SlaterKosterTable ATKPython class. The onsite and offsite matrix elements in the SlaterKosterTable are defined using special keyword arguments.

4.1.3.1 Onsite parameters

The onsite matrix element for Si is simply passed to the SlaterKosterTable using the label silicon.

4.1.3.2 Offsite parameters

All the offsite matrix elements defined above are given as individual keyword arguments when setting up the SlaterKosterTable. These arguments must be on the form element1_element2_XYZ=list, where x and y are the labels of the orbitals on the first and second elements (both can be s, p, d, or f), while z is the type of interaction (s, p, or d for $\boldsymbol{\sigma}, \boldsymbol{\pi},$ or $\boldsymbol{\delta}$ respectively).

Thus, for example, the **sdπ** offsite matrix element between carbon and silicon in some hypothetical SK model would be set with the keyword si_c_sdp. In the present case of pure silicon, the full Slater-Koster table will be generated from both onsite and offsite parameters.

4.1.4 Adding hydrogen

For H-terminated Si nanowires, we need to expand the Slater-Koster table with the parameters for hydrogen from Ref. [76]. As previously discussed, the role of the hydrogen atoms is to eliminate the effects of the unsaturated Si bonds on the surface of the wire, not to represent “real” hydrogen atoms. In an experiment it is of course quite possible that hydrogen atoms, or other atoms, will attach themselves to these dangling bonds, but that is not the point here.

The onsite and offsite parameters are then simply added to the already prepared silicon SlaterKosterTable.

4.2 Electron transport with phonon coupling calculation

The effect of lattice vibrations (phonons) on the electronic current is calculated using the InelasticTransmissionSpectrum module. This module is used to calculate the transmission spectrum of the device in the presence of electron-phonon interactions. The methodology implemented in QuantumATK is based on the Lowest Order Expansion **(LOE)** [72] and the Extended LOE **(XLOE)** [71] methods. In this thesis, we will use the **XLOE** method, which treats the finite energy difference between initial and final states in the transition $\boldsymbol{k} \rightarrow \boldsymbol{k} \pm \boldsymbol{q}$ due to electron-phonon coupling in a more accurate manner.

In order to calculate the InelasticTransmissionSpectrum three main ingredients are needed:

- A DeviceConfiguration to get the Hamiltonian of the system.
- A DynamicalMatrix object for calculating the phonon modes.
- A HamiltonianDerivatives object for calculating the electron-phonon coupling matrix, M_{λ}, for a particular phonon mode, λ.

The device configuration used as input to InelasticTransmissionSpectrum must be exactly the same as used for the HamiltonianDerivatives and DynamicalMatrix objects. For device configurations with a translationally invariant central region, it is possible to calculate the HamiltonianDerivatives and DynamicalMatrix objects for bulk configurations, which can be repeated to form the central region of the device.

4.2.1 Using bulk DynamicalMatrix and HamiltonianDerivatives:

Many device calculations are performed for a structure which is translationally invariant in the C-direction, apart from doping profiles and electrostatic regions. This might be the case for a

junctionless nanowire field effect transistor (JNT) where the electrodes and the central region are composed of the same material as well as the doping profile is also same.

In that case, it is possible to calculate the DynamicalMatrix and HamiltonianDerivatives for the smallest repeatable unit cell, provided that the size of central region is integer multiple of unit cell size. The small bulk configuration should be repeated in order to form the central region.

The calculation of the DynamicalMatrix and HamiltonianDerivatives for the small bulk configuration will be much faster than the corresponding calculations for the full device configuration.

4.2.2 Summing up phonon modes in energy intervals

For a device with, say, 1000 atoms in the central region, there will be 3000 phonon modes. However, by specifying phonon energy intervals the phonon modes will be summed in each interval to form new effective phonon modes. The number of intervals required will depend on the actual system, but typical values between 10 and 50 will often suffice, thus dramatically reducing the number of required calculations.

By using both the phonon energy intervals, bulk dynamical matrix and bulk hamiltonian derivatives it is feasible to perform InelasticTransmissionSpectrum calculations for devices with several thousand of atoms.

Chapter 5

Results and Discussions

5.1 Gate All-around Junctionless Nanowire Transistor Results

To study the electronic transport characteristics and electron-phonon coupling of junctionless nanowire transistor, simulations based on self-consistent analysis using QuantumATK were performed.

The electronic transport characteristics in presence of phonon scattering was determined. Electronic band structure, transmission spectrum and projected local density of states were observed. The phonon band structure, phonon density of states and phonon transmission spectrum were also observed. The elastic and inelastic component of current were analyzed. The inelastic current distribution due to various phonon modes was explained. Then the total current of the device with varying gate and drain voltage was calculated. The drain current vs gate voltage was evaluated by varying oxide thickness, channel thickness, channel length, doping concentration, and channel material crystal orientation.

The device basic structure can be reviewed once again, unless otherwise specified:

Donor doping concentration: 1.5×10^{19} atoms/cm^3

channel length= 3nm

Channel thickness= 1.1nm

Oxide thickness= 1nm

Channel material: Si(110)

5.1.1 Electronic Bandstructure

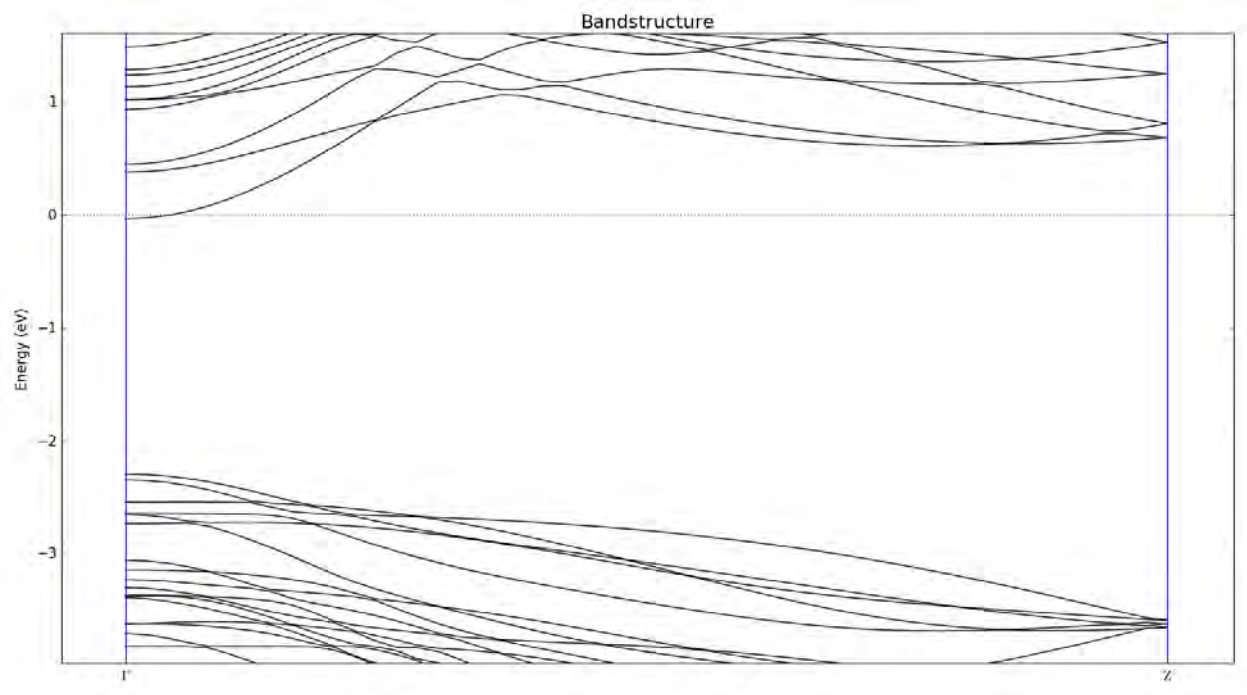

Figure 5.1.1: Electronic bandstructure of nanowire.

From the electronic bandstructure of nanowire structure in Fig. 5.1.1 we see that bandgap is direct bandgap. The conduction band minima and valance band maxima occur at the Gamma (Γ) point. This is expected because when quantum confinement increases, bandgap becomes direct. Also, bandgap is higher in nanowire structure due to quantum confinement. These results are supported by the results found in literature [79].

5.1.2 Electronic Transmission Spectrum

From the electrotonic transmission spectrum we see that transmission coefficient is higher than 1 at higher energies. Actually, it is the total transmission spectrum. At a particular energy total transmission spectrum is the summation of the transmission coefficients of each transmission channels. If several transmission channels contribute to the transmission, there will be more than one eigenvalue and each eigenvalue is restricted to the range [0, 1].

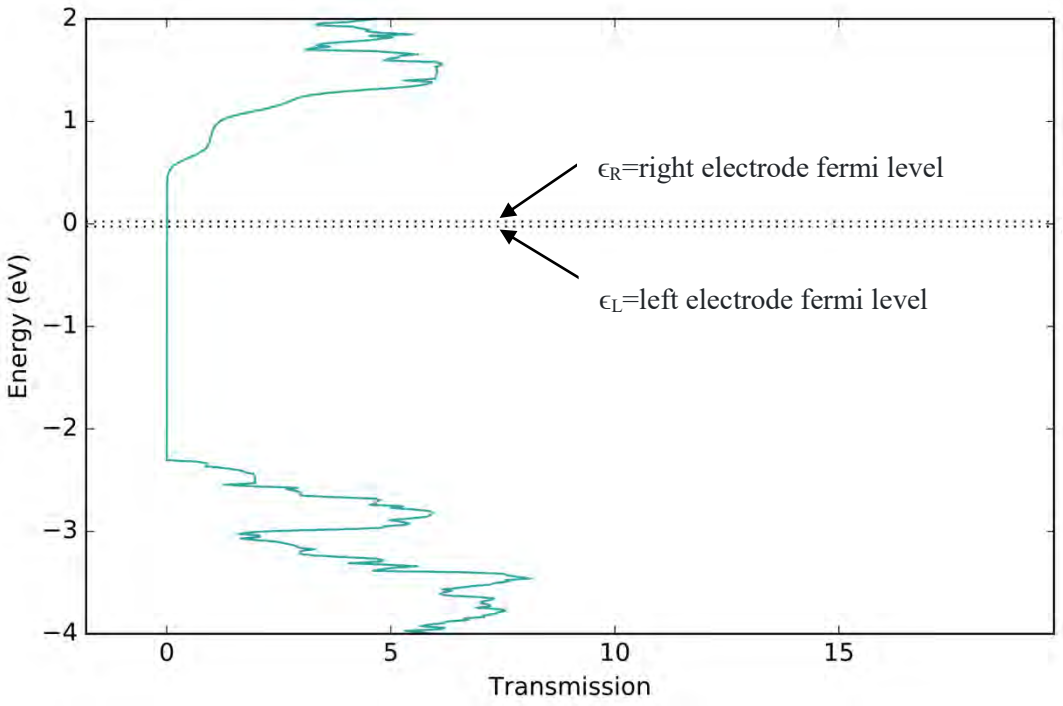

Figure 5.1.2(a): Electronic transmission spectrum of JNT at OFF state (V_{GS}= -1V, V_{DS}= 0.05V). Here the elastic current is 0.01nA

The dashed lines in Fig. 5.1.2 are the fermi energy levels. ϵ_L is the fermi level of left electrode and ϵ_R is the fermi level of right electrode. The separation between these two lines is proportional to the bias voltage shown by Eq. (5.1).

$$eV_{DS} = \epsilon_R - \epsilon_L \tag{5.1}$$

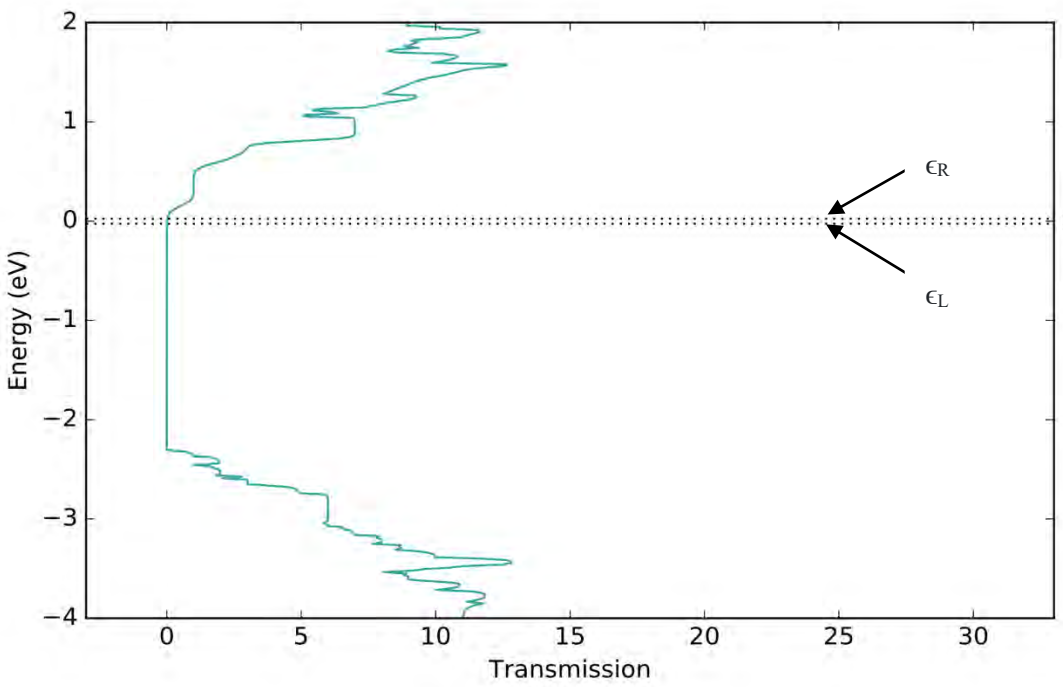

Figure 5.1.2(b): Electronic transmission spectrum of JNT at subthreshold state (V_{GS}= -0.4V, V_{DS}= 0.05V). Here elastic current is 92.512 nA

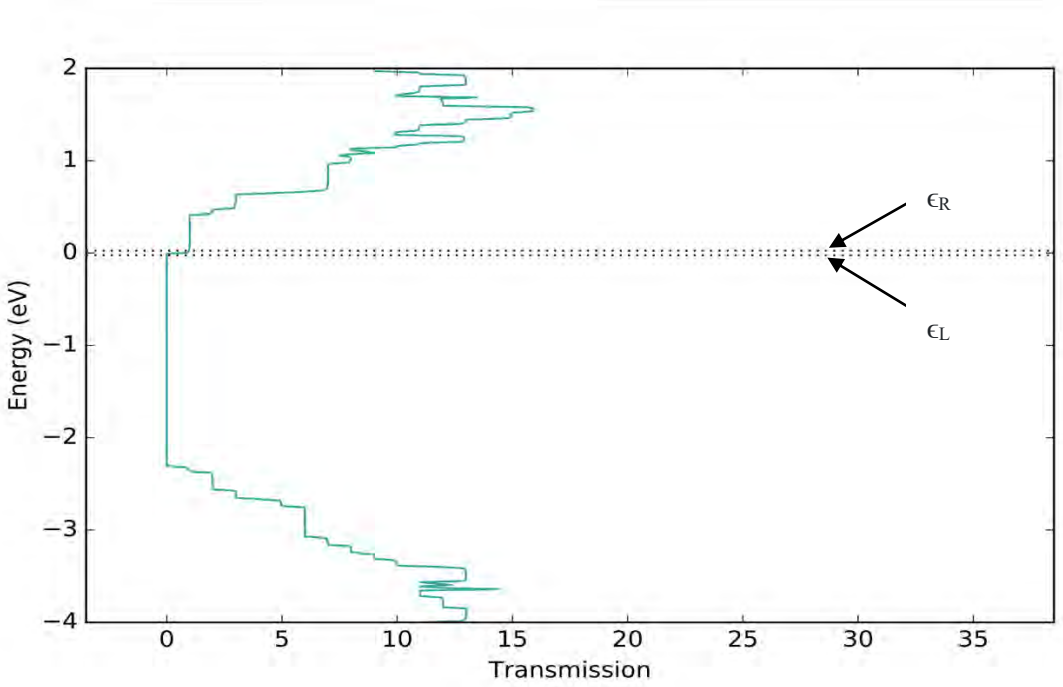

Figure 5.1.2(c): Electronic transmission spectrum of JNT at ON state (V_{GS}=0.0V, V_{DS}= 0.05V). Here elastic current is 1929.14 nA

5.1.3 Projected Local Density of States

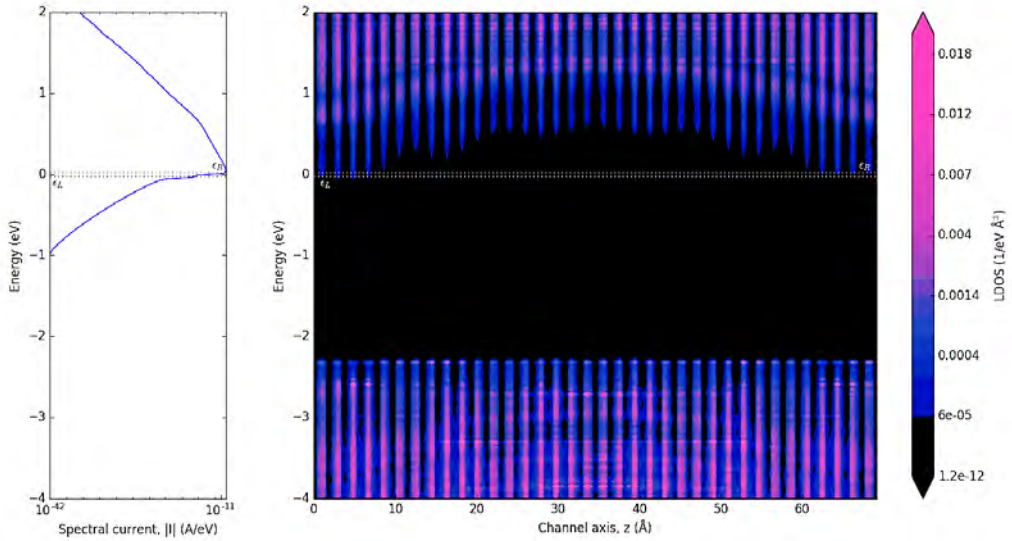

Figure 5.1.3(a): Projected Local Density of States of JNT at OFF state (V_{GS}=-1.0V, V_{DS}=0.05V).

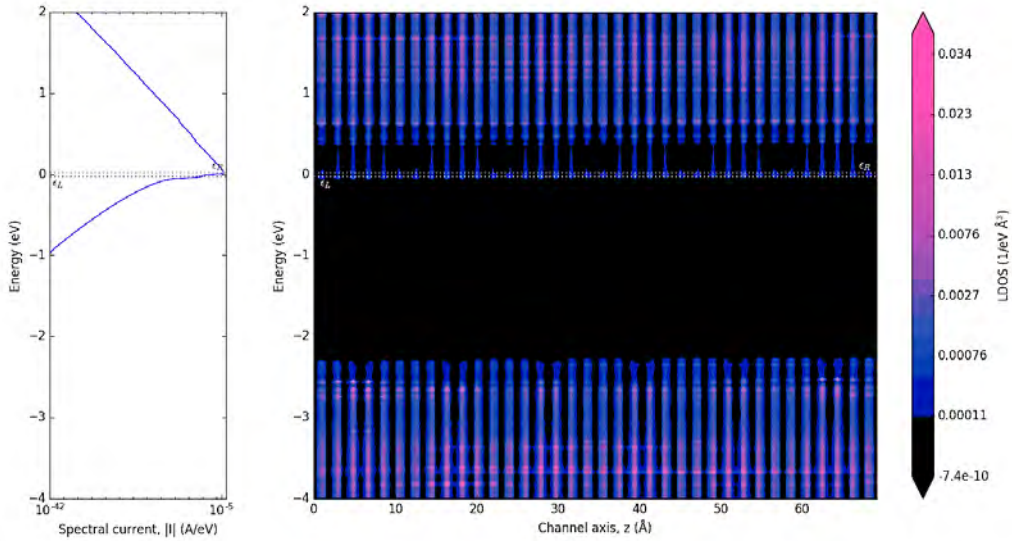

Figure 5.1.3(a): Projected Local Density of States of JNT at ON state (V_{GS}=0.0V, V_{DS}= 0.05V).

From the projected local density of states of JNT, the effect of gate voltage variation is very clear in Fig. 5.1.3. Apart from it, there is a fluctuation in the Projected Local Density of States profile which is called Van Hove singularity. This happens in the narrow and confined structures and complicate the calculation of Hamiltonian Derivatives.

5.1.4 Phonon Vibrational Modes

Inelastic current distribution due to various phonon modes of the device on various states is shown in Fig 5.1.4. In the OFF-state summation of inelastic current is positive because tunneling through potential barrier exists from source to drain. But this tunneling inelastic current is low comparative to elastic current because of high quantum confinement in ultra-narrow nanowire transistor. In quantum well or bulk devices, off state tunneling inelastic current is higher comparative to nanowire structures because of less quantum confinement.

In the sub-threshold state or ON state, summation of inelastic current is negative because here scattering is dominant than tunneling. In these states total current in the device is less than the elastic current.

Another thing can be observed that all phonon modes aren't taken into consideration because the phonon modes with higher energy have low occupation, therefore electron phonon coupling or inelastic component of current will be small for those phonon modes.

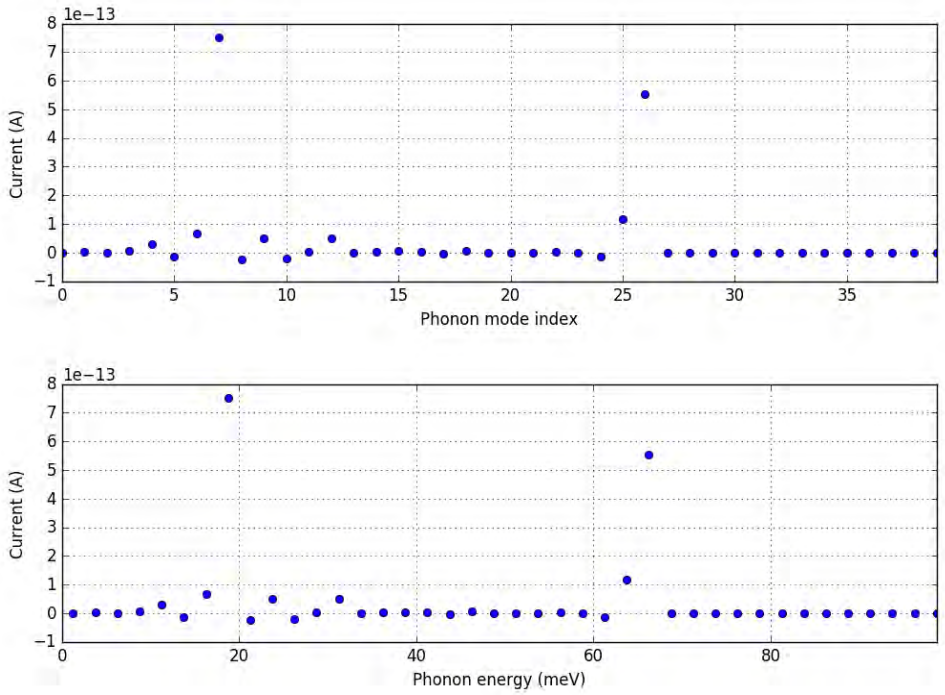

Figure 5.1.4(a): Inelastic current distribution among various phonon modes in the OFF state of the device (V_{GS}= -1V)

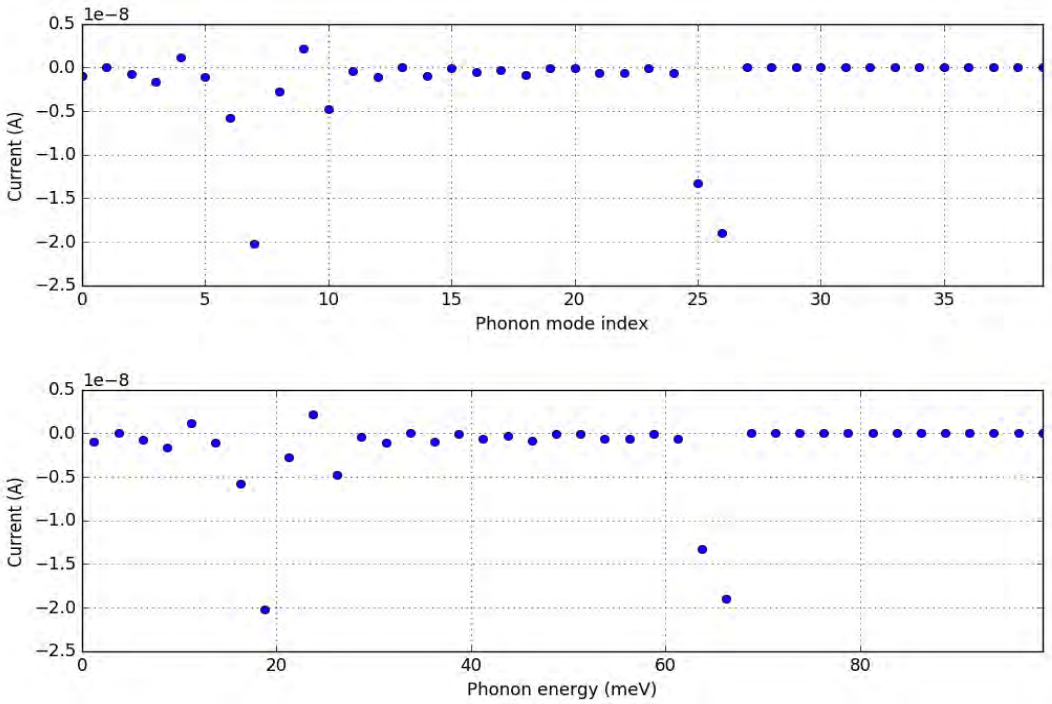

Figure 5.1.4(b): Inelastic current distribution among various phonon modes in the subthreshold state of the device (V_{GS}= -0.3V)

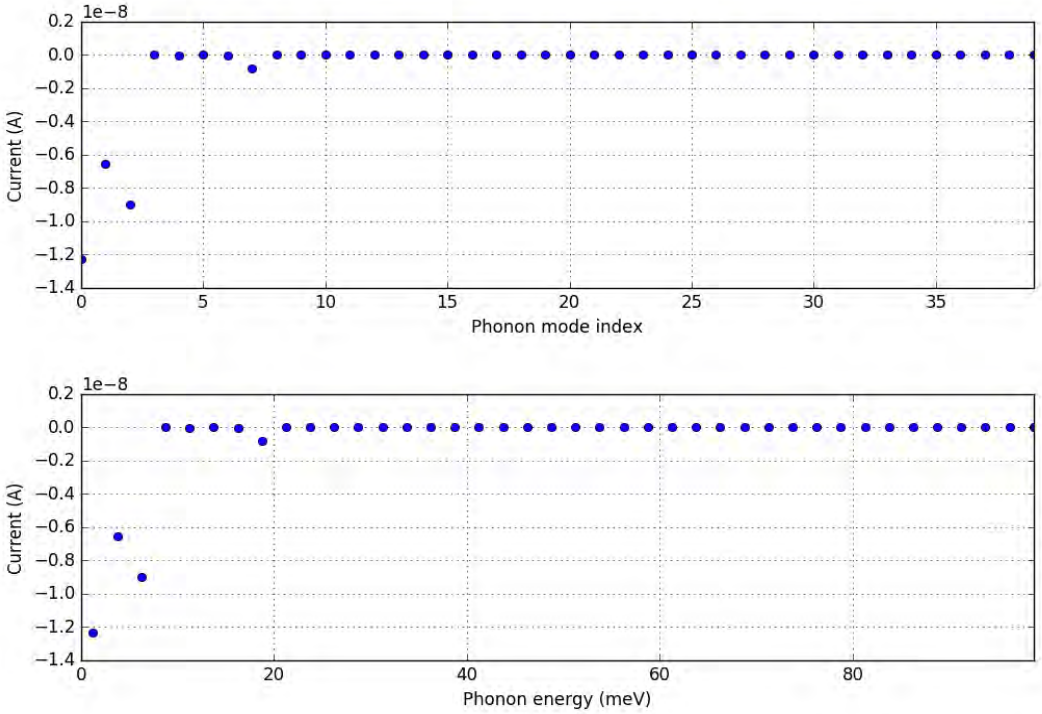

Figure 5.1.4(c): Inelastic current distribution among various phonon modes in the ON state of the device (V_{GS}= 0.0V)

5.1.5 Phonon Transmission Spectrum

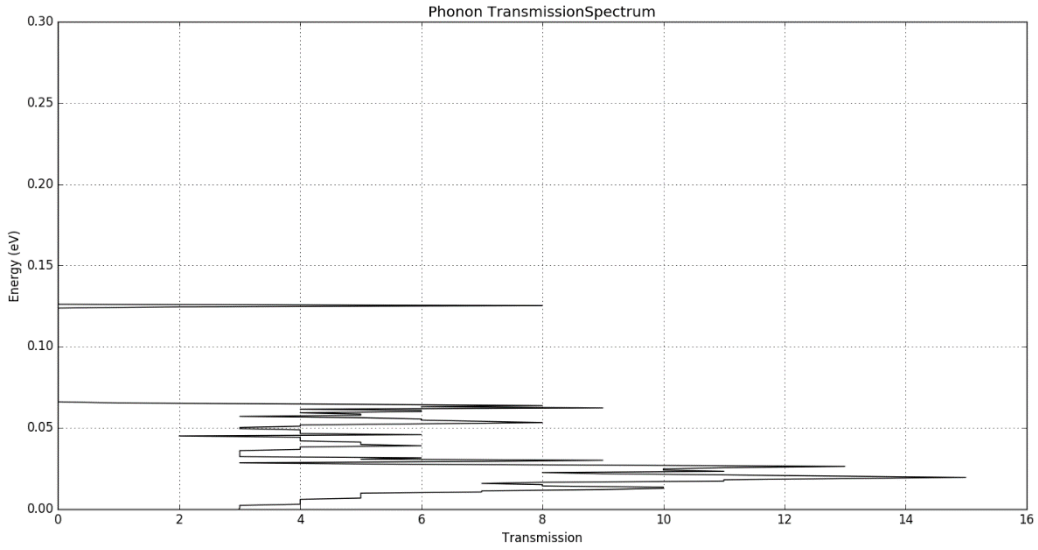

Figure 5.1.5(a): Phonon Transmission Spectrum of JNT

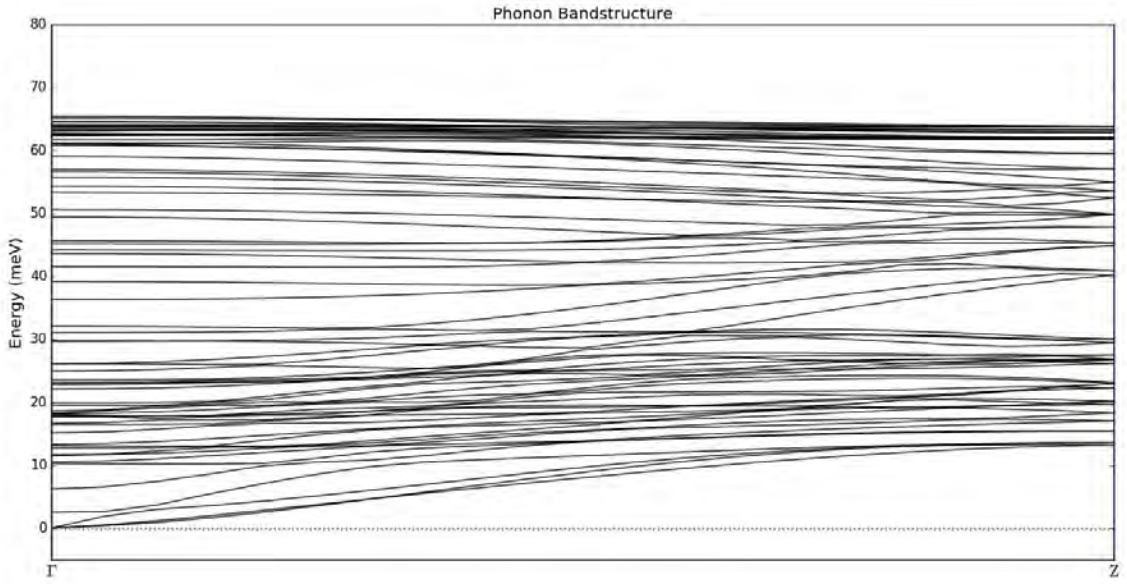

Figure 5.1.5(b): Phonon band-structure

Figure 5.1.5(a) depicts phonon bandstructure where the acoustic phonons and optical phonons are clearly visible. There are 3N number of phonon modes in a device, where, N= number of atoms in the device. Only the three phonon modes of lowest energy are acoustic phonon modes and rest of them are optical phonon modes. Acoustic phonon modes have zero energy at Gamma (Γ) point.

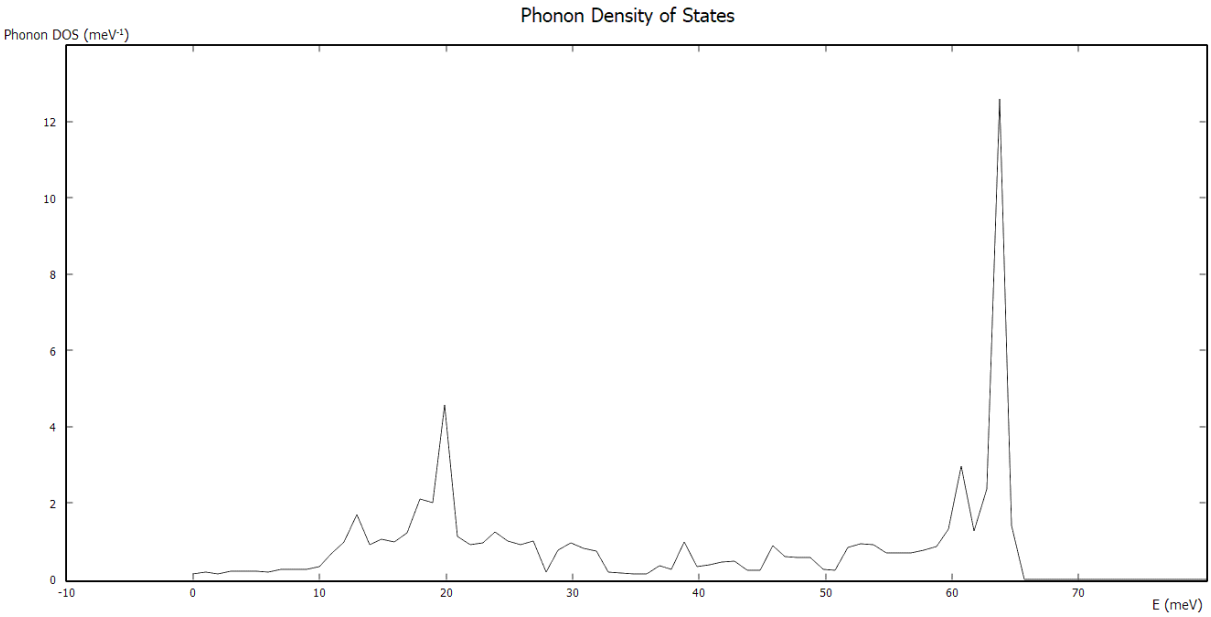

Fig 5.1.5(c): Phonon density of states (DOS) of JNT

From the phonon bandstructure and density of states we can see that phonon with higher energy has lower occupation. So only the lower energy phonons are considered in calculating electron-phonon coupling.

5.2 Drain Current vs Gate voltage

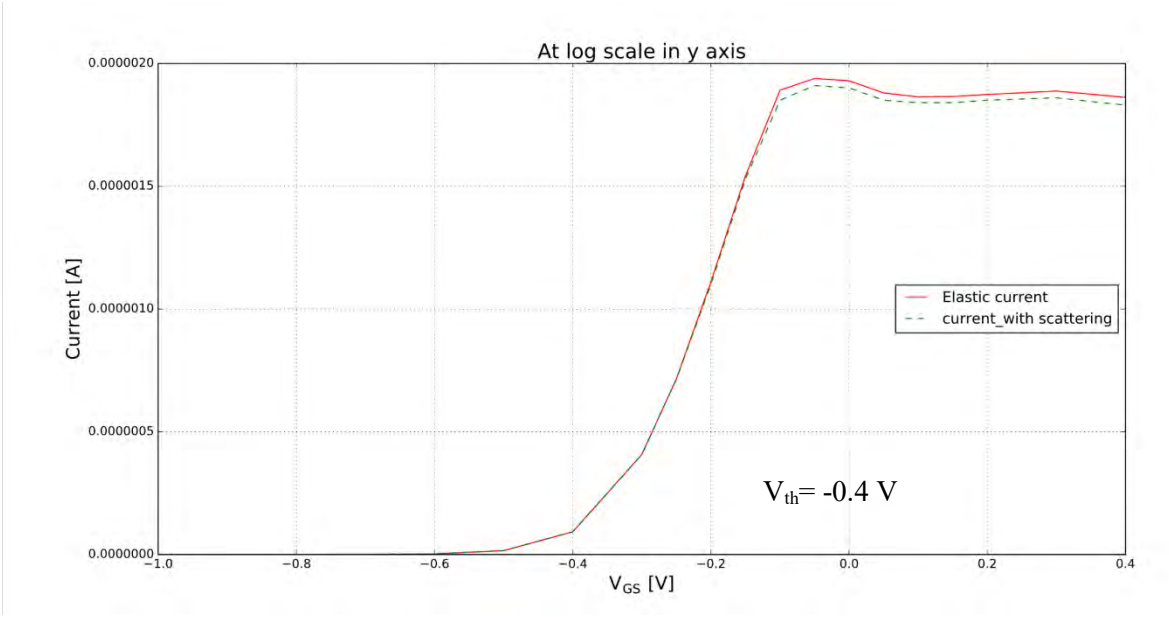

Figure 5.2(a): Drain current vs gate voltages with/without scattering at V_{DS}=0.05V.

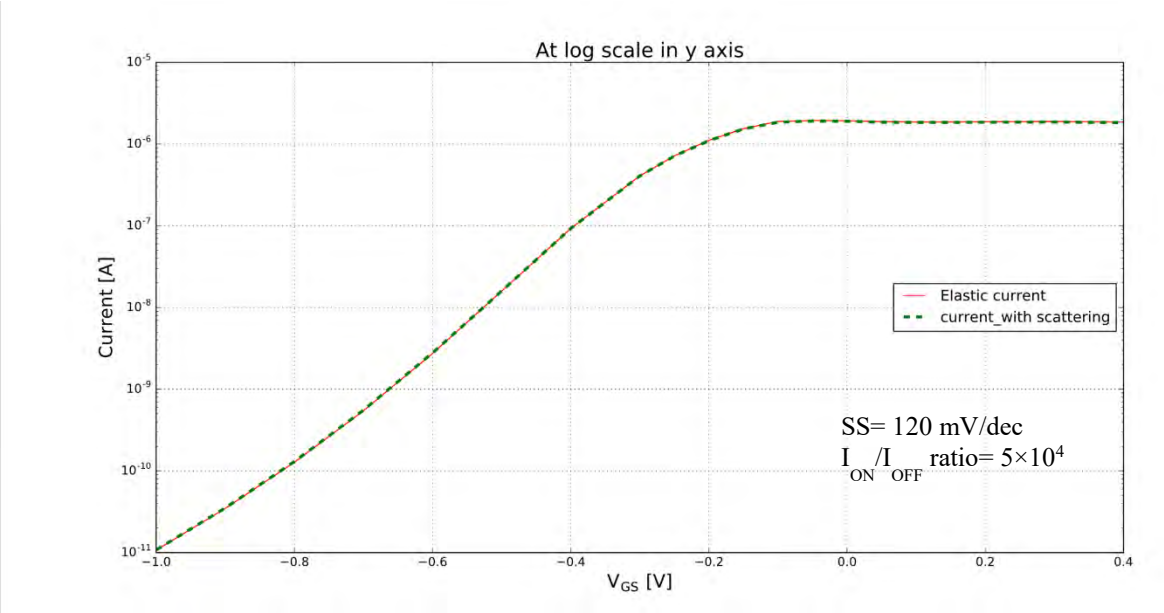

Figure 5.2(b): Drain current vs gate voltages with/without scattering at V_{DS}=0.05V (log scale).

From the drain current vs gate voltage graph in Fig. 5.2, we don't see any significant change at OFF sate because of the confinement of the nanowire structure of JNT. Here two opposite phenomena occur at a time: quantum tunneling and scattering by phonon. At the OFF state the tunneling current is counter balanced by strong scattering present in nanowire due to heavy effective mass of electron. At the ON state the strong scattering effect is clearly visible even in this ultra-short channel device where current should be nearly ballistic.

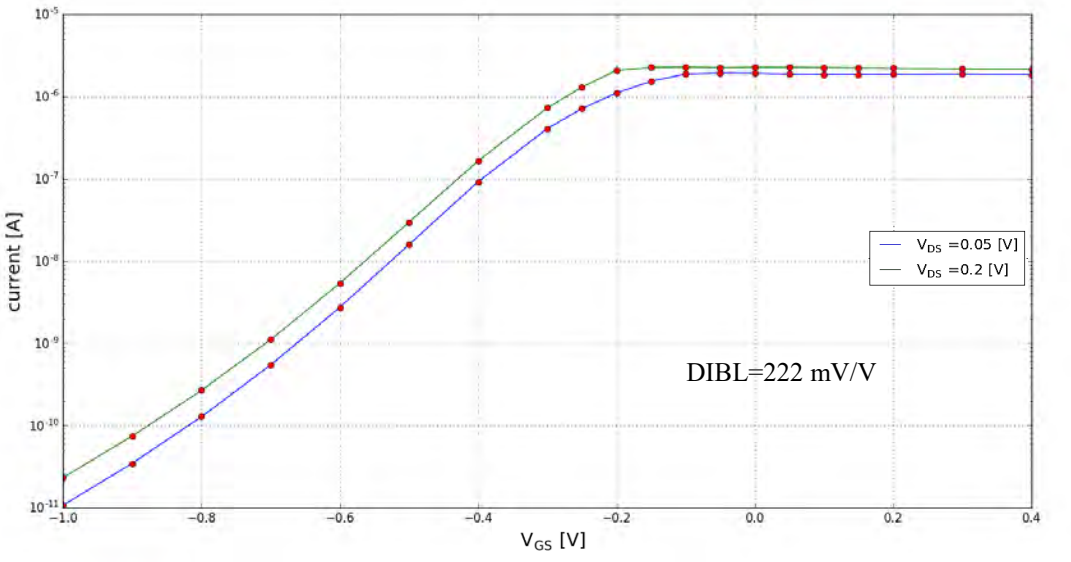

Figure 5.2(c): Drain current vs gate voltages (log scale).

5.3 Drain Current vs Drain voltage

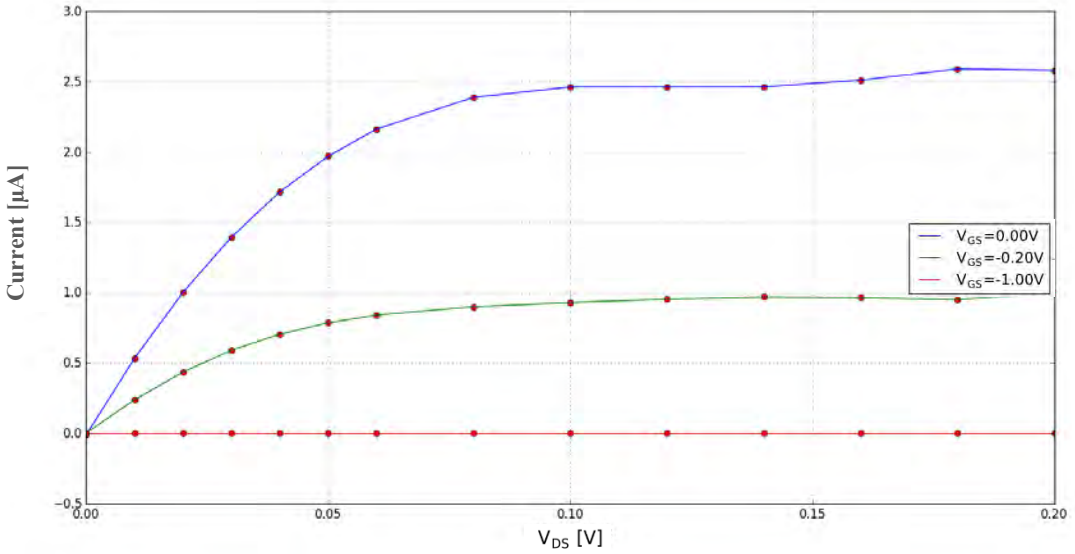

Figure 5.3: Drain current vs drain voltages (log scale).

From the drain current vs drain voltages graph in Fig. 5.3, it is seen that drain current saturates for very small drain voltages. All the current vs voltage graphs here are considering electron phonon scattering.

5.4 Oxide Thickness Variation

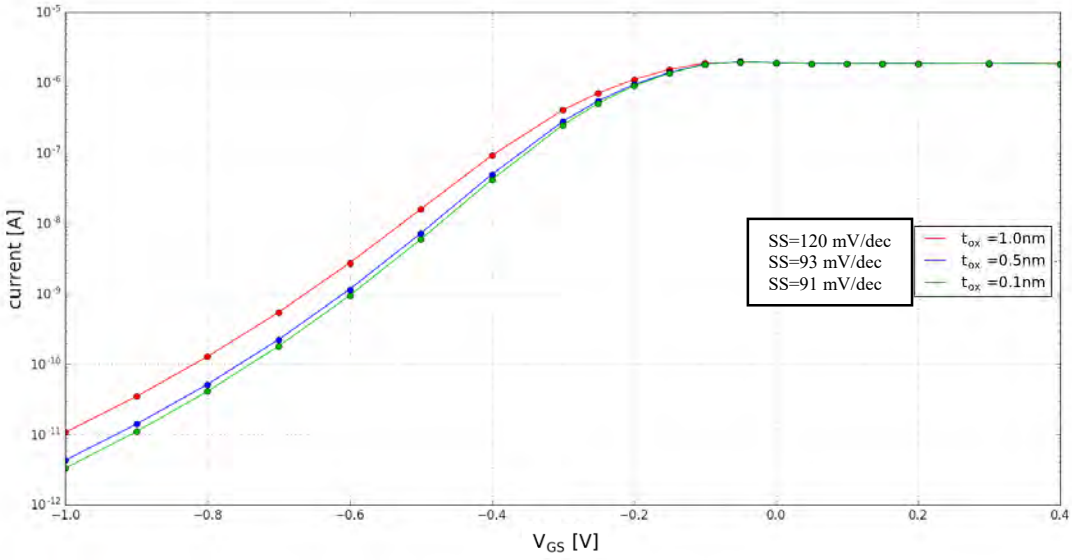

Figure 5.4: Drain current vs gate voltages for various oxide thickness.

Here we can see the effect of oxide thickness on IV characteristics. For low oxide thickness OFF state current is lower thereby decreasing the subthreshold slope.

5.5 Channel Thickness Variation

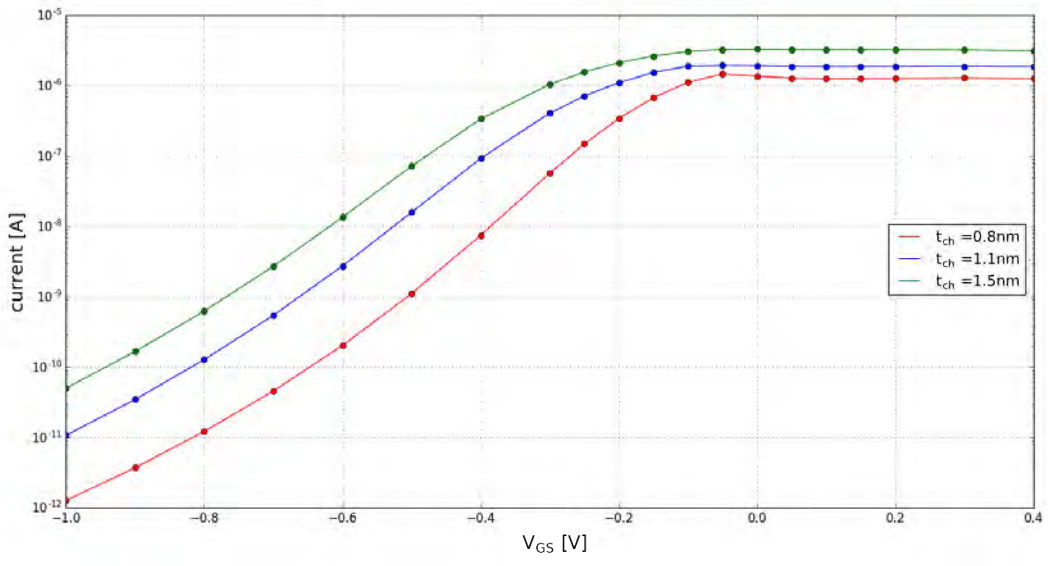

Figure 5.5: Drain current vs gate voltages for various channel thickness.

Form Fig. 5.5 we see that when channel thickness increases, the current in JNT increases and subthreshold slope (SS) increases.

5.6 Channel length Variation

In Fig. 5.6, we see an increase in OFF current with the decrease in channel length of JNT. The subthreshold slope (SS) also increases with decreasing channel length. When the channel length decreases, the direct source to drain tunneling current increases in the OFF state of JNT.

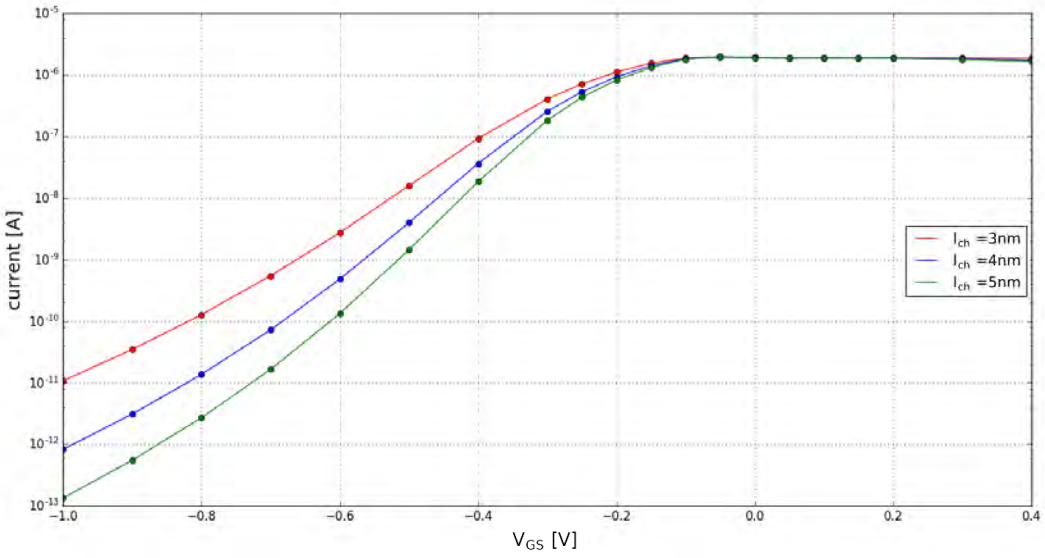

Figure 5.6: Drain current vs gate voltages for various channel length.

5.7 Doping Variation

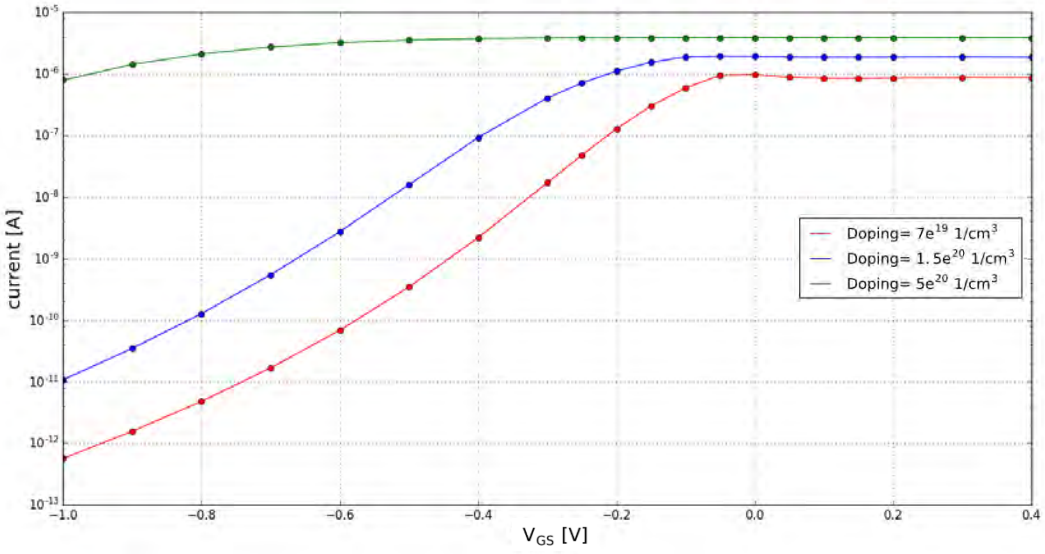

Figure 5.7: Drain current vs gate voltages for various n type doping.

The doping variation greatly changes the subthreshold slope as shown in the Fig. 5.7. The drain current vs gate voltage curve has the lowest subthreshold slope.

5.8 Nanowire Crystal Orientation Variation

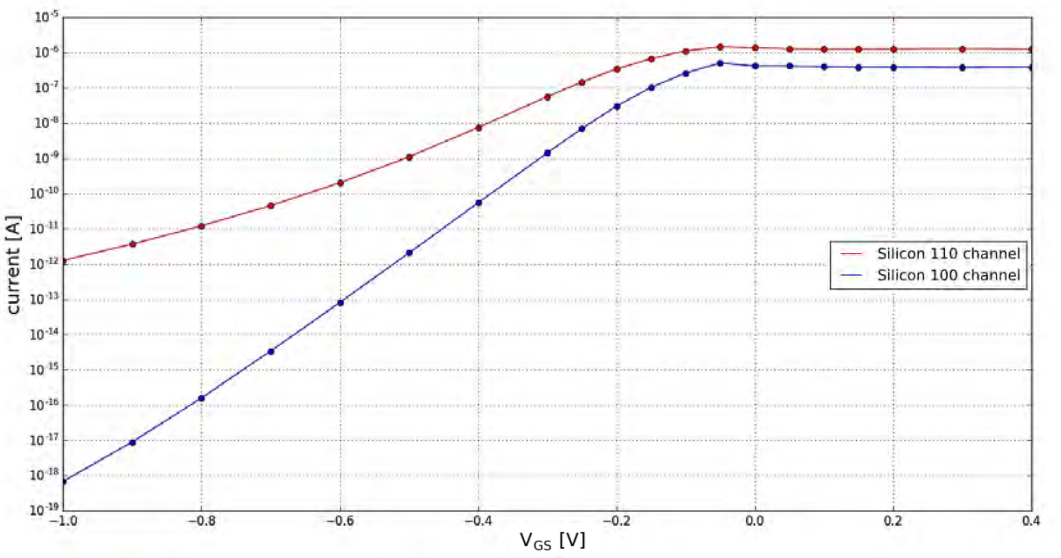

Figure 5.8: Drain current vs gate voltages for various silicon crystal orientation.

The silicon 100 crystal orientation has lower subthreshold slope than silicon 110 crystal orientation as shown in the Fig. 5.8

5.9 Benchmarking

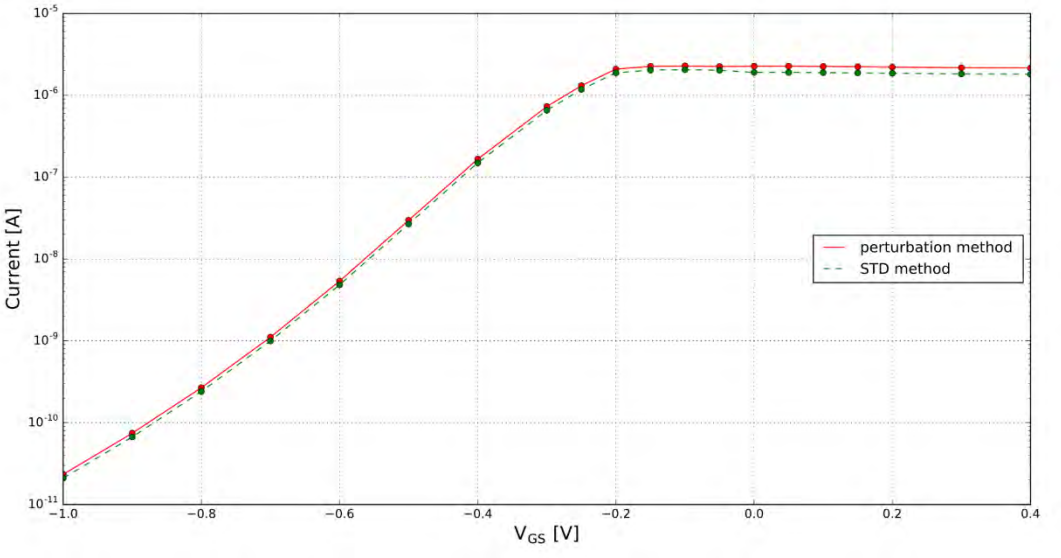

Figure 5.9: Drain current vs gate voltages for perturbation method and STD method.

I have validated my approach by comparing my result with a very different approach called STD method (Special thermal displacement method). In STD method at first the thermally displaced device configuration was determined using phonon dynamical matrix and then the electronic transmission spectrum was evaluated using density functional theorem (DFT). The current with phonon coupling is then calculated from the transmission spectrum. In STD method there is no need to calculate hamiltonian derivatives. On the other hand, the perturbation theory approach requires both dynamical matrix and hamiltonian derivatives calculation. From the Fig. 5.9 we see that the two very different approaches give similar results.

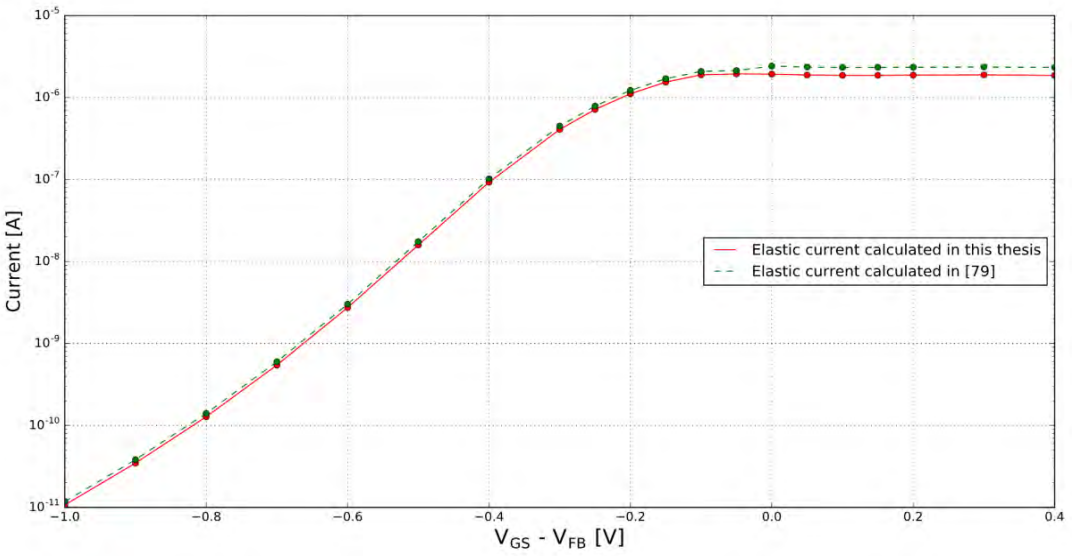

Figure 5.10: Drain current vs gate voltages calculated in this thesis and in [79].

I have also validated my approach by comparing the elastic current calculated in this thesis with that of a paper [79].

From the Fig. 5.10 we see that the two results are approximately same.

Chapter 6

Conclusion

6.1 Summary

A computationally efficient quantum mechanical atomistic approach has been used in this thesis to demonstrate the electronic transport characteristics of the Gate All-Around Junctionless nanowire Transistor (GAA-JNT) in presence of electron-phonon scattering.

To get the accurate electronic transport characteristics of the device, atomistic tight-binding method has been used instead of conventional effective mass approach. The semi-empirical tight binding method is used as atomistic approach instead of Density Functional Theory (DFT) because the semi-empirical method requires less computational time than DFT. Another reason is that DFT has a problem of underestimation of bandgap.

The effect of phonon scattering on electronic current of the device is calculated from the perturbation theory implemented by the extended lowest order expansion (XLOE) method. The phonon scattering is viewed as perturbation to the non-interacting current. Several approximations have been used to reduce the computational burden.

To calculate the inelastic part of the current due to electron phonon inelastic scattering, dynamical matrix and hamiltonian derivatives has been calculated. Dynamical matrix is calculated using force field method. The hamiltonian derivatives calculation is done using SlaterKoster tight-binding method. To reduce the computational burden, dynamical matrix and hamiltonian derivatives is calculated for the smallest repeatable unit cell as the device structure is translationally invariant in the transport direction. To further reduce the computational burden, a small number of dominant phonon vibrational modes has been used.

The electronic transport characteristics of the device has been demonstrated by varying different structural parameters, crystal orientation, etc.

6.2 Future Scope

In this thesis, I have performed a quantum mechanical analysis of the device. However, there is a substantial scope of improvement in the analysis what we have done. Some of them are discussed below in brief:

1. I have used Si as semiconductor and hafnium dioxide and silicon dioxide as insulator oxide. I can implement the method of quantum mechanical analysis for any other semiconductor material and insulator oxide.
2. I have used the Gate All Around structure of JNT in thesis. Double Gate structure or Tri Gate Structure of JNT could be used.
3. Effects of gate tunneling current and leakage was ignored. This could be studied with proper parameter introduction.
4. Instead of tight building model, Density Functional Theory (DFT) could be used. To mitigate the problem of underestimation of bandgap in DFT, another first principle approach LDA+1/2 [18] could be used.
5. To calculate the electron-phonon coupling effect on electronic current, Special Thermal Displacement (STD) method could be used instead of extended lowest order expansion (XLOE) method.
6. The effect of phonon scattering is studied here only for JNT. This could be done for any devices.

Appendix

A.1 Nearest-neighbor tight binding model implementation using Python

A.1.1 Onsite matrix element

```
# Define ionization potentials
Es    = -2.15168*eV
Ep    =  4.22925*eV
Ed    = 13.78950*eV
Es1   = 19.11650*eV

# Define spin-orbit split
split =  0.01989*eV

onsite = SlaterKosterOnsiteParameters(
            element                    = Silicon,
            angular_momenta            = [0,1,2,0],
            number_of_valence_electrons = 4,
            filling_method             = SphericalSymmetric,
            ionization_potential       = [Es,Ep,Ed,Es1],
            onsite_hartree_shift= ATK_U(PeriodicTable.Silicon, ["3p"], 'ncp')[0],
            onsite_spin_split= ATK_W(PeriodicTable.Silicon, [ "3p", "3p", "3p", "3s" ]),
            onsite_spin_orbit_split= [0.0,2*split, 0.0, 0.0]*eV,
           )
```

A.1.2 Offsite matrix elements

```
from math import sqrt

# ------------------------------------------------#
#                    Silicon                      #
#------------------------------------------------#
# a is the cubic lattice constant
a = 5.431*Ang
```

```
# Nearest neighbor distance
d_n1 = sqrt(3.0)/4.0*a
# Second-nearest neighbor distance
d_n2 = sqrt(2.0)/2.0*a

# Setup list of distances
epsilon = numpy.linspace(-0.20, 0.20, 41)
distances = [ d_n1*(1.0+x) for x in epsilon ] + [ 0.5*(d_n1+d_n2) ]

# Setup hopping elements
si_si_sss   = [ -1.95933*eV for x in epsilon ]
si_si_s1s1s = [ -4.24135*eV for x in epsilon ]
si_si_ss1s  = [ -1.52230*eV for x in epsilon ]
si_si_sps   = [  3.02562*eV for x in epsilon ]
si_si_s1ps  = [  3.15565*eV for x in epsilon ]
si_si_sds   = [ -2.28485*eV for x in epsilon ]
si_si_s1ds  = [ -0.80993*eV for x in epsilon ]
si_si_pps   = [  4.10364*eV for x in epsilon ]
si_si_ppp   = [ -1.51801*eV for x in epsilon ]
si_si_pds   = [ -1.35554*eV for x in epsilon ]
si_si_pdp   = [  2.38479*eV for x in epsilon ]
si_si_dds   = [ -1.68136*eV for x in epsilon ]
si_si_ddp   = [  2.58880*eV for x in epsilon ]
si_si_ddd   = [ -1.81400*eV for x in epsilon ]
```

A.1.3 Defining the full Slater-Koster table

A.1.3.1 Onsite parameters

```
# Create Slater-Koster table
basis_set = SlaterKosterTable(silicon     = onsite)
```

A.1.3.2 Offsite parameters

```
# Create Slater-Koster table
basis_set = SlaterKosterTable(silicon     = onsite,
                              si_si_sss   = zip(distances,si_si_sss),
                              si_si_s1s1s = zip(distances,si_si_s1s1s),
                              si_si_ss1s  = zip(distances,si_si_ss1s),
                              si_si_sps   = zip(distances,si_si_sps),
                              si_si_s1ps  = zip(distances,si_si_s1ps),
                              si_si_sds   = zip(distances,si_si_sds),
                              si_si_s1ds  = zip(distances,si_si_s1ds),
                              si_si_pps   = zip(distances,si_si_pps),
                              si_si_ppp   = zip(distances,si_si_ppp),
                              si_si_pds   = zip(distances,si_si_pds),
                              si_si_pdp   = zip(distances,si_si_pdp),
                              si_si_dds   = zip(distances,si_si_dds),
                              si_si_ddp   = zip(distances,si_si_ddp),
                              si_si_ddd   = zip(distances,si_si_ddd),
                             )
```

A.1.4 Adding hydrogen

The **onsite** matrix element for hydrogen is added like this:

```
# Define ionization potentials
Es_H    =  0.999840*eV

onsite_H = SlaterKosterOnsiteParameters(
                element                 = Hydrogen,
                angular_momenta         = [0],
                occupations             = [1.0],
                ionization_potential    = [Es_H],
                filling_method          = SphericalSymmetric,
                onsite_hartree_shift    = ATK_U(PeriodicTable.Hydrogen, ['1s']),
                onsite_spin_split       = [[0.0]]*eV,
                onsite_spin_orbit_split = [0.0]*eV,
                vacuum_level            = 0.0*Hartree,
```

Specifying the **offsite** parameters is done like this:

```
# reference distances
d_h_n1 = 1.4*Angstrom
d_h_n2 = 2.2*Angstrom

# Setup list of distances
h_distances = [d_h_n1 * (1.0+r) for r in epsilon] + [0.5 * (d_h_n1+d_h_n2)]

# Setup hopping elements
h_si_sss  = [ -3.999720*eV / 1.0 for r in epsilon ]
h_si_ss1s = [ -1.697700*eV / 1.0 for r in epsilon ]
h_si_sps  = [  4.251750*eV / 1.0 for r in epsilon ]
h_si_sds  = [ -2.105520*eV / 1.0 for r in epsilon ]
```

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