L-3/T-2/EEE **Date: 13/01/2021**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-II B.Sc. Engineering Examination 2018-19

Sub: **EEE 303** (Digital Electronics)

Full Marks: 180 Time 2 Hours

The Figures in the margin indicate full marks

USE SEPARATE SCRIPTS FOR EACH SECTION

There are 5 page(s) in this question paper.

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**

All the symbols have their usual meaning

Assume reasonable values for missing data.

For answers, show detailed step by step calculations where applicable

1. (a) Convert $2345|_6$ into Binary, Octal and Hexadecimal. (15)

   (b) Explain with timing diagram, for Dynamic RAM, how you can increase the number of addresses with smaller number of address bits?. (15)

2. (a) Figure 2 shows a 7 segment display. Write the SOP logic expression for the segment g for showing Hexadecimal digits with it. (15)

   (b) With a K map, find the minimum logic expression for segment g in Figure 2. (15)

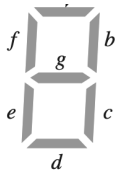

Figure 2 Different Segments of a 7 Segment Display

3. (a) Figure 3(a)(i) shows the different faces of a physical dice. Figure 3(a)(ii) shows a LED dice. Write a Verilog code that takes a 3 bit input ($I_2I_1I_0$) and has outputs as O_2, O_3, O_4, O_5, O_6, O_7, O_8 corresponding to the figure's LEDs (Each circle shows the position of an LED and assume active high (20)

output). Write a verilog code that would light up the LEDs corresponding to the inputs.

(b) Using transmission gates, draw a circuit diagram that gives O_8 output with 3 bit input ($I_2I_1I_0$) (10)

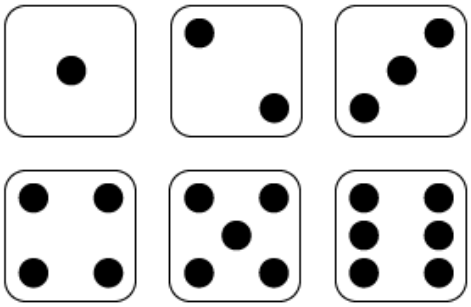

Figure 3(i) All faces of a Physical Dice

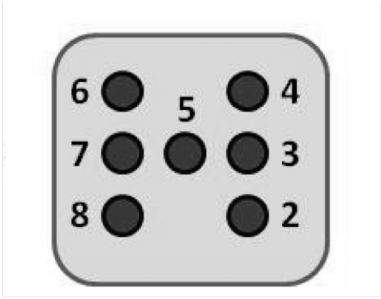

Figure 3(ii) LED Dice

4 (a) Using Diode Transistor Logic, implement the logic circuit shown in Figure 4(a). Assume you have 3 inputs, A,B and C and 1 digital output. 15

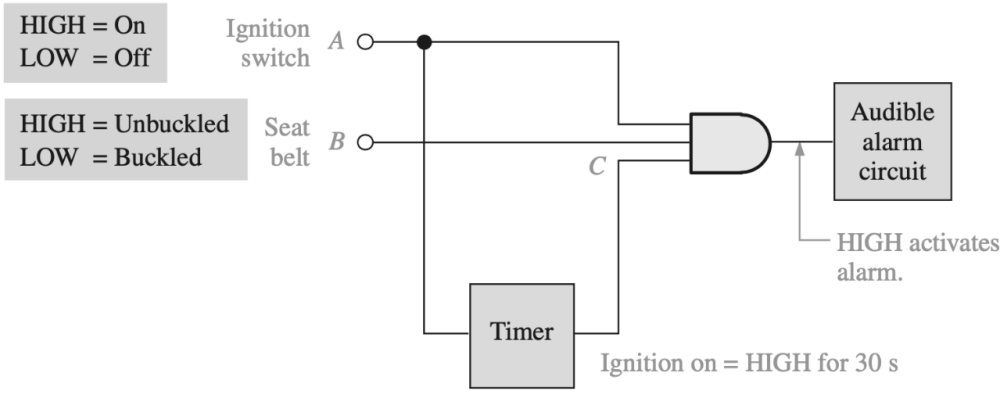

Fig 4(a) Car Seatbelt Alarm Circuit

(b) The Apple M1 SoC processor has Maximum power dissipation of 13.8W, and it has a maximum frequency of 3.204GHz. Assume all dissipated power is equally distributed to the 16 Billion transistors as dynamic power consumption from MOSFETS (ignore quantum effects and resistive losses), if the supply voltage is 0.5V, what will be average value of gate capacitance? (If you don't have a scientific calculator, approximate the values for ease of calculation) 15

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**

All the symbols have their usual meaning.

Assume reasonable values for missing data.

5. **(a)** Joey has been assigned to construct a Binary Coded Decimal (BCD) adder which adds two BCD digits ($X = x_3x_2x_1x_0$ and $Y = y_3y_2y_1y_0$) and a carry-in (C_{in}). It produces the BCD sum ($S = s_3s_2s_1s_0$) and a carry-out (C_{out}). While going through the old documents, he found the following Fig. for Q. 5(a):

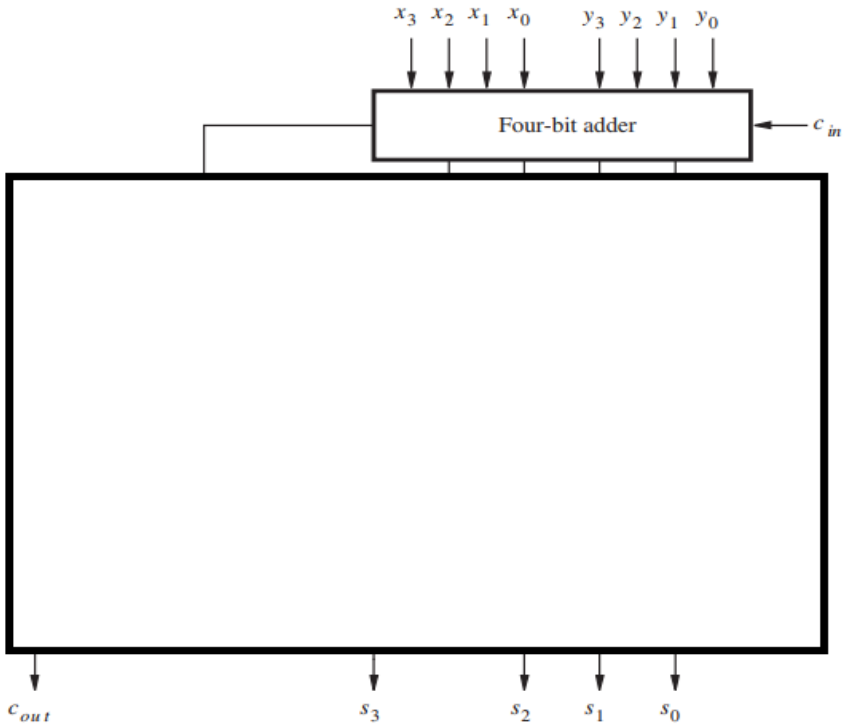

Fig. for Q. 5(a)

Complete the empty box for this BCD adder with as few components as possible. Briefly discuss the reaons behind using these components.

(b) Kimi needs a 10 MHz clock signal for his project. He has been given only a single 40 MHz clock signal. Draw the circuit for obtaining the desired clock signal of 10MHz from the given clock signal using T flip-flops and other necessary logic gates.

6. **(a)** Erwin found the following Fig. for Q. 6(a) in the basement:

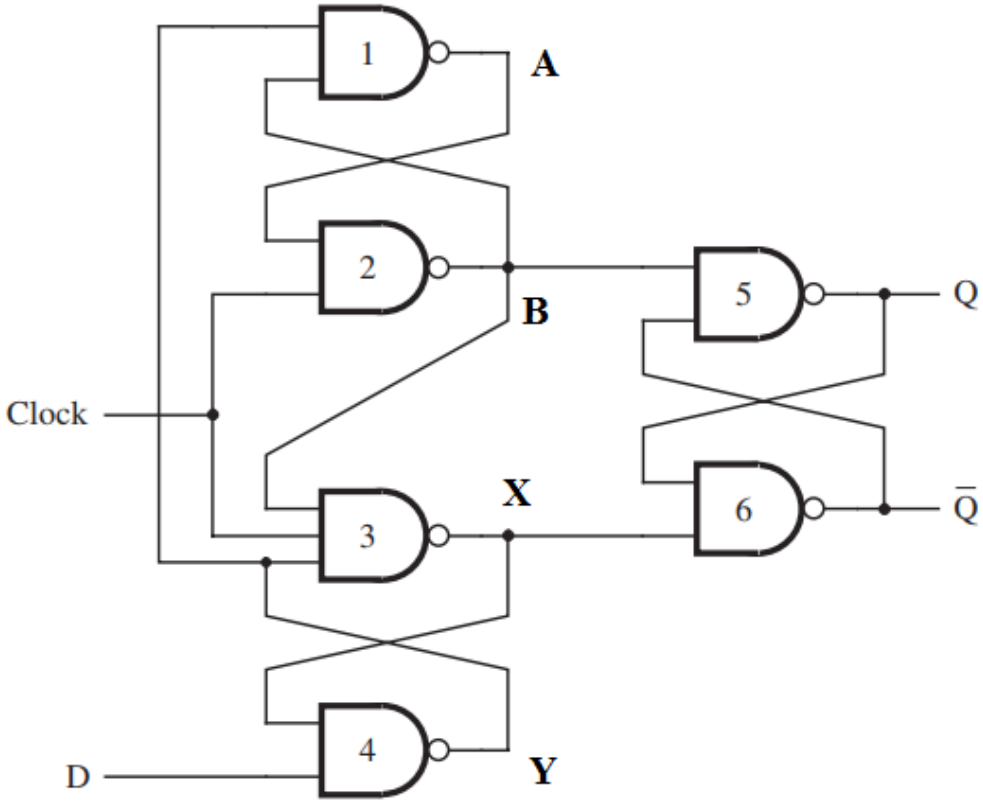

Fig. for Q. 6(a)

Answer the followings:

i. This system accomplishes the task of which component?

ii. What is the value of A, B, X and Y when Clock=0?

iii. Suppose, D=0. Which events take place when the Clock changes to 1 from 0?

iv. Show that, any changes in D will not affect the output (Q and $\bar{Q}$) as long as Clock=1 (only for the case when D=0 at the positive edge of the clock).

(b) Show how a T flip-flop can be constructed using a D filp-flop and other basic logic gates.

7. **(a)** Four sensors (sensor 0, 1, 2 and 3) are used for detecting radioactivity of a sample in a box. Sensor 3 has the highest accuracy, followed by sensors 1, 0 and 2. All the sensors might not be active at the same time. Derive the truth table of the priority encoder that will provide the sensor number (in binary) with the highest accuracy available at any given time. Write down only the

necessary logic expressions for building this encoder. You do not have to draw the circuit.

(b) Cyrus Smith is left in a mysterious island with only a single 3-to-8 binary decoder and a 6-input OR gate. He needs to obtain the function $f(w_1, w_2, w_3) = \sum m(0,2,3,5,7)$ in order to send a signal to a ship. Draw the logic circuit that will perform the function with given components.

8. **(a)** Kageyama has invented a synchronous sequential circuit which provides an output of 1 in the current cycle when two consecutive values are same. Otherwise, the value of z is equal to 0. Answer the following questions:

   i. Why this circuit is a Mealy type circuit?

   ii. Draw the state diagram and complete other steps to derive the necessary logic expressions for constructing this circuit. You do not need to draw the circuit.

(b) Draw only the state diagram of an asynchronous gated D latch which has the following truth table:

Clk	D	$Q(t+1)$
0	x	$Q(t)$
1	0	0
1	1	1

L-3/T-2/EEE **Date: 17/01/2021**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-II B.Sc. Engineering Examination 2019-20

Sub: **EEE 313** (Solid State Devices)

Full Marks: 180 Time 2 Hours

The Figures in the margin indicate full marks

USE SEPARATE SCRIPTS FOR EACH SECTION

There are THREE page(s) in this question paper.

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**

All the symbols have their usual meanings

Assume reasonable values for missing data.

1. Estimate the current density flowing through the Si sample with the energy band diagram shown in Fig. for Q-1 at room temperature. [E_{fe} = electron quasi-Fermi level, E_{fh} = hole quasi-Fermi level, $N_c = 2.9\times10^{19}$ cm^{-3}, electron mobility= 300 cm^2/V-s] (30)

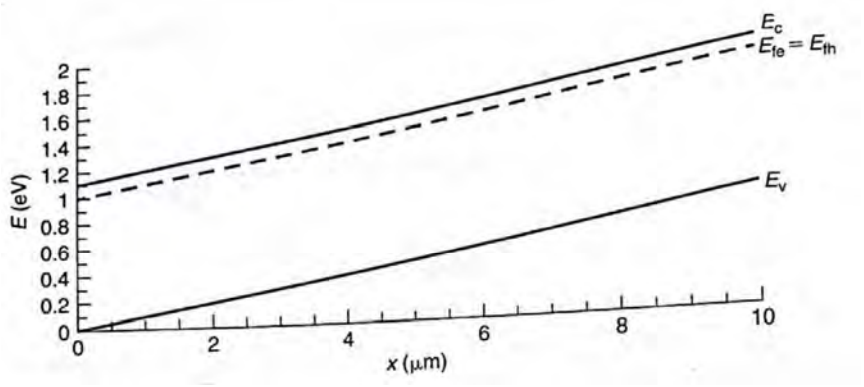

Fig. for Q-1

2. Consider the p-type semiconductor shown in Fig. for Q-2 with the following parameters: $N_a = 5\times10^{16}$ cm^{-3}, $D_n = 25$ cm^2/s, and $\tau_{n0} = 5\times 10^{-7}$ s. The surface recombination velocities at the two surfaces are shown. The electric field is zero. The semiconductor is illuminated at x = 0 with an excess carrier generation rate (30)

equal to g' = 2×10^{21} cm^{-3}-s^{-1}. Determine the excess minority carrier electron concentration versus x in steady state.

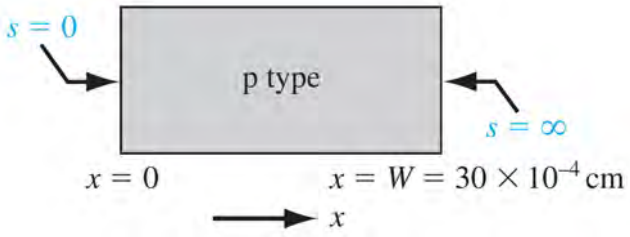

Fig. for Q-2

3. A silicon PIN junction has the doping profile shown in Fig. for Q-3. The "i" corresponds to an ideal intrinsic region in which there is no impurity doping concentration. A reverse-biased voltage is applied to the PIN junction so that the total depletion width extends from -2 μm to +2 μm. (a) Using Poisson's equation, calculate the magnitude of the electric field at x = 0. (b) Sketch the electric field through the PIN junction. (c) Calculate the reverse-biased voltage that must be applied. (30)

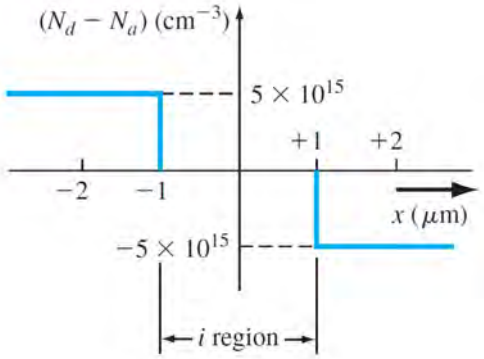

Fig. for Q-3

4 A silicon pn junction with a cross-sectional area of 10^{-4} cm^2 has the following properties at T=300 K: (30)

$N_d = 10^{17}$ cm^{-3}	$N_a = 5\times10^{15}$ cm^{-3}
$\tau_{p0} = 10^{-7}$ s	$\tau_{n0} = 10^{-6}$ s
$\mu_n = 850$ cm^2/V-s	$\mu_n = 1250$ cm^2/V-s
$\mu_p = 320$ cm^2/V-s	$\mu_p = 420$ cm^2/V-s

(a) Sketch the thermal equilibrium energy-band diagram of the pn junction, including the values of the Fermi level with respect to the intrinsic level on each

side of the junction. (b) Calculate the reverse-saturation current I_s and determine the forward-bias current I at a forward-bias voltage of 0.5 V. (c) Determine the ratio of hole current to total current at the space charge edge x_n.

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**

All the symbols have their usual meanings

Assume reasonable values for missing data.

5. A p-channel, n^+-polysilicon-SiO_2-Si MOSFET has $N_d = 10^{17}$ cm^{-3}, oxide charge density is 5×10^{10} cm^{-2}, and oxide thickness is 10 nm. Calculate the threshold voltage. (30)

6. Consider a MOS capacitor made on a p-type substrate with doping of $10^{16} cm^{-3}$. The SiO_2 thickness is 500 Å and the metal gate is made from aluminum. Calculate the oxide capacitance, the capacitance at the flat band, and the minimum capacitance at threshold. (30)

7. Consider an npn Si-BJT at 300 K with the following parameters: $N_{de} = 10^{18}$ cm^{-3}, $N_{ab} = 10^{17}$ cm^{-3}, $N_{dc} = 5 \times 10^{16}$ cm^{-3}, $D_b = 30.0$ $cm^2 s^{-1}$, $L_b = 15.0$ μm, $D_e = 10.0$ $cm^2 s^{-1}$, $L_e = 5.0$ μm. Calculate the maximum base width, W_b, that will allow a current gain β of 100 when the EBJ is forward biased at 1.0 V and the BCJ is reverse biased at 5.0 V. (30)

8. For a tungsten-silicon Schottky diode with $N_D = 10^{16}$ cm^{-3}, find the barrier height and depletion layer width if the saturation current $J_s = 6.5 \times 10^{-5}$ A/cm^2. Consider $A^* = 110$ $A/K^2\text{-}cm^2$, and T = 300° K. Compare the saturation current J_s with J_{p0} assuming that the minority carrier lifetime in Si is 10^{-6} s and $D_p = 10.0$ $cm^2 s^{-1}$. (30)

L-3/T-2/EEE **Date: 1/04/2021**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-II B.Sc. Engineering Examination 2018-19

Sub: **EEE 315** (Power Electronics)

Full Marks: 180 Time 2 Hours

The Figures in the margin indicate full marks

USE SEPARATE SCRIPTS FOR EACH SECTION

There are 3 page(s) in this question paper.

SECTION–A

There are **FOUR** questions in this section. Answer any **THREE**

All the symbols have their usual meanings

Assume reasonable values for missing data.

1. (a) Explain why DIODE, BJT and THYRISTORS cannot be operated in parallel to increase current carrying capacity. **(8)**

   (b) A three-phase diode rectifier is used to supply a DC motor (separately excited with a fixed 100% excitation) rated 10kW, 400V dc. If the motor is to run at rated voltage at rated load, determine **(22)**

   i) Line to Line Supply Voltage (RMS).

   ii) RMS value of the 5^{th} Harmonic current per phase.

2. (a) Explain why RMS output voltage of a single-phase controlled rectifier supplying a highly inductive load does not depend on the firing angle. **(12)**

   (b) A DC rechargeable battery is charged through a single phase full bridge controlled rectifier with an ac supply voltage of 24V (RMS) at 50Hz. The battery internal resistance is 20mΩ. Neglect voltage drop in rectifier switches. There is no other series elements in the charging path to limit the charging current. **(18)**

   i) Determine the average charging current if the firing angle is 30°.

   ii) Power factor of the battery charger.

3. (a) For a 3-phase Full-Bridge controlled rectifier, deduce an expression for the DC output voltage at a given firing angle of α considering a 3-phase balanced AC supply, **(18)**

b) What happens if a 3-phase Full-Brige controlled rectifier is fired at less than 30° from zero voltage crossing and why? **(12)**

4. (a) With a neat diagram and necessary waveforms explain the operation of a TRIAC-DIAC based fan regulator. **(12)**

(b) A single phase AC/AC converter is phase controlled to obtain an RMS voltage of 110V to a heater load from a 220V, 50Hz AC source. Determine the firing angle. **(18)**

SECTION–B

There are **FOUR** questions in this section. Answer any **THREE**

All the symbols have their usual meanings

Assume reasonable values for missing data.

5. (a) Explain SCR IV characteristics. Describe the operation of SCR using the two-transistor model. **(7+8)**

(b) Describe the operation of the following SCR commutation circuit in figure 5(b) where T_M is the main SCR and T_A is the Commutating SCR. **(15)**

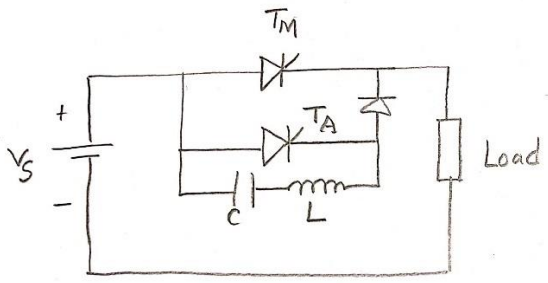

Fig. for question 5(b)

6. (a) Draw the circuit diagram and output waveform of a single-phase SCR current-source inverter. **(10)**

(b) Draw a 3-phase voltage source inverter and explain with necessary control and output waveforms the operation of the inverter in 180° conduction mode. Consider a 3-phase star-connected load. **(20)**

7. Draw the circuit diagram of a SEPIC dc-dc converter and explain its operation showing the direction of current flow when the switch is ON and when the switch is OFF. Derive the relation between the output voltage and the input voltage in continuous conduction mode. From the waveforms of current through both the inductors, find the minimum values of the inductors required to keep the operation in continuous Conduction Mode. **(10+10+10)**

8. (a) "For a non-ideal boost converter voltage gain as predicted by ideal voltage gain expression is not attainable" - explain with necessary derivations. **(15)**

(b) Draw the circuit diagram for a 5 Level inverter. Show the output waveform and explain its operation for any level of the output voltage. **(15)**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-II B.Sc. Engineering Examination 2018-19

Sub: **EEE 317** (Control Systems I)

Full Marks: 180 Time 2 Hours

The Figures in the margin indicate full marks

USE SEPARATE SCRIPTS FOR EACH SECTION

There are 5 page(s) in this question paper.

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**

All the symbols have their usual meanings. Assume reasonable values for missing data.

1. (a) A bridged-T network is often used in AC control systems as a filter network. (15)
The circuit of one bridged-T network is shown in Fig. 1(a). Determine the transfer function, $V_o(s)/V_{in}(s)$, of the network.

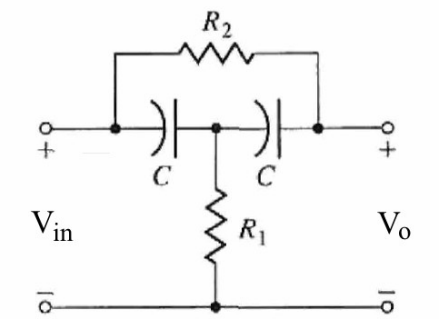

Fig. 1(a)

(b) The state-space model of a system is given by (15)

$$\dot{\mathbf{x}} = \begin{bmatrix} -4 & -1.5 \\ 4 & 0 \end{bmatrix}\mathbf{x} + \begin{bmatrix} 2 \\ 0 \end{bmatrix}u(t)$$

$$y = \begin{bmatrix} 1.5 & 0.625 \end{bmatrix}\mathbf{x}$$

Determine the transfer function of the system.

2. (a) Consider a critically damped system with transfer function: (15)

$$\frac{C(s)}{R(s)} = \frac{a^2}{(s+a)^2}$$

Determine the analytical expression of unit-step response of the system. Show that the settling time can be found by solving for T_s in $e^{-aT_s}(1+aT_s)=0.02$.

(b) Find the unity feedback system that is equivalent to the system shown in Fig. 2(b). (15)

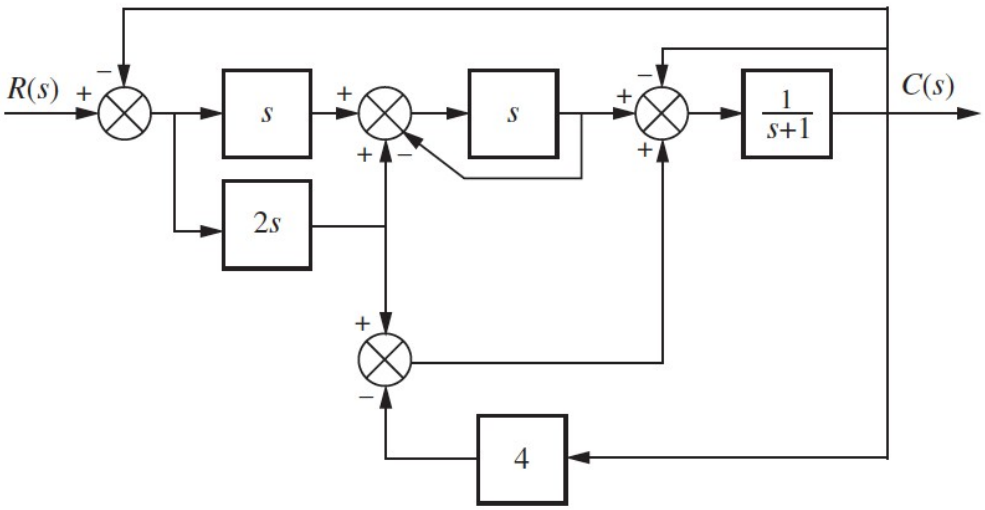

Fig. 2(b)

3. (a) For the system shown in Fig. 3(a), find ζ, ω_n, percent overshoot, peak time, rise time, and settling time. (15)

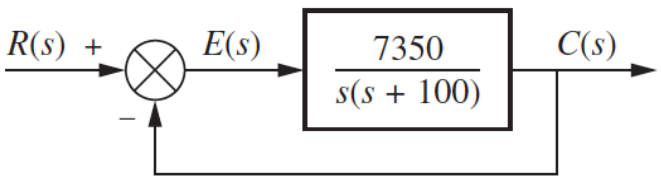

Fig 3(a)

(b) Consider the feedback system shown in Fig. 3(b). Sketch the root locus of the system. Is it possible to consider it a second-order system for very low gain? Explain your answer. (15)

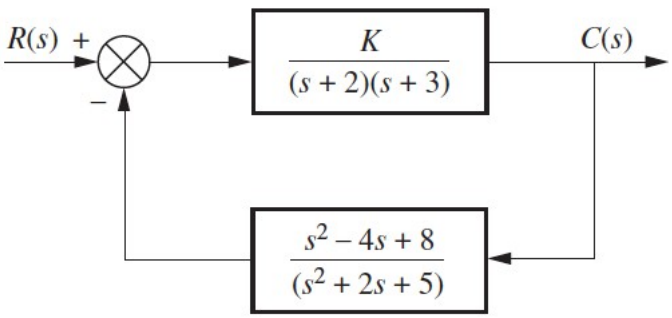

Fig. 3(b)

4 (a) Consider a unity feedback system having the following forward path transfer function: (15)

$$G(s) = \frac{K}{(s+5)^3}$$

Find the location of the dominant poles to yield a settling time of 1.2 second and an overshoot of 15%. If a compensator having a zero at -1 is used to achieve these conditions, find the location of the compensator pole.

(b) Consider a unity feedback system with the forward path transfer function: (15)

$$G(s) = \frac{K}{(s+1)(s+3)(s+10)}$$

The system operates with a damping ratio of 0.4. Design a PI controller to drive the step-response error to zero. How do you choose the location of compensator zero of the PI controller?

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**

All the symbols have their usual meanings. Assume reasonable values for missing data.

5. (a) Consider the following system transfer function T(s) (15)

$$T(s)=\frac{K}{s^4+8s^3+17s^2+10s+K}$$

.

Using the Routh-Hurwitz criterion (*i*) Find the range of K for stability and (*ii*) find the actual location of the closed-loop poles when the system is marginally stable.

(b) Find the total steady-state error due to a unit step input and a unit step disturbance in the system shown in the Fig. for Q. No. 5(b). (15)

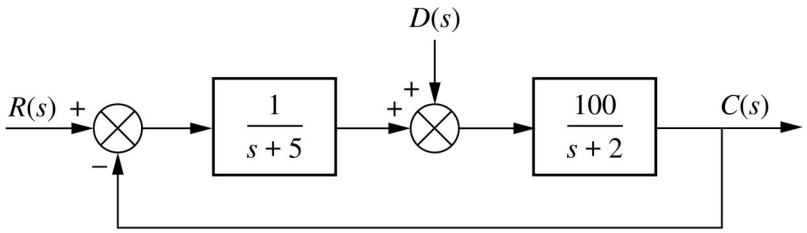

Fig. for Q. No. 5(b)

6. For the system shown in Fig. for Q. No. 6, using the frequency response method, design a Lead Compensator to yield a 20% overshoot (ξ = 0.456) and K_v = 40 with a peak time of 0.1 second. In this case, a phase margin of 48.1° is found for 20% overshoot. (30)

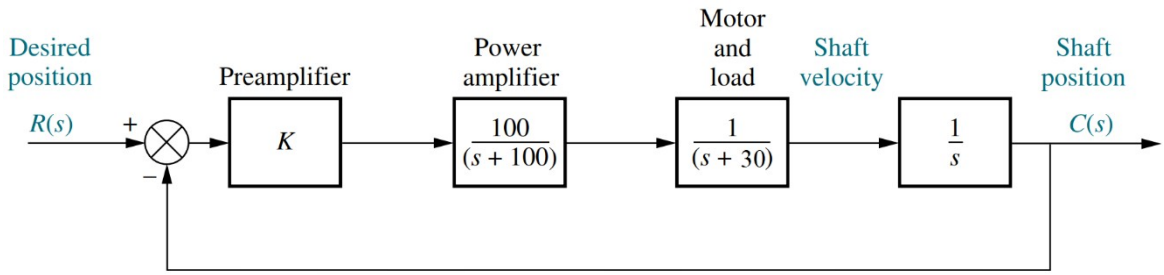

Fig. for Q. No. 6

7. Consider a unity negative feedback control system with (30)

$$G(s)=\frac{K(s+4)(s+6)}{(s-2)(s-5)}$$

.

Sketch the Nyquist diagram. In your sketch mark the critical point and explain the effect of variation of gain K on stability.

8 (a) Carefully observe the following Bode plots shown in Fig. for Q. No. 8(a) and find G(s), phase margin and gain margin. (15)

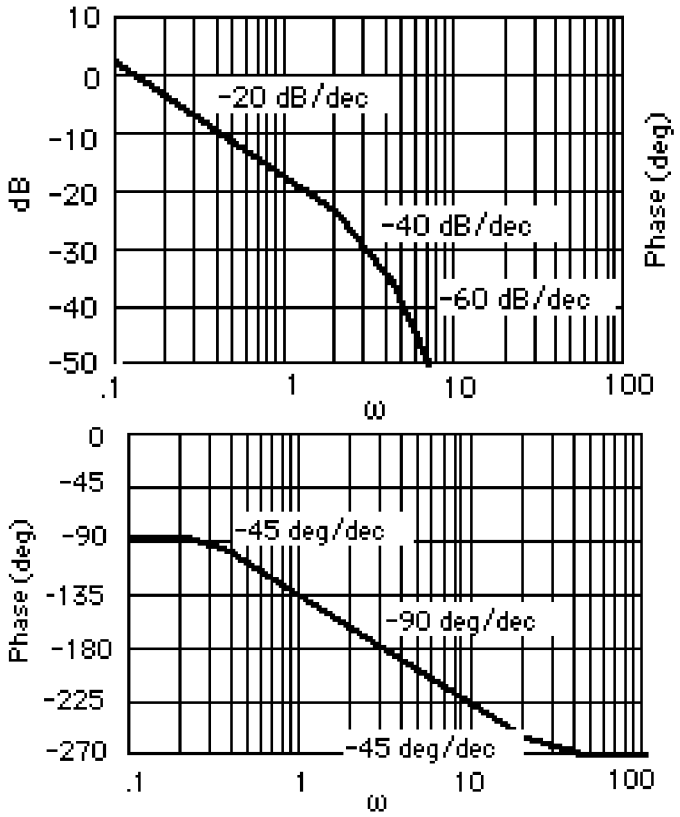

Fig. for Q. No. 8(a)

(b) For the feedback control system shown in the figure for Q. No. 8(b), find G(z) corresponding to G(s) where G(s) is the product of the zero-order hold and the plant. Using G(z), find the steady-state error for ramp input. (15)

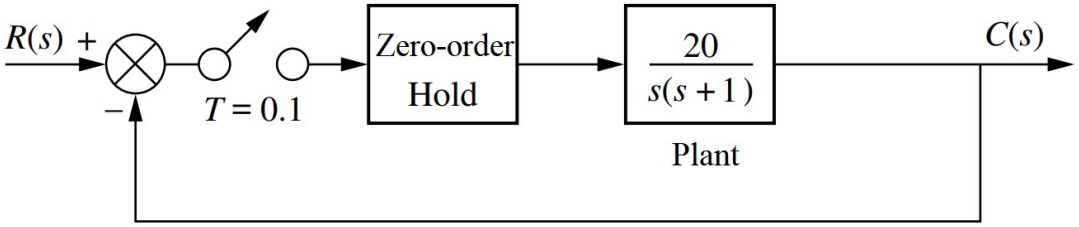

Fig. for Q. No. 8(b)

L-3/T-2/EEE Date: 20/01/2021

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations (January 2020 Term)

Sub: **IPE 493** (Industrial Management)

Full Marks: 180 Section Marks: 90 Time: 2 Hours (Sections A + B)

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks.

SECTION – A

There are **THREE** questions in this section. Answer any **TWO**.

1. (a) Lockheed Martin, the world's largest weapon and military vehicle manufacturer has just completed a feasibility study of what to do with the 16,000 tons of waste it produces every year. The company's CEO asked the board of directors, "Why pay another company to dig out our waste out of our own landfills and then pay another company to put our waste into another landfill? Why not simply burn the waste ourselves?" Thus, the company has decided to build a 10 million dollar incinerator to burn its waste as fuel, and thus saving $2.8 million per year in gasoline purchases. Engineers have estimated that after using the incinerator for four years, it can be sold to a local power company for $5 million. (25)

   (i) Draw the cash-flow diagram.

   (ii) Check for multiple IRR. What is the IRR of this proposed project?

   (iii) If the company's MARR is 15% per year, what is your recommendation about the acceptance of this project?

   According to the estimation of the engineers, the salvage value of the plant is $5 million after four years. What is the lowest acceptable salvage value to ensure the acceptability of the project?

   (b) Briefly describe the factors that influence the "value of money" with suitable real life examples. (10)

   (c) Briefly describe the relative importance of basic managerial skills for different levels of managers. (10)

2. (a) Kiestler GmBH is a local bicycle manufacturer based on Dusseldorf, Germany. They want to develop a precedence diagram for the bicycle assembly tasks. The time requirement of these tasks and their sequence of completion are given in the table below. There are 480 productive minutes of work available per day in Dusseldorf, Germany. Furthermore, the company is required to produce 40 bicycles per working day to satisfy the customer demand. (25)

Task	Assembly Time (minutes)	Leading / Preceding Task
A	10	---
B	11	A
C	5	B
D	4	B
E	12	A
F	3	C, D
G	7	F
H	11	E
I	3	G, H

Required:

(i) Precedence diagram

(ii) Cycle time

(iii) Grouping of the tasks into workstations

(iv) Line efficiency

(b) State and explain the different roles played by the managers according to Henry Mintzberg. (10)

(c) Differentiate between the differential and multiple piece rate incentive plans. Provide suitable examples and write down their relative advantages and disadvantages. (10)

3. (a) What is the span of management control? How is it important in the context of the hierarchy of an organization? Describe the factors that influence the span of control. (15)

(b) Differentiate between: (15)

(i) Product and process layout

(ii) Nominal and effective interest rate

(c) What is the present equivalent of $18,000 to be received in 15 years when the interest rate is 7% per year compounded semiannually? What will be the present equivalent if the compounding is done continuously? (8)

(d) Explain the factors that should be taken into consideration when deciding the right location for a manufacturing facility. Which assumptions do you make when solving continuous location problems? (7)

SECTION – B

There are **THREE** questions in this section. Answer any **TWO**.

4. (a) What is the 'Pareto Rule'? How does this rule help to find out 'Vital Few' and 'Trivial Many' causes? Explain with example. (10)

(b) According to Juran, 100% good quality level may not be of interest to the company in terms of cost. If this is true, then the zero-defect concept is not economically beneficial. Do you agree? Justify with schematic diagrams. (15)

(c) For the following order table, decide the sequence of jobs to be processed based on Johnson's Rule. Also, show the jobs' duration in a time frame. (20)

	Processing Time (days)		
Job	Station 1	Station 2	Station 3
A	7	2	3
B	6	4	2
C	8	5	4
D	9	2	5
E	10	3	7

5. (a) List at least 5 (five) groups/individuals who can conduct performance appraisals. (5)

(b) A recent study showed that CEOs of successful companies have hard-nosed personal traits, such as persistence, efficiency, attention to detail, and a tendency to set high standards, rather than softer strength, such as teamwork, enthusiasm, and flexibility. How do you explain this in light of the leadership theories? (15)

(c) Hewlett-Packard (HP) builds three computer printer models: Inkjet, Laser, and Color Laser. Information for these three products is given in the following table. How do you answer the following questions? Assume any value for the Fixed Cost. (25)

	Inkjet	Laser	Color Laser	Total
Selling price per unit ($)	250	400	1600	
Variable cost per unit ($)	100	150	800	
Sales mix (%)	60	30	10	100

(i) How many printers in total must be sold to break even?

(ii) How many units of each printer model must be sold to break even?

(iii) How many printers in total must be sold to earn an annual profit of $1,000,000?

(iv) How many units of each printer must be sold to earn an annual profit of $1,000,000?

6. (a) A company projects its total sales and profits through plans for existing businesses. The projected sales are less than what management desires. What are the growth opportunities you will suggest this company to explore in order to minimize the gap between projected sales and desired sales? Explain with suitable example. (10)

(b) How different phases of the Technology Life Cycle (TCL) affect strategic analysis and investment planning? Explain with suitable example. (15)

(c) A normally distributed quality characteristic is controlled by $\bar{x}$ and R charts having the following parameters ($n = 4$, both charts are in control): (20)

R Chart	$\bar{x}$ Chart
UCL = 18.795	UCL = 626
Center Line = 8.236	Center Line = 620
LCL = 0	LCL = 614

(i) What is the estimated standard deviation of the quality characteristic x?

(ii) If specifications are 610 ± 15, comment on process capability by observing the graphical distribution and mathematical measures.

Table B. Factors used in 3σ Quality Control Charts.

Sample size n	$\bar{X}$ charts			S charts					R charts					
	Factors for control limits			Factors for central line	Factors for control limits				Factors for central line	Factors for control limits				
	A	A_2	A_3	c_4	B_3	B_4	B_5	B_6	d_2	d_3	D_1	D_2	D_3	D_4
2	2.121	1.880	2.659	0.7979	0	3.267	0	2.606	1.128	0.853	0	3.686	0	3.267
3	1.732	1.023	1.954	0.8862	0	2.568	0	2.276	1.693	0.888	0	4.358	0	2.574
4	1.500	0.729	1.628	0.9213	0	2.266	0	2.088	2.059	0.880	0	4.698	0	2.282
5	1.342	0.577	1.427	0.9400	0	2.089	0	1.964	2.326	0.864	0	4.918	0	2.114
6	1.225	0.483	1.287	0.9515	0.030	1.970	0.029	1.874	2.534	0.848	0	5.078	0	2.004
7	1.134	0.419	1.182	0.9594	0.118	1.882	0.113	1.806	2.704	0.833	0.204	5.204	0.076	1.924
8	1.061	0.373	1.099	0.9650	0.185	1.815	0.179	1.751	2.847	0.820	0.388	5.306	0.136	1.864
9	1.000	0.337	1.032	0.9693	0.239	1.761	0.232	1.707	2.970	0.808	0.547	5.393	0.184	1.816
10	0.949	0.308	0.975	0.9727	0.284	1.716	0.276	1.669	3.078	0.797	0.687	5.469	0.223	1.777
11	0.905	0.285	0.927	0.9754	0.321	1.679	0.313	1.637	3.173	0.787	0.811	5.535	0.256	1.744
12	0.866	0.266	0.886	0.9776	0.354	1.646	0.346	1.610	3.258	0.778	0.922	5.594	0.283	1.717
13	0.832	0.249	0.850	0.9794	0.382	1.618	0.374	1.585	3.336	0.770	1.025	5.647	0.307	1.693
14	0.802	0.235	0.817	0.9810	0.406	1.594	0.399	1.563	3.407	0.763	1.118	5.696	0.328	1.672
15	0.775	0.223	0.789	0.9823	0.428	1.572	0.421	1.544	3.472	0.756	1.203	5.741	0.347	1.653
16	0.750	0.212	0.763	0.9835	0.448	1.552	0.440	1.526	3.532	0.750	1.282	5.782	0.363	1.637
17	0.728	0.203	0.739	0.9845	0.466	1.534	0.458	1.511	3.588	0.744	1.356	5.820	0.378	1.622
18	0.707	0.194	0.718	0.9854	0.482	1.518	0.475	1.496	3.640	0.739	1.424	5.856	0.391	1.608
19	0.688	0.187	0.698	0.9862	0.497	1.503	0.490	1.483	3.689	0.734	1.487	5.891	0.403	1.597
20	0.671	0.180	0.680	0.9869	0.510	1.490	0.504	1.470	3.735	0.729	1.549	5.921	0.415	1.585
21	0.655	0.173	0.663	0.9876	0.523	1.477	0.516	1.459	3.778	0.724	1.605	5.951	0.425	1.575
22	0.640	0.167	0.647	0.9882	0.534	1.466	0.528	1.448	3.819	0.720	1.659	5.979	0.434	1.566
23	0.626	0.162	0.633	0.9887	0.545	1.455	0.539	1.438	3.858	0.716	1.710	6.006	0.443	1.557
24	0.612	0.157	0.619	0.9892	0.555	1.445	0.549	1.429	3.895	0.712	1.759	6.031	0.451	1.548
25	0.600	0.153	0.606	0.9896	0.565	1.435	0.559	1.420	3.931	0.708	1.806	6.056	0.459	1.541