Surface Potential Based Analytical Modeling of Electrostatic and Transport Characteristics of GaN Junctionless Nanowire MOSFET

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MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by
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To my beloved parents

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Abstract

Since tradition planar Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) has reached their scaling limit, further miniaturization, without degradation of device performance, has become very difficult due to sever short channel effect and high complexity of fabrication process resulted from ultra sharp source and drain junction requirement. Junctionless (JL) nanowire (NW) MOSFETs are considered promising for the sub-20 nm era due to their constant doping profile from source to drain. They provide a great scalability without the need for rigorously controlled doping and activation techniques as well as reduced short channel effects (SCEs) compared to the conventional MOSFETs. With its superior electronic properties compared to Si, GaN has shown its potential as a viable alternative of Si as a channel material in ultra scaled devices. Though a number of experimental studies for GaN JL NW MOSFET have been carried out over the past few years, rigorous and accurate analytical study of this device is yet to be reported. This work presents a physically based comprehensive analytical investigation of electrostatic and transport phenomena of GaN JL NW MOSFET. The evolution of the proposed model involves the solution of quasi 2-D Poisson's equation with appropriate boundary condition to obtain effective surface potential as a function of gate voltage. The mobile carrier density derived from the surface potential is used to formulate the core transport model as well as to analyze the electrostatic characteristics for various physical device parameters. Short channel effects and certain non-ideal effects including velocity saturation, mobility degradation, channel length modulation have been incorporated in the core transport model. The impact of physical device parameters including channel length, NW radius and oxide thickness on the performance metrics of the device such as subthreshold slope (SS), drain induced barrier lowering (DIBL) and threshold voltage has been rigorously investigated. Upon analyzing the transport properties of the device, steep SS of 68 mV/dec, DIBL of 27 mV/V and switching figure of merit $Q(= g_m/SS)$ of 0.16 ($\mu S/\mu m/(mV/dec)$ have been attained which makes the GaN NW JL MOSFET a promising candidate for emerging low power application. The results of this work exhibit very good agreement with 3D TCAD simulation and reported experimental results and thereby enhancing the reliability of the proposed model.

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Chapter 1

Introduction

This chapter elaborates on the fundamental concepts pertaining to technology scaling along with the origin and impact of non ideal effects in nanoscale Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). It also presents a brief overview of Junctionless (JL) Field Effect Transistors followed by an rigorous study of existing literature. In addition, it covers the objectives and outline of the thesis.

1.1 Current Trend of CMOS Scaling

Over the past few decades, the computing and communication technologies have played as driving forces in the world economy. About more than 10% of the world economy is built on electronics market and this parcentage is continuously growing. This revolution in semiconductor technology commenced from the invention of the first solid-state device, a bipolar point contact transistor on Germaniun (Ge) substrate, invented by Bardeen, Brattain, and Shockly at Bell labs in 1947. Complementary metal-oxide-semiconductor (CMOS) field-effect-transistor has almost replaced bipolar transistor because the former offers lower power and technology advantages. The outstanding performance and scalability of CMOS have encouraged Intel's co-founder Gordon Moore to make a famous prediction about device scaling. In 1965, Gordon Moore predicted that the number of components per integrated chip will be doubled every year [1]. He revised his prediction in 1975 stating that the doubling will happen approximately in every two years [2]. This prediction, known as "moore's Law", has been acting as a guideline for the semiconductor industry to set their goals and made them push harder

to break the frontier of technology through constant innovation.

The minimum critical feature size (physical gate length) of MOSFET has been suc-

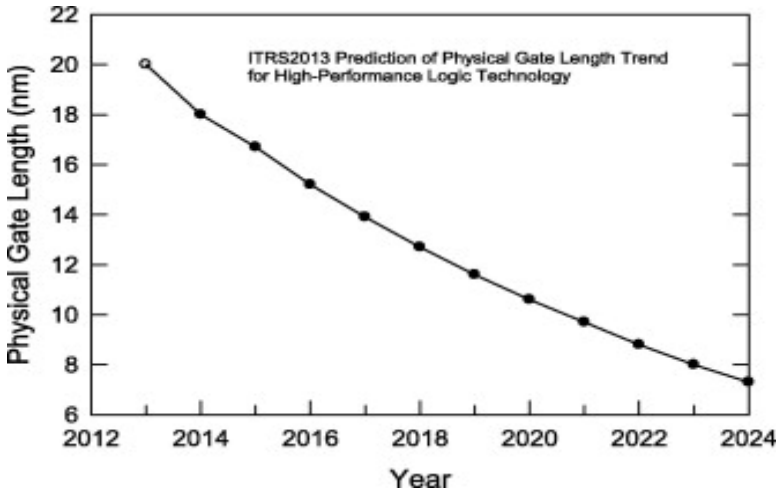

Figure 1.1: *Scaling trend of high performance logic technologies with year [3].*

cessfully reduced by more than two orders of magnitude according to Moore's law until now and International Technology Roadmap of Semiconductors 2012 (ITRS) recently foresaw that the minimum feature size will still decrease from 22 nm in 2011 to around 7 nm in 2024 as displayed in figure 1.1.

1.2 CMOS Scaling Challenges

As the MOSFET dimensions are decreasing, it is difficult to keep long channel behavior due to the unwanted side effects [4]. With the continuous reduction of channel length in deep sub-micron region, some unavoidable effects namely, short channel effects, channel length modulation, drain induced barrier lowering, mobility degradation with vertical field, velocity saturation etc. come into play. We will discuss them qualitatively as below. Researchers have tried to reduce them through different techniques like gate engineering, channel engineering, implementing different device architecture with different working physics etc. Although they are able to reduce it to some extent, it is extremely difficult to nullify this effects in ultra short channel lengths with a single gate control on the silicon region.

1.2.1 Short Channel Effect (SCE)

The short channel effect (SCE) is the decrease of threshold voltage of a MOSFET as the channel length is reduced. It is prominent when drain bias is equal to the power supply voltage. the important difference of long and short channel MOSFET is that, in a long channel MOSFET, the electrostatics of the channel region is controlled by the gate; however, for short channel MOSFET, besides gate, source and drain regions also try to control the channel electrostatics. Therefore, it is now a 2D problem instead of 1D that is valid for a long channel MOSFET. The charge sharing from source and drain regions decreases the threshold voltage of the device [5, 6].

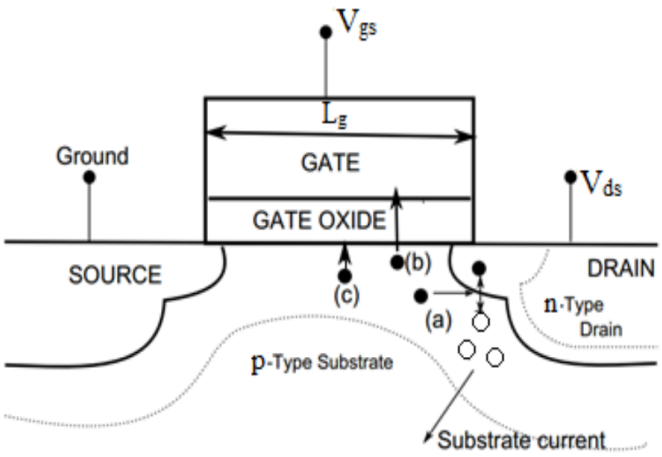

Figure 1.2: *Schematic illustration of hot carrier effects in MOSFETs.*

1.2.2 Hot Carrier Effects

After fabricating a certain device there should not be a drift in performance of the device over time. But hot carrier effect leads to the drift over certain period of operation. This is more dominant in short channel devices where the electric field is higher. The three kind of possible hot carrier injection mechanisms are illustrated in figure 1.2 as mentioned below.

- Carriers generated due to impact ionization on the drain side can multiply and lead to a heavy substrate current.
- The carriers having energy higher than the silicon/gate dielectric conduction band offset can lead to a conduction current to the gate.

- The sufficient high energy electrons can damage the silicon/gate dielectric interface leading to degradation in important device parameters like drain current, threshold voltage etc. [7, 8]

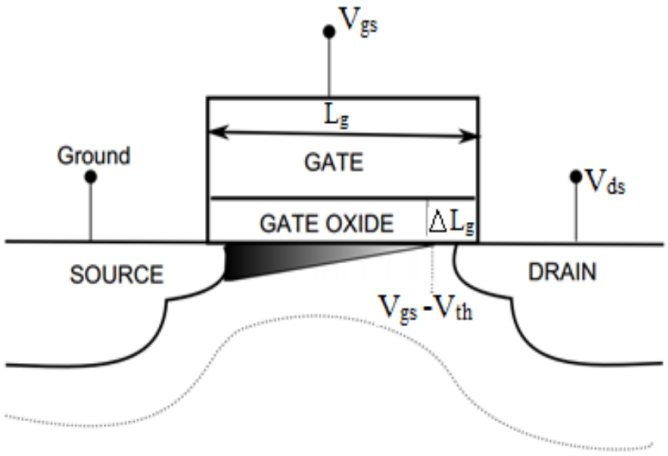

Figure 1.3: *Schematic illustration of channel length modulation effect.*

1.2.3 Channel Length Modulation (CLM)

When drain to source voltage, $V_{DS} > V_{GS} - V_T$, I_D is relatively constant and we say the device operates in saturation region. The local density of inversion layer charge ($Q_d(x)$) is proportional to $V_{GS} - V(x) - V_T$, where $V(x)$ is the channel potential at x (x is along the channel direction). Thus, if $V(x)$ approaches $V_{GS} - V_T$, then $Q_d(x)$ drops to zero. This implies that if V_{DS} is slightly greater than $V_{GS} - V_T$, the inversion layer stops at $x \leq L$ and we say the channel is "pinched off". If V_{DS} is increased further, the point at which Q_d is equal to zero approaches towards source. Therefore, at some point along the channel, the local potential difference between the gate and the oxide-silicon interface is not sufficient to support an inverted channel (figure 1.3). That is, the actual length of the inverted channel gradually decreases as the potential difference between gate and drain increases. This effect is known as channel length modulation. This phenomena results in a nonzero slope in the saturation region of I_D/V_{DS} characteristics [9, 10, 11]

1.2.4 Drain Induced Barrier Lowering (DIBL)

This phenomena occurs when gate voltage is less than the threshold voltage of the device. When drain and source voltages are equal, the depletion region beneath the

source and drain are equal as they are equally doped. Now, with increase in V_{DS}, the depletion region below the drain region is more to compensate with the extra potential connected to drain. For short channel length devices, the electrostatics is not only controlled by the gate but also by the source and drain region. The charges in the drain region contribute to the depletion potential and the barrier between source and channel region decreases. As a result, threshold voltage decreases. This phenomenon is called drain induced barrier lowering. It is determined as the threshold voltage different when V_{DS} changes from 50 mV to 1 V [12, 13].

1.2.5 Gate Oxide Leakage

Silicon dioxide (SiO_2) is a good insulator to be used in the MOS structure. But when gate oxide thickness is reduced to less than $2 - 3nm$, tunneling probability increases and results in an increase of oxide leakage current [14, 15]. High-κ dielectric is used to solve this problem to some extent, as high-κ dielectric can provide a similar gate electric field even with a physically thick gate dielectric. This can reduce the direct tunneling leakage.

1.2.6 Velocity Saturation

The mobility of the carriers depend on the lateral electric field as well. It begins to drop as the field reaches a value of 1 $v/\mu m$. Thus, the carrier velocity, $v(= \mu E)$ reaches a saturated value (10^7 cm/s) for sufficiently high fields along the channel at some point. The parameters, μ and E are the carrier mobility and low electric field respectively. The current thus produced is linearly proportional to overdrive voltage and does not depend on length [16, 17].

1.2.7 Gate Induced Drain Leakage (GIDL)

With a high drain bias and a low gate voltage, the electric field in the gate/drain overlap region is high. Therefore, if the band bending of the gate/drain overlap region at the oxide interface is greater than or equal to the energy band gap E_g of the drain material, band to band tunneling will take place. The electron in the valance band of the drain will tunnel through the thinned band gap into the conduction band and they will be

collected at the drain contact to be a part of the drain current, whereas the remaining holes will be collected at the substrate contact and will contribute to substrate leakage. This phenomenon, first elucidated and modeled in 1987 [18], discerns a potential major contributor to the off-state leakage current and is called the gate induced drain leakage (GIDL) current [19].

1.2.8 Impact Ionization

In the transistor on state, because of the high electric field near the drain end of the channel, carriers in this region can gain enough kinetic energy to ionize the lattice atoms when they collide. This collision frees an electron from the valance-band and leaves a hole behind. The generated hole will drift to the substrate and it will increase the substrate leakage. The released high-energy electron (hot carrier) is collected by the drain and it will be a part of the drain current [20, 21].

1.2.9 Surface Scattering

As the channel length becomes smaller, due to lateral extension of the depletion layer in to the channel region, the longitudinal electric field increases and the surface mobility becomes field-dependent. In the saturated or strong inversion region, the carriers are confined within the narrow inversion layer in a MOSFET. The carriers experience collision suffered by the electrons that are accelerated toward the interface and drain by the vertical electric field. This is called surface scattering which causes reduction of the mobility and this in turn affects both the drain current and transconductance [22, 23].

1.3 Alternative Solution to Continue CMOS Scaling

The increasing difficulties in Si CMOS scaling has created the need of investigation of alternative channel materials and device architectures. Many improvements , in terms of including channel doping profile, gate stack, source/drain design, mechanical strain engineering, three-dimensional architectures with multi-gates and alternate

channel material have been proposed to overcome the scaling challenges of Si CMOS and enhance device performance.

1.3.1 Alternative Device Architecture

In the 90's, retrograde channel doping profiles in the channel allowed punch-through and other SCEs to be better controlled. It also reduced the junction capacitance and threshold voltage sensitivity to substrate bias.

MOS transistor require high gate capacitance to attract charge to the channel. This results into very thin SiO_2 gate dielectric. As a gate leakage current increases unacceptably with decrease of gate oxide thickness in each technology node. To circumvent this issue, high-κ gate dielectric, such as Al_2O_3, HfO_2, ZrO_2, Y_2O_3, La_2O_3, Ta_2O_5 and TiO_2 have been introduced, since they ensure same capacitance with a thicker physical thickness compared to SiO_2.

The Lightly Doped Drain (LDD) was introduced to enhance performance of ultra-scaled device. In the LDD structure, narrow, self-aligned, n^- regions are introduced between the channel and the n^+ source-drain diffusion. This structure increase breakdown voltage and reduces impact ionization (and thus hot-electron emission) by spreading the high electric field at the drain pinch-off region into the n^- region. This allows either an increase in power supply voltage or a reduction in channel length at a given voltage to achieve a performance enhancement [24, 25].

Silicon on insulator (SOI) based devices have less difficulty in controlling SCEs compared to planar bulk Complementary MOS (CMOS) devices. A thin channel body the SOI substrate can successfully remove most problems regarding current leakage through the substrate and punch through effect [26, 27]. It also allows the channel to be lightly doped, giving rise to higher speed. However, there are disadvantages of SOI such as expensive wafer cost, the kink effect due to floating body effect and worse heat conduction.

Strain engineering can give the improvement of device mobility, since the Si crystal

lattice constant altered by external applied stress causes the changing of the band structure, the density of states and the effective mass of the carriers. For instance, embedded SiGe source/drain produces a compressive stress in the channel due to its larger lattice constant than Si. This improves holes mobility in pMOS devices. SiC source/drain structures can also lead to the electron mobility.

As the channel length of tradition bulk MOSFET became smaller in each technology node, the short channel effect induced device degradation became severe. To overcome this problem multiple gate device architecture was introduced. The most simple structure among different multi-gate architectures is the double gate (DG) MOSFET which was first reported in 1984 [28]. Compare to bulk single gate MOSFET, DG MOSFET has two insulated gates known as upper gate and lower gate. Due to presence of two gate, DG MOSFET ensures better electrostatic control over the channel and showcases stronger immunity to short channel related issues compared to single gate device [29]. Three dimensional MOSFET structures was considered several decades ago to be very important for the achievement of superior performance in ultra scaled . But the problems arisen due to floating substrate impeded the integration of 3-D devices in practical circuit. To eliminate the floating substrate issue, a novel structure called fully depleted lean-channel transistor (DELTA) was proposed [30]. The key feature of this device structure include induction of ultra thin SOI effects, formation of bulk single crystal SOI so that neither re-crystallization technology nor SIMOX was required, and channel formation on a vertical surface. This revolutionary device structure paved the way to the proposition of novel self-aligned double-gate MOSFET, popularly known as FinFET [31]. FinFET has not only suppressed the short channel effect, but also solved the complexity of DG MOSFET fabrication process due to incompatibility of gate-channel-gate structure with Si-planar technology.

Among all multigate device structure the gate all around (GAA) MOSFET has been the most attractive since it guarantees the best electrostatic control. The first GAA device, published in 1990, was in reality a double-gate transistor although the gate electrode did wrap around all sides of the channel region [32]. Nowadays the term "GAA" is preferentially used to describe a nanowire-like MOSFET where the gate is

wrapped around the channel region. Using such gate architectures, it is even possible to fabricate MOSFET devices without introducing pn junctions for the source and drain [33] .Such "junctionless"(JL) multigate transistors have a great potential for greatly simplifying the MOSFET fabrication process at the nanometer length scale. It is also possible to insert electron trap layers or nanocrystals in the gate dielectric to create nanowire flash memory transistors [34].

1.3.2 Alternative Channel Material

New channel materials like germanium (Ge) [35] and III-V compound semiconductor [36] have introduced an era of ultra-low-power and high-speed devices. Recently, two dimensional (2D) layered materials (bilayer graphene, bilayer MoS_2) have supported field-controlled bandgap tuning [37]. It gives a new platform to design new electronic and optoelectronic devices. However, a high quality gate dielectric is required to apply large vertical electric fields in such devices. Such attempts for high mobility materials are facing fabrication challenges, as these materials can support either n type (III-V compound semiconductor) or p type (Ge) devices but not both, which are required for CMOS circuit designs. The quantum confinement effects, which are dependent on material thickness scaling can be used as a powerful techniques to optimize the material properties, because materials having different thicknesses can be viewed as different materials with entirely different properties. This sets a new platform for electronics and optoelectronic applications.

1.4 Junctionless Transistor

Since its inception, Junctionless(JL) MOSFET, also called gate resistor has emerged as a strong candidate for future technology node. The device has showcased significant potential in the Nanoscale transistor industry due to its reduced short channel effects and fabrication constraints. Many research groups are focusing on this device as it might become a breakthrough to the frontiers of nanoscale MOSFETs.

1.4.1 Basic Device Structure

The nanowire (NW) JL MOSFET device structure contains two major regions : The channel and the gate.

The primary element of the JL device is the channel. It indicates the major path for current flow in the transistor. It is usually fabricated from lightly doped p or n type semiconductor material. No distinct p-n junction is present in the channel region in the path of current flow. The device properties change polarity along with dopant material. That is, the applied voltage polarity for activation and direction of current flow switches side along with dopant polarity. For simplicity, the n-channel JL FET can be compared with the NMOS structure, while p-channel JL FET is to be compared against PMOS.

The channel consists of two terminals along two distinct edges: the drain terminal and the source terminal. Like normal FET structures, the terminals are completely identical and interchangeable, even during device operations. In case of n-channel JL MOSFET, the terminal with higher voltage is known as the drain terminal and the lower is referred to the source. With switching of terminal voltage during operation, the terminal polarity switches sides. However, in case of p-channel device, the lower voltage terminal is referred to the drain and the higher one is source, to comply with the PMOS notations. As a result, channel current in n-channel device flows from drain to source, and hence it is termed as the Drain current.

The channel can be made using any existing semiconductor device suitable for fabrication. Even recently, a novel JL transistor structure with polysilicon nanowire channel is proposed by Su et al. [38]. However, due to the unique device structure and operating principles, the effective mobility of JL device is lowered compared to inversion mode device. As a result, high mobility semiconductor is preferred as channel material for JL MOSFET. However, considering the cost and feasibility, initial investigation of the device has been constrained within Silicon based channel structure. Recently, III-V materials, especially GaN has shown great potential to be an alternative channel material for JL NW MOSFET.

The second significant device element is the Gate. It is often referred to the Gate

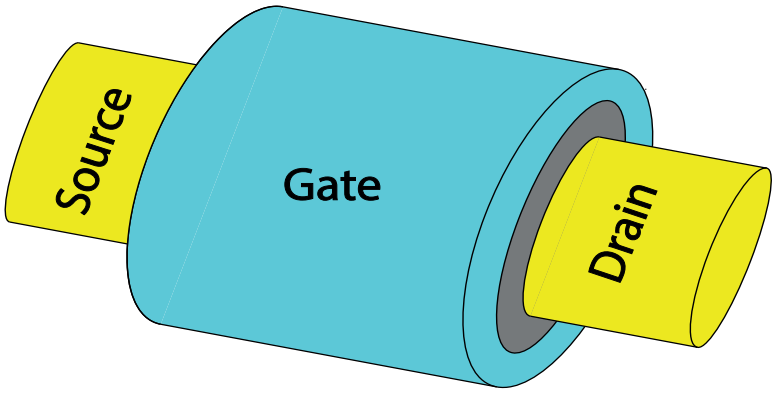

Figure 1.4: *Three Dimensional Schematic View of JL NW MOSFET*

terminal of the device, which combined with the Drain and Source terminals, complete the three-terminal structure of the transistor. The gate of JL MOSFET performs similar function as the Gate terminal of tradition inversion mode FET. That is, the gate acts as the switching regulator of the transistor. When a significant voltage is applied at the gate terminal, the device is turned on, and constant current flows through the channel. The limiting value is generally termed as the threshold voltage of the device. In addition, for JL MOSFET, flat band voltage acts as the Corner Voltage of the device.

The JL MOSFET is a basically a multi-gate device, which means, by definition, there is more than one gate structures present in the device. There are three major configuration of JL MOSFET can be found in the literature:

- The gate-all-around (GAA) structure/ The Θ structure
- The Triple-Gate (TG) structure /The Π structure
- The Double-Gate (DG) structure / The Ξ structure

The GAA structure encloses the device in all four directions. The TG structure basically has 3 directional encapsulations, similar to a doorway arch, as the channel passes through the door. The DG structure, on the other hand, encloses the channel from only two directions, opposite to each other. Hence, for all acts and purposes, the gates and the channel can be viewed as a sandwich structure. In a Double-Gate structure,

the channel is covered from two opposite directions with the gate structures. However, although the gate structures are physically isolated, they are electrically coupled together. That is, both gate structures are connected to the same voltage source, so that both ends of the channel are induced with the same gate voltage. The gates are placed along an axis perpendicular to current flow i.e. if current flow is considered to be along Z axis, the gates are placed along X axis. With variation of gate voltage, the channel surface charge density along YZ plane varies, turning the device ON or OFF or keeping in between. However, more complex variation occurs for TG or GAA structure.

The multigate device structure possesses several improvements over tradition single gate structure. Multi-gate device structure can be used to improve gate control over the channel and hence alleviate the short channel effect. The GAA structure provide the best utilization of the advantages of multigate structure due to the complete encapsulation of the channel region.

To fabricate the gate, various materials are available. Classic metal gate structure is still feasible, while current trend of polysilicon gates are well suited in fabrication perspective.

An insulator layer distinguishes the channel region from the gate material in JL MOSFET, just like in tradition FET. To ensure proper device operation, the insulator should have low conductivity. In addition, to reduce lattice mismatch during fabrication, the lattice constant of insulator and channel material should be closely matched. Traditionally, the Oxide and Nitride layer of the native channel semiconductor is used as the insulator material.

Figure 1.4 portrays a simplified 3D model of the NW JL MOSFET under discussion. As it can be observed in the figure,the gate encloses the device, while the channel has source and drain terminals. The oxide layer separate the channel from the gates, preventing gate current flow.

The effective device model can be better understood for the 2D cross section of

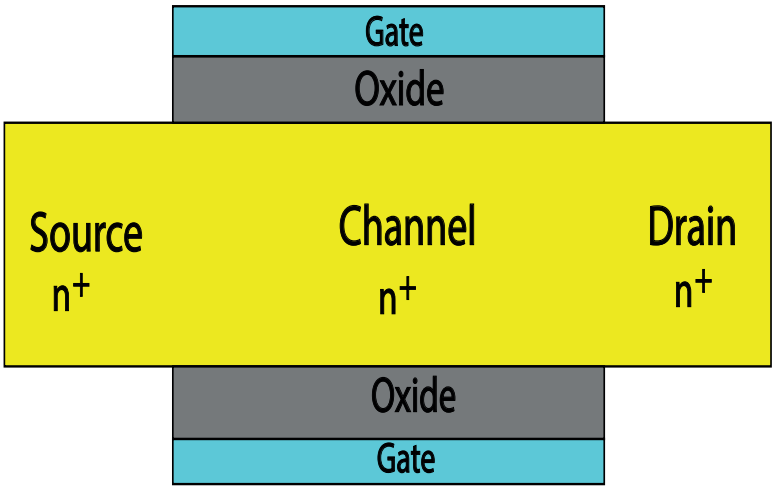

Figure 1.5: *2D Schematic Cutout along Channel of a NW JL MOSFET*

the device exhibited in figure 1.5. This figure highlights the respective position of the gate terminal, oxide layer and the channel in the NW JL MOSFET structure. Figure 1.6 displays the cross sectional view across the channel of the nanowire.

The device structure can be scaled up or down along a very extensive range. The reduction in the doping gradient maintenance constraints allows it to construct far smaller devices possible compared to current FET fabrication technology.

The standard doping density of n-channel region of the JL MOSFET device can

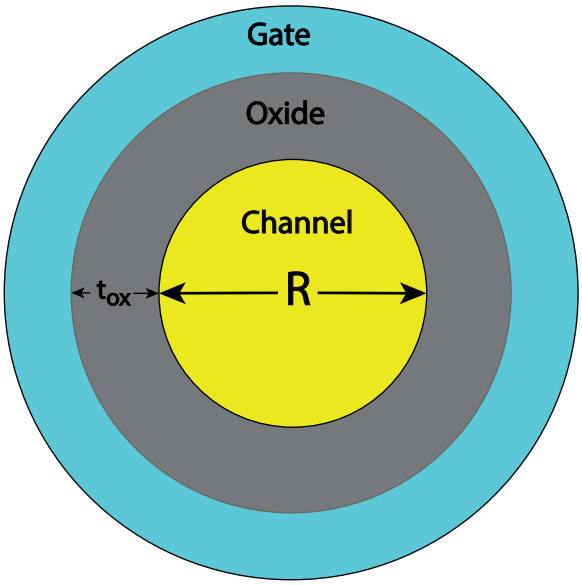

Figure 1.6: *Radial Cross Section of a NW JL MOSFET*

be varied as well. Usually, as no high doped diffusion area has to be fabricated, the

usual doping density of JL FET is higher compared to standard FETs. The usual studies contain the doping density in the range of $2\times10^{19} atoms/cm^3$ to $5\times10^{19} atoms/cm^3$ [33].

1.4.2 Operating Principal of the Device

The device operation of NW JL MOSFET significantly varies from the tradition inversion type FET devices. In the inversion mode device, gate voltage is used to attract or repulse carriers in order to construct an inversion layer near the oxide/semiconductor interface to facilitate current flow through the channel. On the contrary, in the JL device, the gate voltage is used to free already existing channel from the chokehold of junction fermi level mismatch.

The operation of JL device can be well comprehended by analyzing its energy band diagram for different gate voltage conditions. It is already known from the fundamental knowledge of electronics, that during formation of junction, the different materials present in the structure attempt to match their Electrochemical Potentials, also referred to as Fermi Levels along the same energy level. In case of a p-n junction, as seen in traditional electronic devices, the p-type material is doped using Group-III materials with electron deficiency. Hence the fermi level exists closer to the valance band. On the contrary, due to being doped with Group-V materials, the n-type material has its fermi level near the conduction band. Now, during the formation of junction, the levels tend to match along the junction region, resulting in a bending of the conduction band, valance band and intrinsic Fermi level of the materials along the area. The region of band bending, i.e. the depletion or space-charge region, is less n-type inside the n-region due to presence of static positive charge within it. The opposite is true for the p-region.

Now in the case of Gate-Oxide-Semiconductor combination, as observed for both inversion mode and JL FET, the gate is either metal or heavily doped polysilicon. Although no direct junction is formed between gate and channel, the excess charges of the gate and channel regions attract each other through the oxide layer, often with the assistance of trapped oxide charges present in the oxide, but no current can flow. Hence, energy band bending can be observed in the conduction and valance band of the chan-

nel region as space charge region is formed.

Figure 1.7 presents the energy band structure that would have been present in the de-

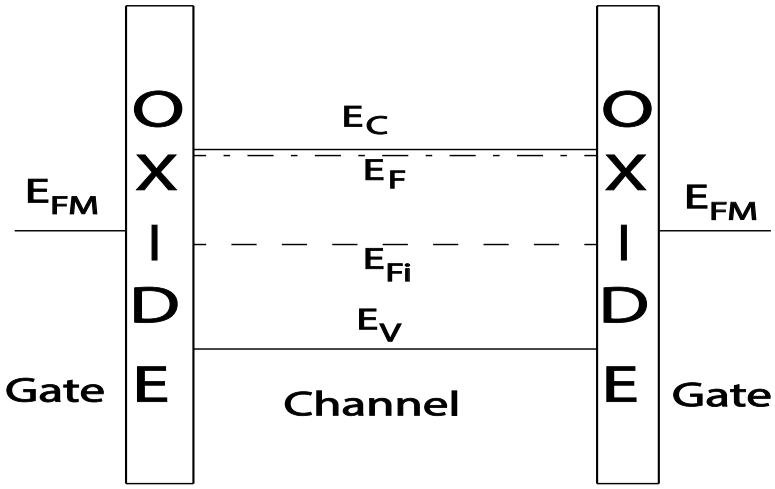

Figure 1.7: *Energy Band Diagram of n-channel NW JL MOSFET before Junction Formation*

vice in absence of electrochemical equilibrium. The n-channel, considered here, has its fermi level near the conduction band, as a large energy gap exists between the channel Fermi level and the gate work function.

In reality, with the formation of contact, the Fermi levels would align, and space charge region would be produced. The trapped charge in oxide layer would also create bending in the conduction and valance band of the oxide layer. Figure 1.8 portrays the energy band diagram that would be present under the assumption of zero gate voltage.

As it can be observed from the figure, the conduction band and valance band bending occur by the amount of ΔE along the surface of the channel-oxide interface. So, potential varies from ϕ_c to ϕ_s from the core of the channel to the surface regions. Hence, a space charge region exists almost throughout the channel cross-section. This is known as the Full Depletion mode of the device operation [39].

Now, with application of gate voltage, the energy band profile varies accordingly. The electrochemical potential decreases as positive electric potential is increased along a material axis. Hence, if a positive gate voltage is applied along the gate terminal, the gate fermi level would decrease, i.e. move toward the valance band. Moreover, since

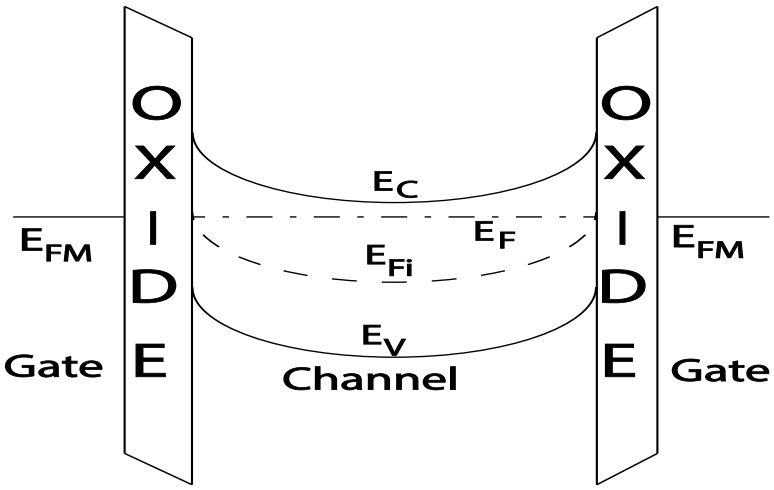

Figure 1.8: *Energy Band Diagram of n-channel NW JL MOSFET in Full Depletion*

potential decreases with distance from source, the channel would experience an effective negative voltage according to Kirchhoff's Voltage Law. As a result, the channel Fermi Level would tend to move upward nearer to the conduction band.

The fermi level matching in thermal equilibrium occurs due to the tendency of materials to maintain equilibrium charge density throughout the surface. But, when a voltage is applied, the equilibrium condition is no longer persists. Hence there would be a mismatch of Fermi levels present in the device, resulting in straightening out of the conduction and valance bands.

Figure 1.9 displays the band diagram under positive gate voltage biasing condition. With the increase of gate bias, the Fermi level drifts apart, and ΔE reduces. Hence, the band bending declines and so the depletion region width decrease with increasing gate voltage. This is known as the Partial Depletion mode of device operation [39].

Now, let's review the device structure to delve into device operation. The channel from drain to source is the active region of the device, which is expected to allow ample current flow under proper gate biasing constraints. When the device has no input gate voltage present, the induced space charge region almost completely covers the channel region. It can be visualized as the gate choking the channel such that little to no current can flow.

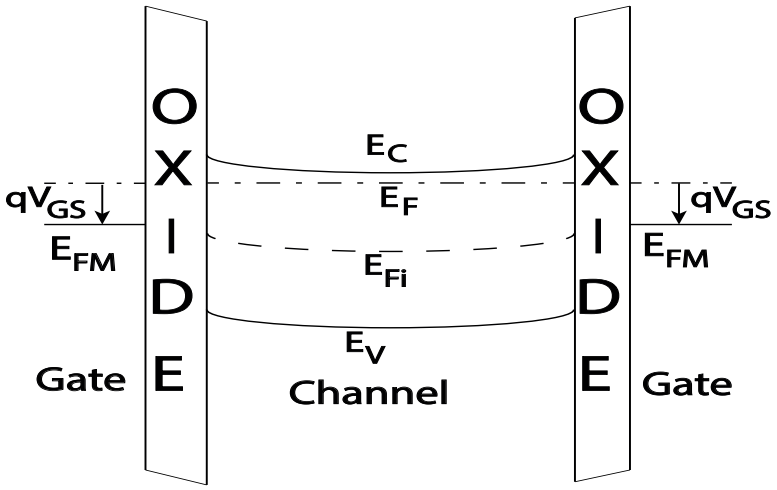

Figure 1.9: *Energy Band Diagram of n-channel NW JL MOSFET in Partial Depletion*

As gate voltage is increased, the space charge region reduces in area, and moves further away from the center. Hence, current now has better potential of flowing than before. As said before, the chokehold of the gate on the channel lessens as current flow path cross section area increases. As a result, drain current flow initiates [33].

After reaching a certain gate voltage, current flow commences. A certain gate voltage can be marked as the "Threshold Voltage" of the device. Up to this point no current can flow through the channel, since sufficient mobile charge density cannot muster up for current flow. At the threshold, finally the current flow can begin.

Another significant bias point of the device can be marked as the "Corner Voltage". Since space charge region diminishes at the "Flat-Band Voltage", The depletion conditions die out as band structure straightens similar to the pre-connection status. Hence, At Flat-band, the band diagram closely resembles Figure 1.10, as conduction and valance band both are completely straightened.

Figure 1.11 shows standard I/V relations of GAA-JL FET compared to inversion and accumulation type MOSFETs. In case of IM MOSFET devices, the band bending is minuscule, as flat-band lies close to zero voltage. On the other hand, for accumulation, flat band is very close to threshold voltage. But, as it can be clearly seen that unlike MOSFET, the flat-band voltage is situated far higher than threshold voltage for JL FET [33].

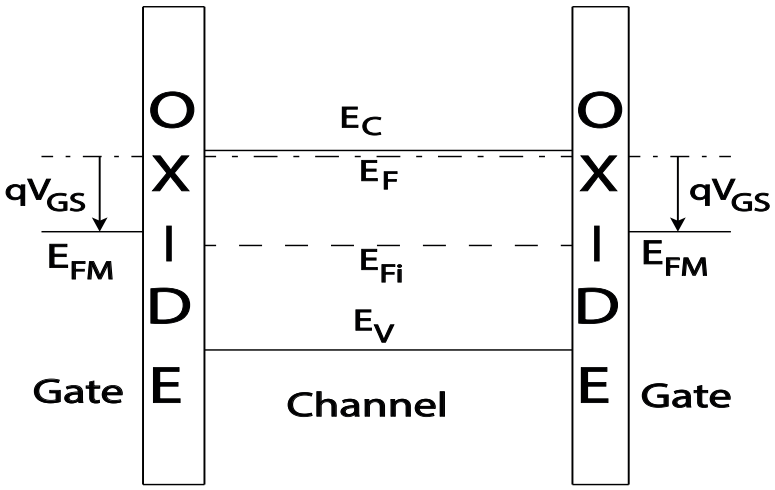

Figure 1.10: *Energy Band Diagram of n-channel NW JL MOSFET in Flat Band*

For voltages higher than the Flat Band voltage, band bending begins again, in the

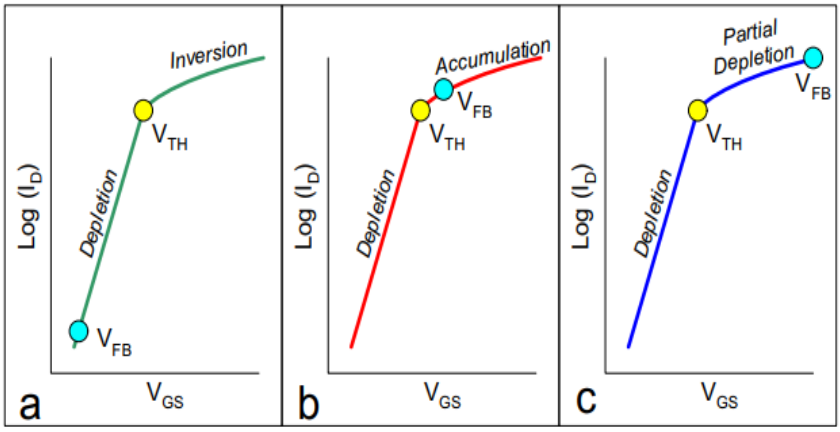

Figure 1.11: *I/V Characteristic of n-channel (a) IM-FET (b) AMFET (c) GAA-JL FET Showing Relative Positions of Threshold and Flat Band Voltage. Figure extracted from [40]*

upward direction, since now accumulation layer of electron is created near the channel surface, which increases surface current carrying capability. Now, current flow occurs due to the accumulation layer of charge present near the junction, similar to AM-MOSFET devices, as opposed to IM devices.

Figure 1.12 Shows the band diagram under a positive gate voltage biasing condition for over the Flat Band Voltage limit. This is the Accumulation Mode of the device operations [39].

The Drain Voltage-Drain Current related I/V Relationship of the NW JL FET device

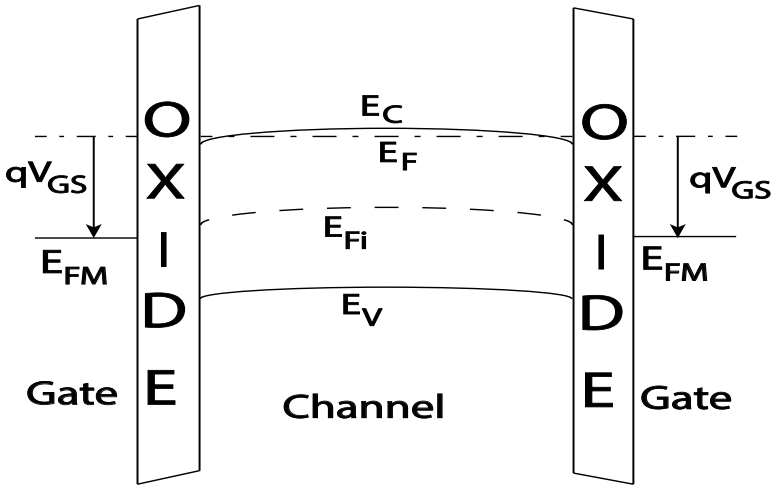

Figure 1.12: *Energy Band Diagram of n-channel NW JL MOSFET in Accumulation*

closely resembles MOSFET I/V relationship. For gate voltage higher than threshold, the drain current increases linearly with drain voltage, as channel current flow path can be considered as resistive. The largest contribution of such resistance comes from impurity scattering of carrier free electrons [33].

However, for sufficiently large input drain to source voltage, the channel charge density varies significantly from drain to source. At a certain high voltage the channel is pinched off, and incremental resistance is nullified. Hence, drain current remains constant for higher voltage constraints. This operation is hence same as FET characteristics.

1.4.3 Advantages of the Device

Since its inception, JL MOSFET has been the center of major study and analysis for its overwhelming potential of near future industrial fabrication and day-to-day applications in electronics sector. The device even has the potential of dethroning MOSFET as the principal supply of transistors, which are the building blocks of modern electronic circuitry. Moreover, the potential of the device in device scaling can even overcome the predictions of Moore's Law. The major advantages of the device are explained in brief as follows.

The junctionless nanowire transistor (JL FET), unlike MOSFET or BJT, contains

no distinct pn junctions in its channel region or any part of the current carrying path of the device. This is a significant departure from the FET based device characteristics, where a pnp or npn junction is a major element of device operations.

The junctions present in a FET based device results in several severe complications in fabrication process. with increasing scaling of the device size, the junctions in the device channel needs to be scaled as well. However, for proper and better device operations, it is expected that abrupt junction ending assumptions can hold up reasonably. To ensure that, very steep doping gradient must be maintained. Even in the deca-nanometer regime, abrupt ending of dopant concentration must be simulated as closely as possible, which results in extremely high doping density gradients near the junctions [9]. The doping gradient increases further with device scaling, which is increasing fast as predicted by Moore's law [1]. This problem is worsened by increased doping density in scaled Nanowire devices for ensuring enhanced properties.

For current fabrication technology, maintaining such intricate slope is proving more and more difficult. The diffusion characteristics and statistical nature of dopant and semiconductor prohibits the formation of ultra-shallow junctions with extremely high doping concentration gradients. This constraint is holding up scaling industry all by itself. Most modern fabrication techniques use novel doping techniques and ultrafast annealing techniques, which must be constantly improved, making evolution increasingly difficult. Even, a tradeoff between device scale and quality is fast prevailing.

The JL FET device, on the other hand, does not contain any explicit pn junctions. In fact, the channel present in the device is uniformly doped p or n type semiconductor with no doping gradient present whatsoever. Hence, the intricacies involved with doping gradient are of little to no consequence for the device at hand. Such freedom, makes it easier to design further scaled down transistors with reduced performance tradeoff.

Ideal FET based devices are supposed to perform as a simple switch, or at least a linear gates resistor, where the gate acts as a switching controller, turning ON or OFF the drain to source channel. However, in reality, several non-linear effects affect the

device operations. Usually, enhanced device design techniques are used to reduce such complication to such an extent as possible, while device operations and characteristics are modeled via equations and diagrams, and appropriate approximations are made in order to simulate ideal device characteristics.

However, with further scaling of the device, several non-ideal factors are becoming more and more significant, which were considered trivial previously. Among them Short-Channel Effects is of major concern.Such non-ideal effects are detrimental to the proper gate control of MOSFETs. However, recent studies show that multi-gate nanowire structure can be used to improve gate control against short channel effects to the highest degree [41]. According to the term proposed by Yan et al. (1992), the Natural Length (λ) of the dual gate device is defined as [42]:

$$\lambda = \sqrt{\frac{\epsilon_s}{2\epsilon_{ox}}(1 + \frac{\epsilon_{ox}t_s}{4t_{ox}\epsilon_s})t_s t_{ox}} \tag{1.1}$$

Where t_s and t_{ox} are the semiconductor and oxide thicknesses and ϵ_s and ϵ_{ox} are the permittivity of semiconductor and oxide, respectively.

In case of multi-gate nanowire structure a term called Effective Number of Gates (n) can be introduced which also depends on threshold voltage on silicon film thickness, which in turn decreases the effective natural length of the device. According to improved relations by Suzuki et al. (1993) for the n-gate MuGFETs [43]:

$$\lambda = \sqrt{\frac{\epsilon_s}{2\epsilon_{ox}}(1 + \frac{\epsilon_{ox}t_s}{4t_{ox}\epsilon_s})t_s t_{ox}} \tag{1.2}$$

A device can be considered free of short-channel effects if the gate length is at least 6-10 times larger than the Natural Length (λ). Hence multi-gate devices show drastically reduced short-channel effects. The GAA-JL FET structure displays especially significant reductions in such effects. For example, highly improved DIBL constraints can be viewed for JL FET devices [43].

Traditional FET devices show aggravated device characteristics with increased temperature. In conventional MOSFET devices, the threshold voltage decreases with

temperature, which in turn increases the drain current. However, carrier mobility decreases with increased temperature due to increased phonon scattering. The two variations counteract each other. At a certain temperature, these two effects cancel out one another. The gate bias for which such effects counteract each other is denoted as the Temperature Coefficient (ZTC) point [44].

However, in case of JL FET devices, the reduction of mobility is significantly less than traditional FET devices. Hence, there is no JL FET, resulting in monotonic increase of current with temperature. The use of the MuGFET structure can further reduce the temperature dependence of the threshold voltage when narrow silicon wires are used due to the reduction in the surface potential variation with the temperature [45]. As a result, better I/V characteristics can be observed at high voltage and higher temperatures. Also, the usual nonideal effects found for MOSFET at high temperature is less significant for GAA-JL FET.

The subthreshold conditions of a transistor are defined as the device characteristics and I/V relations observed for voltage under the threshold limit for the device. Under this condition, usual I/V relations of the device does not hold up. Gate leakage and other non-ideal factors prevail as significantly higher current can be observed for reduced bias voltage.

Such non-idealities constitute the OFF current of the device. The ON-OFF current ration of the device has a high significance as it marks device operation efficiency to some extent. The ratio can be improved by limiting the Subthreshold Slope of the device, i.e. rate of increase of OFF current, and hence reducing the OFF current considerably.

The subthreshold slope of a device limits the on-off current ratio of a device, which has the theoretical minima at 60 mV/decade for MOSFETs. However, that is no longer sufficient with increased device scaling along with gate voltage reduction. Positive feedback loop from increased current due to impact ionization can be used to limit the slope further down. However, multi-gated JL FET structure can be used to find better characteristics [46]. The device displays increased electron temperature but decreased

ionization rate for similar slope, resulting in increased slope efficiency. At voltage under threshold, i.e. under subthreshold conditions, both JL FET and MOSFET are turned off, and a high electric field is found at the drain junction of the MOSFET, which holds the bulk of the applied drain bias which peaks in the channel region. But In the junctionless device, the drain potential drop is found inside the drain electrode, outside of the region covered by the gate, since current blocking is caused by pure electrostatic pinch-off of the heavily doped nanowire structure. Hence the entire channel region is pinched off, and bulk of the drain potential drop is found in the drain, near the gate electrode. The region over which impact ionization takes place is found to be much larger in the junctionless devices than a MOSFET, reducing Drain to Source voltage considerably. Hence JL MOSFET can support an improved subthreshold slope.

1.5 Literature Review of Junctionless Transistor

NW JL MOSFET has gained significant attention in the research community since its introduction. Jean-Pierre Colinge and Lee Chi Woo are considered as the pioneer in the race of unfolding novel attributes and innovations in the field of JL MOSFET.

J. Lilienfeld first proposed and patented JL MOSFET structure in 1930 [47]. His proposed device, also known as "Lilienfeld Transistor" in USA, was patented under the title "Device for controlling electric current". The Lilienfeld transistor is a field effect device, much like modern MOS device. It consists of a thin semiconductor film deposited on a thin insulator layer, itself deposited on a metal electrode [48]. The latter metal electrode serves as the gate of the device. in operation, the current flows in the resistor between two contact electrodes, in much the same way that drain current flows between the source and drain in a modern MOSFET. The Lilienfeld device is a simple resistor, and the application of a gate voltage allows the semiconductor film of carriers to be depleted, thereby modulating its conductivity. ideally, it should be possible to completely deplete the semiconductor film of carriers, in which case the resistance of the device becomes quasi-infinite.

Recently, Lee et al. first proposed and analyzed the characteristics of JL multigate

MOSFET [49]. They investigated the first model of a triple gate JL MOSFET via 3D simulation in ATLAS. Their proposed device structure enclosed n type Si channel with no effective p-n junction. The study performed detailed analysis of JL FET device properties and relative merits and demerits. Due to its junctionless structure, doping gradient related problems were eliminated. They also studied the non-ideal properties and compared it against inversion type MOSFET. In this the JL MOSFET exhibited improved DIBL and subthreshold slope compared to its inversion mode counterpart which indicate the excellent turn-off and short channel characteristics of JL MOSFET.

The first significant progress in the research of JL MOSFET came in 2010 when J. P. Colinge et al [33]. first demonstrated the multigate JL MOSFET experimentally. SOI technology was used for the device construction. The study showed that the current voltage characteristics of JL transistor, also coined as gated resistor, are remarkably similar to those of a regular MOSFET. They fabricated both the n type and p-type JL MOSFET and demonstrated full CMOS functionality of gated resistors. The absence of doping gradients in those devices ensured that the device were much less sensitive to thermal budget issues than regular CMOS devices. From the measurement they have obtained near-ideal subthreshold slope, close to 60 mv/dec at room temperature in JL MOSFET and extremely low leakage current. In addition, their fabricated device exhibited less degradation of mobility with gate voltage increase compared to classical inversion mode MOSFET.

Colinge et al. elaborated on the theoretical aspects of JL multigate MOSFET in 2011 [40]. They explained the conduction mechanism in JL MOSFET and found that the device do not operate in inversion or accumulation, but only in full or partial depletion. They also illustrated the constraints of JL MOSFET- thin and narrow heavily doped semiconductor channel which are required for proper operation of the device. They also found that the threshold voltage depends on doping, equivalent oxide thickness (EOT) as well as on the width and thickness of the nanowire. In addition, they proposed the concept of a bulk multi-gate MOSFET without any lateral source-drain junction. They have demonstrated that JL MOSFET can exhibit low leakage current and excellent short channel behavior. Through simulation study, they have showcased

the potential of JL FET as a strong candidate for future CMOS.

Lee et al. (2010) studied the effect of High Temperature on JL MOSFET [44]. It was observed that the use of the MuGFET structure can reduce the temperature dependence of the threshold voltage when narrow silicon fingers are used due to the reduction in the surface potential variation with the temperature. The study observed the fact that in JL FET, no Zero Temperature Coefficient (ZTC) point exists, resulting in monotonic current increase. This phenomenon results in possible better JL FET operation under high temperature constraints. However, the off leakage current increases with temperature because of the increase of intrinsic carrier concentration, which increases both diffusion and generation currents. Here, DIBL at high temperature is dominated by Band-to-Band Tunneling (BBT), rather than Band-to-Defect Tunneling (BDT) as in the case of MOSFETs. Hence, the usual non-ideal effects at high temperature are less significant for GAA-JL FET as well.

In 2010, J. P. Colinge et al. investigated the variation of Electric field of JL transistor [50]. The effective oxide thickness (EOT) variation with scaling causes increase in the vertical electric field of a FET, resulting in high carrier scattering, and consequently mobility is decreased. When JL FET is turned on, it is in flat-band condition. As a result there is zero electric field in the direction perpendicular to current flow. Hence transconductance decreases less rapidly with applied voltage for JL FET compared to inversion mode device. Since high electric field is responsible for reduction of mobility, this provides and advantage to JL devices in terms of current drive.

Lee et al. compared the improvement of subthreshold slope between standard inversion type multigate NW MOSFET and JL NW MOSFET. It is established that on-off switching capability is represented by subthreshold slope and classical transistor has a theoretical best value limit of SS of 60 mV/dec at room temperature. The impact ionization has the potential to overcome this limit and achieve lower SS which is required for devices of future technology node. The positive feed facilitated by impact ionization results in the rapid on-off transition of device current and hence SS below 60 mV/dec is observed. Under subthreshold conditions, in case of JL FET, the drain

potential drop is found inside the drain electrode, outside of the region covered by the gate. Hence the entire channel region is pinched off, and bulk of the drain potential drop is found in the drain, near the gate electrode. The region over which impact ionization takes place is found to be much larger in the junctionless devices than a MOSFET, reducing Drain to Source voltage considerably. Hence JL MOSFET can support a much sharper subthreshold slope.

Ansari et al. reported a Si Nanowire GAA-JL FET with 3 nm gate length and 1 nm wire diameter in 2010 [51]. This study considered the GAA JL FET structure with 3.1 nm feature size, scaled down from 1 μm one from previous studies, and hence shifting device properties to complete Nanoscale range. They also implanted a very high doping density in the scale of $8 \times 10^{20} atoms/cm^3$. The simulation was performed via full quantum mechanical treatment using Density Functional Tight-Binding ($DFTB^+$) Method, parameters calculated via Density Functional Theory (DFT) over an 800-atom supercell. Mulliken Population Analysis was performed to calculate the localized charge density. The analysis shows adequate carrier density even under undoped channel conditions, which is unlikely for both similar scale MOSFET and larger JL FET devices. However, de-localization would make the junctionless design more robust against dopant fluctuations. The observed I/V characteristics were in accordance with results obtained for larger feature size. Also, the positioning of the dopant in the wire cross section makes a difference in the band structure of the device, which results in steeper I/V relation at low bias.

In 2011, Su et al. proposed a novel junctionless structure with Polysilicon nanowire channel for the first time [38]. They experimentally investigated the feasibility of GAA polycrystalline silicon (poly-Si) nanowire transistors with junctionless configuration by utilizing only one heavily doped poly-Si layer to serve as source, channel, and drain regions in a GAA-JL FET structure. The formation of cavities was carried out by carefully controlling the lateral etching of the Tetraethyl Orthosilicate (TEOS) oxide layer in dilute HF solution. High Resolution Transmission Electron Microscopic (HRTEM) Image was obtained to study the designed model. Better I/V characteristics than a MOSFET structure was observed for this model. A very high transconductance was

also observed compared to the IM device. Channel resistance also decreases considerably, which increases with channel length for obvious reasons. The device also shows very high on-off current ratio and low subthreshold slope.

Doria et al. investigated the analog parameters of JL MOSFET to analyze its feasibility in analog communication field applications [52]. They performed an in-depth comparison of the analog operation of JL and IM trigate devices aiming at low-power applications and attempt to explain the physical mechanisms behind the obtained results. JL transistors were found to exhibit both better Early voltage and larger intrinsic voltage gain than IM devices of similar dimensions at high values of transconductance. The JL transistors showed higher variation of conductance with voltage, which was addressed through 3-D numerical simulations. When the influence of the temperature is taken into consideration, JL transistors are able to provide a constant drain current over a wide temperature range, unlike IM devices. Hence, JL devices present better analog properties than IM transistors in low-moderate frequencies of operation.

Traditionally Silicon has been used as a channel material in ultra-scaled device due to its mature fabrication technology. But in recent times, III-V materials have attracted a lot of attention to their superior electronic properties compared to Si. As a result, III-V materials are extensively studied as a viable candidate to replace Si as channel material in future technology node. As a wide bandgap III-V material, GaN has some remarkable attributes that may prove to be useful in sub-10 nm transistor technology. Its wide band-gap significantly reduces band-to-band tunneling and gate induced drain leakage (GIDL) and allows for high temperature operation as demonstrated by Cai et al [53]. The wide bandgap of GaN can suppress the device off-current, while the high electron mobility and comparatively large density of states mas enables high current density for high switching speed [54]. Besides, the wide bandgap an Chemical resistance also make GaN nanowire MOSFETs promising for operation in harsh environment (such as high temperature, radiation, and extreme pH levels) [55]. Due to high optical phonon energy (93 meV) [56], wide valley separation (nearest valley to Γ is M and it is $>$ 1 eV apart) and high mobility, fully ballistic transport is expected in the sub-30 nm regime [57]. Room temperature ballistic transport in GaN has already been

experimentally demonstrated by Matioli and Palacios in 2015 [58]. GaN-based transistors with a current gain cut-off frequency approaching 500 GHz have already been reported by Shinohara et al. in 2013 [59]. In addition, being a direct bandgap material, GaN-based on chip optical communication is possible thanks to the maturity of GaN based photonic devices [60]. In addition, its spontaneous and piezoelectric polarization offers a new degree of freedom to dope the source and drain region without the impact of Random Dopant Fluctuation (RDF) effects and thermal diffusion of dopants [61]. Finally, it has been demonstrated that the modulation of polarization charge in the III-Nitride system could yield sub-40 mV/dec switching operation [62]. The piezoelectricity in GaN has also been proposed to attain steep subthreshold behavior [63]. All these benefits make a GaN channel an intriguing option for future n-MOSFET devices for digital applications [64], which could complement the well-known markets of GaN for RF [65] and power applications [66].

Im et al. demonstrated the GaN JL FinFET experimentally for the first time in 2013 [67]. In their proposed device, current flowed through the volume of the heavily doped GaN fin rather than at the surface channel, which greatly improved device performance by eliminating the adverse effects related to the interface quality. They used simplified pragmatical technology for GaN epitaxial growth and FinFET process to achieve with a channel width from 40 to 100 nm and a gate length of 1 μm. From device characterization, they obtained excellent on-state performance from the fabricated device, such as maximum drain current of 670 mA/mm and maximum transconductance of 168 mS/mm. In addition, they measured record off-state performance with extremely low leakage current of 10^{-11} mA and source-drain breakdown voltage of 280 V. THey obtained subthreshold slope close to theoretical limit which lead to very high I_{on}/I_{off} ratio of $10^8 - 10^9$.

In 2014, Im et al. investigate experimentally the radio-frequency (RF) performances of a GaN based JL trigate FET along with RF modeling for the first time [68]. The JL GAN FET allowed normally off operation along with reduced fabrication complexity compared to GaN HEMT. Their fabricated device with five fin channels exhibited a maximum drain current of 403 mA/mm and maximum transconductance of

123.6 mS/mm. Furthermore, maximum cutoff frequency and maximum oscillation frequency were obtained as 2.45 and 9.75 GHz respectively. In addition, they presented a small signal model to confirm the potential of GaN JL FinFET in high-frequency application.

The GaN NW JL MOSFET with fully conformal cylindrical gate was first demonstrated experimentally by Blanchard et al.[69]. Their fabricated device was based on individual n-type GaN NW with conformal surrounding gate resulted from atomic layer deposition (ALD) of W/Al_2O_3. Their fabricated device exhibited low leakage current, small threshold voltage, high transconductance and large on/off current ratio. They obtained reverse bias breakdown voltage of 35 V and threshold voltage between -4 V to -12 V. In addition, maximum transconductance exceeding 10 μS and on/off current ratios higher than 10^8 were measured. Apart from these excellent performance, their proposed device exhibited significant deviations from ideal behavior with SS of the order of 190 $mV/decade$ and significant gating hysteresis and memory effect due to charge traps.

In 2016 Gacevic et al. presented a top-gate GaN NW metal semiconductor FET (MESFET) with improved channel electrostatic control [70]. They processed a uniformly n-type doped $GaN : Si$ NW, with a diameter of $d = 90$ nm and a length of 1.2 μm into a MESFET with a semi cylindrical top Ti/Au Schottky gate. The FET was in a normally-on mode, with the threshold at -0.7 V and transconductance of $g_m \approx 2$ μS. The device entered the saturation mode at $V_{DS} \approx 4.5$ V, with the maximum measured drain current $I_{DS} = 5$ μA and the current density exceeding $J_{DS} > 78$ kA/cm^2.

Li et al. investigated GaN NW JL MOSFET experimentally in 2018 [71]. They fabricated wrap-around gate GaN NW MOSFETs using Al_2O_3 as gate oxide. Their fabricated device exhibited a minimum subthreshold slope of 68 mV/dec over three decades of drain current, drain induced barrier lowering of 27 mV/V, an on current of 42 $\mu A/\mu m$, on-off ratio over 10^8, an intrinsic transonductance of 27.8 $\mu S/\mu m$. They obtained a switching efficiency figure of merit, $Q(= g_m/SS$ of 0.41 $(\mu S/\mu m)/(mV/dec)$ which established GaN NW MOSFETs as a promising candidate for emerging low-

power application.

1.6 Objective of the Thesis

NW JL MOSFET, a novel device in the field of nanoscale electronics, has become a major sensation among up-and-comer transistor-based devices. Being similar in device properties as traditional FETs, the device is unique in the sense that it serves several significant advantages over usual MOSFET. Most significantly, the device requires no channel doping gradient moderation, which makes it uniquely qualified for further scaling down of device structure. It also supports higher temperature operations, while displaying reduced non-ideal subthreshold and short channel effects.

Being such a high-utility device, the GAA-JL FET is now a major concern among modern researchers. However, a comprehensive analytical model of electrostatic and transport properties of GaN NW JL MOSFET incorporating various non-ideal effects including short channel effect, velocity saturation, mobility degradation, channel length modulation, parasitic resistance is vital to make a rigorous study of the performance of the device. This is where my thesis work comes into play. The objectives of this work are:

- To derive analytical expression for surface potential and subsequently gate capacitance of GaN NW JL MOSFET.
- To formulate a comprehensive transport model of the device incorporating non ideal effects such as short channel effect, velocity saturation, channel length modulation, mobility degradation, parasitic resistance etc.
- To present explicit analytical expression of important short channel performance metrics such as threshold voltage roll-off, subthreshold slope and DIBL .

The analytical model presented in this work will act as a guideline for design and optimization of GaN based NW FET and pave the way to an extensive investigation of this device as a viable candidate for future application.

1.7 Organization of the Thesis

The entire thesis is broadly divided into five chapters and a brief outline of each chapter is explained below.

The first chapter gives an introduction of the continuous need of MOSFET scaling and the challenges that are associated with aggressive device miniaturization. This chapter also presents some alternative device structure and channel material which have the potential to enable further scaling of MOSFET. In addition, this chapter includes the motivation to this work and important highlights followed by a brief overview of JL NW FET and existing literature about the field of this work.

The evolution of surface potential model of GaN NW JL MOSFET is presented in chapter two. The surface potential model facilitates the derivation of gate capacitance as a function of gate voltage which comprises the electrostatic properties of the device. The model takes into account the crucial role of various device parameters including the doping concentration, nw radius and oxide thickness in influencing the electrostatic properties of the device. In addition, threshold voltage model for long channel device is presented in this chapter.

The third chapter considers the development of transport model of GaN NW JL MOSFET. Several non ideal effects present in deep sub micron device including short channel effect, channel length modulation, velocity saturation, mobility degradation, parasitic source drain resistance have been incorporated in the transport model. Furthermore, explicit equation to calculate device parameters, vital to quantify short channel performance, such as threshold voltage roll-off, subthreshold slope, drain induced barrier lowering have been formulated in this chapter.

The results obtained from analytical modeling of electrostatic and transport properties are exhibited in chapter four. The results obtained from the analytical model are compared with that from reported experimental data and simulation results to confirm the validity of the proposed model.

The fifth chapter draws the conclusion of my entire thesis. It also presents the scopes for further improvement of the work and provides a suggestion of possible areas which can be explored in future.

Chapter 2

Electrostatic Model Development

Reliable and predictive models are necessary for fast developing devices and circuits. This chapter presents the electrostatic model formulation for *GaN* NW JL MOSFET. The electrostatic model development involves the solution of quasi 2-D Poisson equation using appropriate boundary condition. The surface potential obtained from the solution of Poisson equation is used to formulate the mobile carrier density which is subsequently used in derivation of the gate capacitance model. In addition, an analytical threshold voltage model for long channel device is also proposed in this chapter.

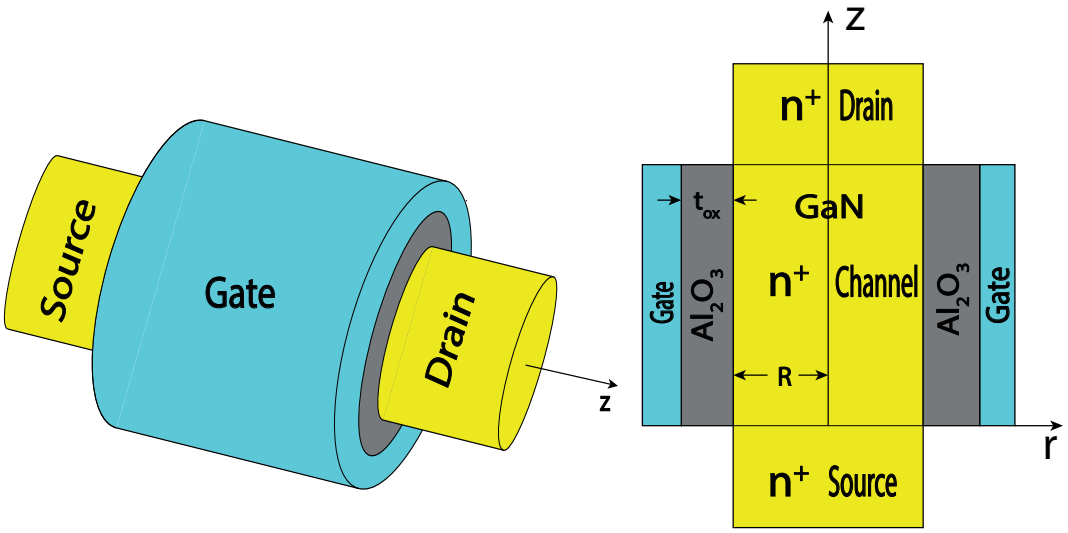

Figure 2.1: *Schematic view of an N-channel GaN NW JL MOSFET (a) and its longitudinal cross section (b)*

2.1 Surface Potential Model

The model has been developed for the long channel GaN NW JL MOSFET shown in figure 2.1. Assuming that the NW has channel radius R, gate length L_G, oxide thickness t_{ox} and a uniform doping concentration N_D in the channel, source and drain region. We can express the effective gate voltage as the sum of the voltage drop across semiconductor and oxide,

$$V_{g(eff)} = V_{GS} - V_{FB} = \phi_s + \phi_{ox} = \phi_s - \frac{Q_{sc}}{C_{ox}} \tag{2.1}$$

where, $V_{FB} \approx \phi_{ms}$ is the flat band voltage, ϕ_{ms} is the metal-semiconductor work function difference, ϕ_s is the surface potential and Q_{sc} is the space charge density per unit area within nanowire. For NW MOSFET gate oxide capacitance per unit area can be expressed as,

$$C_{ox} = \frac{\epsilon_{ox}}{R\left[ln(1+\frac{t_{ox}}{R})\right]} \tag{2.2}$$

For a long channel device, gradual channel approximation is applicable which reduces the Poisson equation to it's 1-D form. With reference to electron quasi fermi level V, for an n-type NW MOSFET with doping concentration N_D, the Poisson equation in the cylindrical coordinate can be written as,

$$\frac{1}{r}\frac{d}{dr}\left(r\left(\frac{d\phi(r)}{dr}\right)\right) = \frac{qN_D}{\epsilon_s}\left(exp\left(\frac{q(\phi - V)}{kT}\right) - 1\right) \tag{2.3}$$

Equation (2.3) must be solved with following boundary conditions,

$$\frac{d\phi}{dr}(r=0) = 0 \quad and \quad \phi(r=R) = \phi_s \tag{2.4}$$

The 1^{st} boundary condition results from the continuity of the electric field and the constraint of radial symmetry whereas the 2^{nd} one is related to the gate bias via (2.1). Despite the apparent simplicity, (2.3) does not possess any closed form analytical solution. To obtain an approximate solution of (2.3), regional approach has been considered along with simplifying assumptions in accumulation and depletion region.

2.1.1 Channel in Accumulation Mode

The accumulation region occurs when $\phi_s > V$, where V is the quasi fermi level, and an asymptotic solution can be taken in the limit of $\lambda_D << R$ where $\lambda_D = \sqrt{(\frac{\epsilon_s kT}{q^2 N_D})}$ is the Debye length. If the above condition holds as usually the case if $N_D \approx 10^{18} cm^{-3}$ and $R \geq 10nm$, no volume accumulation occurs within the NW-FET and the electric field drops quickly to zero, and electric potential becomes $\phi(r) = V$ over the extended central area of the NW. In this limit the NW-FET behaves similar to planar device with a width $W = 2\pi R$. With this simplified approximation we find,

$$\frac{d^2\phi}{dr^2} = \frac{qN_D}{\epsilon_s}\left(exp\left(\frac{q(\phi - V)}{kT}\right) - 1\right) \tag{2.5}$$

This equation can be written as,

$$d\left(\frac{1}{2}\left(\frac{d\phi}{dr}\right)^2\right) = \frac{qN_D}{\epsilon_s}\left(exp\left(\frac{q(\phi - V)}{kT}\right) - 1\right)d\phi \tag{2.6}$$

Integrating both sides we get,

$$\frac{1}{2}(\frac{d\phi}{dr})^2 = \frac{qN_D kT}{\epsilon_s q}\left(exp\left(\frac{q(\phi - V)}{kT}\right) - 1 - \frac{q(\phi - V)}{kT}\right) \tag{2.7}$$

At $r = R$, $\phi(R) = \phi_s$ and $\frac{d\phi}{dr}(r = R) = E_s$ Using these boundary conditions, the surface electric field can be obtained as,

$$E_s = \sqrt{\frac{2N_D kT}{\epsilon_s}\left[exp\left(\frac{q(\phi_s - V)}{kT}\right) - \frac{q(\phi_s - V)}{kT} - 1\right]} \tag{2.8}$$

From the Gauss's law the total charge induced per unit area is,

$$Q_{sc(acc)} = -\epsilon_s E_s = -\epsilon_s\sqrt{\frac{2N_D kT}{\epsilon_s}\left[exp\left(\frac{q(\phi_s - V)}{kT}\right) - \frac{q(\phi_s - V)}{kT} - 1\right]} \tag{2.9}$$

Substituting $Q_{sc(acc)}$ from (2.9) to (2.1) we get,

$$C_{ox}(V_{GS} - V_{FB} - \phi_s) = \sqrt{2N_D kT\epsilon_s\left[exp\left(\frac{q(\phi_s - V)}{kT}\right) - \frac{q(\phi_s - V)}{kT} - 1\right]} \tag{2.10}$$

From this equation we can write,

$$1 + \frac{(V_{GS} - V_{FB} - \phi_s)^2}{\frac{2N_D kT\epsilon_s}{{C_{ox}}^2}} = exp(\frac{q(\phi_s - V)}{kT}) - \frac{q(\phi_s - V)}{kT} \tag{2.11}$$

Since $\phi_s > V$ in accumulation mode, using the approximation $exp(\frac{q(\phi_s - V)}{kT}) >> \frac{q(\phi_s - V)}{kT}$ and subsequently neglecting the term $\frac{q(\phi_s - V)}{kT}$ in (2.11) we get,

$$1 + \frac{(V_{GS} - V_{FB} - \phi_s)^2}{\frac{2N_D kT\epsilon_s}{{C_{ox}}^2}} = exp\left(\frac{q(\phi_s - V)}{kT}\right) \tag{2.12}$$

So the surface potential in the accumulation region becomes,

$$\phi_{s(acc)} = V + \phi_t ln\left[1 + \frac{(V_{GS} - V_{FB} - \phi_{s(acc)})^2}{\beta\phi_t}\right] \tag{2.13}$$

where, $\beta = \frac{2N_D q\epsilon_s}{{C_{ox}}^2}$ and $\phi_t = \frac{kT}{q}$

An exact solution of (2.13) can be obtained using Lambert function [72]. However, since $\phi_{s(acc)}$ is only a few ϕ_t in strong accumulation, $\phi_{s(acc)}$ inside the logarithmic term in the above equation can be ignored [73] which results into following equation.

$$\phi_{s(acc)} = V + \phi_t ln\left[1 + \frac{(V_{GS} - V_{FB})^2}{\beta\phi_t}\right] \tag{2.14}$$

2.1.2 Channel in Depletion Mode

When the device is biased in depletion or subthreshold region, i.e. $\phi_s < V$, instead of considering the usual depletion approximation that involves abrupt transition between neutral and depletion region, we linearize the exponential term in R.H.S. of (2.3) by setting $\phi = \phi_c + \delta\phi$, where ϕ_c is the electrostatic potential at the nanowire symmetry axis and $\delta\phi$ is the perturbation potential. This is the first order approximation of exact carrier concentration in the quasi neutral region [74].

Using this approximation from Poisson's equation we get,

$$\frac{d^2\delta\phi}{dr^2} + \frac{1}{r}\frac{d\delta\phi}{dr} - \frac{qN_D}{\epsilon_s\phi_t}exp\left(\frac{q(\phi_c - V)}{kT}\right)\delta\phi = \frac{qN_D}{\epsilon_s}\left(exp\left(\frac{q(\phi_c - V)}{kT}\right) - 1\right) \tag{2.15}$$

Equation (2.15) holds for $0 \leq r \leq r_0$ where $\delta\phi(r_0) = -\phi_t$. Solving (2.15) using the following initial condition, $\delta\phi(r = 0) = 0$ and $\frac{d\delta\phi}{dr}(r = 0) = 0$, we get,

$$\delta\phi(r) = \phi_t(1 - \alpha^2)I_o\left(\frac{r}{\alpha\lambda_D}\right) - \phi_t(1 - \alpha^2) \tag{2.16}$$

where, $\alpha = \sqrt{exp(\frac{V-\phi_c}{\phi_t})}$.

As mentioned previously, this solution is valid for $0 \leq r \leq r_0$ where $\delta\phi(r_0) = -\phi_t$. Using this boundary condition in (2.16) we obtain the value of r_0 as follows,

$$r_0 = \alpha\lambda_D {I_0}^{-1}\left(1 - \frac{1}{1 - \alpha^2}\right) \tag{2.17}$$

For $r_0 \leq r \leq R$, we consider the depletion approximation instead, i.e.

$$\frac{d^2\delta\phi}{dr^2} + \frac{1}{r}\frac{d\delta\phi}{dr} = -\frac{qN_D}{\epsilon_s} \tag{2.18}$$

From (2.16), the electric field at $r = r_0$ can be expressed as,

$$\frac{d\delta\phi}{dr}(r = r_0) = \phi_t\frac{(1 - \alpha^2)}{\alpha\lambda_D}I_1\left(\frac{r_0}{\alpha\lambda_D}\right) \tag{2.19}$$

Using this electric field as initial condition, solution of (2.18) can be obtained as,

$$\delta\phi(r) = -\frac{qN_D}{\epsilon_s}\left(\frac{r^2 - {r_0}^2}{4}\right) - \phi_t + \left[\frac{qN_D}{\epsilon_s}\left(\frac{{r_0}^2}{2}\right) + r_0\left(\frac{\phi_t(1 - \alpha^2)}{\alpha\lambda_D}I_1\left(\frac{r_0}{\alpha\lambda_D}\right)\right)\right] ln\left(\frac{r}{r_0}\right) \tag{2.20}$$

Here, I_0 and I_1 are modified bessel function of first kind with order 0 and 1 respectively. Using the solution of $\delta\phi(r)$ obtained in (2.16) and (2.20) for 2 regions, the surface potential can be written as,

$$\phi_{s(dep)} = \begin{cases} \phi_c + \phi_t(1 - \alpha^2)I_o(\frac{R}{\alpha\lambda_D}) & \\ -\phi_t(1 - \alpha^2) & \text{if } r_0 > R \\ \phi_c + [\frac{qN_D}{\epsilon_s}(\frac{{r_0}^2}{2}) + r_0(\frac{\phi_t(1-\alpha^2)}{\alpha\lambda_D}I_1(\frac{r_0}{\alpha\lambda_D}))]ln(\frac{R}{r_0}) & \\ -\frac{qN_D}{\epsilon_s}(\frac{R^2-{r_0}^2}{4}) - \phi_t & \text{if } r_0 \leq R \end{cases} \tag{2.21}$$

Differentiating (2.16) and (2.20) with respect to r and using the following relationship between charge density and channel potential, i.e.

$$Q_{sc(dep)}(r = R) = -\epsilon_s \frac{d\phi(r)}{dr}(r = R) \tag{2.22}$$

the space charge density in depletion region can be derived as,

$$Q_{sc(dep)} = \begin{cases} \epsilon_s \left(\frac{\phi_t(\alpha^2-1)}{\alpha\lambda_D} I_1(\frac{R}{\alpha\lambda_D}) \right) & \text{if } r_0 > R \\ \frac{qN_D R}{2} - \frac{\epsilon_s}{R}[\frac{qN_D}{\epsilon_s}(\frac{{r_0}^2}{2}) & \\ +r_0(\frac{\phi_t(\alpha^2-1)}{\alpha\lambda_D} I_1(\frac{R}{\alpha\lambda_D}))] & \text{if } r_0 \leq R \end{cases} \tag{2.23}$$

The computation of $\phi_{s(dep)}$ involves simultaneous solution of (2.1), (2.21) and (2.23).

2.1.3 Continuous Surface Potential from Depletion to Accumulation

When $V_{GS} \geq V_{FB}$ the center potential ϕ_c asymptotically reaches to quasi fermi potential, i.e. $\phi_c \approx V$. This results in $\alpha \approx 1$ which causes $r_o >> R$ according to (2.17). As a result according to the condition imposed in (2.21), the surface potential in the depletion region $\phi_{s(dep)}$ smoothly converges to V when $V_{GS} \geq V_{FB}$. On the contrary, surface potential in the accumulation region should asymptotically reach zero below flat band voltage, i.e. $\phi_{s(acc)} = 0$ for $V_{GS} \leq V_{FB}$ which can be achieved by using following smoothing function.

$$V_{GS(smooth)} = V_{FB} \left(1 + \frac{ln(1 + exp(A_1(-1 + \frac{V_{GS}}{V_{FB}})))}{ln(1 + exp(A_1))} \right) \tag{2.24}$$

A_1 controls the smoothness between different conduction regime which is set to 10 in this work. Using the above smoothing function, the surface potential in accumulation region becomes,

$$\phi_{s(acc)} = \phi_t ln \left[1 + \frac{(V_{GS} - V_{GS(smooth)})^2}{\beta\phi_t} \right] \tag{2.25}$$

The combined surface potential of long channel NW JL MOSFET valid for both accumulation and depletion region can be obtained as,

$$\phi_s = \phi_{s(acc)} + \phi_{s(dep)} \tag{2.26}$$

2.2 Capacitance-Voltage Characteristics

The space charge density can be obtained from surface potential according to following equation,

$$Q_{sc} = -C_{ox}(V_{GS} - V_{FB} - \phi_s) \tag{2.27}$$

Since the total charge density Q_{sc} is the sum of mobile carrier density Q_n and fixed charge density Q_f, absolute mobile charge density can be calculated using following expression,

$$Q_n = Q_{sc} - Q_f = -C_{ox}(V_{GS} - V_{FB} - \phi_s) - \frac{qN_D R}{2} \tag{2.28}$$

The gate capacitance can be obtained by differentiating conduction carrier density with respect to gate voltage,

$$C_g = \frac{dQ_n(V_{GS})}{dV_{GS}} \tag{2.29}$$

2.3 Threshold Voltage Calculation

In the subthreshold regime, the variation of channel potential along the radial direction can be approximated as a parabolic function given below,

$$\phi(r) = \phi_c + (\phi_s - \phi_c)\left(\frac{r}{R}\right)^2 \tag{2.30}$$

Since mobile carrier is negligible in subthreshold region, we can use following approximate Poisson equation,

$$\frac{1}{r}\frac{d}{dr}\left(r\left(\frac{d\phi(r)}{dr}\right)\right) = -\frac{qN_D}{\epsilon_s} \tag{2.31}$$

Substituting the value of $\phi(r)$ from (2.30) in (2.31) we get,

$$\phi_s - \phi_c = -\frac{qN_D R^2}{4\epsilon_s} \tag{2.32}$$

In the deep subthreshold region center potential varies linearly with gate voltage, i.e. $\phi_c \approx V_{GS} - V_T$ where, V_T is the threshold voltage. Moreover, neglecting mobile carrier density in subthreshold region, space charge density can be approximated as fixed charge density, i.e. $Q_{SC} \approx Q_f \approx \frac{qN_DR}{2}$. Substituting the value of ϕ_s from (3.5), $\phi_c \approx V_{GS} - V_T$ and $Q_{SC} \approx \frac{qN_DR}{2}$ in (2.1) we can obtain the threshold voltage for long channel NW JL MOSFET as follows,

$$V_T = V_{FB} - qN_D \left[\frac{A}{C_{ox}} + \frac{1}{\epsilon_s} \left(\frac{A}{P} \right)^2 \right] \tag{2.33}$$

Where, A and P are cross sectional area and the perimeter of the NW respectively.

Chapter 3

Transport Model Development

Transport characteristics is an integral part for the appropriate functioning of a device. This chapter presents a comprehensive model for transport properties of GaN NW JL MOSFET. The model formulation begins with the core drain current model. Later, various non ideal effect pertaining to practical device characteristics including short channel effect, velocity saturation, mobility degradation, channel length modulation and parasitic source-drain resistance have been incorporated in the core transport model to make the model more robust.

The drain current for long channel device can be expressed as,

$$I_D = \frac{\mu_n}{L_g} \int_{V_S}^{V_D} Q_n(V_{GS}) dV_z \tag{3.1}$$

where, μ_n is the electron mobility and Q_n is the mobile carrier density per unit of length.

3.1 SCE Correction

In order to take into account the impact of drain bias on the channel potential i.e. the short channel effect (SCE), we need to solve following 2-D Poisson equation [75] in the subthreshold region considering negligible mobile carrier density,

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi}{dr}\right) + \frac{d^2\phi}{dz^2} = -\frac{qN_D}{\epsilon_s} \tag{3.2}$$

Using parabolic potential approximation in subthreshold region along radial direction, we get,

$$\phi(r,z) = C_0(z) + C_1(z)r + C_2(z)r^2 \tag{3.3}$$

Applying the following boundary conditions, $\phi'(r=0) = 0$, $\phi(r=0) = \phi_c(z)$ and $\phi'(r=R) = \frac{C_{ox}}{\epsilon_s}(V_{GS} - V_{FB} - \phi_s(z))$ in equation (3.3) the channel potential can be written as,

$$\phi(r,z) = \phi_c(z) + \frac{C_{ox}}{2R\epsilon_s}(V_{GS} - V_{FB} - \phi_s(z))r^2 \tag{3.4}$$

where, ϕ_s and ϕ_c satisfy the following equation,

$$\phi_s(z) = \frac{\phi_c(z) + \frac{C_{ox}R}{2\epsilon_s}(V_{GS} - V_{FB})}{1 + \frac{C_{ox}R}{2\epsilon_s}} \tag{3.5}$$

When the NW JL transistor leaves the subthreshold regime at higher gate bias , the carrier predominantly flows along the center of the NW channel which is the most leaky path in the NW. Hence, we are concerned about the ϕ_c. Substituting (3.4) and (3.5) in (3.2) and eliminating ϕ_s we get,

$$\frac{d^2\phi_c}{dz^2} - \frac{1}{\lambda^2}(\phi_c(z) - \phi_{c0}) = 0 \tag{3.6}$$

where, ϕ_{c0} is the long channel minimum central potential and λ is the scaling length. They are given as,

$$\frac{1}{\lambda^2} = \frac{4C_{ox}}{2\epsilon_s R + C_{ox}R^2} \tag{3.7}$$

$$\phi_{c0} = V_{GS} - V_{th(lc)} \tag{3.8}$$

$$V_{th(lc)} = V_{FB} - \frac{qN_D R}{2C_{ox}} - \frac{qN_D R^2}{4\epsilon_s} \tag{3.9}$$

where, $V_{th(lc)}$ is the long channel threshold voltage [74].

The general solution of (3.6) can be obtained as,

$$\phi_c(z) = ae^{\frac{z}{\lambda}} + be^{-\frac{z}{\lambda}} + \phi_{c0} \tag{3.10}$$

With boundary conditions, $\phi_c(z=0)=0$ and $\phi_c(z=L)=V_{DS}$, the expression of a and b in (3.10) can be expressed as,

$$a = \frac{V_{DS} - \phi_{c0}(1 - e^{-\frac{L_g}{\lambda}})}{2sinh(\frac{L_g}{\lambda})} \tag{3.11}$$

$$b = \frac{-V_{DS} + \phi_{c0}(1 - e^{\frac{L_g}{\lambda}})}{2sinh(\frac{L_g}{\lambda})} \tag{3.12}$$

We get the position of minimum center potential as,

$$Z_{min} = \frac{\lambda}{2} ln(\frac{b}{a}) \tag{3.13}$$

Equation (3.13) is valid only in the subthreshold region where $Z_{min} \approx \frac{L}{2}$. Since the position of minimum potential gets shifted towards source side with increasing V_{GS} and V_{DS}, the gate voltage is limited at V_{th} when $V_{GS} > V_{th}$ during the calculation of Z_{min}.

Putting the value of Z_{min} in (3.10) the minimum center potential in short channel NW JL MOSFET can be obtained as,

$$\phi_{c(min)} = 2\sqrt{ab} + \phi_{c0} \tag{3.14}$$

By setting $\phi_{c(min)} = 0$ and solving (3.14) for V_{GS}, the short channel threshold voltage for NW JL MOSFET can be written as,

$$V_{th(sc)} = V_{th(lc)} - \frac{V_{DS} sinh(\frac{Z_{min}}{\lambda})}{sinh(\frac{L_g}{\lambda}) - sinh(\frac{Z_{min}}{\lambda}) - sinh(\frac{L_g - Z_{min}}{\lambda})} \tag{3.15}$$

The difference of minimum center potential for long channel and short channel NW JL MOSFET can be expressed as,

$$\Delta\phi_{c(min)} = \phi_{c(min)} - \phi_{c0} = 2\sqrt{ab} \tag{3.16}$$

To incorporate the SCE in the core transport model for long channel device given in (3.1), $\Delta\phi_{c(min)}$ has been considered as the effective shift in the gate voltage [76]. This effective gate voltage ($V_{GS(eff)} = V_{GS} + \Delta\phi_{c(min)}$) has been used in (3.1) to calculate

the actual drain current given as,

$$I_{D,SCE} = \frac{\mu_n}{L_g} \int_{V_S}^{V_D} Q_n(V_{GS(eff)}) dV_z \tag{3.17}$$

Since the use of (3.17) permits correcting the subthreshold current for short channel NW JL MOSFET, this solution is capable of describing the variation of threshold voltage (V_{th}) and subthrehsold slope (SS) when L decreases and V_{DS} increases. In this paper, the drain induced barrier lowering (DIBL) is defined as,

$$DIBL = \frac{V_{th(sc)}|_{V_{DS}=0.05} - V_{th(sc)}|_{V_{DS}=1}}{\Delta V_{DS}} \tag{3.18}$$

The subthreshold slope is formulated as,

$$SS = \frac{\delta V_{g(eff)}}{\delta log_{10} I_{DS}} \tag{3.19}$$

where, $V_{g(eff)} = V_{GS} - V_{FB}$

Following the similar methodology as in [77, 78], we assume that in subthreshold regime, I_D is proportional to $exp(\frac{\phi(r,z)}{\phi_t})$. Since the current predominantly flows through the center region of NW in subthreshold, the electric potential at $r = 0$ and $z = Z_{min}$ is used for the extraction of subthreshold swing. Therefore the subthrehsold swing can be expressed as,

$$SS = 2.3\phi_t \left(\frac{\delta\phi(0, Z_{min})}{\delta V_{g(eff)}} \right)^{-1} \tag{3.20}$$

Substituting ϕ_c from (3.10) in (3.20), the subthreshold slope can be expressed as,

$$SS = 2.3\phi_t \left(\frac{sinh(\frac{L_g}{\lambda})}{\Gamma} \right) \tag{3.21}$$

where, $\Gamma = sinh(\frac{L_g}{\lambda}) + \frac{\delta Z_{min}}{\delta V_{g(eff)}}((\frac{V_{DS}-\phi_{c0}}{\lambda})cosh(\frac{Z_{min}}{\lambda}) - \frac{\phi_{c0}}{\lambda}cosh(\frac{L_g - Z_{min}}{\lambda}) - sinh(\frac{Z_{min}}{\lambda}) - sinh(\frac{L_g - Z_{min}}{\lambda}))$ and $\frac{\delta Z_{min}}{\delta V_{g(eff)}} = \frac{\lambda}{2}\left[\frac{exp(\frac{L_g}{\lambda})-1}{b} - \frac{1-exp(-\frac{L_g}{\lambda})}{a} \right]$.

Table 3.1: Parameters used in this work

Parameter (unit)	Description	Value
ϵ_s	relative permittivity of GaN	9
ϵ_{ox}	relative permittivity of Al_2O_3	9.2
$V_{FB}(V)$	flat band voltage	-0.7
$R_s(K\Omega)$	parasitic source resistance	2-3
$R_d(K\Omega)$	parasitic drain resistance	2-3
$v_{sat}(10^5 m/s)$	saturation velocity	2.5
$\mu_0(cm^2/V/s)$	low field electron mobility	208
η	velocity saturation parameter	0.15-0.25
κ	channel length modulation parameter	2-2.5
σ	mobility degradation parameter	1-2
θ	mobility degradation coefficient	0.25-0.35
$\phi_B(V)$	schottky barrier height in s/d contact	0.3

3.2 Velocity Saturation

To consider the influence of saturation velocity in short channel device, the following empirical equation [79] is used,

$$V_{DS,sat(sc)} = 0.04 + \eta(L_g v_{sat})^{\frac{1}{3}} V_{DS,sat(lc)} \tag{3.22}$$

where, $V_{DS,sat(lc)} = V_{GS} - V_{th(lc)}$ is drain saturation voltage for long channel device, η is an adjusting parameter and v_{sat} is the saturation velocity. To limit $V_{DS,sat(sc)}$ at $V_{DS,sat(lc)}$, the following expression is used.

$$V_{DS,sat} = \frac{1}{2} V_{DS,sat(sc)}(1 + tanh(5V_{DS,sat(lc)})) + \frac{1}{2} V_{DS,sat(lc)}(1 - tanh(5V_{DS,sat(lc)})) \tag{3.23}$$

In order to provide a continuous expression, the effective drain voltage is calculated as,

$$V_{DS,eff} = V_{DS,sat} + \frac{1}{2}\left(V_{DS} - V_{DS,sat} + \phi_t - \sqrt{(V_{DS} - V_{DS,sat} + \phi_t)^2 + 4\phi_t V_{DS,sat}}\right) \tag{3.24}$$

3.3 Channel Length Modulation

The depletion region between the channel and drain terminal results in the reduction of channel length. The effective channel length can be expressed as [76],

$$L_{eff} = L_g - \sqrt{\frac{\kappa\epsilon_s\zeta}{qN_D}(1 + tanh(10\zeta))} \tag{3.25}$$

where, $\zeta = V_{DS} - V_{DS,sat}$, κ is the adjusting parameter and $V_{DS,sat}$ is the saturation drain voltage. L_{eff} is reduced to L_g for $V_{DS} < V_{DS,sat}$.

3.4 Mobility Degradation

To incorporate mobility degradation with both lateral and vertical field in the core transport model, the effective mobility is defined as,

$$\mu_{eff} = \frac{\mu_1}{\left[1 + (\frac{\mu_1 V_{DS,eff}}{v_{sat}L})^{\sigma}\right]^{\frac{1}{\sigma}}} \tag{3.26}$$

where σ is a constant parameter, v_{sat} is the saturation velocity μ_1 is the vertical field induced mobility degradation which can be described as,

$$\mu_1 = \frac{\mu_0}{1 + \frac{1}{2}\theta(V_{GS} - V_{FB})(1 + tanh(2(V_{GS} - V_{FB}))} \tag{3.27}$$

where, μ_0 is the low field mobility and θ is the mobility degradation coefficient.

3.5 Schottky Barrier in Contacts

The influence of schottky barrier height in source drain contact on the output characteristics of GaN NW JL MOSFET has been observed in experimental study [71]. The existence of schottky barrier source/drain contact forces the device to be turned on at higher V_{DS} than usual, dictated by the height of the schottky barrier. Incorporating the impact of source/drain Schottky contact in the transport formulation, the drain current expression can be obtained as,

$$I_{D,SB} = \frac{1}{2}\left(1 + tanh(5(V_{DS} - \phi_B))\right)\frac{\mu_n}{L}\int_{V_S}^{V_D} Q_n(V_{GS})dV_z \tag{3.28}$$

where, ϕ_B is the Schottky barrier height in source/drain contact whose value has been taken from [71].

3.6 Parasitic Resistance

To incorporate the series resistance effect in drain current model, the total resistance (R_t) has been written as the summation of the channel resistance (R_{ch}) and parasitic ones (R_s at source side and R_d at drain side).

$$R_t = \frac{V_{DS}}{I_D} = R_{ch} + R_s + R_d \tag{3.29}$$

Considering that $I_{D,no\ R_{s/d}} = \frac{\mu_n}{L}\int_{V_S}^{V_D} Q_n(V_{GS})dV_z$ and $R_{ch} = \frac{V_{DS}}{I_{D,no\ R_{s/d}}}$, (3.29) can be written as,

$$\frac{V_{DS}}{I_D} = \frac{V_{DS}}{\frac{\mu_n}{L}\int_{V_S}^{V_D} Q_n(V_{GS})dV_z} + (R_s + R_d) \tag{3.30}$$

Upon incorporating SCE correction, channel length modulation, velocity saturation, mobility degradation, parasitic resistance and Schottky barrier height in source/drain contacts, the final drain current can be obtained as,

$$I_D = \left[\frac{1}{\frac{1}{2}\Big(1 + tanh\Big(5(V_{DS} - \phi_B)\Big)\Big)I_{D0}} + \frac{(R_s + R_d)}{V_{DS,eff}}\right]^{-1} \tag{3.31}$$

where, $I_{D0} = \left(\frac{\mu_{eff}}{L_{eff}}\int_{V_S}^{V_{DS,eff}} Q_n\Big(V_{GS(eff)}\Big)dV_z\right)$.

Table 3.1 presents certain material and device parameters used in this work.

Chapter 4

Simulation Model Development

Since simulation can reduce the testing time drastically along with reduction of cost involved with the fabrication process of the device, use of different simulator for investigation of semiconductor devices has become ubiquitous. Instead of focusing on the details on numerical simulation techniques for Junctionless FET, this work will use numerical tool in an effective way to validate the results obtained from proposed analytical model. The simulation model used in this work is Silvaco ATLAS which will be discussed in this chapter. In addition, a comprehensive discussion on various commands and their meaning will also be presented in this chapter.

4.1 Silvaco ATLAS

Technology Computer Aided Design (TCAD) tools are effective to be used for automation of electronic device design and allows modeling of device fabrication and operation. These tools are widely used in semiconductor device simulation for prediction, analysis and testing purpose. Device fabrication modeling includes modeling of different process steps including ion implantation and diffusion. TCAD is also useful in simulation of the behavior of electronic devices and modeling them based on their underlying fundamental physics. Many TCAD tools are available at present that provide facilities to simulate wide number of semiconductor devices.

Silicon Valley Company (SILVACO) is a leading vendor in TCAD. SILVACO has developed a number of exceptional CAD simulation tool to aid in semiconductor process and

device simulation. In addition, SILVACO has an extended support team for assistance with broad area of semiconductor technologies. Accurate simulation of semiconductor device is critical for industry and research environments. The ATLAS device simulator from SILVACO Inc. is specifically designed for 2-D and 3-D modeling to included electrical, optical and thermal properties within semiconductor device. ATLAS provides an integrated physics-based platform to analyze DC, AC and time-domain responses for all semiconductor-based technologies. The powerful input syntax allows the user to design any semiconductor device using both standard and user-defined material of any size and dimension. Furthermore, ATLAS offers a number of useful device examples to assist one's unique design.

Figure 4.1 presents the types of information that flows in and out of ATLAS. Most ATLAS simulations use two input files. The first input file is a text file containing commands for ATLAS to execute. The second input file is a structure file defining the structure that will be simulated. ATLAS produces three types of output files. The first type of output file is runtime output that provides the progress and the error and warning messages as the simulation proceeds. The second type of output file is the log file storing all terminal voltages and currents from the device analysis. The third type of output file is the solution file that stores 2-D and 3-D data pertaining to the values of solution variables within the device at a given bias point [80].

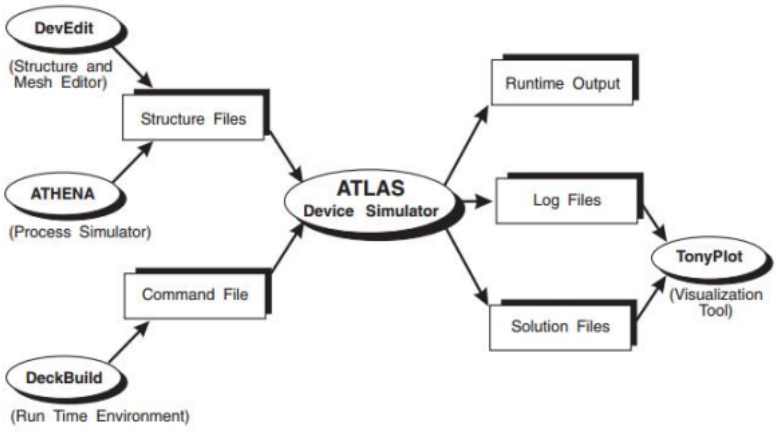

Figure 4.1: *ATLAS inputs and outputs*

Table 4.1: ATLAS command groups

Groups	Statements
Structure Specification	Mesh Region Electrode Doping
Material Models Specification	Material Model Contact Interface
Numerical Method Selection	Method
Solution Specification	Log Solve Load Save
Results Analysis	Extract Tonyplot

4.1.1 ATLAS Commands

In order to simulate semiconductor device, a list of commands has to be delivered to ATLAS. These statements have to follow a certain order so that ATLAS can generate the device after execution. To run ATLAS in the Deckbuild environment, the user must first call the ATLAS simulator with the command,

go atlas

Once ATLAS is called there is a syntax structure that must be followed in order for ATLAS to execute the command file successfully. Table 4.1 shows a list of primary group and statement structure specifications. Although there are a few exceptions, the input file statements follow general format of,

$< statement >$ $< parameter >=< value >$

The order in which statements occur in an ATLAS input file is important. There are five groups of statements that must occur in the correct order. Otherwise, an error message will appear, which may cause incorrect operation or termination of the program. For example, if the material parameters or models are set in the wrong order, then they may not be used in the calculations. The order of statements within the mesh definition, structural definition and solution groups is also important.

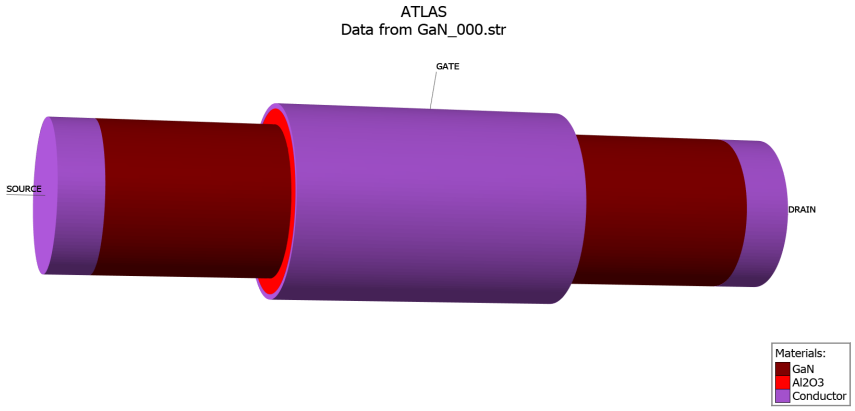

Figure 4.2: *GaN NW JL MOSFET 3D structure for TCAD simulation*

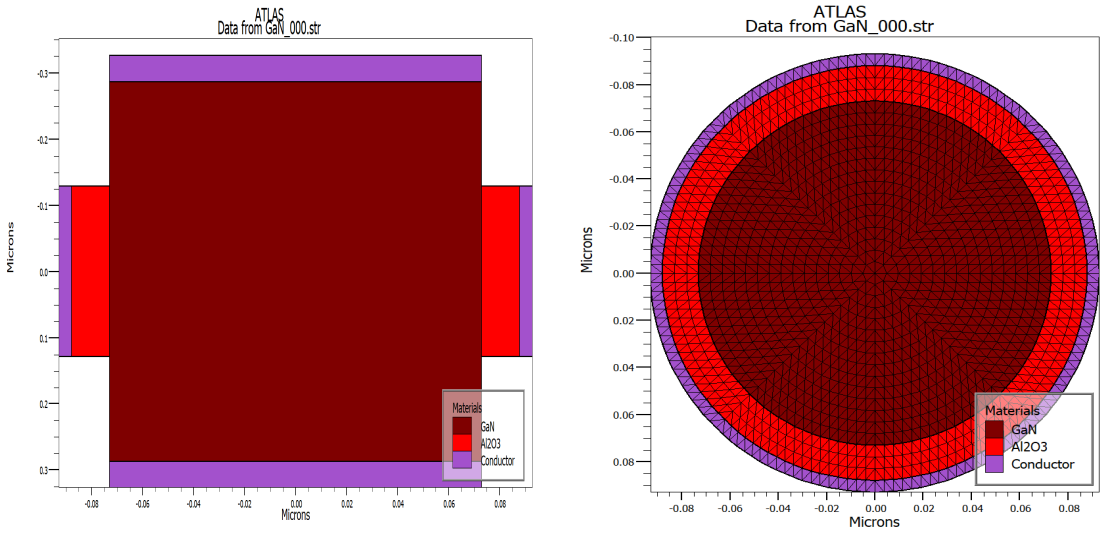

Figure 4.3: *2D Cross-section of GaN NW JL MOSFET along (a)transport direction (b)radial direction*

4.1.2 Structure and Model Development

In order to specify a device structure the mesh, region, electrodes and doping are explicitly defined for simulation. Figure 4.2 and figure 4.3 present the 3D structure and 2D cross section of *GaN* NW JL MOSFET created in the ATLAS simulator. The device created in this manner can then be simulated through incorporation of the desired physical models and numerical methods. Only the necessary steps for the development of simulation environment will be discussed here for readability.

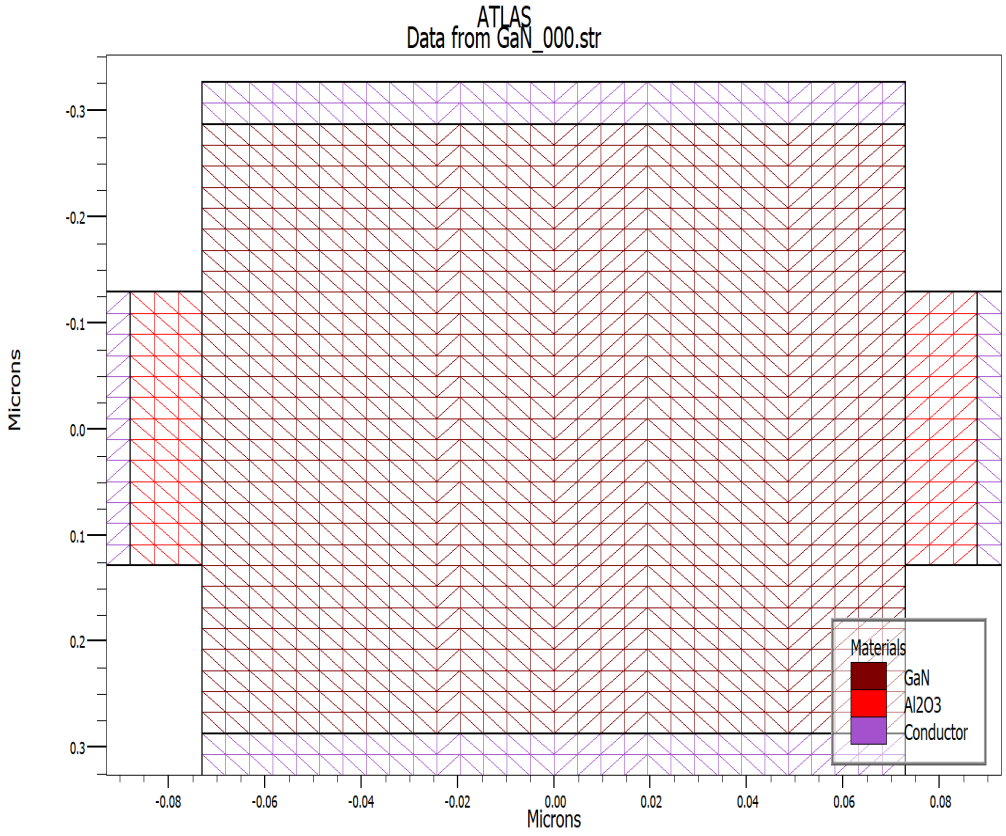

Figure 4.4: *Mesh points of GaN NW JL MOSFET*

4.1.2.1 Mesh

The mesh is defined as the grid of horizontal and vertical lines spanning the dimension of the device. Similar to finite element simulation, this inverted cartesian gridlines area is used to define data points and solution points. For 2-D device simulation only the xy grid definition is sufficient where x-axis spans from left to right and y axis encompasses from bottom to top. The reason for the inverted y-axis is that the manufacturing co-ordinates are usually described as depth below the surface. All coordinates are entered in microns. The general format of defining the mesh is given below.

$mesh \quad space.mult =< value >$

$x.mesh \quad location =< value > \quad spacing =< value >$

$y.mesh \quad location =< value > \quad spacing =< value >$

The *space.mult* parameter value is used as a scaling factor for the mesh created by the $x.mesh$ and $y.mesh$ statements. The default value is 1. Values greater than 1 will create a globally coarser mesh for fast simulation. Values less than 1 will create a globally finer mesh for increased accuracy. The $x.mesh$ and $y.mesh$ statements are used to

specify the locations in microns of vertical and horizontal lines respectively, together with the vertical or horizontal spacing associated with that line. At least two mesh lines must be specified for each direction. ATLAS automatically inserts any new lines required to allow for gradual transitions in the spacing values between any adjacent lines. The x.mesh and y.mesh statements must be listed in the order of increasing x and y. Both negative and positive values of x and y are allowed.

However, for 3-D cylindrical structure such as NW MOSFET, the mesh is defined in a different way. Although quasi-3D cylindrical structure in Atlas2D can be modeled through specification of the cylindrical parameter on the $MESH$ statement, it has the drawback that the solution is independent on the angle around axis of rotation. To circumvent this limitation, Atlas3D comes into play where $CYLINDRICAL$ parameters enable to create a general cylindrical structure. When specifying the CYLINDRICAL parameter, one must now specify the structure in terms of radius, angle, and cartesian Z coordinates.

There are three mesh statements analogous to those used for general structures that are used to specify mesh in radius, angle and Z directions. The R.MESH statement is used to specify radial mesh. The A.MESH statement is used to specify angular mesh. The Z.MESH statement is used to specify mesh in the Z direction.A general format for defining mesh of cylindrical structure is given below,

$MESH \quad THREE.D \quad CYLINDRICAL$

$R.mesh \quad location =< value > \quad spacing =< value >$

$A.mesh \quad location =< value > \quad spacing =< value >$

$Z.mesh \quad location =< value > \quad spacing =< value >$

Here, the $R.MESH$ lines are similar to the familiar $X.MESH$, $Y.MESH$, and $Z.MESH$ except the $R.MESH$ locations and spacing are radial relative to the Z axis in microns. The locations and spacing on the $A.MESH$ lines specify locations and spacing in degrees of rotation about the Z axis. The $Z.MESH$ lines are exactly the same as have been already discussed. Figure 4.4 shows the mesh points generated in ATLAS3D for GaN NW JL MOSFET

4.1.2.2 Region

The region statement is used to separate the initial mesh statement into distinct blocks and sets the initial material parameters that can be referred to later by region number. Once the mesh is specified, every part of it must be assigned a material type using region statement. The general syntax of this command is,

$region \quad no =< integer > \quad material =< material > \quad < position \quad parameters >$

Region numbers must start at 1 and are increased for each subsequent region statement. ATLAS allows the user to define up to 200 different regions. The position parameters are specified in microns using the $x.min$, $x.max$, $y.min$ and $y.max$ parameters for 2D device and $R.min$,$R.max$,$A.min$,$A.max$,$Z.min$ and $Z.max$ parameters for 3D device. If the position parameters of a new statement overlap those of a previous region statement, the overlapped area is assigned as the material type of the new region.Make sure that materials are assigned to all mesh points in the structure. The material type relates physical parameters with the materials assigned to the mesh. The important material parameters for most standard semiconductors are already defined by ATLAS and therefore do not require any changes.

4.1.2.3 Electrode

Electrodes are the external electrical contacts. Once the regions are set, the electrodes must be assigned to the desired region so that it can be electrically analyzed. The electrodes can be assigned to any region or portion of a region. ATLAS has some fixed names for electrodes e.g. anode, cathode, gate, source and drain. The following statements were used to define these parameters.

$electrode \quad name =< electrode \quad name > \quad < position \quad parameters >$

The position parameters are specified in microns using the $x.min$, $x.max$, $y.min$ and $y.max$ parameters for 2D device and $R.min$,$R.max$,$A.min$,$A.max$,$Z.min$ and $Z.max$ parameters for 3D device. ATLAS allows the user to specify up to 50 electrodes. Multiple electrode statements may have the same electrode name. Nodes that are associated with the same electrode name are treated as being electrically connected.

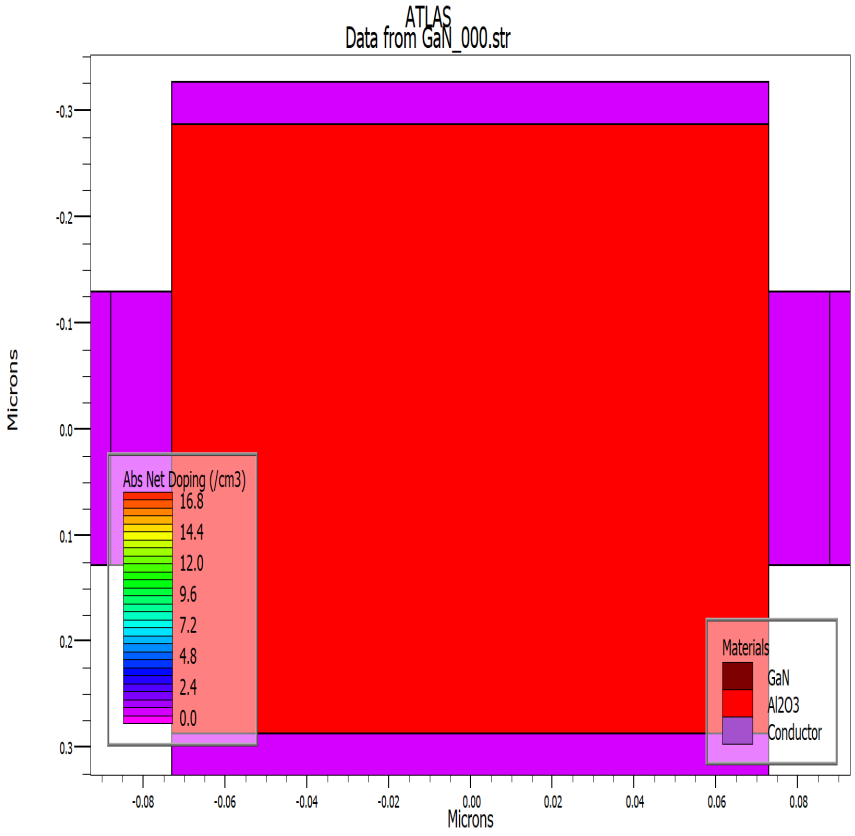

Figure 4.5: *Net doping in different regions for GaN NW JL MOSFET*

4.1.2.4 Doping

The doping statement is used to assign the doping level within the previously assigned regions. Various properties can be appended to the doping statement to specify how the semiconductor is doped and of whether the region is n or p type. The following statements were used to define doping parameters.

doping $< distribution\_type >$ $< dopant\_type >$ $< position\_parameters >$ $concentration =< value >$

Analytical doping profiles can have Uniform or Gaussian forms. The position parameters $x.min$, $x.max$, $y.min$ and $y.max$ for 2D device and $R.min$,$R.max$,$A.min$,$A.max$,$Z.min$ and $Z.max$ for 3D device can be used instead of a region number. Doping concentration of a particular region can be defined using concentration statement. Figure 4.5 highlights the doping profile in different region of *GaN* NW JL MOSFET.

4.1.2.5 Contact

The *contact* statement is used to specify the work-function of the contact material. To introduce the contacts the following syntax is required.

$contact \quad name =< contact \quad name > \quad workfunction =< value >$

Here name of the contact is given by $contact \quad name$ whereas its work-function is specified by *value*. Instead of specifying the work-function it can also be specified by their name in the *contact* statement for the commonly used contacts like n.polysilicon, p.polysilicon, aluminium, tungsten etc. In this case the statement will be as follows.

$contact \quad name =< contact \quad name > \quad < contact \quad material >$

In order to incorporate parasitic resistance in the contacts following statement can be used,

$contact \quad name =< contact \quad name > \quad resistance =< contact \quad resistance >$

4.1.2.6 Model

The *model* statement is essential to the accurate modeling of a particular phenomenon because it sets flags for ATLAS to indicate the inclusion of different mathematical models, physical mechanisms and other global parameters such as substrate temperature. Statement for models used in this work is as follows.

$model \quad incomplete \quad gansat \quad conmob \quad albrct \quad mobmod \quad print$

The description of different model parameters used in this work is given below,

- *gansat* is used for nitride specific field dependent mobility model. This model is based on a fit to Monte Carlo data for bulk nitride.

- *mobmod* specifies mobility degradation by longitudinal electric field only ($mobmod = 1$) or by both longitudinal and transverse electric field ($mobmod = 2$)

- *conmob* is used for concentration-dependent-mobility. The local electric field, lattice temperature, doping variation, surface and material imperfection inside the device will affect the mobility of the carriers.

- *albrct* is used to model low field mobility proposed by Albrecht et al. [81].

- *print* is used to specify the details of material parameters, constants and mobility models at the start of the run-time output. This is a useful way of checking what parameters values and models are being applied in the simulation

4.1.3 Numerical Method Selection

Numerical methods are used to calculate solutions to semiconductor devices problems. The syntax for method used in this work is given below.

method newton

The *newton* method is useful when the system of equations are strongly coupled and has quadratic convergence. It may however spend extra time solving for quantities which are essentially constant or weakly coupled. It also requires a more accurate initial guess to the problem to obtain convergence.

4.1.4 Output Specification

Several quantities are saved by default within a structure file, for example doping concentration, electron concentration and potential profile. We specified additional quantities such as conduction band potential, valence band potential by using the output statement.

output con.band val.band band.temp band.param

4.1.5 Solution Specification

Once the structure, physical model and numerical methods are set correctly, it is quite easy to extract the solution at each node points. The *solve/save/log* statements are used to create data files in ATLAS simulations. These statements work together to provide data to be analyzed by other functions. The *solve* statement specifies which bias points are to be applied to produce an output. The bias points can be set in a number of different way including step, initial and final value depending on what stimulus is desired. Initial solution can also be achieved by *solve init* statement. The *save* statement is used to save all node point data into an output file. With the data stored in an outfile, it is ready to be displayed so that it can be analyzed. The *log* statement allows all terminal characteristics generated by a *solve* statement to be

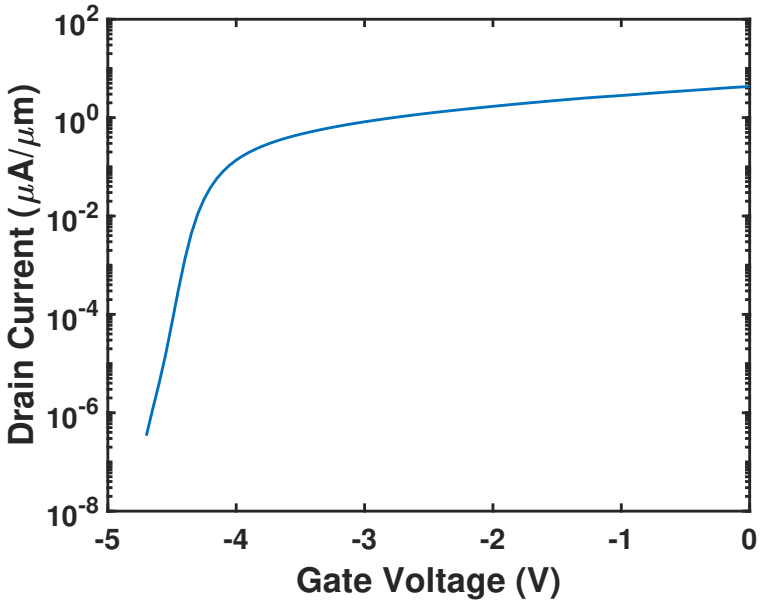

Figure 4.6: *Transfer characteristics of GaN NW JL MOSFET extracted from Silvaco ATLAS simulation for* $V_{ds} = 0.5V$, $N_D = 1e18cm^{-3}$, $R = 73nm$ *and* $t_{ox} = 16\ nm$

saved to a file. It consist of the current and voltages for each electrode during the DC simulations. In transient simulations, the time is saved. Whereas for AC simulations, the conductance, capacitances and the small signal frequency are stored. For instance, to get the solved structure and potential profile of NW JL FET, the following code is enough.

$solve \quad init$

$solve \quad V < electrode \quad name >=< value >$

$save \quad outf = GaN\_JL\_FET\_structure.str$

The ATLAS code for obtaining the drain current for different bias voltages is given below.

$solve \quad v < electrode \quad name >=< value > vstep =< value > vfinal =< value >$

$name =< electrode \quad name >$

$log \quad outf = GaN\_JL\_FET\_current.log$

$save \quad outf = GaN\_JL\_FET\_current.str$

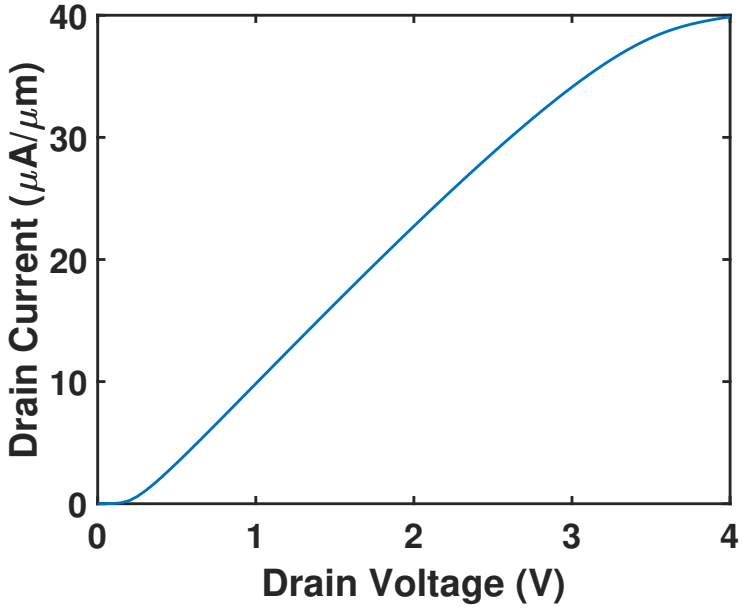

Figure 4.7: *Output characteristics of GaN NW JL MOSFET extracted from Silvaco ATLAS simulation for* $V_{gs} = 0$, $N_D = 1e18cm^{-3}$, $R = 73nm$ *and* $t_{ox} = 16\ nm$

4.1.6 Results

Upon completion of simulation a number of different other parameters can be observed. The *tonyplot* statement is used to start the graphical post-processor tool. The statements in ATLAS to obtain the structure, potential profile and current-voltage characteristics are as follows.

tonyplot $GaN\_JL\_FET\_structure.str$

tonyplot $GaN\_JL\_FET\_current.log$

Figure 4.6 exhibits the transfer characteristics and figure 4.7 presents the output characteristics of GaN NW JL MOSFET extracted from Silvaco ATLAS simulation.

Chapter 5

Results and Discussions

This chapter presents the results pertaining to the electrostatic and transport properties obtained from the proposed analytical model. Furthermore, to confirm the validity of the proposed model, the model results have been compared with experimental data and 3D TCAD simulation results.

Figure 5.1 presents the surface potential, $\phi_s(V_{GS})$ and the center potential,

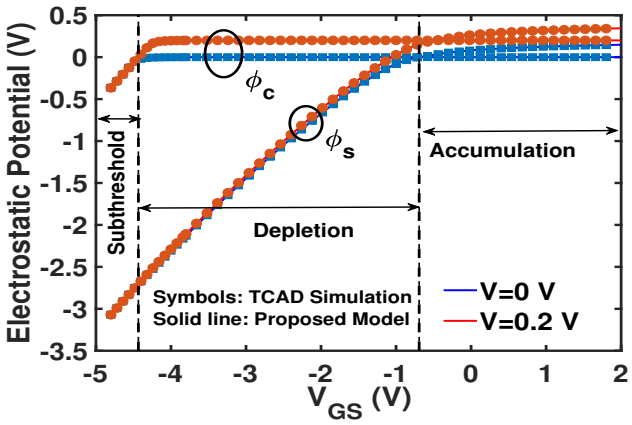

Figure 5.1: *Electrostatic potential at the surface and the symmetry axis of GaN NW JL MOSFET*

$\phi_c(V_{GS})$ for GaN NW JL MOSFET with $N_D = 10^{18}cm^{-3}$, $R = 73nm$, $t_{ox} = 16nm$ and $\phi_{ms} = -0.7V$, for quasi fermi potential values of $V = 0$ and $V = 0.2V$ respectively. The solid line represents present model and the symbols represent numerical solution obtained from 3-D TCAD simulation. As can be observed from the figure, there are three distinct region of operation: subthreshold, depletion and accumulation. Both model and simulation data show excellent agreement in all of these region and their

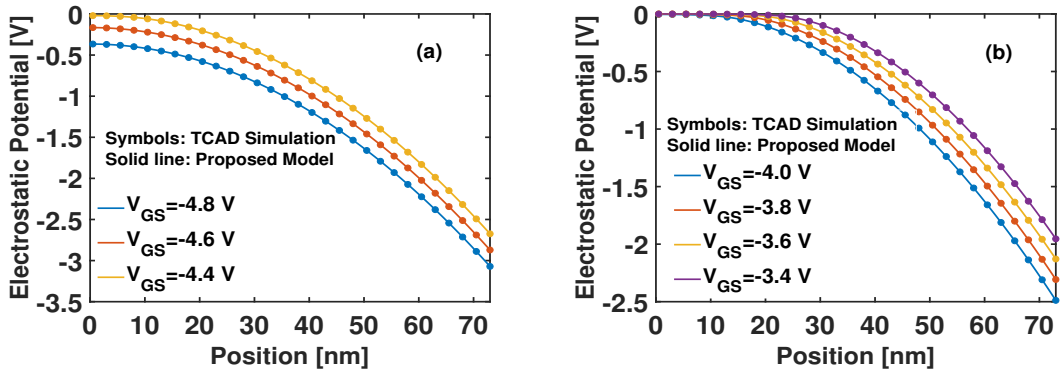

Figure 5.2: *Conduction band potential profile along radial coordinate for gate voltage values (a) below threshold and (b) above threshold*

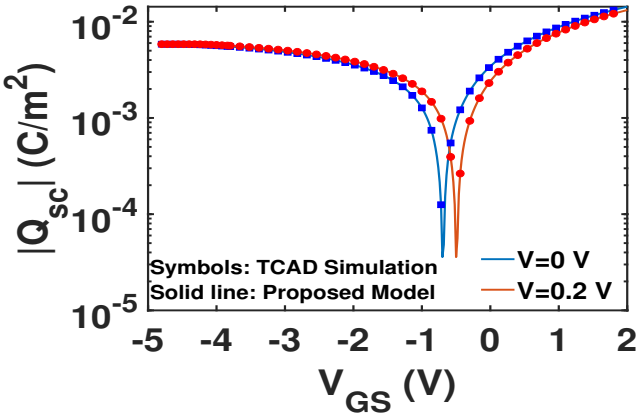

Figure 5.3: *Comparison between simulated and modeled space charge density per unit of area as a function of V_{GS}*

transition is smooth as expected.

The electrostatic potential profile along the radial coordinate for gate voltage V_{GS} values spanning between -4.8V to -3.4V is displayed in Figure 5.2. Both the model and simulation shows good agreement throughout the whole range of applied bias. In the subthreshold region, the NW is completely depleted and the conduction band profile in radial direction can be approximated by parabolic equation as can be seen in figure 5.2(a), but this parabolic relationship is nonexistent in above threshold as shown in figure 5.2(b). Also in above threshold, the depletion width gets smaller and flat potential region in the center of the NW, which initiates mobile carrier accumulation, becomes wider with increasing gate bias.

Figure 5.3 represents the absolute space charge density $|Q_{sc}|$ per unit area as a function of gate voltage. It may be worth mentioning that $Q_{sc} > 0$ in depletion and

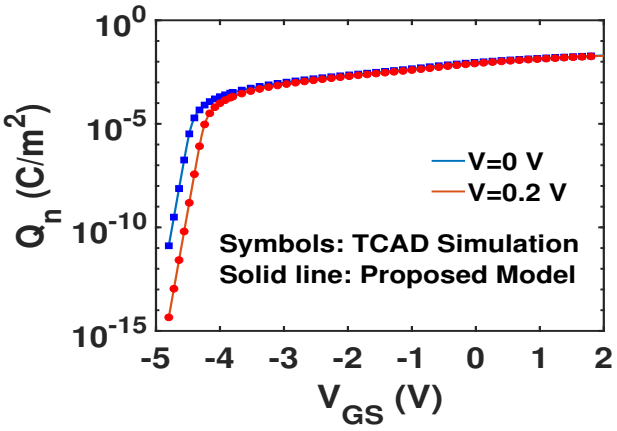

Figure 5.4: *Variation of mobile carrier density per unit of area as a function of* V_{GS}

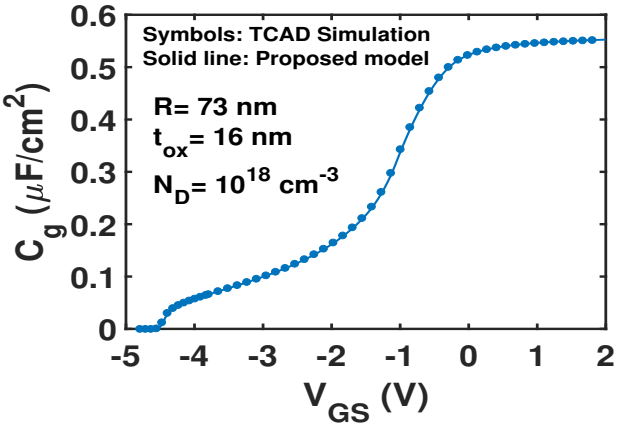

Figure 5.5: *Gate capacitance per unit area as a function of* V_{GS}

$Q_{sc} < 0$ in accumulation which result into a wiggle at $V_{GS} = V_{FB} + V$ in the log plot.

The mobile carrier density Q_n per unit area is portrayed in figure 5.4 for two values of quasi fermi level $V = 0$ and $V = 0.2V$ respectively. The results obtained from TCAD simulation shows excellent agreement with model results from subthreshold to strong accumulation.

Figure 5.5 exhibits the gate capacitance per unit area as a function of gate voltage for the GaN NW JL MOSFET. From the curve, it can be observed that the gate capacitance increases rapidly near the threshold voltage. For $V_{GS} > V_T$ gate capacitance continues to increase, but in a lower rate till it reaches oxide capacitance near $V_{GS} = V_{FB}$.

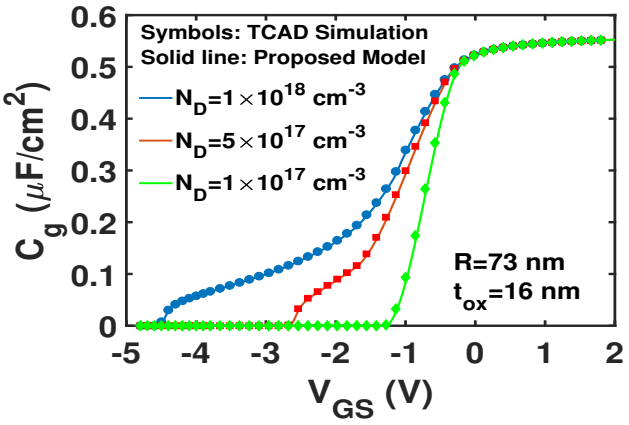

Figure 5.6: *Comparison between simulated and modeled gate capacitance as a function of the V_{GS} for different doping concentrations*

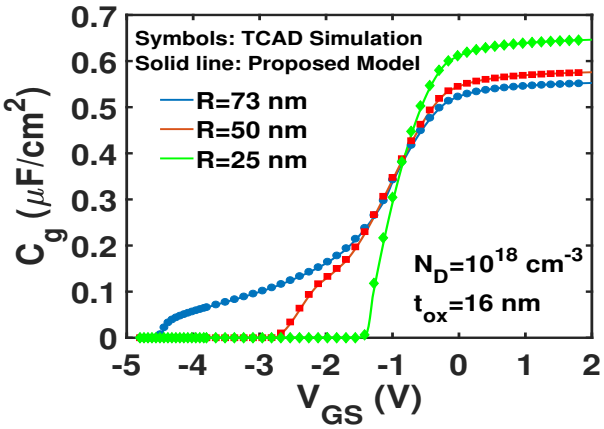

Figure 5.7: *Comparison between simulated and modeled gate capacitance as a function of the V_{GS} for different nanowire radius*

The impact of doping concentration on gate capacitance is presented in figure 5.6. It can be observed from the figure that, as doping concentration is decreased, the threshold voltage shifts in the positive direction. This phenomenon occurs due to the fact that, with higher doping concentration, more negative gate voltage is required to completely deplete the NW and hence threshold voltage becomes more negative. At doping concentration $N_D = 10^{17} cm^{-3}$ the threshold voltage becomes almost equal to flat band voltage V_{FB}.

The variation of gate capacitance with NW radius is portrayed in figure 5.7. As the NW radius becomes smaller, the gate control over the NW becomes tighter which results in the shift of threshold voltage in the positive direction. It can also be observed that the maximum gate capacitance is higher for smaller radius which is due to the

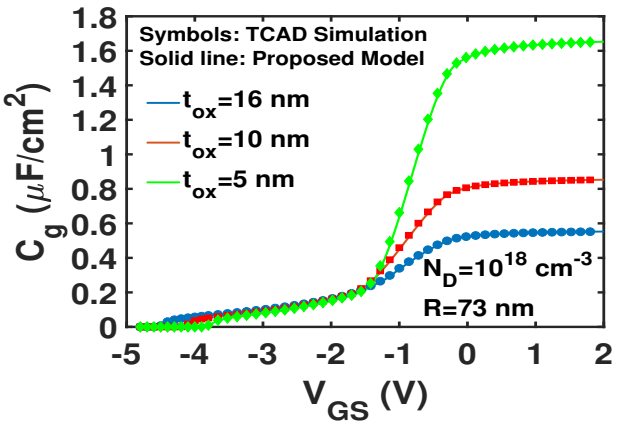

Figure 5.8: *Comparison between simulated and modeled gate capacitance as a function of the V_{GS} for different oxide thickness*

fact that C_{ox} depends on the NW radius and with smaller radius, C_{ox} becomes larger.

The influence of oxide thickness on the gate capacitance is shown in figure 5.8. The oxide thickness has little impact on the threshold voltage, but it changes the maximum gate capacitance significantly. This happens due the fact that the oxide capacitance has logarithmic dependence on the oxide thickness. Since oxide thickness is only a fraction of NW radius, slight change of oxide thickness creates a large variation in value of the logarithmic term in oxide capacitance and hence the maximum capacitance changes significantly.

The variation of long channel threshold voltage with the variation of physical device parameters such as doping concentration, NW radius and oxide thickness as calculated from (2.33) is displayed in figure 5.9. The threshold voltage of GaN NW JL FET shifts towards positive direction as doping concentration or NW radius or oxide thickness decreases. As the doping concentration falls below $10^{17}cm^{-3}$, the threshold voltage approaches towards flat band voltage V_{FB}. Since V_{FB} depends on metal-semiconductor work function difference, ϕ_{ms}, by choosing appropriate metal, positive V_{FB} can be obtained which can ensure enhancement mode operation for moderate to light doping concentration.

Figure 5.10(a) shows the transfer characteristics of GaN NW JL MOSFET obtained from the proposed analytical model. The current densities are normalized by

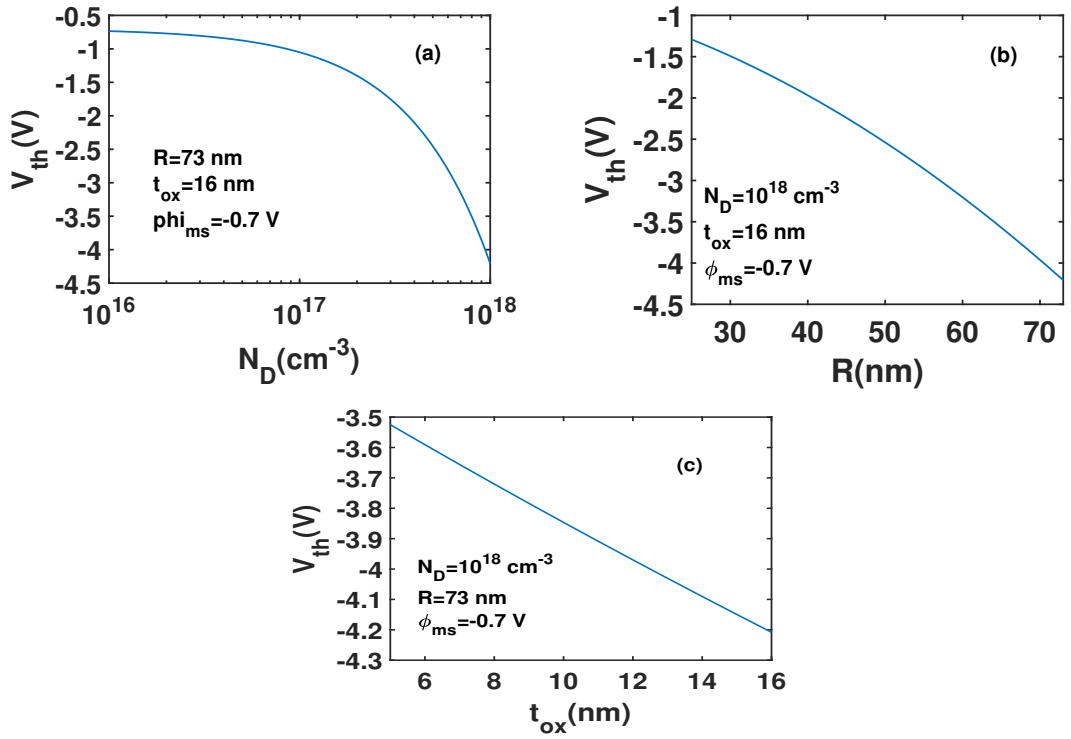

Figure 5.9: *Threshold voltage variation with (a) doping concentration (b) NW radius (c) oxide thickness*

NW circumference. The transfer characteristics extracted from the model shows good agreement with the experimental data. The device presents a sharp turn on behavior in the transfer characteristics with an average subthreshold slope (SS_{avg}) of 68 mV/dec over three decades of drain current and DIBL of 27 mV/V. The large NW radius necessitates a negative gate bias to fully deplete the channel and hence responsible for the depletion mode threshold voltage ($V_{th} = -4.2V$).

Figure 5.10(b) displays the transconductance (g_m) of GaN NW JL MOSFET extracted from the proposed model. The peak g_m occurs at 10.5 $\mu S/\mu m$ for $V_{DS} = 2.5V$.

The output characteristics of GaN NW JL MOSFET extracted from the proposed model is portrayed in Figure 5.11(a). The output characteristics present good saturation with V_{DS}, but an offset voltage exists in the turn on region implying the presence of Schottky barrier at the contacts. The output characteristics obtained from the model through the incorporation of channel length modulation, velocity saturation and source/drain Schottky barrier effect presents good agreement with experimental results.

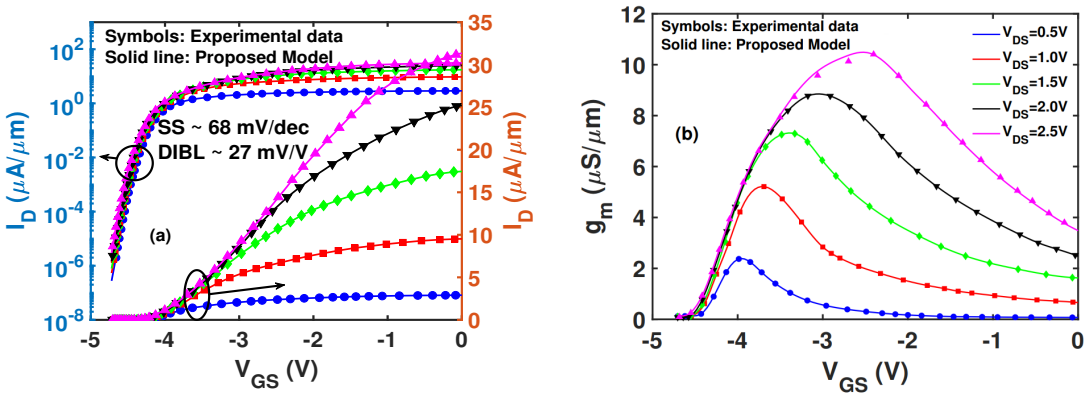

Figure 5.10: *(a) Transfer characteristics and (b) transconductance for different V_{DS}. The device parameters are $N_D = 10^{18}\ cm^{-3}$, $R = 73\ nm$, $t_{ox} = 16\ nm$ and $L_g = 274\ nm$. The experimental data has been extracted from [71].*

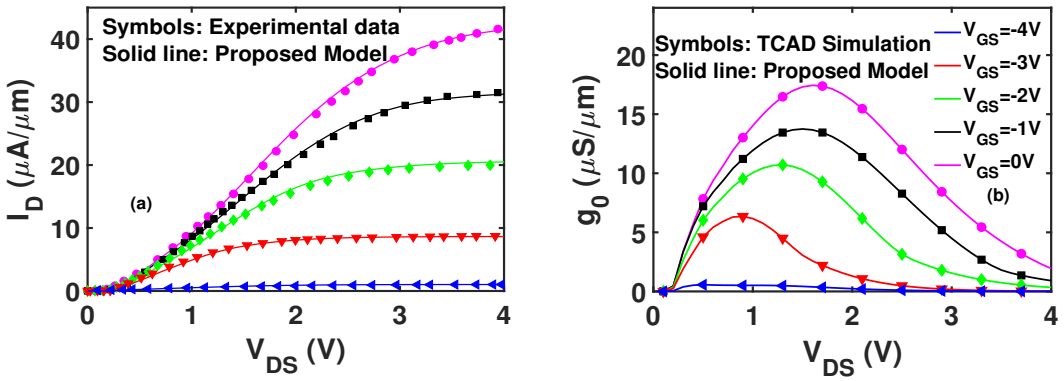

Figure 5.11: *(a) Output characteristics and (b) output conductance for different V_{GS}. The device parameters are $N_D = 10^{18}\ cm^{-3}$, $R = 73\ nm$, $t_{ox} = 16\ nm$ and $L_g = 274\ nm$. The experimental data has been taken from [71].*

Figure 5.11(b) presents the output conductance of GaN NW JL MOSFET extracted from the proposed model. Due to the presence of source/drain Schottky contact, the output conductance increases from zero at low drain voltage, reaches a peak value and becomes zero at high drain voltage due to near saturation of drain current.

Figure 5.12(a) displays the variation of transfer characteristics with NW doping. As the doping concentration decreases the threshold voltage shifts towards higher gate bias. In addition, the peak transconductance occurs at larger gate voltage as shown in figure 5.12(b).

The transfer characteristics of GaN NW JL MOSFET for different NW radius is exhibited in figure 5.13(a). In this work we have considered a good quality in-

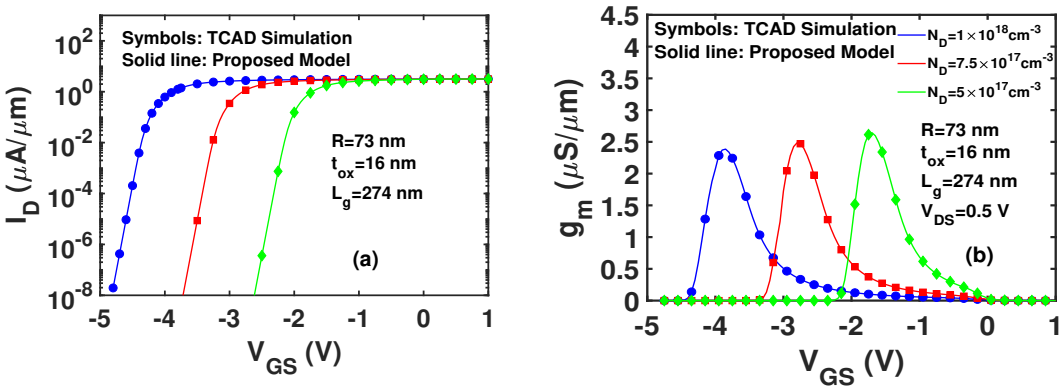

Figure 5.12: *(a) Transfer characteristics and (b) transconductance for different nanowire doping.*

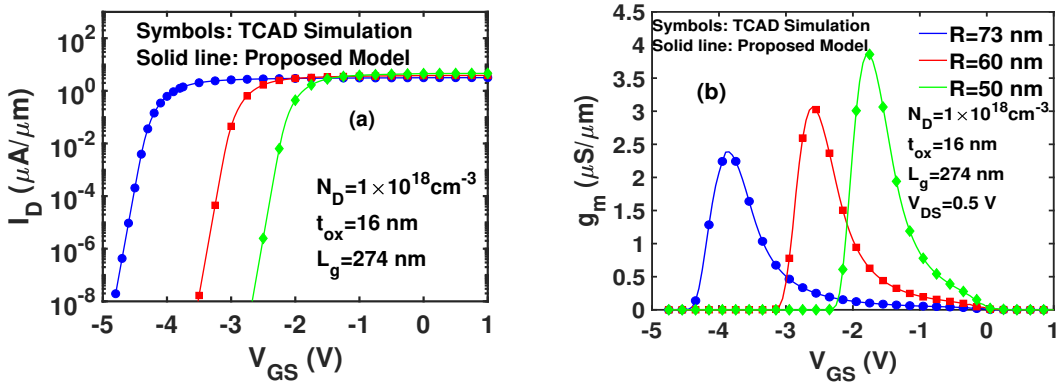

Figure 5.13: *(a) Transfer characteristics and (b) transconductance for different nanowire radius.*

terface between Al_2O_3 and GaN which can be achieved in practice by taking GaN nanowire with m-plane sidewall and passivating the Al_2O_3/GaN interface with forming gas [71].Besides, for large nanowire diameter, the probability of formation of hexagonal nanowire with m-plane area is higher, which subsequently reduces the interface trap. Moreover, the surface induced effects in GaN nanowire such as fermi level pinning can be overcome through ultraviolet radiation [82]. Hence, in the proposed model, the variability of interface trap density with nanowire radius has been considered to be insignificant. This is also evident in figure 5.13(a) and figure 5.13(b) as the transfer characteristics and transconductance are consistent with the nanowire radius. However, if the nanowire diameter is reduced significantly, the nanowire becomes rounder and less hexagonal, so m-plane area is reduced which increase interface traps. In that case the variability of interface traps needs to be incorporated in the proposed model to achieve higher accuracy.

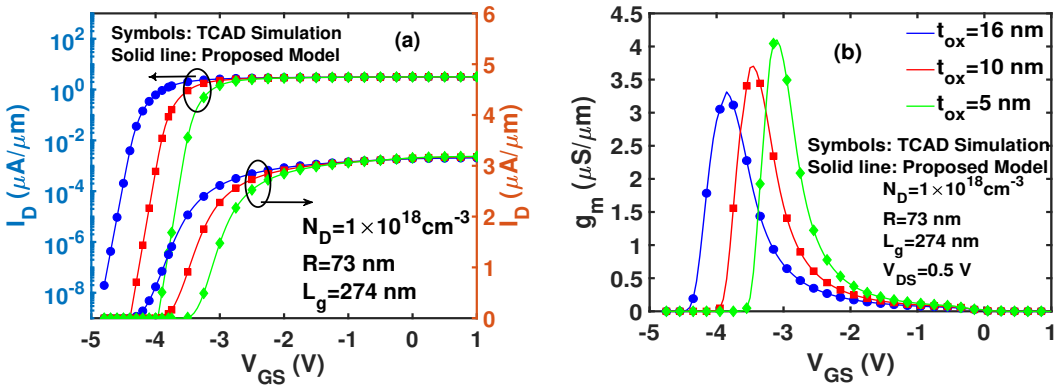

Figure 5.14: *(a) Transfer characteristics and (b) transconductance for different oxide thickness.*

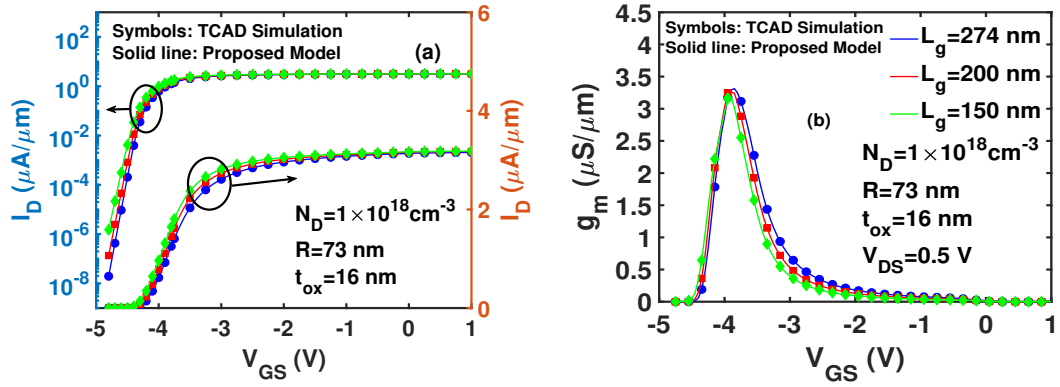

Figure 5.15: *(a) Transfer characteristics and (b) transconductance for different gate length.*

The impact of gate oxide thickness on transfer characteristics and transconductance of GaN NW JL MOSFET is displayed in figure 5.14. An increase in the gate dielectric thickness induces both a decrease in the threshold voltage and a degradation of the current above threshold. The transfer characteristics for different oxide thickness intersect at the same gate voltage corresponding to the flat band voltage i.e. $V_{GS} = V_{FB}$. This interesting property can be understood considering that at flat-band, the semiconductor is at equilibrium and ignores the presence of the gate. This property could be useful to overcome random gate dielectric thickness fluctuation [83].

Figure 5.15 presents the impact of channel length variation on the transport properties of GaN NW JL MOSFET. Reduction of the gate length results in more prominent short channel effect which degrades the threshold voltage and subthreshold slope of the device as will be observed later.The SCE, parasitic resistance and schottky barrier

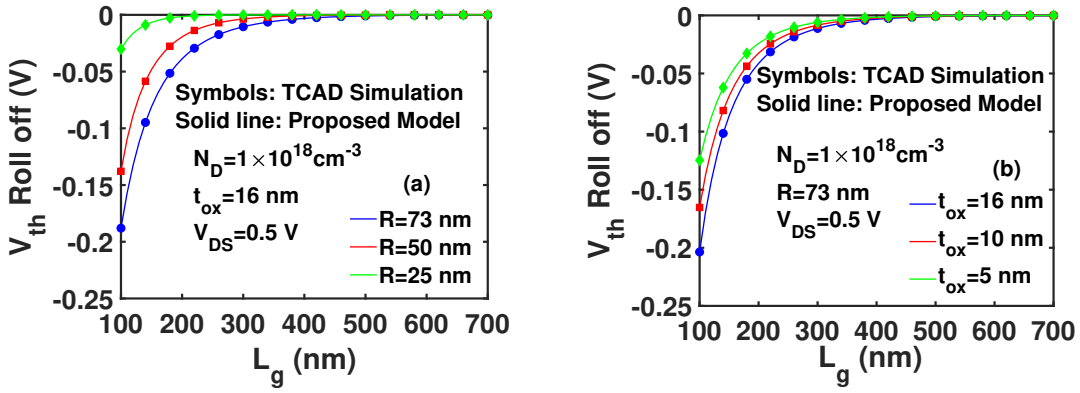

Figure 5.16: *Variation of threshold voltage roll off with channel length for various (a) nanowire radius and (b) oxide thickness.*

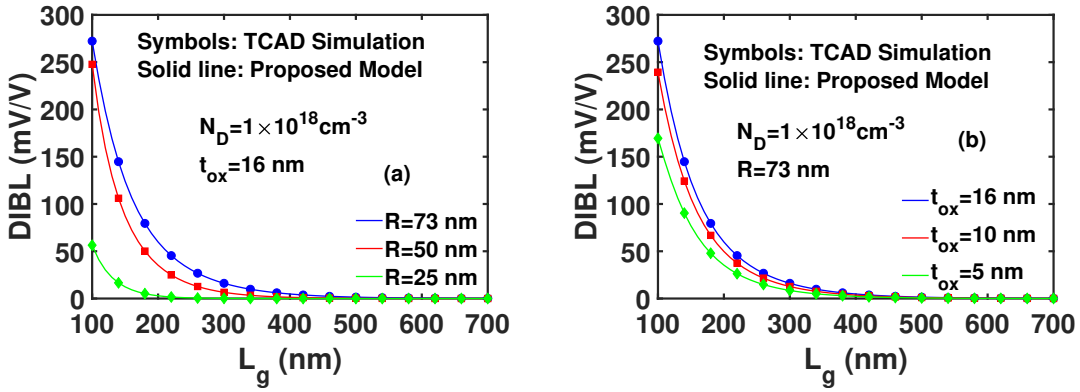

Figure 5.17: *Variation of DIBL with channel length for various (a) nanowire radius and (b) oxide thickness.*

in source/drain contact, incorporated in the proposed model, limit the maximum on current that can flow through the NW JL MOSFET. Hence, the variability of current level is very small despite substantial reduction of channel length.

The influence of NW radius and oxide thickness on threshold voltage of short channel GaN NW JL MOSFET is depicted in figure 5.16. The threshold voltage decreases for reduction of channel length. The threshold voltage degrades further in short channel device with increase in NW radius or oxide thickness due to reduction of gate control over the channel for wider NW or thicker oxide.

Figure 5.17 portrays the variation of DIBL with gate length for different NW radius and oxide thickness. As the channel length shrinks, the DIBL increases due to severity of short channel effect. Short channel effect also becomes prominent for larger NW

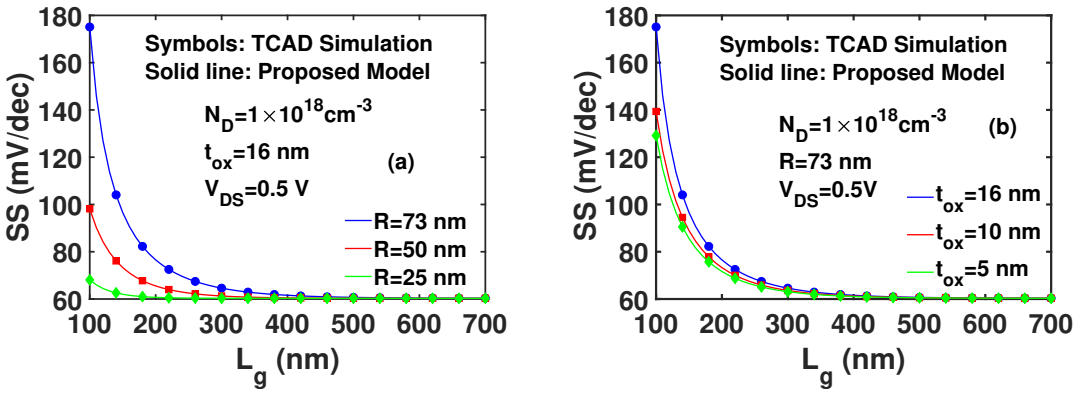

Figure 5.18: *Variation of subthreshold slope with channel length for various (a) nanowire radius and (b) oxide thickness.*

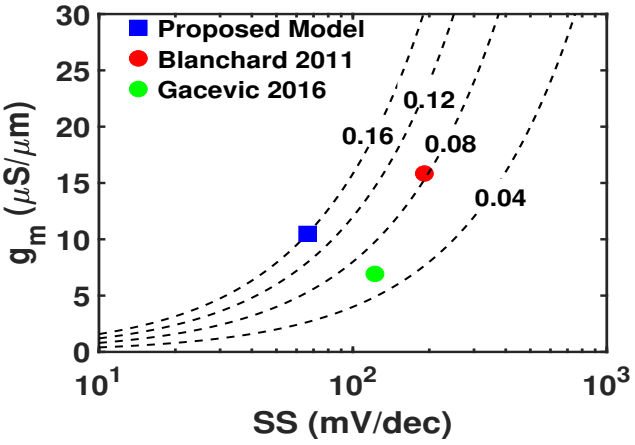

Figure 5.19: *Benchmark plot of g_m versus SS for GaN NW JL MOSFET. The square represents the g_m in this work which has been compared with Blanchard 2011 [69] and Gacevic 2016 [70]. The dashed lines are the constant g_m/SS contour. The device parameters are $N_D = 10^{18}\ cm^{-3}$, $R = 73\ nm$, $t_{ox} = 16\ nm$ and $L_g = 274\ nm$.*

radius or thicker gate oxide which result in the degradation of DIBL.

The impact of gate length on subthreshold slope (SS) for different NW radius and oxide thickness is displayed in figure 5.18. For gate length around 100 nm the device has quite large SS. As the gate length increases, the electrostatic control over the channel increases and the SS of the device approaches to the thermodynamic limit of 60 mV/dec. Also improved short channel performance for smaller NW radius and thinner gate oxide is inferred by the reduction of SS with NW radius and gate oxide thickness.

The comparison of g_m versus average SS for GaN NW JL MOSFET is depicted

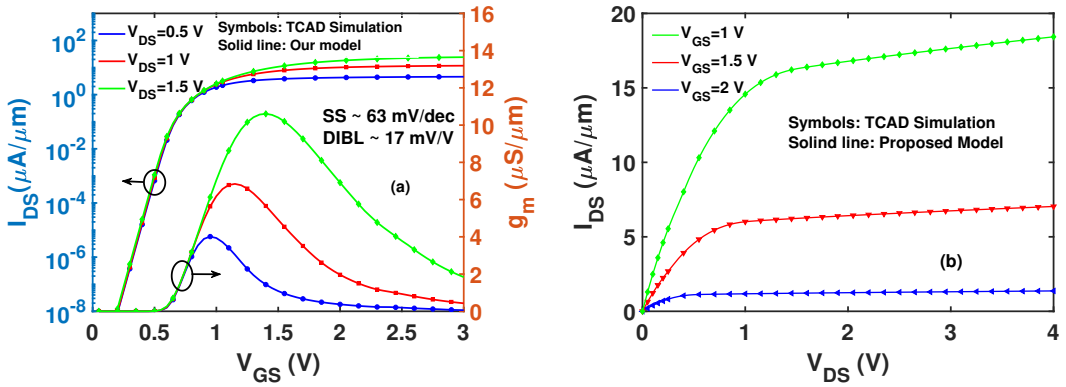

Figure 5.20: *(a) Transfer characteristics and transconductance for different V_{DS} and (b) output characteristics for different V_{GS} of GaN NW JL MOSFET in low voltage normally-off operation. The device parameters set for this operation are $N_D = 10^{18}\ cm^{-3}$, $R = 50\ nm$, $t_{ox} = 10\ nm$ and $L_g = 274\ nm$ and $\phi_{ms} = 1.3V$.*

in figure 5.19. Contours of constant g_m/SS are plotted to present different levels of low power switching efficiency [84]. Compared to previously reported GaN NW JL MOSFETs, the superior switching efficiency of the device used in this work suggests its promising potential in low power applications. The principal limitations of this device for low-power circuits include high saturation drain voltage and negative threshold voltage which can be overcome through optimization of the device design and fabrication process[71].

To further analyze the prospect of GaN NW JL MOSFET in low power application, we have investigated the transport characteristics of the device operated in enhancement mode. This mode of operation can be achieved through tuning the nw radius, oxide thickness and gate metal work function as done in this work. The transfer characteristics highlighted in figure 5.20(a), obtained after setting the device parameters as $N_D = 10^{18}\ cm^{-3}$, $R = 50\ nm$, $t_{ox} = 10\ nm$ and $L_g = 274\ nm$ and $\phi_{ms} = 1.3V$, ensures normally-off operation with $V_{th} = 0.52V$, average subthreshold slope SS_{avg} of 63 mV/dec and $DIBL$ of 17 mV/V. Furthermore, the maximum transconductance extracted at $V_{DS} = 1.5\ V$ from figure 5.20(a) is 10.9 $\mu S/\mu m$ which results in a switching figure of merit Q of 0.18 $(\mu S/\mu m)/(mV/dec)$ and bolsters its potential in low power application. The output characteristics of the normally-off device, illustrated in figure 5.20(b), shows low saturation drain voltage which is desirable for low power application.

Chapter 6

Conclusion

This chapter summarizes the whole work and proposes some unexplored avenue pertinent to this work which can be put under extensive research.

6.1 Summary

In this work, a physically based analytical model of surface potential for GaN NW JL MOSFET has been proposed. The evolution of the proposed model involves the solution of quasi 2-D Poisson's equation in the channel region with appropriate boundary condition. The model includes various device parameters like doping concentration, NW radius, oxide thickness, applied gate bias, flat band voltage etc. The surface potential facilitates the calculation of mobile carrier density which is used to formulate the gate capacitance of the device. In addition, a threshold voltage model for long channel GaN NW JL MOSFET is proposed. The variation of gate capacitance and threshold voltage with various device parameters including doping concentration, NW radius, oxide thickness is thoroughly investigated.

The mobile carrier density extracted from surface potential model is further used to formulate the transport properties of the device. Several non ideal effects including short channel effect, velocity saturation, mobility degradation, channel length modulation, parasitic source drain resistance have been incorporated in the transport model to enhance the robustness of the model. The accuracy and applicability of the proposed

model is bolstered through benchmarking of the model results against experimental data and the results obtained from 3D TCAD simulation. Furthermore, explicit expression of several short channel performance metrics such as threshold voltage roll-off, subthreshold slope and drain induced barrier lowering have been presented. The transport characteristics and short channel performance metrics have been analyzed with the variation of device parameters such as channel length, NW radius and Oxide thickness.

6.2 Suggestion for Future Work

- Reducing the NW radius below 10 nm will cause quantization of mobile carriers in the channel which is basically a quantum mechanical effect (QME). Similar study can be carried out incorporating QME in the channel region. In order to include these effects a self-consistent analysis can be performed by developing a Schrodinger-Poisson solver.

- Interface trap states were ignored in this study, which can be included in future studies.

- Gate tunneling current and leakage performance analysis by quantum mechanical treatment is essential for evaluation of devices as an efficient nanoscale transistor. The proposed can be extended to incorporate this effect.

- This work can be extended to incorporate the device study with modification of device structure which include the use of stack gate and high-κ oxide

List of Publications

- M. I. Khan, I. K. M. R. Rahman and Q. D. M. Khosru, "Surface Potential-Based Analytical Modeling of Electrostatic and Transport Phenomena of GaN Nanowire Junctionless MOSFET," in IEEE Transactions on Electron Devices, vol. 67, no. 9, pp. 3568-3576, Sept. 2020, doi: 10.1109/TED.2020.3011645.

- M. I. Khan, I. K. M. Reaz Rahman and Q. D. M. Khosru, "Analytical Modeling of Capacitance-Voltage Characteristics of GaN Nanowire Junctionless MOSFET," 2020 IEEE 20^{th} International Conference on Nanotechnology (IEEE-NANO), Montreal, QC, Canada, 2020, pp. 67-72, doi: 10.1109/NANO47656.2020.9183461.

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