ADAPTIVE CLARKE TRANSFORMATION BASED THREE-PHASE PLL UNDER AMPLITUDE AND PHASE UNBALANCES IN PRESENCE OF HARMONICS

A thesis submitted in partial fulfillment of the requirement for the degree of
Masters of Science in Electrical and Electronic Engineering

by

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It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Abstract

Precise and fast estimation of the phase information of grid voltages is crucial for grid synchronization of various power electronic devices, which is a research trend in modern smart grid technology. However, the task of instantaneous phase estimation has become difficult as the grid voltages may contain harmonics, DC offset, frequency variations, and voltage unbalances due to an increase in renewable energy penetration to grid, and domestic and industrial non-linear loads. In this dissertation, a fast and accurate instantaneous phase estimation technique is developed to overcome the present limitations in this field.

This dissertation proposes a three-phase phase locked loop (PLL) algorithm relying on adaptive Clarke transformation (ACT) for tracking the phase angle of unbalanced grid voltages associated with harmonics and DC offset. A meticulously tuned band pass filter (BPF) is inserted in each phase to remove harmonics and DC offset. Two separate algorithms are proposed to estimate the amplitudes and the phase-angle deviations of three-phase voltages. Using the estimated amplitudes and phase angle deviations, a set of analytical expressions is derived for the coefficients of Clarke transformation (CT) matrix to make them adaptive under both amplitude and phase unbalances, which is named as ACT. The ACT is capable of generating orthogonal signals from unbalanced three-phase voltages, whereas the conventional CT based on constant matrix fails to do so. After getting the orthogonal voltages, a conventional SRF-PLL is used to track the phase-angles of all three-phases. A phase-correction technique is also developed to make the PLL frequency adaptive without using any frequency feedback loop.

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List of Abbreviations

Abbreviations	**Description**
PV	Photo Voltaic
DPGS	Distributed Power Generation System
RES	Renewable Energy System
DG	Distributed Generation
AC	Alternating Current
DC	Direct Current
DVR	Dynamic Voltage Restorer
APF	Active Power Filter
STATCOM	Static Compensator
UPQC	Unified Power Quality Controller
CUPS	Custom Power Systems
FACTS	Flexible AC Transmission Systems
SVC	Static Voltage Compensator
SSSC	Static Synchronous Series Compensator
UPFC	Unified Power Flow Controller
PLL	Phase Locked Loop
FLL	Frequency Locked Loop
SRF-PLL	Synchronous Reference Frame-PLL

MAF	Moving Average Filter
QT1-PLL	Quasi-Type-1 PLL
CNF	Complex Notch Filter
MCCF-PLL	Multiple Complex Coefficient Filter based PLL
SOGI-PLL	Second Order Generalized Integrator based PLL
CDSC-PLL	Cascaded Delayed Signal Cancellation based PLL
IPT-PLL	Inverse Park Transformation-Based PLL
DDSRF-PLL	Decoupled Double SRF-PLL
FFPS	Fundamental Frequency Positive Sequence
FFNS	Fundamental Frequency Negative Sequence
ACT	Adaptive Clarke Transformation
VCO	Voltage Controlled Oscillator
BPF	Band Pass Filter
PWM	Pulse Width Modulation

List of Symbols

Symbol	Nomenclature
v_a, v_b, v_c	Three-Phase Grid Instantaneous Voltages of Phase 'a', 'b', and 'c', Respectively
v_A, v_B, v_C	Three Phase Voltages Obtained from Each BPF
V_a, V_b, V_c	Amplitudes of Fundamental Voltages of Phases 'a', 'b', and 'c', Respectively
V_A, V_B, V_C	Amplitudes of Three Phase Filtered Voltages
θ_b, θ_c	Phase Angles of Phases 'b' And Phase 'c', Respectively
v_α, v_β	Stationary Frame Orthogonal Signals
ϕ_A	Instantaneous Phase of Phase 'a' Obtained from SRF-PLL
$\Delta\omega$	Frequency Deviation
ϕ_a	Actual Instantaneous Phases of Phase 'a','b', and 'c', Respectively.
θ_F	Phase Error Due to BPF in Case of off-Nominal Frequencies
H_1	Transfer Function of 2nd Order BPF.
T_s	Sampling Time
T	Fundamental Time Period
v_B^A, v_C^A	Instantaneous Magnitude of Phase 'b' and 'c', Respectively at The Zero-Crossing Point of Phase 'a'
v_A^B, v_C^B	Instantaneous Magnitude of Phase 'a' and 'c', Respectively at the Zero-Crossing Point of Phase 'b'

v_A^C, v_B^C	Instantaneous Magnitude of Phase 'a' and 'b', Respectively at the Zero-Crossing Point of Phase 'c'
α_A, α_B, α_C, β_A, β_B, β_C	Coefficients of the CT Matrix
n	Index of Voltage Sample
$\lvert v_A(n) \rvert$	Absolute Value of Instant Voltage Sample

Chapter 1 : Introduction

1.1 Importance

The day-by-day increasing demand for energy and environmental issues of using fossil fuel yield in an increased development of distributed power generation units using renewable energies [1]. Distributed generation system mainly includes wind and PV systems, which are the most growing renewables in the world [2, 3]. The wind and PV systems have low efficiency and their dependency based on both wind and sun are their main drawback. As a consequence, their connection to the utility network can lead to grid instability or even failure without proper control strategies [4]. The distributed power generation system (DPGS) have some requirements and restrictions in order to run over short grid disturbances [5, 6]. Restrictions for renewable energy system (RES) and distributed generation (DG) power quality are given in each country in so called "grid codes" [7, 8]. Operation with certain power factor (close to unity), limited harmonic content of injected current, continuous operation under voltage distortions, etc. are some of the grid requirements for RES [9]. Most of these requirements can be satisfied with proper control of grid connected converter. Therefore, DG and RES are connected to the AC grid through power converters [10, 11].

In DPGS, there are two main control strategies- one is for the input-side converter (e.g, for wind turbines this is an AC-DC converter) and another is for grid-side converter (e.g., for wind turbines this is a DC-AC converter). The input-side controller ensures the maximum power extraction from the input source, generally achieved by using maximum power point tracking algorithm [12]. Moreover, input-side converter protects the input source in case of grid failure. The grid-side converter performs many jobs. It must ensure the quality of output power that is to mitigate voltage dips/swells, flicker, voltage unbalance, harmonics, and transients by controlling the output current. It must control the active power generated to the grid as well as the reactive power exchanged between the DPGS and the grid [13]. Finally, it must play a vital role to synchronize the DPGS with the grid voltage [14].

On the other hand, the power system network at distribution level faces many types of challenges, primarily related to load unbalance, reactive power and current harmonics etc. These issues must be addressed in order to generate and transmit quality power to the

consumers without any disturbance [15, 16]. With the development of sophisticated power electronics technology, lot of custom power devices like dynamic voltage restorer (DVR) [17, 18], active power filters (APF) [19, 20] may be series or shunt type, static compensator (STATCOM) [21, 22], unified power quality controller (UPQC) [23] are widely being used to mitigate power quality problem. Among them DVR, APF, D-STATCOM, UPS etc., known as CUPS (Custom Power Systems), are used to protect against voltage dips, higher harmonics or flicker. There are also devices installed for transmission system support, called flexible AC transmission systems (FACTS), like: STATCOM, SVC, SSSC, UPFC and others [24].

Each of the above-mentioned grid-connected devices has to be precisely synchronized with grid voltage and thus they need accurate control strategies [25]. The controller uses instantaneous phase angle of the grid voltage to produce synchronized reference signal that is used in pulse-width modulation process of the power converters [26]. Therefore, accurate phase angle information of grid voltage is indispensable for proper operation of every grid-connected power converter [27].

Table 1: Grid-connected devices, employing power converters with grid synchronization.

Group of devices	**Applications**
Renewable Energy Sources (RES)	Wind power plants, Photovoltaic plants etc.
Custom Power Systems (CUPS)	UPS, APF, DVR, D-STATCOM, etc.
Flexible AC Transmission Systems (FACTS)	STATCOM, SVC, SSSC, etc.
Loads	DC loads with AC/DC converters.

1.2 Background and Motivation

Many useful methods are available for the estimation of grid phase information. Those methods can be separated into two categories. One is open loop estimation method and another is close loop estimation method. Some of the open loop algorithms are based on Fourier transformation [28-30], least-error squares [31], weighted least-square-estimation [32], gradient estimator [33], notch filter [34], extended Kalman filter [35, 36], demodulation technique [37], and space vector filtering [38, 39] etc. One advantage of the open loop method is that they can track the phase angle faster in comparison with close loop method as additional time delay in feedback system is absent in open loop methods. However, if the system frequency deviates from the

nominal frequency, these methods generate error in phase calculation. To make them frequency adaptive, some advanced methods have been proposed by modifying the existing methods [40-42]. But they add complexity and increase computational burden.

On the other hand, close loop methods such as phase locked loop (PLL), frequency locked loop (FLL) [43, 44] have better performance but slower response. Among the close loop estimation techniques, the most useful algorithm to track the phases is based on the synchronous reference frame PLL (SRF-PLL) for their simplicity and robustness. The conventional SRF-PLL has excellent phase tracking capability and dynamic performance under ideal grid conditions [45, 46]. However, when the grid voltage is unbalanced and distorted, the SRF-PLL can cause oscillation and accuracy problems [47]. Incorporating an in-loop filter or pre-filter in the SRF-PLL can improve the performances of the PLL.

Using a moving average filter (MAF) in the PLL control loop is suggested in [48, 49]. MAF works as low pass filter (LPF), which mitigates the influence of harmonics [50]. However, the open-loop bandwidth of a MAF incorporated PLL is drastically reduced that results in slower dynamic response [51]. To overcome the dynamic problem of MAF-PLL, some advanced MAF based structures are proposed. In [52], MAF-PLL with phase-lead compensator is proposed that reduces the settling time to 1.79 cycles of fundamental period. In [53], another MAF-based PLL named quasi-type-1 PLL (QT1-PLL) is proposed with a feed forward control path to compensate the phase tracking error, which achieves less settling time (1.75 cycles of fundamental period). However, the MAF-PLLs are unable to reject the DC offsets of the grid voltages. A CNF-QT1-PLL is proposed in [54], which adds a complex notch filter along with MAF to improve the PLLs performance. The settling time is further reduced in the CNF-QT1-PLL. However, MAF-PLLs become more complex to implement and produce error in phase estimation in case of frequency deviation, harmonics and DC offset of the grid voltages. In [48], a hybrid in-loop filter based on CNF and *dq*CDSC is used, which shows better dynamics during frequency deviation condition. Other in-loop filtering techniques are multiple complex-coefficient-filter-based PLL (MCCF-PLL) [55], the *dq*-frame delayed signal cancellation operator [56-58], the repetitive regulator [59], which are implemented by considering both filtering capability and dynamic response of the PLL.

Another method to improve the performance of the PLL is using the pre-filtering techniques, which add control strategies before the PLL loop, such as complex-coefficient filter (CCF) [60], multiple second-order generalized integrator based PLL (DSOGI-PLL) [61, 62], multiple

reference frame based PLL (MRF-PLL) [63], MAF [64], DSC operator [57, 58, 65-67]. In [55], a MCCF based SRF-PLL is presented that can extract fundamental positive and negative sequence signals adaptively, but it neglects the dynamic interaction between the SRF-PLL and CCF, which results in error in phase estimation. A solution to the problem is proposed in [60] to enhance the performance of MCCF without additional computational loads. Another effective method, Delayed signal cancellation PLL (DSC-PLL), is proposed recently in [67, 68] using multiple DSC operator that shows good capability in phase estimation. However, the cascading filters require complex calculation and affect the dynamic response. Recently, a signal reforming-based algorithm is used for removing the negative consequences caused by the unbalanced conditions in [69, 70]. The algorithm in [69] uses an amplitude balanced signal generator and a phase balanced signal generator to produce the amplitude and phase balanced FFPS from the unbalanced signals.

1.3 Objectives

The main purpose of this thesis is to develop a phase estimation technique for three-phase voltages in both balanced and unbalanced conditions in presence of harmonics. A conventional SRF-PLL is unable to estimate the phase-angle accurately in presence of harmonics or voltage imbalances. This thesis aims at enhancing the over-all performance under such circumstances.

By using conventional Clarke transformation matrix, it is only possible to transform three-phase balanced system to a stationary frame $\alpha\beta$ system. As a result, conventional SRF-PLL that uses conventional Clarke transformation produces error in phase estimation in case of unbalanced condition. In the proposed method, coefficients of the Clarke transformation matrix have been adaptively updated so that it can directly transform three phase unbalanced voltages to a stationary frame $\alpha\beta$ voltages. As it is known, if the stationary frame $\alpha\beta$ voltages are available, phase angles of three-phase voltages can be easily tracked by using conventional SRF-PLL. The proposed method has also presented two separate algorithms for tracking the amplitudes and phase angle deviations of both amplitude and phase unbalanced three-phase system. The amplitudes and phase angle deviations are needed to calculate the adaptive coefficients of the Clarke transformation matrix.

The objectives of the proposed research are –

- To derive analytical expressions for the coefficients of Clarke transformation matrix for adaptively generating accurate orthogonal voltage signals under amplitude and/or phase unbalanced condition.

- To develop an algorithm for tracking the deviations of the amplitudes and phase angles from the balanced condition.
- To build up a three-phase PLL algorithm relying on adaptive Clarke transformation for tracking the phase angles of all three phases under harmonics and both balanced and unbalanced conditions.

1.4 Methodology

The thesis has been conducted by following several steps as follows.

Firstly, the proposed research has been carried out in MATLAB/Simulink environment. Three-phase fundamental voltages have been produced using three sinusoidal blocks in Simulink. Additional sinusoidal harmonics have been generated based on the IEEE 519 standard [9]. Fundamental voltages and harmonics have been added up to create distorted voltages.

Secondly, three band-pass filters, each per phase, have been used for rejecting the unwanted voltages from the three-phase distorted voltages. An algorithm has been proposed for tracking the amplitudes of the three phases. An additional algorithm has been used to track the phase angle deviations in case of balanced or unbalanced voltages conditions. The estimated value of amplitudes and phase angle deviations have been used to compute the coefficients of the Clarke transformation matrix, which has been used to transform the unbalanced three-phase voltages to orthogonal stationary-frame $\alpha\beta$ signals. The output of the Clarke transformation has been used as the input of a conventional SRF-PLL.

Finally, in the SRF-PLL block, a Park transformation (phase detector) has been used to generate direct and quadrature axis components from the stationary-frame $\alpha\beta$ signals. Then, the q-axis component, which contains the phase error information, has been passed through a proportional-integral (PI) controller that acts as a low pass filter to generate frequency error. The output of the PI controller has been applied to a voltage-controlled oscillator (VCO) to estimate the phase angle of phase ‘a’ that is the reference phase. The phase angles of phase ‘b’ and phase ‘c’ are also estimated without any additional PLL. The performance of the proposed PLL has also been compared with conventional PLL algorithms reported in the technical literature.

1.5 Thesis organization

The thesis entitled "Adaptive Clarke Transformation Based Three-Phase PLL under Amplitude and Phase Unbalances in Presence of Harmonics" is divided into several chapters, which are organized as follows.

In chapter 1, the writing is started by mentioning the importance of estimating phase of three phase voltages and previous works on phase estimation. The objectives of this dissertation are also mentioned to summarize the whole thesis. After that, the methodology of the developed PLL algorithm is presented which describes about adaptive Clarke transformation, amplitude and phase angle deviation estimation, conventional SRF PLL, etc.

Chapter 2 focuses on the review of various common PLL techniques. At first, the basic structure of the PLL is described. Then, the two types of PLL, one is single phase PLL and another is three phase PLL techniques have been presented. Among the single phase PLLs, power based PLL, time delay based PLL, IPT-based PLL, SOGI based PLL are added. Similarly, SRF-PLL, MAF based PLL, SOGI based PLL, DSC-PLL, CCF-PLL, and decoupled SRF-PLL are defined from the three phase PLLs.

In chapter 3, the new developed PLL algorithm is presented in a block diagram to summarize the thesis. At first, a band pass filter is designed to remove harmonics from the input signals. Second, two separate algorithms are developed for amplitude estimation and phase angle deviation estimation of three phase voltages. Finally, a conventional SRF-PLL is constructed to estimate the instantaneous phase angles of all three phases.

The simulation results of the proposed PLL are described in Chapter 4. The results are presented in two categories- first, the performance of the proposed PLL is evaluated without presence of harmonics in input voltages and second, the performance is evaluated in presence of harmonics. The performance of the proposed PLL is also verified by performing some experimental results, which are also included in this chapter.

Chapter 5 concludes the thesis by summarizing the outcome from the thesis and suggesting the future work based on the thesis.

2.1 The Basic Structure of Phase Locked Loop

PLL consists of three parts.

- Phase Detector (PD)
- Loop Filter (LF)
- Voltage Controlled Oscillator (VCO)

The PLL works as basic feedback control system that helps to synchronize between the input and output signals. In this system, The PD tracks the difference in phase between the input and output signal of the PLL and the LF filters out the high order harmonics, disturbances from the error signal. The filtered signal is then forwarded toward the VCO, that generates the output of the PLL. Then, the output is feedbacked to the input of PLL.

The PD, as seen in Fig. 2.1 compares the phase of the input signal $x_i(t)$ against the phase of the VCO output $x_o(t)$ and produces an error signal $v_e(t)$. This error signal is then filtered in order to remove noise and other unwanted components of the input spectrum. The sum of filter output and an additive external control voltage controls the instantaneous VCO frequency. If a VCO input voltage is $e_o(t)$, its output is a sinusoid of frequency ω given by $\omega(t) = \omega_{vco} + ce_o(t)$, where, c is a constant of the VCO and ω_{vco} is the free-running frequency of the VCO. A nonzero output voltage must be provided by the PD, in order to tune the VCO frequency to the input one if the input frequency differs from the VCO center frequency. Consequently, the PLL tracks the phase of input signal with some phase error. However, this phase error can be kept very small in a well-designed PLL.

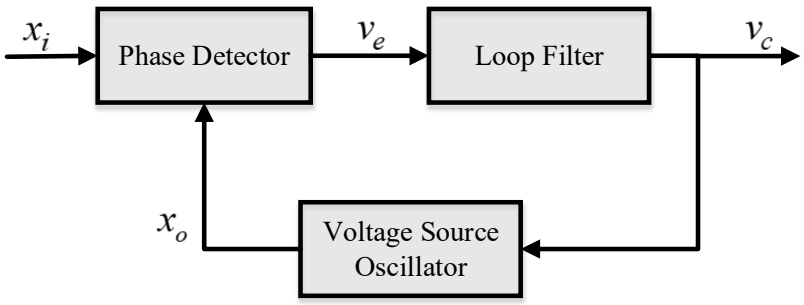

Fig. 2.1 Basic PLL structure.

Let, x_i and x_o are the input and VCO signals, which can be expressed as,

$$x_i(t) = A\cos(\omega_i t + \theta_i) \tag{2.1}$$

$$x_o(t) = B\cos(\omega_o t + \varphi_o) \tag{2.2}$$

ω_i and ω_o are angular frequencies of the input and the VCO; θ_i and φ_o are their phase constants.

The PD is a single multiplier that perform multiplication between the input and VCO signals. The PD output can be written as,

$$v_e(t) = K_d\{\cos[(\omega_i - \omega_o)t + \theta_i - \varphi_o)] + \cos[(\omega_i + \omega_o)t + \theta_i + \varphi_o)]\} \tag{2.3}$$

Where K_d is the gain of the PD. The higher frequency component of PD is eliminated by LF that is a low pass filter. The output of the LP is,

$$v_c(t) = K_d\cos[(\omega_i - \omega_o)t + \theta_i - \varphi_o)] \tag{2.4}$$

After transient period, the VCO signal synchronize with the input signal and can be expressed as

$$x_o(t) = B\sin(\omega_i t + \phi_o) \tag{2.5}$$

By comparing (2.2) and (2.5), the initial phase angle of VCO can be stated as below that is a linear function of time.

$$\varphi_o = (\omega_i - \omega_o)t + \phi_o \tag{2.6}$$

By substituting the value of φ_o in (2.4), the following expression is obtained

$$v_c(t) = K_d\cos(\theta_i - \phi_o) \tag{2.7}$$

The VCO is a frequency-modulated oscillator and instantaneous angular frequency is proportional to its input control signal ($v_c(t)$) with an offset of central frequency (ω_o), that is

$$\omega_{inst} = \frac{d}{dt}(\omega_o t + \varphi_o) = \omega_o + K_v v_c(t) \tag{2.8}$$

$$\frac{d\varphi_o}{dt} = K_v v_c(t) \tag{2.9}$$

where K_v is the VCO sensitivity. From (2.6), (2.7), and (2.9)

$$\omega_i - \omega_o = K_v v_c \tag{2.10}$$

$$\Rightarrow \omega_i - \omega_o = K_d K_v \cos(\theta_i - \phi_o)$$

$$\Rightarrow \phi_o = \theta_i - \cos^{-1} \frac{\omega_i - \omega_o}{K_d K_v} \tag{2.11}$$

From (2.8) and (2.10), it can be observed that the dc signal v_c is responsible for changing the VCO frequency from central frequency (ω_o) to the input signal angular frequency (ω_i). From eq (11), it can be observed that when $\omega_i - \omega_o \approx 0$, the phase difference between VCO and input signal become $\pi/2$, indicating that the VCO signal is in phase quadrature with the input signal when the loop is in lock. Letting output angle $\theta_o = \phi_o + \pi/2$, (2.7) becomes $v_c = K_d \sin(\theta_i - \theta_o)$. When the phase difference is small, the above $v_c = K_d \sin(\theta_i - \theta_o)$ can be approximated as $v_c \approx K_d (\theta_i - \theta_o)$, which indicates that as far as VCO phase is unequal to input signal phase, v_c contributes to make them equal. When the phase difference is zero, it is said that the output voltage is locked with the input voltage.

2.2 Commonly Used PLL Algorithms

This section describes the most commonly used PLL techniques. The PLL algorithms are mainly two types, which are single phase PLL and three phase PLL algorithm. The single phase PLLs are used to track the instantaneous phase of a phase of the grid voltages, whereas three phase PLLs track the instantaneous phases of all three phases of grid voltages. The most commonly used PLLs are described in this section in detail.

2.3 Review of Single Phase PLLs

2.3.1 Power-based PLL (pPLL)

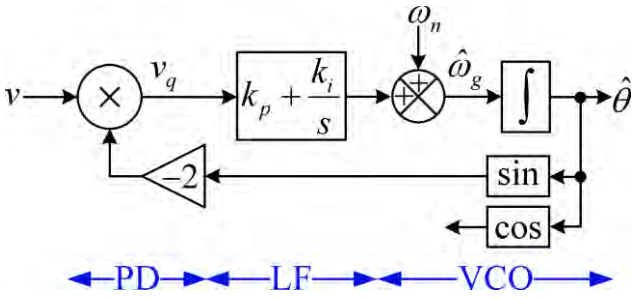

Fig. 2.2 Block diagram of pPLL.

In Fig. 2.2 basic structure of power-based PLL (pPLL) is shown, where, v is the single-phase input signal, ω_g and θ are the estimated frequency and phase angle, respectively, ω_n is the nominal value of the grid frequency, and k_p, k_i are the proportional and integral gains of the PI controller, which acts as the LF. In the PLL, a product type PD is used to produce quadrature component of the input voltage. The model produces double frequency term which creates double frequency oscillatory error in the estimated phase. Another drawback is that grid amplitude information cannot be obtained from the pPLL model and so the pPLL dynamics may not be decoupled from the amplitude variation of the grid voltage. To overcome the drawbacks, double frequency and amplitude compensation (DFAC) method is used, which is shown in Fig. 2.3. In this method, double frequency terms in both quadrature and direct axis are nullified by multiplying equal but opposite double-frequency components. DFAC-pPLL method also decouples the amplitude variation effect on phase estimation as the quadrature axis component is being normalized.

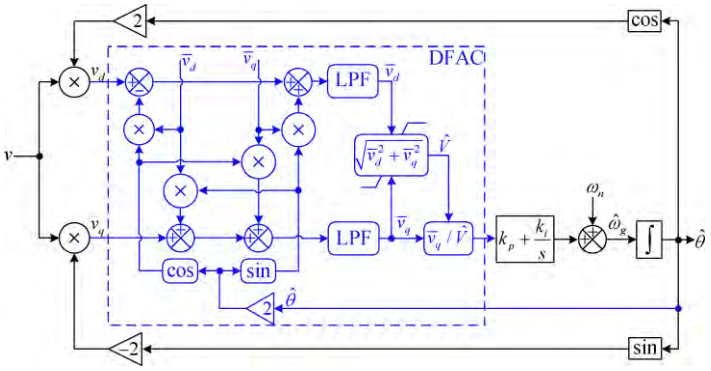

Fig. 2.3 Modified block diagram of pPLL [71].

2.3.2 Transfer delay (TD) PLL

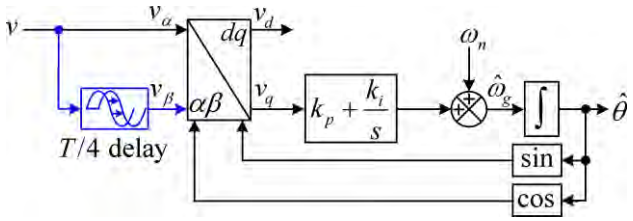

Fig. 2.4 Block diagram of Transfer Delay (TD) PLL [72].

In Fig. 2.4, the transfer delay (TD) PLLs structure is shown, which is a quadrature signal generation-based PLLs (QSG-PLLs). In TD-PLL, an orthogonal signal v_β is generated by introducing $T/4$ time delay to the original voltage, where T is the fundamental voltage period. Then, direct and quadrature signals are generated from the orthogonal signals by using Park

transformation. This is easily comparable to the conventional SRF-PLL, which will be discussed later. The shortcoming of the standard TD-PLL is that, it cannot generate orthogonal signals under distorted grid voltages that results in error in the phase estimation. To overcome this drawback, some advanced algorithms are proposed in literature.

Mathematically, a single-phase system can be represented by two-phase system where a phase is equal to zero, which is mathematically equivalent to $\alpha\beta$ frame delayed signal cancellation operator with the delay factor 4 (or briefly the $\alpha\beta$DSC4). By using two cascaded DSC4 operators, a wider notch around the fundamental voltage of the negative sequence is obtained, which results in better performance during frequency drift. The DC offset error in phase estimation in standard TD-PLL is due to phase shift in $\alpha\beta$DSC operators, that is also eliminated by subtracting the phase error from the actual estimation. A better performance can be obtained by cascading several DSCs. The modified structure is called enhanced TD-PLL that is shown in Fig. 2.5.

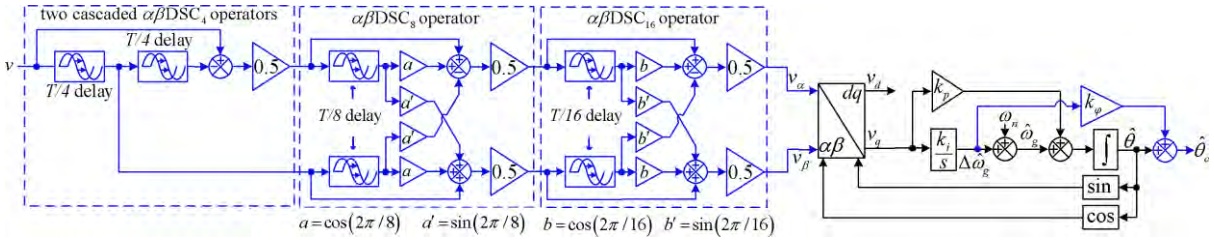

Fig. 2.5 Modified block diagram of Transfer Delay (TD) PLL [73].

2.3.3 Inverse Park transformation-based PLL (IPT-PLL)

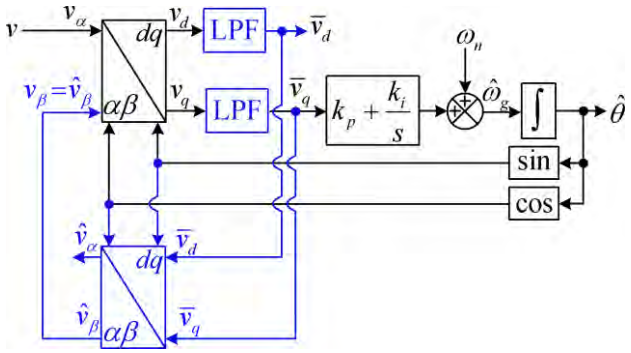

Fig. 2.6 Block diagram of IPT based PLL.

The inverse Park transformation-based PLL (IPT-PLL) shown in Fig. 2.6 is a well-known and popular PLL in single-phase applications [74]. In this PLL, orthogonal signal is generated by using dq-to-$\alpha\beta$ transformation, that is inverse Park transformation. At first, Park transformation

is used to generate *dq*-frame signals, then inverse Park transformation is used to generate *αβ* signals from *dq*-frame signals. When, in addition to the fundamental component, extracting the DC offset and some harmonic components are needed and/or for applications where a high filtering capability is required, the IPT-PLL can be extended as shown in Fig. 2.7. Obviously, selecting the number of filtering modules involves a tradeoff between the detection accuracy and the computational burden.

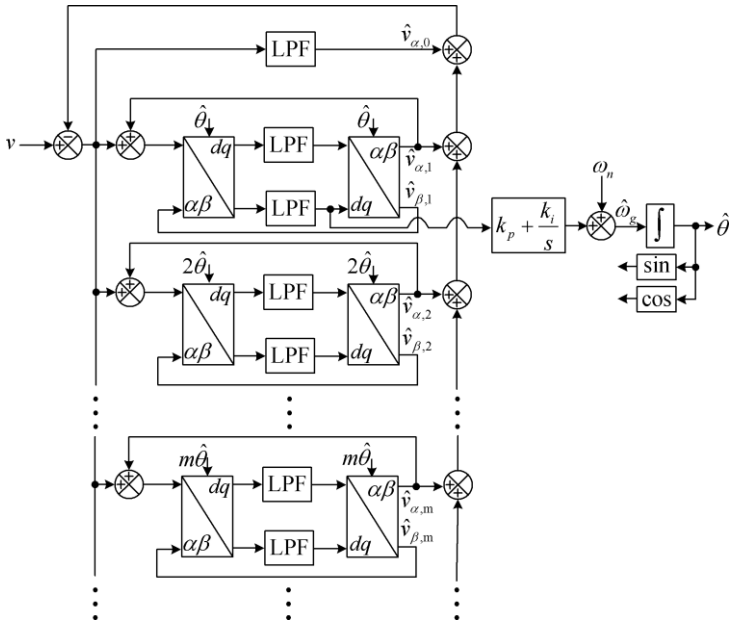

Fig. 2.7 Modified block diagram of IPT based PLL [71].

2.3.4 Second Order Generalized Integrator (SOGI) based PLL

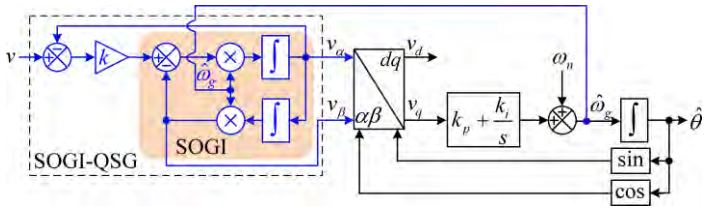

Fig. 2.8 Block diagram of SOGI based PLL [75].

Fig. 2.8 shows the diagram of a single-phase SOGI based PLL. SOGI has double integrator block and requires both grid voltage and angular frequency to produce orthogonal signals. The integrators represent two second-order filters with an adjustable bandwidth and resonance frequency equal to the frequency of the input signal. If the grid frequency is at the resonance frequency of the SOGI, the signal v_α has the same phase and amplitude as the fundamental of the input signal and v_β is orthogonal to v_α. The behavior of the whole PLL structure will be affected by the transients of the SOGI and the feedback control loop.

2.4 Review of Three Phase PLLs

2.4.1 Three Phase SRF-PLL

In the SRF-PLL, Clarke and Park transformation (phase detector) is used to generate direct and quadrature axis components from the three phase voltages. Then, the q-axis component, which contains the phase error information, is passed through a proportional-integral (PI) controller that acts as a low pass filter to generate frequency error. The output of the PI controller is then applied to a voltage-controlled oscillator (VCO) to estimate the phase angle. The conventional SRF-PLL has excellent phase tracking capability and dynamic performance under ideal grid conditions. However, when the grid voltage is unbalanced and distorted, the SRF-PLL can cause oscillation and accuracy problems. To solve this problem, numerous advanced PLLs have been intensively studied [46]. Details about the SRF-PLL will be discussed later.

2.4.2 MAF based PLL

Incorporating a moving average filter (MAF) in the SRF-PLL improves the performances of the SRF-PLL. The MAF block is placed before the PI filter block, as seen in Fig. 2.9. MAF works as low pass filter (LPF), which mitigates the influence of harmonics. However, the open-loop bandwidth of a MAF incorporated PLL is drastically reduced that results in slower dynamic response [51]. To overcome the dynamic problem of MAF-PLL, some advanced MAF based structures are proposed. In [52], MAF-PLL with phase-lead compensator is proposed that reduces the settling time to 1.79 cycles of fundamental period. In [53], another MAF-based PLL named quasi-type-1 PLL (QT1-PLL) is proposed with a feed forward control path to compensate the phase tracking error, which achieves less settling time (1.75 cycles of fundamental period). However, the MAF-PLLs are unable to reject the DC offsets of the grid voltages.

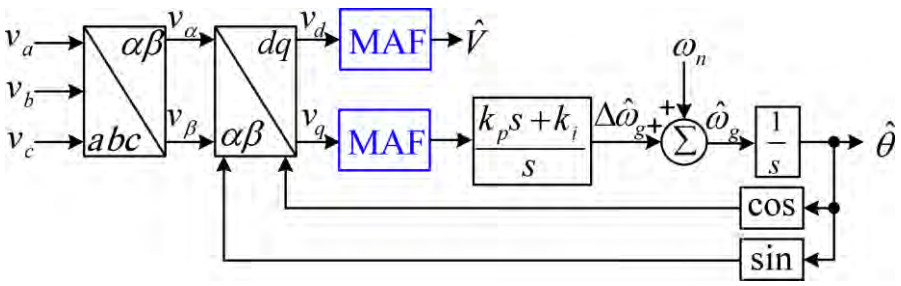

Fig. 2.9 Block diagram of MAF based PLL [76].

2.4.3 Second Order Generalized Integrator based PLL

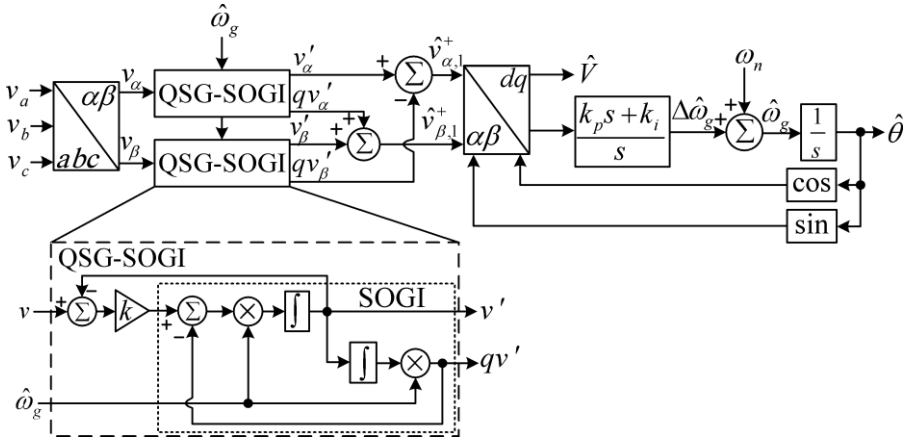

Fig. 2.10 Block diagram of SOGI based PLL [46].

A second-order generalized integrator (SOGI) is a useful tool for the extraction and separation of the FFPS and FFNS components of three-phase signals, which is shown in Fig. 2.10 [77]. As shown, two QSG-SOGIs are used to extract the filtered direct and quadrature versions of v' and qv'. The FFPS component is then calculated based on the instantaneous symmetrical components (ISC) method. This PLL structure, is often called the dual QSG-SOGI based PLL (DSOGI-PLL). Some improved SOGI such as third-order generalized integrator (TOGI) is also proposed for better performance [78].

2.4.4 Delayed Signal Cancellation PLL

In delayed signal cancelation (DSC) method, FFPS and FFNS components of the grid voltage are separated. This procedure contains stationary reference frame voltage and a voltage vector delayed by a quarter of cycle. After the separation, the obtained positive-sequence and components are input to an SRF-PLL to calculate its amplitude and angular position. The DSC operators are cascaded to get better performance in presence of harmonics and voltage unbalances. The Cascaded DSC is two types. One is pre-filter based method, where the DSC operates before the loop-filter of the SRF-PLL. Another is in-loop filter based method, which is known as *dq*CDSC. Multiple CDSC operators can then be arranged in parallel to simultaneously track multiple harmonics. DSC is also used to cancel out the negative-sequence fundamental component in unbalanced grid voltage. By combining the original α and β components of grid voltage and their quarter-cycle delayed versions, DSC-PLL can effectively eliminate the oscillatory errors resulted from voltage unbalance.

2.4.5 Complex Coefficient Filter

Complex coefficient filters (CCFs) have an asymmetrical frequency response around zero frequency, which enables them to distinct between the positive and negative sequences (polarities) of the same frequency. By using this feature, fundamental positive, negative and other harmonics can be easily extracted from the distorted grid voltages. The Fig. 2.11 shows multiple CCFs based PLL (MCCF), which is popularly used in the literatures. To extract the positive sequence fundamental frequency component only two CCFs are used, which is referred as dual CCF-based PLL (DCCF-PLL). To make the model frequency adaptive, estimated frequency from the PLL is feedbacked to the CCFs.

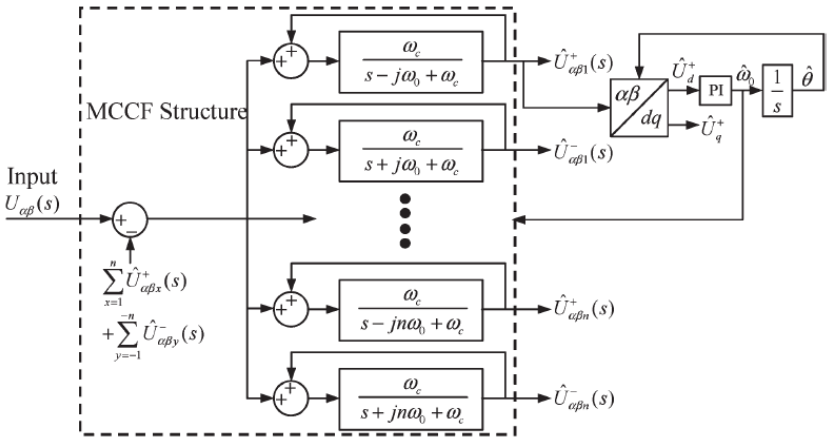

Fig. 2.11 Block diagram of CCF based PLL [46].

2.4.6 Decoupled SRF-PLL

The decoupled double SRF (DDSRF)-PLL extracts both the positive and negative-sequence voltage components in the *dq0* reference frame from *abc* voltages. Fig. 2.12 shows the block diagram of DDSRF-PLL, where two transformation blocks are used for the positive- and negative sequence components. The decoupling cells cancels the oscillations in $+dq0$ and $-dq0$ components that improves the PLL performances during input voltages' unbalances. Like SRF-PLL, a closed-loop structure with a PI controller is used to obtain the signals' phase-angle and frequency. DDSRF-PLL eliminates the drawback of the classical SRF-PLL and can estimate the phase-angle of the distorted asymmetrical three-phase systems.

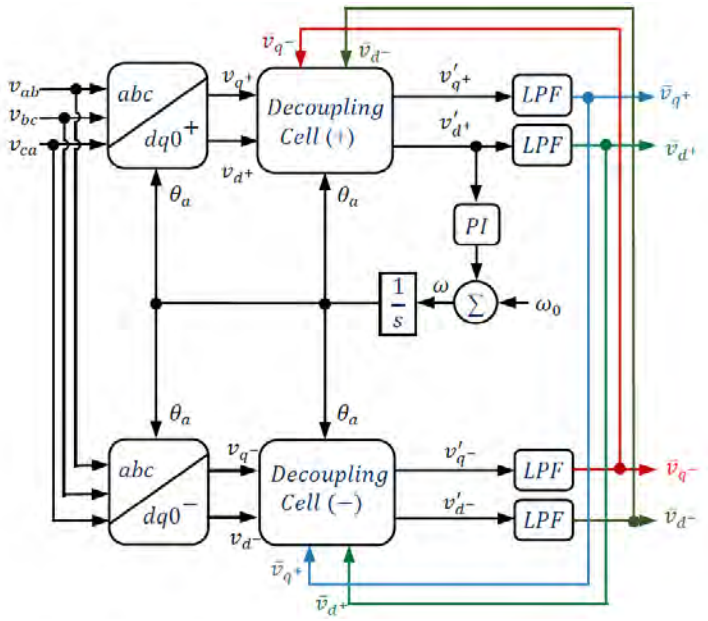

Fig. 2.12 Block diagram of Decoupled SRF-PLL [79].

2.5 The Performance of Conventional SRF-PLL Algorithm

In conventional SRF-PLL, Clarke and Park transformation are used to obtain direct (v_d) and quadrature (v_q) axis components from three-phase input voltages. The quadrature component is then passed through a proportional-integral filter to filter out noises and high order components from the v_q. The output of the PI contains frequency deviation information, which is added with nominal frequency to get the actual frequency of the input voltages. Finally, the phase is attained by integrating the frequency component. However, coefficients of Clarke and Park transformation matrix are constant at conventional SRF-PLL. As a result, the conventional SRF-PLL results in error in case of unbalanced amplitude and/or phase angle deviations conditions.

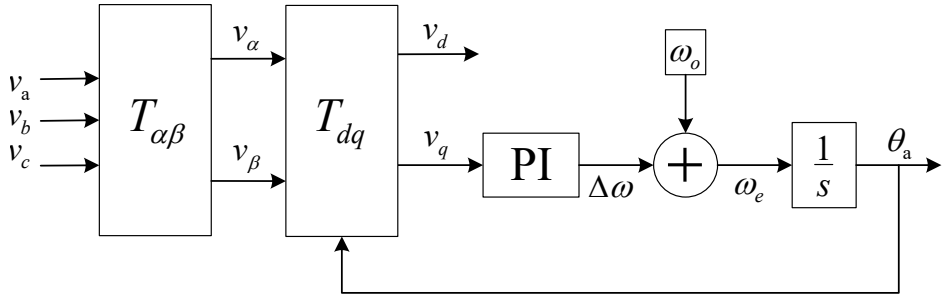

Fig. 2.13 Structure of Conventional SRF-PLL.

In Fig. 2.13, three-phase input voltages are denoted by v_a, v_b, and v_c. Clarke transformation matrix, $T_{\alpha\beta}$ converts the input voltages to orthogonal voltages, v_α and v_β. The park transformation function is symbolized by T_{dq}, which converts orthogonal voltages to the direct and quadrature axis components v_d, and v_q. The output of PI filter is marked as $\Delta\omega$, which is the frequency deviation from fundamental frequency ω_o, and the estimated angular frequency is denoted by ω_e. The integration block is shown as 1/s and θ_a is the estimated phase of phase 'a'.

The following equations are necessary to estimate the phase by using conventional SRF-PLL.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = T_{\alpha\beta} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = T_{dq} \cdot \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}$$

$$T_{\alpha\beta} = \sqrt{\tfrac{2}{3}} \cdot \begin{bmatrix} 1 & -\tfrac{1}{2} & -\tfrac{1}{2} \\ 0 & \tfrac{\sqrt{3}}{2} & -\tfrac{\sqrt{3}}{2} \end{bmatrix}$$

$$T_{dq} = \frac{2}{3} \begin{bmatrix} \sin\theta & -\cos\theta \\ \cos\theta & \sin\theta \end{bmatrix}$$

$$\theta = \int (\omega_o + \Delta\omega)\, dt$$

In the subsequent sections, the performance of SRF-PLL is demonstrated for both the balanced and unbalanced input voltages in absence or presence of harmonics.

2.6 SRF-PLL without Harmonics

2.6.1 Case1: Balanced

The performance of SRF-PLL is demonstrated in Fig. 2.14 for balanced three phase input voltages. Fig. 2.14(a) shows the balanced three phase input voltages with 1 p.u. amplitudes. In Fig. 2.14(b), stationary frame orthogonal voltages are shown. Fig. 2.14(c) illustrates the quadrature axis component of PD output, which contributes to lock the VCO phase to the input signal phase by controlling the VCO signal. In Fig. 2.14(d), the phase error, difference between the input and estimated phase, is shown, which depicts that SRF-PLL estimate the phase perfectly during the balanced condition.

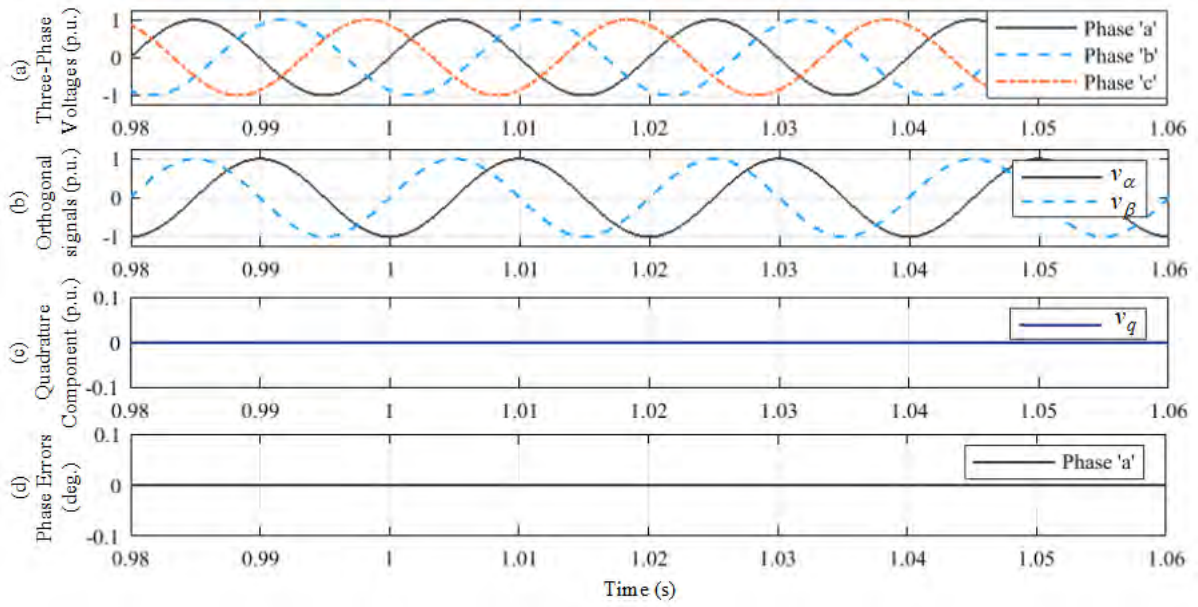

Fig. 2.14 Simulation results of SRF-PLL for balanced input voltages. (a) Three-Phase Voltages (p.u.) (b) Orthogonal Signals (p.u.) (c) Quadrature Axis Component (p.u.) (d) Estimated Phase Error (deg.).

2.6.2 Case 2: Amplitude Step

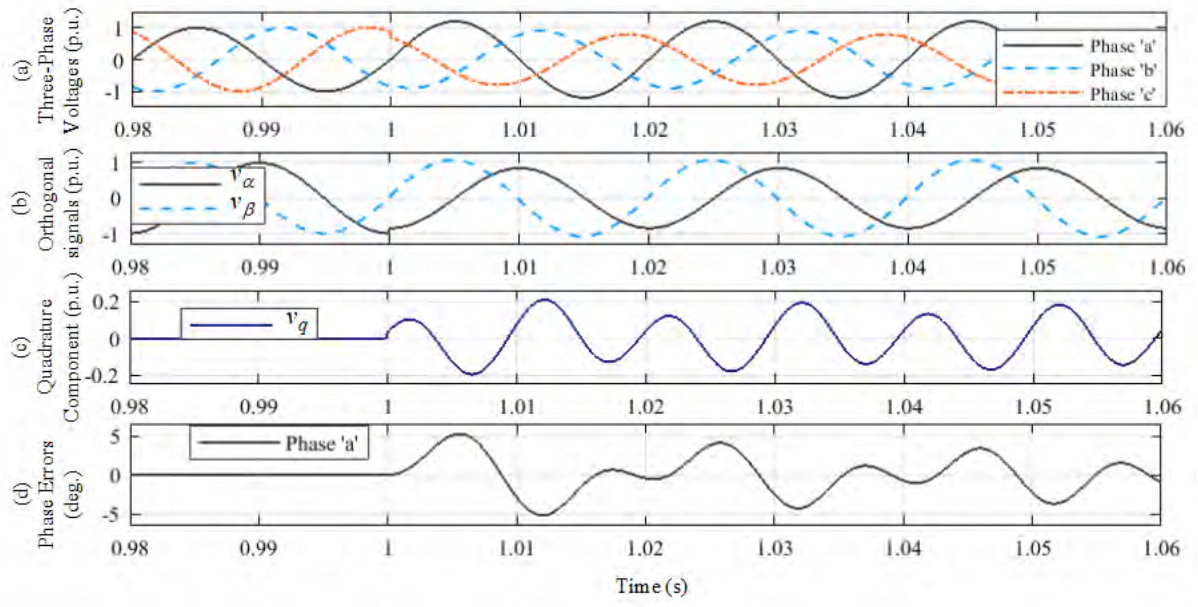

Fig. 2.15 Simulation results of SRF-PLL, when amplitude steps (v_a = 20%, v_b = -10%, v_c = -20%) occur at t=1s. (a) Three-Phase Voltages (p.u.) (b) Orthogonal Signals (p.u.) (c) Quadrature Axis Component (p.u.) (d) Estimated Phase Error (deg.).

The performance of SRF-PLL is demonstrated in Fig. 2.15 for amplitude unbalanced three phase input voltages. Fig. 2.15(a) shows the input voltages with amplitude steps (v_a = 20%, v_b

= -10%, v_c = -20%) at t=1s. As it can be seen in Fig. 2.15(b), SRF-PLL is unable to produce orthogonal signals of equal amplitudes after the step change. Fig. 2.15(c) illustrates the quadrature axis component, where almost 0.2 p.u. oscillation occurs after the step change. In Fig. 2.15(d), the phase error, difference between the input and estimated phase, is shown, which depicts that SRF-PLL produces almost 2° oscillatory error in phase estimation if amplitude unbalanced condition occurs.

2.6.3 Case 3: Phase Step

The performance of SRF-PLL is demonstrated in Fig. 2.16 for unbalanced phase angle condition. Fig. 2.16(a) shows the input voltages with phase angle steps (θ_b=30°, θ_c=20°) occur at t=1s. As it can be seen in Fig. 2.16(b), SRF-PLL produce unequal orthogonal signals after the step change. Fig. 2.16(c) illustrates the quadrature axis component, where almost 0.4 p.u. oscillation occurs after the step change. In Fig. 2.16(d), the phase error, difference between the input and estimated phase, is shown, which depicts that SRF-PLL produces almost 15° offset error and ±1.5° oscillatory error after the step change occurs.

2.6.4 Case 4: Frequency Step

The performance of SRF-PLL is demonstrated in Fig. 2.17 for frequency deviation of input signals from nominal frequency. Fig. 2.17(a) shows the input voltages with frequency step (Δf=-5 Hz) at t=1s. As it can be seen in Fig. 2.17(b), SRF-PLL produce non-orthogonal signals after the step change. Fig. 2.17(c) illustrates the quadrature axis component, where almost 0.05 p.u. oscillation occurs after the step change. In Fig. 2.17(d), the phase error, difference between the input and estimated phase, is shown, which depicts that SRF-PLL produces almost 1.5° oscillation in phase estimation after the step occurs.

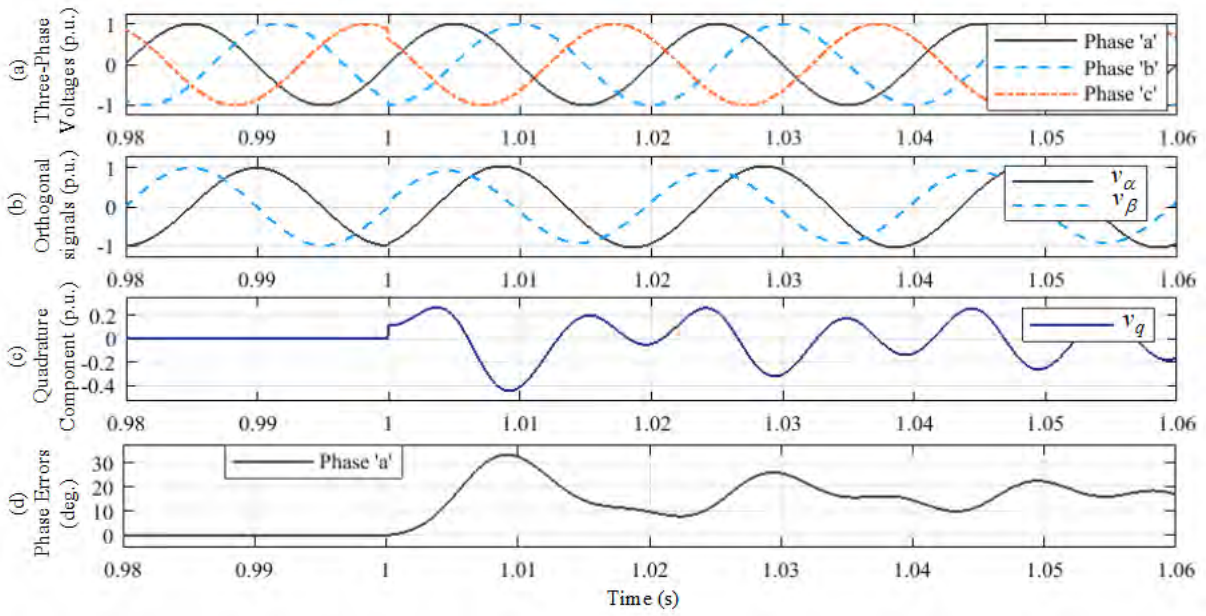

Fig. 2.16 Simulation results of SRF-PLL, when phase angle steps (θ_b=30°, θ_c=20°) occur at t=1s. (a) Three-Phase Voltages (p.u.) (b) Orthogonal Signals (p.u.) (c) Quadrature Axis Component (p.u.) (d) Estimated Phase Error (deg.).

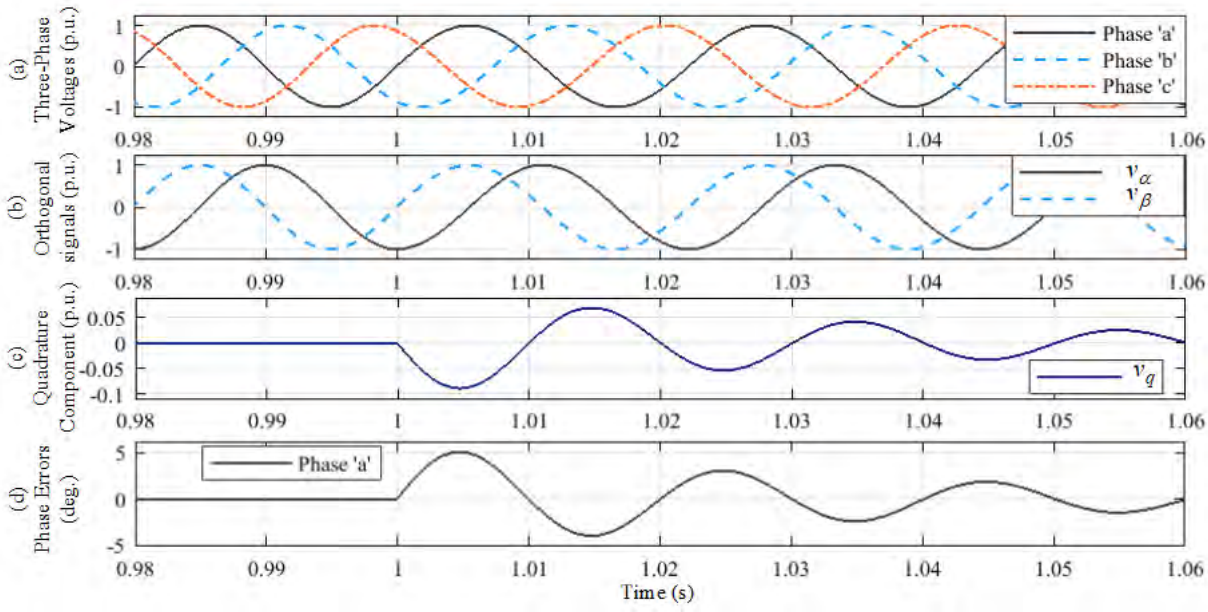

Fig. 2.17 Simulation results of SRF-PLL, when frequency step (Δf=-5 Hz) occur at t=1s. (a) Three-Phase Voltages (p.u.) (b) Orthogonal Signals (p.u.) (c) Quadrature Axis Component (p.u.) (d) Estimated Phase Error (deg.).

2.6.5 Case 5: Amplitude and Phase Steps

The performance of SRF-PLL is demonstrated in Fig. 2.18 for amplitude and phase angle unbalanced three phase input voltages. Fig. 2.18(a) shows the input voltages with amplitude steps (v_a = 20%, v_b = -10%, v_c = -20%) and phase angle steps (θ_b=30°, θ_c=20°) at t=1s. As it can be seen in Fig. 2.18(b), SRF-PLL is unable to produce orthogonal signals of equal amplitudes after the step change. Fig. 2.18(c) illustrates the quadrature axis component, where almost 0.3 p.u. oscillation occurs after the step change. In Fig. 2.18(d), the phase error, difference between the input and estimated phase, is shown, which depicts that SRF-PLL produces almost 12° offset error and ±4° oscillatory error in phase estimation with 5 ms transient time.

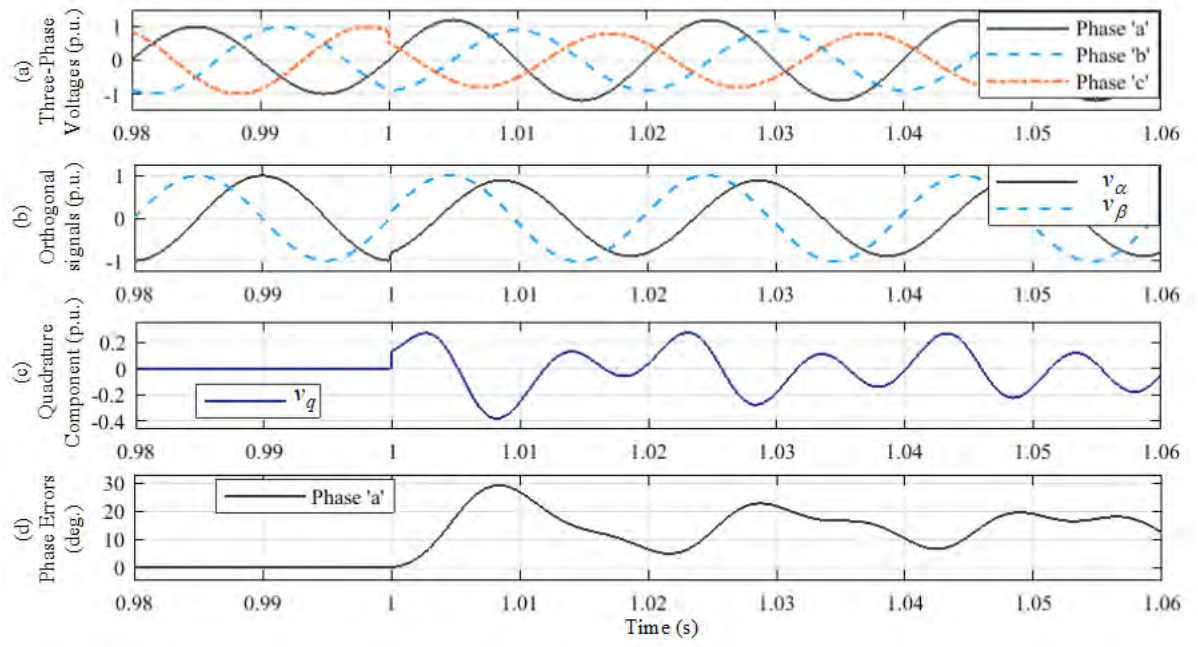

Fig. 2.18 Simulation results of SRF-PLL, when amplitude steps (v_a = 20%, v_b = -10%, v_c = -20%) and phase angle steps (θ_a=30°, θ_b=20°) occur at t=1s. (a) Three-Phase Voltages (p.u.) (b) Orthogonal Signals (p.u.) (c) Quadrature Axis Component (p.u.) (d) Estimated Phase Error (deg.).

2.6.6 Case 6: Amplitude and Frequency Steps

The performance of SRF-PLL is demonstrated in Fig. 2.19, when amplitude unbalance and frequency deviation occur simultaneously. Fig. 2.19(a) shows the input voltages with amplitude steps (v_a = 20%, v_b = -10%, v_c = -20%) and frequency step (Δf=-5 Hz) at t=1s. As it can be seen in Fig. 2.19(b), SRF-PLL is unable to produce orthogonal signals of equal amplitudes after the step change. Fig. 2.19(c) illustrates the quadrature axis component, where

almost 0.3 p.u. oscillation occurs after the step change. In Fig. 2.19(d), the phase error, difference between the input and estimated phase, is shown, which depicts that SRF-PLL produces almost 6° error in phase estimation with 2 ms transient time.

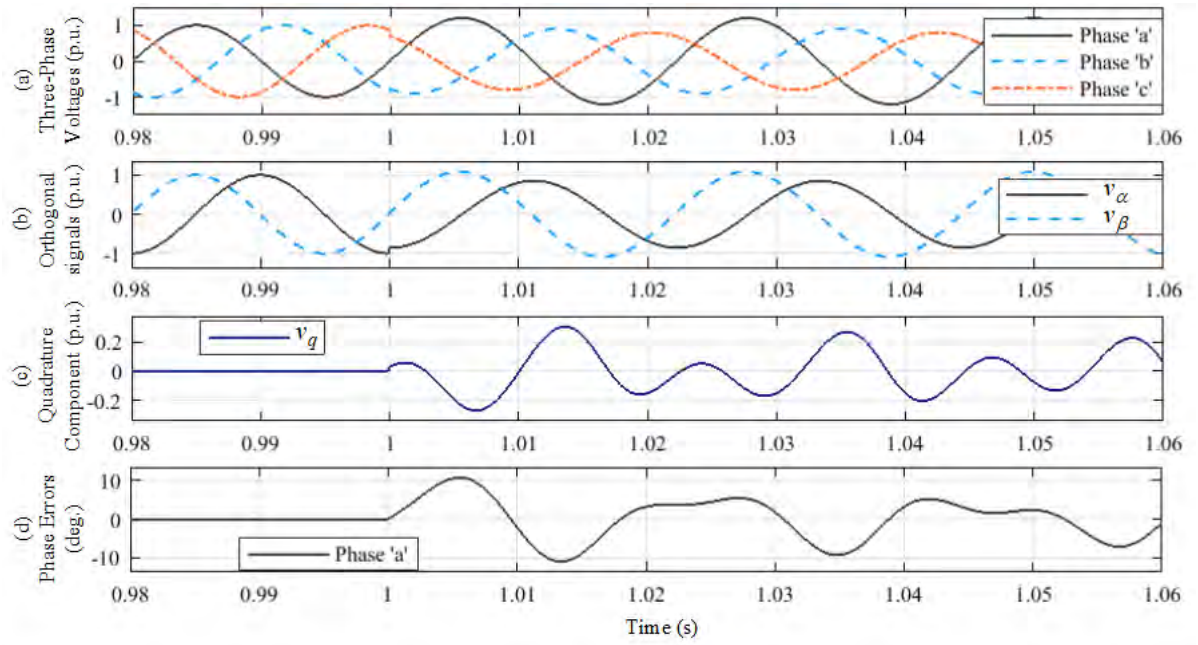

Fig. 2.19 Simulation results of SRF-PLL, when amplitude steps (v_a = 20%, v_b = -10%, v_c = -20%) and frequency step (Δf=-5 Hz) occur at t=1s. (a) Three-Phase Voltages (p.u.) (b) Orthogonal Signals (p.u.) (c) Quadrature Axis Component (p.u.) (d) Estimated Phase Error (deg.).

2.6.7 Case 7: Phase and Frequency Steps

The performance of SRF-PLL is demonstrated in Fig. 2.20, when phase angle unbalance and frequency deviation occur simultaneously. Fig. 2.20(a) shows the input voltages with phase angle steps (θ_b=30°, θ_c=20°) and frequency step (Δf=-5 Hz) at t=1s. As it can be seen in Fig. 2.20(b), SRF-PLL is unable to produce orthogonal signals of equal amplitudes after the step change. Fig. 2.20(c) illustrates the quadrature axis component, where almost 0.5 p.u. oscillation occurs after the step change. In Fig. 2.20(d), the phase error, difference between the input and estimated phase, is shown, which depicts that SRF-PLL produces almost 10° offset error and ±4° oscillatory error in phase estimation with 5 ms transient time.

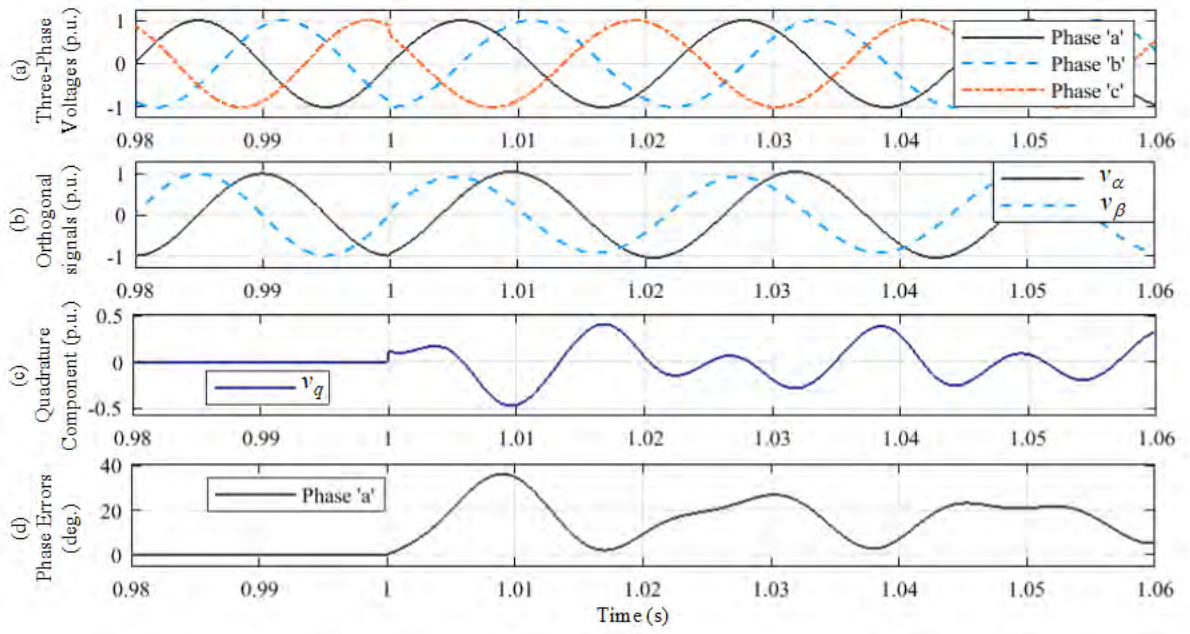

Fig. 2.20 Simulation results of SRF-PLL, when phase angle steps (θ_b=30°, θ_c=20°) and frequency step (Δf=-5 Hz) occur at t=1s. (a) Three-Phase Voltages (p.u.) (b) Orthogonal Signals (p.u.) (c) Quadrature Axis Component (p.u.) (d) Estimated Phase Error (deg.).

2.6.8 Case 8: Amplitude, Phase and Frequency Steps

The performance of SRF-PLL is demonstrated in Fig. 2.21, when amplitude, phase angle unbalance and frequency deviation occur simultaneously. Fig. 2.21(a) shows the input voltages with amplitude steps (v_a = 20%, v_b = -10%, v_c = -20%), phase angle steps (θ_b=30°, θ_c=20°), and frequency step (Δf=-5 Hz) at t=1s. As it can be seen in Fig. 2.21(b), SRF-PLL is unable to produce orthogonal signals of equal amplitudes after the step change. Fig. 2.21(c) illustrates the quadrature axis component, where almost 0.3 p.u. oscillation occurs after the step change. In Fig. 2.21(d), the phase error, difference between the input and estimated phase, is shown, which depicts that SRF-PLL produces almost 10° offset error and ±5° oscillatory error in phase estimation with 5 ms transient time.

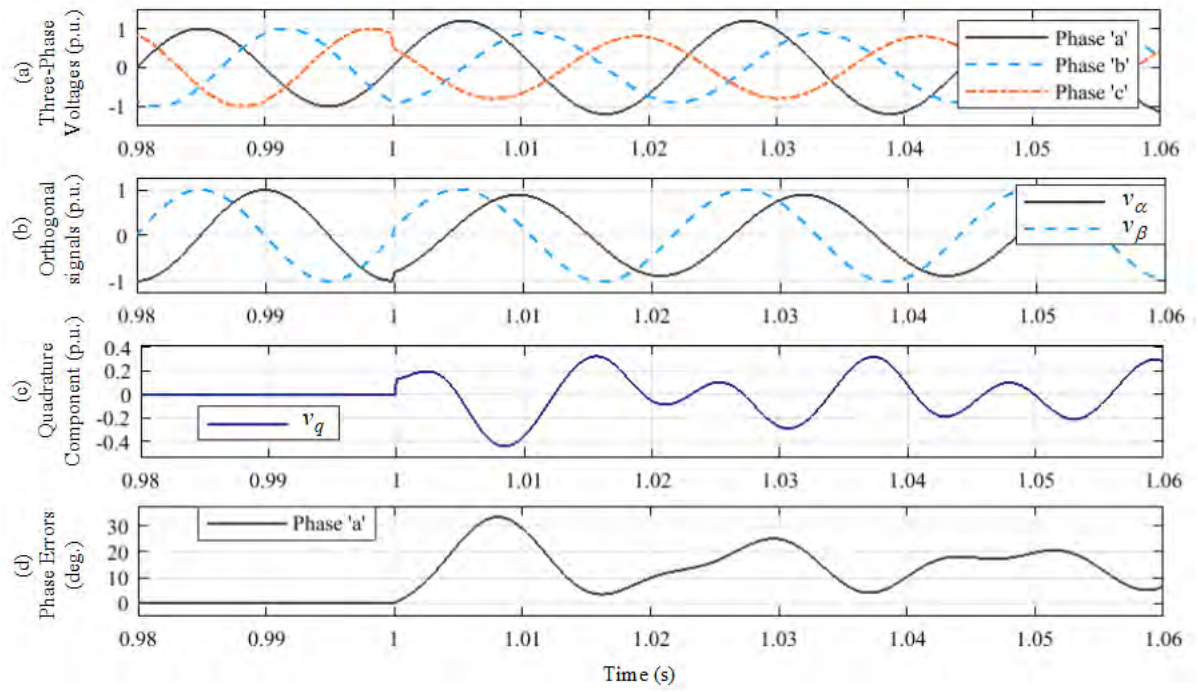

Fig. 2.21 Simulation results of SRF-PLL, when amplitude steps (v_a = 20%, v_b = -10%, v_c = -20%), phase angle steps (θ_b=30°, θ_c=20°), and frequency step (Δf=-5 Hz) occur at t=1s. (a) Three-Phase Voltages (p.u.) (b) Orthogonal Signals (p.u.) (c) Quadrature Axis Component (p.u.) (d) Estimated Phase Error (deg.).

2.6.9 Case 9: DC Offset

The performance of SRF-PLL is demonstrated in Fig. 2.22 for unequal DC offset in three phase input voltages. Fig. 2.22(a) shows the input voltages with unequal DC offset steps (v_a = 15%, v_b = 40%, v_c = -20%) occur at t=1s. As it can be seen in Fig. 2.22(b), SRF-PLL is unable to produce orthogonal signals of equal amplitudes after the step change. Fig. 2.22(c) illustrates the quadrature axis component, where almost 1 p.u. oscillation occurs after the step change. In Fig. 2.22(d), the phase error, difference between the input and estimated phase, is shown, which depicts that SRF-PLL produces large error and becomes unstable with time.

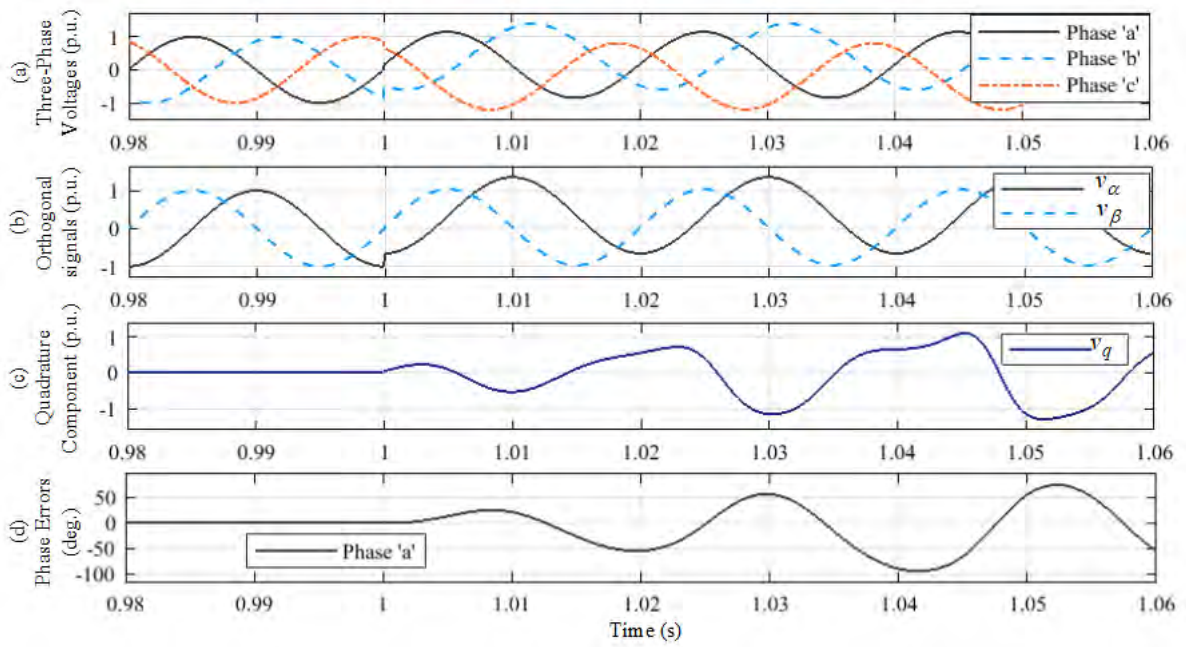

Fig. 2.22 Simulation results of SRF-PLL, when unequal DC offset steps (v_a = 15%, v_b = 40%, v_c = -20%) occur at t=1s. (a) Three-Phase Voltages (p.u.) (b) Orthogonal Signals (p.u.) (c) Quadrature Axis Component (p.u.) (d) Estimated Phase Error (deg.).

2.7 SRF-PLL with Harmonics

The performance of the SRF-PLL is shown in Fig. 2.23, when input balanced signals contain harmonics. In each phase, 5th, 7th, 11th and 13th harmonic components are considered and the amplitude of each harmonic is selected as 5% of input signals amplitudes to add harmonics. Fig. 2.23(a) shows the input balanced voltages with harmonics. The produced orthogonal $\alpha\beta$ signals are depicted in Fig. 2.23(b), which shows that SRF-PLL is unable to produce orthogonal signals of equal amplitudes if the input signals contain harmonics. Fig. 2.23(c) illustrates the quadrature axis component, where almost 0.2 p.u. oscillation occurs from the beginning of simulation. In Fig. 2.23(d) the phase error, difference between the input and estimated phase, is shown, which depicts that SRF-PLL produces almost ±0.2° error in phase estimation.

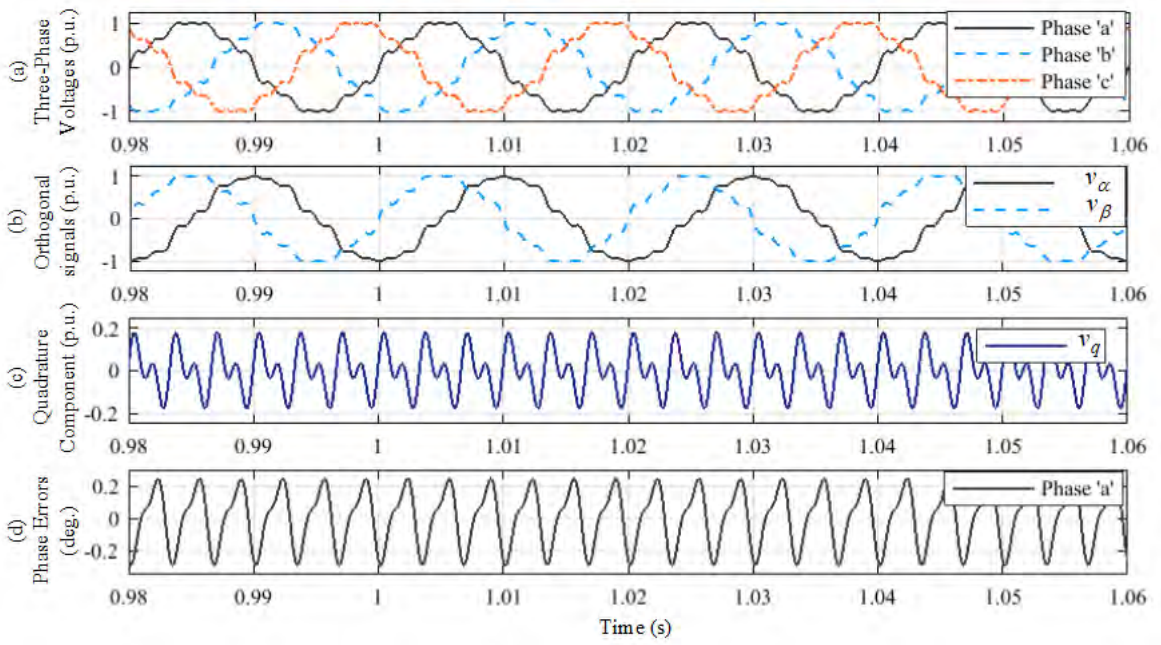

Fig. 2.23 Simulation results of SRF-PLL for balanced input voltages in presence of 5% harmonics. (a) Three-Phase Voltages (p.u.) (b) Orthogonal Signals (p.u.) (c) Quadrature Axis Component (p.u.) (d) Estimated Phase Error (deg.).

From the above analysis, it can be said that the SRF-PLL has limitations in instantaneous phase estimation in case of sudden changes in amplitudes, phases, frequencies of input voltages. This is because the conventional SRF-PLL depends on constant coefficients of Clarke transformation to produce orthogonal signals. Therefore, when the voltage parameters change but the coefficients of the transformation remain constant, the SRF-PLL fails to produce accurate orthogonal signals. Moreover, in presence of harmonics, though the input signals are balanced, the SRF-PLL produce large oscillation in phase estimation. In the next section, a three-phase phase-locked loop (PLL) algorithm relying on an adaptive Clarke transform (CT) is proposed to estimate instantaneous phases of three-phases under amplitude and/or phase angle unbalanced condition.

Chapter 3 : The Developed PLL Algorithm

3.1 Block Diagram of Proposed PLL

The block diagram representation of the proposed technique for phase estimation is shown in Fig. 3.1. As it can be seen, at first, three-phase grid instantaneous voltages of phase 'a', 'b', and 'c' incorporating with harmonics and dc offset are symbolized by v_a, v_b, and v_c, respectively. Then, the distorted input voltage of each phase passes through a band-pass filter (BPF). The purpose of the BPF is to reject harmonics and dc voltages from the input voltages. The output of BPF contains three-phase fundamental voltages that is denoted by v_A, v_B, and v_C, respectively. The fundamental voltages are then forwarded to amplitude and phase-deviation estimation block. This block is used to track V_A, V_B, and V_C, amplitudes of the fundamental voltages of phases 'a', 'b', and 'c', respectively. The block also estimates phase deviations of phases 'b' and 'c' from 120° with respect to the reference phase 'a', which are denoted by θ_b and θ_c, respectively. Then, an Adaptive Clarke Transformation (ACT) is used. The ACT helps to generate orthogonal in-phase and quadrature voltages, v_α and v_β, from the three-phase unbalanced/balanced voltages. The input of the ACT are the three-phase fundamental voltages, and their amplitudes and phase deviations information. The main feature of the ACT is that it can generate orthogonal in-phase and quadrature voltages in both amplitude and/or phase unbalanced condition of the phase voltages. At this stage, a conventional SRF-PLL is used to track the phase-angle, ϕ_A, of phase 'a' from the orthogonal input signals. However, BPF introduces error in the estimated phase when frequency deviates from fundamental frequency. A phase correction block is added to estimate the error, θ_F. The phase correction block uses the estimated frequency error, $\Delta\omega$, obtained from SRF-PLL to calculate the phase error. Finally, the phase error is subtracted from ϕ_A to obtain actual phase angle (ϕ_a) of v_A. The phase angles (ϕ_b and ϕ_c) of other two phase voltages is attained by processing ϕ_a, θ_b, and θ_c, as demonstrated in Fig. 3.1. The detail functions of each block shown in Fig. 3.1 is described in following subsections.

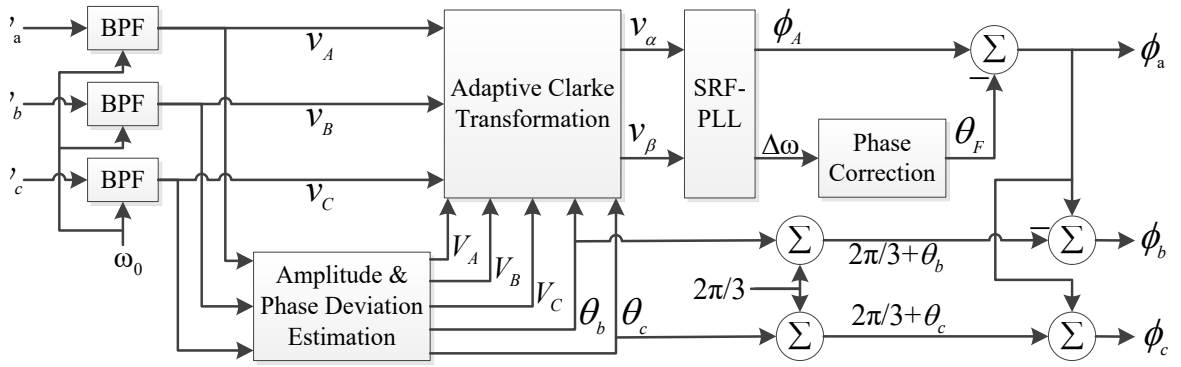

Fig. 3.1 Block Diagram Representation of the Proposed Technique.

The three phase grid voltages may include DC offset and harmonics due to non-linear loads, measurement devices, grid faults and can be expressed as follows.

$$\left.\begin{aligned} v_{\mathrm{a}}(n) &= V_{\mathrm{a}} \sin\{\phi_{\mathrm{a}}(n)\}\text{+DC offset+Harmonics} \\ v_b(n) &= V_b \sin\{\phi_{\mathrm{a}}(n) - 2\pi/3 + \theta_b\}\text{+DC offset+Harmonics} \\ v_c(n) &= V_c \sin\{\phi_{\mathrm{a}}(n) + 2\pi/3 + \theta_c\}\text{+DC offset+Harmonics} \end{aligned}\right] \tag{3.1}$$

where n is the sampling index, V_{a}, V_b, and V_c are the amplitudes of fundamental voltages of phases 'a', 'b', and 'c', respectively, $\phi_{\mathrm{a}}(n)$, $[\phi_{\mathrm{a}}(n)\text{-}2\pi/3+\ \theta_b]$, and $[\phi_{\mathrm{a}}(n)+2\pi/3+\ \theta_c]$ are instantaneous phase angles of phases 'a', 'b', 'c', respectively.

3.2 Attenuation of Harmonics: Design of Band Pass Filter

In order to reject harmonics from the grid voltages, a band pass filter (BPF) is tuned in this sub-section. The tuned BPF is based on the following transfer function [80],

$$H_1(s) = \frac{1-\alpha}{2}\,\frac{1-z^{-2}}{1-\beta(1+\alpha)z^{-1}+\alpha z^{-2}} \tag{3.2}$$

Where, α and β are the tuning parameters of the filter. In Fig. 3.2, the magnitude and phase response of 2nd and 8th order filters are shown for α=0.95, 0.98 and $\beta=2\pi fT_s$, where f is nominal frequency and T_s is sampling time. The 2nd order band-pass filter of (3.2) mitigates higher order harmonics perfectly. However, a significant portion of the lower order harmonics pass through the filter. Harmonics rejection capacity of filters can be increased by changing the tuning parameters, α and β. In Fig. 3.2(a), it is seen that by changing the value of α from 0.95 to 0.98 the bandwidth of the filter decreases. Though the harmonic rejection capacity increases with lower bandwidth, the speed of the filter decreases. To maintain higher harmonic rejection

capacity and higher speed, the order of the filter can be increased by cascading several 2nd order filters without changing the tuning parameters. In Fig. 3.2(a), it is observed that the same speed with better harmonic rejection capacity is achieved while using 8th order filter (four cascaded 2nd order filter) and α=0.95. Therefore, in this article, an 8th order filter with α=0.95 and $\beta=\pi/100$ is used in each phase as BPF to reject harmonics and DC offset from the phase voltage. Now, the tuned BPF can remove the prominent grid harmonics efficiently.

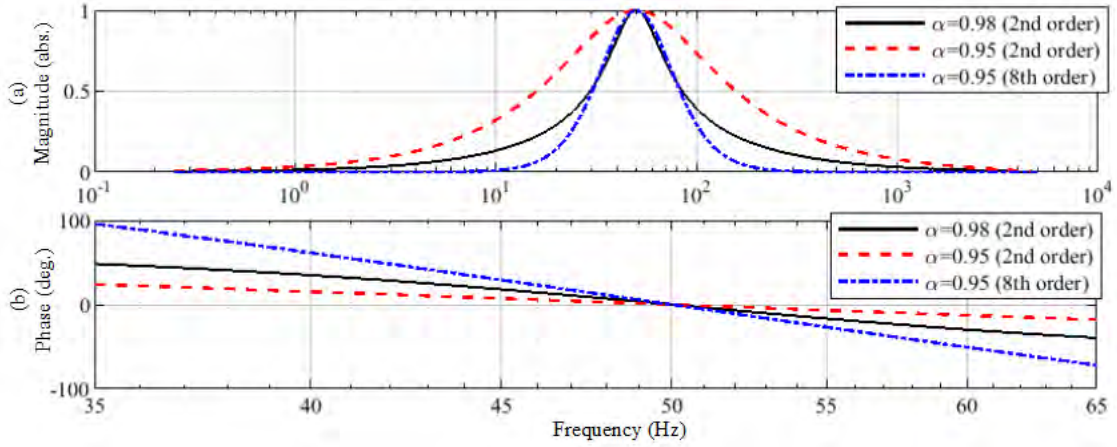

Fig. 3.2 Magnitude and Phase response of BPF.

From Fig. 3.2(b), it is seen that the BPF has zero phase response at 50 Hz frequency. As a result, if the grid's frequency deviates from the nominal frequency, BPF introduces error in phase estimation. The error can be corrected by using phase response of the filter, if frequency deviation is known, which will be discussed in section 3.4. The BPF is fixed tuned at 50 Hz (nominal frequency) under any conditions of grid voltages, that is why, there is no need to estimate system frequency at the filtering stage. After filtering out the harmonics and DC offset, the unbalanced three phase voltages are expressed as below.

$$\left.\begin{aligned} v_A(n) &= V_A \sin\{\phi_A(n)\} \\ v_B(n) &= V_B \sin\{\phi_A(n) - 2\pi/3 + \theta_b\} \\ v_C(n) &= V_C \sin\{\phi_A(n) + 2\pi/3 + \theta_c\} \end{aligned}\right] \tag{3.3}$$

3.3 Adaptive Clarke Transform for Unbalanced System

In this section, six analytical expressions are derived to calculate the six coefficients of 2x3 Clarke transformation (CT) matrix for generating accurate orthogonal voltage signals under amplitude and/or phase unbalanced condition.

The Clarke transformation can be expressed as follows,

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \alpha_A & \alpha_B & \alpha_C \\ \beta_A & \beta_B & \beta_C \end{bmatrix} \begin{bmatrix} v_A & v_B & v_C \end{bmatrix}^* \tag{3.4}$$

where * denotes transpose operation and α_A, α_B, α_C, β_A, β_B, β_C are the coefficients of the CT matrix. The matrix is elaborated by substituting v_A, v_B, and v_C from (3.3) to get the following expressions.

$$\begin{aligned} v_\alpha = &\{\alpha_A V_A - \alpha_B V_B \cos(\theta_b + \pi/3) - \alpha_C V_C \cos(\theta_c - \pi/3)\} \sin\{\phi_A(n)\} \\ &-\{\alpha_B V_B \cos(\theta_b - \pi/6) - \alpha_C V_C \cos(\theta_c + \pi/6)\} \cos\{\phi_A(n)\} \end{aligned} \tag{3.5}$$

$$\begin{aligned} v_\beta = &\{\beta_A V_A - \beta_B V_B \cos(\theta_b + \pi/3) - \beta_C V_C \cos(\theta_c - \pi/3)\} \sin\{\phi_A(n)\} \\ &-\{\beta_B V_B \cos(\theta_b - \pi/6) - \beta_C V_C \cos(\theta_c + \pi/6)\} \cos\{\phi_A(n)\} \end{aligned} \tag{3.6}$$

The coefficient of $\sin\{\phi_A(n)\}$ in v_α is set equal to the coefficient of $\cos\{\phi_A(n)\}$ in v_β and the coefficient of other terms are set to zero in order to get orthogonal signals. For simplicity, the equal nonzero coefficients are set equal to 1. Therefore,

$$\alpha_A V_A - \alpha_B V_B \cos(\theta_b + \pi/3) - \alpha_C V_C \cos(\theta_c - \pi/3) = 1 \tag{3.7}$$

$$\alpha_B V_B \cos(\theta_b - \pi/6) - \alpha_C V_C \cos(\theta_c + \pi/6) = 0 \tag{3.8}$$

$$\beta_A V_A - \beta_B V_B \cos(\theta_b + \pi/3) - \beta_C V_C \cos(\theta_c - \pi/3) = 0 \tag{3.9}$$

$$\beta_B V_B \cos(\theta_b - \pi/6) - \beta_C V_C \cos(\theta_c + \pi/6) = 1 \tag{3.10}$$

After replacing the values of the above coefficients in (3.5) and (3.6), we get orthogonal signals which can be expressed as, $v_\alpha = \sin\{\phi_A(n)\}$ and $v_\beta = -\cos\{\phi_A(n)\}$.

By setting $\alpha_B = \alpha$ and solving (3.7) and (3.8), the values of α_A, α_C are obtained as follows,

$$\alpha_A = (1 + \alpha V_B q) / V_A \tag{3.11}$$

$$\alpha_C = p\alpha \tag{3.12}$$

where $q = \cos(\theta_b + \pi/3) + \cos(\theta_b - \pi/6)\cos(\theta_c - \pi/3)/\cos(\theta_c + \pi/6)$ and $p = V_B \cos(\theta_b - \pi/6)/\{V_C \cos(\theta_c + \pi/6)\}$. Similarly, By setting $\beta_B = \beta$ and solving (3.9) and (3.10), the values of β_A, β_C are attained as follows,

$$\beta_A = \beta V_B \{\cos(\theta_b + \pi/3) + \cos(\theta_b - \pi/6)\tan(\theta_c + \pi/6)\} / V_A - \tan(\theta_c + \pi/6) / V_A \tag{3.13}$$

$$\beta_C = \{\beta V_B \cos(\theta_b - \pi/6) - 1\} / \{V_C \cos(\theta_c + \pi/6)\} \tag{3.14}$$

In order to get unique solution of (3.11)-(3.14), the values of α and β need to be specified that require another set of equations. Another set of equations is obtained by minimizing signal incorporated noises [81]. The following equation is acquired by applying CT to individual three-phase signal noises, w_A, w_B, and w_C.

$$w = (\alpha_A w_A + \alpha_B w_B + \alpha_C w_C) + j(\beta_A w_A + \beta_B w_B + \beta_C w_C)$$

The noise variance is formulated as follows considering independence of noise samples [81].

$$\sigma_{out}^2 = E(ww^*) = (\alpha_A^2 + \alpha_B^2 + \alpha_C^2 + \beta_A^2 + \beta_B^2 + \beta_C^2)\sigma^2/2 \tag{3.15}$$

After substituting the values of α_A, α_B, and α_C, the above equation is minimized by differentiating with respect to α and setting to zero.

$$\begin{aligned} &(2V_B q + 2V_B^2 q^2 \alpha)/V_A^2 + 2\alpha + 2p^2\alpha = 0 \\ &\Rightarrow \alpha = \alpha_B = -V_B q / \{V_B^2 q^2 + (p^2+1)V_A^2\} \end{aligned} \tag{3.16}$$

Now, the values of α_A and α_C can be obtained from (3.11) and (3.12), respectively. β is acquired from (3.15) by following the similar procedure of getting α, as follows

$$\beta = \beta_B = Y / X \tag{3.17}$$

$$\begin{aligned} \text{where } Y = &\{2V_B/V_A^2\}\tan(\theta_c+\pi/6)\{\cos(\theta_c+\pi/3)+\cos(\theta_b-\pi/6) \\ &\times\tan(\theta_c+\pi/6)\} + 2V_B\cos(\theta_b-\pi/6)/\{V_C^2\cos^2(\theta_c+\pi/6)\} \\ X = &2+2V_B^2\{\cos(\theta_b+\pi/3)+\cos(\theta_b-\pi/6)\tan(\theta_c+\pi/6)\}^2/V_A^2 \\ &+2V_B^2\cos^2(\theta_b-\pi/6)/\{V_C^2\cos^2(\theta_c+\pi/6)\} \end{aligned}$$

After getting β, the values of β_A and β_C can be obtained from (3.13) and (3.14), respectively. By putting V_A=V_B=V_C=*1* and θ_b=θ_c=0° for a balanced system, the CT matrix converges to conventional transformation matrix. However, for unbalanced system, the values of V_A, V_B, V_C, θ_b, and θ_c are unknown. In order to find the unknown parameters, an auxiliary algorithm is proposed in the following sections. The expressions of α_a, α_b, α_c, β_a, β_b and β_c are derived by minimizing the output noise variance given in (3.15). In this case, the effect of noise on the

performance of the proposed adaptive CT is shown in Fig. 3.3, where the unbalanced three-phase voltage signals include Gaussian noise with mean=0 and variance=0.01. The amplitudes and phase deviations of the unbalanced voltage signals are V_a=1.2 pu, V_b=1.0 pu, V_c=0.8 pu, θ_b=-20° and θ_c=10°. The outputs of the adaptive CT are shown in Fig. 3.3(b), where the values of V_a, V_b, V_c, θ_b and θ_c are assumed to be known. It can be seen from Fig. 3.3(b) that the orthogonal signals (v_α and v_β) generated by the adaptive CT contain very small amount of noise signal, as the expressions for coefficients of the adaptive CT are obtained for the minimum output noise variance.

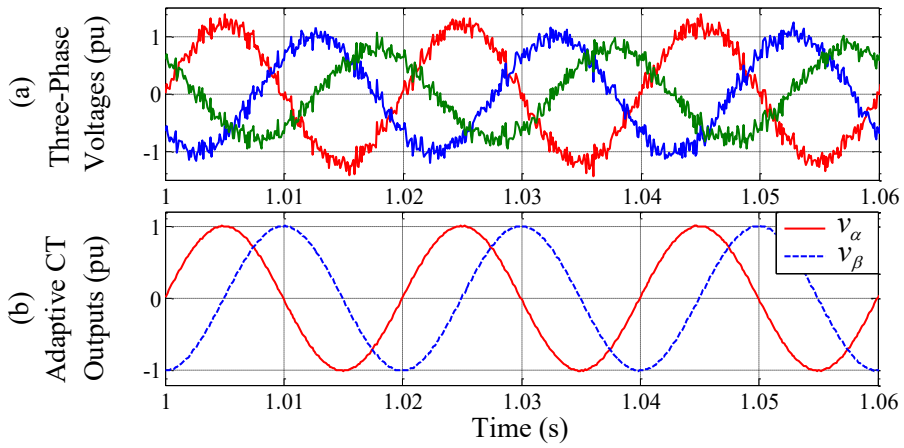

Fig. 3.3 Simulated performance of the proposed adaptive CT under Gaussian noise with mean=0 and variance=0.01 including both the amplitude (V_a=1.2 pu, V_b=1.0 pu and V_c=0.8 pu) and phase angle (θ_b=-20° and θ_c=10°) unbalanced condition. (a) Three-phase voltage signals. (b) Generated orthogonal voltage signals by using the proposed adaptive CT.

3.3.1 Amplitudes Estimation

In this section, by using zero-crossing detection algorithm, the instantaneous magnitudes of two other phases corresponding to the zero-crossing point of each phase (v_A, v_B, and v_C) are recorded and used for obtaining the amplitudes. The instantaneous magnitudes of phases 'b' and 'c', at the zero-crossing point of phase 'a' are denoted by v_B^A and v_C^A, respectively. Similarly, at the zero-crossing point of phases 'b' and 'c', instantaneous magnitudes of two other phases are symbolized by (v_A^B, v_C^B) and (v_A^C, v_B^C), respectively.

For the zero-crossing detection, one sample delay is introduced in each phase voltage, and then, the current sample and one delay sample are multiplied. If the product of the adjacent samples is positive, then no zero-crossing is detected, whereas if the product is negative or equal to

zero, then a phase voltage is just crossed zero-crossing point at that moment. At the exact zero-crossing point of a phase, the product will be zero, and instantaneous magnitudes of two other phases corresponding to the zero-crossing point of the phase can be obtained. However, if the exact zero-crossing point is missed in available samples of a phase, then product of the current and one delay sample of the phase around the zero-crossing point will be negative. As a result, exact zero-crossing of a reference phase and instantaneous magnitudes of phases corresponding to the reference phase cannot be detected, which produce error in the developed algorithm to estimate the amplitudes. To overcome the problem, from the phase samples of the reference phase (for instance, phase 'a'), the absolute values of current sample $|v_A(n)|$, one sample delay $|v_A(n\text{-}1)|$, and their average $|\{v_A(n)+ v_A(n\text{-}1)\}|/2$ around the zero-crossing point are compared and the minimum value is selected as zero-crossing point. The minimum value ensures that the closest value to the zero-crossing point is attained and used to estimate the amplitudes, which minimizes the error due to the exact zero-crossing detection failure. At the minimum value of the reference phase, instantaneous magnitudes of two other phases are recorded. For instance, at any zero-crossing point of phase 'a', if $|v_A(n)+ v_A(n\text{-}1)|/2$ is the minimum among $|v_A(n)|$, $|v_A(n\text{-}1)|$, and $|v_A(n)+ v_A(n\text{-}1)|/2$, then $(v_B^{\mathrm{A}}(n)+v_B^{\mathrm{A}}(n\text{-}1))/2$ and $(v_C^{A}(n)+v_C^{A}(n\text{-}1))/2$ are selected as instantaneous magnitudes of phase 'b' and 'c', respectively. By using this approach, the instantaneous magnitudes corresponding to zero-crossing point of each phase are obtained. Three equations are formulated by using the instantaneous magnitudes to estimate amplitudes of the three phases.

At the zero-crossing point of each phase, the instantaneous magnitudes of two other phases are measured and kept fixed at that values before the next zero-crossing comes. Hence, the amplitudes are updated at every $T/6$ interval under balanced condition of input voltages, where T is the fundamental time period of grid voltages. However, under unbalanced phase angle condition, this delay will be around $T/6$, which depends on the values of the unbalanced phase angle deviations (θ_b and θ_c).

To derive the expressions, absolute value of instantaneous samples is considered for simplicity regardless of positive or negative zero-crossing point of the phases.

From (3.3), v_B and v_C can be elaborated as follows,

$$v_B(n) = V_B(\sin\{\phi_A(n)\}\, cos(\theta_b - 2\pi/3) + cos\{\phi_A(n)\}\, sin(\theta_b - 2\pi/3)) \tag{3.18}$$

$$v_C(n) = V_C(\sin\{\phi_A(n)\}\, cos(\theta_c + 2\pi/3) + cos\{\phi_A(n)\}\, sin(\theta_c + 2\pi/3)) \tag{3.19}$$

Equation (3.18) and (3.19) can be rewritten as bellow, respectively by substituting $\sin\{\phi_A(n)=0\}$ and $\cos\{\phi_A(n)\}=1$ for the positive zero-crossing point of v_A.

$$v_B^A(n) = V_B \sin(-2\pi/3 + \theta_b) \tag{3.20}$$

$$v_C^A(n) = V_C \sin(2\pi/3 + \theta_c) \tag{3.21}$$

At the zero-crossing point of v_B, $\sin\{\phi_A(n)\}=v_A^B(n)/V_A$, $\cos\{\phi_A(n)\}=\sqrt{\{1-(v_A^B(n)/V_A)^2\}}$, which are obtained from (3.3), and (3.18) is equal to zero. Equation (3.18) can be reorganized as bellow by substituting the values of $[\sin\{\phi_A(n)\}, \cos\{\phi_A(n)\}]$ got from zero-crossing point of v_B, and $[\sin(-2\pi/3+\theta_b), \cos(-2\pi/3+\theta_b)]$ obtained from (3.20).

$$\frac{v_A^B}{V_A}\left\{1-\left(v_B^A/V_B\right)^2\right\}^{1/2} + \left\{1-\left(v_A^B/V_A\right)^2\right\}^{1/2}\frac{v_B^A}{V_B} = 0 \tag{3.22}$$

At the zero-crossing point of v_C, $\sin\{\phi_A(n)\}=v_A^C(n)/V_A$, $\cos\{\phi_A(n)\}=\sqrt{\{1-(v_A^C(n)/V_A)^2\}}$, which are obtained from (3.3), and (3.19) is equal to zero. Equation (3.18) is rearranged to get (3.23) by substituting the values of $[\sin\{\phi_A(n)\}, \cos\{\phi_A(n)\}]$ got from zero-crossing point of v_C, and $[\sin(-2\pi/3+\theta_b), \cos(-2\pi/3+\theta_b)]$ obtained from (3.20). Similarly, (3.19) is rewritten to get (3.24) by substituting the same values of $[\sin\{\phi_A(n)\}, \cos\{\phi_A(n)\}]$, and the values of $[\sin(2\pi/3+\theta_c), \cos(2\pi/3+\theta_c)]$ found from (3.21).

$$\frac{v_B^C}{V_B} = \frac{v_A^C}{V_A}\left\{1-\left(v_B^A/V_B\right)^2\right\}^{1/2} + \left\{1-\left(v_A^C/V_A\right)^2\right\}^{1/2}\frac{v_B^A}{V_B} \tag{3.23}$$

$$\frac{v_A^C}{V_A}\left\{1-\left(v_C^A/V_C\right)^2\right\}^{1/2} + \left\{1-\left(v_A^C/V_A\right)^2\right\}^{1/2}\frac{v_C^A}{V_C} = 0 \tag{3.24}$$

Equation (3.22) and (3.24) can be elaborated to get the following expressions respectively.

$$V_B / V_A = v_B^A / v_A^B \tag{3.25}$$

$$V_C / V_A = v_C^A / v_A^C \tag{3.26}$$

The denominators of (3.25) and (3.26) are normally non-zero values at normal operating conditions. In case of three-phase to ground fault, which possibility is very low, the denominators can be zero. In this case,

Now, (3.23) can be expanded as bellow by substituting V_B from (3.25).

$$V_A = \left[\frac{4(v_B^A)^2 (v_B^C)^2 (v_A^C)^2}{4(v_B^A)^2 (v_B^C)^2 - \{(v_B^A)^2 + (v_B^C)^2 - (v_A^C)^2 (v_B^A)^2 / (v_A^B)^2\}^2} \right]^{1/2} \tag{3.27}$$

After getting V_A, (3.25) and (3.26) can be used to obtain V_B and V_C, respectively. The denominators of (3.25), (3.26) and (3.27) are normally non-zero values at normal operating conditions. In case of three-phase to ground fault, which possibility is very low, the denominators can be zero. In this case, the previous sample values of V_A, V_B, V_C are hold to avoid ill condition.

3.3.2 Estimation of Phase Angle Deviation:

For estimating the phase deviations, zero-crossing point of phase 'a' is considered. As the instantaneous magnitudes of phase 'b' and 'c' are available at each zero-crossing point of phase 'a', (3.20) and (3.21) can be rewritten as bellow to estimate phase deviations, θ_b and θ_c respectively.

$$\theta_b = \sin^{-1}\left(v_B^A(n)/V_B\right) + 2\pi/3 \tag{3.28}$$

$$\theta_c = \sin^{-1}\left(v_C^A(n)/V_C\right) - 2\pi/3 \tag{3.29}$$

However, an error (θ_{er}) will be induced in estimated phase deviation in case of exact zero-sample detection failure. If the zero-crossing of phase 'a' is detected as $v_A(n)$ instead of zero, then the error can be expressed as $\theta_{er}=sin^{-1}\{v_A(n)/V_A\}$. To obtain exact θ_b and θ_c, the error should be subtracted from (3.28) and (3.29). In case of large sampling frequency, θ_{er} will be small and can be avoided from calculation. However, for low sampling frequency, θ_{er} should be considered to get accurate phase angles of all three phases. The phase deviations, as obtained by (3.28) and (3.29), are updated at every zero-crossing point of phase 'a' (both negative-to-positive and positive-to-negative). Hence, the time delay for updating the phase angle deviations will be always $T/2$ (=T180°/360°) under both the balanced and unbalanced phase angle condition.

3.4 Instantaneous Phase Angles Estimation

After getting the amplitudes and phase deviations of three-phases, orthogonal voltages (v_α, v_β) can be obtained from ACT as mentioned in section 3.3. Then, a conventional SRF-PLL is used to obtain instantaneous phase angle, $\{\phi_A(n)\}$ of phase 'a'. However, calculated phase angle includes error in case of off-nominal frequency because of BPF's non-zero phase response, as

it is seen from phase response of BPF in Fig. 3.2(b). The actual phase angle can be obtained by subtracting the error from the estimated phase angle. To calculate phase error from frequency deviation, a phase correction block is introduced in our model, as seen in Fig. 3.1. In the phase correction block, a 2nd order curve fitting algorithm is used to fit phase response of the filter in range of ±10 Hz of the nominal frequency. MATLAB's built-in 'Polyfit' function is used for curve fitting purposes. In polyfit function, 201 samples from phase response of the filter are taken in the range of ±10 Hz at every 0.1 Hz interval, and the coefficients of 2nd order polynomial are calculated. After getting the coefficients, phase error (θ_F) can be approximated by using 2nd order polynomial as seen in (3.30) for any known frequency deviation (Δf).

$$\theta_F(n) = 0.0548\Delta f^2(n) - 11.0883\Delta f(n) + 417.4158 \tag{3.30}$$

Actual phase response of BPF in the range of ±10 Hz of nominal frequency and corresponding 2nd order approximation using (3.30) is shown in Fig. 3.4.

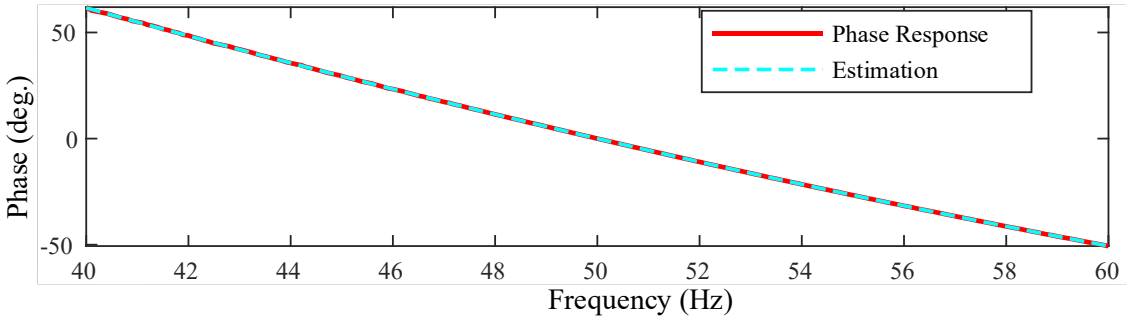

Fig. 3.4 Actual phase response and estimation of phase response of BPF in range of ±10 Hz of the nominal frequency.

As SRF-PLL provides frequency of the system along with phase angle, Δf is attained by subtracting nominal frequency from estimated frequency. The Fig. 3.4 shows that phase response of the BPF and the approximation by using (3.30) are overlapped. The actual phase-angle ($\phi_a(n)$) can be obtained by subtracting the phase error (θ_F) from estimated phase-angle, $\phi_A(n)$. By using this approach, the PLL becomes frequency adaptive without using any close-loop that improves dynamic response and stability of PLL.

After getting corrected phase angle of phase 'a', the phase angles of phase 'b' and 'c' can be obtained respectively, as follows.

$$\phi_b = \phi_a - \frac{2\pi}{3} + \theta_b \tag{3.31}$$

$$\phi_c = \phi_a + \frac{2\pi}{3} + \theta_c \tag{3.32}$$

3.5 Tuning Parameters of the PLL

In the developed PLL, there are some parameters which should be tuned to get better performance. Inside the SRF-PLL block, the PI controller have two parameters, which are k_p = Proportional gain; k_i = Integral gain. The values of k_p and k_i are chosen by using trial and error method. In [82], it is shown that SRF-PLL is actually a first order complex filter. For constant fundamental frequency, the transfer function of SRF-PLL is derived as below.

$$G_{SRF-PLL}(s) = \frac{k}{(s - j\omega_e) + k} \tag{3.33}$$

The SRF-PLL is a CBF (with center frequency ω_e) whose bandwidth is determined by the parameter k. The higher the value of k, the higher the bandwidth and, therefore, the lower the filtering capability. So, selection of k, is a trade-off between the filtering capability and the transient time. The relation between the settling time, t_s and the parameter k can be estimated as follows [82].

$$t_s = \frac{4}{k} \tag{3.34}$$

The close-loop transfer function of the SRF-PLL can be expressed as [82],

$$G_{cl}(s) = \frac{k_p s + k_i}{s^2 + k_p s + k_i} \tag{3.35}$$

The above close-loop function is a 2nd order transfer function having a zero. After setting a convenient value for k and defining $k=k_p=2\zeta\omega_n$ and $k_i=\omega_n^2$, the parameter k_i can be determined by

$$k_i = \frac{k^2}{4\zeta^2} \tag{3.36}$$

where, ζ is the damping factor and ω_n is the natural frequency.

In literature, often $\zeta=1/\sqrt{2}$ and sometime $\zeta=1$ is recommended as damping factor [58, 83].

In this dissertation, by following the above procedure and applying trial and error method, the best performance is obtained, when k_p=700, and k_i=49000 are set as PI controller parameter for both with and without harmonics cases.

Chapter 4 : Simulation and Experimental Results

4.1 Simulation Environments

The ACT based PLL model is simulated using MATLAB/Simulink. For simulation purposes, the fundamental grid frequency is set to 50 Hz, the three-phase voltage amplitude is normalized to 1 p.u., and sampling frequency is set to 10 kHz. The parameters of Proportional-Integral (P-I) controller, k_p = Proportional gain; k_i = Integral gain, are chosen according to the selection procedure described in section 3.5. The most commonly used PLL algorithm, CDSC and *dq*CDSC methods are used for the comparison purposes [56, 58]. The parameters for the CDSC and *dq*CDSC are selected as they are used in the respective literature.

4.2 Performance of Proposed PLL Without Disturbances

In this section, simulation results of three-phase input voltages without harmonics and DC offset including step change in amplitudes, phase angle deviations and frequency have been presented to verify the proposed technique.

4.2.1 Case 1: Balanced

This case reveals the performance of the proposed technique for balanced three phase voltages. In Fig. 4.1(a), balanced voltages with 1 p.u. amplitudes, zero phase deviations, and 50 Hz frequency are shown. Fig. 4.1(b) and Fig. 4.1(c) show that the proposed technique can estimate the amplitudes and zero phase angle deviations of the voltages. Fig. 4.1(d) dictates the coefficients of CT matrix and Fig. 4.1(e) demonstrates the orthogonal signals. Finally, Fig. 4.1(f) illustrates the phase angle estimation errors of all three phases. Additionally, in Fig. 4.1(g), comparison of the proposed method with CDSC and *dq*CDSC is shown.

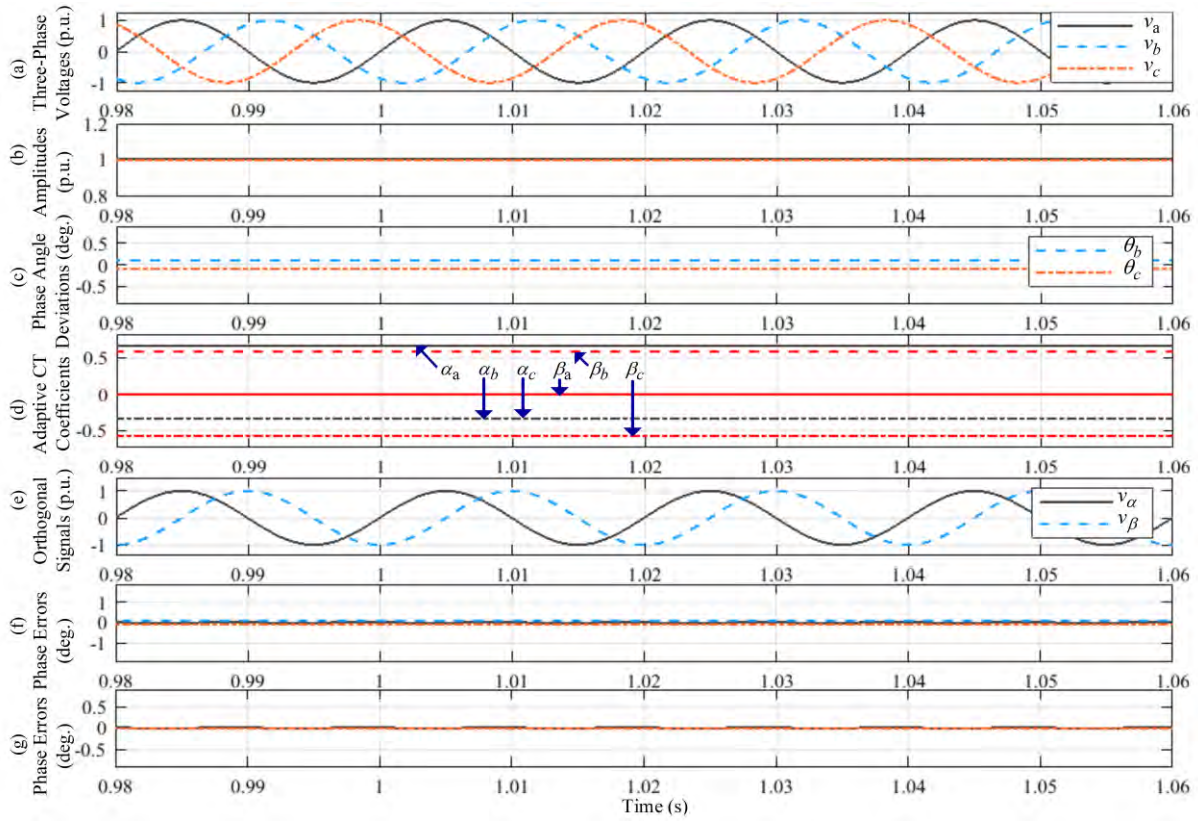

Fig. 4.1 Simulated results for balanced inputs with 1p.u. amplitudes, zero phase deviations and 50 Hz frequency. (a) Three-Phase Voltages (p.u.) (b) Amplitudes (p.u.) (c) Phase Angle Deviations (deg.) (d) Adaptive CT Coefficients (e) Orthogonal Signals (p.u.) (f) Phase Errors (deg.) (g) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

4.2.2 Case 2: Amplitude Step

This case reveals the performance of the proposed technique when an unbalanced amplitude steps occur in input voltages. As it can be seen in Fig. 4.2(a), amplitude steps (v_a = 20%, v_b = -20%, v_c = -40%) are created in the three phase input voltages at t=1s. Fig. 4.2(b) and Fig. 4.2(c) show that the proposed technique can estimate the unbalanced amplitudes and zero phase angle deviations of the voltages after the step change with a transient time of 10 ms. Fig. 4.2(d) dictates that the coefficients of CT matrix changes adaptively after the step change in order to generate orthogonal signals and Fig. 4.2(e) demonstrates the orthogonal signals. Finally, Fig. 4.2(f) illustrates the phase angle estimation errors of all three phases. Additionally, in Fig. 4.2(g), comparison of the proposed method with CDSC and *dq*CDSC is shown, which reflects that all the three methods can track phase angle under amplitude unbalanced condition.

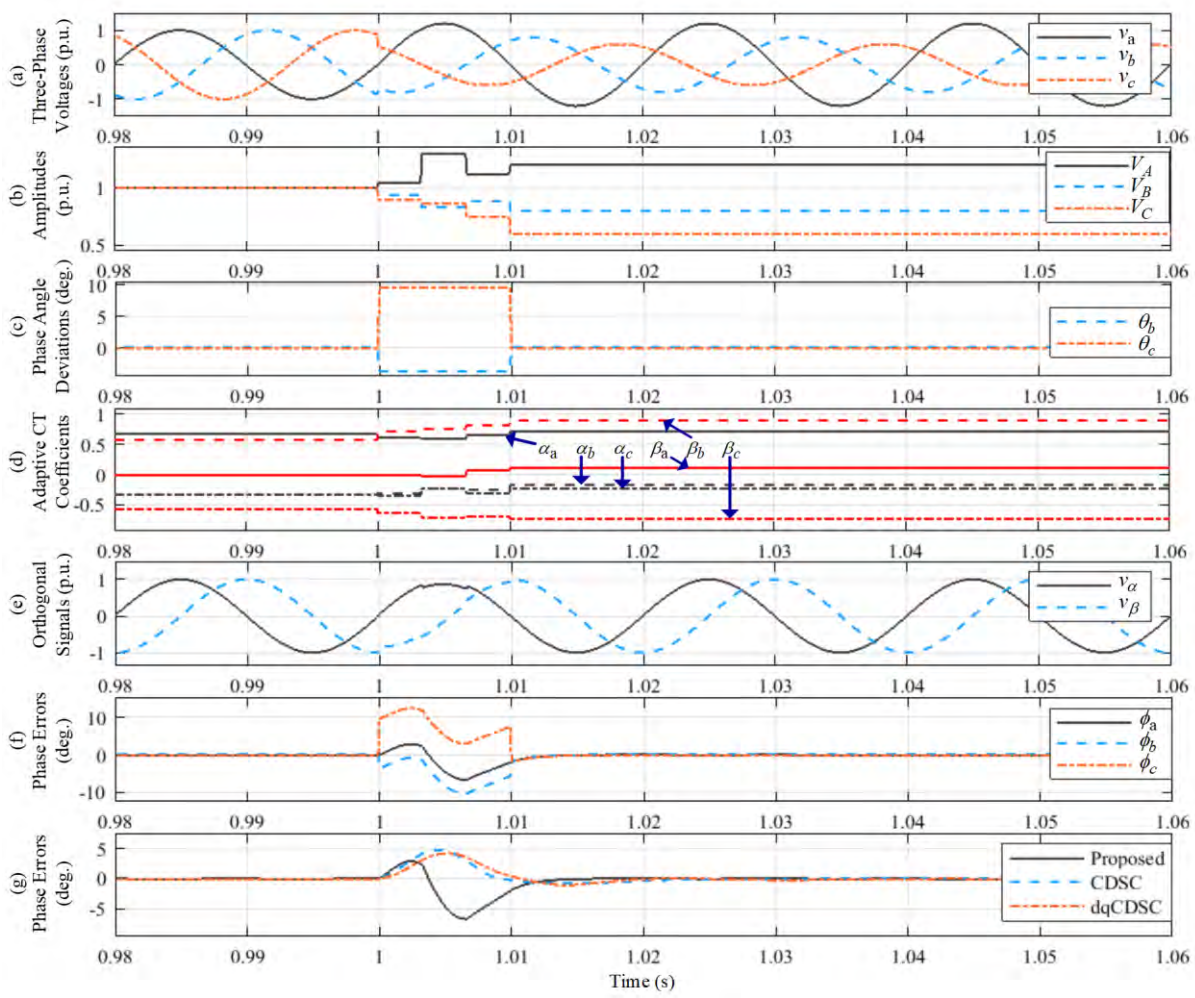

Fig. 4.2 Simulated results when an amplitude step (v_a = 20%, v_b = -20%, v_c = -40%) is created at t=1s from balanced condition. (a) Three-Phase Voltages (p.u.) (b) Amplitudes (p.u.) (c) Phase Angle Deviations (deg.) (d) Adaptive CT Coefficients (e) Orthogonal Signals (p.u.) (f) Phase Errors (deg.) (g) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

4.2.3 Case 3: Phase Step

Case 3 reveals the performance of the proposed technique when phase deviations step occurs in input voltages. As it can be seen in Fig. 4.3(a), phase deviations step (θ_b = +30°, θ_c = +20°) are created in the three phase input voltages at t=1s. Fig. 4.3(b) and Fig. 4.3(c) show that the proposed technique can estimate the balanced amplitudes and unbalanced phase angle deviations of the voltages after the step change with a transient time of 10 ms. Fig. 4.3(d) dictates that the coefficients of CT matrix changes adaptively after the step change in order to generate orthogonal signals and Fig. 4.3(e) demonstrates the orthogonal signals.

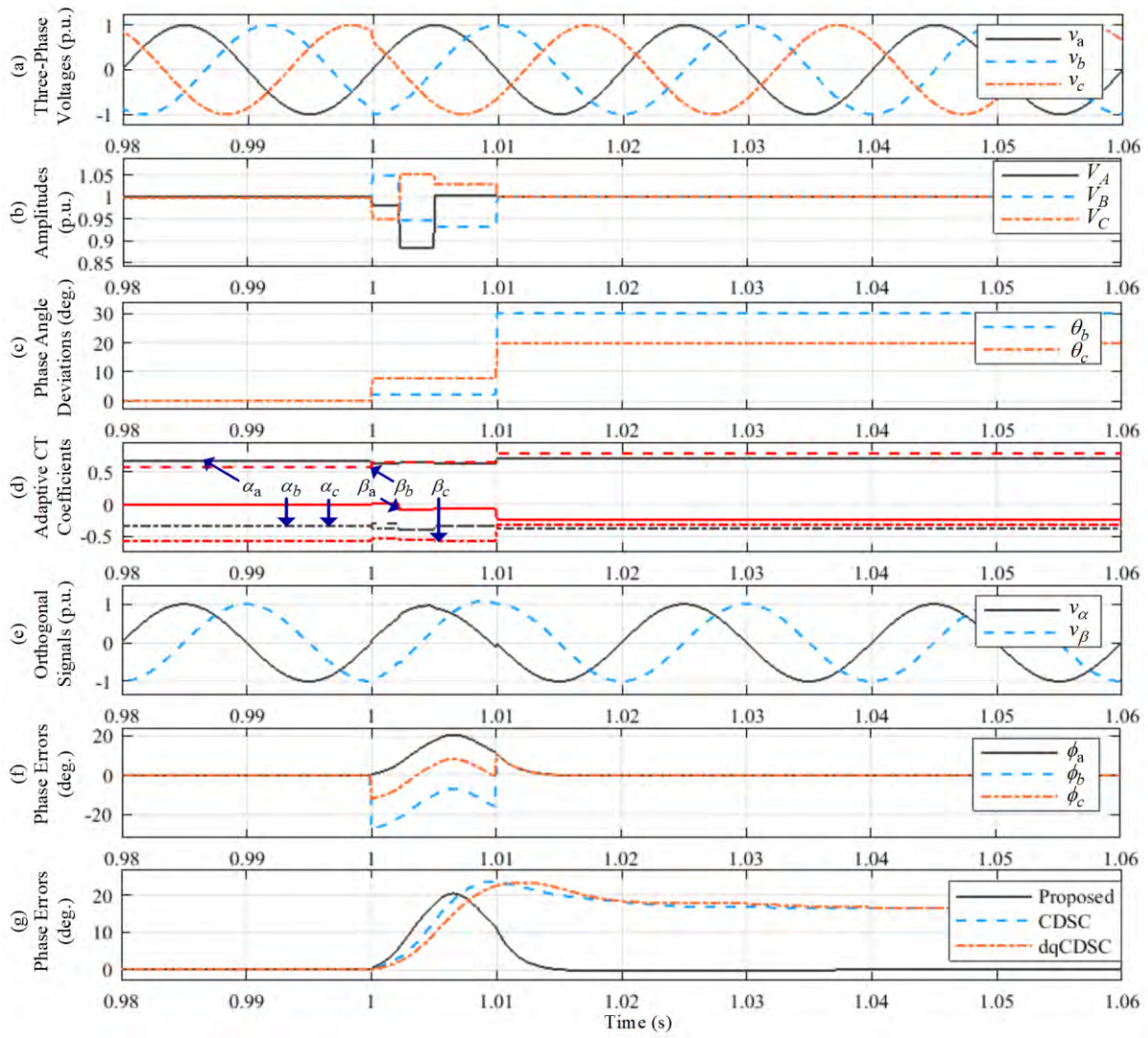

Fig. 4.3 Simulated results when phase deviations step ($\theta_b = +30°$, $\theta_c = +20°$) are created at t=1s from balanced condition. (a) Three-Phase Voltages (p.u.) (b) Amplitudes (p.u.) (c) Phase Angle Deviations (deg.) (d) Adaptive CT Coefficients (e) Orthogonal Signals (p.u.) (f) Phase Errors (deg.) (g) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

Finally, Fig. 4.3(f) illustrates the phase angle estimation errors of all three phases. Additionally, in Fig. 4.3(g), comparison of the proposed method with CDSC and *dq*CDSC is shown, which reflects that the proposed technique can track phase angle accurately for the whole time, whereas CDSC and *dq*CDSC methods fail to do so with around 17° offset error after the step change.

4.2.4 Case 4: Frequency Step

The performance of the proposed technique is demonstrated when frequency steps occur in input voltages.

As it can be seen in Fig. 4.4(a), frequency steps (-2 Hz) are created in the three phase input voltages at t=1s. Fig. 4.4(b) and Fig. 4.4(c) show that the proposed technique can estimate the balanced amplitudes and zero phase angle deviations of the voltages after the step change without significant transient time. Fig. 4.4(d) dictates that the coefficients of CT matrix changes adaptively after the step change in order to generate orthogonal signals. In Fig. 4.4(e), the orthogonal signals are shown and it depicts that even after the step change the CT generates orthogonal signals. Finally, Fig. 4.4(f) illustrates the phase angle estimation errors of all three phases. Additionally, in Fig. 4.4(g), comparison of the proposed method with CDSC and *dq*CDSC is shown, which reflects that all the three methods can track phase angle under amplitude and frequency unbalanced condition.

4.2.5 Case 5: Amplitude and Frequency Steps

This case reveals the performance of the proposed technique when an unbalanced amplitude and frequency steps occur simultaneously in input voltages.

As it can be seen in Fig. 4.5(a), amplitude steps (v_a = 20%, v_b = -20%, v_c = -40%) and frequency steps (-2 Hz) are created in the three phase input voltages at t=1s. Fig. 4.5(b) and Fig. 4.5(c) show that the proposed technique can estimate the unbalanced amplitudes and zero phase angle deviations of the voltages after the step change with a transient time of 10 ms. Fig. 4.5(d) dictates that the coefficients of CT matrix changes adaptively after the step change in order to generate orthogonal signals. In Fig. 4.5(e), the orthogonal signals are shown and it depicts that even after the step change the CT generates orthogonal signals. Finally, Fig. 4.5(f) illustrates the phase angle estimation errors of all three phases. Additionally, in Fig. 4.5(g), comparison of the proposed method with CDSC and *dq*CDSC is shown, which reflects that all the three methods can track phase angle under amplitude and frequency unbalanced condition.

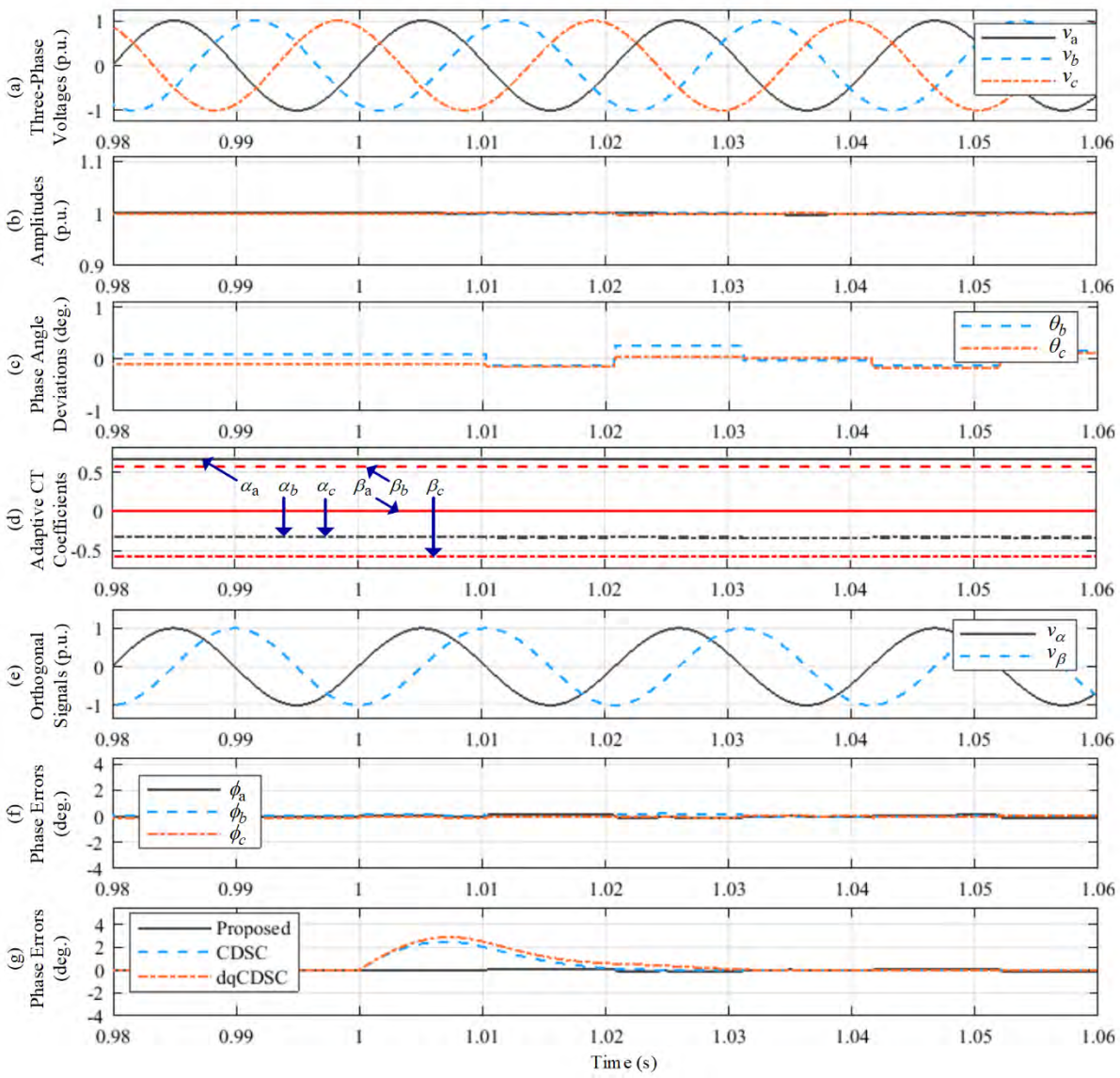

Fig. 4.4 Simulated results when frequency steps (-2 Hz) are created at t=1s from balanced condition. (a) Three-Phase Voltages (p.u.) (b) Amplitudes (p.u.) (c) Phase Angle Deviations (deg.) (d) Adaptive CT Coefficients (e) Orthogonal Signals (p.u.) (f) Phase Errors (deg.) (g) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

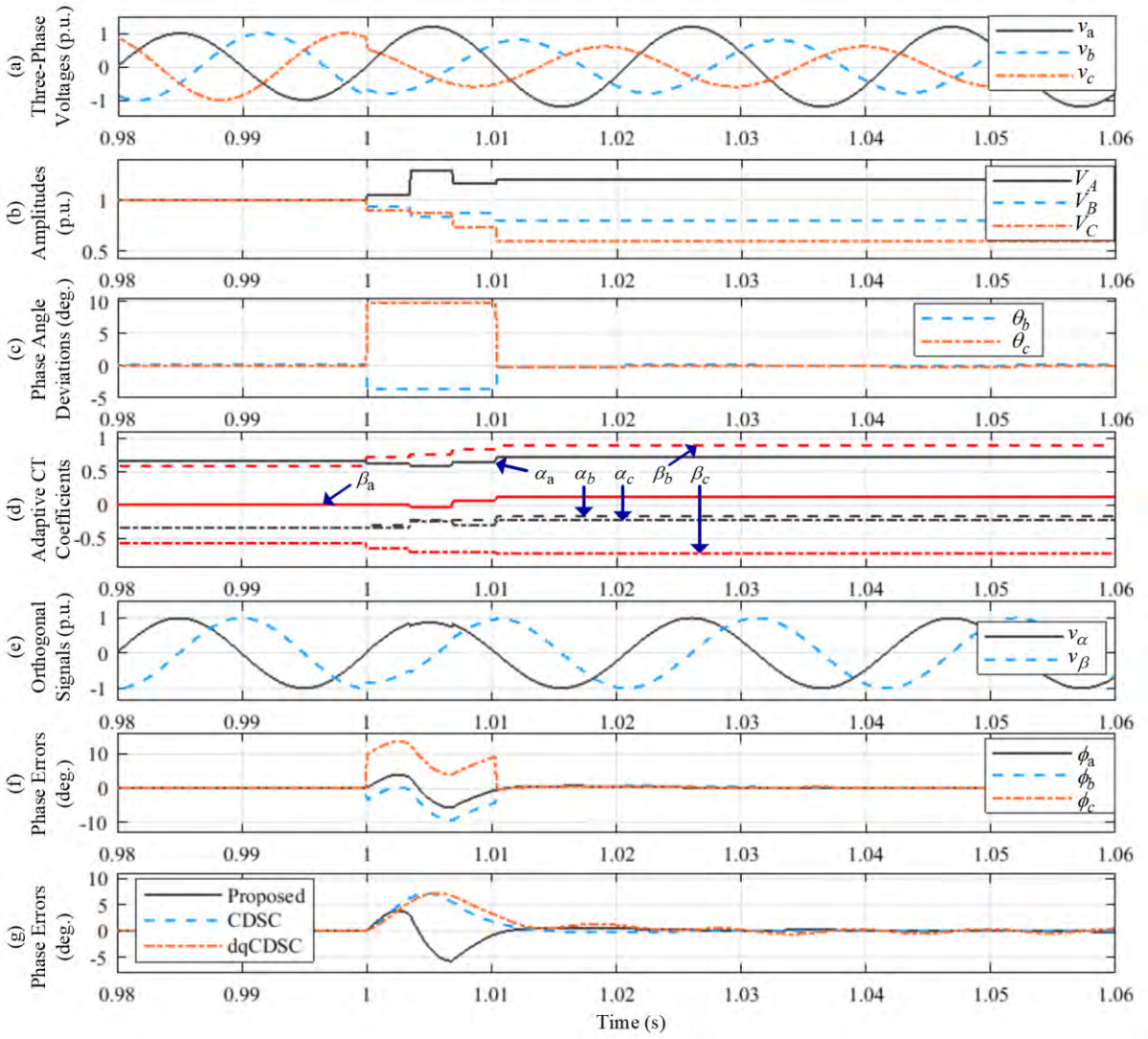

Fig. 4.5 Simulated results when an amplitude steps (v_a = 20%, v_b = -20%, v_c = -40%) and frequency steps (-2 Hz) is created at t=1s from balanced condition. (a) Three-Phase Voltages (p.u.) (b) Amplitudes (p.u.) (c) Phase Angle Deviations (deg.) (d) Adaptive CT Coefficients (e) Orthogonal Signals (p.u.) (f) Phase Errors (deg.) (g) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

4.2.6 Case 6: Amplitude and Phase Steps

Case 6 reveals the performance of the proposed technique when an unbalanced amplitude and phase steps occur simultaneously in input voltages. As it can be seen in Fig. 4.6(a), amplitude steps (v_a = 20%, v_b = -20%, v_c = -40%) and phase steps (θ_b = +30°, θ_c = +20°) are created in the three phase input voltages at t=1s. Fig. 4.6(b) and Fig. 4.6(c) show that the proposed technique can estimate the unbalanced amplitudes and phase angle deviations of the voltages after the step change with a transient time of 10 ms. Fig. 4.6(d) dictates that the coefficients of CT matrix

changes adaptively after the step change in order to generate orthogonal signals. In Fig. 4.6(e), the orthogonal signals are shown and it depicts that even after the step change the CT generates orthogonal signals. Finally, Fig. 4.6(f) illustrates the phase angle estimation errors of all three phases. Additionally, in Fig. 4.6(g), comparison of the proposed method with CDSC and *dq*CDSC is shown, which reflects that the proposed technique can track phase angle accurately for the whole time, whereas CDSC and *dq*CDSC methods fail to do so with around 14° offset error after the step change.

4.2.7 Case 7: Phase and Frequency Steps

The performance of the proposed technique is discussed when phase deviations and frequency steps occur simultaneously in input voltages. As it can be seen in Fig. 4.7(a), phase deviations step (θ_b = +30°, θ_c = +20°) and frequency steps (-2 hz) are created in the three phase input voltages at t=1s. Fig. 4.7(b) and Fig. 4.7(c) show that the proposed technique can estimate the balanced amplitudes and unbalanced phase angle deviations of the voltages after the step change with a transient time of 10 ms. Fig. 4.7(d) dictates that the coefficients of CT matrix changes adaptively after the step change in order to generate orthogonal signals and Fig. 4.7(e) demonstrates the orthogonal signals. Finally, Fig. 4.7(f) illustrates the phase angle estimation errors of all three phases. Additionally, in Fig. 4.7(g), comparison of the proposed method with CDSC and *dq*CDSC is shown, which reflects that the proposed technique can track phase angle accurately for the whole time, whereas CDSC and *dq*CDSC methods fail to do so with around 17° offset error after the step change.

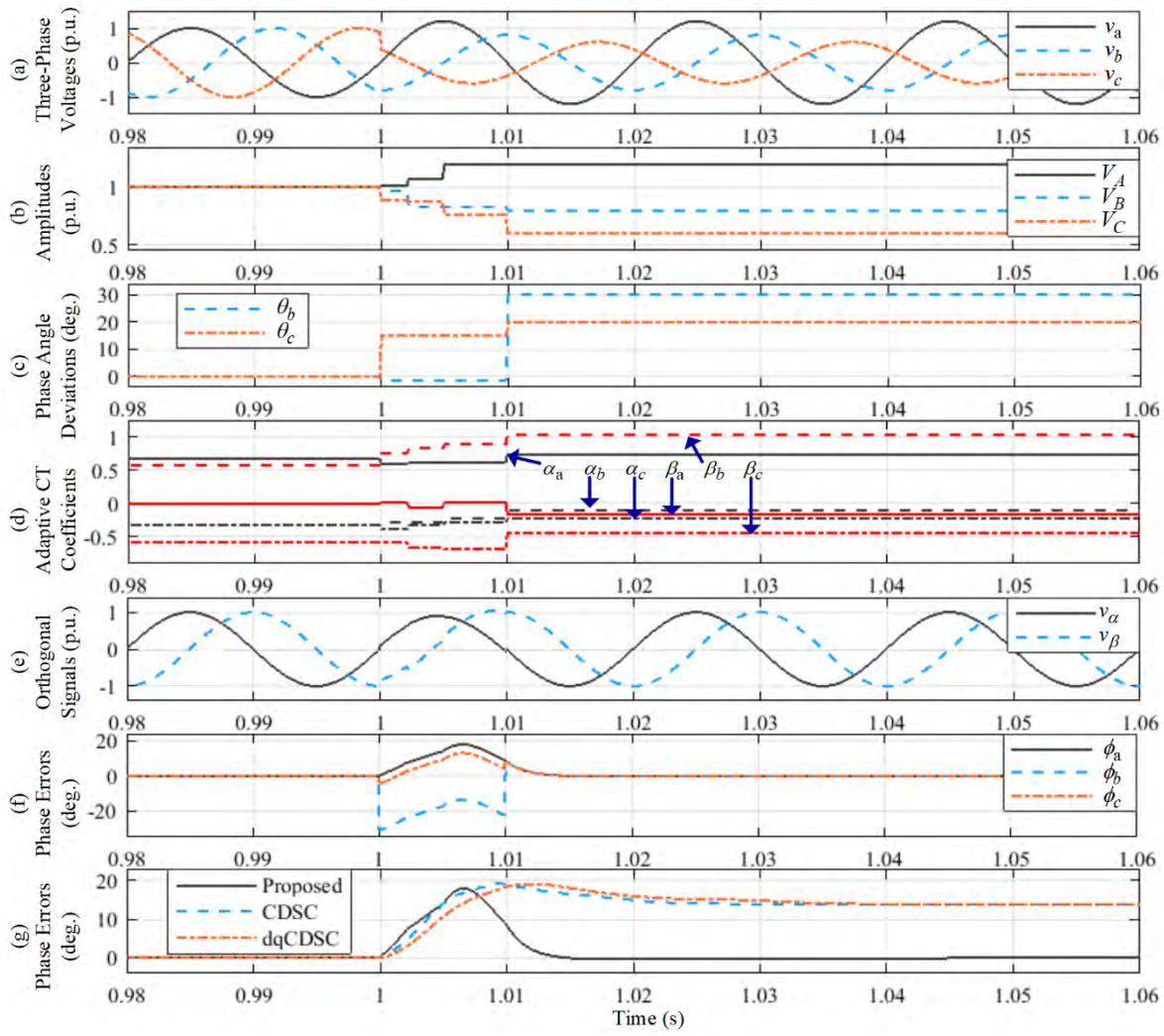

Fig. 4.6 Simulated results when an amplitude steps (v_a = 20%, v_b = -20%, v_c = -40%) and phase steps (θ_b = +30°, θ_c = +20°) are created at t=1s from balanced condition. (a) Three-Phase Voltages (p.u.) (b) Amplitudes (p.u.) (c) Phase Angle Deviations (deg.) (d) Adaptive CT Coefficients (e) Orthogonal Signals (p.u.) (f) Phase Errors (deg.) (g) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

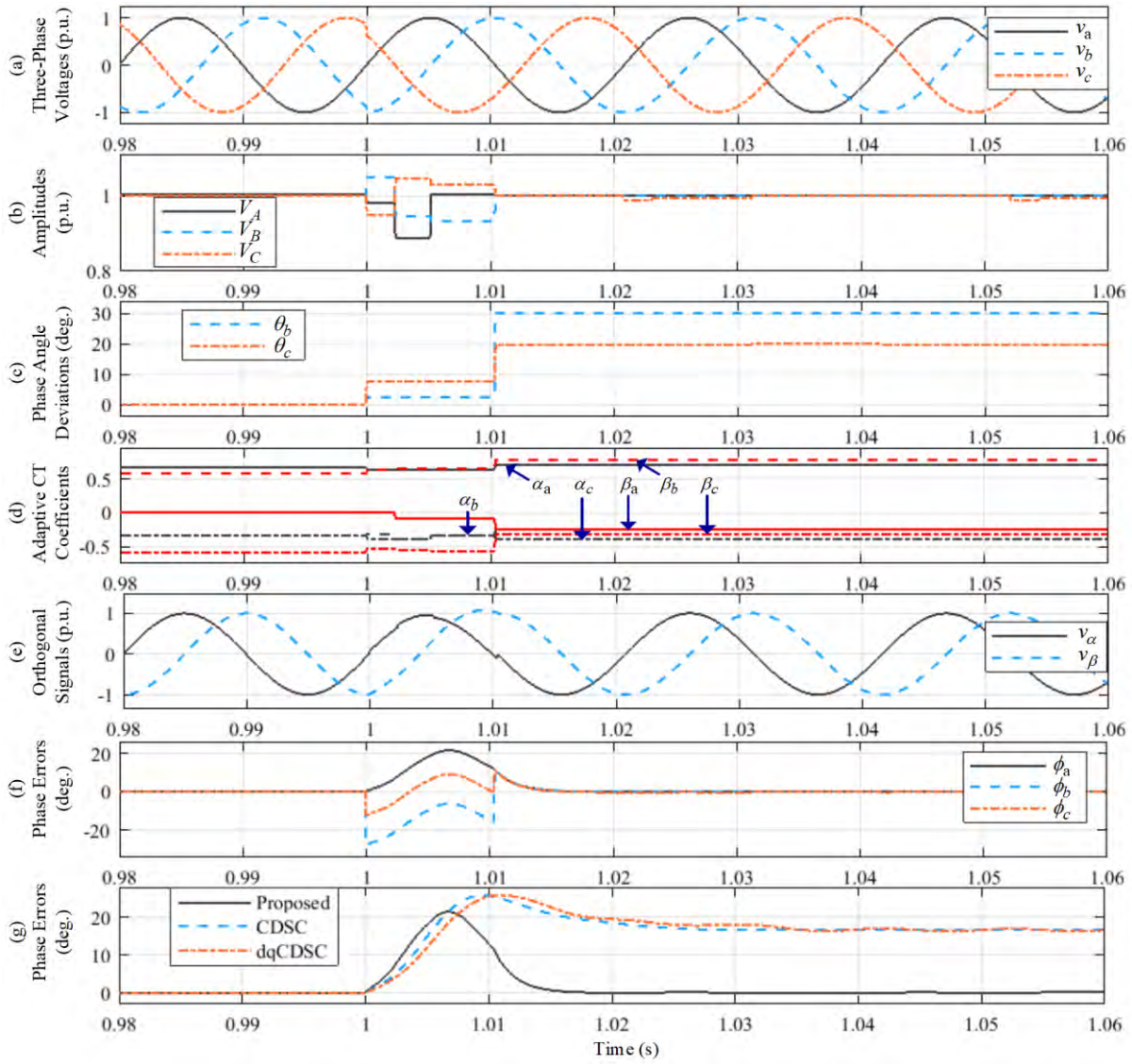

Fig. 4.7 Simulated results when phase steps ($\theta_b = +30°$, $\theta_c = +20°$) and frequency steps (-2 Hz) are created at t=1s from balanced condition. (a) Three-Phase Voltages (p.u.) (b) Amplitudes (p.u.) (c) Phase Angle Deviations (deg.) (d) Adaptive CT Coefficients (e) Orthogonal Signals (p.u.) (f) Phase Errors (deg.) (g) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

4.2.8 Case 8: Amplitude, Phase and Frequency Steps

This case reveals the performance of the proposed technique when an unbalanced amplitude, phase angle deviations and frequency steps occur simultaneously in input voltages.

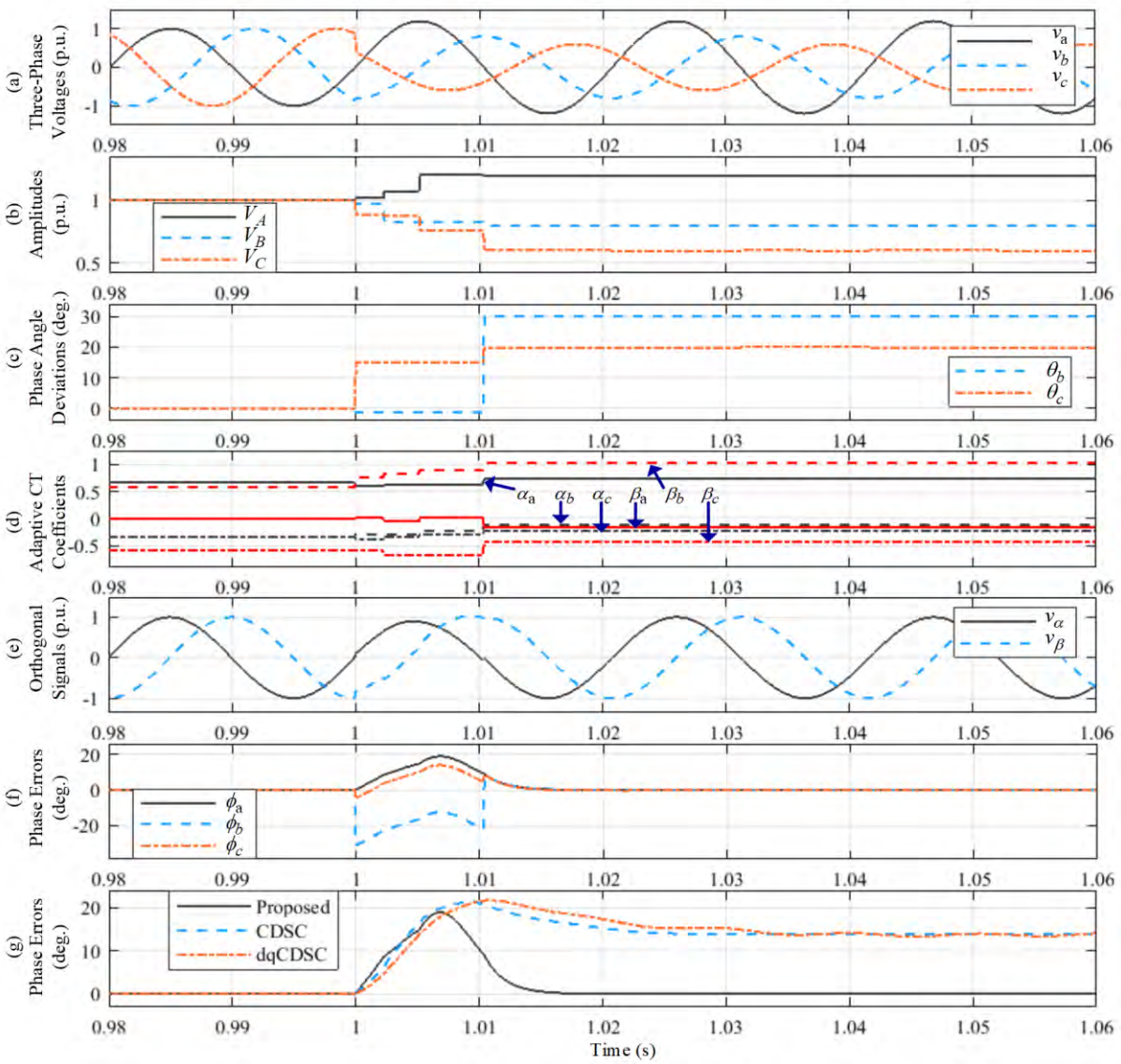

Fig. 4.8 Simulated results when an amplitude (v_a = 20%, v_b = -20%, v_c = -40%), phase deviation (θ_b = +30°, θ_c = +20°), and frequency (-2 Hz) steps are created at t=1s from balanced condition. (a) Three-Phase Voltages (p.u.) (b) Amplitudes (p.u.) (c) Phase Angle Deviations (deg.) (d) Adaptive CT Coefficients (e) Orthogonal Signals (p.u.) (f) Phase Errors (deg.) (g) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

As it can be seen in Fig. 4.8(a), amplitude steps (v_a = 20%, v_b = -20%, v_c = -40%), phase deviation steps (θ_b = +30°, θ_c = +20°), and frequency step (-2 Hz) are created in the three phase input voltages at t=1s. Fig. 4.8(b) and Fig. 4.8(c) show that the proposed technique can estimate the unbalanced amplitudes and phase angle deviations of the voltages after the step change with a transient time of 10 ms. Fig. 4.8(d) dictates that the coefficients of CT matrix changes adaptively after the step change in order to generate orthogonal signals and Fig. 4.8(e)

demonstrates the orthogonal signals. Finally, Fig. 4.8(f) illustrates the phase angle estimation errors of all three phases. Additionally, in Fig. 4.8(g), comparison of the proposed method with CDSC and *dq*CDSC is shown, which reflects that the proposed technique can track phase angle accurately for the whole time, whereas CDSC and *dq*CDSC methods fail to do so with around 14° offset error after the step change.

4.2.9 Case 9: Random Step Changes in Amplitudes

At t=1s, amplitude steps (V_a = 20%, V_b = -20%, V_c = -40%) are created in the three-phases, again at t=1.04s, amplitude steps (V_a = -30%, V_b = +40%, V_c = +30%) are created in the three-phases, which is shown in Fig. 4.9(a). From the Fig. 4.9(b)-(e), it is seen that the proposed PLL can estimate the amplitudes and phase-angle deviations, produce orthogonal voltages by updating the coefficients of the CT matrix, estimate instantaneous phases of the three-phase voltages with a transient period of 10 ms during the both step changes. Fig. 4.9(f) presents the performance comparison among proposed, CDSC and *dq*CDSC PLL, which depicts that all the three PLLs generate accurate instantaneous phases. The proposed PLL takes around 10 ms, whereas the CDSC and *dq*CDSC methods take around 20 ms as transient time after the step change occurs.

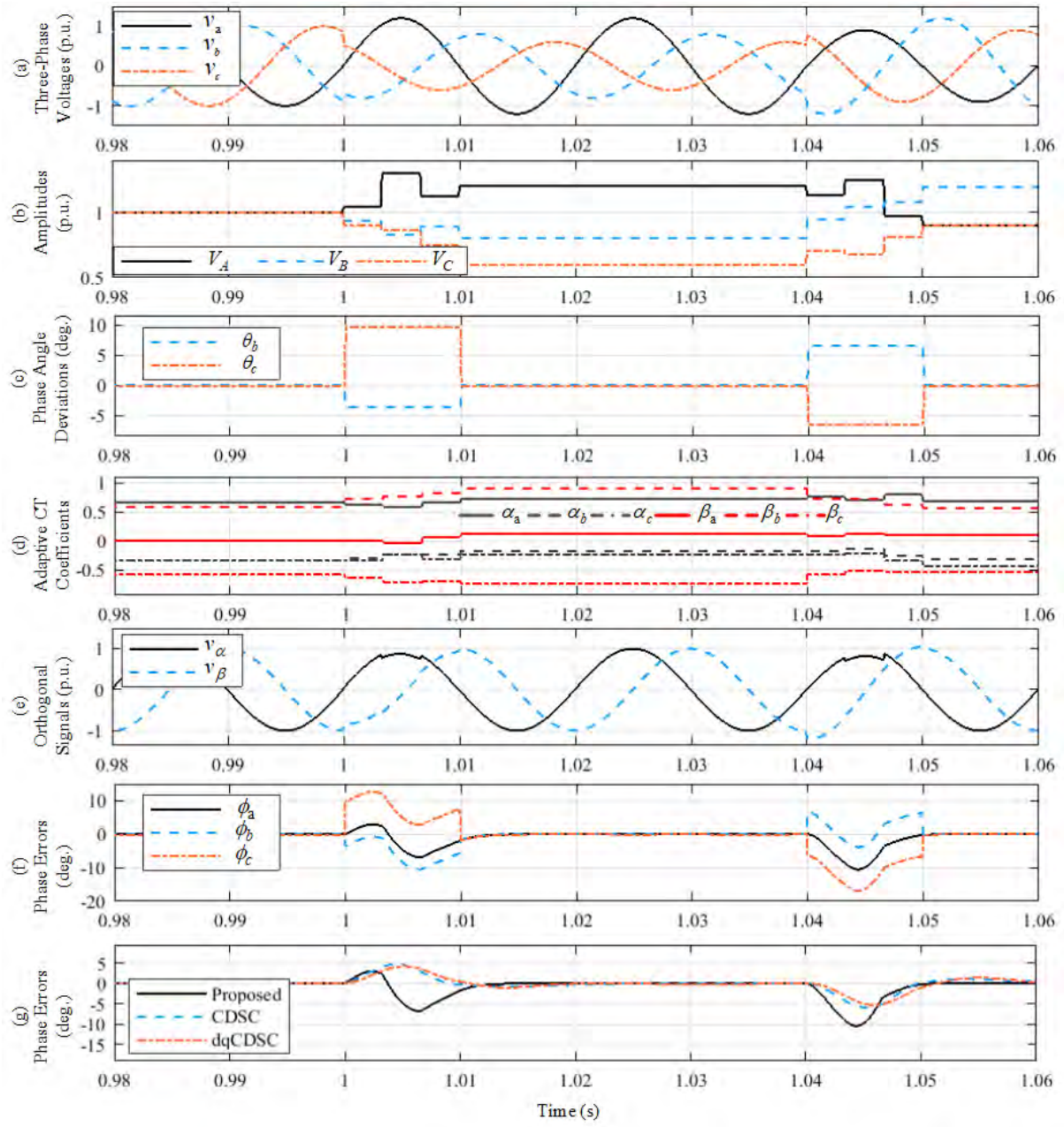

Fig. 4.9 Simulated results when an amplitude steps (V_a = 20%, V_b = -20%, V_c = -40%) and (V_a = -30%, V_b = +40%, V_c = +30%) are created at t=1s and t=1.04s, respectively from balanced condition. (a) Three-Phase Voltages (p.u.) (b) Amplitudes (p.u.) (c) Phase Angle Deviations (deg.) (d) Adaptive CT Coefficients (e) Orthogonal Signals (p.u.) (f) Phase Errors (deg.) (g) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

4.3 Performance of the Proposed Method in Presence of Harmonics and DC Offset

The simulation results are carried out using MATLAB/ Simulink software. For simulation purposes, the grid frequency is set to 50 Hz, the three-phase voltage amplitude is normalized to 1 p.u., and sampling frequency is set to 10 kHz. The 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonic components are considered to add harmonics and their amplitudes are selected as 5% (THD= 10%) of fundamental voltage amplitudes.

4.3.1 Case 1: Balanced System Distorted by Harmonics

Fig. 4.10 demonstrates the performance of the proposed PLL for a balanced normalized input voltages distorted by harmonics. In each phase, 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic components are considered and the amplitude of each harmonic is selected as 5% of input signals amplitudes to add harmonics. Fig. 4.10(a) shows the input three phase balanced voltages incorporating harmonics. Each phase is marked using different notation that is mentioned in the legend of the figure. The output after the BPF block is shown in Fig. 4.10(b), which shows that the harmonics have been attenuated from the input voltages to get the fundamental voltage signals. The amplitudes of the filtered signal are obtained from amplitudes estimation block in Simulink and the results are depicted in Fig. 4.10(c), which shows the normalized amplitudes of three phase filtered signals. Fig. 4.10(d) shows the phase angle deviations of the input voltages. As the input voltages are balanced, the phase angle deviations should be zero. However, the predictions of phase angle deviations contain errors less than 0.1°. The coefficients of ACT are obtained and shown in Fig. 4.10(e). The coefficients are constant during the simulation time, as the signals are balanced. Now, the orthogonal $\alpha\beta$-signals are obtained by multiplying the coefficients with the input filtered voltages. As seen in Fig. 4.10(f), the proposed PLL generates orthogonal signals without any major distortions. In Fig. 4.10(g), the estimated instantaneous phase errors are drawn for three phase voltages. As it is seen, the estimated phases contain small ripples, however, the errors due to the ripples are less than 0.1° which are negligible. Finally, Fig. 4.10(h) contains the comparison analysis of the proposed PLL with CDSC, and *dq*CDSC PLLs. From the comparison, it is seen that CDSC and *dq*CDSC PLLs have less ripple than the proposed PLL.

4.3.2 Case 2: Amplitude Unbalanced Signals Distorted by Harmonics

Fig. 4.11 demonstrates the performance of the proposed PLL when amplitudes of input voltages undergo sudden changes. For the simulation purpose, the three-phase amplitude steps (v_a =-0.1 p.u, v_b= -0.3 p.u, v_c= -0.5 p.u.) are created in input voltages and corresponding voltages are shown in Fig. 4.11(a). The same amount of harmonics is considered to add harmonics in each phase. The output after the BPF block is shown in Fig. 4.11(b), which shows that the harmonics have been attenuated from the input voltages to get the fundamental voltage signals. The amplitudes of the filtered signal are obtained from amplitudes estimation block in Simulink and the results are depicted in Fig. 4.11(c), which shows that the method tracks the amplitudes of three phases with 50 ms of transient time after the step changes occur. Fig. 4.11(d) depicts the phase angle deviations of input voltages. After the step changes, the proposed algorithm takes 50 ms as transient period to track the phase angle deviations. The coefficients of ACT are obtained and shown in Fig. 4.11(e). The coefficients have constant values before the step occur, but changed after the amplitude step occur. As seen in Fig. 4.11(f), the proposed PLL generates orthogonal $\alpha\beta$-signals with small distortions during the step change. In Fig. 4.11(g), the estimated instantaneous phase errors are drawn for three phase voltages. As it is seen, the proposed PLL can track the three phases with around 55 ms transient time after the step change. Finally, Fig. 4.11(h) contains the comparison analysis of the proposed PLL with CDSC, and *dq*CDSC PLLs. From the comparison, it is seen that the proposed PLL have larger transient steps but smaller offset error than CDSC and *dq*CDSC PLLs. All the PLLs need same amount of transient time (60 ms) before reaching the steady state.

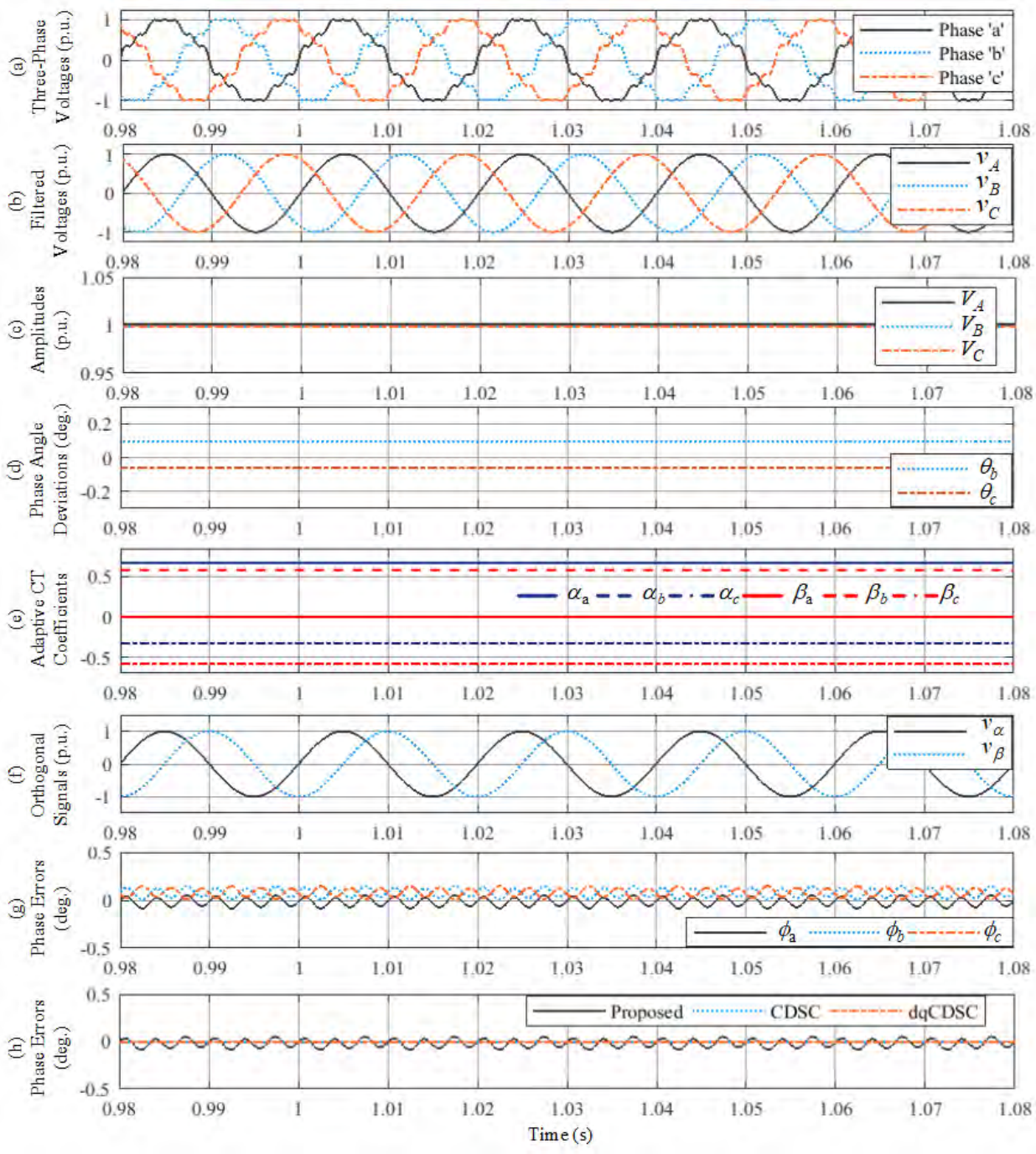

Fig. 4.10 Simulated results for balanced inputs in presence of harmonics. (a) Three-Phase Voltages (p.u.) (b) Three-Phase Filtered Voltages (p.u.) (c) Amplitudes (p.u.) (d) Phase Angle Deviations (deg.) (e) Adaptive CT Coefficients (f) Orthogonal Signals (p.u.) (g) Phase Errors (deg.) (h) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

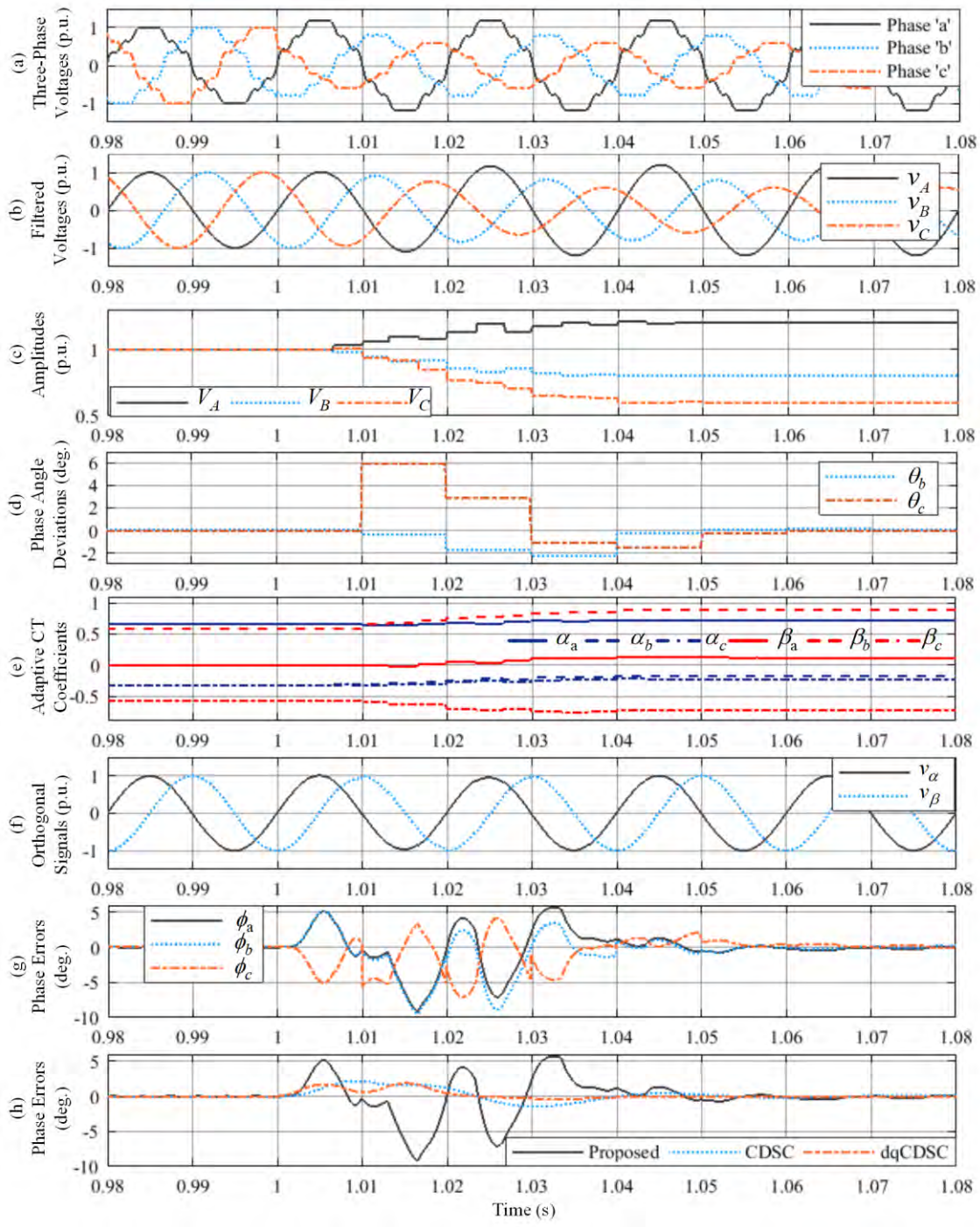

Fig. 4.11 Simulated results when an amplitude steps (v_a = 20%, v_b = -20%, v_c = -40%) are created at t=1s. (a) Input Voltages (p.u.) (b) Filtered Voltages (p.u.) (c) Amplitudes (p.u.) (d) Phase Angle Deviations (deg.) (e) Adaptive CT Coefficients (f) Orthogonal Signals (p.u.) (g) Phase Errors (deg.) (h) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

4.3.3 Case 3: Phase Unbalanced Signals Distorted by Harmonics

The experimental performances of the proposed PLL for unequal phase-angle deviations are presented in Fig. 4.12. To create phase unbalances, +30° and +20° unequal phase-angle deviations are inserted in phase 'b' and 'c' voltages, respectively and corresponding voltages are shown in Fig. 4.12(a). The same amount of harmonics is considered to add harmonics in each phase. The output after the BPF block is shown in Fig. 4.12(b), which shows that the harmonics have been attenuated from the input voltages to get the fundamental voltage signals. The amplitudes of the filtered signal is obtained from the amplitudes estimation block in Simulink and the results are depicted in Fig. 4.12(c), which shows that the method tracks the amplitudes of three phases with 60 ms of transient time after the step changes occur. Fig. 4.12(d) depicts the phase angle deviations of input voltages. After the step changes, the proposed algorithm takes 60 ms as transient period to track the phase angle deviations. The coefficients of Adaptive CT are obtained and shown in Fig. 4.12(e). The coefficients have constant values before the step occur, but changed after the phase angle step occur. As seen in Fig. 4.12(f), the proposed PLL generates orthogonal $\alpha\beta$-signals with small distortions during the step change. In Fig. 4.12(g), the estimated instantaneous phase errors are drawn for three phase voltages. As it is seen, the proposed PLL can track the three phases with around 60 ms transient time after the step change. Finally, Fig. 4.12(h) contains the comparison analysis of the proposed PLL with CDSC, and *dq*CDSC PLLs. From the comparison, it is seen that the proposed PLL can track the phases information with 60 ms of transient period but the CDSC and *dq*CDSC PLLs produce around 17° offset error after the step change.

4.3.4 Case 4: Effects of Off-Nominal Frequencies and Harmonics in Balanced Signals

Fig. 4.13 demonstrates the performance of the proposed PLL when frequency of input voltages undergo sudden changes. For the simulation purpose, a frequency step (-2 Hz) is created in input voltages and corresponding signals are shown in Fig. 4.13(a). The same amount of harmonics is considered to add harmonics in each phase. The output after the BPF block is shown in Fig. 4.13(b), which shows that the harmonics have been attenuated from the input voltages to get the fundamental voltage signals. The amplitudes of the filtered signal are depicted in Fig. 4.13(c), which shows that the method tracks the amplitudes of three phases with 60 ms of transient time after the step changes occur, which contain ripples. The amplitudes are truncated in a small fraction by BPF due to the presence of off-nominal frequency, however, it has no effect on phase estimation. Fig. 4.13(d) depicts the phase angle deviations of input

voltages. After the step changes, the proposed algorithm takes 60 ms as transient period to track the phase angle deviations. The coefficients of ACT are obtained and shown in Fig. 4.13(e). The coefficients have constant values before the step occur, but changed after the phase angle step occur. As seen in Fig. 4.13(f), the proposed PLL generates orthogonal $\alpha\beta$-signals with small distortions during the step change. In Fig. 4.13(g), the estimated instantaneous phase errors are drawn for three phase voltages. As it is seen, the proposed PLL can track the three phases with around 60 ms transient time after the step change, which contain ripples. Finally, Fig. 4.13(h) shows the comparison analysis of the proposed PLL with CDSC, and *dq*CDSC PLLs. From the comparison, it is seen that the proposed PLL, CDSC and *dq*CDSC PLLs have almost similar performances due to sudden frequency changes.

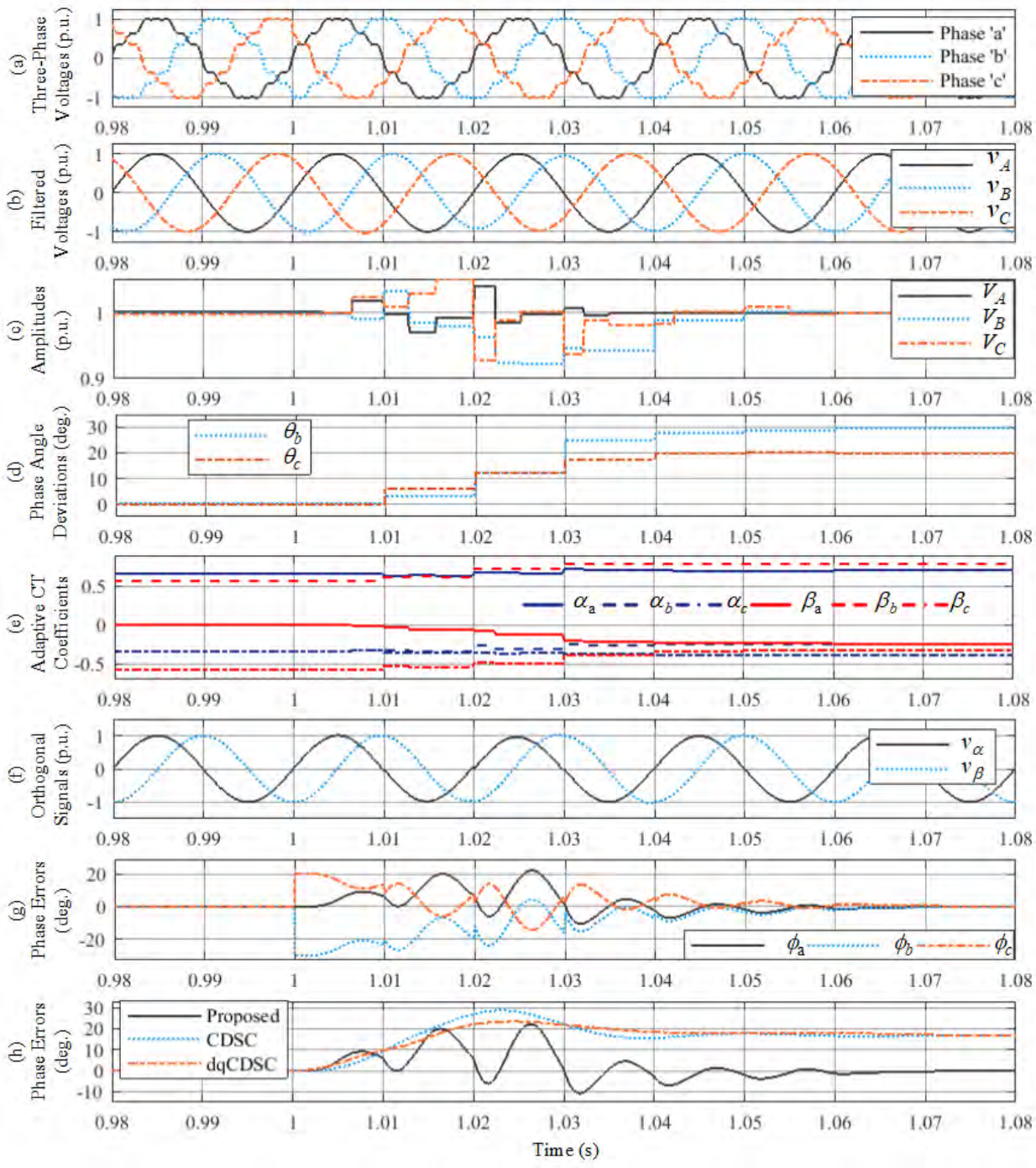

Fig. 4.12 Simulated results when phase deviation step ($\theta_b = +30°$, $\theta_c = +20°$) are created at t=1s. (a) Input Voltages (p.u.) (b) Filtered Voltages (p.u.) (c) Amplitudes (p.u.) (d) Phase Angle Deviations (deg.) (e) Adaptive CT Coefficients (f) Orthogonal Signals (p.u.) (g) Phase Errors (deg.) (h) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

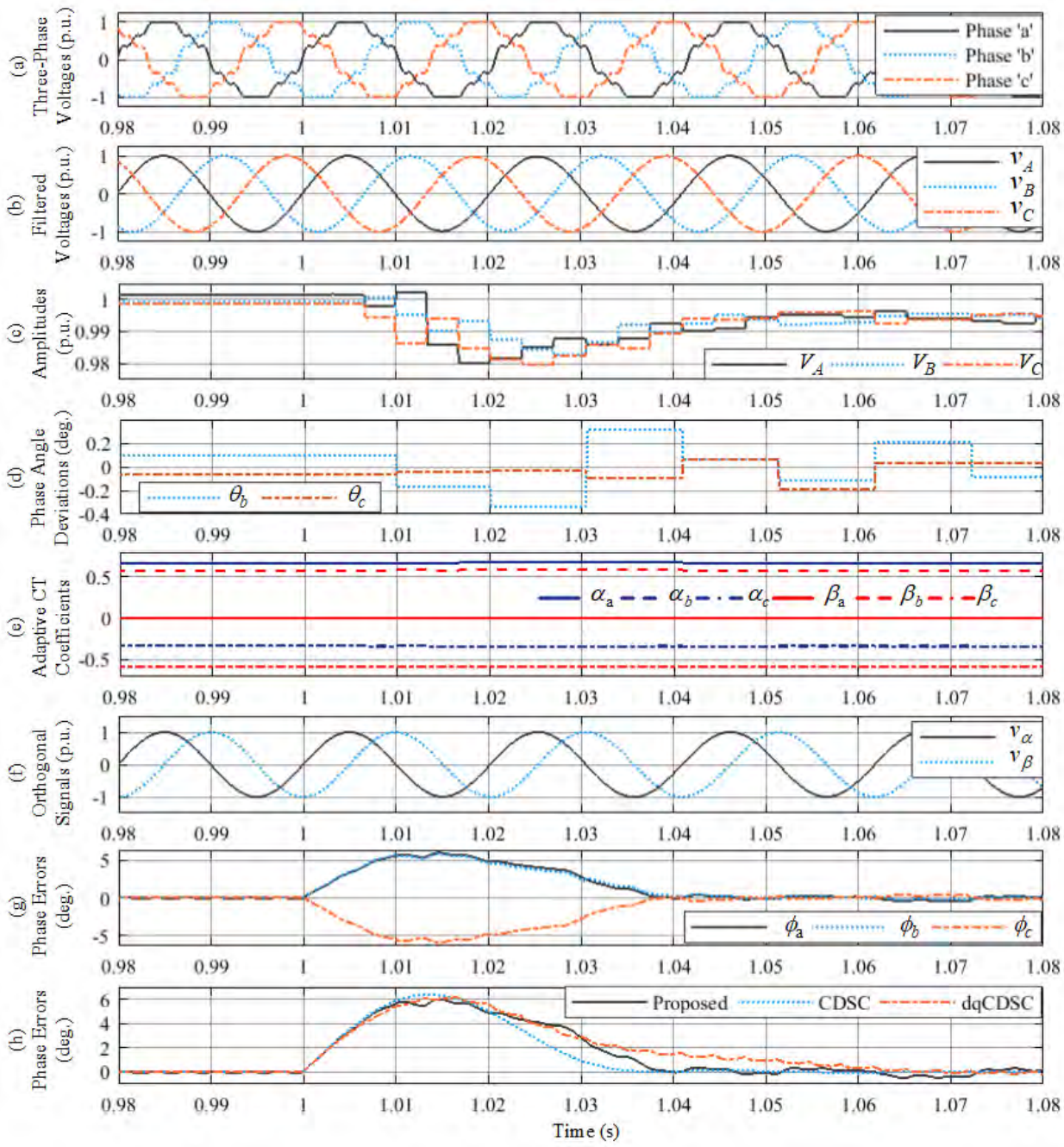

Fig. 4.13 Simulated results when a frequency step (-2 Hz) is created in each phase simultaneously at t=1s. (a) Input Voltages (p.u.) (b) Filtered Voltages (p.u.) (c) Amplitudes (p.u.) (d) Phase Angle Deviations (deg.) (e) Adaptive CT Coefficients (f) Orthogonal Signals (p.u.) (g) Phase Errors (deg.) (h) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

4.3.5 Case 5: Both Amplitude and Phase Unbalanced Signals Distorted by Harmonics

The effectiveness of the suggested PLL is demonstrated in this case, when input voltages experience abrupt change in both amplitudes and phases. The amplitude are changed by a step of (v_a = -0.1 p.u, v_b = -0.3 p.u, v_c = -0.5 p.u.), and phases by (θ_b = +30°, θ_c = +20°), and output performances are shown in Fig. 4.14. The same amount of harmonics is considered to add harmonics in each phase. The output after the BPF block is shown in Fig. 4.14(b), which shows that the harmonics have been attenuated from the input voltages to get the fundamental voltage signals. The amplitudes of the filtered signal is obtained from amplitudes estimation block in Simulink and the results are depicted in Fig. 4.14(c), which shows that the method tracks the amplitudes of three phases with 60 ms of transient time after the step changes occur. Fig. 4.14(d) depicts the phase angle deviations of input voltages. After the step changes, the proposed algorithm takes 60 ms as transient period to track the phase angle deviations. The coefficients of ACT are obtained and shown in Fig. 4.14(e). The coefficients have constant values before the step occur, but changed after the phase angle step occur. As seen in Fig. 4.14(f), the proposed PLL generates orthogonal $\alpha\beta$-signals with small distortions during the step change. In Fig. 4.14(g), the estimated instantaneous phase errors are drawn for three phase voltages. As it is seen, the proposed PLL can track the three phases with around 60 ms transient time after the step change. Finally, Fig. 4.14(h) contains the comparison analysis of the proposed PLL with CDSC, and *dq*CDSC PLLs. From the comparison, it is seen that the proposed PLL can track the phases information with 60 ms of transient period but the CDSC and *dq*CDSC PLLs produce around 14° offset error after the step change.

4.3.6 Case 6: Effects of Off-Nominal Frequencies and Harmonics in Amplitude Unbalanced Signals

Fig. 4.15 demonstrates the performance of the proposed PLL when both the amplitude and frequency of the input voltages undergo sudden changes. In this case, Amplitude steps (v_a = -0.1 p.u, v_b = -0.3 p.u, v_c = -0.5 p.u.) and frequency step (-2 Hz) are created simultaneously at t=1s in input voltages, and the corresponding experimental waveforms are shown in Fig. 4.15(a). The same amount of harmonics is considered to add harmonics in each phase. The output after the BPF block is shown in Fig. 4.15(b), which shows that the harmonics have been attenuated from the input voltages to get the fundamental voltage signals. The amplitudes of the filtered signal are depicted in Fig. 4.15(c), which shows that the method tracks the amplitudes of three phases with 60 ms of transient time after the step changes occur. Fig. 4.15(d) depicts the phase

angle deviations of input voltages. After the step changes, the proposed algorithm takes 60 ms as transient period to track the phase angle deviations. The coefficients of ACT are obtained and shown in Fig. 4.15(e). The coefficients have constant values before the step occur, but changed after the amplitude step occur. As seen in Fig. 4.15(f), the proposed PLL generates orthogonal $\alpha\beta$-signals with small distortions during the step change. In Fig. 4.15(g), the estimated instantaneous phase errors are drawn for three phase voltages. As it is seen, the proposed PLL can track the three phases with around 55 ms transient time after the step change. Finally, Fig. 4.15(h) contains the comparison analysis of the proposed PLL with CDSC, and *dq*CDSC PLLs. From the comparison, it is seen that the proposed PLL, CDSC and *dq*CDSC PLLs have almost similar performances due to sudden amplitude and frequency changes.

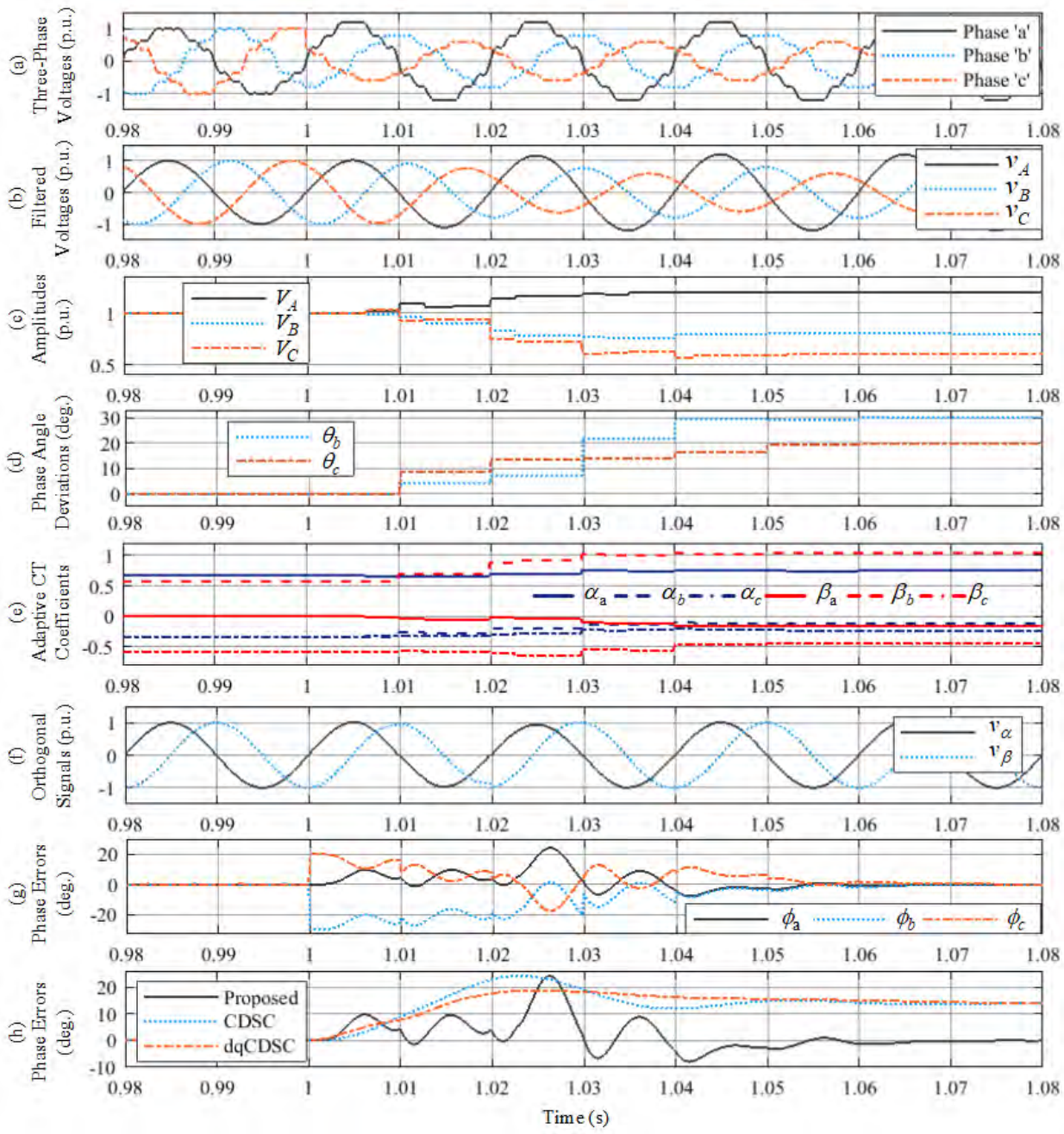

Fig. 4.14 Simulated results when an amplitude step (v_a = 20%, v_b = -20%, v_c = -40%) and phase deviation (θ_b = +30°, θ_c = +20°) are created simultaneously at t=1s. (a) Input Voltages (p.u.) (b) Filtered Voltages (p.u.) (c) Amplitudes (p.u.) (d) Phase Angle Deviations (deg.) (e) Adaptive CT Coefficients (f) Orthogonal Signals (p.u.) (g) Phase Errors (deg.) (h) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

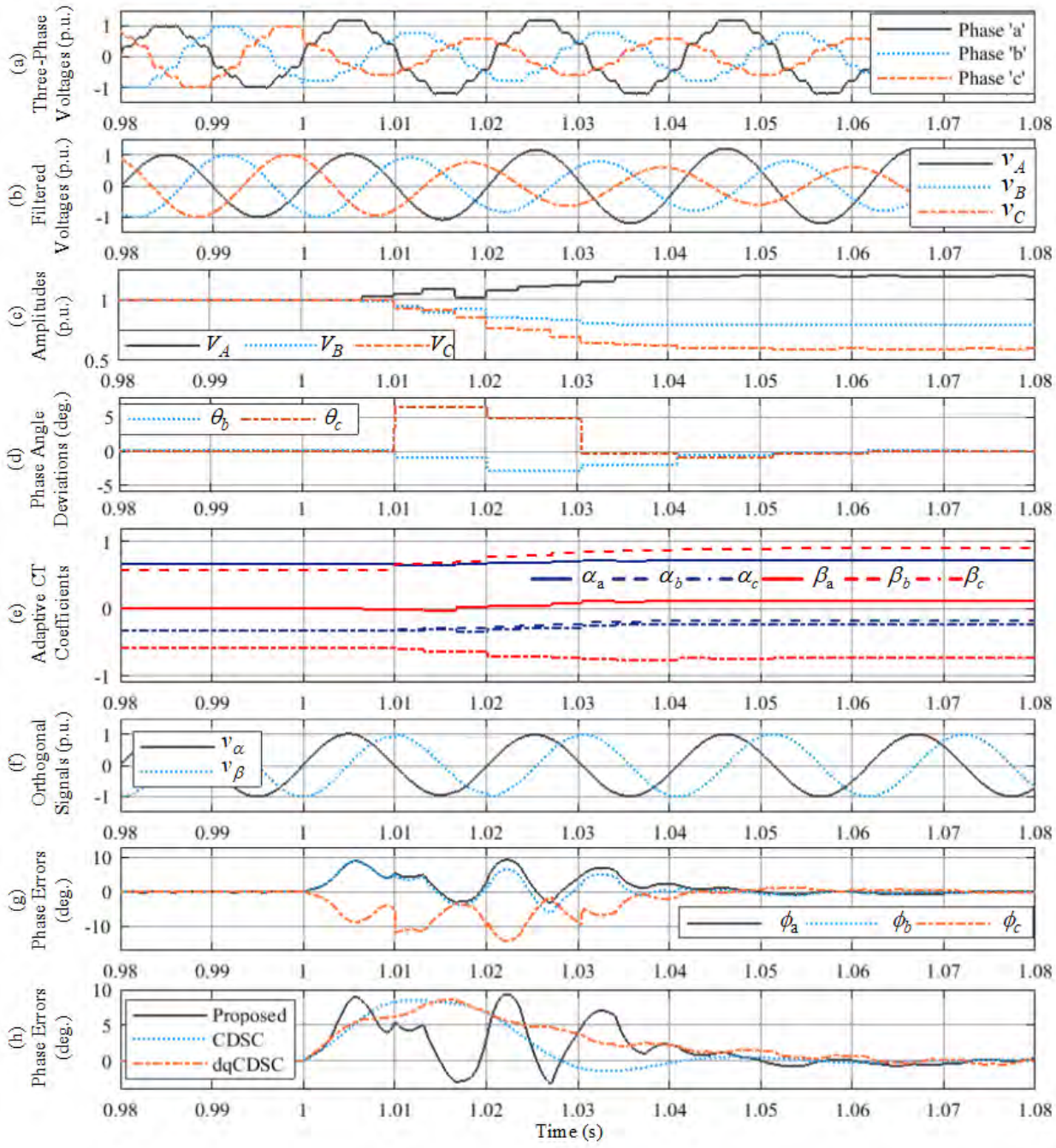

Fig. 4.15 Simulated results when an amplitude step (v_a = 20%, v_b = -20%, v_c = -40%) and frequency steps (-2 Hz) are created simultaneously at t=1s. (a) Input Voltages (p.u.) (b) Filtered Voltages (p.u.) (c) Amplitudes (p.u.) (d) Phase Angle Deviations (deg.) (e) Adaptive CT Coefficients (f) Orthogonal Signals (p.u.) (g) Phase Errors (deg.) (h) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

4.3.7 Case 7: Effects of Off-Nominal Frequencies and Harmonics in Phase Unbalanced Signals

The effectiveness of the suggested PLL is demonstrated in this case, when input voltages experience abrupt change in both phases and frequency. Both the phase and the frequency steps are formed concurrently as follows: +30°, +20° phase steps, respectively in phase 'b' and 'c', and -2Hz frequency step and the output performances are shown in Fig. 4.16. The same amount of harmonics is considered to add harmonics in each phase. The output after the BPF block is shown in Fig. 4.16(b), which shows that the harmonics have been attenuated from the input voltages to get the fundamental voltage signals. The amplitudes of the filtered signal are depicted in Fig. 4.16(c), which shows that the method tracks the amplitudes of three phases with 60 ms of transient time after the step changes occur. Fig. 4.16(d) depicts the phase angle deviations of input voltages. After the step changes, the proposed algorithm takes 60 ms as transient period to track the phase angle deviations. The coefficients of ACT are obtained and shown in Fig. 4.16(e). The coefficients have constant values before the step occur, but changed after the phase angle step occur. As seen in Fig. 4.16(f), the proposed PLL generates orthogonal $\alpha\beta$-signals with small distortions during the step change. In Fig. 4.16(g), the estimated instantaneous phase errors are drawn for three phase voltages. As it is seen, the proposed PLL can track the three phases with around 60 ms transient time after the step change. Finally, Fig. 4.16(h) contains the comparison analysis of the proposed PLL with CDSC, and *dq*CDSC PLLs. From the comparison, it is seen that the proposed PLL can track the phases information with 60 ms of transient period but the CDSC and *dq*CDSC PLLs produce around 14° offset error after the step change.

4.3.8 Case 8: Effects of Off-Nominal Frequencies and Harmonics in Both Amplitude and Phase Unbalanced Signals

In this case, a combination of amplitude (v_a = -0.1 p.u, v_b = -0.3 p.u, v_c = -0.5 p.u.), phase (θ_b = +30°, θ_c = +20°), and frequency steps (-2 Hz) are inserted in input voltages and corresponding dynamic performance is shown in Fig. 4.17. The same amount of harmonics are considered to add harmonics in each phase. The output after the BPF block is shown in Fig. 4.17(b), which shows that the harmonics have been attenuated from the input voltages to get the fundamental voltage signals. The amplitudes of the filtered signal are depicted in Fig. 4.17(c), which shows that the method tracks the amplitudes of three phases with 60 ms of transient time after the step changes occur. The amplitudes are truncated in a small fraction by BPF due to the presence of off-nominal frequency, however, it has no effect on phase estimation. Fig. 4.17(d) depicts the

phase angle deviations of input voltages. After the step changes, the proposed algorithm takes 60 ms as transient period to track the phase angle deviations. The coefficients of Adaptive CT are obtained and shown in Fig. 4.17(e). The coefficients have constant values before the step occur, but changed after the phase angle step occur. As seen in Fig. 4.17(f), the proposed PLL generates orthogonal $\alpha\beta$-signals with small distortions during the step change. In Fig. 4.17(g), the estimated instantaneous phase errors are drawn for three phase voltages. As it is seen, the proposed PLL can track the three phases with around 60 ms transient time after the step change. Finally, Fig. 4.17(h) contains the comparison analysis of the proposed PLL with CDSC, and *dq*CDSC PLLs. From the comparison, it is seen that the proposed PLL can track the phases information with 60 ms of transient period but the CDSC and *dq*CDSC PLLs produce around 14° offset error after the step change.

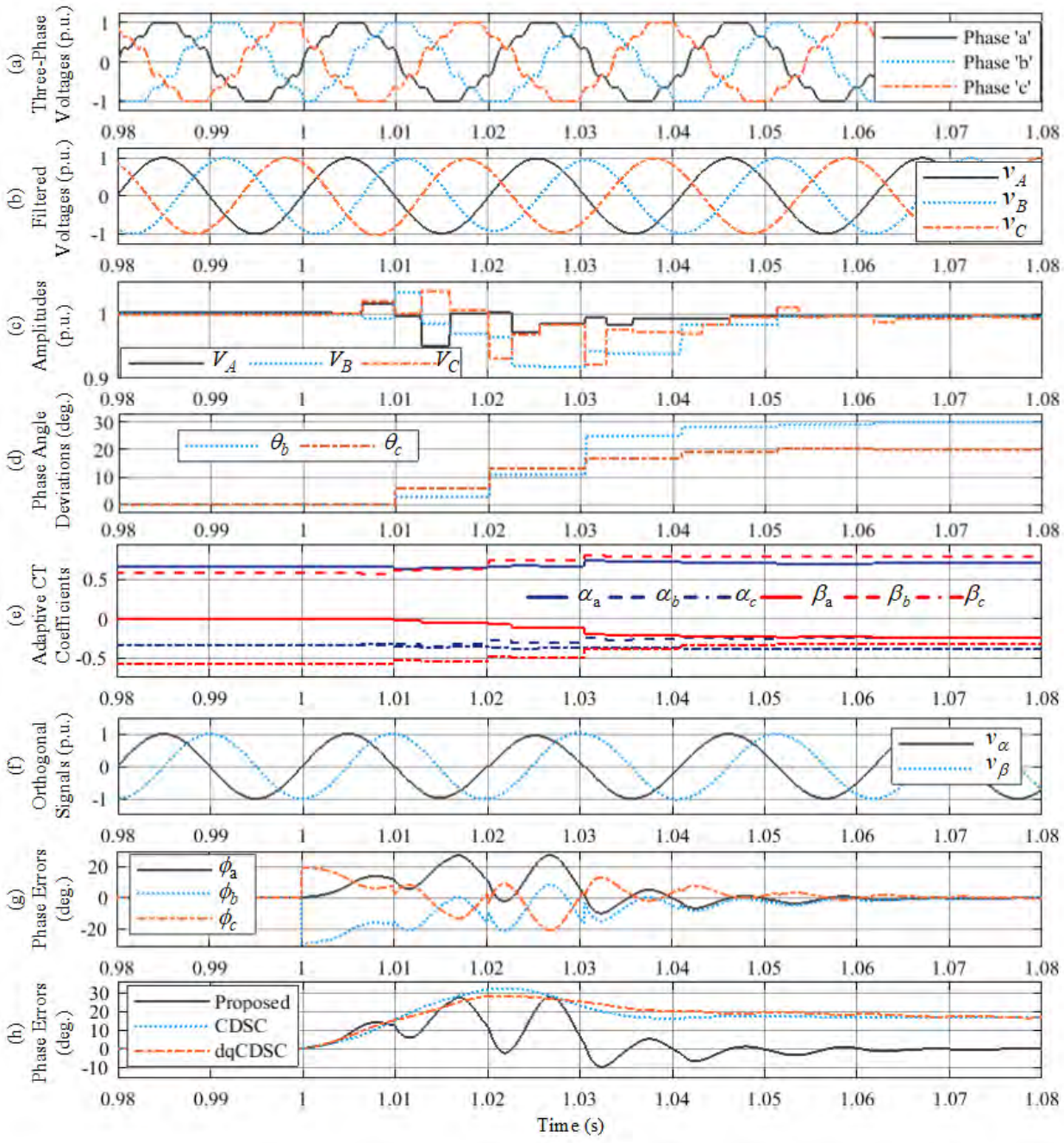

Fig. 4.16 Simulated results when a phase deviation ($\theta_b = +30°$, $\theta_c = +20°$) and frequency steps (-2 Hz) are created simultaneously at t=1s. (a) Input Voltages (p.u.) (b) Filtered Voltages (p.u.) (c) Amplitudes (p.u.) (d) Phase Angle Deviations (deg.) (e) Adaptive CT Coefficients (f) Orthogonal Signals (p.u.) (g) Phase Errors (deg.) (h) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

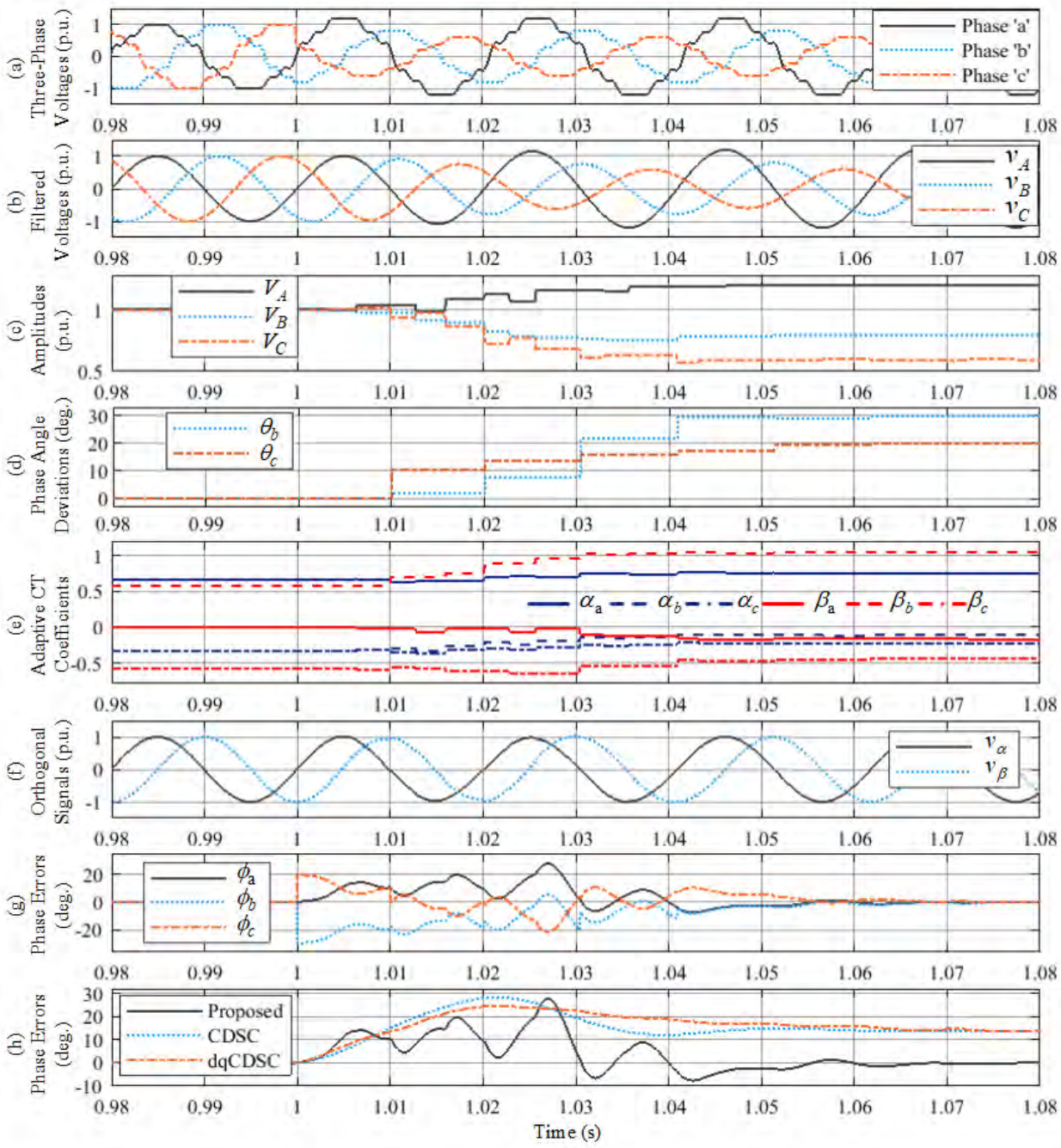

Fig. 4.17 Simulated results when an amplitude step (v_a = 20%, v_b = -20%, v_c = -40%), phase deviation (θ_b = +30°, θ_c = +20°), and frequency steps (-2 Hz) are created simultaneously at t=1s. (a) Input Voltages (p.u.) (b) Filtered Voltages (p.u.) (c) Amplitudes (p.u.) (d) Phase Angle Deviations (deg.) (e) Adaptive CT Coefficients (f) Orthogonal Signals (p.u.) (g) Phase Errors (deg.) (h) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

4.3.9 Case 9: DC Offset

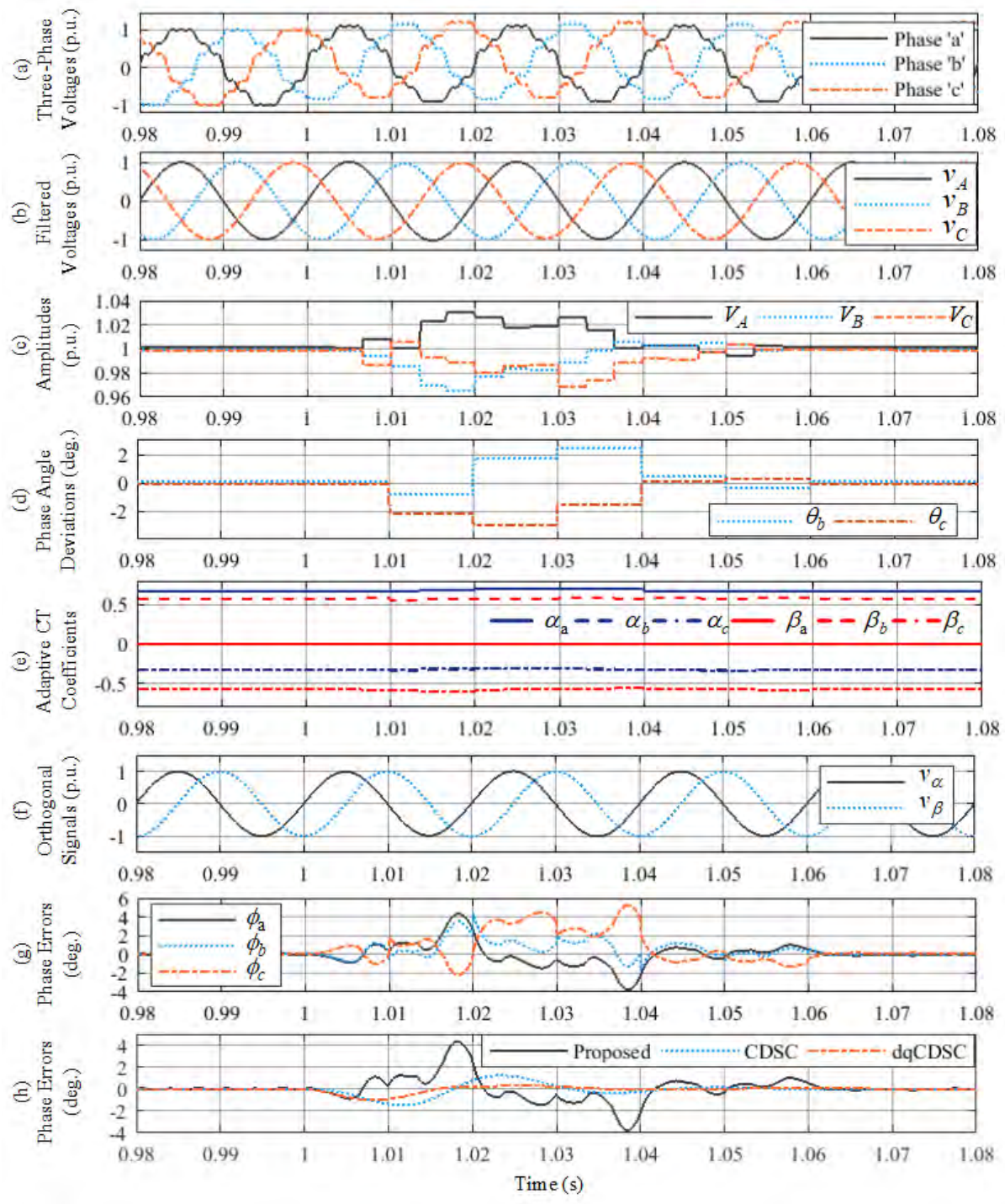

Fig. 4.18 Simulated results when DC offset (10%, 15%, 20%) are created simultaneously at t=1s. (a) Input Voltages (p.u.) (b) Filtered Voltages (p.u.) (b) Amplitudes (p.u.) (c) Phase Angle Deviations (deg.) (d) Adaptive CT Coefficients (e) Orthogonal Signals (p.u.) (f) Phase Errors (deg.) (g) Comparison of phase errors among Proposed, CDSC, and *dq*CDSC methods.

Fig. 4.18 demonstrates the performance of the proposed PLL when input voltages contain DC offset. For the simulation purpose, DC offset (10%, 15%, 20%) are created at t=1s in input voltages and corresponding signals are shown in Fig. 4.18(a). The same amount of harmonics is considered to add harmonics in each phase. The output after the BPF block is shown in Fig. 4.18(b), which shows that the harmonics have been attenuated from the input voltages to get the fundamental voltage signals. The amplitudes of the filtered signal are depicted in Fig. 4.18(c), which shows that the method tracks the amplitudes of three phases with 60 ms of transient time after the changes occur. Fig. 4.18(d) depicts the phase angle deviations of input voltages. After the step changes, the proposed algorithm takes 60 ms as transient period to track the phase angle deviations. The coefficients of ACT are obtained and shown in Fig. 4.18(e). The coefficients have constant values before the change occur, but updated after the phase angle step occur. As seen in Fig. 4.18(f), the proposed PLL generates orthogonal $\alpha\beta$-signals with small distortions during the step change. In Fig. 4.18(g), the estimated instantaneous phase errors are drawn for three phase voltages. As it is seen, the proposed PLL can track the three phases with around 60 ms transient time after the step change, which contain ripples. Finally, Fig. 4.18(h) shows the comparison analysis of the proposed PLL with CDSC, and *dq*CDSC PLLs. From the comparison, it is seen that the CDSC and *dq*CDSC PLLs show better results than the proposed PLL.

4.4 Experimental Results

The performance of the proposed technique is evaluated by doing some experiments in this section. The experimental setup to implement the proposed method is shown in Fig. 4.19. A dSPACE DS1104 control board is employed to carry out the experiments. The real-time three-phase voltage signals are generated by using the digital-to-analog converter (DAC) of the DS1104. The produced voltage signals are then digitalized by the analog-to-digital converter (DAC) of the DS1104. An 8 channels Tektronix MSO58 oscilloscope is used for capturing the experimental results. The other parameters are kept as same as they are used in the simulation.

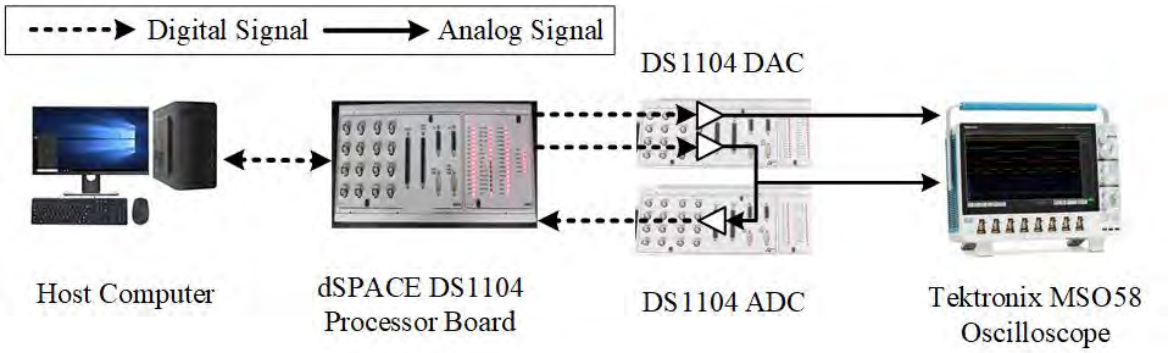

Fig. 4.19 Experimental Setup

4.5 Experimental Performance without Harmonics

4.5.1 Case 1: Amplitude Steps

The performance of the proposed PLL is shown in Fig. 4.20 for unbalanced amplitude steps in input voltages. To create the unbalances, amplitude steps of (+20%, -20% and -40%) are created in the input voltages. The phase angle deviations estimation is shown in the 2nd sub-figure of Fig. 4.20. Sub-figure 3 shows the estimated stationary $\alpha\beta$ orthogonal voltages. Finally, the phase estimation of phase 'a' is depicted in the last sub-figure, which shows that the PLL track the phase correctly without producing any error after the step changes.

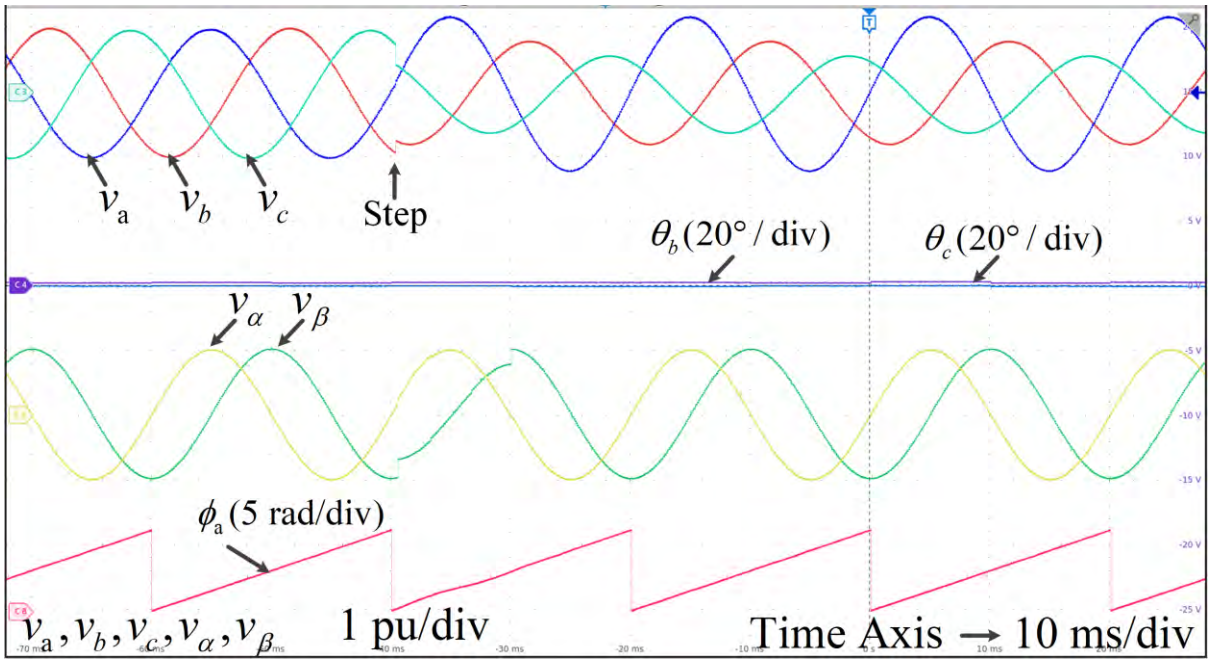

Fig. 4.20 Experimental performance of the proposed PLL method for unbalanced Amplitude steps (+20%, -20% and -40%).

4.5.2 Case 2: Phase Steps

The performance of the proposed PLL is shown in Fig. 4.21 for unbalanced phase steps in input voltages. To create the unbalances, phase steps of (θ_b=+20° and θ_c=-20°) are created in phase 'b' and phase 'c', respectively. The phase angle deviations estimation is shown in the 2nd sub-figure of Fig. 4.21. Sub-figure 3 shows the estimated stationary $\alpha\beta$ orthogonal voltages. Finally, the phase estimation of phase 'a' is depicted in the last sub-figure, which shows that the PLL track the phase correctly without producing any error during the step changes.

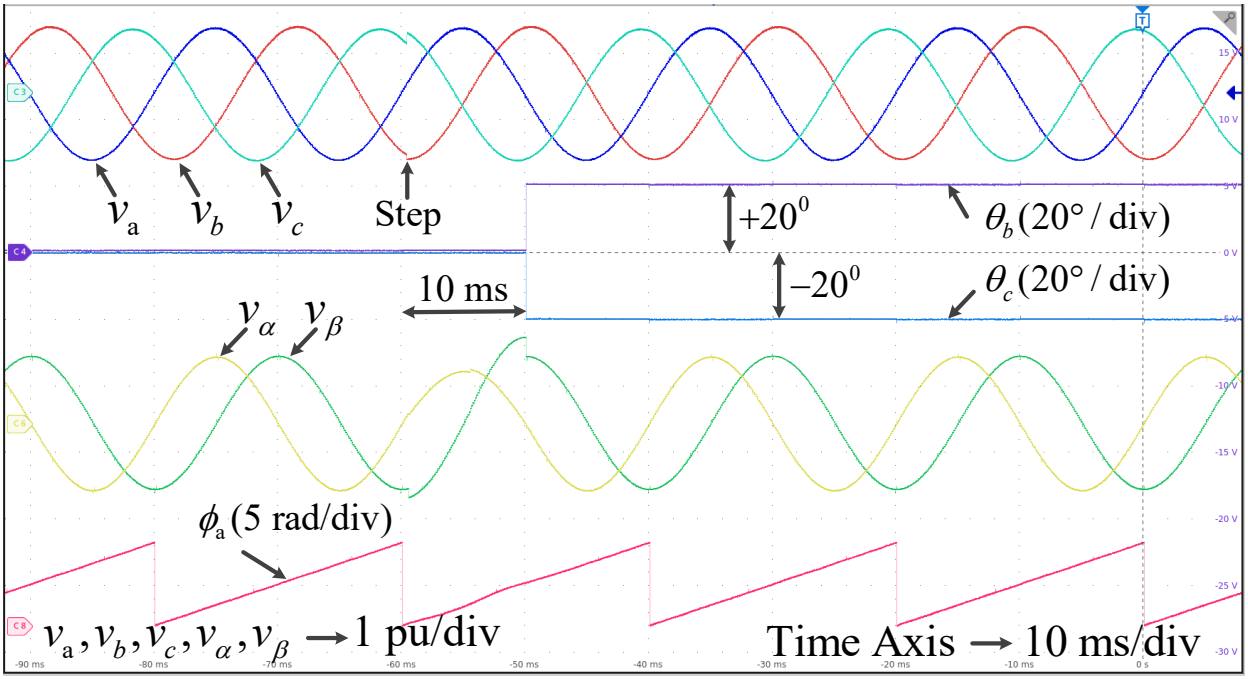

Fig. 4.21 Experimental performance of the proposed PLL method for unbalanced phase steps (θ_b=+20° and θ_c=-20°).

4.5.3 Case 3: Amplitude and Phase Steps

The performance of the proposed PLL is shown in Fig. 4.22 for unbalanced amplitude and phase steps in input voltages. To create the unbalances, amplitude steps (+20%, -20% and -40%) and phase steps of (θ_b=+20° and θ_c=-20°) are created in phase 'b' and phase 'c', respectively. The phase angle deviations estimation is shown in the 2nd sub-figure of Fig. 4.22. Sub-figure 3 shows the estimated stationary $\alpha\beta$ orthogonal voltages. Finally, the phase estimation of phase 'a' is depicted in the last sub-figure, which shows that the PLL track the phase correctly without producing any error during the step changes.

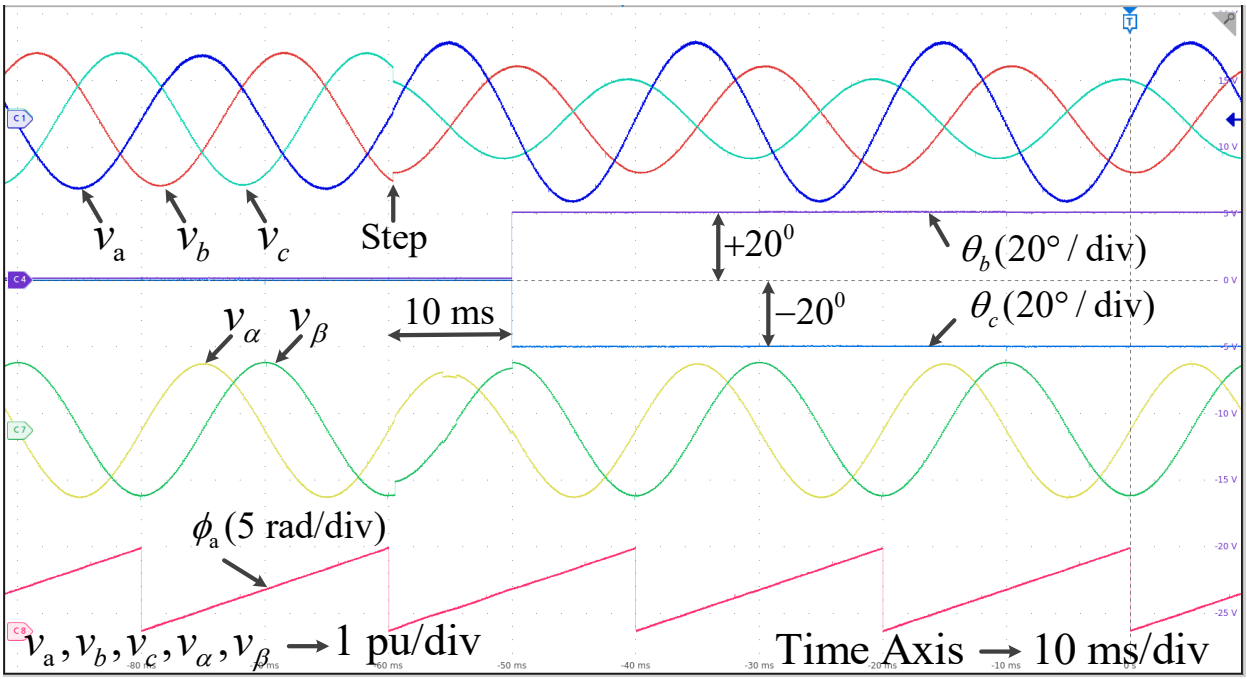

Fig. 4.22 Experimental performance of the proposed PLL method a combination of unbalanced amplitude steps (+20%, -20% and -40%) and unbalanced phase steps (θ_b=+20° and θ_c=-20°).

4.5.4 Case 4: Amplitude, Phase and Frequency Steps

The performance of the proposed PLL is shown in Fig. 4.23 for unbalanced amplitude and phase steps in input voltages. To create the unbalances, amplitude steps (+20%, -20% and -40%), unbalanced phase steps (θ_b=+20° and θ_c=-20°), and -2 Hz frequency step are induced in input voltages. The phase angle deviations estimation is shown in the 2nd sub-figure of Fig. 4.23. Sub-figure 3 shows the estimated stationary $\alpha\beta$ orthogonal voltages. Finally, the phase estimation of phase 'a' is depicted in the last sub-figure, which shows that the PLL track the phase correctly without producing any error during the step changes.

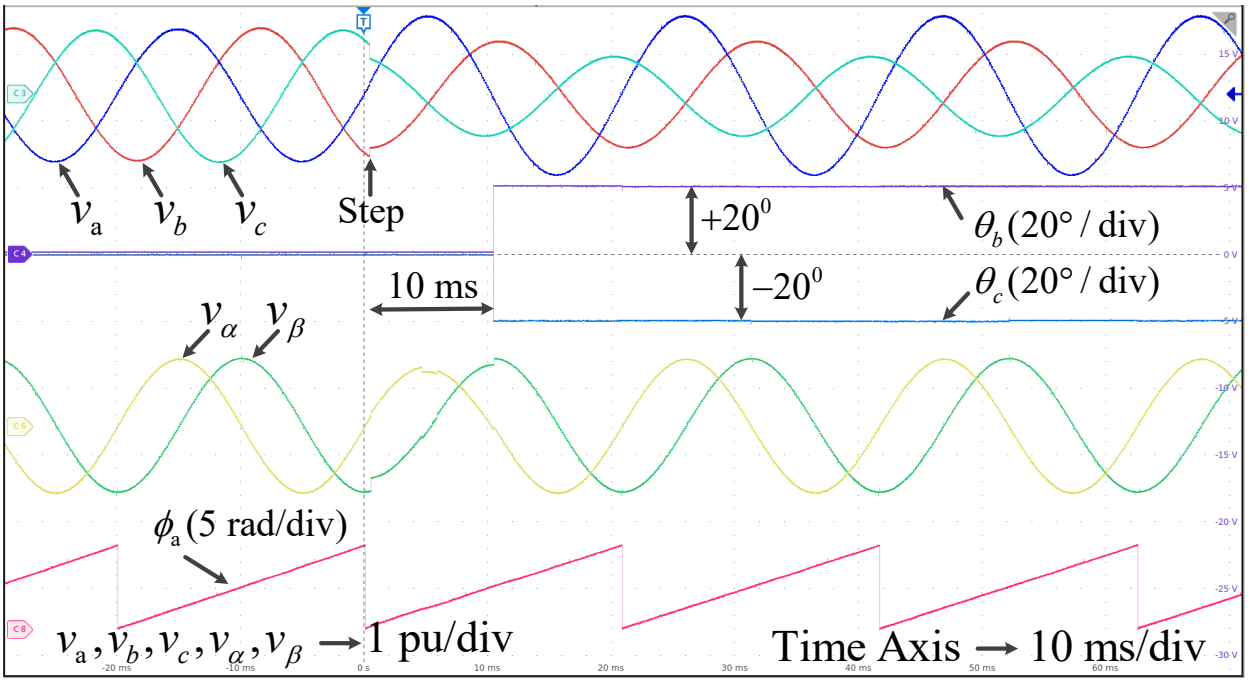

Fig. 4.23 Experimental performance of the proposed PLL method for a combination of unbalanced amplitude steps (+20%, -20% and -40%), unbalanced phase steps (θ_b=+20° and θ_c=-20°) and -2 Hz frequency step.

4.6 Experimental Performance with Harmonics

4.6.1 Case 1: Amplitude Step

When amplitudes of input voltages undergo sudden changes, the performance of proposed PLL is discussed in this case. For the experimental purpose, the three-phase amplitude steps (v_a = -0.1 p.u, v_b = -0.3 p.u, v_c = -0.5 p.u.) are created in input voltages and corresponding results are shown in Fig. 4.24. As it is observed from the Fig. 4.24, the proposed PLL can generate orthogonal signals and track the phase-angle after 60 ms of transient time. The phase differences between three-phases are 120° and thus the estimated phase angle deviations are 0°, which also takes 60 ms to become 0° after the step changes.

4.6.2 Case 2: Phase Step

The experimental performances of proposed PLL for unequal phase-angle deviations are presented in Fig. 4.25. To create phase unbalances, +30° and +20° unequal phase-angle deviations are inserted in phase ‘b’ and ‘c’ voltages, respectively. The results, as seen in Fig. 4.25, reveals that the proposed PLL can generate orthogonal signals and track the phase-angle

with a small disturbance within 3 fundamental cycles after the step change. Additionally, using similar transient time, the proposed PLL can estimate the phase-angle deviations.

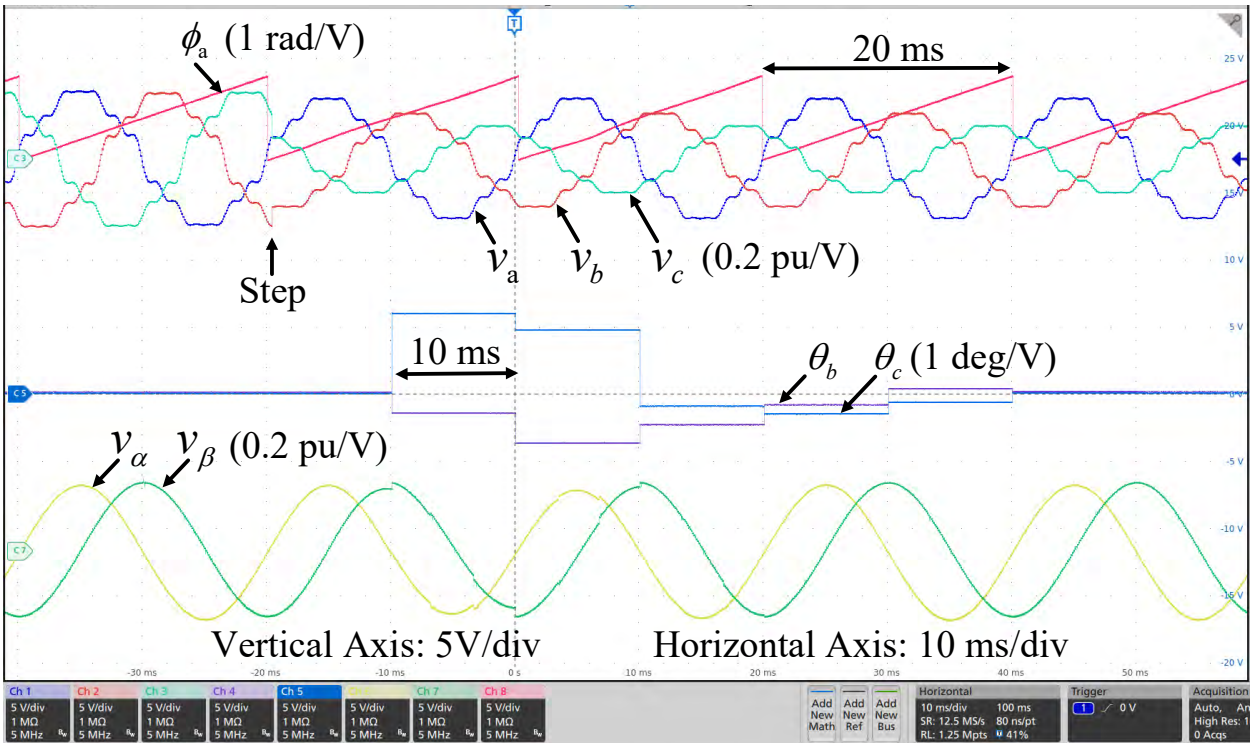

Fig. 4.24 Experimental results when three-phase amplitudes have a sudden step change from 1p.u. to (v_a=-0.1 p.u, v_b=-0.3 p.u, v_c=-0.5 p.u.).

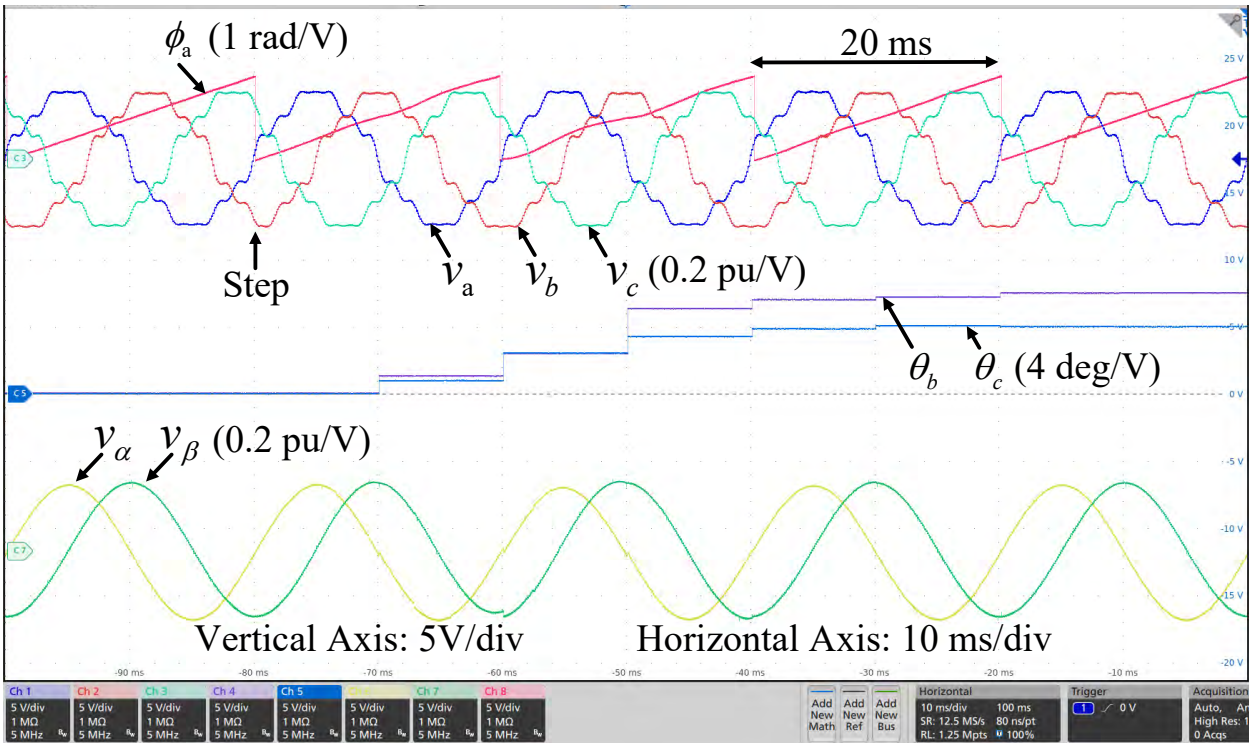

Fig. 4.25 Experimental results when phase (θ_b=+30° and θ_c=+20°) steps are occurred from balanced condition.

4.6.3 Case 3: Frequency Step

Fig. 4.26 demonstrates the experimental results when +5 Hz frequency step is introduced in input voltages. The proposed PLL can track the instantaneous phase of phase 'a', where the phase becomes synchronized with input voltages within 3 fundamental cycle after the step change, as seen in Fig. 4.26. It is also seen that, the proposed PLL can produce orthogonal signals and estimate phase deviations with same transient time.

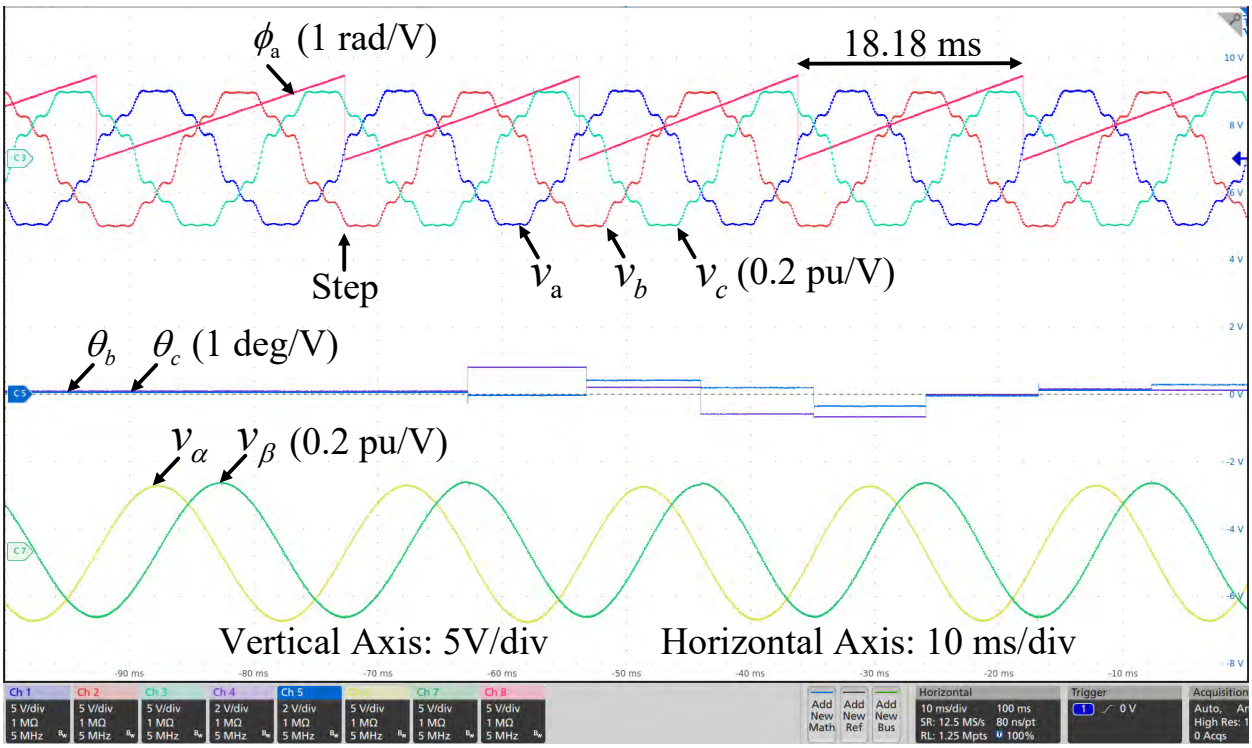

Fig. 4.26 Experimental results when frequency step (+5 Hz) is occurred from 50 Hz.

4.6.4 Case 4: Amplitude and Phase Steps

The effectiveness of the suggested PLL is demonstrated in this case, when input voltages experience abrupt change in both amplitudes and phases. The amplitude are changed by a step of (v_a = -0.1 p.u, v_b = -0.3 p.u, v_c = -0.5 p.u.), and phases by (θ_b = +30°, θ_c = +20°), and output performances are shown in Fig. 4.27. From Fig. 4.27, it is perceived that the proposed PLL is capable of tracking phase-angle using 60 ms transient time. Similar time is required for estimating the phase deviations and producing orthogonal signals.

4.6.5 Case 5: Amplitude and Frequency Steps

In this case, amplitude steps (v_a = -0.1 p.u, v_b = -0.3 p.u, v_c = -0.5 p.u.) and frequency step (+5 Hz) are created simultaneously in input voltages, and the corresponding experimental waveforms are shown in Fig. 4.28. With 60 ms dynamic adjustment time, the proposed PLL can estimate phase deviations and generates the orthogonal signals. The PLL can also track the phase-angle with same dynamics.

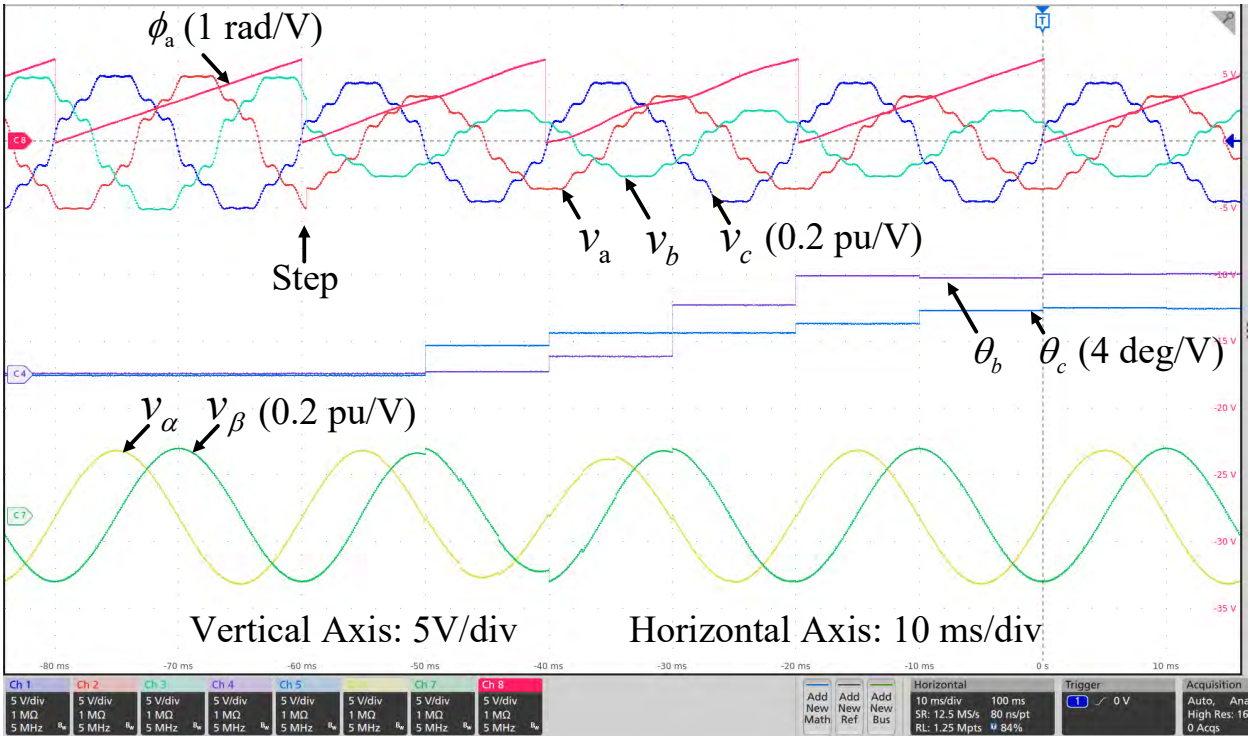

Fig. 4.27 Experimental results when a combination of amplitudes (v_a=-0.1 p.u, v_b=-0.3 p.u, v_c=-0.5 p.u.) step, and phase (θ_b=+30° and θ_c=+20°) step are occurred from 1p.u. and 0°, respectively.

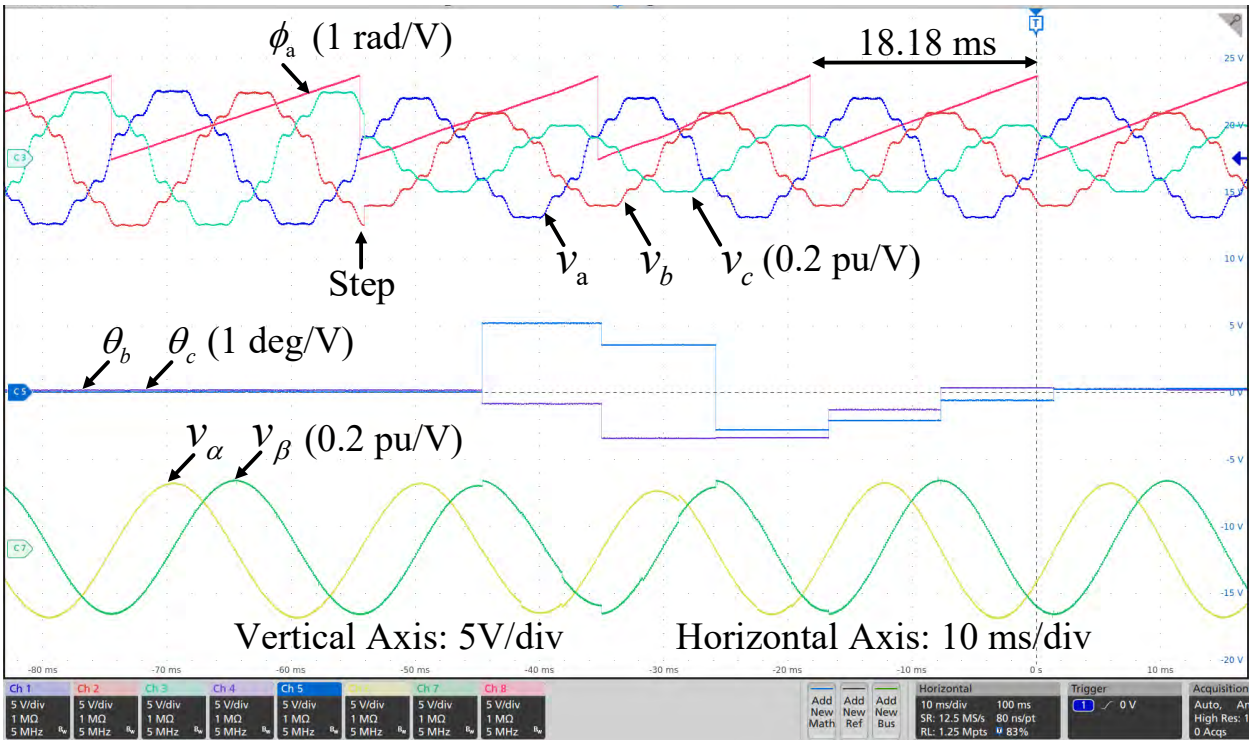

Fig. 4.28 Experimental results when a combination of amplitudes (v_a=-0.1 p.u, v_b=-0.3 p.u, v_c=-0.5 p.u.) step, and frequency (+5 Hz) step are occurred from 1p.u. and 50 Hz, respectively.

4.6.6 Case 6: Phase and Frequency Steps

Both phase and frequency steps are formed concurrently in this case as follows: +30°, +20° phase steps, respectively in phase 'b' and 'c', and +5 Hz frequency step. The experimental outcomes are depicted in Fig. 4.29, which describe that the proposed PLL requires 3 fundamental cycles to track the phase-angle accurately. It can also estimate the phase deviations and generate orthogonal signals with the same speed.

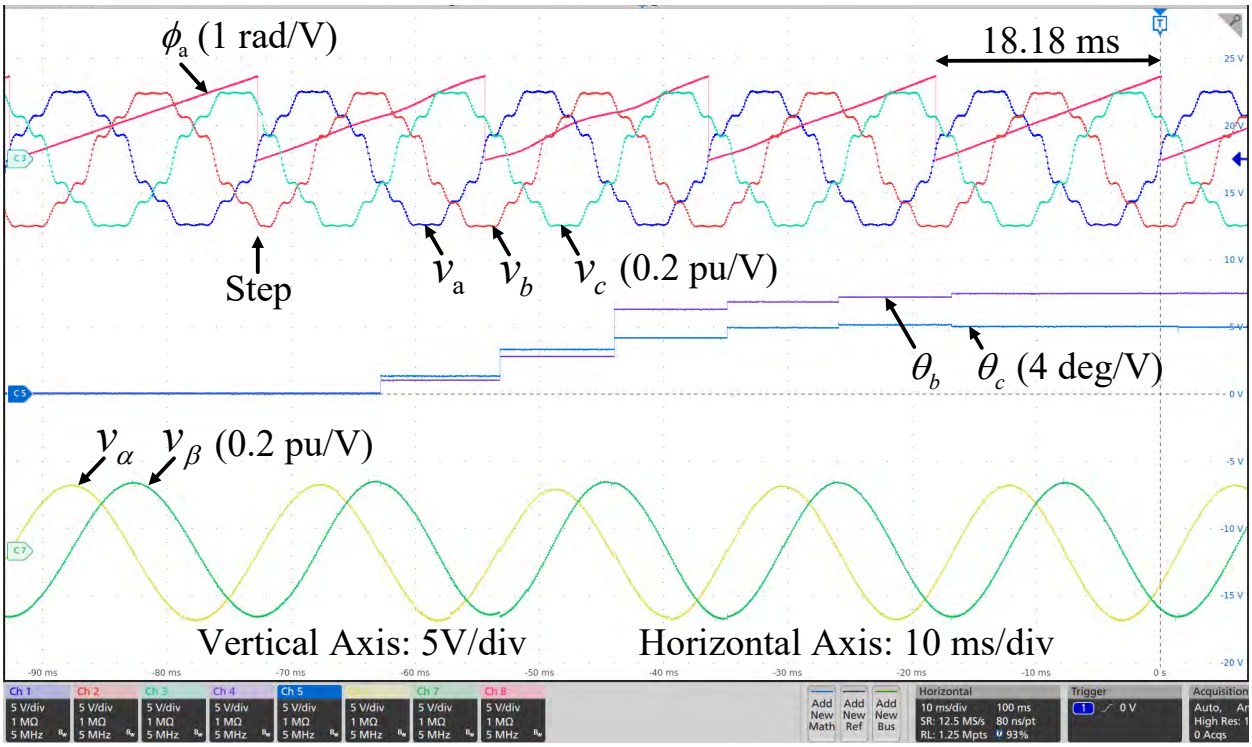

Fig. 4.29 Experimental results when a combination of phase (θ_b=+30° and θ_c=+20°) step, and frequency (+5 Hz) step are occurred from 0° and 50 Hz, respectively.

4.6.7 Case 7: Amplitude, Phase and Frequency Steps

A combination of amplitude (v_a = -0.1 p.u, v_b = -0.3 p.u, v_c = -0.5 p.u.), phase (θ_b = +30°, θ_c = +20°), and frequency steps (+5 Hz) are inserted in input voltages and corresponding dynamic performance is shown in Fig. 4.30. As it is noticed in Fig. 4.30, the PLL shows similar performance as the previous experiments to generate the orthogonal signals and to estimate the phase deviations and the phases.

4.6.8 Case 8: DC Offset

This case presents the performance of the proposed technique for presence of 10% DC offset in all three-phases. As it is seen in Fig. 4.31, the proposed PLL needs 60 ms transient time while estimating the phases, phase deviations, and generating orthogonal signals.

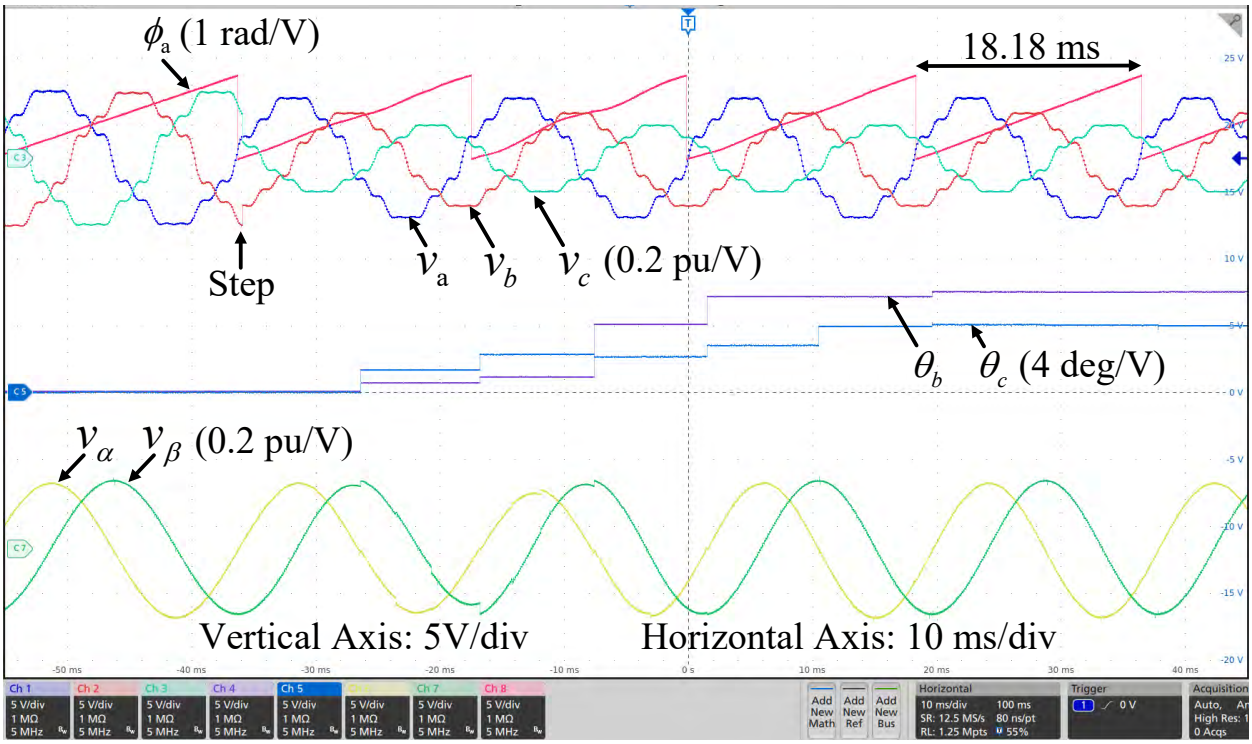

Fig. 4.30 Experimental results when a combination of amplitudes (v_a=-0.1 p.u, v_b=-0.3 p.u, v_c=-0.5 p.u.) step, phase (θ_b=+30° and θ_c=+20°) step, and frequency (+5 Hz) step are occurred from 1p.u., 0°, and 50 Hz, respectively.

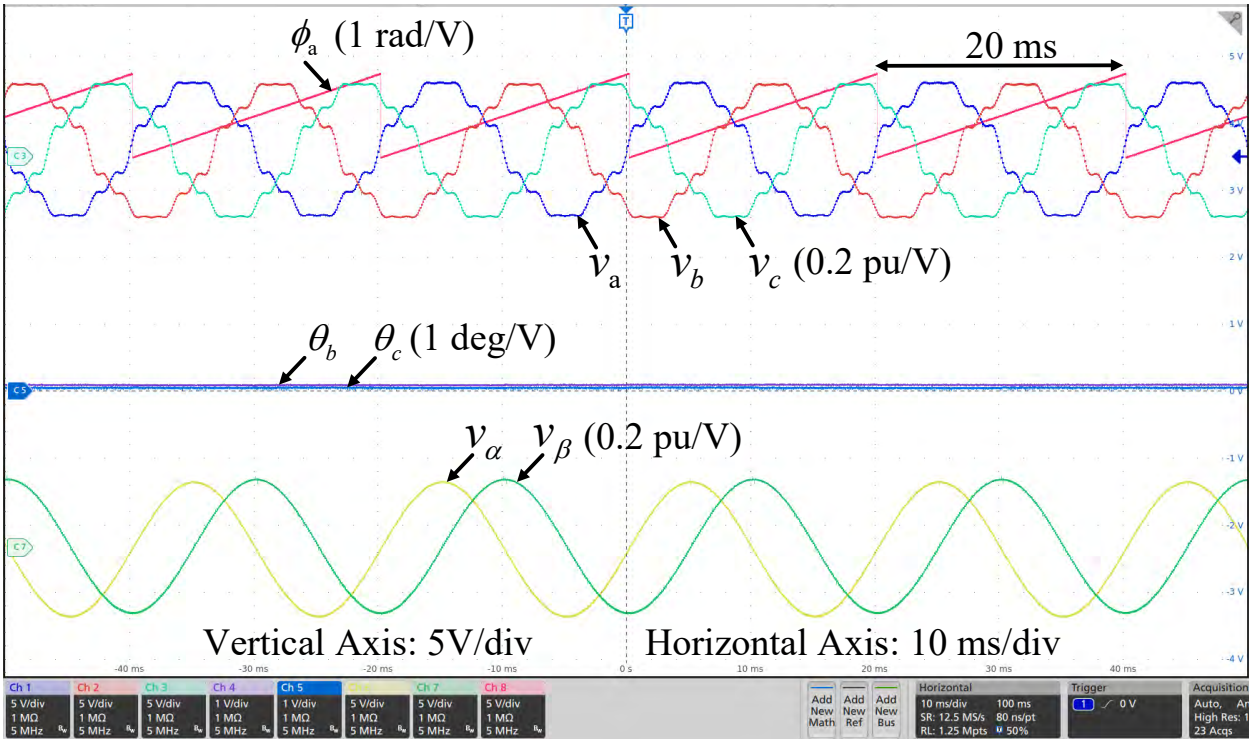

Fig. 4.31 Experimental results in presence of 10% DC offset in all phases.

Chapter 5 : Conclusions

5.1 Conclusions

In this dissertation, at first, the importance of instantaneous phase estimation is described and the state of art methods for phase estimation are reviewed. The performance of the most popular SRF-PLL model is evaluated due to the changes in parameters of three phase input voltages. It is also shown that the conventional SRF-PLL fails to correctly estimate the instantaneous phases of all three phases in presence of harmonics, DC offsets and voltage imbalances. To overcome the limitations, a novel PLL technique based on ACT algorithm has been developed in this dissertation.

The proposed PLL can estimate the phase-angle of all three-phases when input voltages associate harmonics, DC offset, and unbalances. A fine-tuned BPF is designed which can reject the harmonics and DC offset from grid-voltages. Then, with the help of the proposed ACT, both amplitudes and/or phase unbalanced voltages can be transformed directly into orthogonal voltages. Unlike the conventional CT based on constant-coefficient matrix, the ACT updates the CT coefficients adaptively to generate the orthogonal voltages from the three-phase unbalanced voltages. An auxiliary algorithm associated to the CT is also suggested which estimates the three-phase amplitudes and phase deviations. After generating orthogonal voltages, a conventional SRF-PLL is used to track the phase-angles of all three-phases. Additionally, in case of frequency deviations from nominal frequency, a phase correction technique is reported for correcting the error in estimated phase induced by BPF. The benefits of the proposed method have been ensured by comparing it with the most common PLL algorithms. In contrast to the CDSC and *dq*CDSC methods shown in the simulation and experimental results, the proposed PLL can track the instantaneous phases of all the three-phases without any error for any disturbances in the grid voltages. The proposed PLL uses only one PLL to track the phases of all the three-phase balanced or unbalanced voltages. The proposed technique can also estimate the amplitudes and phase-angle deviations of the three-phase voltages. Furthermore, the technique is frequency adaptive without using any frequency feedback loop, which enhance the stability and dynamics of the proposed PLL.

5.2 Future Works

The proposed PLL has some limitations, which will be solved in the future works. One limitation of the model is that when the phase angle deviations exceed ±30° limits, then the model produces error in proper phase angle deviations estimation. The reason of this limitation is that if the phase angle deviations are outside of the above mentioned limit, the phases would change its quadrant and would need further logic to correct the phase angle deviations. Another limitation is that when the frequency steps in grid voltages become larger, the ripple in steady state phase estimation becomes larger. This limitation can be corrected by using a modified/different BPF, which would be studied in future. Again, in case of adding harmonics in fundamental voltages, 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics are only considered. In the future works, the effects of other lower and higher order harmonic components will be studied.

The additional future work could be implementing the proposed PLL model in a DSP or an FPGA board for verifying the practical performance of the model. The PLL model can also be used in any PV or wind power project where instantaneous phase angle information is necessary for synchronizing the PV or wind system to the grid. Small signal analysis of the model would also be studied to verify the stability of the model in the future work.

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