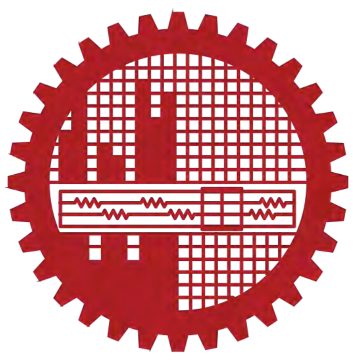
Analytical Modeling of Electrostatic and Transport Phenomena in Inversion-Type InGaAs Nanowire MOSFET



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MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by
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February, 2021

Approval

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It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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To my beloved parents

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Abstract

The prime motivation driving the semiconductor industry to fabricate devices of extremely reduced dimension is the innovation of novel technologies that enable manufacturers to create transistors in the sub 22-nm node, where short-channel effects (SCE) become a barrier for silicon technology in planar field effect transistors. Researchers are now moving to multi-gate structure that offer enhanced gate control over short channel effects to the highest degree. Particularly, gate-all-around (GAA) nanowire transistor have shown tremendous success in terms of improved electrostatic control but at the expense of mobility degradation at the surface due to oxide charges present at the oxide-semiconductor interface. Integration of III-V materials in the channel instead of silicon provides a viable solution for this dilemma, the bottleneck being the availability of a suitable native oxide unlike SiO_2 on silicon. Previous reports on InGaAs nanowire MOSFETs include electrostatic characterization and transport modeling in uncoupled mode space (UMS) approach both of which rely on quantum mechanical simulation that is computationally expensive. This work presents an analytical investigation of the electrostatic and drain current model for symmetric short channel InGaAs gate-all-around MOSFET valid from depletion to strong inversion using a continuous expression. The development of the core model is facilitated by the solution of quasi 2-D Poisson equation in the doped channel, accounting for interface trap defects and fixed oxide charges. Correction to short channel effects such as threshold voltage roll-off, drain induced barrier lowering and subthreshold slope degradation are later introduced, complemented with channel length modulation, velocity saturation and mobility degradation from surface roughness, leading to an accurate mobile charge density for electrostatic capacitance-voltage and transport characterization. A threshold voltage model is presented for long channel gate-all-around device that utilizes the well-known double derivative method, which is crucial for determining threshold voltage roll-off with scaling of transistors.The effect of physical process parameters like fin width, oxide thickness and channel length scaling are thoroughly investigated in both on and off state of the transistor. The robustness of the model is reflected from the precise match with published experimental reports in the literature. An R_{on} of 1160 $\Omega.\mu m$ is obtained from output characteristics and switching efficiency (ratio of

maximum transconductance to subthreshold slope) improvement of 2.5 times is estimated from incorporating high-κ dielectric into the GAA transistor. Numerical 3-D simulations from TCAD corroborates the validity of the proposed model in all regions of operation.

Contents

Approval ii

Declaration iii

Acknowledgement v

Abstract vii

Contents viii

Figures x

Tables xvi

1 Introduction 1

1.1 Motivation 1

1.2 A Historical Perspective: Literature Review 7

1.3 Contribution of the Thesis 18

1.4 Objective of the Thesis 20

1.5 Organization of the Thesis 22

2 Electrostatic Model Development 24

2.1 Basic Device Structure 25

2.2 Charge Modeling 27

2.2.1 Energy Band Diagram 28

2.2.2 Surface Potential and Mobile Charge 30

2.2.3 Capacitance-Voltage Characteristics 37

2.3 Threshold Voltage Development 38

3 **Transport Model Development** 40
3.1 Short Channel Effect Correction . . . 41
3.2 Velocity Saturation . . . 44
3.3 Mobility Degradation . . . 46
3.4 Channel Length Modulation . . . 47
3.5 Parasitic Resistance . . . 47

4 **Simulation Model Development** 49
4.1 Sentaurus Device . . . 49
4.2 Structure Creation . . . 50
4.2.1 Mesh Generation . . . 55
4.2.2 Simulation Flow . . . 56
4.3 Script for SDevice . . . 57
4.3.1 The File Section . . . 58
4.3.2 The Electrode Section . . . 59
4.3.3 The Physics Section . . . 59
4.3.4 The Plot Section . . . 62
4.3.5 The Math Section . . . 62
4.3.6 The Solve Section . . . 64

5 **Results and Discussions** 65

6 **Conclusion** 85
6.1 Summary . . . 85
6.2 Suggestions for Future Work . . . 86

Appendices 87

A **Difference of potential** 88
A.1 Difference of potential in deep subthreshold . . . 88
A.2 Difference of surface-center potential in terms of Lambert function . . . 89
A.3 Characteristic natural length of a symmetric GAA MOSFET . . . 90

Bibliography 92

List of Figures

1.1 **The evolution of transistor gate length (minimum feature size) and the density of transistors in microprocessor over time.** Between 1970 and 2011, the gate length of the MOSFETs shrank from 10μm to 28nm (yellow circles; y axis, right), and the number of transistors per square millimeter increased from 200 to over 1 million (diamonds, triangles and squares show data for the four main microprocessor manufacturers; y axis, left). AMD, Advanced Micro Devices; IBM, International Business Machines. [3] 2

1.2 **Types of multigate MOSFET.** The different ways in which the gate electrode can be wrapped around the channel region of a transistor are shown. (a) A silicon-on-insulator (SOI) fin field-effect transistor (FinFET). Gate control is exerted on the channel from the lateral sides of the device. (b) SOI triple-gate (or tri-gate) MOSFET. Gate control is exerted on the channel from three sides of the device (the top, as well as the left and right sides). (c) SOI π-gate MOSFET. (d) SOI Ω-gate MOSFET. Gate control of the bottom of the channel region is better than in the SOI π-gate MOSFET. (e) SOI gate-all-around MOSFET. Gate control is exerted on the channel from all four sides of the device. (f) A bulk tri-gate MOSFET. In this case, there is no buried oxide underneath the device. [3] 4

1.3 **First experimental demonstration of a transistor based on germanium crystal substrate placed on a metal plate with two gold contacts.** (Photo by Jacopo Werther) [35] 8

1.4 **A multi fingered (three-finger) nanowire transistor.** (a) Scanning electron microscopy image of a device with three parallel nanowires that have a common gate electrode. Scale bar, 5μm. (b) Transmission electron microscopy image of the three nanowires. Scale bar, 50 nm. (c) High resolution transmission electron microscopy image of a nanowire. Scale bar, 5 nm. [3] . 10

1.5 **Various configuration of nanosheet stacking.** (a) Nanosheet double stack, W_{eff}=1.04x (b) Nanosheet double stack, W_{eff}=1.3x (c) [47] 10

2.1 **Schematic view of a GAA MOSFET.** The source/drain is heavily doped for ohmic contacts and the $In_{0.53}Ga_{0.47}As$ channel is p-doped. (a) Perspective view. (b) Lateral view. 27

2.2 **Schematic view of an inversion mode GAA n-channel $In_{0.53}Ga_{0.47}As$ ($2 \times 10^{16}/cm^{-3}$) MOSFET with ALD 10nm Al_2O_3/20nm WN gate stack.** A heavily doped wide bandgap InP lies underneather the bottom gate. [60] 28

2.3 **Energy band diagram of a GAA MOSFET having p-doped channel in Flat band condition.** The channel width is W, oxide thickness t_{ox}. E_F, E_{Fi} and E_{Fm} are the Fermi level of the p-doped channel, intrinsic Fermi level and work function of the gate metal. 29

2.4 **Drain current as the function of V_g in an inversion-mode device.** [109] 31

2.5 **Energy band diagram of a GAA MOSFET having p-doped channel near threshold condition.** The channel width is W, oxide thickness t_{ox}. E_F, E_{Fi} and E_{Fm} are the Fermi level of the p-doped channel, intrinsic Fermi level and work function of the gate metal. 31

2.6 **Energy band diagram of a GAA MOSFET.** (a) In thermal equilibrium. (b) At strong inversion. The mismatch in the gate Fermi level and that of the semiconductor results due to application of a large gate bias. 32

2.7 **Variation of electrostatic potential along width and height direction at different gate voltages covering from subthreshold to strong inversion.** The symmetry of the gradient of the electrostatic potential from center to surface verifies the assumption $\frac{d\phi}{dx} = \frac{d\phi}{dy}$ made to simplify Equation (2.2) 34

2.8 **Surface potential (ϕ_s), center potential (ϕ_0) and their normalized difference (α) in subthreshold and strong inversion region with moderate levels of channel doping.** The vertical line roughly differentiates between the two regions of operation. The normalized difference of potential is low and remains constant below threshold condition. 35

2.9 **Fringe capacitance schematic for the cross-section of a gate-all-around MOSFET.** The origin is taken as the central nanowire axis. Perpendicular-plate capacitance arising from the corners are denoted by C_{fr} and the oxide thickness is t_{ox}. 36

3.1 **Competition between the different electric fields for an elemental volume in the channel region.** The elemental volume is represented by the small grey cube. The vertical component of the electric field (E_y) arises from the top and bottom gates; the lateral component (E_x), from the side gates; and the longitudinal component (E_z) from the source and drain regions. L, channel length; W, fin width. [3] 41

3.2 **Early saturation of drain voltage in short channel operation.** The hashed line shows the saturation voltage of a long channel MOSFET given by $V_{GS} - V_T$. The symbols denote that of a short channel MOSFET. The use of equation (3.19) gradually limits the drain saturation voltage, denoting that mobile carriers reach saturation velocity before the expected drain voltage. Experimental data has been extracted from [60]. 45

4.1 **Cross-section of the InGaAs GAA MOSFET.** The gate oxide wraps around the active InGaAs channel in concentric formation. The fin width is 30 nm and the gate oxide 10 nm on all sides. 52

4.2 **Completed structure of the GAA MOSFET created in Sentaurus Device Editor.** (a) Schematic showing source/drain region with the wrap-around gate. (b) Schematic without the wrap-around gate, revealing the doping profile and mesh throughout the entire channel. It can be seen that dense mesh are formed near the oxide-semiconductor interface and near source/drain region to realize important physical effects in the active channel. 54

4.3 **Illustration of a 2D triangular mesh over a control area W (red) using the box method.** Figure redrawn from [122]. 57

4.4 **Typical simulation flow diagram of Sentaurus Device, starting from the structure editing, device simulation and visualization of the simulation output.** [124] 58

4.5 **Spatial carrier density of electrons taken at cross-section of the GAA MOSFET at mid-channel.** (a) At low gate bias near threshold region. (b) At high gate bias in strong inversion regime. (c-d) The corresponding electron density along cutlines A-A' from gate-to-gate direction and along B-B' direction diagonally. The corner effect at strong gate bias in the GAA geometry is evident from (b) and (d), showing that TCAD simulation is successful in accounting for this effect. 63

5.1 **Mobile charge density as a function of gate bias for a GAA MOSFET at $N_{\mathrm{A}} = 2 \times 10^{16}\, cm^{-3}$.** (a) Comparison between model and simulated charge density in both linear and log scale at low $\mathrm{V_{DS}}$. (b) Error in charge density from using (2.18) instead of Lambert function. Largest error occurs near threshold region. 66

5.2 **Capacitance-voltage characteristics of a GAA nanowire MOSFET with $N_{\mathrm{A}} = 2 \times 10^{16}\,\mathrm{cm}^{-3}$.** (a) For various oxide thickness. (b) For various fin width. The fin width has greater impact on $C - V$ characteristics in comparison to oxide thickness which is reflected by a shift in threshold voltage. The impact of quantum effect on CV profile is seen for a fin width of 10nm where simulation results reflect a rightward shift in CV arising from threshold voltage shift in subthreshold region and gate capacitance degradation in strong inversion region. 67

5.3 **Effect of channel material properties on CV curve of $\mathbf{In_{1-x}Ga_xAs}$ GAA MOSFET.** (a) For various channel doping (x=0.47). (b) For various x-composition ($\mathrm{N_A} = 2 \times 10^{16}\ \mathrm{cm}^{-3}$). A significant shift in CV profile takes place for heavily doped channel. 69

5.4 **Threshold voltage dependence on channel doping for different oxide thickness.** The classical threshold voltage model based on critical band bending in strong inversion deviates from the predicted result for lightly doped transistor. 70

5.5 **Non-monotonic dependence of threshold voltage on:** (a) t_{ox} for various channel doping. (b) fin width for various channel doping. 71

5.6 **The trend of MOSFET scaling from ITRS.** Picture taken from ITRS Corp. [136] 72

5.7 **Transfer characteristics of a 50nm GAA MOSFET.** (a) Drain current as a function of gate voltage. (b) Extrinsic transconductance. (c) DIBL and subthreshold slope extracted from the I_D-V_G plot. Experimental data has been extracted from [60]. 74

5.8 (a) Output characteristics of a 50nm GAA MOSFET. An R_{on} of 1160 $\Omega \cdot \mu$m is obtained from the slope at V_{GS} = 2V (b) Output conductance of the same device, showing that drain current remains continuous from linear to saturation region. Experimental data has been extracted from [60]. 75

5.9 **On-state and off-state characteristics of an InGaAs GAA transistor.** Variation of (a) DIBL (b) SS with W/L ratio. Best fit straight lines are also plotted based on least square regression to highlight proportional relation with W/L. (c) Maximum ON-current as a function of gate length obtained at $V_{GS} = 2$V and different drain bias. For comparison, the dotted line shows when the drain current starts to saturate due to non-ideal effects in the short channel MOSFET. 76

5.10 **Transfer characteristics of a GAA MOSFET for various fin width having** $N_A = 2 \times 10^{16}$cm^{-3}**.** (a) Normalized drain current as a function of gate voltage. Inset figure shows that total current of the wider nanowire is more as expected. (b) Transconductance as a function of gate voltage. . . . 77

5.11 **Transfer characteristics of a GAA MOSFET for various oxide thickness having** $N_A = 2 \times 10^{16}$cm^{-3}**.** (a) Drain current as a function of gate bias. The cross-over of the curves indicate an invariant point where the effect of oxide thickness variation due to process limitation is minimized. (b) Transconductance as a function of gate bias. 78

5.12 (a) Threshold voltage roll-off (b) Drain induced barrier lowering and (c) Subthreshold slope degradation due to gate length scaling at various fin width. (d) Threshold voltage roll-off (e) Drain induced barrier lowering and (f) Subthreshold slope degradation due to gate length scaling at various oxide thickness. The subthreshold properties are affected to greater extent due to fin width variation. 79

5.13 **Benchmarking g_m·EOT of contemporary planar and non-planar InGaAs surface-channel MOSFETs.** [60] 80

5.14 **Capacitance-voltage profile for different gate dielectric.** 81

5.15 **Impact of high-κ dielectric on threshold voltage of heavily doped GAA transistor.** 82

5.16 I_{on}/I_{off} **ratio as a function of oxide thickness for various gate dielectric.** $I_{on(off)}$ is defined as the drain current at maximum (minimum) V_{GS} and high drain bias. The high drain junction leakage current of InGaAs GAA MOSFETs result in a small on-off ratio. 83

5.17 **Radar plot presenting a quantitative analysis between Al_2O_3 and HfO_2 as gate dielectric in 50nm InGaAs GAA MOSFET having fin width 30nm and t_{ox} 10nm at V_{DS} = 50mV.** A switching figure of merit of 0.82 (μS/μm)/(mV/dec) is obtained from using HfO_2, resulting in an improvement of 2.5 times over using Al_2O_3. 84

List of Tables

3.1 Relevant parameters used in the transport model. 48

4.1 Box method coefficients for 1,2 and 3-D discretization. 56

4.2 Numerical approximation of the coupled differential equations, solved in each vertex of the mesh. 56

5.1 Process/device parameters used in this work. 70

Chapter 1

Introduction

This chapter expands on the motivation to search for alternative channel material in non-planar multi-gate device structure, mainly to overcome the limitations posed by single gate and double-gate transistor and how the industry has shifted to the adoption of gate-all-around (GAA) geometry from FinFET architecture in a seamless fashion, with an aim to perpetuate Moore's Law that has so long driven the semiconductor industry towards scaling of nanoscale Metal Oxide Semiconductor Field Effect Transistor (MOSFET). In addition, a brief overview of the experimental demonstrations realized for GAA transistors along with a rigorous study of the extant analytical models will be presented. Finally the object and outline of the thesis will be covered.

1.1 Motivation

Scaling of MOSFET has continued over the past several decades without any major change in the basic planar structure. One of the many reasons for the predilection of the semiconductor industry towards a miniaturized MOSFET is the possibility of packing more transistors into a given area with smaller feature size. The apparent benefit is an improvement in the functionality of the chip with enormous cost-saving in manufacturing. In 1965, Gordon Moore made a famous prediction that the density of transistors on a chip would double every 18 months [1]. Despite the empirical nature of this prediction and the basis being only on six years' data, the law has upheld remarkably well in the past 50 years (Figure 1.1). In addendum, smaller transistor means faster switching speed resulting from the proportional down scaling of all the device

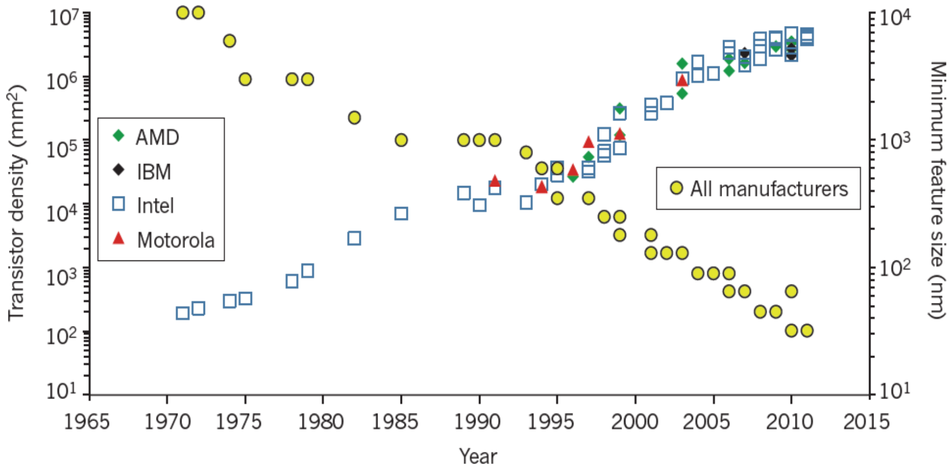


Figure 1.1: **The evolution of transistor gate length (minimum feature size) and the density of transistors in microprocessor over time.** Between 1970 and 2011, the gate length of the MOSFETs shrank from 10μm to 28nm (yellow circles; y axis, right), and the number of transistors per square millimeter increased from 200 to over 1 million (diamonds, triangles and squares show data for the four main microprocessor manufacturers; y axis, left). AMD, Advanced Micro Devices; IBM, International Business Machines. [3]

dimensions. Doubling the density of transistors on a chip is equivalent to reducing the chip's linear dimensions, such as length and width, by a scaling factor of $\sqrt{2}$. Let this scaling factor be represented by 'l'. In 1974 Dennard *et al.* demonstrated the benefits of scaling in his seminal paper [2], where he showed that for a constant electric field inside the transistor, scaling the device by a factor of l increases the switching speed by l, reduces the power dissipation by l^2 and improves the power-delay product by l^3. The gate capacitance is reduced, leading to minimum RC delay, thereby contributing to the enhance device switching speed. It is noteworthy to mention that Dennard's scaling law implies a reduction in the supply voltage and threshold voltage by 'l', although the latter has not been achieved due to the lack of feasibility in achieving a subthreshold slope value of less than 59.6 mV/decade in conventional MOSFETs.

The halcyon of the booming semiconductor industry was thwarted by the many challenges of simple down scaling in recent times. Dennard's scaling law was followed by the semiconductor industry until approximately 2005 when performance improvement due to scaling reached a saturation. Firstly, as MOSFET dimensions are shrunk, the designed gate voltage should also be smaller to maintain device reliability. In order to maintain performance, the threshold voltage must also decrease. This creates a bottleneck with the limitation of the device to turn off completely, making subthreshold

conduction non-negligible in scaled devices. The down scaled MOSFET has thinner gate oxide layer which increases gate leakage, the sole factor with major contribution to static power dissipation and degraded reliability of logic and memory devices. Moreover, as gate length scaling reaches sub-nanometer domain, the source/drain junction depletion width becomes comparable to the short channel length, giving rise to new challenges known as short channel effect (SCE). The induced SCE results into device threshold voltage roll-off and increased junction leakage [4,5]. As can be seen in Figure 1.1, the gate length of microprocessors in the current timeline is close to 25 nm. In practice, accounting for the reduced distance between the source and drain in comparison to gate electrode yields an effective channel length of only 15 nm. It goes without saying that SCE will be more prominent in ultra-scaled devices.

To ameliorate some of these issues, researchers are exploring the prospect of high-κ dielectric to maintain the dielectric physical thickness while scaling down effective thickness, suppressing the static leakage current through the gate terminal due to quantum mechanical tunneling [6]. Hafnium oxide and lanthanum lutetium oxide have dielectric constants higher than that of silicon dioxide [7]. The use of these high-κ dielectric results in improved control of the channel by the gate voltage and thus reduces SCEs.

Channel doping engineering is another viable solution to counteract SCE in the prevailing technological impasse. However, there is little room for further down scaling on planar geometry even with these new device design techniques.

The effort to maintain device down scaling trend needs some novel solution based on alteration of the device structure. In a bulk planar MOSFET, the gate electrode is positioned on top of an insulator to cover the active channel region between the source and drain. In such a configuration, the gate achieves electrostatic control of the channel region by capacitive coupling through gate insulator. The electrostatics of a long channel MOSFET are essentially one dimensional. The physics of the elementary device is governed by solving one-dimensional Poisson equation vertically from the gate towards the substrate direction. Short channel effects, where electric fields from the source to

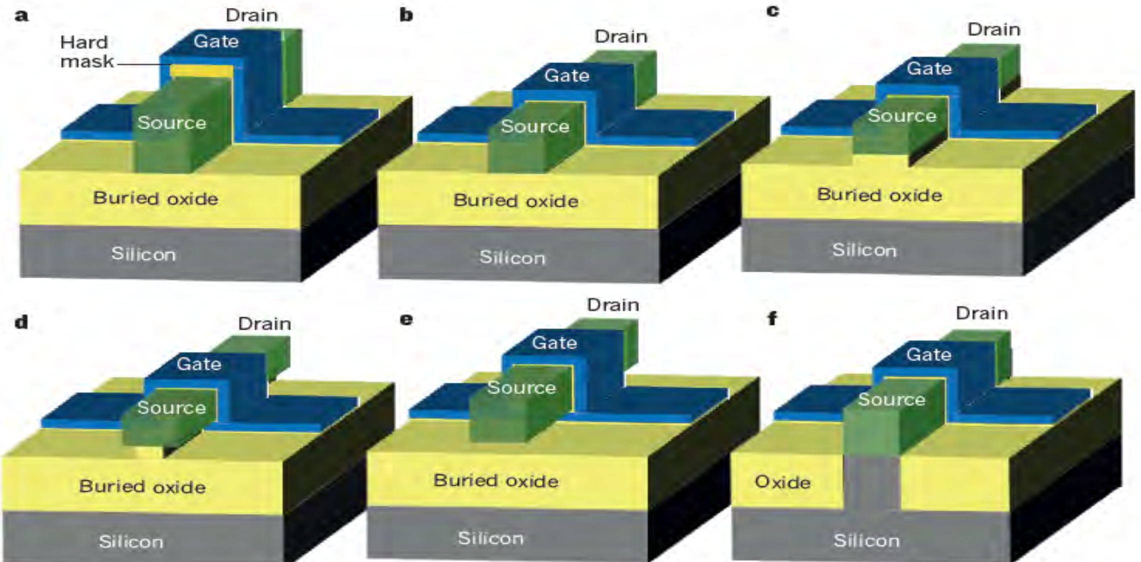


Figure 1.2: **Types of multigate MOSFET.** The different ways in which the gate electrode can be wrapped around the channel region of a transistor are shown. (a) A silicon-on-insulator (SOI) fin field-effect transistor (FinFET). Gate control is exerted on the channel from the lateral sides of the device. (b) SOI triple-gate (or tri-gate) MOSFET. Gate control is exerted on the channel from three sides of the device (the top, as well as the left and right sides). (c) SOI π-gate MOSFET. (d) SOI Ω-gate MOSFET. Gate control of the bottom of the channel region is better than in the SOI π-gate MOSFET. (e) SOI gate-all-around MOSFET. Gate control is exerted on the channel from all four sides of the device. (f) A bulk tri-gate MOSFET. In this case, there is no buried oxide underneath the device. [3]

the drain encroach laterally into the channel region adds a second dimension to this problem. Multi-gate transistors take the advantage of the third dimension to counteract the SCE. Figure 1.2 shows some of the advanced multigate architectures namely fin field-effect transistors (FinFETs), triple-gate (tri-gate) MOSFETs, gate-all-around (GAA) MOSFETs (in which the gate electrode wraps around the entire periphery of the channel region) and the π-gate and Ω-gate structures (which are so named because of the shape of their gate electrodes [8, 9]).

Multi-gate devices are lucrative for their ability to harness large on-state current in addition to better gate controllability. The improved gain and lower output resistance is desirable for circuit designers. With the ability to extend effective channel width into the third dimension, device miniaturization has been continued by shrinking the footprint on chip area. As the most promising multi-gate MOSFET, the FinFET has been in production by Intel since 2012 [10]. The GAA FET has a similar structure as the FinFET, but the gate material extends to surround the channel on all four sides.

The GAA MOSFET is the ultimate successor, designed to eliminate SCE to the greatest extent. The GAA FET is expected to dominate the next generation nano-device industry [11–16].

The GAA FET has been successfully implemented based on the extant silicon nanowire technology. However, one of the central pitfalls of silicon-based MOSFETs is the increase in parasitic capacitance and resistance relative to their intrinsic counterparts as device dimensions decrease. As Dennard's scaling law dictates, voltage reduction is crucial in order to curtail power dissipation, otherwise increased parasitics translate into stagnation of performance in terms of current drive. A potential solution to circumvent this dilemma is to substitute the silicon channel by a new material, one that offers carrier with higher injection velocity and mobility. In this regard III-V compound semiconductor holds immense promise [17]. InGaAs for electrons and InGaSb for holes offer a good balance among the many requirements imposed on a MOSFET channel material: low contact resistance, high mobility, adequate interfacial quality with high-κ dielectrics and bandgap energy. There has been an explosion in research on InGaAs-based MOSFET both in industry and academia, the ramification being massive progress in III-V semiconductor device design in planar geometry as well as 3D architectures such as FinFETs and nanowire FETs [18–20].

The high mobility of the channel carriers augmented with the low density effective mass has enabled planar InGaAs MOSFET to make great strides in recent times. For future high-speed low-power logic applications, inversion-type enhancement-mode III-V MOSFET holds the foreground amongst prevalent logic devices. Intense research effort expended in the past four decades behind the search for the "perfect" insulator suitable for III-V MOS system has solved a long standing problem that is Fermi level pinning at the oxide-semiconductor interface. This phenomenon is believed to be due to the formation of native oxides that create high concentration of defects at the semiconductor interface [21]. Fermi level pinning prevents modulation of the surface potential by the gate and the charge control that is essential for efficient operation of MOSFET. Until recently, a technological breakthrough has addressed this prevailing problem by finding the use of atomic layer deposition (ALD) to integrate thermody-

namically stable high-κ dielectric on III-V semiconductor to form gate oxide involving a "self-cleaning effect" that eliminates the native oxides and associated defects at the semiconductor surface [22, 23]. Subthreshold swings in MOSFETs with values approaching 60 mV/decade have been demonstrated [24–26], having excellent interface quality with trap densities in the range of 10^{11} $\mathrm{eV^{-1}cm^{-2}}$ [27, 28].

Another key element contributing to the dramatic rise of the InGaAs MOSFET performance has been the development of self-aligned fabrication methodology. Self-alignment of contacts and gate is vital for manufacturability and to minimize parasitics and footprint. In essence, four different self-aligned designs have emerged in the last few years.

- A contact-first, gate last process in which the gate is located in an opening created in the ohmic contacts [25, 29, 30].
- Raised, self-aligned source and drain epitaxial regions selectively grown around a dummy gate [31, 32].
- A thin Ni layer thermally reacted with InGaAs to give rise to a highly conducting and very shallow intermetallic compound with very low resistivity [33].
- A combination of self-aligned ion implanted source and drain extensions and in-situ doped raised source and drain regions around a gate [34].

In spite of these advancements in fabrication methodologies, planar MOSFETs are limited in their scaling potential. Since channel thickness has a strong correlation with device characteristics, a thick channel is beneficial to ON-state figures of merit, such as $\mathrm{g_m}$, whereas a thin channel influences OFF-state metrics like subthreshold swing (SS) and drain-induced barrier lowering (DIBL). To reap the benefits provided by the multi-gate architecture in suppression of SCEs compounded by the advantages of the III-V channel carriers, InGaAs nanowire MOSFET has become the quintessential solution for ultra-scaled devices.

As a deeply scaled device, the GAA nanowire MOSFET behaves differently from the classical large scale transistors in many aspects such as volume inversion and quantization effects impacting carrier transport. The small device feature makes the device

performance sensitive to fin width scaling and oxide thickness. A physics-based analytical modeling of InGaAs GAA MOSFET is imperative to study the behavior of the device, to serve as a guideline for optimization of process parameters and use in circuit simulation. Given the quality of interface trap states as the major detrimental factor, limiting performance of InGaAs nanowire MOSFET to subpar levels, the incorporation of these trap charges is essential to accurately determine the mobile charges responsible for carrier transport. A comprehensive understanding of the device physics is obtained from the core transport model. However, in keeping with the convention of the ITRS guidelines for device scaling, certain non-ideal effects need to be complemented into the core model to facilitate the accurate reflection of the device electrostatics and transport characteristics. As such, the impact of physical process parameters are vital for optimization of device design, for which their impact must also be studied under the scope of the analytical model outlined in this thesis.

1.2 A Historical Perspective: Literature Review

Humanity experienced a tremendous advancement in computational power in the second half of the last century. During the war, semiconductor diodes made of high-purity germanium were explored at Bell Labs with an aim for potential use in radar applications. Using this newfound gumption in semiconductors, William Shockley dedicated resources in the development of semiconductor amplifier. At the same period, John Bardeen and Walter Brattain began work on what would be the point-contact transistor at the AT&T Laboratories, which was demonstrated in December of 1947 (Figure 1.3). There were two closely spaced gold contacts on one side of a germanium crystal in this device positioned on a metal plate. On application of a small current to one of the gold contacts resulted into amplification of the current flowing from the other contact to the metal plate. This was the first experimental demonstration of a transistor that brought the Nobel Prize in Physics in 1956 for the three scientists.

In the 1950's, shortly after Shockley invented the bipolar junction transistor, tran-

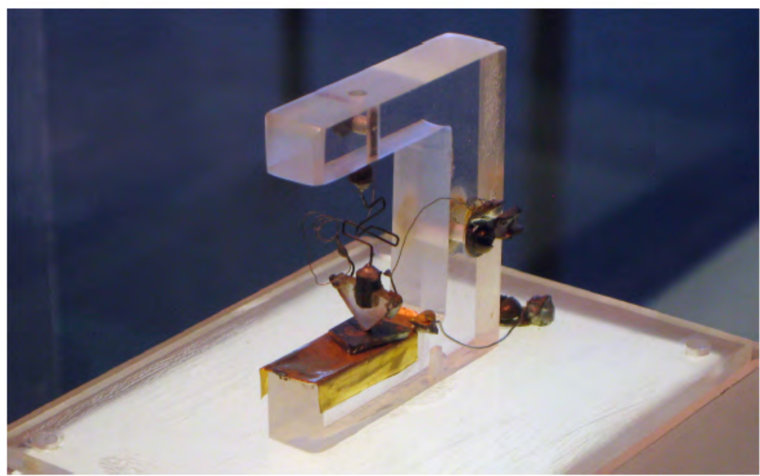


Figure 1.3: **First experimental demonstration of a transistor based on germanium crystal substrate placed on a metal plate with two gold contacts.** (Photo by Jacopo Werther) [35]

sistors were commercialized. Primary applications of the then novel device included transistor radios and hearing aids. In 1958, IBM introduced the first transistor-based commercial computer which was the IBM 7070. Soon after, the first integrated circuit was built by Jack Kilby at Texas Instruments which incorporated all the circuit components on the same semiconductor crystal, making it feasible to create compact circuit designs.

Robert Noyce of Fairchild Semiconductor invented a similar circuit in 1959. Robert started Intel with his colleague Gordon Moore, initially manufacturing bipolar random access memory (SRAM) in 1968 and later adopting the commercial MOSFET SRAM based on silicon. Gordon Moore recapitulated the pursuit of the integrated circuit industry in the title of his famous paper from 1965 [1], "Cramming more components onto integrated circuits", which led to the vaunted prediction known as Moore's Law. In a nutshell the law states that the number of transistors in an integrated circuit doubles every year (later revised to double biennially) [1]. The pursuit for compact integration was upheld thanks to a number of fortuitous events including but not limited to vast technological possibilities as well as tremendous economical incentives driving the increase in transistor count in a typical central processing unit (CPU) from tens of thousands in 1970's to billions in 2020, ushering the next industrial revolution at the frontier of cutting edge technology.

The first report on multigate transistor was published in 1984 describing a double-gate MOSFET [36]. The device received the acronym XMOS because of the resemblance of the structure with the Greek letter Ξ. In this paper it was shown that the short-channel characteristics could be improved through implementation of a double-gate architecture instead of the conventional single-gate approach. Soon after, the transistor model went into fabrication in 1989, containing a vertically positioned silicon film which, for the orientation of the film, came to be known as the fully DEpleted Lean-channel TrAnsistor (DELTA) [37]. As a vertical ultra-thin SOI device, DELTA offered a high storage area with high packing density in DRAM cell.

With some modification, the vertical channel double-gate transistor took the form of a FinFET (Fig. 1.2a) [38] with successful implementation in the sub 50-nm channel length. High drive currents of 410 μA/μm were obtained at V_d=V_g=1.2V owing to the use of doped poly-SiGe films for raised source/drain contacts. The quasi-planar nature of this variant allowed industries to adopt its fabrication using the conventional planar MOSFET process technologies.

The continued scaling of fully depleted SOI transistor brings additional challenge when scaling the dimensions of the active channel region. For a single-gate fully depleted channel, the silicon body thickness needs to be at least a third or one-half of the electrical gate length in order to ensure full depletion under the gate. Doyle *et al.* demonstrated that tri-gate MOSFET ensures fully depleted behaviour at thickness dimensions greater than those of double-gate transistors, making them excellent candidate for future scaled CMOS technologies [39]. Improved version of the tri-gate MOSFET feature a field-induced pseudo-fourth gate such as the π-gate MOSFET (Fig. 1.2c) [40] and the Ω-gate devices (Fig. 1.2d) [41, 42], created to improve gate electrostatic control over the channel charges and consequently reduce the SCEs. Jean-Pierre Colinge and Xiong *et al.* provided a comparative study of the impact of radii of curvature in the cross-section on the electrical characteristics among these class of devices [8, 43]. In essence, it was demonstrated that fully cylindrical devices imposed the greatest control over the channel carriers in the subthreshold regime Such devices include the CYNTHIA device (circular-section device) [44] and the pillar surrounding-gate MOSFET

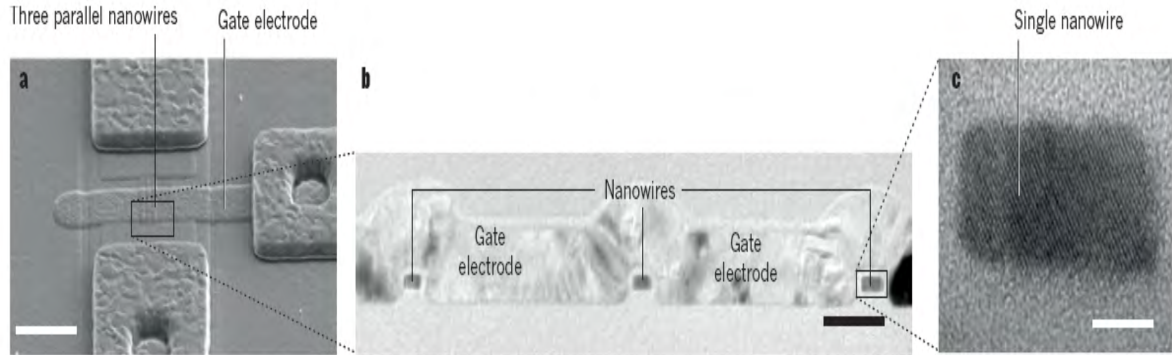


Figure 1.4: **A multi fingered (three-finger) nanowire transistor.** (a) Scanning electron microscopy image of a device with three parallel nanowires that have a common gate electrode. Scale bar, 5μm. (b) Transmission electron microscopy image of the three nanowires. Scale bar, 50 nm. (c) High resolution transmission electron microscopy image of a nanowire. Scale bar, 5 nm. [3]

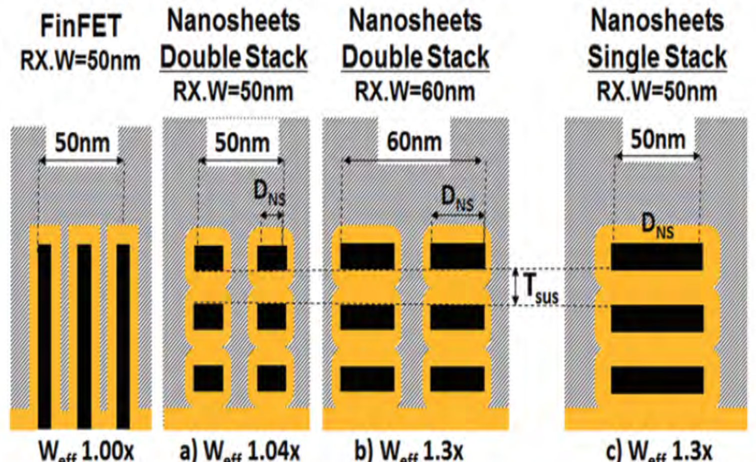


Figure 1.5: **Various configuration of nanosheet stacking.** (a) Nanosheet double stack, W_{eff}=1.04x (b) Nanosheet double stack, W_{eff}=1.3x (c) [47]

(square-section MOSFET) [45].

The first reported gate-all-around device dates back to 1990, where the gate electrode is wrapped around all the sides of the channel region [46]. Though the device was used as a double-gate transistor back then, GAA geometry gained popularity once the benefits obtained from FinFETs reached a saturation. Apart from the suppression of SCE to the greatest extent, the GAA MOSFET allows high current drive simply by increasing the number of fingers or parallel stacking of nanowires as depicted in Figure 1.4 and 1.5.

Tremendous effort expended behind silicon nanowires and the incorporation of strain engineering reveal the potential of silicon as a favorable channel material for CMOS technology [48–50]. However, phonon scattering and surface roughness from wrap-around gate configuration limits the mobility to subpar levels, impeding the performance of silicon nanowires to reach near ballistic limits. This opens room for further improvement in carrier transport by utilizing high mobility III-V semiconductor channel materials.

To this end InGaAs has attracted the attention of researchers as a viable candidate to provide superior drain current in both on and off-state [51–53]. On the one hand, intense research in the past four decades have ushered significant progress on the use of atomic layer deposition to integrate thermodynamically stable high-κ dielectric on III-V semiconductor, which drastically reduces gate leakage current of InGaAs based transistors, offering better effective oxide thickness (EOT) for minimization of static power dissipation [54]. On the other hand, the inherent high mobility of III-V semiconductor as the active channel material truncates dynamic power dissipation in the transistor, offering the same drive current at a reduced supply voltage [55]. This favoured InGaAs gate-all-around MOSFETs to gain popularity in switching and logic applications [53].

Although III-V FETs could not decisively outperform industrial silicon FETs at the beginning, partly due to the lack of native gate oxide problem, when aluminum oxide (Al_2O_3) was discovered to be an excellent oxide on the InGaAs system, rapid progress began in this class of material devices and state-of-the-art gate stacks now exhibit defect densities similar to those of silicon FETs [22, 56]. III-V multigate MOSFETs received extensive consideration from the research community for potential use in digital application. Kim *et al.* demonstrated InGaAs tri-gate FETs with channel width and height of 20 nm, exhibiting on-current of 410μA/μm (at V_{DD}=0.5V and I_{OFF}=100nA/μm). Radosavljevic *et al.* also reported tri-gate InGaAs FETs, demonstrating good electrostatic control and relatively high-quality oxide interface [57–59]. Gu *et al.* demonstrated gate-all-around InGaAs FETs with superb electrostatic control [60]. Waldron *et al.* also demonstrated gate-all-around InGaAs devices fabricated on Si substrate with excellent performance [28]. In all these reports, the non-planar

channel were created by etching using a mask for channel definition.

Other published works include non-etching methodologies. For instance, Schmid *et al.* used templated-assisted selective-epitaxy (TASE), allowing for integration on silicon substrates as well as implementation of heterostructure systems [61, 62]. Lee *at al.* also used TASE along with a gate-last process to demonstrate a 39 nm-L_g InGaAs GAA nanosheet whose peak g_m was reported to be 1.37 mS/μm and an excellent subthreshold slope of 72 mV/decade. Vertical transistors characterized by the flow of carriers in the channel from source to drain in vertical direction have also gained attention in recent times.

State-of-the-art vertical transistors utilizing vapour-liquid-solid (VLS) catalyst-based growth to form the nanowire channel, have been reported by Berg *et al.*, demonstrating excellent performance [63], as well as Svensson *et al.*, demonstrating co-integration with gallium antimonide (GaSb) p-channel FET for CMOS circuits [64]. Contrary to the top-down approach, VLS is a bottom-up approach producing high-aspect ratio nanowires with atomically smooth sidewalls and uniform diameters along the axial directions. It is also convenient to scale down the diameter in this process, which is primarily determined by the size of the seed dots. Jung *et al.* recently demonstrated sub-10 nm InAs nanowire with a minimum diameter of 2 nm from Au seeded growth [65]. Also by defining Au dots in a lithographical method, ordered nanowires can be realized. The most attractive benefit of the VLS method is probably the direct integration of III-Vs on a lattice-mismatched substrate, such as silicon. Below a certain critical diameter [66], high-quality nanowires can be grown epitaxially on a foreign substrate without generating axial dislocations, which is an alluring prospect of III-V nanowires for CMOS application, requiring both n-channel and p-channel materials on one substrate. Other forms of bottom-up approach for growing III-V nanowire are outlined in [19], elaborating on the pros and cons of each fabrication viewpoint.

Nanowires with one-dimensional columnar shape has gained enormous attention, particularly for their ability to confine carriers in 2-dimensions, thereby allowing them to propagate freely in the third dimension [67–69]. Owing to the good optoelectronic

properties of III-V semiconductor materials, a wide range of methods have been used to fabricate nanowires in photovoltaic applications, typically as solar energy harvesters, such as laser ablation, metal-organic vapor phase epitaxy, chemical beam epitaxy and molecular beam epitaxy to name a few [70–74]. Thus, III-V nanowires have a strong hold in the optoelectronic area as the successor of next generation photovoltaics.

Besides experimental demonstrations of the various forms of multigate transistors in the literature, there had been a concomitant progress in the analytical studies conducted by various luminaries to provide an in-depth analysis of the device physics undergirding each type of transistor in operation.

In 1994, Francis *et al.* proposed an analytical expression for the potential, charge and electric field within the channel region of a double-gate nMOS/SOI device [75]. Given the apparent simplicity of the model, the results were confined to weak inversion and below threshold operation of the device. In the subsequent year, the extent of the model was elaborated to moderate inversion regime with drain current and transconductance bearing strong resemblance with MEDICI simulations [76].

Taur *et al.* provided an analytical solution to double-gate MOSFET with undoped body by incorporating only the mobile charge term into the Poisson equation [77]. Four years later, the authors succeeded in devising a continuous drain-current model for the same device, derived directly from Pao-Sah integral without the necessity of charge sheet approximation [78]. Given the compact nature of the expression, this work gained popularity among the circuit designers for simulation of double-gate devices with undoped channel.

In 2002, Pei *et al.* conducted an extensive investigation for FinFET design consideration using three-dimensional (3-D) simulation [79]. Analytical solution of the 3-D Laplace's equation was employed to establish the design equations on the subthreshold behavior in the fully depleted silicon fins. The critical geometrical parameters considered for the FinFET were,

- Physical gate length of the FinFET defined by the spacer gap

- Height of the silicon fin, defined by the distance between top gate and buried oxide
- Thickness of silicon fin, defined by the distance between front and back gate oxides
- Effective channel length of FinFET estimated by the metallurgical junction for abrupt concentration gradient between the source (drain)-channel
- Geometrical channel width, defined at the net gated perimeter of the transistor

These guidelines also serve fruitful for the gate-all-around transistor utilizing III-V channel material.

Chen & Meindl devised a compact, physics-based, short-channel model of subthreshold swing and threshold voltage for undoped symmetric double-gate MOSFETs, the novelty of which includes quantum-mechanical and fringe-induced-barrier-lower effects [80]. In short-channel devices, the channel center has a higher electrostatic potential than anywhere else because of the influence of the source/drain and weakened gate control. Considering the most leakiest path inside the channel, a compact analytical subthreshold swing model was obtained under evanescent-mode analysis [81]. Moreover, it was shown that the conventional way of defining the threshold voltage by the surface band bending equal to $2\phi_{\mathrm{B}}$ becomes irrelevant, where ϕ_{B}=(kT/q)ln($N_{\mathrm{A}}/n_{\mathrm{i}}$) with N_{A} and n_{i} being the doping concentration and intrinsic carrier concentration in the channel respectively. This issue was addressed by solving the 2-D Poisson equation with the inclusion of inversion charge term.

In 2004, Jiménez *et al.* derived a continuous analytic current-voltage model for cylindrical undoped (lightly doped) surrounding gate MOSFETs [82]. The model was shown to agree with three-dimensional numerical simulation from DESSIS-ISE in all operating regions (linear, saturation, subthreshold) and traces the transition between them without fitting parameters, being ideal for the kernel of SGT MOSFET compact models. The channel current was written as an explicit function of the applied voltage, based on a unified charge control model [83]. Ortiz-Conde *et al.* worked on a similar device to unfold the Lambert function-based analytic solution for the surface potential of the

double-gate device. The works of Wei Bian *et al.* though similar to Jiménez *et al.*, differs from previous works in that the drain-current equation accounts for both drift and diffusion current components in terms of the potential at the oxide-semiconductor interface as well as at the center of the device body evaluated at the source and drain terminals [84]. This model allows room for inclusion of other second-order physical effects integrated in the form of add-on modules.

With much research on analytic reports of double-gate and surrounding gate MOSFETs, Yu *et al.* suggested a unified explicit solution of drain current for multi-gate MOSFETs, based on the former two devices [85, 86]. The primary assumption underlying this union was that the inversion charge in subthreshold is proportional to the silicon cross-sectional area (volume inversion), whereas the inversion charge above threshold is proportional to the gated perimeter of the silicon body. Using Ward-Dutton linear charge partitioning, fully compact expression of all the nine capacitance coefficients were obtained directly based on the charge conservation law [87].

In 2007, Tsormpatzoglou *et al.* semi-analytically studied the short channel effects in silicon and germanium double-gate MOSFETs [88]. 2-D potential distribution is derived along the channel of the symmetric double-gate device in weak inversion regime. A semi-analytical expression for the subthreshold current is proposed along with extraction of other vital subthreshold performance metrics such as drain induced barrier lowering and threshold voltage roll-off. An analysis between Si and Ge as channel material reveals that Ge double-gate MOSFETs are more prone to SCEs.

Moldovan *et al.* studied a similar device with highly-doped channel which are more opted for baseband analog applications [89]. By this time, numerous analytic reports for undoped body double-gate MOSFETs were available in the literature. This work presents a unified charge control model for the first time for doped double-gate transistors. The difference of surface and center potential was assumed constant from subthreshold to well above threshold, an approximation that remains valid for highly-doped channel and expedites the solution of transcendental equation formed by the relation of surface potential with gate bias. In addition, fully compact expression for

intrinsic capacitances were obtained, making the model highly desirable in circuit simulation.

The effect of body doping on threshold voltage and channel potential of double-gate MOSFET was only analyzed in the below threshold region. Liu *et al.* formulated a global continuous channel potential solution, valid for a wide range of doping concentrations from accumulation to strong inversion operation [90]. The study reveals that in the doped transistors, the geometric parameter dependence of the threshold voltage are different from that in intrinsic ones. The robustness of the model is verified from a good initial guess to facilitate the solution of channel potential.

Han *et al.* developed a continuous and analytic channel potential model for lightly doped GAA nanowire FET based on 6H-SiC [91]. The model adequately describes the inversion charge, incorporating the influence of incomplete dopant ionization, backed up by TCAD simulation. In spite of a unified drain current model in [87], the notion of equivalent capacitance was proposed by Chevillon *et al.* to generalize the so-called equivalent-thickness concept to model arbitrary shapes of lightly doped non-planar multigate MOSFETs without adoption of any unphysical parameters [92]. The model merely maps any multigate geometry such as quadruple-gate, triple-gate, triangular gate, cylindrical gate-all-around and double-gate FinFET into the renowned double-gate MOSFET topology. The robustness of the model is verified for a range of temperatures without the need for any additional empirical parameters.

With strong motivation to reduce SCE in deeply scaled transistors, it was imperative to incorporate quantum mechanical effect into the physics based analytical reports. In this respect, an analytical model was proposed to calculate the potential and inversion charge of III-V cylindrical Surrounding-Gate MOSFET (SGT) by Marin *et al.* [93]. The developed model contains expression for the calculation of subband energies and their corresponding wavefunctions, taking into account their penetration into the gate insulator and the effective mass discontinuity in the semiconductor-insulator interface for this class of device, which is imperative to accurately devise the physics of low-effective-mass materials such as InGaAs. The model considers Fermi-Dirac statistics

in conjunction with two-dimensional quantum confinement of the carriers. The solution of Poisson and Schrodinger equation is accompanied by the cylindrical symmetry of the device and the isotropic effective mass of Γ valley of the III-V material. Given the higher electron mobility in $In_xGa_{1-x}As$ channel in comparison to silicon, and the superb control of the channel charge exerted by the surrounding gate configuration is well presented by the self-consistent analytical results, accurately mapping the spatial charge distribution within the channel in coherence with quantum confinement. This work is later expanded into a physically based gate capacitance and drain current model for III-V nanowires [94, 95]. Different factors were explicitly accounted to reflect their contribution to gate capacitance. In this manner, the total gate capacitance is more meaningful in that it distinguishes between insulator and quantum capacitance exhibited by the short-channel device.

In a similar fashion Khosru *et al.* and Khan *et al.* studied the electrostatics and transport behavior in a gate-all-around InGaAs nanowire MOSFET with square cross-section [96, 97]. Finite element method was implemented to determine the solution of Poisson and Schrodinger equation in a coupled manner, taking wave function penetration, energy level splitting and other quantum effects into account. The impact of various physical/process parameters such as alloy composition, oxide thickness, fin-width and doping density on capacitance-voltage characteristics were explored. The prospect of utilizing high-κ gate dielectric has long been favoured in the semiconductor industry. The effect of such high-κ insulators on long channel threshold voltage were semi-analytically explored. The study reveals that for lower channel doping fin width mostly affects threshold voltage whereas in highly doped channel, the threshold voltage variation is prone to oxide thickness and permittivity. Transport characterization of experimentally demonstrated nanowire MOSFET in near-ballistic regime were performed using Uncoupled Mode Space approach [98]. As an appendage, ballistic transport characterization of the same device were carried out in axially composition graded $In_{1-x}Ga_xAs$ channel, revealing an on-off current ratio of 10^7, drain induced barrier lowering of 43.79 mV/V and near ideal subthreshold swing of 61.37 mV/dec [99].

Eventhough potential distribution were previous studied in the transport direction and

confinement direction separately, a precise modeling framework that spatially maps the potential variation in the three-dimensional space could only be obtained from the more computationally expensive numerical simulation. Borli *at al.* proposed a framework based on conformal mapping analysis of the potential distribution in the device body arising from the interelectrode capacitive coupling, combined with self-consistent procedure to include the effects of inversion charge [100]. The work relates the interelectrode coupling dominating the subthreshold behavior of double-gate device to cylindrical GAA MOSFET by means of a simple geometric scaling transformation, accounting for the difference in gate control of the two device. Moreno *et al.* provided an analytical description of the 2D inversion charge distribution function (ICDF) in square GAA MOSFET [101]. The ICDF is an effective robust formulation that successfully describes the inversion charge centroid and gate-to-channel capacitance, circumventing the complex self-consistent simulation process. From compact modeling viewpoint, this method is considered a good candidate for future scaled integrated circuit technologies.

1.3 Contribution of the Thesis

Electrostatic control in three dimensions has become imperative to reduce the short channel effects (SCEs) in deeply scaled transistors beyond the 22nm technology node. Aggressive scaling of transistors to conform Moore's Law have eventually convinced researchers to investigate the prospects of multi-gate MOSFETs [5]. The gate-all-around (GAA) MOSFET has proven to provide greatest immunity to SCEs with the shortest natural length (λ) and imposing stronger gate control over surface carriers. Although both cylindrical nanowires and rectangular GAA MOSFETs have exhibited excellent transport and subthreshold performance recently [28, 102], the rectangular geometry offers additional advantage in terms of fabrication viewpoint:

- Rectangular GAA MOSFET can be grown epitaxially into thin and wider nanosheets in stacked configuration unlike cylindrical nanowire MOSFETs which are grown by vapor-liquid-solid (VLS) method [19]. This enables precise control of nanowire height in rectangular geometry. One of the challenges in fabricating cylindrical

nanowire is controlling the shape of the nanowire, since transport properties rely heavily on nanowire diameter [103]. This difficulty is circumvented in rectangular GAA MOSFET with etching techniques allowing exact control of nanosheet width.

- Monolithic 3D transistor stacking can be employed with ease for rectangular nanosheet. The use of interlayer dielectric has resulted into reduction of parasitic capacitance for a given active width, giving more W_{eff} for the same footprint [47]. Even though pitch scaling allows cell height scaling, thereby rendering a viable path for density scaling in next generation transistors, it has been shown that a single wide nanosheet stack has superior intrinsic performance making it lucrative for use in 3D stacked configuration with monolithic heterogeneous integration through layer transfer technologies.

- The semiconductor industry is already reaping the advantages offered by FinFET transistor. Rectangular horizontal nanowires bear strong similarity with FinFET architecture, having minimal deviation. Thus fabrication of GAA MOSFET could be easily adopted by the industry with little technology shift.

- Strain engineering is essential to improve short channel performances [104]. The extent of strain incorporated in the lateral or vertical rectangular GAA MOSFET depends on the orientation of nanowire growth. Integration of inner spacers and raised source/drain may induce strain relaxation or inject excess compressive strain in the InGaAs channel, thus offering the potential for process-induced strain modulation in 3D stacked nanowire devices.

There have been numerous experimental reports on InGaAs MOSFET exhibiting high drain current and excellent subthreshold characteristics [51,52,105,106]. Recently, short channel InGaAs GAA nanowire has been demonstrated via top down approach and numerical simulation of such device illustrated volume inversion inside the active region for fin width as low as 30 nm, which otherwise would require deca-nanometer dimensions for silicon counterparts [60, 107]. Quantum mechanical simulations were carried out by Khan *et al.* to determine electrostatic charge and carrier transport under uncoupled mode space approach which is computationally expensive and often depend on the numerical convergence of the solution. Existing analytical models de-

veloped for double-gate MOSFETs cannot be extrapolated to GAA geometry without involving proper physics into the Poisson equation. Compact models developed for silicon nanowires uses a constant difference of potential between center and surface which results into deviations near threshold region and cannot be applied into strong inversion operation [89]. Moreover, in InGaAs MOSFETs, a saturation of the decrease of subthreshold current is observed due to high drain junction leakage which is not reflected by silicon based analytic reports [55]. Besides, fixed oxide charge and interface trap defects are neglected in those models, which is significant in high-κ oxide/semiconductor interface and crucial for device performance evaluation. An efficient analytical model is therefore due for characterizing the electrostatic and transport behaviour of depletion mode GAA MOSFET that would predict the performance metrics with scaling of process parameters, taking interface trap states into account and provide a feasible pathway for implementation in circuit simulation.

1.4 Objective of the Thesis

An analytical model capable of regenerating the device performance metrics with impeccable accuracy utilizing minimal computational resources is highly desirable for circuit designers. Given the plethora of analytic reports on cylindrical surrounding gate MOSFETs with undoped/doped channel, the need for an amenable formulation of surface potential without the use of empirical parameters or regional approximation is necessary to gain insight into the device physics of a symmetric square gate-all-around MOSFET utilizing InGaAs as channel material. Though interface defects have been reduced to benign levels in practical demonstrations, their impact must be taken into consideration in the modeling framework.

A rigorous investigation of the electrostatics and transport properties of InGaAs gate-all-around nanowire MOSFET is vital to make a comprehensive study of the device performance metrics. Based on a core long channel model, and keeping the scaling guidelines set by ITRS, various non-ideal effects including short channel effect, mo-

bility degradation at the interface due to surface roughness and phonon scattering, carrier-carrier scattering, corner effects in the rectangular cross-section, velocity saturation, channel length modulation and inherent parasitic resistance arising from the source/drain contacts were imposed to reflect a true picture of the complex physics underpinning short channel operation of this high-utility GAA device. My thesis serves the research community by including all the effects mentioned above. The objectives of this work are recapitulated below:

- To derive an analytical formulation for the surface potential as a function of gate bias, facilitating the capacitance-voltage profile which serve as a blue print for efficient operation of GAA InGaAs MOSFET.

- To devise a comprehensive transport model for the GAA device in long channel operation under classical drift-diffusion formalism, which is later complemented with non-ideal phenomena such as short channel effects, mobility degradation, parasitic resistance, velocity saturation, channel length modulation, etc to implicate the underlying physics of short channel operation.

- To present an explicit analytical expression for long channel threshold voltage of the device, necessary for predicting the threshold-voltage roll-off with aggressive scaling of the channel length.

- Extraction of performance metrics in the ON-state and OFF-state of the device with scaling of certain process parameters such as fin width, oxide thickness, doping concentration, material composition, etc.

- To explore the feasibility of incorporating high-κ dielectric as the gate insulator, thereby providing a comparative analysis between two gate insulator with excellent interfacial quality on InGaAs.

The analytical model laid out in this work will act as a precedent for device design and optimization of high current drive, gate-stacked nanosheet using high mobility III-V channel material and pave the way to acquire compact solutions for next generation ultra-scaled GAA devices suited for future application.

1.5 Organization of the Thesis

The entire thesis can be broadly categorized into five chapters, the details of which will be briefly outlined below.

The first chapter introduces the motivation for exploring multi-gate transistors along with adoption of III-V channel materials over traditional silicon. An extensive historical perspective of transistors is drawn out in a chronological order, encompassing the concomitant progress in both experimental demonstrations and analytical model formulation, and how the gate-all-around nanowire MOSFET has slowly supplanted the double-gate and FinFET devices for logic and switching applications.

The electrostatic model development is laid out in chapter two, leading to the determination of surface potential and eventually the capacitance-voltage profile. The model implicitly accounts for the impact of various device parameters including fin width, oxide thickness and doping concentration on the electrostatics of the gate-all-around MOSFET. In addition, a threshold voltage model is presented in this chapter for a long channel InGaAs GAA transistor utilizing the well-known double derivative methodology.

The third chapter mainly deals with the development of carrier transport in InGaAs gate-all-around MOSFET. To cohere with the internal physics of short channel operation, several non-ideal effects present in deep submicron devices are included such as short channel effect, mobility degradation at the interface and bulk, velocity saturation, channel length modulation and parasitic source/drain resistance. Transfer and output characteristics obtained from the transport model are utilized to obtain several off-state performance metrics such as threshold voltage roll-off, subthreshold slope and drain induced barrier lowering.

In the fourth chapter, several aspect of Sentaurus Device TCAD is highlighted, which are necessary complete simulation of GAA nanowire MOSFET. The process of creating a proper meshed device structure is outlined, followed by a thorough review of the several segments that comprise the pseudo programming script of Sentaurus SDevice

module. Several exemplary snippets are also employed in this chapter to elucidate the workflow of the TCAD.

The results obtained from the electrostatic and transport model in the preceding sections are exhibited in the fifth chapter. The soundness of the analytical results are verified with published experimental reports and numerical simulations. An elaborate performance evaluation is conducted with scaling of physical process parameters in order to perceive a deeper understanding of this high-utility device subject to varying high-κ dielectric for improved device operation.

The final chapter draws the conclusion of my entire thesis, tracing the objectives fulfilled in this venture and highlight possible scope for further improvement in future studies.

Chapter 2

Electrostatic Model Development

Predictive models are necessary for fast developing devices that must be reliable at the same time. To ensure this feature, a robust analytical model must always be validated with results obtained from experimental demonstrations or technology computer-aided design (TCAD) simulation with inclusion of physics model pertinent to realistic device operation. The electrostatic model development of this thesis involves the solution of quasi 2-D Poisson equation using gradual channel approximation and simplifying assumptions which are validated by numerical analysis. The surface potential obtained from the solution of the Poisson equation accompanies the determination of mobile carrier density which are modulated by the gate bias and responsible for participating in the transport mechanism.

This chapter first describes the geometry of the GAA device under consideration with Cartesian coordinates defined to ease the solution of the Poisson equation. The carrier density obtained is used in derivation of the gate capacitance. A threshold voltage model for long channel operation is also proposed in this chapter which will be used in the subsequent chapter for short-channel operation.

2.1 Basic Device Structure

The gate-all-around nanowire device structure can be divided into two major regions: the channel and the gate.

The primary element of the GAA device structure is the channel. It contains the major path for current flow in the transistor. There is an abrupt n^+-p junction present at either ends of the channel in the path of the current flow to ensure ohmic contacts for n-channel operation and vice versa. The device properties change polarity along with dopant material. In other words, the applied voltage polarity for activation and direction of current flow switches side along with dopant polarity. For simplicity, n-channel operation with an initial p-doped channel region will be described which holds true for the opposite polarity as well.

The channel consists of two terminals along two distinct edges: the drain terminal and the source terminal. The terminals are completely identical and interchangeable in lateral nanowires just like a basic FET structure. However, in vertically grown nanowires, the drain is usually located at the upper end of the channel. In lateral GAA devices, the terminal with higher voltage is known as the drain terminal and the lower is referred to the source as in NMOS structure. With switching of terminal voltage during operation, the terminal polarity switches sides. In case of p-channel device, the lower voltage terminal is referred to the drain and the higher one is source, to comply with the PMOS notations. As a result, channel current in n-channel device flows from drain to source, and hence it is termed as the Drain current.

The second significant device element is the Gate. It is often referred to the Gate terminal of the device, which combined with the Drain and Source terminals, complete the three-terminal structure of the transistor. The gate acts as the switching regulator of the transistor. When a significant voltage is applied at the gate terminal, the device is turned on, and constant current flows through the channel. The limiting value is generally termed as the threshold voltage of the device.

The GAA structure encloses the device in all four directions. The triple-gate (TG)

structure basically has 3 directional encapsulations, similar to a doorway arch, as the channel passes through the door. The double-gate (DG) structure, on the other hand, encloses the channel from only two directions, opposite to each other. Hence, for all acts and purposes, the gates and the channel can be viewed as a sandwich structure. In a Double-Gate structure, the channel is covered from two opposite directions with the gate structures. However, although the gate structures are physically isolated, they are electrically coupled together. That is, both gate structures are connected to the same voltage source, so that both ends of the channel are induced with the same gate voltage. The gates are placed along an axis perpendicular to current flow i.e. if current flow is considered to be along Z axis, the gates are placed along X axis. With variation of gate voltage, the channel surface charge density along YZ plane varies, turning the device ON or OFF or keeping in between. However, more complex variation occurs for TG or GAA structure.

The multigate device structure possesses several improvements over tradition single gate structure. Multi-gate device structure can be used to improve gate control over the channel and hence alleviate the short channel effect. The GAA structure provide the best utilization of the advantages of multigate structure due to the complete encapsulation of the channel region.

To fabricate the gate, various materials are available. Classic metal gate structure is still feasible, while current trend of polysilicon gates are well suited in fabrication perspective. For the sake of this study, a low work-function metal, specifically tungsten nitride (WN) will be used as the gate metal.

An insulator layer distinguishes the channel region from the gate material. To ensure proper device operation, the insulator should have low conductivity. In addition, to reduce lattice mismatch during fabrication, the lattice constant of insulator and channel material should be closely matched. Traditionally, the Oxide and Nitride layer of the native channel semiconductor is used as the insulator material. Since very high interface quality can be produced with atomic-layer-deposited (ALD) Al_2O_3 over InGaAs, the respective oxide is used as the gate dielectric.

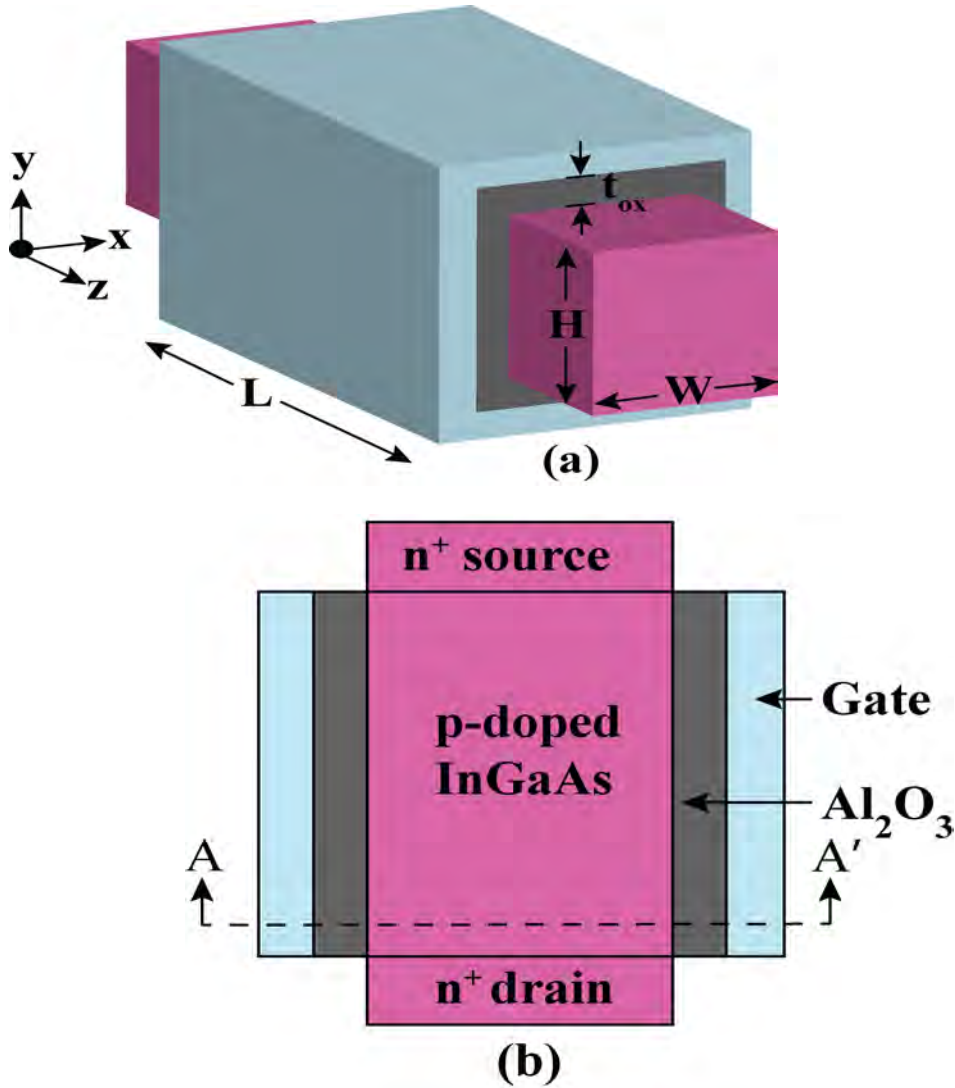


Figure 2.1: **Schematic view of a GAA MOSFET.** The source/drain is heavily doped for ohmic contacts and the $In_{0.53}Ga_{0.47}As$ channel is p-doped. (a) Perspective view. (b) Lateral view.

2.2 Charge Modeling

The symmetric gate-all-around MOSFET under consideration has acceptor doping concentration N_A in the InGaAs channel with equal width (W) and height (H), gate length L and ALD Al_2O_3 having thickness t_{ox} as shown in Figure 2.1a. The central nanowire axis is taken as the origin so that the oxide/semiconductor interface is at $x = y = \mp W/2$. The present study encompasses lateral nanowires grown via top-down

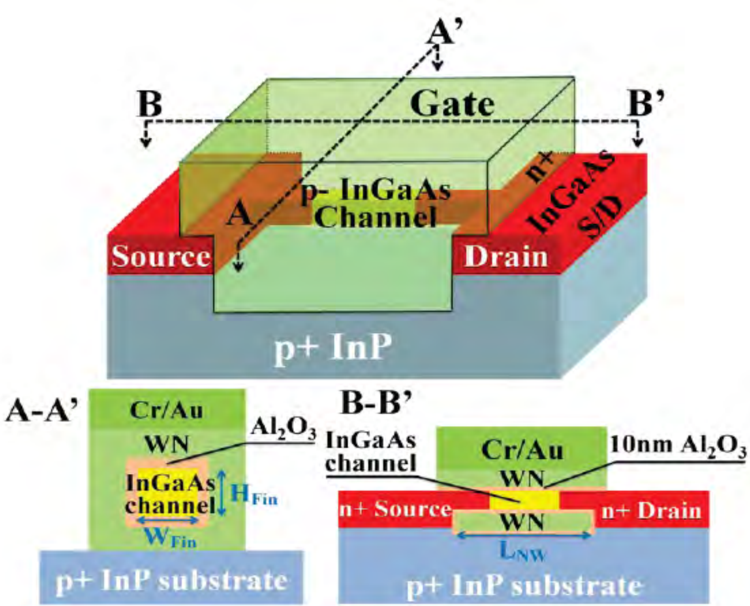


Figure 2.2: **Schematic view of an inversion mode GAA n-channel $In_{0.53}Ga_{0.47}As$ ($2 \times 10^{16}/cm^{-3}$) MOSFET with ALD 10nm Al_2O_3/20nm WN gate stack.** A heavily doped wide bandgap InP lies underneather the bottom gate. [60]

approach on a p^+ (100) InP substrate by molecular beam epitaxy as illustrated in Figure 2.2

2.2.1 Energy Band Diagram

As an inversion mode device with n-channel operation, gate voltage in the GAA MOSFET is used to attract or repulse carriers in order to construct an inversion layer near the oxide/semiconductor interface to facilitate current flow through the channel. The operation of the GAA MOSFET can be well comprehended by analyzing its energy band diagram for different gate voltage conditions. It is already known from the fundamental knowledge of electronics, that during formation of junction, the different materials present in the structure attempt to match their Electrochemical Potentials, also referred to as Fermi Levels along the same energy level. In case of a p-n junction, as seen in traditional electronic devices, the p-type material is doped using Group-III materials with electron deficiency. Hence the Fermi level exists closer to the valance band. On the contrary, due to being doped with Group-V materials, the n-type material has its Fermi level near the conduction band. Now, during the formation of

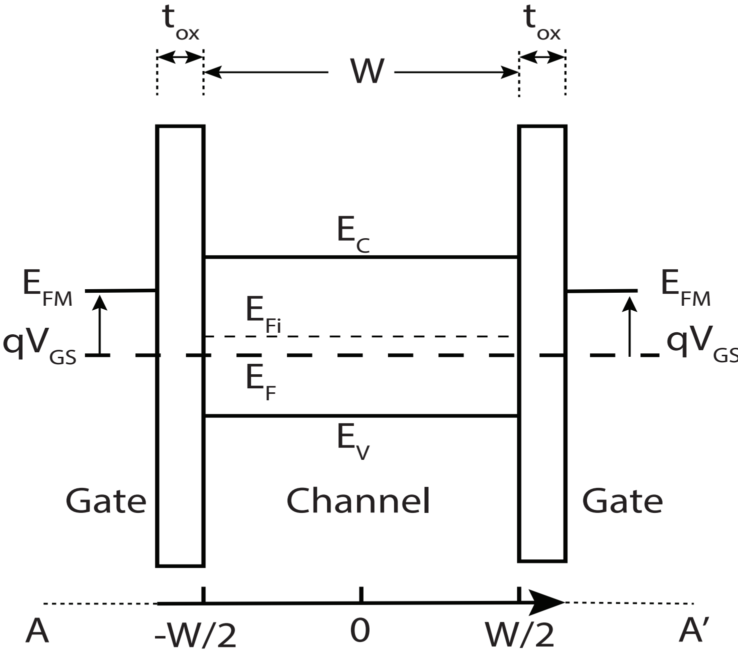


Figure 2.3: **Energy band diagram of a GAA MOSFET having p-doped channel in Flat band condition.** The channel width is W, oxide thickness t_{ox}. E_{F}, E_{Fi} and E_{Fm} are the Fermi level of the p-doped channel, intrinsic Fermi level and work function of the gate metal.

junction, the levels tend to match along the junction region, resulting in a bending of the conduction band, valance band and intrinsic Fermi level of the materials along the area. The region of band bending, i.e. the depletion or space-charge region, is less n-type inside the n-region due to presence of static positive charge within it. The opposite is true for the p-region.

Although no direct junction is formed between gate and channel, the excess charges of the gate and channel regions attract each other through the oxide layer, often with the assistance of trapped oxide charges present in the oxide, but no current can flow. Hence, energy band bending can be observed in the conduction and valance band of the channel region as space charge region is formed. Figure 2.3 presents the energy band structure that would have been present in the device in absence of electrochemical equilibrium. The p-doped channel, considered here, has its Fermi level closer to the valence band, as a large energy gap exists between the channel Fermi level and the gate work function.

For voltages higher than the Flat Band voltage, band bending begins. The elec-

trochemical potential decreases as positive electric potential is increased along the material axis. With increasing gate voltage along the gate terminal, the gate Fermi level would decrease, i.e. move toward the valance band. Moreover, since potential decreases with distance from source, the channel would experience an effective negative voltage according to Kirchhoff's Voltage Law. As a result, the channel Fermi Level would tend to move upward nearer to the conduction band.

From standard I/V relations of an inversion-type GAA MOSFET in Figure 2.4, we can see that with increasing gate voltage from the Flat band condition, the transistor approaches threshold condition where sufficient mobile charge density gathers in the active channel for current flow. The conduction band and valance band bending occur by the amount of ΔE along the surface of the channel-oxide interface. So, potential varies from ϕ_{c} to ϕ_{s} from the core of the channel to the surface regions. Hence, a space charge region exists almost throughout the channel cross-section. This is known as the Full Depletion mode of the device operation [108]. The energy band diagram of the GAA MOSFET near threshold is portrayed in Figure 2.5.

The Fermi level matching in thermal equilibrium occurs due to the tendency of materials to maintain equilibrium charge density throughout the surface. But, when a voltage is applied, the equilibrium condition no longer persists. Hence there would be a mismatch of Fermi levels present in the device, resulting in sharp bending of the conduction and valance bands as shown in Figure 2.6.

2.2.2 Surface Potential and Mobile Charge

In the normal operating regime, the majority carriers can be neglected, which leads to charge density ρ as,

$$\rho = -q\left(\frac{n_{\mathrm{i}}^2}{N_{\mathrm{A}}}\mathrm{e}^{\frac{\phi - V}{\phi_{\mathrm{t}}}} + N_{\mathrm{A}}\right) \tag{2.1}$$

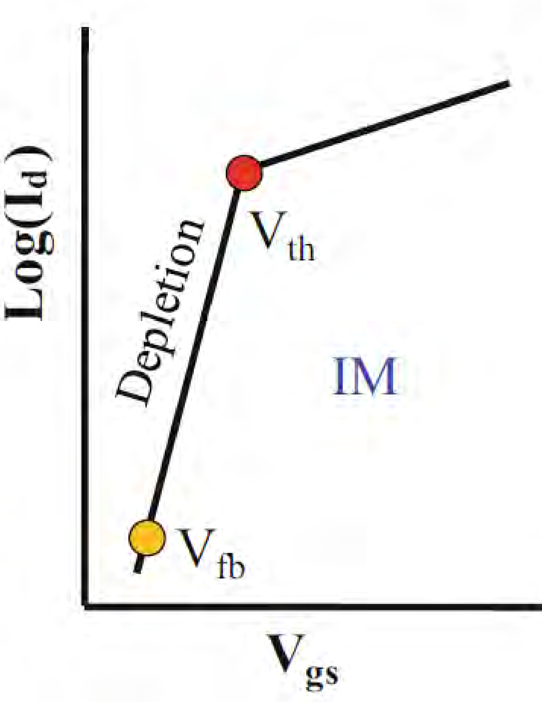


Figure 2.4: **Drain current as the function of V_g in an inversion-mode device.** [109]

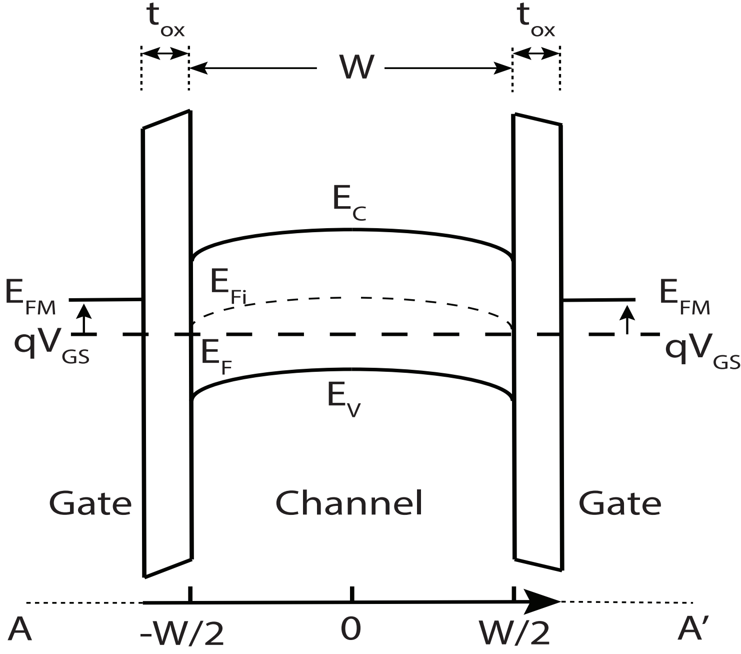


Figure 2.5: **Energy band diagram of a GAA MOSFET having p-doped channel near threshold condition.** The channel width is W, oxide thickness t_{ox}. E_F, E_{Fi} and E_{Fm} are the Fermi level of the p-doped channel, intrinsic Fermi level and work function of the gate metal.

where q is the electronic charge, n_i is the intrinsic carrier density of $In_{0.53}Ga_{0.47}As$, N_A is the acceptor doping concentration, V is the quasi fermi level of electron with

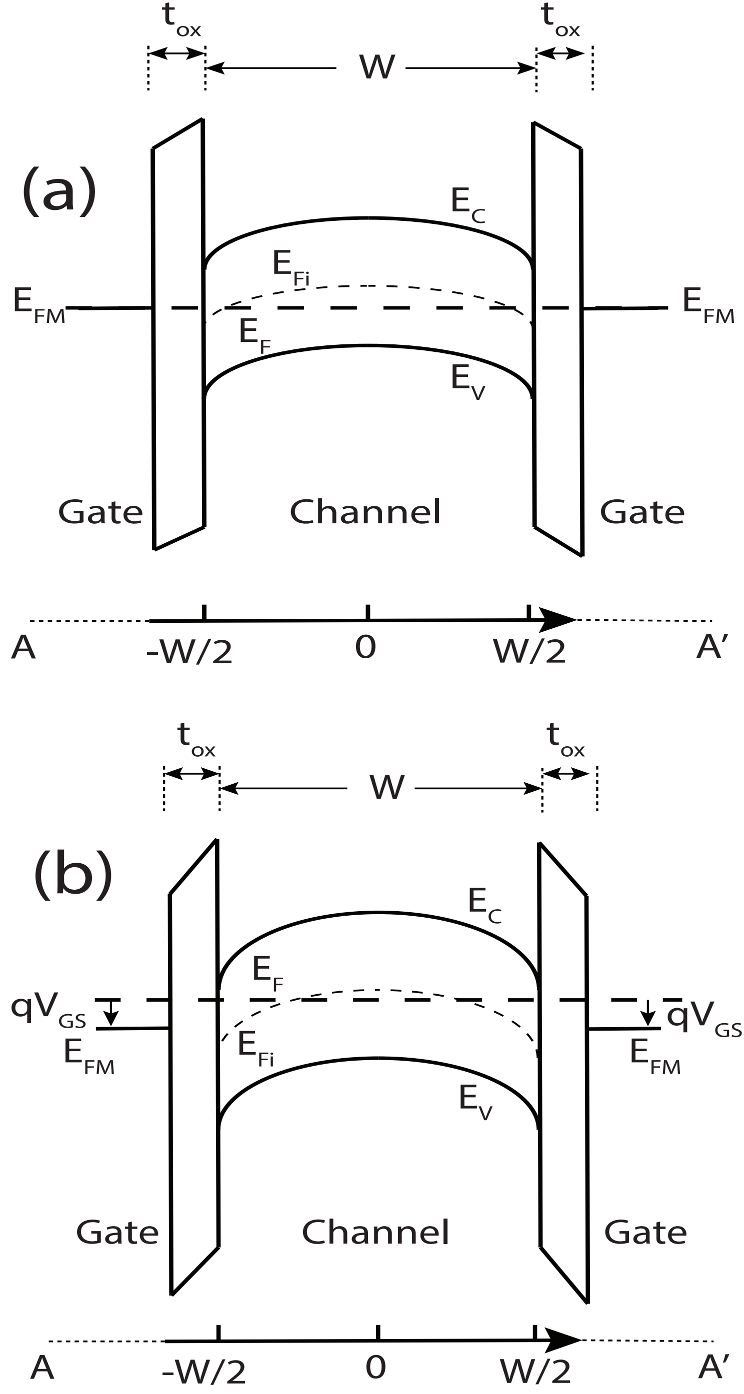


Figure 2.6: **Energy band diagram of a GAA MOSFET.** (a) In thermal equilibrium. (b) At strong inversion. The mismatch in the gate Fermi level and that of the semiconductor results due to application of a large gate bias.

reference to source and $\phi_{\mathrm{t}} = kT/q$ is the thermal voltage.

Since the channel is much larger than fin width, gradual channel approximation applies to quasi 2-D Poisson equation of a long channel GAA MOSFET [110],

$$\frac{\mathrm{d}^2\phi}{\mathrm{dx}^2} + \frac{\mathrm{d}^2\phi}{\mathrm{dy}^2} = \frac{qN_{\mathrm{A}}}{\epsilon_{\mathrm{s}}}\left(\mathrm{e}^{\frac{\phi-2\phi_{\mathrm{f}}-V}{\phi_{\mathrm{t}}}} + 1\right) \tag{2.2}$$

here, ϵ_s is the semiconductor permittivity, $\phi_f = \phi_t \ln\left(N_A/n_i\right)$, x and y represent the width and height directions respectively.

Due to symmetric cross-section, the electric field is identical in magnitude in both x and y direction, verified by 3-D numerical simulations as shown in Figure 2.7. Thus, the simplifying assumption $\frac{\mathrm{d}\phi}{\mathrm{dx}} = \frac{\mathrm{d}\phi}{\mathrm{dy}}$ applies in (2.2) and multiplying both sides of this equation by $\frac{\mathrm{d}\phi}{\mathrm{dx}}\frac{\mathrm{d}\phi}{\mathrm{dy}}$ leads to,

$$\frac{\mathrm{d}}{\mathrm{d}\phi}\left[\frac{1}{2}\left(\frac{\mathrm{d}\phi}{\mathrm{dx}}\right)^2\right] + \frac{\mathrm{d}}{\mathrm{d}\phi}\left[\frac{1}{2}\left(\frac{\mathrm{d}\phi}{\mathrm{dy}}\right)^2\right] = \frac{qN_{\mathrm{A}}}{\epsilon_{\mathrm{s}}}\left(\mathrm{e}^{\frac{\phi-2\phi_{\mathrm{f}}-V}{\phi_t}} + 1\right) \tag{2.3}$$

$$\frac{\mathrm{d}}{\mathrm{d}\phi}\left(\frac{\mathrm{d}\phi}{\mathrm{dx}}\right)^2 = \frac{qN_{\mathrm{A}}}{\epsilon_{\mathrm{s}}}\left(\mathrm{e}^{\frac{\phi-2\phi_{\mathrm{f}}-V}{\phi_t}} + 1\right) \tag{2.4}$$

Since equation (2.4) does not possess a closed form solution, integrating once from the central nanowire axis to the oxide/semiconductor interface with appropriate boundary conditions [75,110], which are $\phi = \phi_0$, $\frac{\mathrm{d}\phi}{\mathrm{d}x} = 0$ at the central nanowire axis and $\phi = \phi_{\mathrm{s}}$, $\frac{\mathrm{d}\phi}{\mathrm{d}x} = E_{\mathrm{s}}$ at the interface, we get,

$$\int_0^{E_{\mathrm{s}}} \mathrm{d}\left(\frac{\mathrm{d}\phi}{\mathrm{dx}}\right)^2 = \int_{\phi_0}^{\phi_{\mathrm{s}}} \frac{qN_{\mathrm{A}}}{\epsilon_{\mathrm{s}}}\left(\mathrm{e}^{\frac{\phi-2\phi_{\mathrm{f}}-V}{\phi_t}} + 1\right)\mathrm{d}\phi \tag{2.5}$$

$$E_{\mathrm{s}} = \sqrt{\frac{qN_{\mathrm{A}}}{\epsilon_{\mathrm{s}}}\phi_{\mathrm{t}}}\sqrt{\mathrm{e}^{\frac{\phi_{\mathrm{s}}-2\phi_{\mathrm{f}}-V}{\phi_{\mathrm{t}}}}\left(1 - \mathrm{e}^{-\frac{\phi_{\mathrm{s}}-\phi_0}{\phi_{\mathrm{t}}}}\right) + \frac{\phi_{\mathrm{s}} - \phi_0}{\phi_{\mathrm{t}}}} \tag{2.6}$$

where, ϕ_{s} and ϕ_0 are the surface and center potential of the nanowire MOSFET. The surface electric field depends on the surface potential which in turn depends implicitly on the center potential. For simplicity, the difference of surface-center potential is defined as $\alpha = (\phi_{\mathrm{s}} - \phi_0)/\phi_{\mathrm{t}}$ normalized by thermal voltage. In deep subthreshold, full depletion approximation applies to Poisson equation, leading to a constant difference

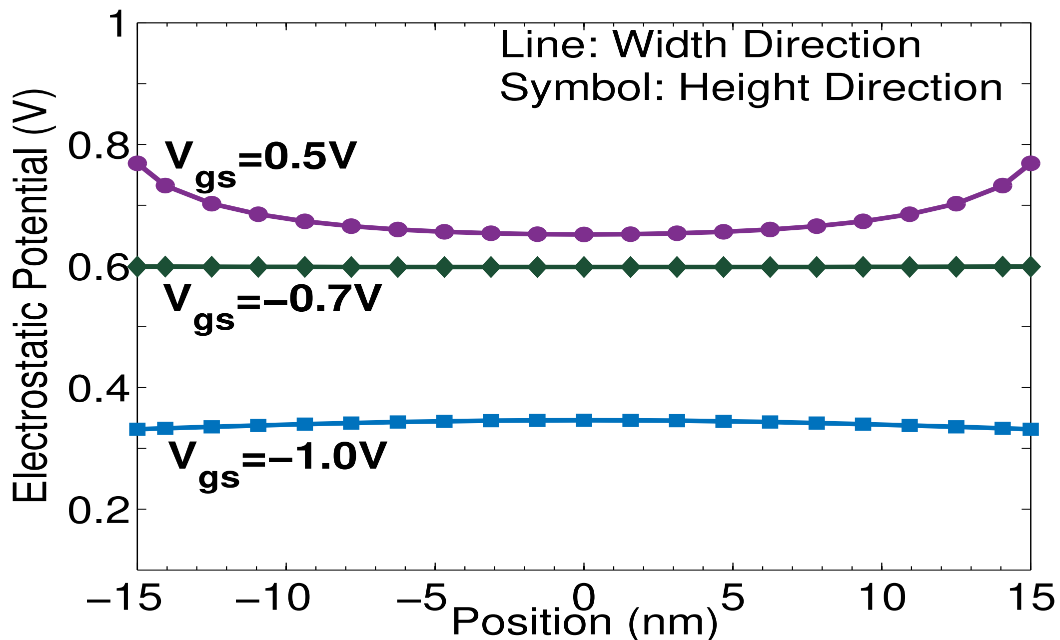


Figure 2.7: **Variation of electrostatic potential along width and height direction at different gate voltages covering from subthreshold to strong inversion.** The symmetry of the gradient of the electrostatic potential from center to surface verifies the assumption $\frac{\mathrm{d}\phi}{\mathrm{dx}} = \frac{\mathrm{d}\phi}{\mathrm{dy}}$ made to simplify Equation (2.2)

of normalized surface-center potential α_{st} defined as [89] (Appendix A.1),

$$\alpha_{\mathrm{st}} = \frac{qN_{\mathrm{A}}W^2}{16\epsilon_{\mathrm{s}}\phi_{\mathrm{t}}} = \frac{Q_{\mathrm{b}}}{16\epsilon_{\mathrm{s}}\phi_{\mathrm{t}}} \tag{2.7}$$

where Q_{b} is the total fixed charge per unit length.

Although the use of constant α_{st} well above threshold is a crude approximation [89], as the transistor moves into strong inversion regime, the difference of potential is no longer constant as portrayed in Figure 2.8. By relying on a coarse finite difference method, an exact expression of the normalized difference of potential above threshold can be written in terms of principle branch of Lambert function [111] (Appendix A.2),

$$\alpha(\phi_{\mathrm{s}}) = \alpha_{\mathrm{st}} + \mathrm{LW}\left(\alpha_{\mathrm{st}}\mathrm{e}^{-\alpha_{\mathrm{st}}}\mathrm{e}^{\frac{\phi_{\mathrm{s}}-2\phi_{\mathrm{f}}-V}{\phi_{\mathrm{t}}}}\right) \tag{2.8}$$

Using equation (2.8) into (2.6) helps to reduce surface electric field in terms of ϕ_{s} only.

$$E_{\mathrm{s}}(\phi_{\mathrm{s}}) = \sqrt{\frac{qN_{\mathrm{A}}}{\epsilon_{\mathrm{s}}}\phi_{\mathrm{t}}}\sqrt{\mathrm{e}^{\frac{\phi_{\mathrm{s}}-2\phi_{\mathrm{f}}-V}{\phi_{\mathrm{t}}}} + \left(1 - \frac{1}{\alpha_{\mathrm{st}}}\right)\alpha + 1} \tag{2.9}$$

Since the space charge density per unit length in the semiconductor is given by $Q_\mathrm{s} = 4W\epsilon_\mathrm{s}E_\mathrm{s}$, from charge conservation, the mobile charge density per unit length follows from the difference of space charge density and fixed charge density.

$$Q_\mathrm{n} = 4W\sqrt{qN_\mathrm{A}\phi_\mathrm{t}\epsilon_\mathrm{s}}\,\sqrt{\frac{n_\mathrm{i}^2}{N_\mathrm{A}^2}\mathrm{e}^{\frac{\phi_\mathrm{s}-V}{\phi_\mathrm{t}}} + \left(1-\frac{1}{\alpha_\mathrm{st}}\right)\alpha + 1} - Q_\mathrm{b} \tag{2.10}$$

In spite of advancement in ALD techniques, significant trap defects exist in the high-κ oxide/semiconductor interface, which are accounted from the flat $\mathrm{D_{it}}$ profile through the relation [97],

$$Q_\mathrm{it} = \int_{E_i}^{E_j} D_\mathrm{it}\,\mathrm{d}E \tag{2.11}$$

where, $E_i = E_0$ and $E_j = E_\mathrm{F}$ if E_F lies above E_0 and vice versa. E_0 is the charge neutrality level of interface defects (~ 0.27eV), which are mainly donor type for Al_2O_3-$In_{1-x}Ga_xAs$ interface [112]. The presence of positive fixed oxide charges Q_f distributed throughout the gate dielectric affects the flat-band voltage V_fb by,

$$V_\mathrm{fb} = \phi_\mathrm{ms} - \frac{Q_\mathrm{f}}{C_\mathrm{ox}} \tag{2.12}$$

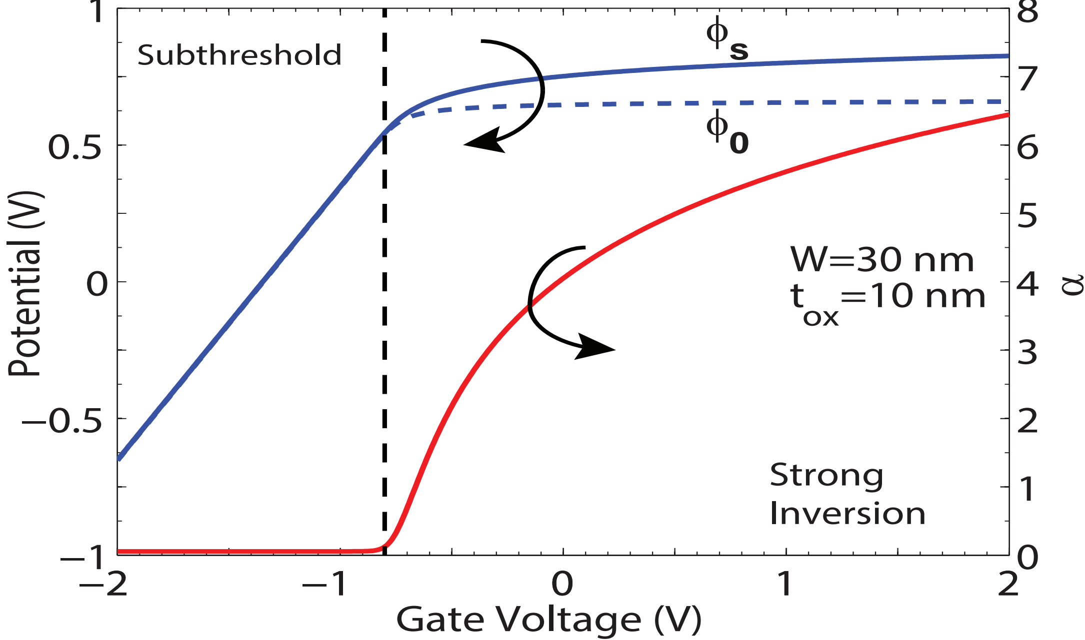


Figure 2.8: **Surface potential (ϕ_s), center potential (ϕ_0) and their normalized difference (α) in subthreshold and strong inversion region with moderate levels of channel doping.** The vertical line roughly differentiates between the two regions of operation. The normalized difference of potential is low and remains constant below threshold condition.

where, ϕ_{ms} is the metal-semiconductor work function difference and C_{ox} is the oxide capacitance per unit length defined as,

$$C_{\text{ox}} = \frac{4W\epsilon_{\text{ox}}}{t_{\text{ox}}} + 8C_{\text{fr}} \tag{2.13}$$

Corner effect in the rectangular cross-section of the MOSFET contributes to oxide capacitance in the form of fringing effects. Depending on the geometry, a simplified expression for fringing capacitance of triple-gate FinFET is proposed in [113,114] which is adapted for the GAA structure to reflect corner effects in electrostatic phenomena as elaborated in Figure 2.9.

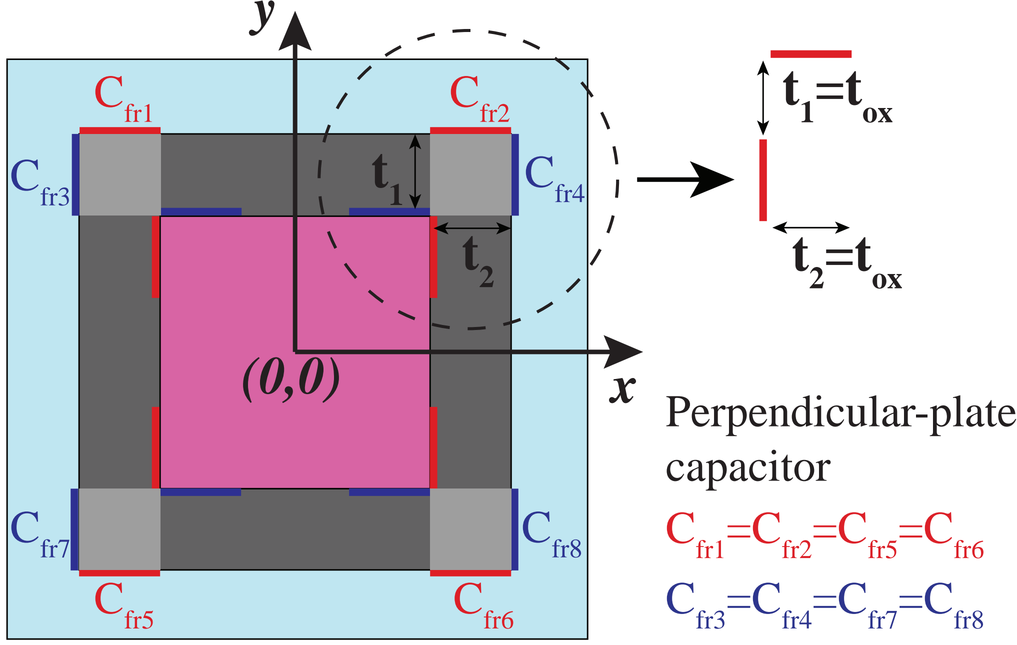


Figure 2.9: **Fringe capacitance schematic for the cross-section of a gate-all-around MOSFET.** The origin is taken as the central nanowire axis. Perpendicular-plate capacitance arising from the corners are denoted by C_{fr} and the oxide thickness is t_{ox}.

$$C_{\text{fr}} = \frac{2\epsilon_{\text{ox}}}{\pi} \ln\left(1 + \frac{t_1}{t_2}\right) \tag{2.14}$$

Here C_{fr} is the fringing capacitance resulting from the perpendicular plate alignment in the corners of the GAA MOSFET, ϵ_{ox} is the permittivity of the gate oxide, $t_{1,2}$ are the oxide thickness as indicated in the schematic diagram. The symmetry of width and height of the GAA MOSFET simplifies the fringing capacitance C_{fr} into,

$$C_{\mathrm{fr}} = \frac{2\epsilon_{\mathrm{ox}}}{\pi} \ln(2) \tag{2.15}$$

The factor of 8 in equation (2.13) comes from the four corners of the GAA geometry.

Applying Gauss's Law to the oxide/semiconductor interface and using (2.9) relates the gate voltage to the surface potential given by,

$$C_{\mathrm{ox}}(V_{\mathrm{G}} - V_{\mathrm{fb}} - \phi_{\mathrm{s}}) = 4W\epsilon_{\mathrm{s}}E_{\mathrm{s}} \tag{2.16}$$

The solution of (2.16) facilitates the evaluation of surface potential necessary for determining mobile charge that is modulated under electrostatic condition and takes part in carrier transport.

$$Q_{\mathrm{n}} = Q_{\mathrm{s}} - Q_{\mathrm{b}} + Q_{\mathrm{it}} \tag{2.17}$$

The approximation of the Lambert function given by (2.18) remarkably improves the speed of the solution in (2.16) with only a minor error introduced in the threshold region as will be discussed in section (5) [115].

$$\mathrm{LW}(\gamma) \approx \ln(1+\gamma)\left(1 - \frac{\ln(1+\ln(1+\gamma))}{2+\ln(1+\gamma)}\right) \tag{2.18}$$

2.2.3 Capacitance-Voltage Characteristics

The quasi-static capacitance-voltage profile is obtained from gated mobile charge density by differentiating Q_{n} obtained in the previous section with respect to gate voltage,

$$C_{\mathrm{G}} = \frac{\mathrm{d}Q_{\mathrm{n}}(V_{\mathrm{G}})}{\mathrm{d}V_{\mathrm{G}}} \tag{2.19}$$

where C_{G} depends implicitly on physical dimensions, material properties and gate dielectric.

2.3 Threshold Voltage Development

As the GAA nanowire MOSFET nears threshold condition from deep subthreshold regime, the difference of surface-center potential can be approximated to be constant as given in (2.7). This assumption is valid since the transistor remains fully depleted at threshold condition [75]. The surface electric field then becomes,

$$E_{\mathrm{s}} = \frac{qN_{\mathrm{A}}W}{4\epsilon_{\mathrm{s}}}\sqrt{1+\frac{1}{\alpha_{\mathrm{st}}}\mathrm{e}^{\frac{\phi_{\mathrm{s}}-2\phi_{\mathrm{f}}-V}{\phi_{\mathrm{t}}}}\left(1-\mathrm{e}^{\frac{-\alpha_{\mathrm{st}}}{\phi_{\mathrm{t}}}}\right)} \tag{2.20}$$

Using (2.20), the effective voltage drop across the oxide-semiconductor can be rewritten as,

$$V_{\mathrm{G}} - V_{\mathrm{fb}} = \phi_{\mathrm{s}} + \frac{Q_{\mathrm{b}}}{C_{\mathrm{ox}}}\sqrt{1+\frac{1}{\alpha_{\mathrm{st}}}\frac{Q(\phi_{\mathrm{s}})}{Q_{\mathrm{b}}}} \tag{2.21}$$

Here, $Q(\phi_{\mathrm{s}}) = Q_{\mathrm{b}}\exp((\phi_{\mathrm{s}} - 2\phi_{\mathrm{f}} - V)/\phi_{\mathrm{t}})(1 - \exp(-\alpha_{\mathrm{st}}/\phi_{\mathrm{t}}))$ is the minority carrier charge controlled by the gate in addition to the depletion charge.

The usual threshold voltage definition, which states threshold voltage to be the gate bias necessary for a surface band bending of $2\phi_{\mathrm{f}}$, is no longer valid for GAA MOSFET. Instead, due to weak volume inversion mechanism, a component of current corresponding to minority carrier flows in threshold condition. The maximum transconductance method provides an accurate description of threshold voltage as the gate bias when $\delta g_{\mathrm{m}}/\delta V_{\mathrm{G}}$ reaches peak value. This translates into [75],

$$\frac{\delta^3 I_{\mathrm{D}}}{\delta V_{\mathrm{G}}^3} = \frac{\delta^3 E_{\mathrm{s}}}{\delta V_{\mathrm{G}}^3} = \frac{\delta^3 \phi_{\mathrm{s}}}{\delta V_{\mathrm{G}}^3} = 0 \tag{2.22}$$

Hence (2.21) is differentiated thrice with respect to gate voltage to reach,

$$\frac{\mathrm{d}^3\phi_{\mathrm{s}}}{\mathrm{d}V_{\mathrm{G}}^3} = \frac{1}{\phi_{\mathrm{t}}^2}\frac{a(\phi_{\mathrm{s}})}{(1+a(\phi_{\mathrm{s}}))^4}\left(b(\phi_{\mathrm{s}})(1-2b(\phi_{\mathrm{s}})) + \frac{2a(\phi_{\mathrm{s}})-1}{1+a(\phi_{\mathrm{s}})}(1-b(\phi_{\mathrm{s}}))^2\right) \tag{2.23}$$

where $a(\phi_\mathrm{s})$ and $b(\phi_\mathrm{s})$ are functions of surface potential given by,

$$a(\phi_\mathrm{s}) = \frac{1}{2u}\frac{Q(\phi_\mathrm{s})/Q_\mathrm{b}}{\sqrt{1+\frac{1}{\alpha_\mathrm{st}}\frac{Q(\phi_\mathrm{s})}{Q_\mathrm{b}}}} \tag{2.24}$$

$$b(\phi_\mathrm{s}) = \frac{\frac{1}{2\alpha_\mathrm{st}}\frac{Q(\phi_\mathrm{s})}{Q_\mathrm{b}}}{1+\frac{1}{\alpha_\mathrm{st}}\frac{Q(\phi_\mathrm{s})}{Q_\mathrm{b}}} \tag{2.25}$$

and $u = C_\mathrm{ox}/16\epsilon_\mathrm{s}$. Equation 2.23 is a non-linear function of ϕ_s only. Solving $\delta^3\phi_\mathrm{s}/\delta V_\mathrm{G}^3 = 0$ provides the surface potential at threshold point (ϕ_sT), which is substituted into (2.21) to determine threshold voltage (V_T) of a long channel gate-all-around MOSFET.

Chapter 3

Transport Model Development

Transport characteristics are essential in that they verify the appropriate functioning of a device. This chapter presents a comprehensive model for transport properties of InGaAs gate-all-around MOSFET. The model formulation begins with the core drain current model applicable for a long channel device. Certain non-ideal effects are later complemented to increase the efficacy of the analytic solution in order to realize the internal physics associated with short channel operation such as short channel effect, mobility degradation due to surface roughness and various scattering mechanisms, velocity saturation, channel length modulation and parasitic source-drain resistance, making the model robust in terms of speed and computational efficiency.

The core drain current of the short channel GAA transistor is expressed in terms of the following integral,

$$I_{\mathrm{D}} = \frac{\mu_{\mathrm{eff}}}{L_{\mathrm{eff}}} \int_{V_{\mathrm{S}}}^{V_{\mathrm{D}}} Q_{\mathrm{n}}(V_{\mathrm{G}} + \Delta\phi_{\mathrm{min}})\ \mathrm{d}V \tag{3.1}$$

where, μ_{eff} and L_{eff} are effective mobility and channel length respectively after accounting for mobility degradation and channel length modulation and $\Delta\phi_{\mathrm{min}}$ is the minimum potential barrier change in the conduction channel as elaborated below.

3.1 Short Channel Effect Correction

Short-channel effects result from the sharing of the electrical charges in the channel region between the gate, on the one hand, and the source and the drain, on the other hand. The source and drain junctions create depletion regions that penetrate the channel region from both sides of the gate, thus shortening the effective channel length. These depletion regions carry electric fields that penetrate the channel region to a certain distance and weakens some of the control of the channel from the gate. Figure 3.1 shows how the gates compete with the source and the drain for the charge in the channel. When the drain voltage is increased, this penetration is amplified. As a result, the potential in the channel region and the resultant concentration of electrons are no longer controlled solely by the gate electrode but are also influenced by the distance between the source and the drain and by the voltage applied to the drain. There are two observable effects that result from this loss of charge control by the gate: drain-induced barrier lowering (DIBL), which causes the threshold voltage to decrease when the drain voltage increases, and a degradation in the subthreshold slope. The effects are additive and both increase the leakage current of the transistors, constituting a serious impediment to further scaling of MOSFETs.

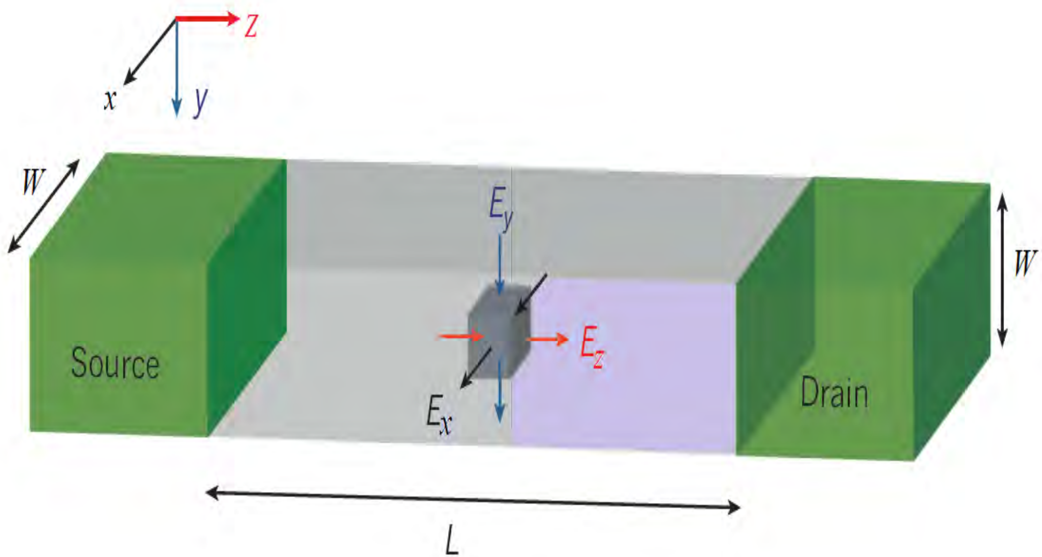


Figure 3.1: **Competition between the different electric fields for an elemental volume in the channel region.** The elemental volume is represented by the small grey cube. The vertical component of the electric field (E_y) arises from the top and bottom gates; the lateral component (E_x), from the side gates; and the longitudinal component (E_z) from the source and drain regions. L, channel length; W, fin width. [3]

The GAA structure is the most promising candidate to follow the scaling trend of next generation ultra-short channel device, providing the least distance between source and drain for a given oxide thickness due to enhanced electrostatic control from multi-gate architecture. Critical geometry parameters responsible for short-channel behavior includes gate length, fin height, fin thickness, oxide thickness and doping in the active region. A rigorous model must therefore include these parameters to reflect accurate scalability over a wide range of device parameters.

The degree of SCE affecting threshold voltage (V_{th}) roll-off, DIBL and subthreshold slope degradation of the short channel transistor can be modeled by the change of the minimum potential barrier inside the conduction channel due to potential coupling from the drain terminal. The potential barrier along the conduction path is minimum in the leakiest path of the transistor which lies in the central nanowire axis of the MOSFET [116]. This minimum potential change is obtained from the solution of quasi 2-D Poisson equation written in terms of ϕ_0 under full-depletion approximation and ignoring inversion carriers,

$$2\frac{\mathrm{d}^2\phi(x,z)}{\mathrm{d}x^2} + \frac{\mathrm{d}^2\phi(x,z)}{\mathrm{d}z^2} = \frac{qN_{\mathrm{A}}}{\epsilon_{\mathrm{s}}} \tag{3.2}$$

In the subthreshold region, parabolic potential profile is assumed in the direction of carrier confinement from gate-to-gate.

$$\phi(x,z) = K_0(z) + K_1(z)\cdot x + K_2(z)\cdot x^2 \tag{3.3}$$

Invoking the two boundary conditions at the central nanowire axis (x=0) and oxide/semiconductor interface (x=$\pm W/2$),

$$\left.\frac{\mathrm{d}\phi(x,z)}{\mathrm{d}x}\right|_{x=0} = 0 \tag{3.4}$$

$$\left.\frac{\mathrm{d}\phi(x,z)}{\mathrm{d}x}\right|_{x=\pm W/2} = \frac{C_{\mathrm{ox}}}{4W\epsilon_{\mathrm{s}}}(V_{\mathrm{G}} - V_{\mathrm{fb}} - \phi_{\mathrm{s}}(z)) \tag{3.5}$$

The generalized potential profile is then expressed in terms of surface potential as,

$$\phi(x,z)=\phi_{\mathrm{s}}(z)-\frac{C_{\mathrm{ox}}}{4W\epsilon_{\mathrm{s}}}(V_{\mathrm{G}}-V_{\mathrm{fb}}-\phi_{\mathrm{s}}(z))\left(x+\frac{W}{2}\right)+\frac{C_{\mathrm{ox}}}{4W^2\epsilon_{\mathrm{s}}}(V_{\mathrm{G}}-V_{\mathrm{fb}}-\phi_{\mathrm{s}}(z))\left(x+\frac{W}{2}\right)^2 \tag{3.6}$$

The potential at the center plane of the channel (ϕ_0) is obtained by evaluating equation (3.6) at x=0.

$$\phi_0(z)=\phi_{\mathrm{s}}(z)-\frac{C_{\mathrm{ox}}}{16\epsilon_{\mathrm{s}}}(V_{\mathrm{G}}-V_{\mathrm{fb}}-\phi_{\mathrm{s}}(z)) \tag{3.7}$$

The potential profile $\phi(x,z)$ can now be expressed in terms of $\phi_0(z)$. The resulting expression is substituted in the 2-D Poisson's equation of potential. We can formulate the differential equation of potential at the center plane of the channel in terms of characteristic field penetration length (λ) [117],

$$\frac{\mathrm{d}^2\phi_0(z)}{\mathrm{d}z^2}+\frac{V_{\mathrm{G}}-V_{\mathrm{fb}}-\phi_0(z)}{\lambda^2}=\frac{qN_{\mathrm{A}}}{\epsilon_{\mathrm{s}}} \tag{3.8}$$

where the characteristic natural length of the symmetric GAA MOSFET is defined as [5] (Appendix A.3),

$$\lambda=\sqrt{\frac{\epsilon_{\mathrm{s}}Wt_{\mathrm{ox}}}{4\epsilon_{\mathrm{ox}}}\left(1+\frac{\epsilon_{\mathrm{ox}}W}{4\epsilon_{\mathrm{s}}t_{\mathrm{ox}}}\right)} \tag{3.9}$$

Here, the natural length of the GAA MOSFET has been derived from parabolic potential model which was proposed by Suzuki *et al.* [116] and Auth *et al.* [118], and further corroborated by [117, 119, 120]. Applying boundary conditions $\phi_0(0)=V_{\mathrm{bi}}$ at source end and $\phi_0(L)=V_{\mathrm{bi}}+V_{\mathrm{DS}}$ at drain end, (3.8) is solved to obtain,

$$\phi_{0,\mathrm{min}}=\frac{A\sinh\left(\frac{L-z_{\mathrm{min}}}{\lambda}\right)+B\sinh\left(\frac{z_{\mathrm{min}}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}+V_{\mathrm{SL}} \tag{3.10}$$

where the point of minimum potential is given by,

$$z_{\mathrm{min}}=\frac{\lambda}{2}\ln\left(\frac{A\mathrm{e}^{\frac{L}{\lambda}}-B}{B-A\mathrm{e}^{-\frac{L}{\lambda}}}\right) \tag{3.11}$$

Here, built-in potential $V_{\mathrm{bi}} = \phi_{\mathrm{t}} \ln\left(N_{\mathrm{D}} N_{\mathrm{A}} / n_{\mathrm{i}}^{2}\right)$ depends on the concentration of heavily doped source/drain region N_{D},

$$A = V_{\mathrm{bi}} - V_{\mathrm{SL}} \tag{3.12}$$

$$B = V_{\mathrm{bi}} - V_{\mathrm{SL}} + V_{\mathrm{DS}} \tag{3.13}$$

$$V_{\mathrm{SL}} = V_{\mathrm{G}} - V_{\mathrm{fb}} - \frac{q N_{\mathrm{A}}}{\epsilon_{\mathrm{s}}} \lambda^{2} \tag{3.14}$$

It is to be noted that (3.11) is valid in subthreshold region only. Hence, to determine $z_{\min}$, the gate voltage is limited to threshold voltage.

At low V_{DS}, the approximation $A \approx B$ leads to $z_{\min} = L/2$ and facilitates the determination of threshold voltage for short channel GAA transistors ($V_{\mathrm{th,SC}}$) given by,

$$V_{\mathrm{th,SC}} = V_{\mathrm{T}} - \phi_{\mathrm{min,th}} \tag{3.15}$$

where V_{T} is the threshold voltage of long channel GAA MOSFET obtained from the double derivative method in section (2.3) and $\phi_{\mathrm{min,th}}$ is the threshold voltage roll-off due to scaling of gate length, evaluated by considering $\phi_{\mathrm{min,th}}$ as the difference between the long channel minimum potential and the shift in minimum potential induced by SCE [119],

$$\phi_{\mathrm{min,th}} = \frac{2 V_{\mathrm{SL}} \sinh\left(\frac{L}{2\lambda}\right)}{2 \sinh\left(\frac{L}{2\lambda}\right) + \sinh\left(\frac{L}{\lambda}\right)} \tag{3.16}$$

The difference between (3.10) and (3.14) provides the change in minimum potential barrier $\Delta\phi_{\min}$ necessary for SCE correction in core transport model (3.1).

$$\Delta\phi_{\min} = \phi_{0,\min} - V_{\mathrm{SL}} \tag{3.17}$$

3.2 Velocity Saturation

The drain saturation voltage of long channel devices $V_{\mathrm{GT}} = V_{\mathrm{GS}} - V_{\mathrm{T}}$ is no longer followed by short channel transistors due to velocity saturation. An empirical relation, derived from numerous simulations for channel length lower than 300nm, models the

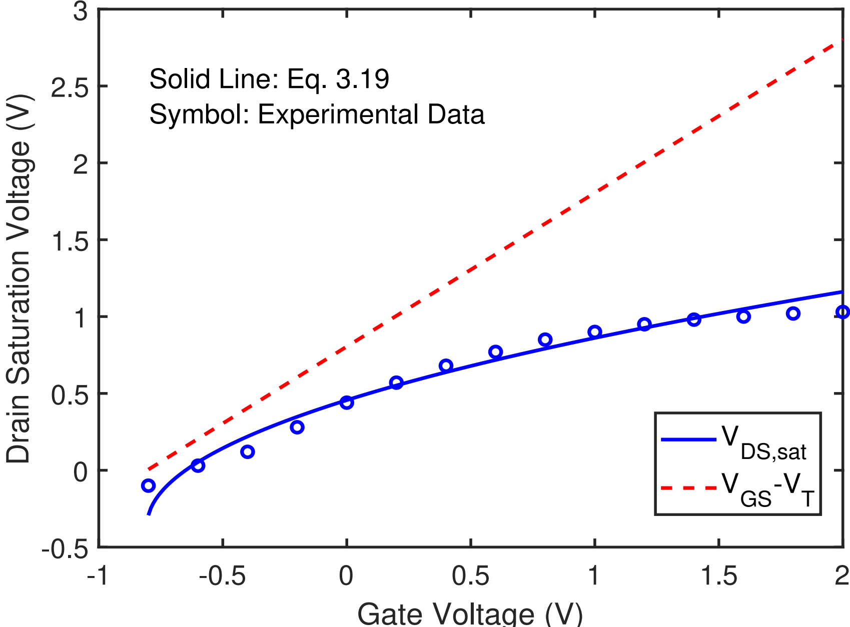


Figure 3.2: **Early saturation of drain voltage in short channel operation.** The hashed line shows the saturation voltage of a long channel MOSFET given by $\mathrm{V_{GS} - V_T}$. The symbols denote that of a short channel MOSFET. The use of equation (3.19) gradually limits the drain saturation voltage, denoting that mobile carriers reach saturation velocity before the expected drain voltage. Experimental data has been extracted from [60].

drain saturation voltage as [114],

$$V_{\mathrm{DS,sat(SC)}} = -0.36 + \eta (L v_{\mathrm{sat}})^{\frac{1}{3}} V_{\mathrm{GT}}^{\frac{1}{2}} \tag{3.18}$$

where, η is an adjusting parameter and v_{sat} is the saturation velocity. The drain saturation voltage $V_{\mathrm{DS,sat(SC)}}$ is gradually limited from its long channel counterpart by the relation,

$$V_{\mathrm{DS,sat}} = \frac{1}{2} V_{\mathrm{DS,sat(SC)}} \left(1 + \tanh\left(3V_{\mathrm{GT}}\right)\right) + \frac{1}{2} V_{\mathrm{GT}} \left(1 - \tanh\left(3V_{\mathrm{GT}}\right)\right) \tag{3.19}$$

Figure 3.2 shows how equation (3.19) models the early saturation of drain voltage in a short channel device in comparison to long channel MOSFET. This effect is due to the higher lateral electric field, responsible for accelerating the mobile carriers, which reach the saturation velocity before the expected saturation drain voltage, leading the drain current to saturate at lower values of $\mathrm{V_{DS}}$.

An effective drain voltage is used in the core model where the drain voltage from

the terminal is restricted to drain saturation voltage by the continuous expression,

$$V_{\mathrm{DS,eff}} = V_{\mathrm{DS,sat}} \frac{1 - \ln\left(\mathrm{e}^{A_1\left(1-\frac{V_{\mathrm{DS}}}{V_{\mathrm{DS,sat}}}\right)} + 1\right)}{\ln\left(\mathrm{e}^{A_1} + 1\right)} \tag{3.20}$$

where A_1 controls the degree of smoothness and is set to '8' in this work.

3.3 Mobility Degradation

In a short channel gate-all-around MOSFET, mobility of the channel carriers are affected by several mechanisms such as surface roughness, phonon scattering and internal collision between the carriers. The degradation of mobility in the active region, resulting from high lateral field due to proximity of drain terminal to source end and surface scattering induced by vertical electric field, is incorporated into the transport model by the effective mobility expression given by,

$$\mu_{\mathrm{eff}} = \frac{\mu_1}{\left[1 + \left(\frac{\mu_1 V_{\mathrm{DS,eff}}}{v_{\mathrm{sat}} L}\right)^{\sigma}\right]^{\frac{1}{\sigma}}} \tag{3.21}$$

Here, σ is a constant parameter which takes into account the carrier-carrier scattering in the channel region arising from the high lateral field and μ_1 is the vertical field mobility degradation expressed in terms of low field mobility μ_0 and mobility degradation coefficient θ as,

$$\mu_1 = \frac{\mu_0}{1 + \frac{1}{2}\theta(V_{\mathrm{GS}} - V_{\mathrm{th,SC}})[1 + \tanh\left(A_1(V_{\mathrm{GS}} - V_{\mathrm{th,SC}})\right)]} \tag{3.22}$$

The mobility degradation coefficient θ is calibrated with experimental reports [60] such that contributions from surface scattering are incorporated into the model. Consequently, corner effect in the GAA structure becomes strong at high overdrive voltage. The hyperbolic tangent factor in the denominator of (3.22) brings about this degradation at high gate field, thus mitigating the complexity of the numerical simulation.

3.4 Channel Length Modulation

As drain voltage exceeds saturation voltage, the short channel device suffers from reduced L due to extension of drain-channel depletion region. For $V_{\mathrm{DS}} > V_{\mathrm{DS,sat}}$, the effective channel length then follows [119],

$$L_{\mathrm{eff}} = L - \sqrt{\frac{\kappa \epsilon_{\mathrm{s}} \beta}{q N_{\mathrm{A}}} \left(1 + \tanh\left(10\beta\right)\right)} \tag{3.23}$$

where κ is a fitting parameter and $\beta = V_{\mathrm{DS}} - V_{\mathrm{DS,sat}}$.

3.5 Parasitic Resistance

The reduction of drain current in the saturation regime is attributed to the presence of parasitic resistance causing voltage drop between gate-source and drain-source region. The total resistance can then be expressed in terms of channel resistance R_{ch} and parasitic resistance $R_{\mathrm{S}}(R_{\mathrm{D}})$ at source(drain) end as [121],

$$R_{\mathrm{T}} = R_{\mathrm{ch}} + R_{\mathrm{S}} + R_{\mathrm{D}} = \frac{V_{\mathrm{DS,eff}}}{I'_{\mathrm{D}}} \tag{3.24}$$

Taking (3.1) to be the drain current without parasitic resistance and using $R_{\mathrm{ch}} = V_{\mathrm{DS,eff}}/I_{\mathrm{D}}$, we get the final drain current model (I'_{D}) in the form,

$$I'_{\mathrm{D}} = \left[\frac{1}{I_{\mathrm{D}}} + \frac{R_{\mathrm{S}} + R_{\mathrm{D}}}{V_{\mathrm{DS,eff}}}\right]^{-1} \tag{3.25}$$

Table 3.1 lists some of the transport model parameters used to calibrate the model with published experimental reports which account for velocity saturation, mobility degradation, channel length modulation and series resistance.

Table 3.1: Relevant parameters used in the transport model.

Parameter Description (unit)	**Value**
Parasitic source (drain) resistance (kΩ)	$0.5 - 5$
Saturation velocity (10^5 m/s)	2
Low field electron mobility (cm^2/Vs)	903
Mobility degradation parameter, σ	1.5
Mobility degradation coefficient, θ	15
Velocity saturation parameter, η	4.14
Channel length modulation parameter, κ	1×10^{-5}

Chapter 4

Simulation Model Development

Simulation can reduce the testing time drastically along with reduction of cost involved with the fabrication process of the device. As a result, use of different simulator for investigation of semiconductor devices has become ubiquitous. In this thesis, Technology Computer-Aided Design (TCAD) Sentaurus Device from Synopsis tools have been used to verify the scaling trends of gate-all-around MOSFET with process parameters. On the one hand, the simulation results help to seek explanation of the reported experimental results, on the other hand, to deepen our understanding of the various underlying physics responsible for short channel operation of GAA MOSFET, TCAD simulation corroborates the results determined from the analytical formulation. Instead of focusing on the details on numerical simulation techniques for GAA MOSFET, this work will use numerical tool in an effective way to validate the results obtained from proposed analytical model.

4.1 Sentaurus Device

The complexity of semiconductor process and device physics increases dramatically in the advance technology. It is difficult to perform essential first principle analysis on semiconductor device, however, further compact device modeling needs physics driven modeling result. The technology computer aided design (TCAD) becomes an effective solution as it takes the advantages of powerful numerical computing resource on solv-

ing the complex device physics equations, also its physical approach provides excellent accuracy from its modeling simulation. In the industry, TCAD is widely used as fast turnover and low cost solution for semiconductor technology research and development.

TCAD includes two major branches, process simulation and device simulation [122]:

- In TCAD process simulation, the fabrication steps, such as deposition, etching, implantation and annealing, are simulated based on process physics equations. Multi-dimensional device structure can be built by defining complete process step commands. Physical parameters from the device fabrication process can be extracted for further optimization usage. Also external calibration data can be imported to make process simulation to be more comparative to the real process.

- Device simulation characterizes the device virtually in TCAD environment. Device used in simulation has to be a meshed, finite element based structure. Based on the given device structure, plus proper boundary condition definition, device physics model definition and numerical simulation parameter plugin, a TCAD device simulation is modeled. The basic result extracted from device simulation is the electric representations, such as current, voltage, charge and field. Furthermore, the result related to device physics can also be extracted, such as trap concentration, impact ionization generation and band structure. Multiple simulation modes, such as static, transient and AC, are supported in commercial TCAD environment. Also various device physics models are provided in TCAD for essential study.

Details on the TCAD simulation setup and physics theories related to simulation modeling in this work are going to be briefly discussed in the subsequent sections.

4.2 Structure Creation

The simulated nanowire structure is the same as in the previous chapter, namely the InGaAs nanowire MOSFET experimentally demonstrated by Gu *et al.* [60]. The first

step includes the realistic modeling of the physical device with the Sentaurus Device Editor (SDE) included in the TCAD framework.

Sentaurus Device has a two dimensional (2D) and a three dimensional (3D) device editor with graphical users interface (GUI). The full 3D option was utilized since the aim of this work is to simulate transistors with multi-dimensional gates (GAA structures).

The general modeling procedure can be summarized as follows:

- Create device geometry and assign material properties.
- Generate contact regions.
- Define doping profile.
- Define discretization rules for the mesh.
- Create device mesh.

The device geometry definition in step (1) can be either manually user-specified or automatically generated from a process emulation step. Process emulation implies that the entire physical process is not simulated (for this another tool of the TCAD framework is available, Sentaurus Process) but merely emulated. For example, the emulation of an etching process is performed by simply specifying the etch depth rather than simulating the physical etching rate.

The device geometry is manually defined out of 3D primitives: cuboids and cylinders. In GAA architecture, the lateral nanowires can be fabricated either by top-down approach or bottom-up, where the active channel region are suspended by etching the surrounding oxide layer, segregating the channel from the substrate. Therefore in simulation process, a GAA MOSFET does not require any supporting substrate material for successful compilation. Two large cuboids are defined in concentric formation, where the inner layer is the active InGaAs channel with the outer layer as gate dielectric. This is configured by setting the overlap behavior: 'new overlaps old' so that from the concentric cuboids we obtain a nanowire with square cross-section surrounded by the

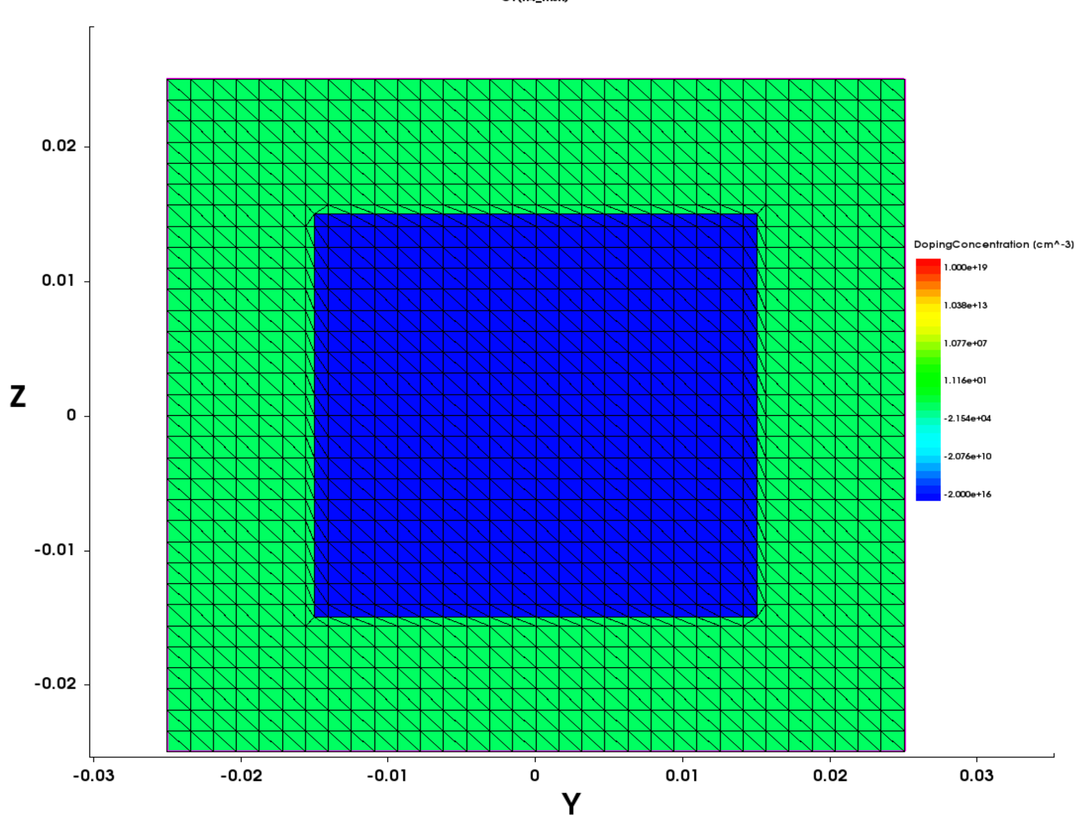


Figure 4.1: **Cross-section of the InGaAs GAA MOSFET.** The gate oxide wraps around the active InGaAs channel in concentric formation. The fin width is 30 nm and the gate oxide 10 nm on all sides.

gate dielectric. By carefully applying Boolean operations to these primitives the gate-all-around structure was constructed. The dimension of the outer cuboid was chosen such that the oxide thickness is initially 10 nm from all directions as shown in Figure 4.1.

Sentaurus Device Editor has a huge material database with all the common semiconductors, oxides and insulators which can be assigned to a geometrical primitive by simply clicking on them. However the user has the option to define its own material files and to link them (call by reference) with existing shapes via a parameter file. This offers the great advantage of changing material parameters (value of saturated velocity, maximum field corresponding to this velocity and so on) without having to rebuild the mesh. This feature was exploited to explore different suitable high-κ dielectrics over InGaAs. The following line shows the syntax for defining the cuboid of the rectangular channel region with (x_1, y_1, z_1) and (x_2, y_2, z_2) as the coordinate of the opposite two diagonal end-points in the cuboid.

(sde:set-default-material "InGaAs")
(sdegeo:create-cuboid (position $x_1\, y_1\, z_1$) (position $x_2\, y_2\, z_2$) "InGaAs" "channel")

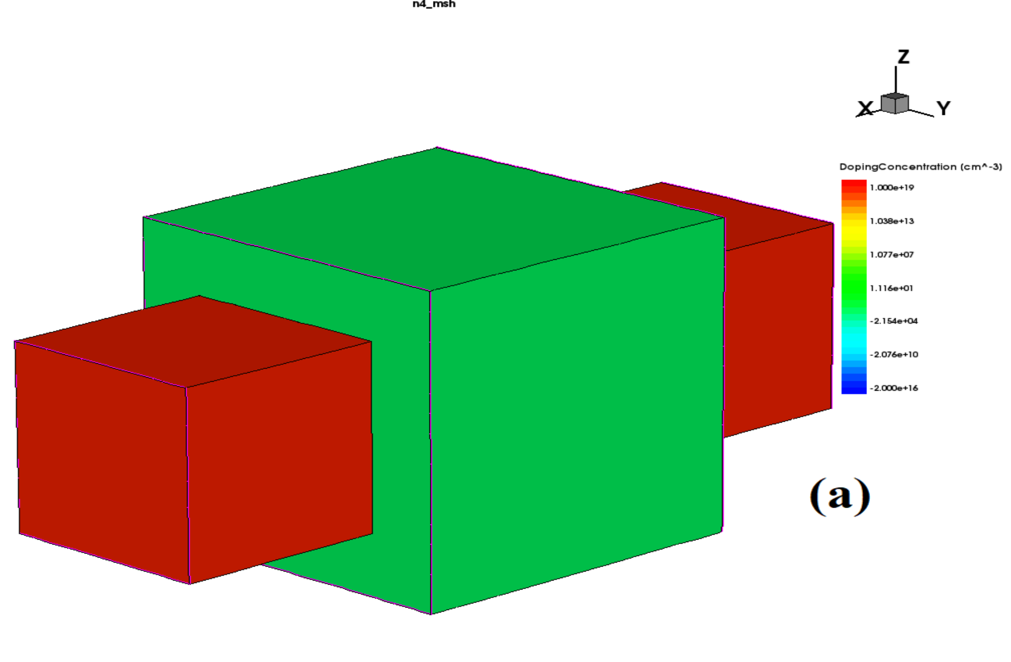
In a similar fashion by selecting different oxides as material, the outer insulator layer under the gate metal can be defined.

The next step includes creating the contacts: source, drain and wrap-around gate metal. Different types of contact (electrodes, thermodes) can be selected; for the source/drain, a constant high n-doping of $1{\times}10^{19}$ cm^{-3} was chosen to ensure ohmic contacts with series resistance set for emulating the parasitic and contact counterparts as illustrated in the code snippet below:

(sdegeo:define-contact-set "S" 4 (color:rgb 0 0 1) "##")
(sdegeo:set-current-contact-set "S")
(sdegeo:define-3d-contact (list (car (find-face-id (position ($x_3\, y_3\, z_3$))))) "S"))
(sdedr:define-constant-profile "ConstantProfileDefinitionName" "PhosphorusActiveConcentration" Nd-sd)
(sdedr:define-constant-profile-region "ConstantProfilePlacementName" "ConstantProfileDefinitionName" "source")

Here (x_3, y_3, z_3) is a point on the plane of the contacts. Doping InGaAs with a group V element (Phosphorus) results into n-doping, as for the channel, group III element (Boron) is used to accomplish p-doping. The channel doping was kept p-type with a constant value of $2{\times}10^{16}$ cm^{-3} for a lightly doped channel region. The gate contact was kept Schottky type be setting the gate work function to 4.6 eV, in coherent with the low work function tungsten nitride.

All the preceding steps described above are carried out in the Sentaurus Device Editor module. Figure 4.2(a) shows the completed structure of the GAA device after creation in SDE. The mesh specification was made finer near the oxide-semiconductor interface and near source/drain region to realize the impact of trap charges and mo-



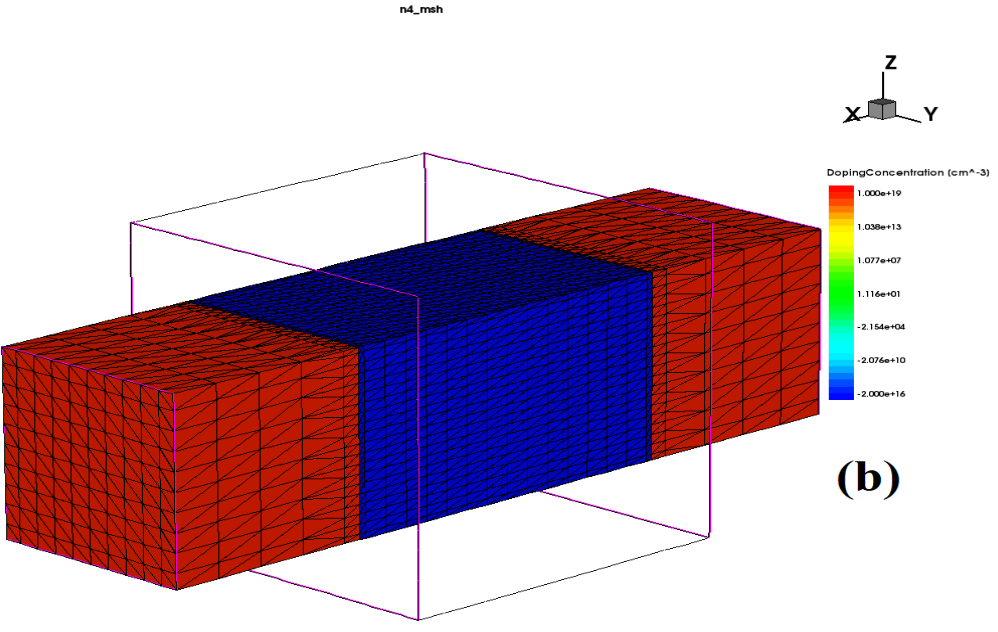


Figure 4.2: **Completed structure of the GAA MOSFET created in Sentaurus Device Editor.** (a) Schematic showing source/drain region with the wrap-around gate. (b) Schematic without the wrap-around gate, revealing the doping profile and mesh throughout the entire channel. It can be seen that dense mesh are formed near the oxide-semiconductor interface and near source/drain region to realize important physical effects in the active channel.

bility degradation in the electrostatic and transport simulation as depicted in Figure 4.2(b). From this figure it can be seen that dense mesh are formed near the region of interest which can be defined by the following code snippet.

(sdedr:define-refinement-size "channel-refinement" $x_{max}\, y_{max}\, z_{max}\, x_{min}\, y_{min}\, z_{min}$*)*

where $(x_{max}\, y_{max}\, z_{max})$ and $(x_{min}\, y_{min}\, z_{min})$ are the maximum and minimum spacing limits in the respective direction.

4.2.1 Mesh Generation

After having defined the device geometry and doping profiles, the discretization step follows as will be described below. Since the system of partially differential equations that defines charge transport in our device (Partial Differential Equations) is using continuous quantities but our mesh is now made out of a discrete number of nodes, we have to discretize the PDEs as well. The method of choice is the box method also known as finite volumes method [123]. A typical differential equation of the form.

$$\nabla \cdot J + R = 0 \tag{4.1}$$

gets transformed, by applying the Gaussian theorem over a test volume and discretizing the resulting expression, into:

$$\sum_{j \neq i} k_{ij} \cdot j_{ij} + \mu(\Omega_i) \cdot r_i = 0 \tag{4.2}$$

In Table 4.1 the coefficients and measures for 1D, 2D and 3D case are specified, whereas Table 4.2 shows the discretized Poisson together with the hole and electron continuity equations.

One of the four Maxwell's equations, that ensures charge conservation, is Gauss law.

Table 4.1: Box method coefficients for 1,2 and 3-D discretization.

Dimension	k_{ij}	$\mu(\Omega_i)$
1D	$1/\mathrm{l}_{ij}$	Box length
2D	d_{ij}/l_{ij}	Box area
3D	D_{ij}/l_{ij}	Box volume

Table 4.2: Numerical approximation of the coupled differential equations, solved in each vertex of the mesh.

Equation	j_{ij}	r_i
Poisson	$\epsilon(\mu_i - \mu_j)$	$-\rho_i$
Electron continuity	$\mu^n(n_i B(\mu_i - \mu_j) - n_j B\mu_j - \mu_i)$	$R_i - G_i + \frac{d}{dt}n_i$
Hole continuity	$\mu^p(p_i B(\mu_i - \mu_j) - p_j B\mu_j - \mu_i)$	$R_i - G_i + \frac{d}{dt}p_i$

In its integral form it states the electric flux through a closed surface of a test volume equals the electric charge inside the volume times $1/\epsilon$. In the finite volume method the Gaussian theorem is the prescription applied over the test volumes to unite them, which makes it the natural method of choice for discretizing semiconductor devices. In fact other methods like finite elements have major problems when ensuring charge conservation over a discretized simulation volume.

In Table 4.1 and Table 4.2 shows all the prescriptions to discretize the PDE, the only open issue remaining is the choice of the box method coefficients, k_{ij}. In order to obtain the k_{ij}, a special type of mesh needs to be build, a so called Delaunay mesh [123]. A simple definition of a Delaunay mesh states that the circumsphere of each mesh element cannot contain any other mesh vertices. This definition is illustrated in Figure 4.3.

4.2.2 Simulation Flow

Sentaurus TCAD is a complete simulation framework consisting of a large number of individual programs or tools. Figure 4.4 presents the complete simulation flow diagram where the names of the different tools are also given. After the mesh is generated Sentaurus Device Editor creates an output file with **.tdr** extension. This file contains

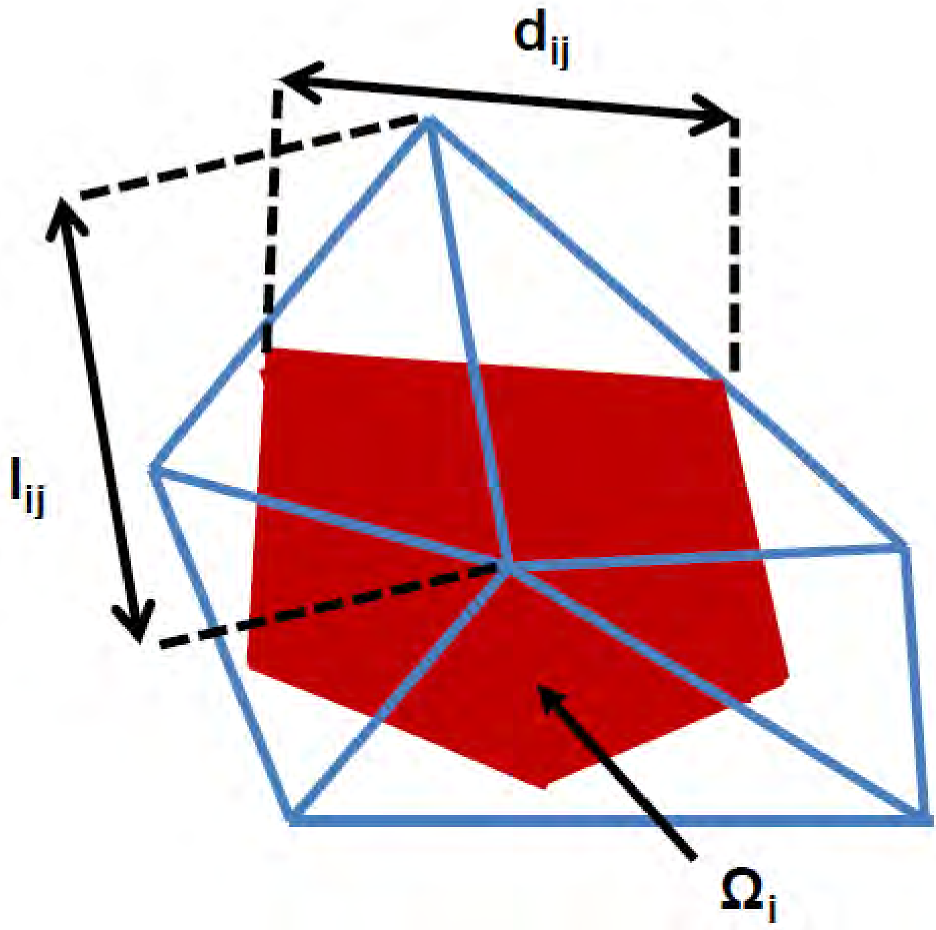


Figure 4.3: **Illustration of a 2D triangular mesh over a control area W (red) using the box method.** Figure redrawn from [122].

both the discretized geometry and the doping profiles and will serve as input to the actual device simulator.

4.3 Script for SDevice

Sentaurus Device is the core of the TCAD framework, containing a multidimensional (1D, 2D and 3D) electrical, thermal and optical simulator . It has no graphical user interface therefore the entire simulation is controlled by a command/script file employing a pseudo-programming language run by the SDevice module which is very well documented in the users guide [122]. It is made out of six (or eight) sections delimited by brackets and containing specific keywords. The simulator is not case sensitive and the

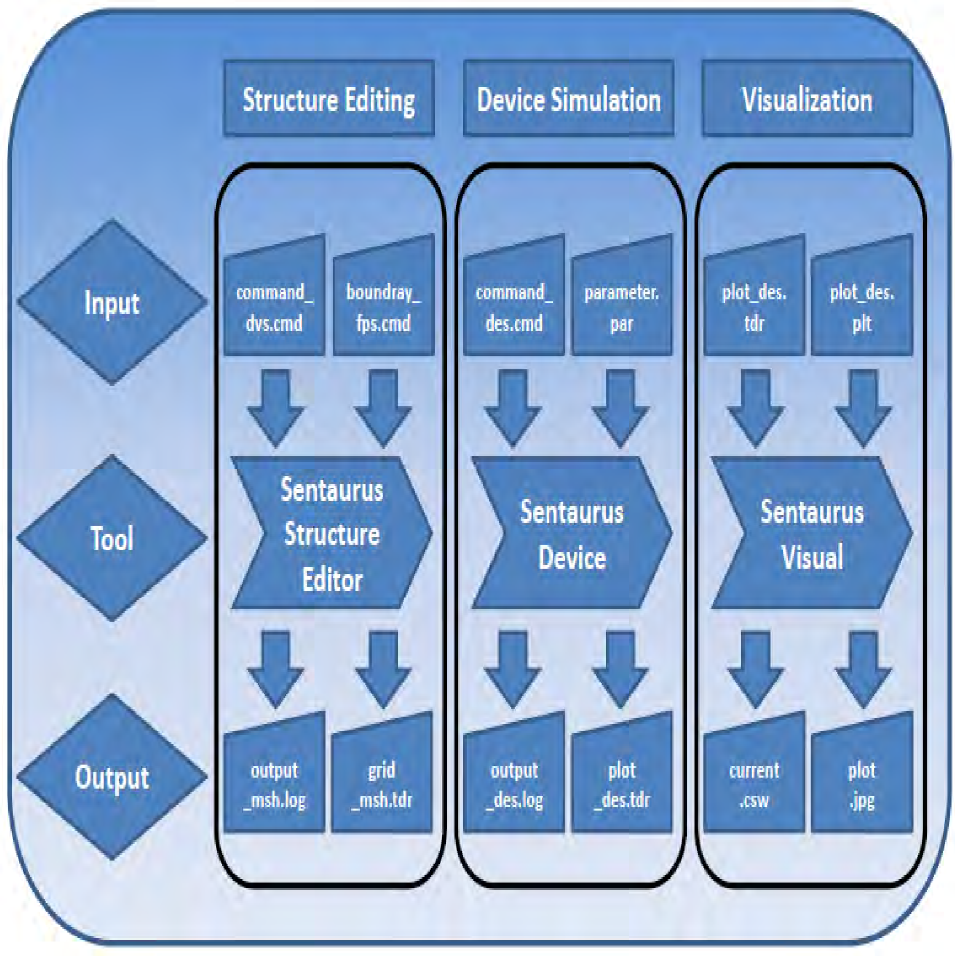


Figure 4.4: **Typical simulation flow diagram of Sentaurus Device, starting from the structure editing, device simulation and visualization of the simulation output.** [124]

sections can be arranged in an arbitrary order but it is syntax sensitive (use of parentheses must be consistent, variables must be declared between quotation marks, etc.). This section will briefly describe each of the six sections (eight in the case of Mixed Mode simulation) and explain what they contain for the specific case of a nanowire simulation.

4.3.1 The File Section

The input and output files of the simulation are defined here. As input we have the previously generated mesh file and optionally the parameter file with the user-defined materials. The output files are of three sorts: plots were current-voltage $(I - V)$ or

capacitance-voltage ($C - V$) curves are stored, spatially resolved maps of flux quantities or vector fields (electric field inside the device) and finally log files where all the relevant information of the simulation flow are stored.

4.3.2 The Electrode Section

The contact details are provided in this section. In the default case perfect Ohmic contacts are assumed but also Schottky contacts or tunneling barriers can be declared. The very high doping in source/drain end of the channel ensures ohmic contacts where additional series resistance are added to capture the influence of parasitic resistance. The gate contact is declared as Schottky type by specifying the gate metal work function to 4.6 eV as shown below.

Electrode{
name="D" voltage=0 Resist=500
name="S" voltage=0 Resist=500
name="G" voltage=0 workfunction=4.6
}

4.3.3 The Physics Section

The physics section is the most important section of the simulation file and it can be either global, material specific, region specific or region interface-specific. Here all the physical models relevant for the accurate simulation of the device are specified.

By default, drift-diffusion model is incorporated in the global physics section. Electron and hole densities can be computed from the electron and hole quasi-Fermi potentials using either Boltzmann statistics or Fermi statistics using the formula:

$$n = N_{\mathrm{C}} \exp\left(\frac{E_{\mathrm{F},n} - E_{\mathrm{C}}}{kT}\right) \tag{4.3}$$

$$p = N_{\mathrm{V}} \exp\left(\frac{E_{\mathrm{V}} - E_{\mathrm{F},p}}{kT}\right) \tag{4.4}$$

where $N_{\mathrm{C,V}}$ are the effective density-of-states, $E_{\mathrm{F},n(p)}$ is the quasi fermi energy for electron (hole), $E_{\mathrm{C(V)}}$ is the conduction (valence) band edges defined as,

$$E_{\mathrm{C}} = -\chi - q(\phi - \phi_{\mathrm{ref}}) \tag{4.5}$$

$$E_{\mathrm{V}} = -\chi - E_{\mathrm{g,eff}} - q(\phi - \phi_{\mathrm{ref}}) \tag{4.6}$$

here, χ denotes the electron affinity, $E_{\mathrm{g,eff}}$ is the effective band gap and ϕ_{ref} is a constant reference potential. For Fermi statistics both equation (4.3) and (4.4) are multiplied by the Fermi integral of order 1/2, $F_{1/2}$.

The gate-all-around device suffers from various mobility degradation mechanisms such as scattering at the interface from surface roughness and surface phonon, carrier-carrier scattering which stems from the doping within the channel region. In order to emulate the different degradation schemes, Sentaurus Device has various mobility models.

Initially the bulk mobility is computed using the Arora model proposed by [125] that takes into account the doping concentration of the InGaAs channel. To capture the degradation of mobility at the interface, Sentaurus Device TCAD calculates the electric field perpendicular to the oxide-semiconductor interface using the Lombardi Model [126] which determines the surface contribution due to acoustic phonon scattering and the contribution attributed to surface roughness separately. These components of mobility are combined with the bulk mobility by Matthiessen's rule given as,

$$\frac{1}{\mu_{\mathrm{comb}}} = \frac{1}{\mu_{\mathrm{b}}} + \frac{1}{\mu_{\mathrm{ac}}} + \frac{1}{\mu_{\mathrm{sr}}} \tag{4.7}$$

here, μ_{b}, μ_{ac} and μ_{sr} are bulk mobility, contributions to mobility from acoustic phonon scattering and surface roughness respectively. Carrier-carrier scattering is supported by the model based on Choo [127] and Fletcher [128] which accompanies the Conwell-Weisskopf [122] screening theory. This is combined with the mobility contributions from other mobility degradation models (μ_{comb}) according to Matthiessen's rule, where the carrier-carrier contribution to the overall mobility degradation is captured in the

μ_{eh} term.

$$\frac{1}{\mu} = \frac{1}{\mu_{\mathrm{comb}}} + \frac{1}{\mu_{\mathrm{eh}}} \tag{4.8}$$

The velocity saturation model is adopted for InGaAs in transport simulation under drift-diffusion formalism, where the velocity of the carriers are saturated upon reaching a certain v_{sat} level given in Table 3.1.

Generation-recombination processes account for exchange of carriers between the conduction and valence band. They are very important for device physics, as such, these were implemented during device simulation. Recombination through deep defect levels in the bandgap is usually labeled Shockley-Read-Hall (SRH) recombination. For the sake of simulation, the lifetimes of the SRH recombination model used by Sentaurus Device are modeled as a product of a doping-dependent factor based on the Scharfetter relation [122].

As oxide thickness, channel width and gate length are scaled towards decananometer regime, certain non-ideal effects come into play and degrade subthreshold characteristics. These effects are included by invoking the quantization model for important quantum effects. To include quantization effects in classical MOS device, a potential-like quantity $\Lambda_{\mathrm{n/p}}$ is used in the classical density formula. For the GAA MOSFET it is imperative that the quantization model is capable of capturing the quantum effects in 3D. The density gradient model is used for computation of the potential-like quantity for its numerical robustness compared to other quantization models in 2D or 3D. As a result, any impact on threshold voltage or subthreshold swing arising from scaling of physical parameters are accounted for in the 3D numerical simulation.

It is well known that quantum-confinement effects begin to appear when the cross-section dimension of the gate-all-around MOSFET becomes less than 10 nm [129, 130]. Our proposed model uses semi-classical drift-diffusion formalism to compute drain current complemented with several non-ideal effects. Due to the semi-classical nature of the transport equations, the scaling limits have been restricted from reaching decananometer regime, thus alleviating the use of quantization effects in the analytical model. Nevertheless, in Sentaurus Device TCAD, in addition to solving Poisson equa-

tion for carrier transport under drift-diffusion model to evaluate current densities, quantization model was incorporated to capture the 3D quantum effects, if any, in the gate-all-around geometry. The density gradient model is numerically robust compared to other quantization models in 2D or 3D, thus this model was invoked to determine the potential-like quantity $\Lambda_{n/p}$, considering only Γ valley in InGaAs. Figure 4.5 shows that the density gradient quantization model in addendum with the fine mesh spacing used at the periphery of the device successfully captures the corner effect at the square cross-section which was predicted by [97].

In the material specific Physics section, the mole fraction of the InGaAs channel region is defined and can be varied accordingly to study the impact of changing channel material composition on electrostatics of the device.

Despite the recent advancement in atomic deposition layer techniques, significant trap charges exist in the interface and throughout the oxide. For the interface traps, donor type trap states are specified at ~ 0.27 eV below the conduction band minimum [106]. From experimental reports [112], a positive fixed oxide charge density of 9×10^{18} cm^{-3} distributed throughout the Al_2O_3 was adopted in the region interface-specific Physics section.

4.3.4 The Plot Section

A list of variables to be plotted in the output file is included here. Electron and hole quasi Fermi levels, potential, space-charge, electron and hole densities are among the most common quantities to be included.

4.3.5 The Math Section

In this section some convergence parameters can be adjusted like the minimum norm of the right hand side (RHS), the maximum relative error in each iterative or the max-

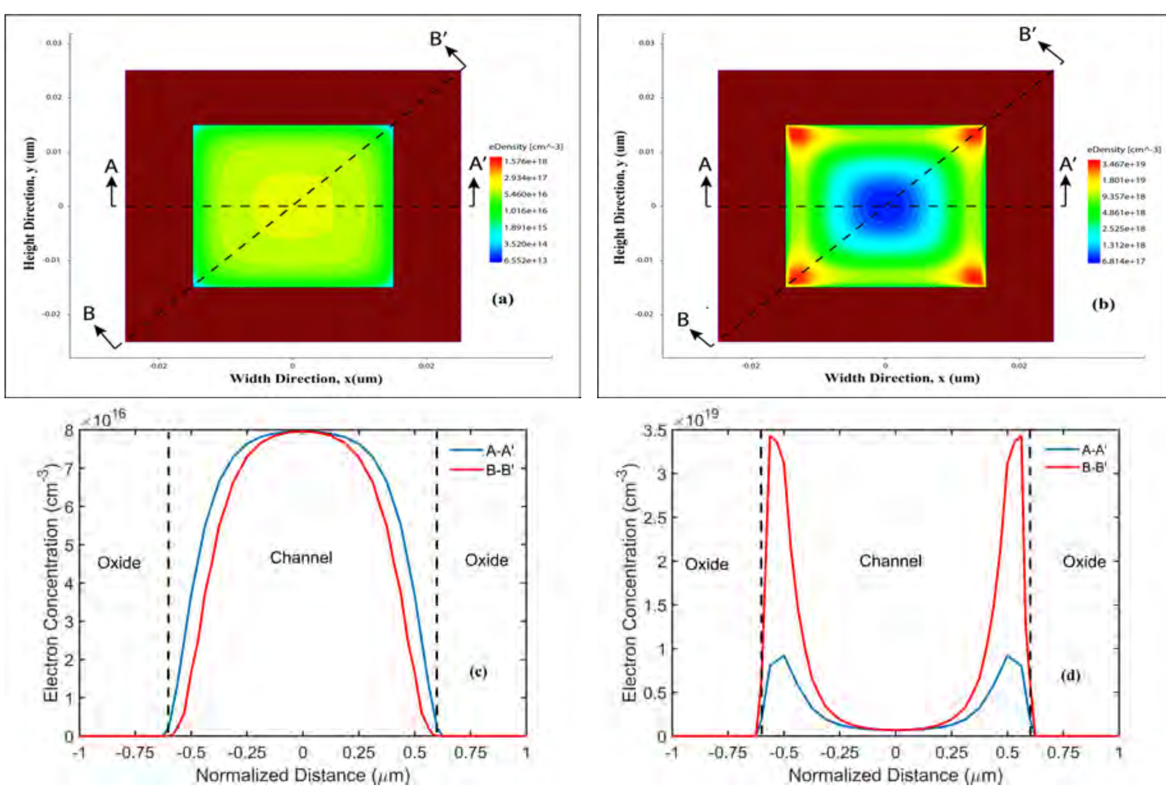


Figure 4.5: **Spatial carrier density of electrons taken at cross-section of the GAA MOSFET at mid-channel.** (a) At low gate bias near threshold region. (b) At high gate bias in strong inversion regime. (c-d) The corresponding electron density along cutlines A-A' from gate-to-gate direction and along B-B' direction diagonally. The corner effect at strong gate bias in the GAA geometry is evident from (b) and (d), showing that TCAD simulation is successful in accounting for this effect.

imum number of iterations. A deeper insight in the numerical methods and the various schemes used in the simulator can be found in [122].

4.3.6 The Solve Section

This is the second most important section after the physics section. The user can specify between various types of simulations: quasistationary, transient, small signal, harmonic balance but also optical or thermal. Each simulation type must have a goal defined; this can be either an electrode that will be ramped, the voltage of a voltage generator or the power of an optical source that will be switched on. For computation of electrostatic $C-V$ profile, the device structure was simulated at zero drain bias and the charge concentration at the mid-channel was integrated for varying gate bias. On the contrary, during carrier transport, the drain bias was ramped to a certain voltage (50 mV or 1 V) before sweeping the gate voltage to determine transfer characteristics and vice versa for output characteristics.

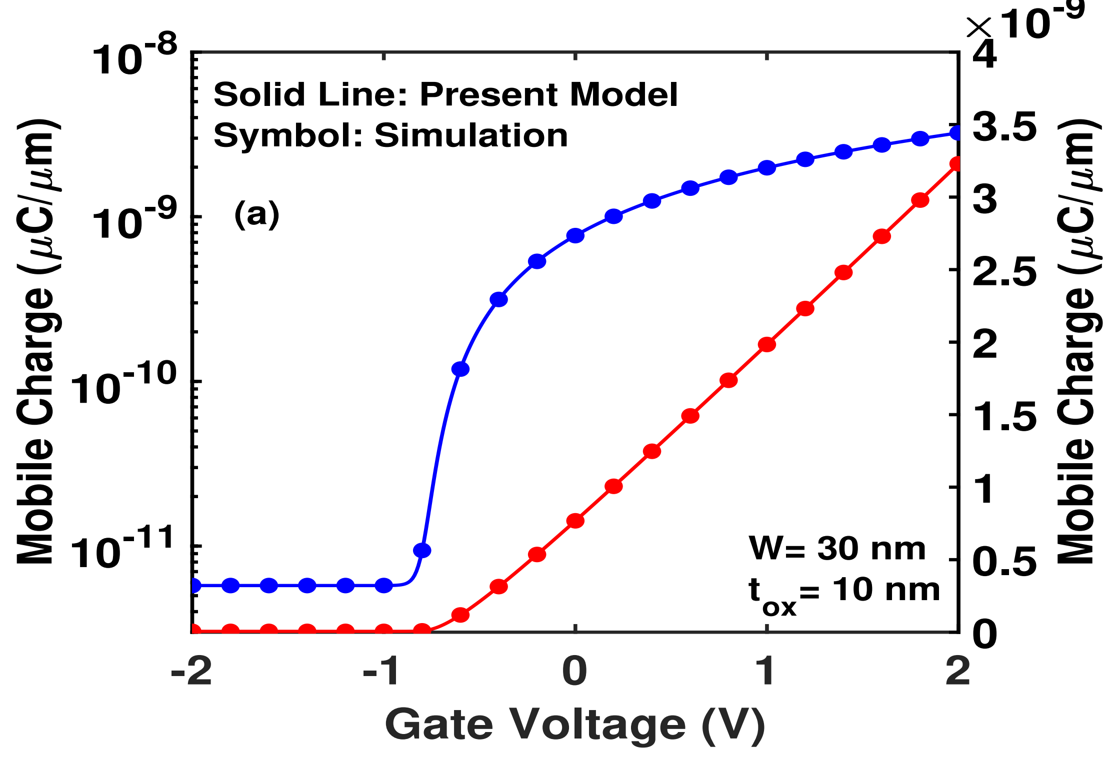
Chapter 5

Results and Discussions

In this chapter the results pertaining to the electrostatic and transport behavior are obtained from the proposed model. The transport results are validated with published experimental reports where possible. The electrostatics of the device is ensured by 3D numerical simulation in Sentaurus TCAD. Additionally, the scaling of various process parameters were studied for optimum design of scaled nanowire transistor with high-κ dielectrics demonstrating superior subthreshold and ON-state performance.

As can be seen in Figure 5.1a, the model accurately predicts the mobile charge density from below threshold to strong inversion with that of simulation extracted at mid-channel of the device. The incorporation of interface trap defect assists inversion as well as models the saturation of decrease of mobile charge below threshold. The use of equation (2.18) in determining channel charge improves the efficiency of the model with only an error of about 0.51% near threshold region as shown in Figure 5.1b.

The effect of physical parameters on the $C - V$ characteristics of a GAA MOSFET is shown in Figure 5.2. The proposed model spans from depletion to strong inversion operation, accounting for minority carrier concentration only. This is reflected in the $C - V$ profile where capacitance decreases to zero in depletion and saturates to oxide capacitance in strong inversion. As dictated by (2.13), the oxide capacitance is a function of oxide thickness as well as fin width, therefore the transistor with the thinnest t_{ox} and greatest W possess the highest saturated capacitance as portrayed in Figure 5.2. With reduction of fin width, the geometric confinement of the transistor body leads to



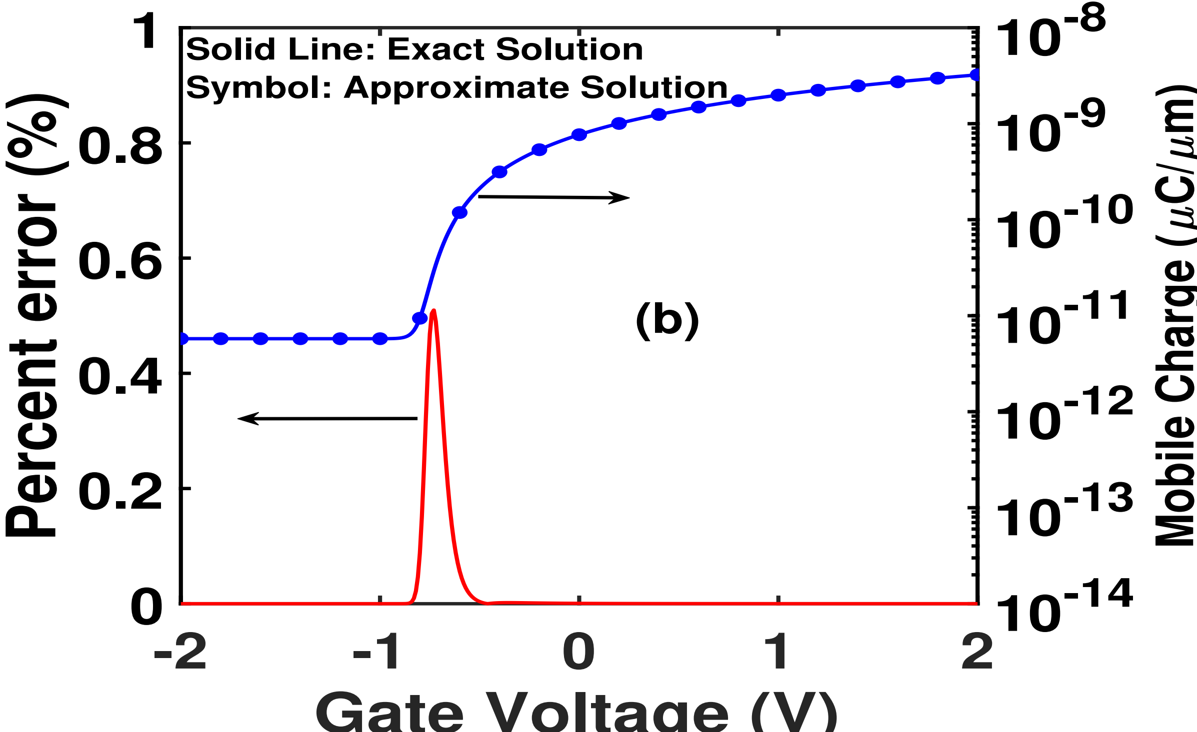


Figure 5.1: **Mobile charge density as a function of gate bias for a GAA MOSFET at $N_{\rm A} = 2 \times 10^{16}\, cm^{-3}$.** (a) Comparison between model and simulated charge density in both linear and log scale at low V_{DS}. (b) Error in charge density from using (2.18) instead of Lambert function. Largest error occurs near threshold region.

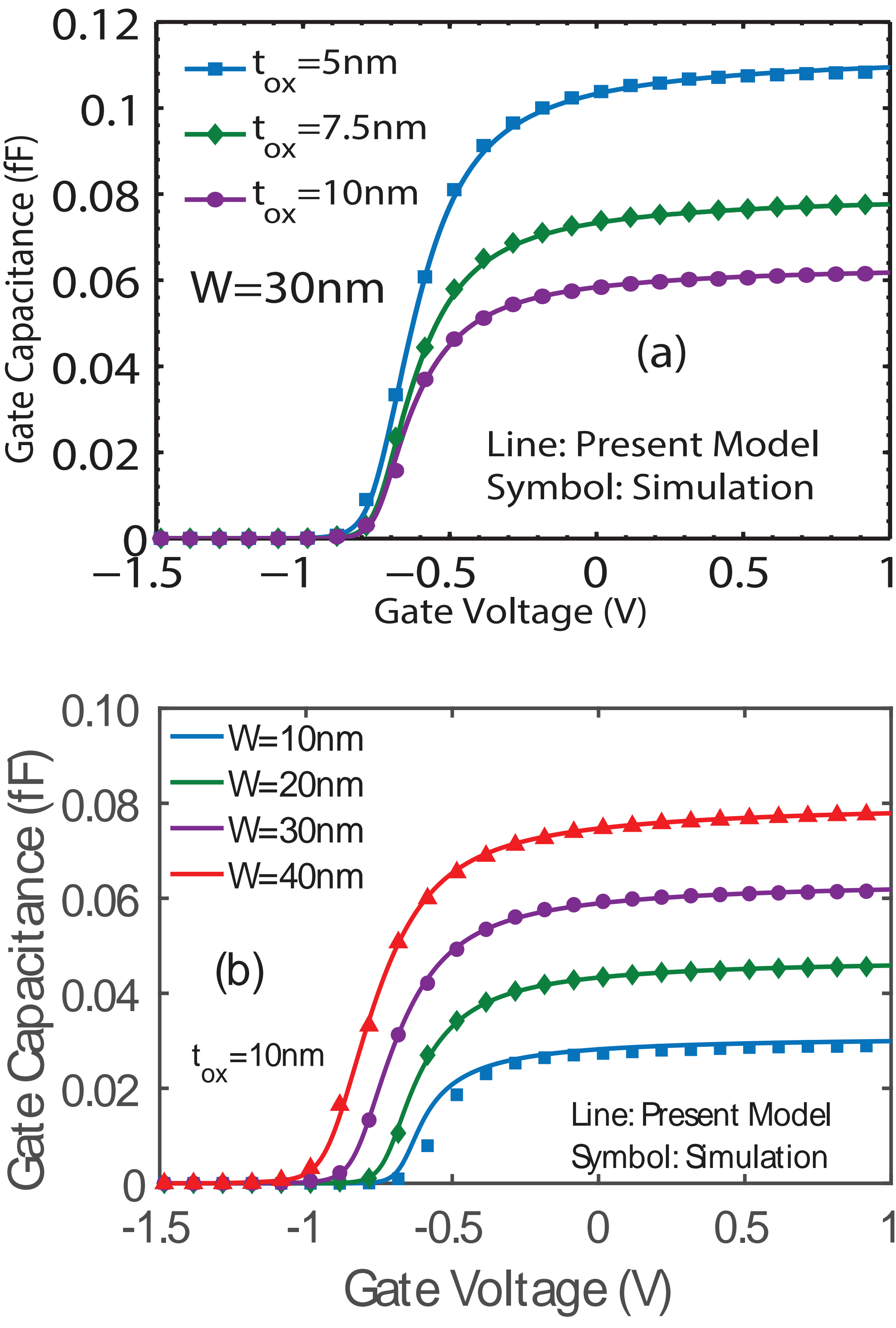


Figure 5.2: **Capacitance-voltage characteristics of a GAA nanowire MOSFET with $N_A = 2 \times 10^{16}\,\mathrm{cm}^{-3}$.** (a) For various oxide thickness. (b) For various fin width. The fin width has greater impact on $C - V$ characteristics in comparison to oxide thickness which is reflected by a shift in threshold voltage. The impact of quantum effect on CV profile is seen for a fin width of 10nm where simulation results reflect a rightward shift in CV arising from threshold voltage shift in subthreshold region and gate capacitance degradation in strong inversion region.

volume inversion, where the surface as well as the whole body is inverted [107]. This phenomenon leads to an increase in threshold voltage as shown in Figure 5.2b, indicating that gate capacitance is a strong function of fin width. The analysis of devices with fin width smaller than 10nm is restricted from the proposed model due to negligence of quantum effect. With inclusion of density gradient quantization model in TCAD, the simulation results reflect a rightward shift in the CV curve for a fin width of 10nm, indicating the impact of quantum effect in threshold voltage shift near subthreshold region and a degradation of gate capacitance in strong inversion regime.

Figure 5.3 highlights the impact of channel properties on the electrostatic behaviour of the $\mathrm{In}_{1-x}\mathrm{Ga}_x\mathrm{As}$ GAA MOSFET. For low channel doping, there is negligible effect on $C - V$ characteristics. However as channel doping increases beyond 1×10^{17} cm^{-3} the CV curve shifts right. The fin width is only a few nanometers, which conduces to full depletion of the MOSFET at moderate doping levels. For heavily doped devices, the channel may enter partial depletion, requiring a greater gate bias to create the inverted channel. Variation of Ga-mole fraction influences the bandgap of $\mathrm{In}_{1-x}\mathrm{Ga}_x\mathrm{As}$. A decrease in x-composition reduces the bandgap, making it easier for electron transition between valence and conduction band, thus lowering threshold voltage. The patent shift of $C - V$ curve in Figure 5.3b illustrates this behavior.

The long channel threshold voltage model developed for $\mathrm{In}_{0.53}\mathrm{Ga}_{0.47}\mathrm{As}$ GAA MOSFET is compared with numerical simulation as illustrated in Figure 5.4 and 5.5. The low drain bias threshold voltage from simulation matches well with the model for the range of oxide thickness, channel doping and dielectric constant studied in this work (Table 5.1). Figure 5.4 reveals that threshold voltage depends strongly on heavily doped channel, as was previously anticipated from the $C - V$ characteristics shown in Figure 5.3a, but remains constant for lightly doped body [134]. Additionally, we deduce that geometric parameters strongly influence threshold voltage of the GAA transistor at low doping levels due to prominent volume inversion effect, which subsides as channel tends to leave full depletion with increment of acceptor concentration. The classical threshold voltage model ($V_\mathrm{T} = V_\mathrm{fb} + 2\phi_\mathrm{f} + Q_\mathrm{b}/C_\mathrm{ox}$) fails to account vol-

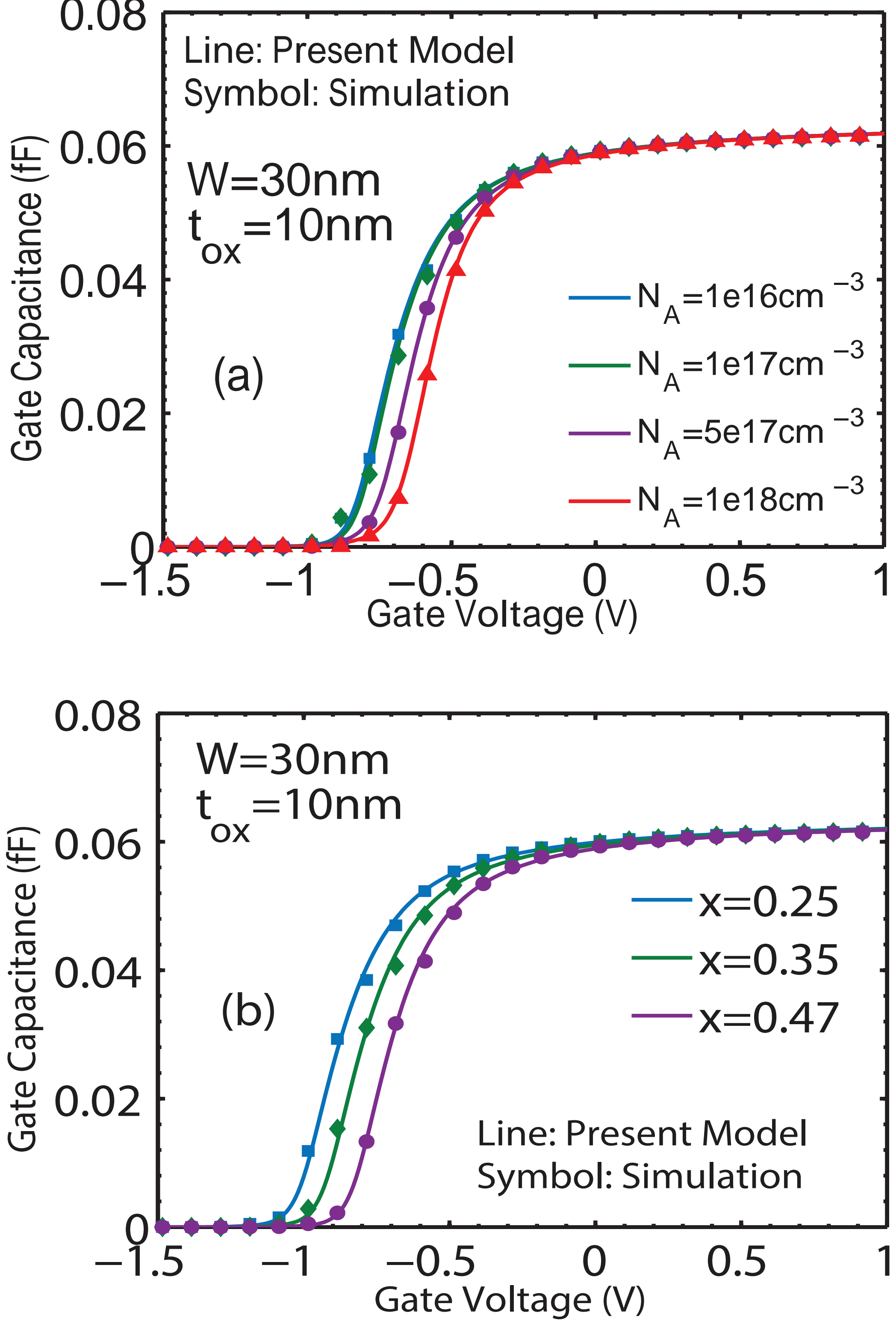


Figure 5.3: **Effect of channel material properties on CV curve of $In_{1-x}Ga_xAs$ GAA MOSFET.** (a) For various channel doping (x=0.47). (b) For various x-composition ($N_A = 2 \times 10^{16}$ cm^{-3}). A significant shift in CV profile takes place for heavily doped channel.

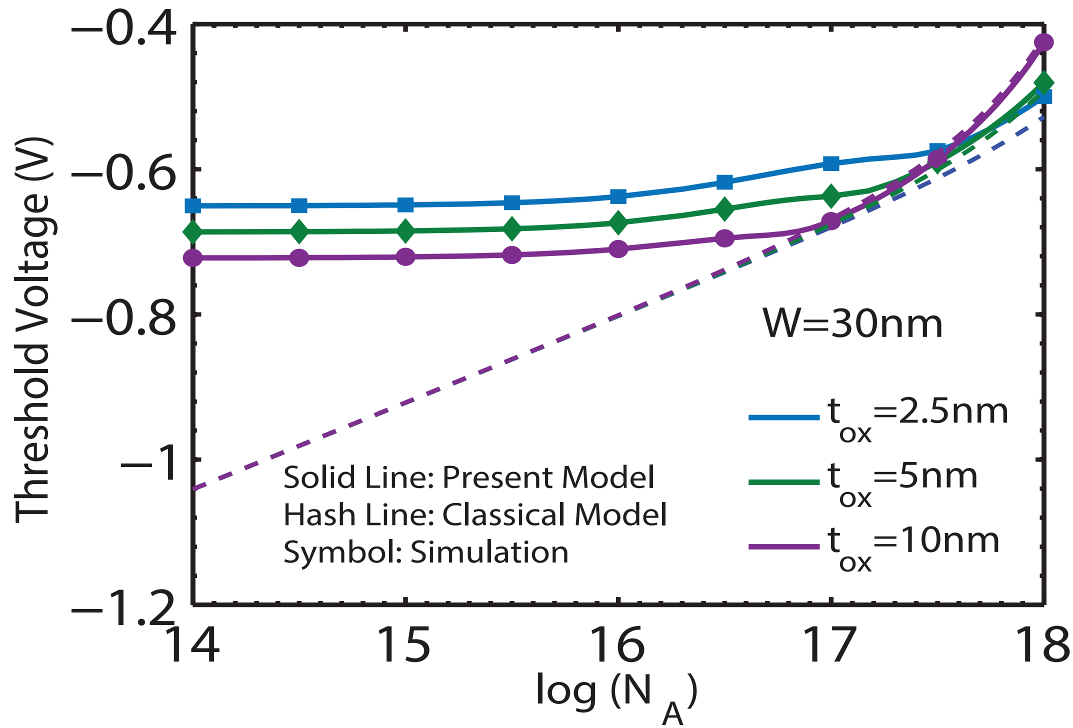


Figure 5.4: **Threshold voltage dependence on channel doping for different oxide thickness.** The classical threshold voltage model based on critical band bending in strong inversion deviates from the predicted result for lightly doped transistor.

Table 5.1: Process/device parameters used in this work.

Parameter Description (unit)	**Value**
Fin width (nm)	$20 - 40$
Oxide thickness (nm)	$2.5 - 10$
Acceptor concentration (cm^{-3})	$1 \times 10^{16} - 1 \times 10^{18}$
Mole fraction	$0.25 - 0.47$
Gate metal work function (eV)	4.6
Midgap D_{it} ($cm^{-2}eV^{-1}$)	5.6×10^{12}
Intrinsic carrier density (cm^{-3})	$6.3 \times 10^{11} - 5 \times 10^{13}$
Flat band voltage (V)	$-1.35 \sim -1.28$
Relative permittivity of $In_{1-x}Ga_xAs$	$13.9 - 14.2$
Relative permittivity of Al_2O_3	9.3 [106]
Relative permittivity of $Ga_2O_3(Gd_2O_3)$	15 [131]
Relative permittivity of $LaAlO_3$	17 [132]
Relative permittivity of HfAlO	21 [133]
Relative permittivity of HfO_2	25

ume inversion due to full depletion approximation. The proposed model also predicts the non-monotonic variation of V_T on t_{ox} and W as reported in Figure 5.5. This phenomenon was first reported by Shi *et al.* [135] for double-gate doped MOS device and

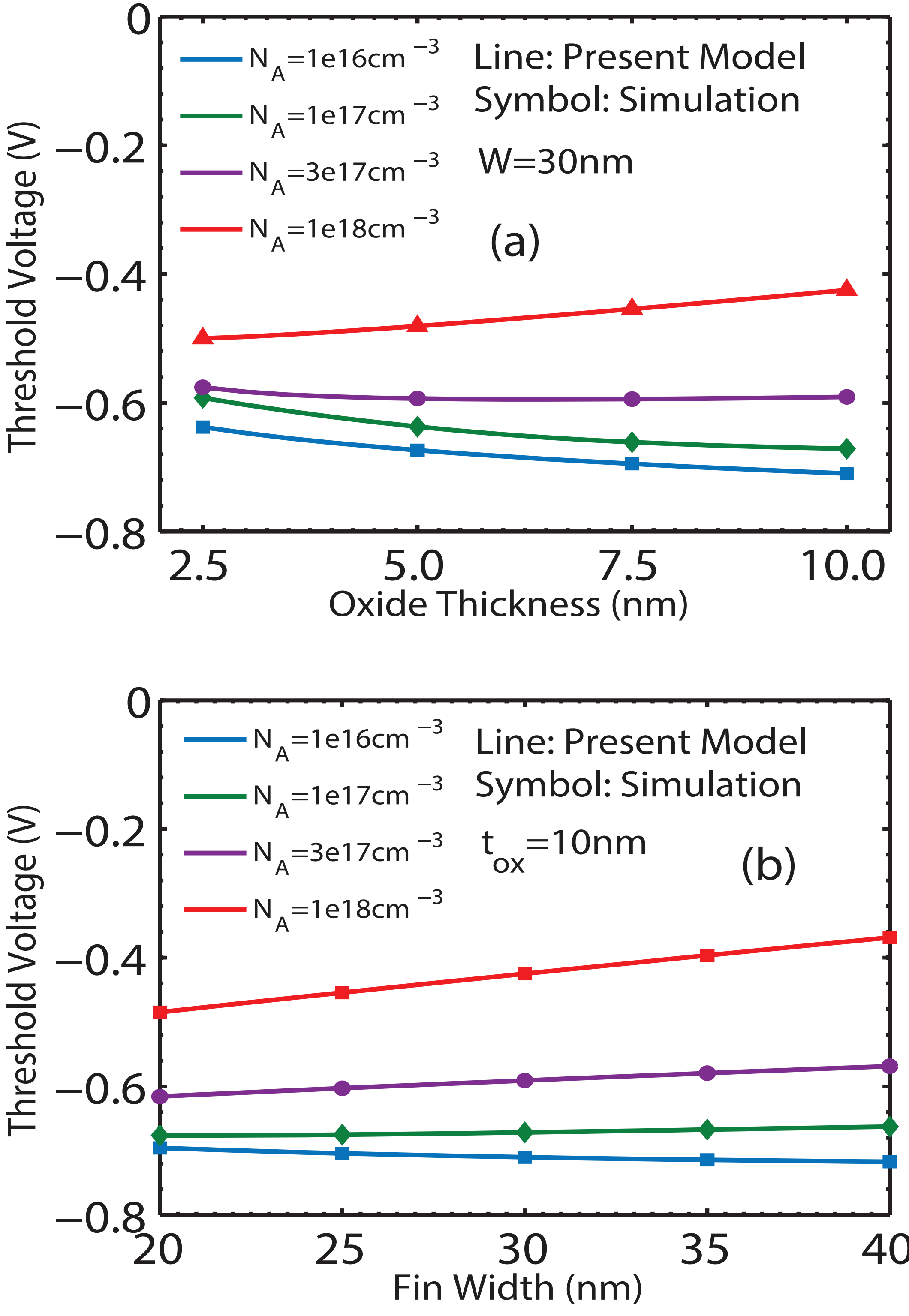


Figure 5.5: **Non-monotonic dependence of threshold voltage on:** (a) $t_{\rm ox}$ for various channel doping. (b) fin width for various channel doping.

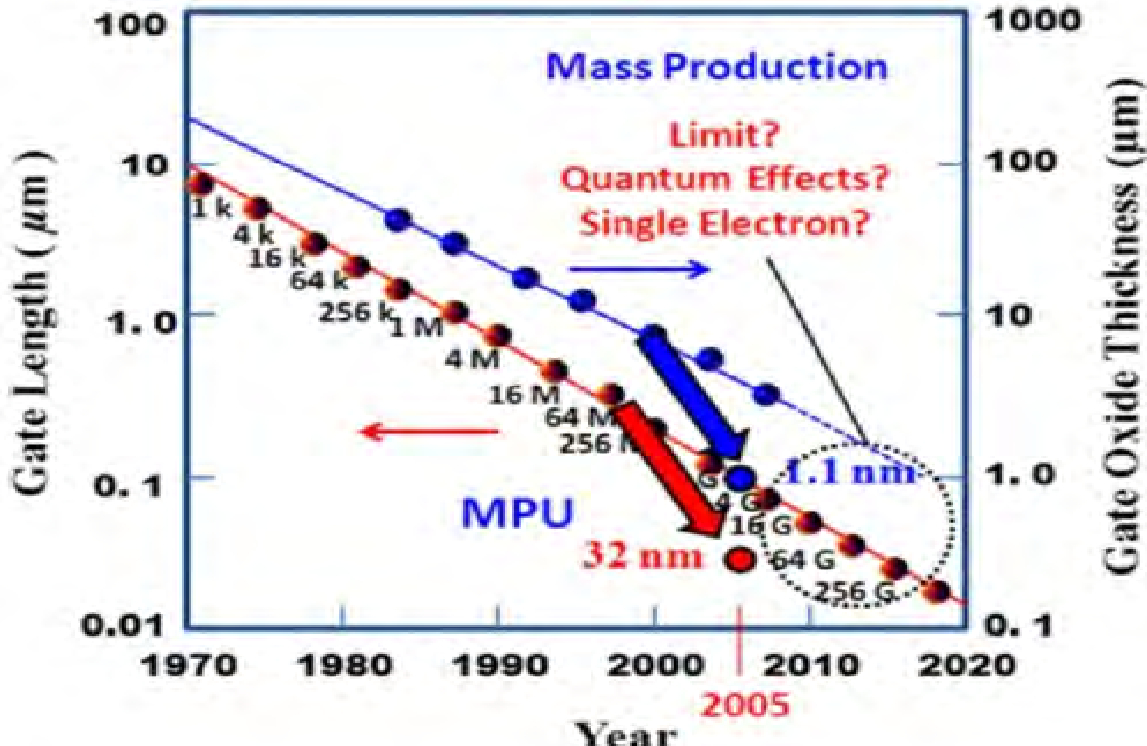


Figure 5.6: **The trend of MOSFET scaling from ITRS.** Picture taken from ITRS Corp. [136]

is inherent in GAA MOSFETs as well. Hence the need for quantum analysis becomes imperative for aggressively scaled transistor with lightly doped channel.

The primary motivation for using a scaled gate length of 50 nm with oxide thickness 10 nm arose due to the availability of experimental published reports [60] for symmetric GAA MOSFET having InGaAs channel. This converts to an equivalent oxide thickness (EOT) of 4.5 nm which is much larger than the International Technology Roadmap for Semiconductors (ITRS) guideline for device dimension as shown in Figure 5.6.

In our proposed model, the initial devices dimensions were kept similar to that of [60] for the sake of benchmarking the device transfer and output characteristics as will be described shortly. Later we evaluated the performance metrics with scaling of oxide thickness, fin width and gate length in both on and off state. The oxide thickness was scaled down to 2.5 nm which translates to an EOT of less than 1nm, keeping in convention with the ITRS guidelines.

The transfer characteristics obtained from the proposed model is displayed in Figure 5.7. The drain current and extrinsic transconductance g_{m} is normalized by the active region perimeter (2W+2H). Some of the transport model parameters used to calibrate the model with published experimental reports are shown in Table 3.1 which accounts for velocity saturation, mobility degradation, channel length modulation and series resistance. The numerical solution of (2.16) provides a smooth transition in the threshold regime which is further confirmed by continuous g_{m}, producing distinct peaks near threshold point as shown in Figure 5.7b. The incorporation of interface trap charge is essential in evaluating subthreshold performance metrics as portrayed in Figure 5.7c. The threshold voltage in DIBL evaluation is extracted from the I_{D}-V_{G} plot at a constant current level of 2 μA/μm due to high drain junction leakage current. The subthreshold slope (SS) obtained from the inverse of the steepest slope of transfer characteristics and DIBL at different gate length falls in the range of reported data, providing a precedent for comparing off-state performance of next generation GAA transistors.

The output characteristics of the GAA transistor matches well with the published report in [60] in both linear and saturation regime. From Figure 5.8, an ON-resistance of 1160 $\Omega \cdot \mu$m is obtained from the initial slope of the I_{D}-V_{D} curve at $V_{\mathrm{GS}} = 2$V. The continuity of the output characteristics is reflected from the gradual transition in output conductance as illustrated in Figure 5.8b.

Before delving into the scaling properties of GAA transistors, the degree of SCE affecting such devices are explored semi-analytically in both on and off state. Double-gate MOSFETs suffer from severe SCE as W/L ratio approaches unity [88]. Gate-all-around MOSFETs, on the other hand, provide better off-state performance in this regard, with DIBL and SS demonstrating roughly proportional variation with W/L ratio. As shown in Figure 5.9, for the range of fin width shown in Table 5.1, the maximum W/L ratio studied was 0.8 after which the DIBL and SS stray away from the linear relation. The impact of SCE on subthreshold slope is even more at higher drain bias, which is evident from the sparsity of SS from the best fit linear graph in Figure 5.8b. The scaling

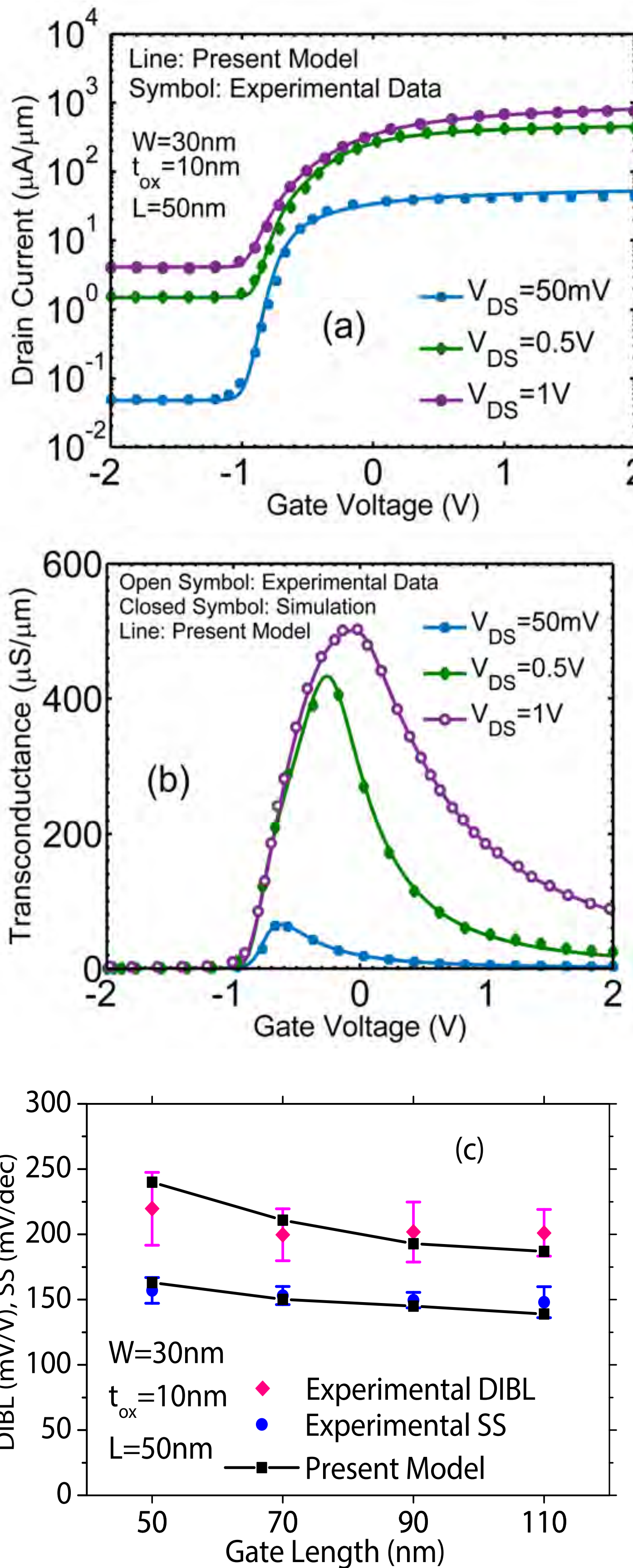


Figure 5.7: **Transfer characteristics of a 50nm GAA MOSFET.** (a) Drain current as a function of gate voltage. (b) Extrinsic transconductance. (c) DIBL and subthreshold slope extracted from the I_D-V_G plot. Experimental data has been extracted from [60].

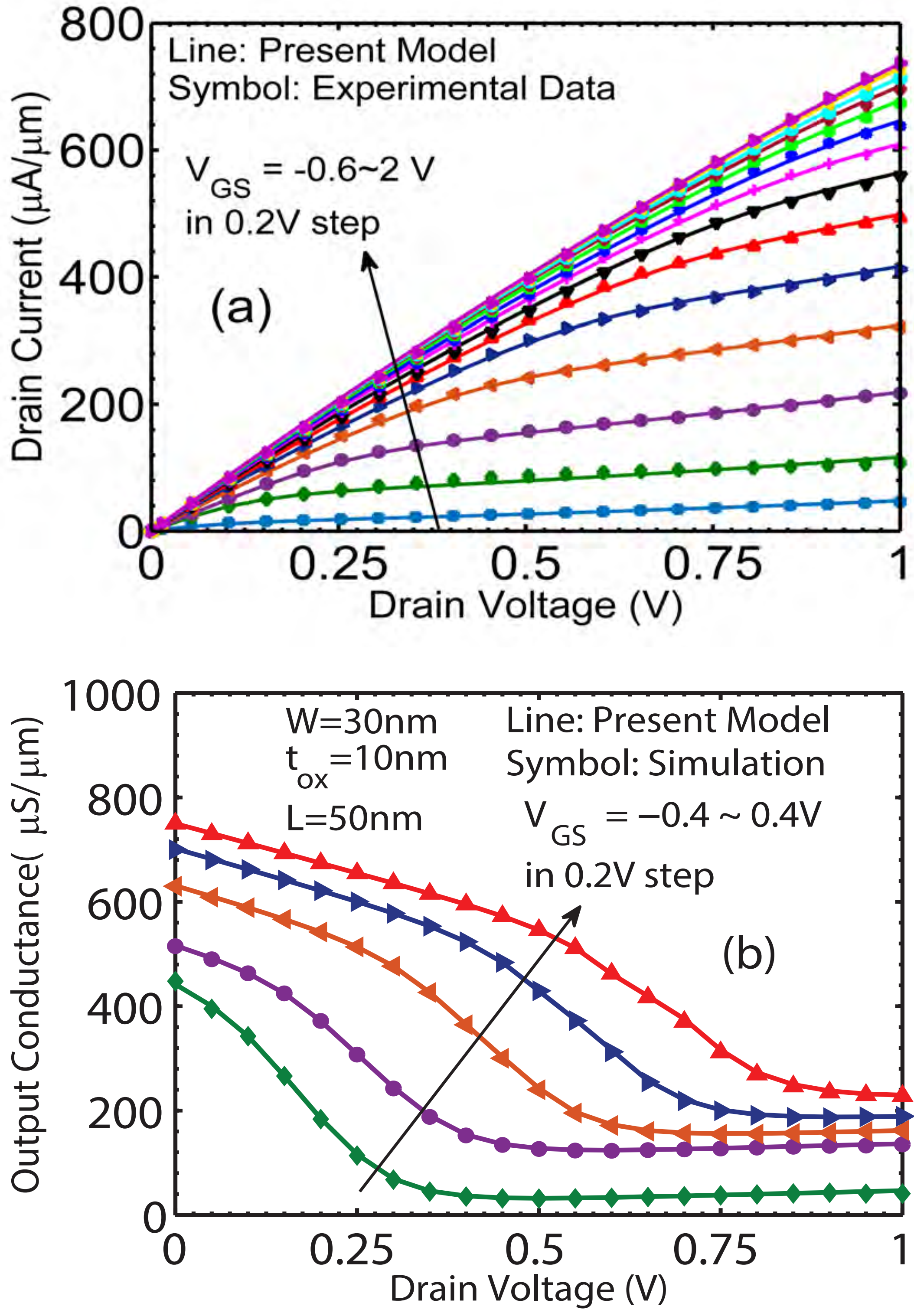


Figure 5.8: (a) Output characteristics of a 50nm GAA MOSFET. An R_{on} of 1160 $\Omega \cdot \mu m$ is obtained from the slope at V_{GS} = 2V (b) Output conductance of the same device, showing that drain current remains continuous from linear to saturation region. Experimental data has been extracted from [60].

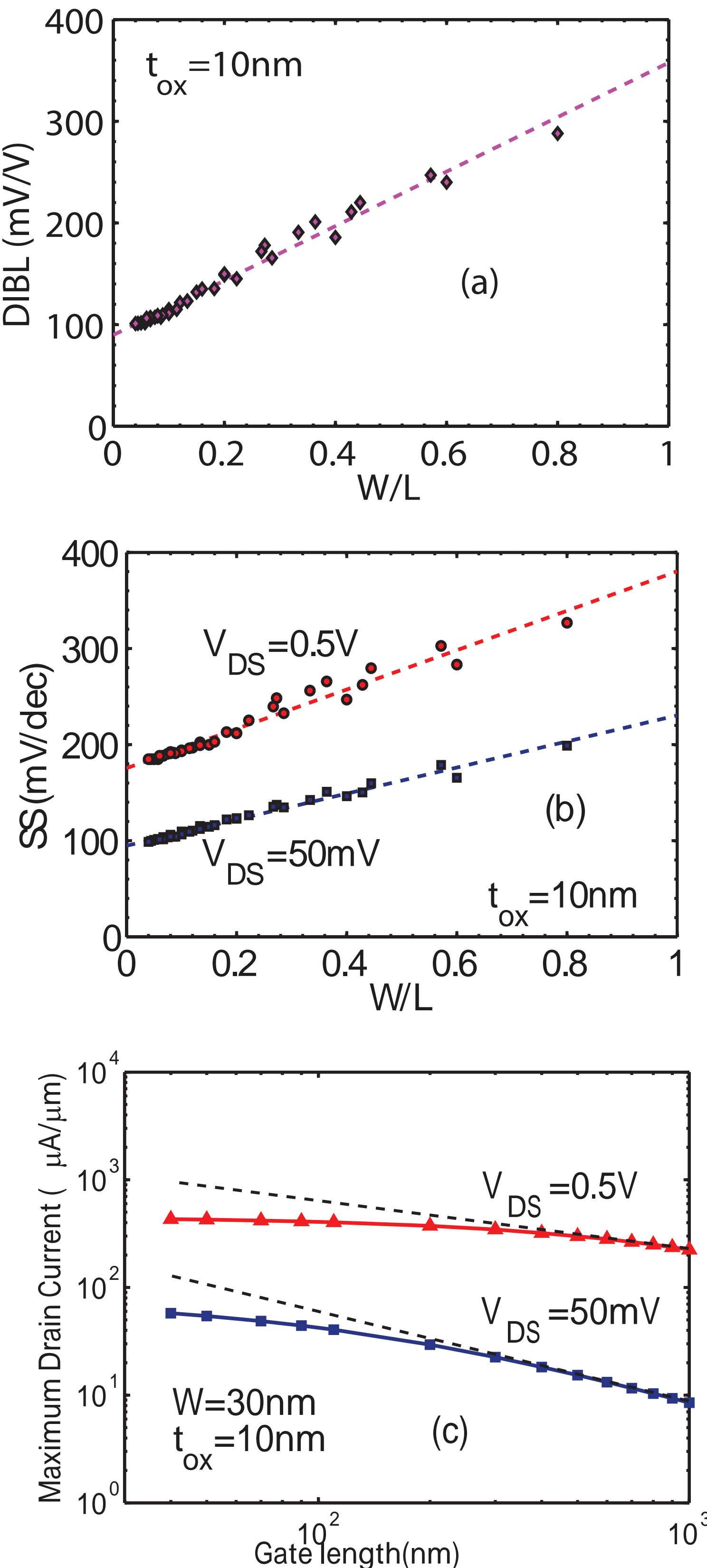


Figure 5.9: **On-state and off-state characteristics of an InGaAs GAA transistor.** Variation of (a) DIBL (b) SS with W/L ratio. Best fit straight lines are also plotted based on least square regression to highlight proportional relation with W/L. (c) Maximum ON-current as a function of gate length obtained at $V_{\mathrm{GS}} = 2\mathrm{V}$ and different drain bias. For comparison, the dotted line shows when the drain current starts to saturate due to non-ideal effects in the short channel MOSFET.

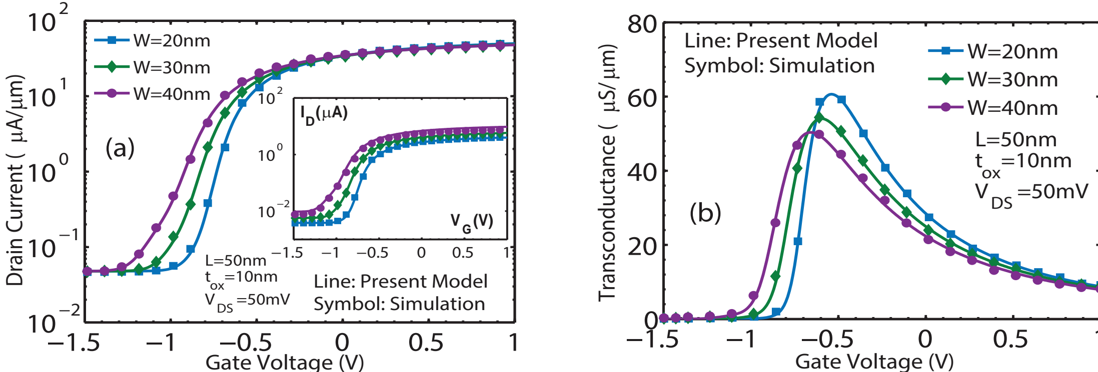


Figure 5.10: **Transfer characteristics of a GAA MOSFET for various fin width having $N_A = 2 \times 10^{16}\text{cm}^{-3}$.** (a) Normalized drain current as a function of gate voltage. Inset figure shows that total current of the wider nanowire is more as expected. (b) Transconductance as a function of gate voltage.

behaviour of drain current in the ON-state of the transistor is displayed by tracing the maximum drain current from submicron to long channel lengths as shown in Figure 5.8c. In the absence of non-ideal effects, the GAA transistor could reach drain current as high as 1 mA/μm at a gate length of around 40 nm. However, saturation induced by SCE, limits the channel current from reaching near ideal values.

The transfer characteristics of a symmetric GAA MOSFET for various fin width is presented in Figure 5.10. The saturation levels of the normalized drain current in strong inversion region is less dependent on fin width, although fin width scaling affects threshold characteristics strongly and indicates an improvement of threshold behavior by shifting the transition from threshold to weak inversion to the right. This is attributed to volume inversion of InGaAs channel caused by confinement of charge carriers at sub-nanometer dimensions, which otherwise would require further reduction in fin width for silicon technology. Inset figure reveals that the total current of a wider nanowire MOSFET is more as expected due to increased surface carriers near the oxide/semiconductor interface. There is only a slight increment in g_m peak as evidenced from Figure 5.10b, which can be further enhanced by scaling to deca-nanometer dimension, the analysis of which is restricted from the proposed model due to negligence of quantum effects [107]. Nevertheless, the excellent match between numerical simulations having quantization model and analytical results justify the relaxation of quantum effect incorporation in the proposed model for the range of dimension under study.

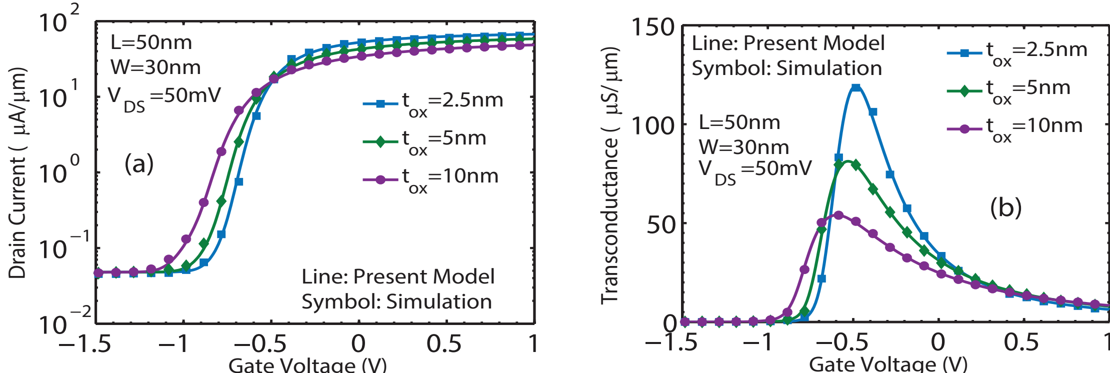


Figure 5.11: **Transfer characteristics of a GAA MOSFET for various oxide thickness having $N_A = 2 \times 10^{16} cm^{-3}$.** (a) Drain current as a function of gate bias. The cross-over of the curves indicate an invariant point where the effect of oxide thickness variation due to process limitation is minimized. (b) Transconductance as a function of gate bias.

Figure 5.11 explores the trend in transfer characteristics with oxide thickness variation. As was previously explained, an initial physical oxide thickness of 10 nm was used for a gate length of 50 nm, after which the trend of oxide scaling was investigated, keeping in compliance with the proposition of ITRS. It was found that increasing the gate oxide thickness induces a reduction in channel current, besides lowering the threshold voltage. The existence of a cross-over in the transfer characteristics was previously observed for long channel devices with wrap-around gate [137]. This phenomenon is extant in short channel transistors as well, occurring near threshold point of doped nanowire MOSFETs and serves as an invariant point, particularly important where oxide thickness variation could not be strictly controlled due to process limitations. The g_m peak increases by 2.4 times by reducing gate dielectric thickness from 10 nm to 2.5 nm as portrayed in Figure 5.11b. This highlights a potential scope for EOT scaling which, alternately, can be achieved by introducing high-κ dielectric into the MOS transistor.

Figure 5.12 gives us an elaborate comparative analysis of the impact of dimension scaling on the subthreshold performance of GAA nanowire MOSFET. Due to presence of SCE, the minimum gate bias required for the turn-on of the MOSFET is lowered as channel length is scaled down. From Figure 5.12a and 5.12d, it is observed that fin width causes greater threshold voltage roll-off at sub-nanometer gate lengths. The loss of gate control over electrostatic charges in thicker nanowire means that threshold

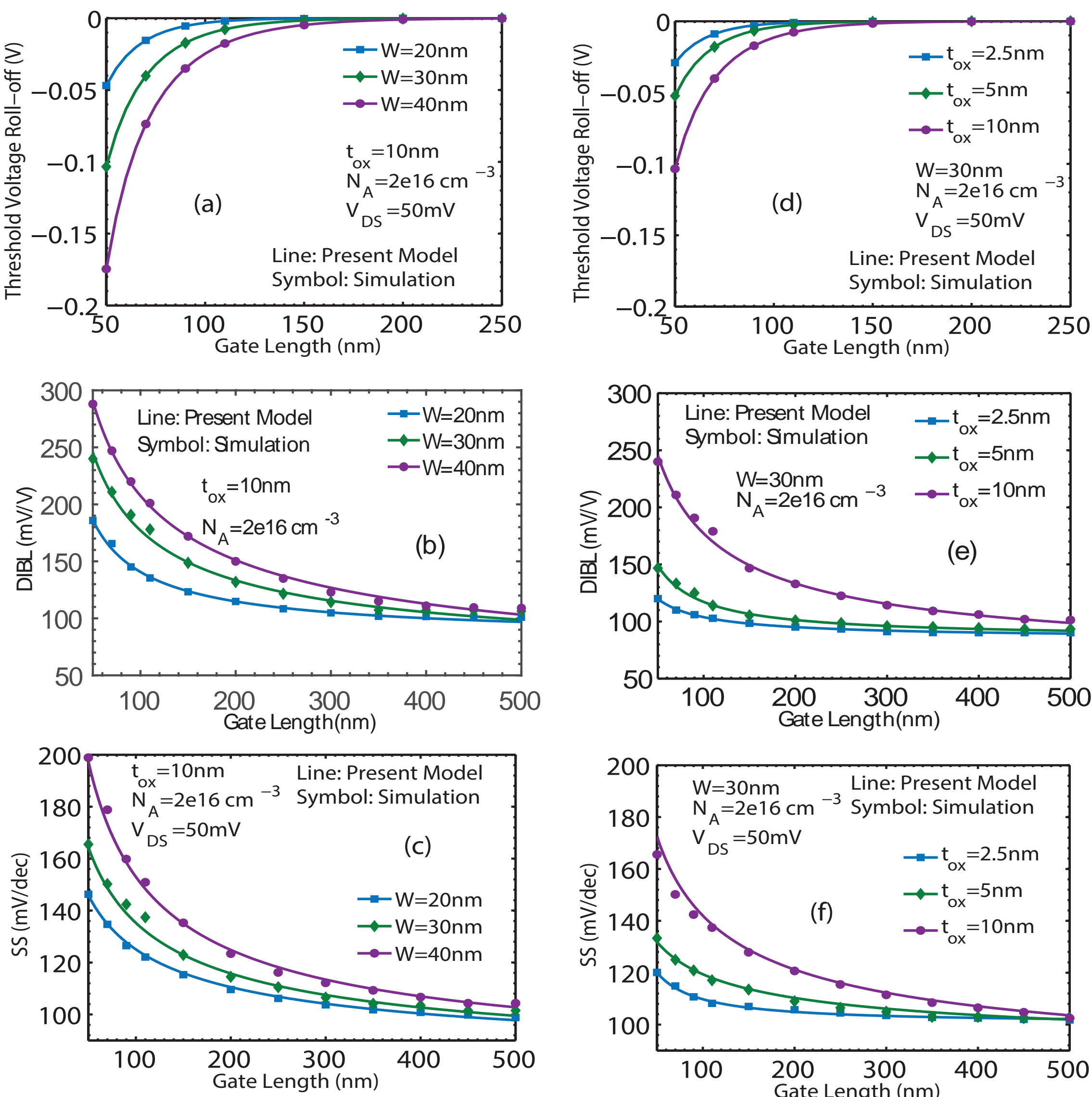


Figure 5.12: (a) Threshold voltage roll-off (b) Drain induced barrier lowering and (c) Subthreshold slope degradation due to gate length scaling at various fin width. (d) Threshold voltage roll-off (e) Drain induced barrier lowering and (f) Subthreshold slope degradation due to gate length scaling at various oxide thickness. The subthreshold properties are affected to greater extent due to fin width variation.

voltage decreases drastically with gate length reduction. The effect of scaling on DIBL for various fin width and oxide thickness are displayed in Figure 5.12b and 5.12e. The effect of DIBL is severe for nanowires with larger fin width, which is particularly inherited from the aggravated threshold voltage roll-off described earlier and only slight improvement is obtained by reduction of fin width to practical limits. On the other hand, a dramatic enhancement of DIBL is identified for GAA MOSFETs with thinner oxide thicknesses. Similar variation of SS is observed from dimension scaling, where the minimum slope of the InGaAs MOSFET is far from the ideal SS of 60 mV/dec. The poor DIBL and SS is attributed to the high interface trap density between the Al_2O_3/InGaAs interface. This could be overcome by stacking the gate oxide with $LaAlO_3$ as was successfully demonstrated in [105].

The present state of the gate-all-around device under consideration is reflected in Figure 5.13 showing the g_m·EOT product vs. L_{ch} of $In_{0.53}Ga_0.47As$ GAA FETs with other contemporary InGaAs MOSFETs [106,138–141]. Despite the low indium concentration (53%), the $In_{0.53}Ga_0.47As$ GAA MOSFETs demonstrate the highest g_m·EOT

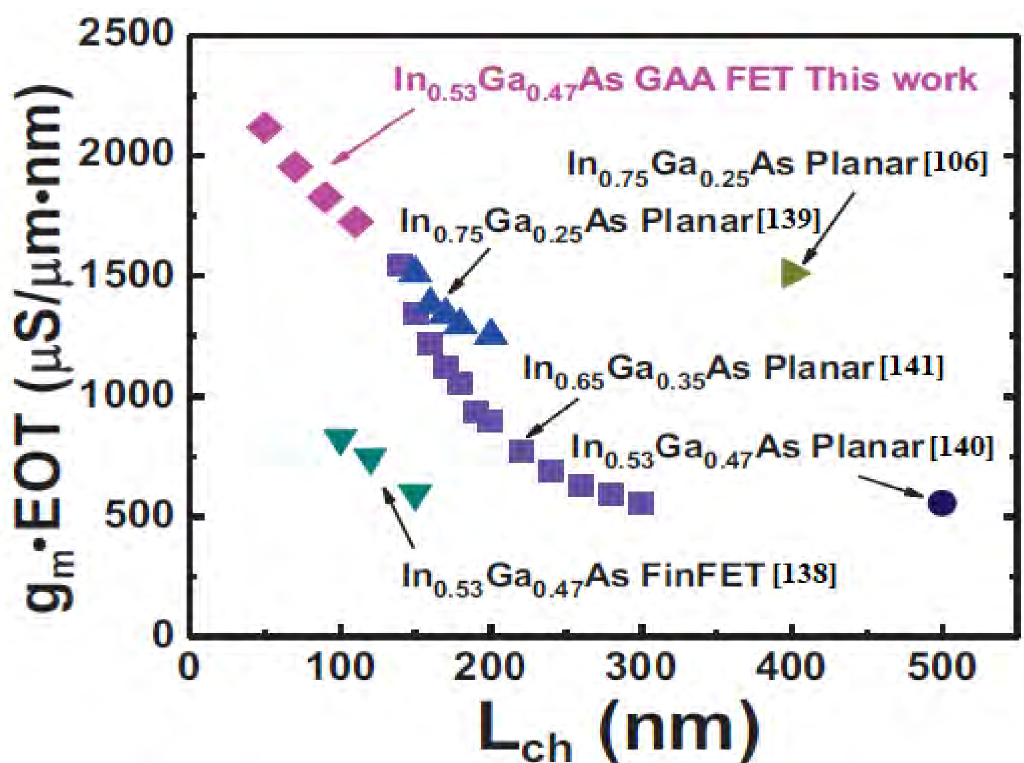


Figure 5.13: **Benchmarking g_m·EOT of contemporary planar and non-planar InGaAs surface-channel MOSFETs.** [60]

product with a prospect for reacher higher value through increment of the indium content. This is facilitated by the higher electron mobility of the InGaAs channel and the charge neutrality level being closer to the conduction band edge.

It is evident that the ultimate scalability of GAA MOSFETs can be achieved by incorporating high-κ dielectric having suitable integrability with the channel material. Although ALD Al_2O_3 is reported to have the best interface quality with InGaAs, the performance of such GAA transistors is limited by poor I_{on}/I_{off} ratio resulting from high drain junction leakage current. Surface Fermi level pinning has lead to the exploration of high-κ dielectrics on InGaAs, boosting transport property of GAA MOSFET in terms of improved I_{on}/I_{off} ratio and reduced gate leakage.

To this end, besides Al_2O_3, other high-k dielectrics like Ga_2O_3 (Gd_2O_3), $LaAlO_3$, HfAlO and HfO_2 have demonstrated excellent interface quality with reduced trap density [131–133, 142]. Figure 5.14 displays how the integration of various gate dielectrics affect the $C-V$ characteristics of a GAA MOSFET. The proportional increase in oxide capacitance from high-κ dielectric is evident with HfO_2 demonstrating the highest

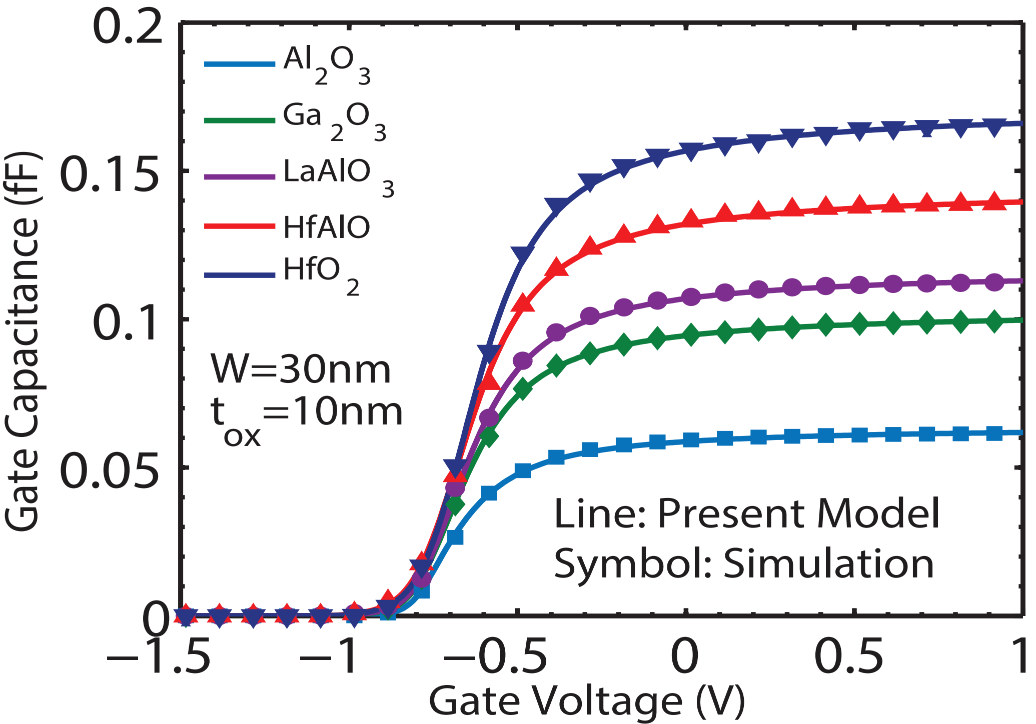


Figure 5.14: **Capacitance-voltage profile for different gate dielectric.**

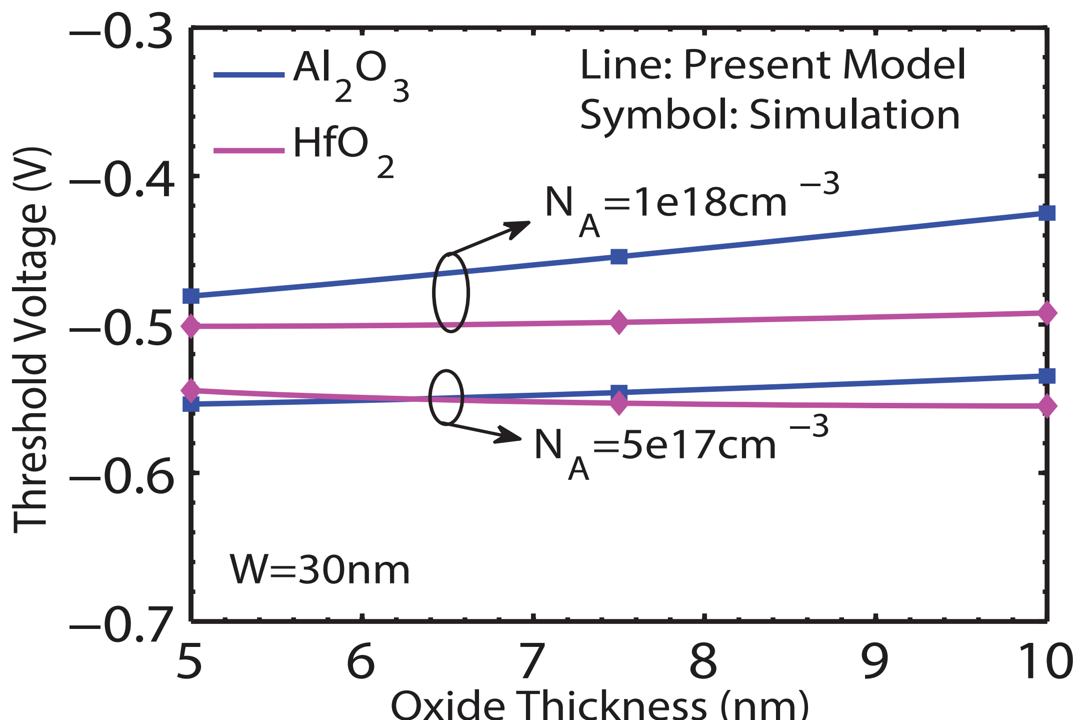


Figure 5.15: **Impact of high-κ dielectric on threshold voltage of heavily doped GAA transistor.**

capacitance with minimal change in threshold region.

Figure 5.15 identifies the behaviour of GAA transistor in threshold regime using high-κ dielectric. In spite of excellent cohesion with III-V semiconductor, Al_2O_3 is undesirable for heavily doped transistor due to greater variance in threshold voltage with oxide thickness scaling. Therefore, in fabrication processes where oxide thickness variation cannot be strictly controlled, it is desirable to use high-κ dielectric like HfAlO or HfO_2 which avoids any unnecessary threshold voltage roll-off besides providing superior capacitance coupling with the channel.

The switching efficiency (Q=gm/SS) is an important figure of merit to quantify the potential of inserting III-V channel material in CMOS technology that evaluates I_{on}-versus-I_{off} metric to capture the trade-off between dynamic switching speed and standby power [129]. The incorporation of $LaAlO_3$ or HfO_2 results into better switching efficiency as clarified by Figure 5.16 where thicker HfO_2 results into a larger $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio.

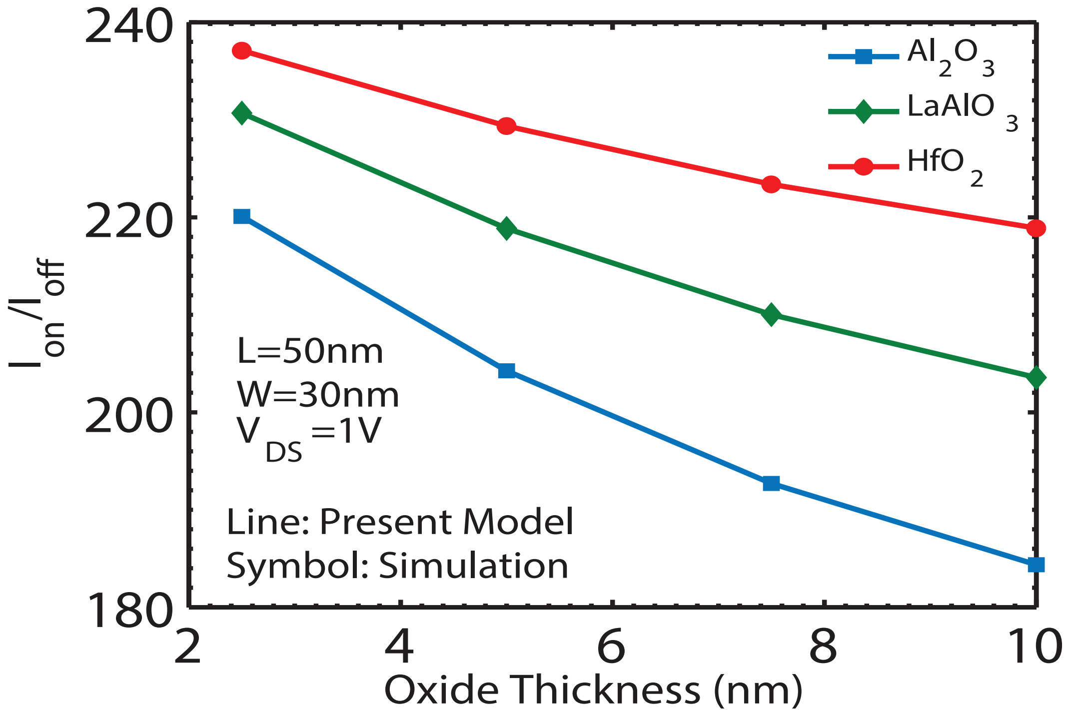


Figure 5.16: $I_{\text{on}}/I_{\text{off}}$ **ratio as a function of oxide thickness for various gate dielectric.** $I_{\text{on(off)}}$ is defined as the drain current at maximum (minimum) V_{GS} and high drain bias. The high drain junction leakage current of InGaAs GAA MOSFETs result in a small on-off ratio.

A high D_{it} of $12\times10^{12}/\text{cm}^2\text{eV}$ at $\sim$ 0.15 eV below conduction band was adopted for HfO_2 from published reports into the analytical framework [130, 143].

Figure 5.17 illustrates a radar plot comparing the key features and benefits of using HfO_2 over Al_2O_3 as gate dielectric. At low drain bias, the subthreshold behaviour is remarkably improved by replacing the gate oxide with HfO_2, reducing DIBL, subthreshold slope and threshold voltage roll-off to a greater extent. An increment of I_{max} indicates the superior current drivability in the ON-state of the GAA transistor with high-κ dielectric. A switching figure of merit Q($=g_m$/SS) of 0.82 (μS/μm)/(mV/dec) is obtained from using HfO_2, resulting in an improvement of 2.5 times over Al_2O_3. The high switching efficiency indicates InGaAs MOSFETs as potential candidate for switching application and logic devices.

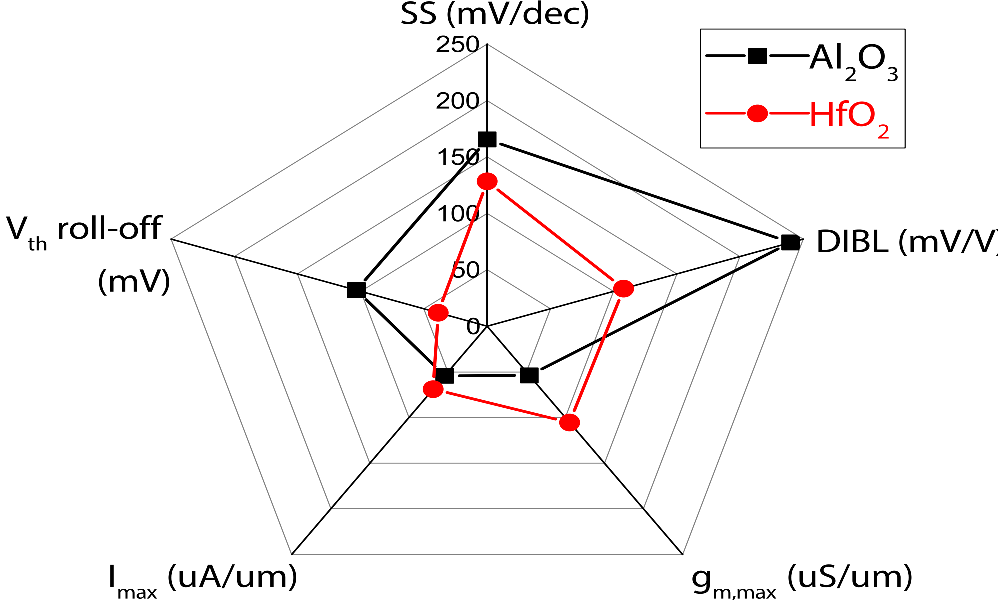


Figure 5.17: **Radar plot presenting a quantitative analysis between Al_2O_3 and HfO_2 as gate dielectric in 50nm InGaAs GAA MOSFET having fin width 30nm and t_{ox} 10nm at $V_{DS} = 50$mV.** A switching figure of merit of 0.82 (μS/μm)/(mV/dec) is obtained from using HfO_2, resulting in an improvement of 2.5 times over using Al_2O_3.

Chapter 6

Conclusion

This chapter summarizes the whole work and proposes some unexplored avenue pertinent to this work which can be put under extensive research.

6.1 Summary

Capacitance-voltage profile and threshold voltage comprise the electrostatic behaviour of a transistor. Based on a physics based continuous model, that avoids any fitting parameter, the channel charge of an inversion-type $In_{1-x}Ga_xAs$ GAA MOSFET is presented. The capacitance-voltage profile is rigorously investigated with variation in physical process parameters. The CV curve shows strong dependence in threshold region for variation of fin width, body doping and mole fraction of III-V semiconductor channel. Contrary to this, oxide thickness scaling and use of high-k gate oxide affects strong inversion capacitance. The proposed long channel threshold voltage model proves effective from low to heavily doped devices and provides a clear intuition of volume inversion effect in lightly doped transistor.

The latter half of the thesis comprises an analytical drain current model, catered for InGaAs with inclusion of interface defects and trap charges existing near the oxide/semiconductor interface. Certain non-ideal effects are included to emulate the SCEs in ultra scaled transistors. The model parameters have been calibrated with published reports based on symmetric InGaAs MOSFET. An extensive analysis of the GAA transistor is presented with variation in physical process parameters. The sub-

threshold performance metrics such as threshold voltage roll-off, DIBL and subthreshold slope have been thoroughly investigated. Further, the benefits of EOT scaling and integration of high-κ dielectric is explored to realize the scalability of GAA MOSFETs in the sub-nanometer domain, making them potential candidate for switching and logic applications. The analysis presented in this work will provide the impetus necessary for further investigation in gate-all-around transistors, thereby serving as a platform for examination of more complex nanosheet structures.

6.2 Suggestions for Future Work

- For a fin width less than 10 nm, quantization of mobile carriers in the channel region is dominated by quantum mechanical (QM) effect. For a square cross-section, an analytical approach can be developed incorporating this QM effect which was previously modeled numerically.
- Apart from fringing capacitance, other intrinsic/extrinsic capacitances can be modeled via compact expression.
- For ultra-scaled gate dielectric thickness, the gate tunneling and leakage performance analysis are essential for determination of static power dissipation. The proposed model can be extended to devise a method for computing leakage parameters.
- Only square cross-section was considered in the evolution of this model. For stacked nanosheet, a wider single stack has proven to be more efficient than multiple smaller-fin stacks. This results into rectangular sheet-like structure, where potential distribution across the channel is not symmetric due to non-unity W/H ratio. The development of compact model for rectangular GAA nanosheet can be carried out.

Appendices

Appendix A

Difference of potential

A.1 Difference of potential in deep subthreshold

Let us consider the normalized difference of potential as $\alpha=(\phi_{\rm s}\text{-}\phi_0)/\phi_{\rm t}$ where $\phi_{\rm s}$ and ϕ_0 are the surface and center potential inside the semiconductor layer respectively, $\phi_{\rm t}$=kT/q is the thermal voltage.

In subthreshold region, only depletion charges appear in the 2-D Poisson equation, simplifying to,

$$\frac{\mathrm{d}^2\phi}{\mathrm{dx}^2}+\frac{\mathrm{d}^2\phi}{\mathrm{dy}^2}=\frac{qN_{\rm A}}{\epsilon_{\rm s}} \tag{A.1.1}$$

$$2\frac{\mathrm{d}^2\phi}{\mathrm{dx}^2}=\frac{qN_{\rm A}}{\epsilon_{\rm s}} \tag{A.1.2}$$

Integrating equation (A.1.2) once using the condition $\frac{\mathrm{d}\phi}{\mathrm{dx}}=0$ at x=0, we obtain,

$$\frac{\mathrm{d}\phi}{\mathrm{dx}}=\frac{qN_{\rm A}}{2\epsilon_{\rm s}}x \tag{A.1.3}$$

Integrating once more with boundary condition at the center and oxide-semiconductor interface leads to,

$$\int_{\phi_0}^{\phi_s} \mathrm{d}\phi = \int_0^{W/2} \frac{qN_\mathrm{A}}{2\epsilon_\mathrm{s}} x \, \mathrm{dx} \tag{A.1.4}$$

$$\phi_\mathrm{s} - \phi_0 = \frac{qN_\mathrm{A}}{4\epsilon_\mathrm{s}} \left(\frac{W^2}{4} \right) \tag{A.1.5}$$

$$\frac{\phi_\mathrm{s} - \phi_0}{\phi_\mathrm{t}} = \alpha_\mathrm{st} = \frac{qN_\mathrm{A} W^2}{16 \epsilon_\mathrm{s} \phi_\mathrm{t}} \tag{A.1.6}$$

A.2 Difference of surface-center potential in terms of Lambert function

Generally the double derivative of potential can be written using coarse finite difference method [111] resulting into,

$$\left. \frac{\mathrm{d}^2\phi}{\mathrm{dx}^2} \right|_{x=0} = \left(\frac{\phi(-\frac{W}{2}) - \phi_0}{W/2} - \frac{\phi_0 - \phi(\frac{W}{2})}{W/2} \right) \frac{1}{W/2} \tag{A.2.1}$$

Under symmetric operation, $E|_{x=0} = 0$ and using simplifying assumption leads to,

$$\phi(W/2) = \phi(-W/2) \tag{A.2.2}$$

Substituting (A.2.1) into (2.2) we get,

$$\frac{8}{W^2} \left(\phi\left(\frac{W}{2} \right) - \phi_0 \right) = \frac{qN_\mathrm{A}}{2\epsilon_\mathrm{s}} \left(\frac{n_\mathrm{i}^2}{N_\mathrm{A}^2} \mathrm{e}^{\frac{\phi_0 - V}{\phi_\mathrm{t}}} + 1 \right) \tag{A.2.3}$$

$$\phi_\mathrm{s} - \phi_0 = \frac{qN_\mathrm{A} W^2}{16\epsilon_\mathrm{s}} \left(\frac{n_\mathrm{i}^2}{N_\mathrm{A}^2} \mathrm{e}^{\frac{\phi_0 - V}{\phi_\mathrm{t}}} + 1 \right) \tag{A.2.4}$$

After some mathematical manipulation, the normalized difference of potential can be expressed as,

$$\alpha = \alpha_\mathrm{st} + \mathrm{LW} \left(\frac{n_\mathrm{i}^2}{N_\mathrm{A}^2} \alpha_\mathrm{st} \mathrm{e}^{-\alpha_\mathrm{st}} \mathrm{e}^{\frac{\phi_\mathrm{s} - V}{\phi_\mathrm{t}}} \right) \tag{A.2.5}$$

From (A.2.5) the following relation also holds, which will be used in the derivation of long channel threshold voltage for GAA MOSFET.

$$\frac{n_\mathrm{i}^2}{N_\mathrm{A}^2} \mathrm{e}^{\frac{\phi_0 - V}{\phi_\mathrm{t}}} - \alpha = -1 - \alpha \left(1 - \frac{1}{\alpha_\mathrm{st}} \right) \tag{A.2.6}$$

A.3 Characteristic natural length of a symmetric GAA MOSFET

Considering only depletion charge in subthreshold region, the quasi 2-D Poisson's equation can be written as,

$$2\frac{\mathrm{d}^2\phi(x,z)}{\mathrm{d}x^2}+\frac{\mathrm{d}^2\phi(x,z)}{\mathrm{d}z^2}=\frac{qN_{\mathrm{A}}}{\epsilon_{\mathrm{s}}} \tag{A.3.1}$$

In the subthreshold region, parabolic potential profile is assumed in the direction of carrier confinement from gate-to-gate.

$$\phi(x,z)=K_0(z)+K_1(z)\cdot x+K_2(z)\cdot x^2 \tag{A.3.2}$$

Using the boundary conditions at the central nanowire axis (x=0) and oxide/semiconductor interface (x=± W/2),

$$\phi(0,z)=\phi_0(z) \tag{A.3.3}$$

$$\phi(\pm W/2,z)=\phi_{\mathrm{s}}(z) \tag{A.3.4}$$

$$\left.\frac{\mathrm{d}\phi(x,z)}{\mathrm{d}x}\right|_{x=0}=0 \tag{A.3.5}$$

$$\left.\frac{\mathrm{d}\phi(x,z)}{\mathrm{d}x}\right|_{x=\pm W/2}=\frac{C_{\mathrm{ox}}}{4W\epsilon_{\mathrm{s}}}(V_{\mathrm{G}}-V_{\mathrm{fb}}-\phi_{\mathrm{s}}(z)) \tag{A.3.6}$$

we obtain potential profile $\phi(x,z)$ in terms of $\phi_{\mathrm{s}}(z)$, where ϵ_{ox} and t_{ox} are the permittivity and thickness of the oxide layer respectively.

$$\phi(x,z)=\phi_{\mathrm{s}}-\frac{V_{\mathrm{G}}-V_{\mathrm{fb}}-\phi_{\mathrm{s}}(z)}{t_{ox}}\frac{\epsilon_{\mathrm{ox}}}{\epsilon_{\mathrm{s}}}\frac{W}{4}+\frac{V_{\mathrm{G}}-V_{\mathrm{fb}}-\phi_{\mathrm{s}}(z)}{Wt_{\mathrm{ox}}}\frac{\epsilon_{\mathrm{ox}}}{\epsilon_{\mathrm{s}}}x^2 \tag{A.3.7}$$

The potential profile $\phi(x,z)$ can now be expressed in terms of $\phi_0(z)$ by setting x=0.

$$\phi_0(z)=\phi_{\mathrm{s}}-\frac{V_{\mathrm{G}}-V_{\mathrm{fb}}-\phi_{\mathrm{s}}(z)}{t_{\mathrm{ox}}}\frac{\epsilon_{\mathrm{ox}}}{\epsilon_{\mathrm{s}}}\frac{W}{4} \tag{A.3.8}$$

Substituting equation (A.3.8) into (A.3.7) for $\phi_{\mathrm{s}}(z)$, we obtain a simplified expression of potential profile given by,

$$\phi(x,z)=\phi_0(z)+\frac{V_{\mathrm{G}}-V_{\mathrm{fb}}-\phi_0(z)}{a_1Wt_{\mathrm{ox}}}\frac{\epsilon_{\mathrm{ox}}}{\epsilon_{\mathrm{s}}}x^2 \tag{A.3.9}$$

where $a_1 = 1 + \epsilon_{\text{ox}} W / 4\epsilon_{\text{s}} t_{\text{ox}}$. Differentiating equation (A.3.9) twice with respect to x and z and replacing in (A.3.1) gives us the differential equation of potential at the center plane of the channel in terms of characteristic field penetration length (λ).

$$\frac{\mathrm{d}^2\phi_0(z)}{\mathrm{d}z^2} + \frac{V_{\text{G}} - V_{\text{fb}} - \phi_0(z)}{\lambda^2} = \frac{qN_{\text{A}}}{\epsilon_{\text{s}}} \tag{A.3.10}$$

The characteristic natural length of the symmetric GAA MOSFET is defined as,

$$\lambda^2 = \frac{\epsilon_{\text{s}}}{4\epsilon_{\text{ox}}} a_1 W t_{\text{ox}} \tag{A.3.11}$$

$$\lambda = \sqrt{\frac{\epsilon_{\text{s}} W t_{\text{ox}}}{4\epsilon_{\text{ox}}} \left(1 + \frac{\epsilon_{\text{ox}} W}{4\epsilon_{\text{s}} t_{\text{ox}}}\right)} \tag{A.3.12}$$

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