M.SC. ENGG. THESIS

WIDE TUNING MULTIMODE SPLIT-LOAD RING OSCILLATOR FOR LEAKAGE-TOLERANT STUCK-ON FAULT DETECTION IN SUBMICRON CMOS CIRCUITS

by

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Submitted to

Department of Electrical and Electronic Engineering

in partial fulfillment of the requirements for the degree of

Master of Science in Electrical and Electronic Engineering

Department of Electrical and Electronic Engineering

Bangladesh University of Engineering and Technology (BUET)

Dhaka 1000

October 2021

Approval Certificate

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This is declared that the work entitled "Wide Tuning Multimode Split-Load Ring Oscillator for Leakage-Tolerant Stuck-On Fault Detection in Submicron CMOS Circuits" is the outcome of research carried out by me under the supervision of Dr. Apratim Roy, in the Department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, Dhaka 1000. It is also declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Acknowledgment

I would like to express my sincere gratitude to my supervisor, Dr. Apratim Roy for his supportive guidance and constructive suggestions throughout this research work. He is an amazing academician and I am blessed to work with him in my M.Sc. thesis. His constant encouragements and invaluable assistance motivated me to push my boundaries harder. Throughout my life, I will benefit from the experience and knowledge I gained working with Dr. Apratim Roy.

It is my pleasure to acknowledge Dr. Md. Kamrul Hasan, Dr. Md. Shafiqul Islam, Dr. Ahmed Zubair and Dr. Md. Anwarul Abedin for serving as members on my examination committee. I would like to formally thank them for reviewing this thesis and giving their valuable time and suggestions.

I owe more than words that can describe to my parents, S. M. Ihtishamul Huq and Salma Huq for their constant support, encouragement and faith which works as a positive reinforcement, especially during my failures. This work is dedicated to them.

Finally, all praise and glory to the Almighty for giving me the patience, strength, knowledge and capability to complete this research work successfully.

Abstract

This thesis focuses on designing robust and reliable fault testing methods using oscillators to detect transistor stuck-on (TSON) faults in submicron CMOS circuits. Simulations are performed in Cadence Virtuoso platform using 90 nm technology models. There are several structures for voltage controlled oscillators (VCO), among which the single-ended ring oscillator (SERO) structure is utilized for its superiority in terms of power penalty and manufacturability. The conventional structure has been modified with split-load technique for dual-mode tuning to facilitate greater control in frequency regulation. Meanwhile, the low power requirement of the circuit is maintained through device sizing. While considering the effects of parasitic capacitances, the proposed architecture provided the maximum tuning range when compared with other presented works in literature. Next, the frequency response of the oscillator has been investigated as a function of the controlling parameters tuning voltages, number of stages in the ring, and transistor width ratio to derive an empirical model for the operating point. Unlike the existing approximate models which only apply for the conventional SERO circuit, the frequency model in this work will assist the designer to accurately set the desired operating point. Finally, the SERO architecture with its load adaptation has been utilized to propose two fault-testing methods where the oscillator functions as current- and voltage-controlled oscillators, respectively. The test schemes exploit triggered output oscillations during the presence of a fault in the circuit under test (CUT). Computational ease and system reliability are improved by avoiding average quiescent current calculation in the I_{DDQ} method and indeterminate voltages of the logic voltage method. The proposed testing schemes remain more effective in high-leakage CMOS regime through threshold regulation achieved by multimode tuning of the split-load SERO and mirror device sizing, circumventing complex circuitry compared to built-in-current-sensor (BICS) protocols for on-chip fault detection.

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List of Abbreviations

Abbreviation	Description
BICS	Built-In Current Sensor
CCO	Current Controlled Oscillator
CMOS	Complementary Metal-Oxide Semiconductor
CS-VCO	Current Starved Voltage Controlled Oscillator
CUT	Circuit Under Test
FoM	Figure of Merit
FTR	Frequency Tuning Range
LC	Inductor-Capacitor
PDN	Pull-Down Network
PLL	Phase Locked Loop
PN	Phase Noise
PUN	Pull-Up Network
RFIC	Radio Frequency Integrated Circuits
RO	Ring Oscillator
SERO	Single-Ended Ring Oscillator
SESLRO	Single-Ended Split-Load Ring Oscillator
STSCL	Subthreshold Source Coupled Logic
TG	Transmission Gate
TSON	Transistor Stuck-ON
TSV	Through Silicon Via
VCO	Voltage Controlled Oscillator

List of Symbols

Symbol	Description
$H(s)$	Transfer function of feedback system
f_{VCO}	Frequency of VCO
f_{OSC}	Oscillation frequency
f_O	Center or operating frequency
Δf	Offset frequency
K_{VCO}	Gain of VCO
V_{ctrl}	Control voltage
ω_{osc}	Oscillation frequency in radian
φ	Arbitrary phase reference
α	Switching factor
C_L	Parasitic load capacitance
V_{DD}	Supply voltage
V_{bias}	Gate bias voltage of load transistor in SESLRO
t_{dHL}	Propagation delay during high to low transition
t_{dLH}	Propagation delay during low to high transition
λ	Channel length modulation of MOSFET
N	Number of stages in ring oscillator
W_R	PMOS to NMOS width ratio

Chapter 1

Introduction

1.1 Background

Oscillators represent one of the fundamental blocks in electronic systems that are employed for system-controlling operations such as clock generation, frequency synthesis and frequency translation [1]. Recent growth in wireless communication has demanded application-specific research to develop high quality phase locked loop (PLL) circuits which is an essential component in the radio frequency integrated circuits (RFICs). One of the driving blocks of the PLL segment is the voltage controlled oscillator (VCO) which is associated with signal processing tasks in the locked loop, mainly in frequency selection of the received signal. The block diagram of a typical PLL is shown in Fig. 1.1. An ideal VCO generates a signal whose frequency is a linear function of a controlled input voltage and its main characteristics in a PLL circuit include a wide tuning range to utilize maximum frequency spectrum in the communication channel [2] and a high operating-point to support increasing carrier frequency (in gigahertz range) [3]. Figure 1.2 shows the spectral growth for cellular communication in the United States of America (USA) over a span of 29 years due to the increase in traffic. In 2021, spectral occupancy has reached above the 21 GHz band.

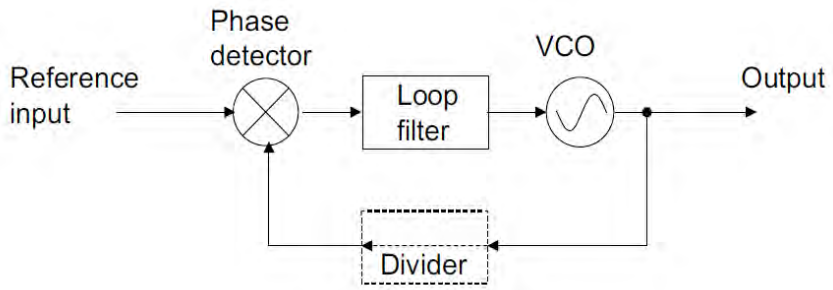


Fig. 1.1: Block diagram of PLL

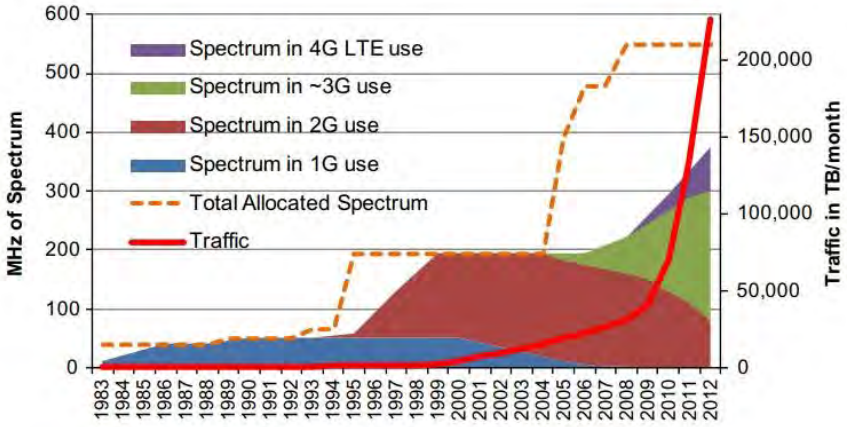


Fig 1.2: Spectrum growth versus traffic growth [2]

The current trend of VCO design categorizes it into two architectures: (i) inductor-capacitor (LC) oscillator and (ii) ring oscillator (RO) [4]. Compared to LC oscillators, RO takes smaller chip area and provides a larger tuning range at the cost of higher power consumption and phase noise (PN). The RO can be further classified into single-ended (SERO) and differential structures. With reduced cost due to smaller die area, improved utilization of the frequency spectrum due to wide tuning and easy integration, RO has proven to be a popular choice for the design of VCOs.

On the other hand, with aggressive scaling of semiconductor devices and higher circuit complexity, possibility of occurrence of predominant error-inducing circuit events like transistor stuck-on (TSON) faults increases [5]. A TSON fault is a permanent fault that may occur due to shorted connection or a voltage spike at the drain terminal causing the device to reach its breakdown condition. Such a fault always generates errors when the failing device is exercised. Therefore, testing of integrated circuits is a fundamental task to ensure high manufacturing yield.

1.2 Motivation of the Thesis

The study of RO is still being widely researched and studies on various architectures in literature reveal that a significant trade-off frequently exists between power overhead and operating-point. Therefore, there is a requisite to further investigate oscillator structures which provide wide flexible tuning with sensitivity to controlling parameters while maintaining a cap on power penalties.

Additionally, conventional logic method for TSON fault detection renders unreliable as it fails to detect the ambiguous logic level occurring at the output of static complementary metal-oxide semiconductor (CMOS) circuit. The alternative current measurement method typically involve device-heavy compound circuitry with high area overhead and limited functionality in sub-micron domain where fault current becomes difficult to distinguish from increased leakage current. Although ROs have been previously used to detect through-silicon-via (TSV) faults in 3D stacked ICs, their employment is logistically burdensome. Hence, there remains a scope to develop a homogeneous leakage-tolerant and area-efficient TSON detection scheme for CMOS circuits based on ROs.

1.3 Objectives of the Thesis

The objectives of this work are the following:

1. To devise a three-stage single-ended split-load ring oscillator (SESLRO) with multimode tuning leading to regulation of oscillator sensitivity.
2. To propose two area-efficient reliable SESLRO based testing schemes which support a wide range of supply rails for accelerated TSON fault detection in submicron CMOS architectures.
3. To develop a homogeneous leakage-tolerant TSON sensing method which achieves functionality in high leakage deep submicron regime with adaptable threshold regulation.

In brief, the aim of this thesis is to develop a multimode split-load ring oscillator architecture that will significantly curtail the circuit area and cost of TSON testing

methods, support increased detection reliability, and help overcome the limitations of time-consuming quiescent current measurement approaches, making them compatible with leakage-heavy regimes.

1.4 Thesis Organization

The overall thesis is organized into five chapters. A brief abstract of the succeeding chapters are given below.

Chapter 1 presents the background and motivation behind this research work. Additionally, the objectives of the thesis with specific aims are mentioned.

Chapter 2 briefly provides a review of the theory of voltage controlled oscillators including VCO specifications and categories like LC and ring oscillators. Then, literature study is provided for single-ended ring oscillators and their adaptations. Finally, issues related with operating-point models necessary for oscillator design are addressed.

Chapter 3 demonstrates the development of the proposed multimode single-ended split-load ring oscillator architecture with description of the simulation environment. Additionally, simulation results and analysis are presented in terms of frequency-voltage characteristics and fine tuning frequency response. Finally, the use of an empirical model of VCO operating-point is briefly described.

Chapter 4 initially discusses conventional fault detection methods with regard to error inducing events like TSON faults. After that, it introduces the proposed methodology of fault-testing schemes based on SEROs. Simulation results and analysis are then provided for conventional and proposed SERO-fault detecting architectures with focus on leakage tolerant TSON fault detection, adaptable threshold regulation and built-in current sensor performances. Finally, the scheme is validated by making comparison with testing methods in literature.

Chapter 5 finally concludes the outcome of this work providing insight for the scope of future work.

Chapter 2

Review of Voltage Controlled Oscillators

This chapter briefly provides a review of the theory of voltage controlled oscillators including VCO specifications and categories like LC and ring oscillators. Then, literature study is provided for single-ended ring oscillators and their adaptations. Finally, issues related with operating-point models necessary for oscillator design are addressed.

2.1 Fundamentals of VCO Operation

A simple oscillator produces a periodic output, usually a voltage. So how can a circuit oscillate? Consider a feedback system in Figure 2.1 with transfer function H(s). In order for steady oscillation to occur, the circuit must satisfy with Barkhausen criteria:

$$|H(s)| \geq 1 \tag{2.1}$$

$$\angle H(s) = 180^0 \tag{2.2}$$

These conditions are necessary but may not be sufficient to ensure oscillation [6]. Usually the loop gain of the system is twice to three times the required value [7].

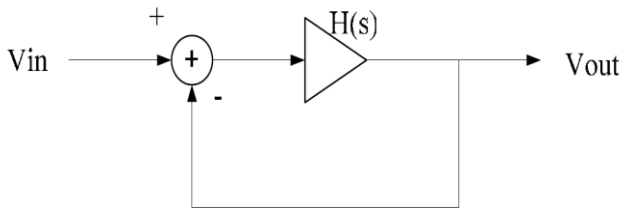


Fig. 2.1: Simple feedback system

The VCO is a useful circuit because its oscillation frequency can be set to a desired value. The governing equation for a VCO is given in (2.3), where f_O is the center frequency (operating-point), K_{VCO} is the gain of the VCO that controls how much a change in the control voltage will change the VCO's frequency. V_{ctrl} is the input voltage to the VCO that sets it to the desired operating-point. The ideal relation of oscillating frequency and gain with the control voltage is shown in Fig. 2.2.

$$f_{VCO} = f_O + K_{VCO}V_{ctrl} \tag{2.3}$$

CMOS oscillators are typically implemented as ring oscillators or LC oscillators, though there are many other types of oscillators. One advantage of ring and LC oscillators is that they can be easily modified to be able to change the operating-point for a given control voltage, thus making them prime candidates for VCOs.

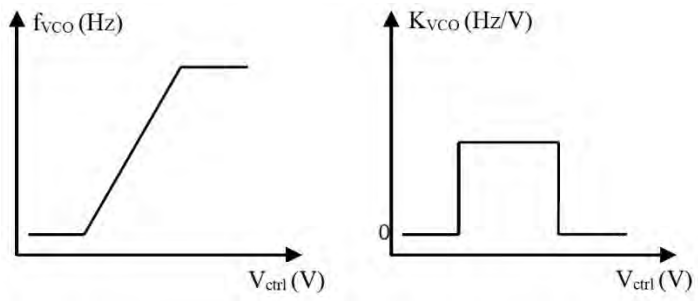


Fig. 2.2: VCO frequency transfer function [4]

2.2 Important VCO Specifications

When choosing a VCO architecture and topology, there are many important characteristics which must be taken into account. The relative importance of these characteristics usually depends on the target application. The characteristics can be placed into different categories. In the noise category, there are jitter, phase noise (PN) and figure of merit (FoM). In the frequency category, there are tuning range, the maximum operating-point and the effect of process and temperature variations on the operating-point. In the power category, there are static and dynamic power consumption. Finally in the manufacturing category: ease of integration with digital CMOS circuitry, and again, the effect of process variations.

2.2.1 Phase Noise and Jitter

A vital design concern in VCOs is the PN in frequency domain, corresponding to jitter in the time domain. Phase noise is defined as the noise that is associated with phase fluctuations in the oscillating signal. The output of an ideal sinusoidal oscillator is of the form given in (2.4) where A is the amplitude, f_{VCO} is the oscillation frequency and φ is an arbitrary phase reference.

$$V_{out}(t) = A \cdot \cos(2\pi f_{VCO} t + \varphi) \tag{2.4}$$

However, the output of a practical oscillator will be of the form given in (2.5), where A(t) and f(t) are now functions of time due to internal and external noise sources.

$$V_{out}(t) = A(t) \cdot \cos(2\pi f_{VCO} t + \varphi(t)) \tag{2.5}$$

The PN is observed as a noise spectrum in the frequency domain, spreading out in either side of the oscillation frequency as sidebands as shown in Fig. 2.3. The single sideband (SSB) phase noise is measured in dBc/Hz at a given frequency offset (usually 1MHz) from the center or operating frequency of oscillation by equation (2.6) [4].

$$\mathcal{L}\{\Delta f\} = 10 \cdot \log\left[\frac{P_{sideband}(f_O + \Delta f, 1Hz)}{P_{carrier}}\right] \tag{2.6}$$

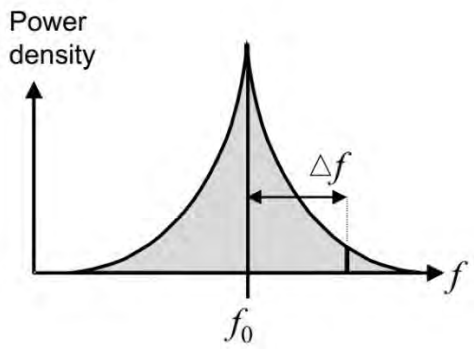


Fig. 2.3: Illustration of Phase Noise [4]

If the VCO is used in a wireless application, the phase noise can cause adjacent channels to be down-converted into the desired signal band. If the VCO is used to sample data, the jitter will affect the sample point and could degrade the signal-to-noise ratio (SNR).

2.2.2 Figure of Merit (FoM)

The performance of VCOs is difficult to compare as they feature different operating-points, power consumption and phase noise over offset frequency. A widely accepted figure of merit has been introduced in [8]:

$$\mathrm{FoM} = \mathrm{PN}\{\Delta f\} - 20\log\left(\frac{f_{VCO}}{\Delta f}\right) + 10\log\left(\frac{P_{dc}}{1\mathrm{mW}}\right) - 20\log\left(\frac{\mathrm{FTR}}{10}\right) \quad (2.7)$$

where, $\mathrm{PN}\{\Delta f\}$ is the single sideband PN at offset frequency Δf from oscillation frequency f_{VCO}, P_{dc} is the supply power and FTR is the frequency tuning range. The performance of a VCO is regarded to be better with a more negative value or higher absolute value of the FoM.

2.2.3 Characteristics of Operating-Point

The characteristics related to the operating-point of a VCO are the tuning range, the maximum operating-point and the predictability of the operating-point over process and temperature variations. The tuning range of a VCO is the range within which the operating-point can be regulated for stable operation. For example, if the operating-point of a VCO can be varied from 1.8 GHZ to 2.0 GHz, it would have a tuning range of 0.2 GHz (or 10.5% with respect to the midpoint of the range). The tuning range can be important for two reasons. First, if the VCO is to be used in a system which has a large possible range of incoming frequencies, the tuning range should encompass them. This might occur in a chip which is designed to work with multiple standards. The second reason tuning range is important is related to the predictability of the VCO i.e. how close the actual operating-point will be with respect to the designed specification, as it can vary substantially due to process variations. Therefore, if the operating-point can vary substantially, a large tuning range is necessary so that the VCO will oscillate in the desired frequency range.

The maximum attainable operating-point of a VCO architecture is also important in high speed systems. As internet traffic increases, it is desirable to increase the serial data rate. Therefore, high-speed VCOs are needed for data recovery circuits.

2.2.4 Power Consumption

Another important characteristic of VCO circuits is the power consumption. The dynamic power of a CMOS circuit is directly related to the frequency as per (2.8) where α is the switching factor, C_L is the parasitic load capacitance and V_{DD} is the supply voltage. Switching factor or switching activity is the measurement of signal value change in terms of probability and switching density.

$$\text{Dynamic power} = \alpha C_L {V_{DD}}^2 f_{VCO} \tag{2.8}$$

Another major concern of power consumption is the static/leakage power of a digital circuit. The static power equation is given by (2.9) where $I_{Leakage}$ is the steady state leakage current of the circuit. While static power remains relatively low in digital circuits, it is a major concern along with static power in analog circuits.

$$\text{Static power} = I_{Leakage} V_{DD} \tag{2.9}$$

2.2.5 Manufacturability

To reduce overall system cost and complexity, it is often desired to design an entire system, including analog and digital circuitry, on a single chip. Therefore, the ease with which the VCO can be integrated with other circuits is important. For example, the digital circuitry can create substrate and supply noise, so it is important that the VCO be able to reject this noise. Also, the physical size of the VCO is important, as a larger VCO will correspond to a larger die size, which will correspond to a higher cost.

2.3 LC-based Oscillator

A general LC-VCO consists of a passive LC resonance tank and an active element to compensate for the losses of the resonator. The active element is constructed as an amplifier which can be configured in single-stage or differential mode, the latter being more popular [9]. The capacitor, which is dependent on the input voltage, is associated with tuning the oscillation of the circuit and the frequency of oscillation is given by

$$\omega_c = \frac{1}{\sqrt{LC}} \tag{2.10}$$

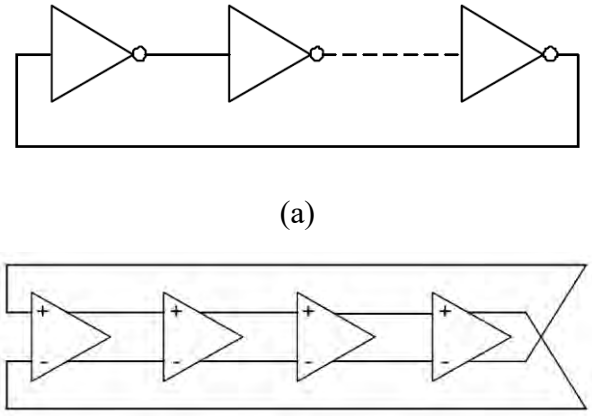
The inductor in LC oscillators has allowed the attainment of low levels of PN and power consumption over the years, but with several limitations when implemented with standard complementary metal-oxide-semiconductor (CMOS) processes [10]. It is very difficult to obtain a good quality factor (Q) for the inductor which is essential in determining the PN contributions. Quality factor of an inductor is defined as the ratio of its reactance to resistance for a given frequency and indicates the efficiency. Although inductance and resistance are constant at low frequencies, for high frequency, the Q degrades due to the ohmic loss of the spiral inductors [11].

2.4 Ring Oscillator (RO)

A ring oscillator consists of a chain of inverting amplifiers, or delay stages, in a ring structure where the output is fed back into the input. Its basic operation relies on the principle of propagation delay where the oscillating signal passes twice through the chain of a RO. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the frequency of oscillation. For a given structure with N number of stages, each delay stage must provide a phase shift of π/N and the remaining phase shift of π is provided by the DC inversion. If the propagation delay of a single stage is defined as t_{pd}, the total delay can be approximated as $2Nt_{pd}$. Therefore, the frequency of oscillation f_{osc} of the total RO is given by the following equation [12]:

$$f_{osc} = \frac{1}{2Nt_{pd}} \tag{2.11}$$

Depending on the design of the delay stage, the RO topology can be categorized into two types: (i) single ended ring oscillator (SERO) and (ii) differential ring oscillator (DRO) [13]. The SERO topology consists of a chain of odd number of inverters, whereas the DRO topology can have an odd or even number of differential amplifiers. The basic structure is shown in Fig. 2.4.



(a)

(b)

Fig. 2.4: RO with (a) single-ended, and (b) differential delay stages [14]

Based on the output voltage swing, the output of SERO compared to DRO is always saturated i.e. the output voltage always reaches the supply rail. As a result, the SERO shows better PN performance and power consumption compared to DRO for the same number of delay stages. The differential structure also adds complexity and space requirement to design compared to the single-ended structure. The use of SERO over DRO, therefore, is a better choice for vast number of applications.

2.5 RO vs. LC-VCO

When choosing a VCO architecture, one must determine the specifications related to the VCO characteristics described above and then decide whether a ring or LC VCO would better suit the application, as they each have their strengths and weaknesses.

2.5.1 Phase Noise

Phase noise is often the most important specification that must be met when choosing a VCO architecture. If excellent phase noise characteristics are required, an LC VCO will usually be necessary. Two of the main parameters related to phase noise are the attainable quality factor (Q) of the oscillator and the oscillator's ability to reject supply and substrate noise. The quality factor, Q, of an oscillator is related to the loss of the circuit, and a common definition is given in (2.12) [14].

$$Q = 2\pi \frac{\text{energy stored}}{\text{energy dissipated/cycle}} \tag{2.12}$$

An LC oscillator will have a higher Q than RO. This is because in an ideal LC oscillator, the energy will transfer between the inductive and capacitance elements with no loss, resulting in an infinite Q. In a practical LC oscillator, there are losses associated with each element, such as series resistance losses in the inductor, but energy still switches between the two reactive elements. However, in a ring oscillator, the energy is stored in the equivalent capacitance of the next stage, and the energy is fully charged and then discharged every cycle. As shown by the denominator of (2.12), this characteristic substantially reduces the Q. Typical Q values for a ring oscillator are about 1.3 to 1.4 [15]. The Q of an LC tank can be about an order of magnitude higher [16].

A second reason why ROs have poor PN performance is observed by analyzing the oscillator output. The effect of injected noise on phase depends on the point in the cycle at which the noise is injected [17]. This is shown in Fig. 2.5. When the impulse is during the peak, there is a shift in the amplitude of the output signal while the phase remains the same. When the impulse is during the transition period, there is a phase shift that persists over time. This is a problem in ring VCOs because the device noise is the highest during transitions, which is the worst case scenario in terms of PN performance.

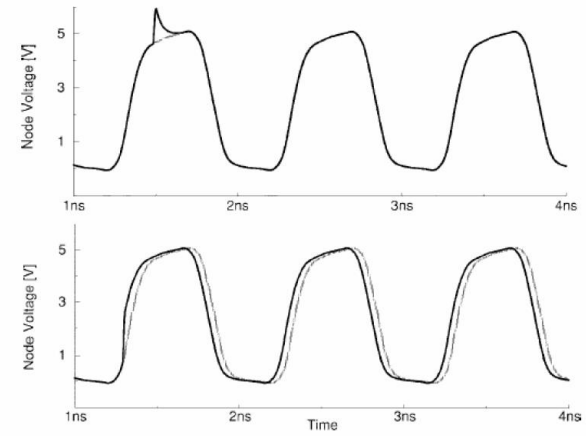


Fig. 2.5: Effect of noise impulse on oscillator output during peak and transition [14]

2.5.2 Maximum Operating-Point

An LC tank has higher maximum attainable operating-point compared to a RO. As shown in (2.10), the oscillation frequency of an LC tank is inversely proportional to the square root of inductor and capacitor. The value of these parameters can be made extremely low, and hence, the frequency of the oscillator very high. The maximum operating-point of a CMOS RO is much lower.

2.5.3 Tuning Range

A high tuning range is often required, whether to account for process variations or to work with multiple standards. A RO should be utilized to obtain high frequency tuning range. From (2.11), it can be seen that the RO frequency depends on the number of stages N and the propagation delay of each stage. A more detailed expression of the operating-point will be discussed in section 2.8 which will show that there are numerous parameters which can control the frequency of a RO. Meanwhile, the only parameter that is typically varied in a monolithic LC tank is the capacitance of the varactor. This tends to result in a lower tuning range percentage compared to RO [18].

2.5.4 Power Consumption

The use of inductors in LC tanks results in a very high power demand by the oscillator compared to a RO. The leakage power of a CMOS RO is very low while the dynamic power exists only for the time period when both PMOS and NMOS transistor networks are ON to create a shorted path from supply to ground.

2.5.5 Manufacturability

There are two issues related to the manufacturability of the VCO. These are how easily the VCO can be integrated into a monolithic solution, and how much the center frequency will vary over process parameters. A RO is preferred over LC oscillator if die area is a large concern. Monolithic inductors can occupy a large area, which corresponds to higher cost [19]. However, the center frequency of a RO can also vary more than an LC tank due

to process variations. Despite of this larger variation, ROs are still more likely to be used at the desired frequency because of their wide tuning range.

Table 2.1 summarizes the relative strengths of ROs and LC oscillators by marking ✓ to show the oscillator with the superior performance.

Table 2.1: Summary of Ring vs. LC oscillator

	Ring Oscillator	LC Oscillator
Phase Noise		✓
Maximum Frequency		✓
Tuning Range	✓	
Power Consumption	✓	
Manufacturability	✓	

2.6 CMOS Inverter-based Single-Ended RO (SERO)

A basic 3-stage CMOS inverter based RO is shown in Fig. 2.6 where the parasitic output capacitances are included. It can be said on the basis of inverter controlled operation, when the input of the first stage is rising, the output of the third stage will be falling. Since the falling output is fed back to the input, it changes the input to falling, but not immediately because of the propagation delay incurred at every stage. After this first half cycle, the opposite scenario is realized when the input starts falling and in this way an oscillation is generated.

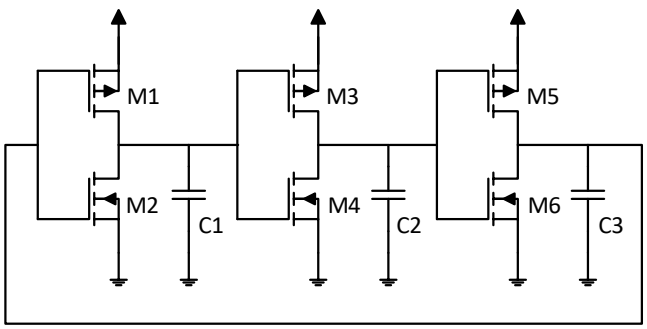


Fig. 2.6: Conventional SERO

The oscillation of a RO can be analyzed with respect to gain and transfer function of each stage. A typical RO consists of multiple gain stages within the loop. The minimum

gain required in each stage can be easily derived from the transfer function of each stage and the Barkhausen criteria. The transfer function of each stage in the conventional SERO is given by (2.13), where A_O is the minimum gain required per stage [7]. Neglecting the effect of the gate-drain overlap capacitance, the loop gain of the system is then obtained as in (2.14).

$$A(s) = -\frac{A_O}{1 + \frac{s}{\omega_O}} \tag{2.13}$$

$$H(s) = -\frac{{A_O}^3}{\left(1 + \frac{s}{\omega_O}\right)^3} \tag{2.14}$$

The system oscillates when the total phase shift equals 180º, where each stage contributes 60º. The frequency at which the oscillation occurs is given by:

$$\tan^{-1}\frac{\omega_{osc}}{\omega_O} = 60^0 \tag{2.15}$$

Solving (2.15) for ω_{osc}, the expression of the oscillating frequency obtained is:

$$\omega_{osc} = \sqrt{3}\omega_O \tag{2.16}$$

The minimum voltage gain per stage is then evaluated using the Barkhausen criteria in (2.17) where the magnitude of the loop gain at ω_{osc} is equal to unity [7]. Using (2.16) and (2.17), the value of A_O is approximately 2.

$$\frac{{A_O}^3}{\left[\sqrt{1^2 + \left(\frac{\omega_{osc}}{\omega_O}\right)^2}\right]^3} = 1 \tag{2.17}$$

Therefore, a three stage RO can oscillate at $\sqrt{3}\omega_O$, where ω_O is the 3-dB bandwidth of each stage, and requires a minimum gain of 2 per stage. Higher number of stage will result in a lower gain required per stage, but at the cost of lower frequency of oscillation.

2.7 Adaptations of Single-Ended Ring Oscillators

Several SERO architectures have been proposed over the years customized for specific applications, which can be divided into different categories based on their delay stage structure [20]. This section discusses their relative merits and compares their performances.

2.7.1 Current Starved RO

A second conventional SERO topology suitable particularly for low power applications is the current starved VCO (CS-VCO). It consists of the basic inverter stages along with PMOS current sources and NMOS current sinks which are biased at the desired voltage. This bias voltage can be generated by a separate biasing circuit. Various CS architectures have been presented [20-24], each utilizing a different biasing technique. The single delay stage structure of a traditional CS-VCO is shown in Fig. 2.7 which serves as the unit block of cascaded architectures. Transistors M5-M7 form the bias circuit and the frequency is tuned by varying the gate voltage V_{ctrl} of M7. Current mirror technique is used to provide the current generated by the bias circuit to all the stages. As the resulting current in the circuit is directly controlled by a separate voltage, it can be limited to a desired value to ensure low power consumption. Additional current source and current sink sections may also be employed to increase the equivalent resistance and further regulate the current. In this way, the circuit is starved of current and better management of power can be provided. However, the decrease in current eventually has a detrimental effect on frequency. Moreover, the topology also suffers from low and nonlinear tuning range.

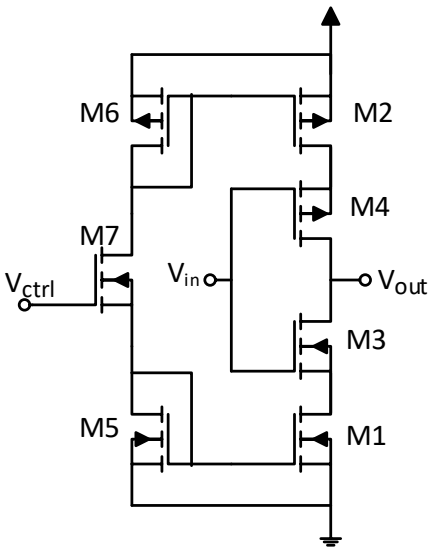


Fig. 2.7**:** CS-VCO delay stage serving as the unit block of multistage structure [20]

The propagation delay of CS-VCO is derived in [25] and observed to be proportional to V_{DD}. Hence, compared to the basic inverter based RO, the frequency of CS topology is inversely proportional to V_{DD}. The CS architecture also faces a drawback in terms of non-linearity. The linear variation of bias current with respect to the control voltage depends on the region of operation of M5. Therefore in order to achieve a linear relation between f_{osc} and V_{ctrl}, M5 should be operated in the saturation region until the control voltage reaches V_{DD}. Rajahari et. al. [26] have provided a minimum width ratio for M6 and M5 to ensure that this condition is fulfilled. The equation is given by:

$$\frac{W_{M6}}{W_{M5}} = \frac{K_{M6}}{K_{M5}}\left[\left(\frac{V_{DD} - V_t}{V_{bias(min)} - V_{DD} - V_t}\right)^2 - 1\right] \tag{2.18}$$

where $K = \frac{\mu C_{ox}}{L}$ and $V_{bias(min)}$ is the minimum drain voltage of M6.

Several other CS-SEROs are presented in [27] which simplify the unit block to improve the area overhead of the circuit and analyze the performance in terms of key features. Comparison with existing circuit structures demonstrate significant trade-offs between frequency and power overhead, and between phase-noise and frequency bandwidth. While power-delay product (PDP) addresses the frequency-power trade-off, a new proposed parameter in [27] known as the phase-noise-bandwidth product (PNBP) addresses the trade-off between phase-noise performance and frequency tuning range.

2.7.2 Negative-Skewed RO

Lee et. al. [28] have proposed a modified inverter based RO where the input of the PMOS device has a negative delay element placed in front of it. As a result, when the output of a stage changes from low to high, the PMOS of that stage turns on before the NMOS turns off. This speeds up the operation of the RO and achieves a higher maximum frequency compared to that of the conventional structure. Since the topology supports a larger period of time when both MOSFETs are on, there is an increased static current which raises the power consumption of this architecture. Additionally, the control of the delay demands deliberation because if it becomes significantly higher, the speed of the circuit eventually degrades. Unlike the basic CMOS structure, the input of the PMOS in the structure is not derived from adjacent cell outputs. For example, the PMOS of stage 4 is driven by the output of stage 1. The output of stages 1 and 3 are similar. So when input of stage 1 changes from high to low, output of stages 1 and 3 are rising. Since the output of stage 1 increases before that of stage 3 due to propagation delay, the PMOS of stage 4 is switched off prior to NMOS turn-on. Negative skewed scheme can also be implemented with NMOS gate inputs. To satisfy the requirements, the minimum number of stages for a negative skewed RO is determined to be 5. An example of a five-stage negative skewed VCO is demonstrated in Fig. 2.8 where the circuit offers a 62% higher operating frequency compared to the design point of basic SERO.

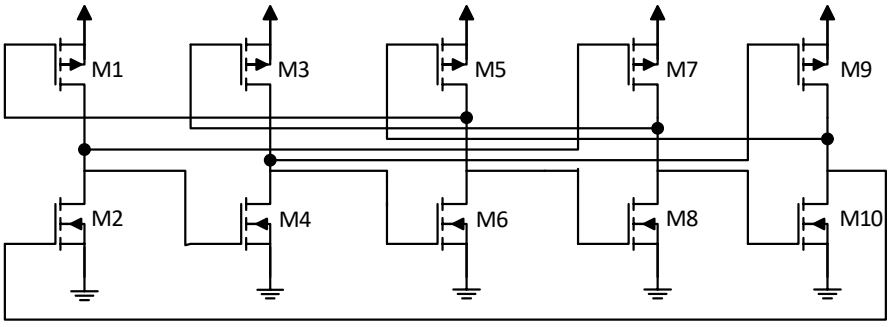


Fig. 2.8: Five-stage RO using negative skewed scheme [28]

2.7.3 Transmission-Gate (TG) RO

Oscillators with a wide tuning range can fulfill a fundamental need often required in the communication world. Different methods exist to increase the range of frequency

tuning, as mentioned in [29], but at the cost of greater power consumption and chip area. To tackle these challenges, Sheu et. al. [29] described a design of wide tuning range ring oscillator using TG at the output of each stage. The tuning of the frequency is achieved by varying the parasitic load capacitance through the control voltage V_{ctrl}, which is applied at the NMOS of the TG as shown in Fig. 2.9. Summation of the drive voltages being applied to NMOS and PMOS of the TG should be equal to the supply voltage. Compared to the transmission gate based design proposed in [30], the circuit provides symmetric paths for both charging and discharging cycles, eliminating the variation in duty cycle in response to the regulation of the control voltage. Joeres et. al. [31] compared both CS and TG based ROs and shows that the TG scheme gives a wider and linear tuning range.

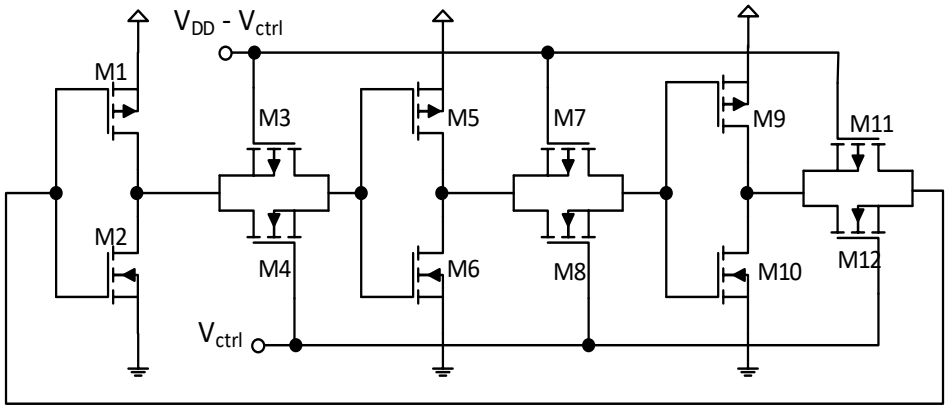


Fig. 2.9: Three-stage transmission gate supported RO [29]

2.7.4 RO using Bulk Voltage Effect

The adjustment of supply and bias voltages have a direct impact on the power consumption of electronic circuits. Therefore, in order to operate in low voltages, one of the adopted techniques could be reducing the threshold voltage which can be achieved by applying a direct biasing voltage to the bulk terminal of MOSFETs. A quadrature output SERO is proposed in [32] which exploits the bulk voltage effect where a control voltage is applied to the bulk terminals of both PMOS and NMOS of the inverter circuit to manipulate the threshold voltages. This provides the best result in terms of low voltage requirements and achievement of a suitable FoM compared to a structure which uses biasing either one of the MOSFETs.

2.7.5 Symmetrical Even-phase Outputs SERO

As mentioned before, the conventional SERO cannot provide symmetrical even-phase outputs since they consist of an odd number of inverting stages. The circuit proposed in [33] provides this feature with a four-stage SERO and its circuit is shown in Fig. 2.10. The transistor M_{n1} provides the required phase shift to get the desired quadrature output. Transistors M_{n1} and M_{p1} set the gain of the VCO and the frequency tuning is achieved by the control voltage driving the device M_{p3}. By increasing the control voltage, the operating frequency of the circuit decreases i.e. the circuit has a negative linear relation between the control voltage and frequency. By replacing the PMOS M_{p3} with an NMOS M_{n3}, a positive linear relation can be obtained between the frequency and the control voltage. A modified circuit involving additional NMOS and PMOS switching transistors for a band switch technique is also proposed by the author which can operate at two different frequency modes (low and high) with the help of a control switch. Due to the band switch technique and full-swing characteristics, the circuit improves noise performance and signal to noise ratio (SNR) with a wide tuning range. SNR is the ratio of signal power to noise power and a high SNR means better noise performance i.e. low noise in the output signal. The topology is suggested to be beneficial in the field of consumer electronics, communication and medical appliances.

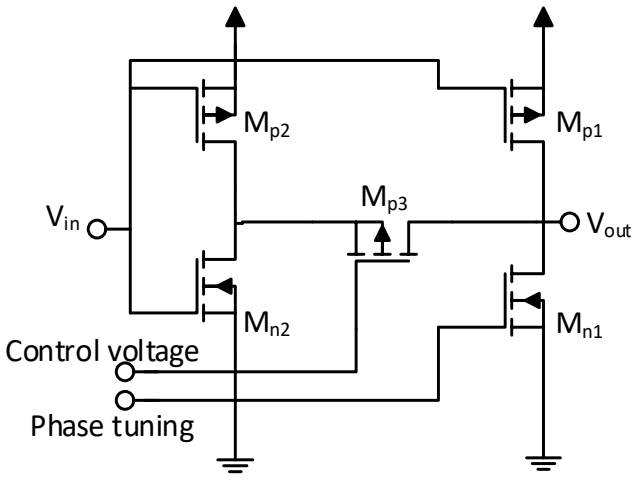


Fig. 2.10: Delay cell for symmetrical even-phase output SERO [33]

2.7.6 NMOS-sink CS-VCO

Conventional CS-VCO uses both current sources and sinks where bias voltages, as mention earlier, are provided through current mirror circuits. Suhas et. al. in [34] adapts the basic CS circuit by using only the NMOS current sinks in a three-stage CS-RO. The control voltage is directly applied to the first NMOS sink instead of using current mirrors. The renovated topology simplifies the existing design and improves power consumption and area penalties significantly providing wide and linear frequency tuning. Keeping the control voltage fixed, the frequency is rather tuned by varying the supply voltage which contributes to the linear frequency versus voltage curve due to the smaller drain-source capacitance compared to gate-source capacitance. In relation to multiple reported oscillators in 180nm technology, the proposed circuit is observed to demand a low power rating of 0.598mW with 176.4% tuning range which was achieved when control voltage was fixed at 2.5V and the supply voltage was varied from 0.6V-2.5V. The properties of the oscillator is appropriate for microwave applications.

2.7.7 RO using STSCL Load Device

Goyal et. al. [35] describes a three-stage RO which implements a sub-threshold source coupled logic (STSCL) PMOS load device. STSCL allows MOS gates to operate with ultra-low voltages by placing them in the sub-threshold region where the current density is very low. As a result, the power dissipation is reduced and the circuit can be used for low power applications. However, it leads to the requirement of a scaled-down supply voltage which could result in a degradation of output voltage swing. To overcome this problem, the PMOS load is converted to a high resistance load by shorting bulk and drain terminals together. Additionally, the circuit uses a pseudo NMOS architecture [36] with a single NMOS sink. The bias voltages are provided by a current mirror technique as presented in Fig. 2.11. Drawbacks of this design involve a reduced frequency of oscillation and a subsequent curtailed tuning range. With a supply rail of 1V in 180nm technology, the STSCL-based design requires a power of only 6.75uW at 123.9MHz compared to the figure of 206uW at 1220.50MHz as achieved by a conventional CS-VCO. Such low power ROs are suitable for biomedical electronics.

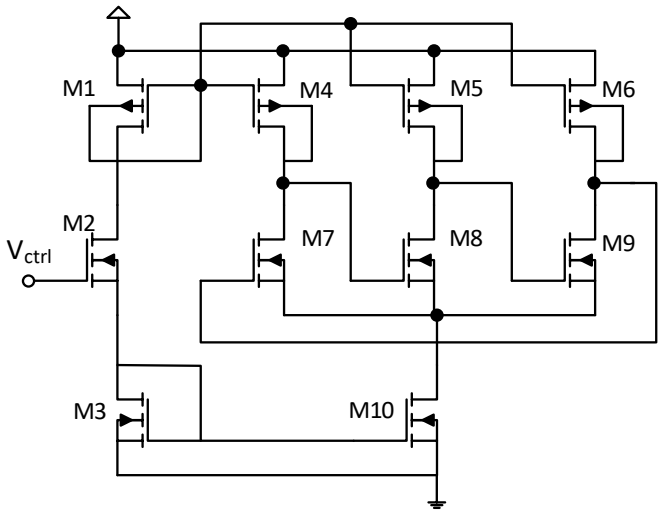


Fig. 2.11: Multistage oscillator with source-coupled logic load [35]

2.7.8 Hybrid SEROs

Hybrid ring oscillators entail the combination of basic inverter stages, CS schemes and negative skewed techniques which can be associated to combine their benefits and compensate for their limitations while making performance trade-offs.

2.7.8.1 Combined RO

It was described in section I that the frequency of inverter based ROs is proportional to the supply rail and that of CS-VCOs has a reciprocal relationship with the supply voltage. Therefore, a variation in the supply voltage due to noise may alter the frequency of oscillation affecting the stability of the transceiver. In order to improve the frequency stability in this regard, multiple (3, 5 and 7) stages are combined in a hybrid oscillator which includes both of the aforementioned oscillator units [37]. The design ultimately consists of basic CMOS inverters for the odd stages and CS-inverters for the even stages. It leads to an improvement of reliability where frequency deviation of less than 2% was obtained with respect to variation in the power supply. The major drawback of the combined structure is the degradation of maximum oscillation frequency.

2.7.8.2 CS-Skewed RO

Nayak et. al. in [38] adapts the CS and the negative skewed schemes simultaneously to propose the CS Skewed RO. Two seven-stage ROs were presented where one chain

uses NMOS skewed units while the other uses PMOS skewed blocks. The structure has to make a calculated trade-off between frequency and power consumption, as the used chains have the possibility of adversely affecting these features. The authors measure a crucial parameter, the power delay product (PDP) of the circuit. PDP is the product of the power consumption and propagation delay of the circuit which is used in to analyze circuit performance in terms of energy efficiency. It measures the energy consumed by the circuit per switching event. The result shows more than 30 and 50% improvement in terms of PDP for NMOS skewed and PMOS skewed respectively, compared to the benchmark of individual CS and skewed topologies. Good performance was also observed against variations in operating conditions like temperature and supply voltage. The structure is useful in IoT system applications.

2.7.8.3 Combined-Skewed RO

Simultaneous use of basic inverters, CS units and skewed stages can lead to a combined skewed RO as described in [39]. A five-stage RO is proposed, as presented in Fig. 2.12, where the front and the ultimate stage consists of the inverter units, the three stages in the middle consist of CS inverters, while gates of all the PMOS loads are negative skewed. The resulting circuit, in comparison with the combined RO structure, improves the frequency of oscillation significantly (3.31GHz compared to 960MHz) and also maintains good frequency stability with respect to supply voltage and temperature variations.

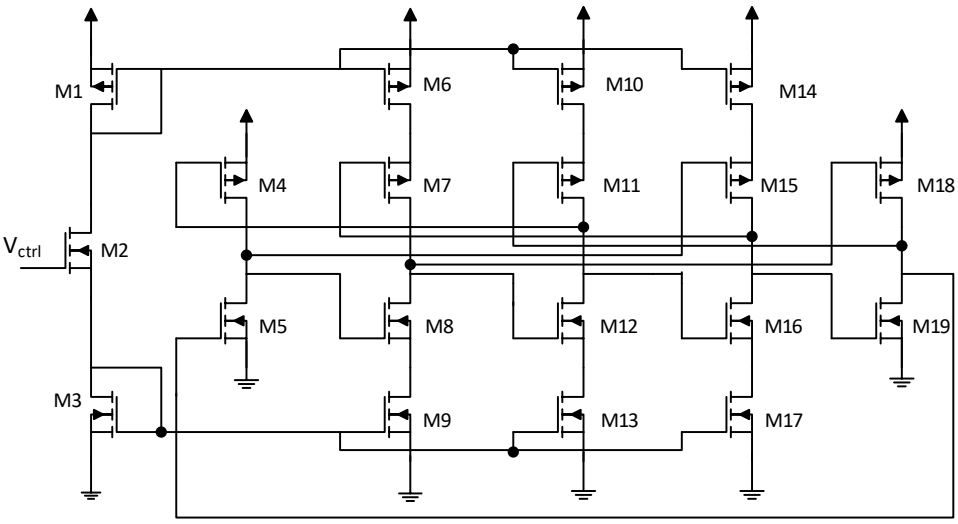


Fig. 2.12: Multistage skewed RO using three types of units [39]

2.7.9 LC based SEROs

Although LC tuned oscillators and ROs belong to different categories offering unique advantages, inductors and capacitors can also be implemented in ring structures to attain their benefits. Ring architectures which also include load tanks and passive components are discussed in this section.

2.7.9.1 RO using Inductor Peaking

Four three-stage ROs with peaking inductors are described in [40] where the circuits employ inductive loads along with PMOS loads in each of the delay stages of a pseudo NMOS RO, as shown in Fig. 2.13. The modification is exploited to obtain an ultra-wide tuning range and good PN performance. It leads to the realization of two VCOs which show a tuning range of 189% and 196% along with 195.3 and 194.7 FoMs respectively. While the size of the inductor influences the frequency tuning, the quality factor plays the dominating role on the determination of PN. Additionally, the circuit is observed to give a significantly higher power consumption compared to other works.

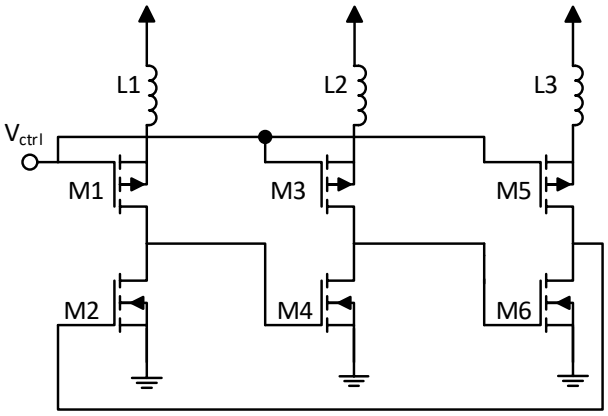


Fig. 2.13: Three-stage RO using peaking inductors [40]

2.7.9.2 Quadrature RO using Series LC Tank

A four-stage RO with series LC tank at the output node of the individual stages is described in [41]. Each inverter stage with the series LC tank produces a 90 degree phase shift, which results in the accumulation of the required phase shift for oscillation. The circuit, therefore, provides symmetrical even-phase outputs. With the inclusion of low-Q inductors, the chip area and PN performance are regulated while maintaining a good

tuning range. The frequency tuning of the topology is controlled by the capacitors in the output tanks (C_1-C_4) as shown in Fig. 2.14.

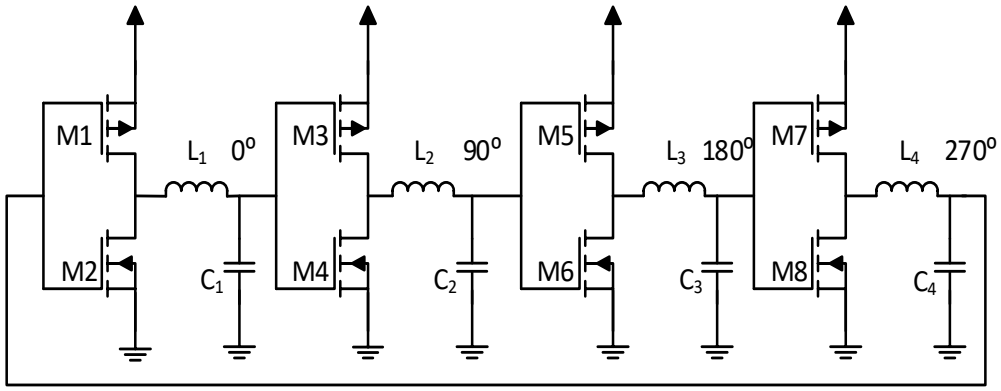


Fig. 2.14**:** Quadrature RO using series LC tanks [41]

2.7.10 Summary

The choice of an SERO architecture for a specific application is dependent on its performance and so detailed analysis is important. Study demonstrates that few moderately modified SEROs can enhance the performance in terms of a single feature while degrading another characteristic. Hybrid oscillators were observed to improve the operating-point stability and LC based ring oscillators improved noise performance, operating-point and tuning range while sacrificing the performance in terms of power requirement.

2.8 Approximate Operating-Point Models

The expression of the operating-point in a RO is given by (2.11), which shows that the frequency is inversely proportional to the number of delay stages N and propagation delay t_{pd} at each stage. The propagation delay t_{pd} is an average of the high-to-low and low-to-high propagation delays, t_{dHL} and t_{dLH} respectively. Equation (2.11) can then be written as in (2.19).

$$f_{osc} = \frac{1}{N(t_{dHL} + t_{dLH})} \tag{2.19}$$

Therefore, in order to analyze and estimate the operating-point, it is essential to correctly model the propagation delays t_{dHL} and t_{dLH} [42]. Two conventional methods exist to determine an approximate delay equation, each modeling the CMOS inverter circuit differently. In the first method, the transistors are modeled as current sources with a constant current supply which charges and discharges the load capacitance C_L [43]. In the second method, the transistor is modelled as a resistor and an equivalent RC circuit is solved for the delay expression [44]. The point at which the delay is calculated can also vary and results in a similar equation with a different coefficient value. The propagation delay can be calculated when the output is at either 50%, 90% or 100% level of the supply voltage. Although the delay is calculated at the 50% level conventionally [45], as shown in Fig. 2.15, some equations mentioned in literature [14, 46] have considered the 90% and 100% levels.

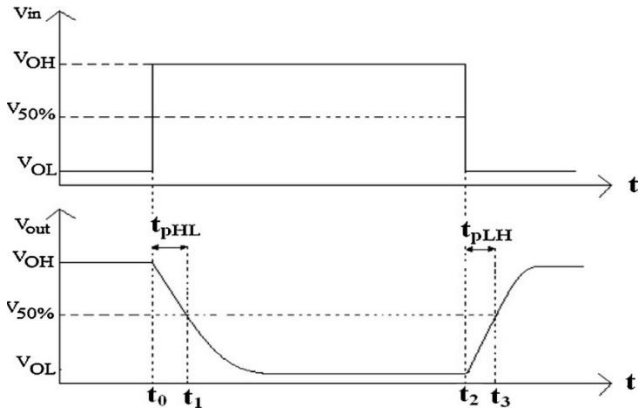


Fig. 2.15: Propagation delay calculation at 50% level [45]

These analyses can lead to 5 different operating-point equations for a single circuit. Moreover, the equations are based on the assumption that the PMOS to NMOS width ratio, W_p/W_n is 2.

2.8.1 Current Source (CS) Model and Delay at 50%

As mentioned before, one way to model the propagation delay is by assuming the transistors as current sources which charge and discharge the load capacitance. The charging and discharging current equations are then given by [42]:

$$C_L \int_0^{\frac{V_{DD}}{2}} dV_{out} = \int_0^{t_{dLH}} I_p dt \tag{2.20}$$

$$C_L \int_{V_{DD}}^{\frac{V_{DD}}{2}} dV_{out} = -\int_0^{t_{dHL}} I_n dt \tag{2.21}$$

where, I_n and I_p are saturation currents of NMOS and PMOS transistors, respectively. The propagation delays t_{dLH} and t_{dHL} are obtained as (2.22) and (2.23). Assuming the PMOS to NMOS width ratio $W_p/W_n = 2$ and, hence, $I_n = I_p = I_s$, the resultant expression of operating-point is obtained in (2.23), where I_s is the current through each delay stage.

$$t_{dLH} = \frac{V_{DD} C_L}{2 I_p} \tag{2.22}$$

$$t_{dHL} = \frac{V_{DD} C_L}{2 I_n} \tag{2.23}$$

$$f_{osc} = \frac{I_S}{N V_{DD} C_L} \tag{2.24}$$

2.8.2 CS Model and Delay at 90% Level

For the delay calculation at 90% level, the integral limits are changed from $V_{DD}/2$ to $0.9V_{DD}$ and $0.1V_{DD}$ in (2.20) and (2.21), respectively. The two propagation delay expressions then obtained are given by (2.25) and (2.26). The resultant operating point expression is given by (2.27).

$$t_{dLH} = \frac{0.9 V_{DD} C_L}{I_p} \tag{2.25}$$

$$t_{dHL} = \frac{0.9 V_{DD} C_L}{I_n} \tag{2.26}$$

$$f_{osc} = \frac{I_S}{1.8 N V_{DD} C_L} \tag{2.27}$$

2.8.3 CS Model and Delay at 100% Level

For the 100% level, the delay is calculated when the output reaches the voltage rails, V_{DD} or 0. In a similar method as before, the integral limits are now from 0 to V_{DD} and V_{DD} to 0 in (2.20) and (2.21), respectively. The propagation delays then obtained are given by (2.28) and (2.29) which leads to the operating-point expression in (2.30). This is the most common equation in literature.

$$t_{dLH} = \frac{V_{DD} C_L}{I_p} \tag{2.28}$$

$$t_{dHL} = \frac{V_{DD} C_L}{I_n} \tag{2.29}$$

$$f_{osc} = \frac{I_S}{2N V_{DD} C_L} \tag{2.30}$$

2.8.4 RC Models

The inverter can also be modelled as an RC network to obtain the propagation delay. Suppose, C_L is being charged to a voltage V_{out} from supply voltage V_{DD} when $V_{in} = 0$, as shown in Fig. 2.16. The operation of the network is described by the following differential equation [47]:

$$C_L \frac{dV_{out}}{dt} + \frac{V_{out} - V_{in}}{R_p} = 0 \tag{2.31}$$

where, R_p is the equivalent PMOS resistance. The solution to the differential equation is given by:

$$V_{out} = \left(1 - e^{-\frac{t_{dLH}}{R_p C_L}}\right) V_{DD} \tag{2.32}$$

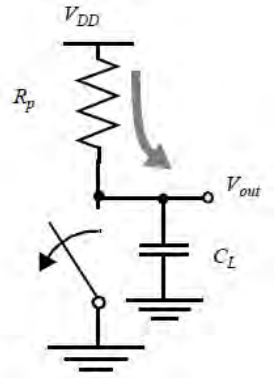


Fig. 2.16: RC model of CMOS inverter at $V_{in} = 0$ [47]

For calculating delay at 50% voltage level, $V_{out} = 0.5V_{DD}$ and the expression of t_{dLH} obtained is given by (2.33). Similarly for the discharging scenario, the expression of t_{dHL} is given by (2.34), where R_n is the equivalent NMOS resistance.

$$t_{dLH} = \ln(2)\, R_p C_L \tag{2.33}$$

$$t_{dHL} = \ln(2)\, R_n C_L \tag{2.34}$$

The average on-resistances R_n and R_p can be calculated by integrating the I-V characteristic curves of the NMOS and PMOS, respectively, over the interval of interest. For example, for 50% delay calculation, the expression of R_p is given by (2.35) where λ is the channel length modulation constant for short channel devices. Assuming $\lambda = 0$, the approximate expressions of R_p and R_n are given by (3.36) and (2.37).

$$R_p = \frac{1}{-\frac{V_{DD}}{2}} \int_{V_{DD}}^{\frac{V_{DD}}{2}} \frac{V dV}{I_p(1+\lambda V)}$$

$$\approx \frac{3V_{DD}}{4I_p}\left(1 - \frac{7}{9}\lambda V_{DD}\right) \tag{2.35}$$

$$R_p = \frac{3V_{DD}}{4I_p} \tag{2.36}$$

$$R_n = \frac{3V_{DD}}{4I_n} \tag{2.37}$$

Substituting equations (2.36) and (2.37) in (2.33) and (2.34), the resulting expression of operating-point is given by (2.38) where $I_s = I_n = I_p$, assuming $W_p/W_n = 2$.

$$f_{osc} = \frac{I_S}{1.5\ln(2)NV_{DD}C_L} \tag{2.38}$$

For calculating delay at 90% voltage level, $V_{out} = 0.9V_{DD}$ in equation (2.32) and the delay expressions obtained are given by (2.39) and (2.40).

$$t_{dLH} = \ln(10)\, R_p C_L \tag{2.39}$$

$$t_{dHL} = \ln(10)\, R_n C_L \tag{2.40}$$

Following similar procedure, the resulting operating-point expression obtained is given by (2.41).

$$f_{osc} = \frac{I_S}{2\ln(10)\, NV_{DD}C_L} \tag{2.41}$$

Note that, using the RC model, the delay cannot be calculated at the 100% voltage level as the value of t_{dLH} from (2.32) evaluates to 0.

2.8.5 Sources of Inaccuracy in Approximate Models

The equations discussed above for the operating-point of a RO are approximate equations with several assumptions where many details are neglected. Therefore, the equations are not very accurate. The following points mention the reasons of approximation and inaccuracy [42, 48]:

i. The first order transistor equations are used which are not very accurate in the nanometer dimension.

ii. The load capacitor of the transistor vary at different supply voltage and transistor regions.

iii. The voltage swing is considered to be $0 \rightarrow V_{DD}$ for the first method (integral method) which is not accurate. In practical, the integral limit is lower than V_{DD} and higher than 0.

iv. The saturation currents of the transistors are considered in the equations. However, in the delay interval, the transistors may enter the linear region.

v. The currents in the equations (2.20) and (2.21) are considered to be constant and got out of the integrals, whereas they are voltage dependent.

vi. In the propagation delay equations, only the effect of one transistor is considered instead of both transistors.

2.9 Modeling of Parasitic Load Capacitance

The oscillating frequency of an SERO is inversely proportional to the load capacitance of each stage, so it is important to analyze the different components which influence this parasitic load capacitance. Figure 2.17 shows a cascaded CMOS inverter pair and the various parasitic capacitances of the MOSFETs [47]. The total load capacitance of a conventional SERO at each stage is a summation of the following components: gate-drain capacitances (C_{gd1}, C_{gd2}), diffusion capacitances (C_{db1}, C_{db2}), gate capacitances of the load stage (C_{g3}, C_{g4}) and interconnect capacitance (C_w). The expressions of these capacitances are given in Table 2.2. Table 2.3 defines the variables present in the expressions of these capacitor components.

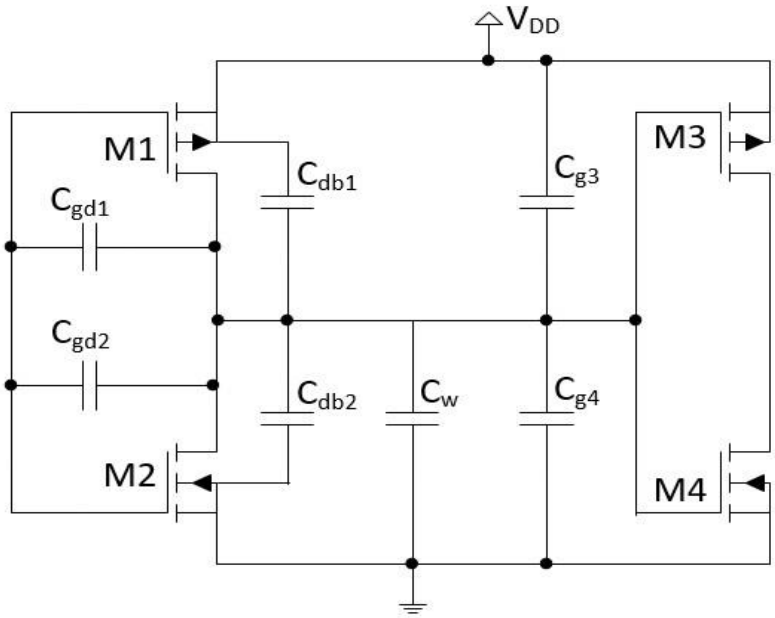


Fig. 2.17: Components of parasitic capacitances in cascaded CMOS inverter

Table 2.2**:** Expressions of parasitic capacitance components

Capacitance components	**Expression**
C_{gd1}	$2C_{GDOp}W$
C_{gd2}	$2C_{GDOn}W$
C_{db1}	$K_{eqp}A_{Dp}C_J + K_{eqswp}P_{Dp}C_{JSW}$
C_{db2}	$K_{eqn}A_{Dn}C_J + K_{eqswn}P_{Dn}C_{JSW}$
C_{g3}	$(C_{GDOp} + C_{GSOp})W_p + C_{OX}W_pL_p$
C_{g4}	$(C_{GDOn} + C_{GSOn})W_n + C_{OX}W_nL_n$
C_W	From extraction
C_L	$\sum$

Table 2.3**:** Definition of variables in parasitic components

Variable	**Definition**
C_{GDO}	Gate-drain overlap capacitance
C_{GSO}	Gate-source overlap capacitance
K_{eq}	Multiplication factor to relate the linearized capacitor value to the junction capacitance for bottom wall under zero bias condition
K_{eqsw}	Multiplication factor to relate the linearized capacitor value to the junction capacitance for side-wall under zero bias condition
A_D	Area of drain
P_D	Perimeter of drain area
C_J	Bottom junction capacitance
C_{JSW}	Side-wall junction capacitance
C_{OX}	Oxide capacitance

Chapter 3

Multimode Single-Ended Split-Load Ring Oscillator

In this chapter, the development of the proposed multimode single-ended spit-load ring oscillator architecture is discussed with description of the simulation environment. Additionally, simulation results and analysis are presented in terms of frequency-voltage characteristics and fine tuning frequency response. Finally, the use of an empirical model of VCO operating-point is briefly described.

As discussed in the previous chapter, several SERO architectures have been proposed over the years customized for specific features such as low power consumption, low phase noise, wide tuning range or high operating frequency. It has been observed that transmission-gate and inductors have been used in the load section to increase frequency tuning range. However, the regulation of control voltage in the transmission-gate based oscillator remains a difficult design issue. On the other hand, the use of inductors results in high power penalty and affects the linearity of the frequency-voltage characteristics adversely. Hence, a modified SERO topology with split-load technique has been proposed in this work for wide tuning characteristic while maintaining a cap on power penalty.

3.1 SERO with Active-Load

The proposed SERO circuit is developed by initially converting the CMOS inverter delay stage into an active-load inverter [36], where the PMOS is diode-connected and always operates in the saturation region. Diode-connected PMOS loads have been previously used in parallel symmetric loads arrangements in [20, 49, 50] to increase the oscillating frequency and improve the sinusoidal shape of the curve i.e. eliminate distortion at peaks. Transistors M1, M3 and M5 in Fig. 3.1 are the active loads of the circuit.

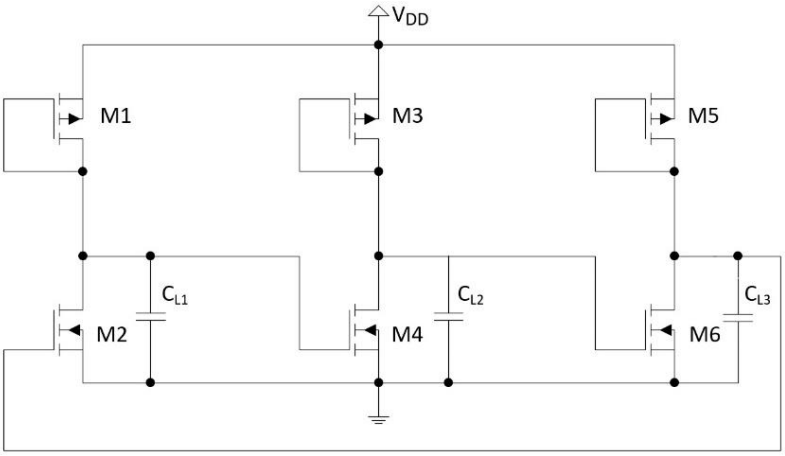


Fig. 3.1: SERO with active-load inverter

From Fig. 3.1, it can be observed that the intermediate (input) nodes do not drive the PMOS gate of the following delay stage. Therefore, the parasitic component C_{g3} in Fig. 2.17, which was discussed in the previous chapter, would be eliminated. Similarly, since the gate and drain terminals of the PMOS transistor are shorted, the corresponding parasitic component ($C_{gd1\sim3}$) may also be assumed absent. Compared to the summation of all other capacitances, the interconnect capacitance can be considered negligible [48] having minimal influence on frequency, and hence, the overall parasitic load capacitance of the first stage for the modified circuit may be given by:

$$C_L = C_{gd2} + C_{db1} + C_{db2} + C_{g4} \tag{3.1}$$

Since the total load capacitance is lowered, the overall propagation delay and eventually the frequency of oscillation of the circuit is improved. However, the major drawbacks of the circuit are significantly reduced output voltage swing and frequency tuning range. The maximum and minimum output voltages of an active-load inverter are

given by (3.2) and (3.3) where, V_{tp} is the PMOS threshold voltage, V_t is the threshold voltage of the transistors assuming threshold voltage of NMOS and PMOS are equal, and β_1 and β_2 are the conduction parameters of the two transistors where $\beta = \frac{\mu C_{ox} W}{L}$ (μ = carrier mobility, C_{ox} = oxide capacitance, W = channel width, L = channel length).

$$V_{out(max.)} \cong V_{DD} - |V_{tp}| \tag{3.2}$$

$$V_{out(min.)} = V_{DD} - V_t - \frac{V_{DD} - V_t}{\sqrt{1 + \left(\frac{\beta_1}{\beta_2}\right)}} \tag{3.3}$$

3.2 Single-Ended Split-Load Ring Oscillator (SESLRO) with Multimode Tuning

In order to mitigate the problems of the circuit in section 3.1, a parallel PMOS transistor is connected in the load section of each stage (a split-load structure) with a bias voltage V_{bias} applied at the gate terminal, as shown in Fig. 3.2.

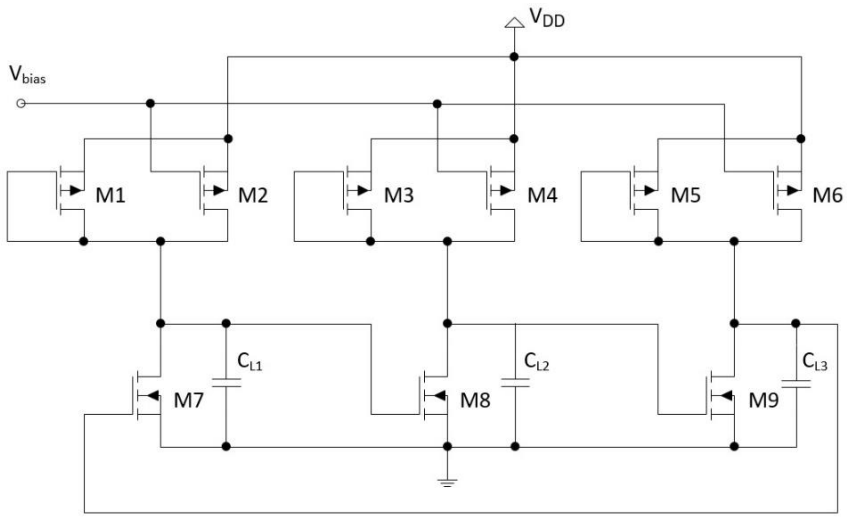


Fig. 3.2**:** Proposed SESLRO

Transistors M2, M4 and M6 work as a current source and the operating region of these transistors can be obtained from the condition of saturation region of a PMOS transistor. For transistor M2 to operate in the saturation region,

$$V_{SD2} \geq V_{SG2} - |V_{tp}| \tag{3.4}$$

From (3.4), the condition for operating in the saturation region of the current source PMOS transistors is given by:

$$V_{out} \leq |V_{tp}| + V_{bias} \tag{3.5}$$

The split-load current source transistors in the proposed circuit compensate for the loss of oscillation in the previous circuit in section 3.1 [51] and increases operating-point, as well as power requirement of the circuit due to the additional current path [52]. Since the current through a MOSFET is also influenced by the applied gate voltage, the operating-point of the circuit can be regulated through the variation of both V_{bias} and $V_{DD,}$ creating the multimode tuning operation.

The parasitic load capacitance can be analyzed in a similar way as in the previous section (3.1). The input gate capacitance components (C_{g2}, C_{g4} and C_{g6}) of transistors M2, M4 and M6 in Fig. 3.2 may assumed to be absent since they are not driven by the output of the previous stage. However, the gate-drain capacitance C_{gd} of the current source transistors will remain. The total load capacitance at the first intermediate node is given by:

$$C_L = C_{gd2} + C_{gd7} + C_{db1} + C_{db2} + C_{db7} + C_{g8} \tag{3.6}$$

Comparing (3.1) and (3.6), it can be concluded that the total load capacitance of the proposed circuit is higher than the active-load SERO. This results in an adverse effect on the oscillator's operating-point. However, the increased current in the circuit dominates over the effect of increased capacitance to cause a resultant increase in the operating-point.

3.3 Simulation Environment

Three oscillator circuits (conventional SERO, SERO with active-load and SESLRO) are simulated in 90 nm technology using Cadence Virtuoso platform. The results are divided into three parts:

i. The circuits are first simulated without considering parasitic-effect and compared in terms of frequency tuning range and output voltage swing.
ii. Next, the circuits are simulated with capacitors connected at the output of each

stage to take parasitic-effect into consideration. Capacitor values evaluated from the equations are applied to show the effect of the parasitic capacitances in the frequency-voltage characteristics. Simulation results are then compared with existing circuits in literature in terms of various features.

iii. Finally, the frequency characteristic of the circuit in response to the controlling parameters (V_{bias}, V_{DD}, width ratio and stage number) are investigated to obtain an empirical model for the operating-point of the proposed circuit.

3.3.1 Wide Tuning with Multimode Operation

The multimode tuning of the proposed circuit consists of coarse tuning and fine tuning. The coarse tuning is achieved by varying the supply voltage V_{DD} in the range from 0.3 V to 2 V maintaining the voltage V_{bias} constant at a particular voltage level. This tuning mode results in an ultra-wide frequency tuning range with higher sensitivity. In the fine tuning mode, the frequency is tuned in a smaller range by varying the V_{bias} from 0 V to 2 V keeping V_{DD} constant. The fine tuning mode provides more precise regulation of frequency allowing to make smaller changes at higher frequency band.

3.3.2 Device Sizing

In order to minimize the power penalty and chip area, the widths of PMOS transistors are considered 120 nm for all three circuits. The diode-connected transistors in active-load inverter circuit require the pull-down network to be stronger than the pull-up network so that the former is able to drive the output voltage to 0 and achieve proper oscillation. Therefore, the widths of NMOS transistors are taken 360 nm and this NMOS-PMOS width ratio is kept constant for all three circuits for uniform comparison and optimizing the frequency-power trade-off.

3.4 Simulation Results and Analysis

3.4.1 Frequency-Voltage Characteristics

The frequency response of the three oscillators under comparison without parasitic effects in consideration are shown in Fig. 3.3. The proposed RO is operated in the coarse

tuning mode in this situation. The figure shows that the proposed RO can obtain the highest operating-point at any corresponding supply voltage and also the highest frequency range among the three circuits. The loss of oscillation for the active-load inverter based RO is also visible from the figure for supply voltages below 1.5 V.

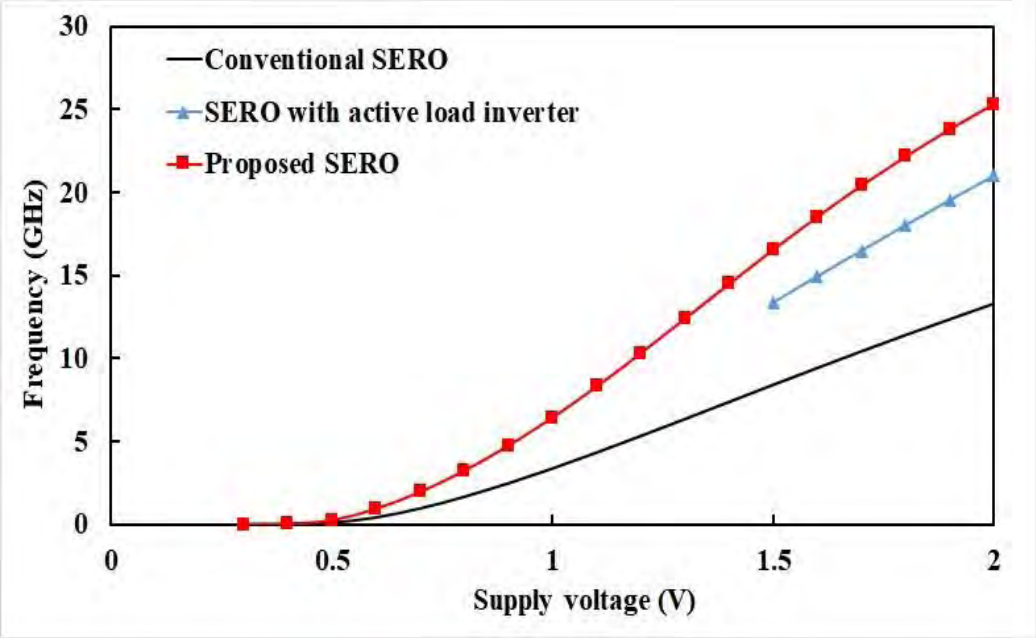


Fig. 3.3: Frequency response of three different SEROs

Figure 3.4 shows difference in the voltage swing of the three oscillators by plotting the oscillating signals at V_{DD} = 2 V. The decrease in frequency bandwidth and voltage swing of the RO with active-load is evident from figures 3.3 and 3.4, respectively. The additional parallel PMOS transistors in the proposed circuit help to retain the oscillation for supply voltages below the level of 1.5 V and simultaneously improve the voltage swing from the active-load inverter based design.

The total parasitic load capacitance of the three oscillators in comparison are calculated by taking the different components from Table 2.2, and equations (3.1) and (3.6) into consideration. The values of these components are extracted from the list of model parameters in the Cadence software and are presented in Table 3.1. The circuits are then re-simulated with load capacitance having the calculated value connected at the output of each stage. Figure 3.5 shows the expected effect of parasitics on the frequency-voltage characteristics.

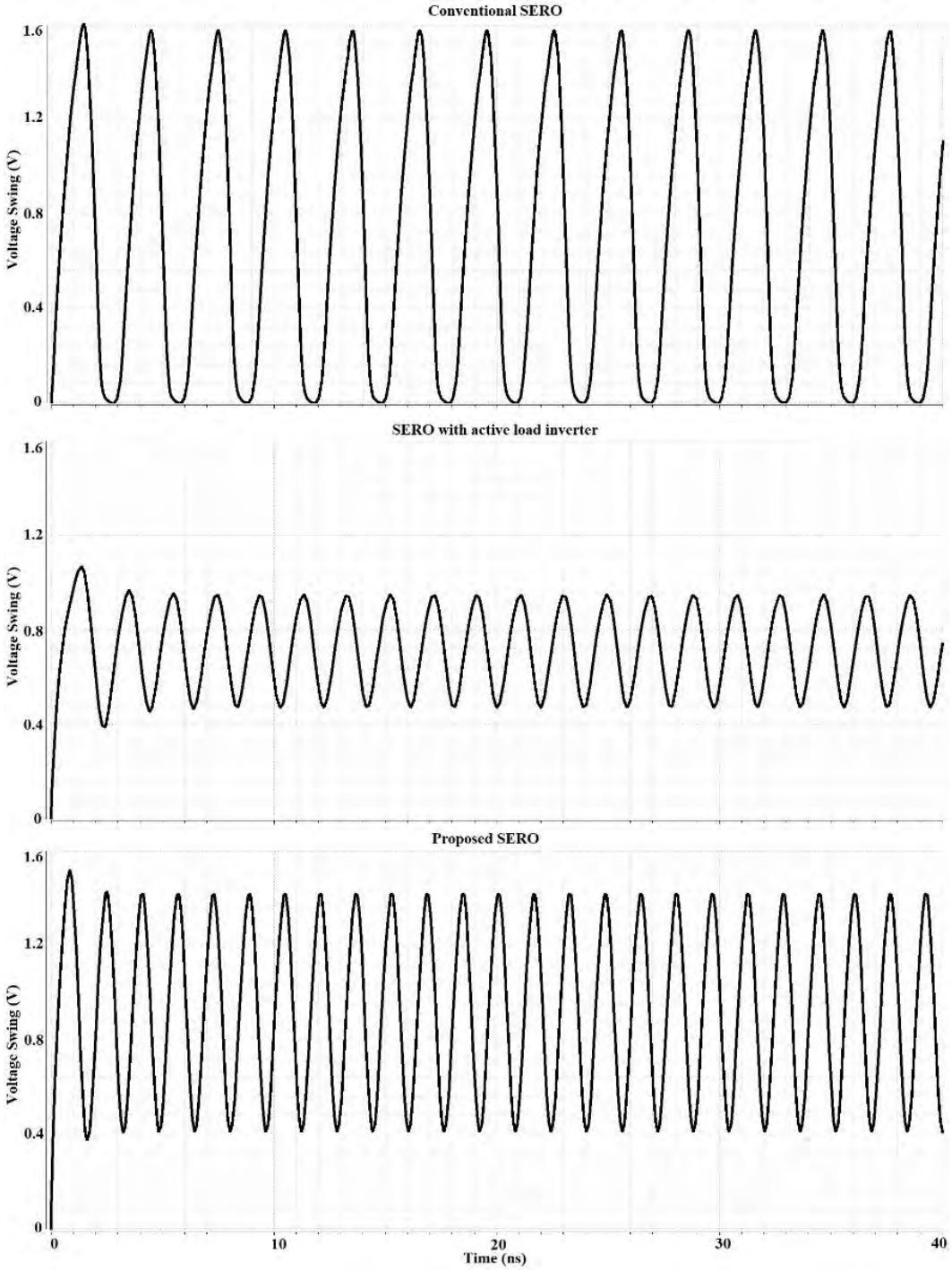
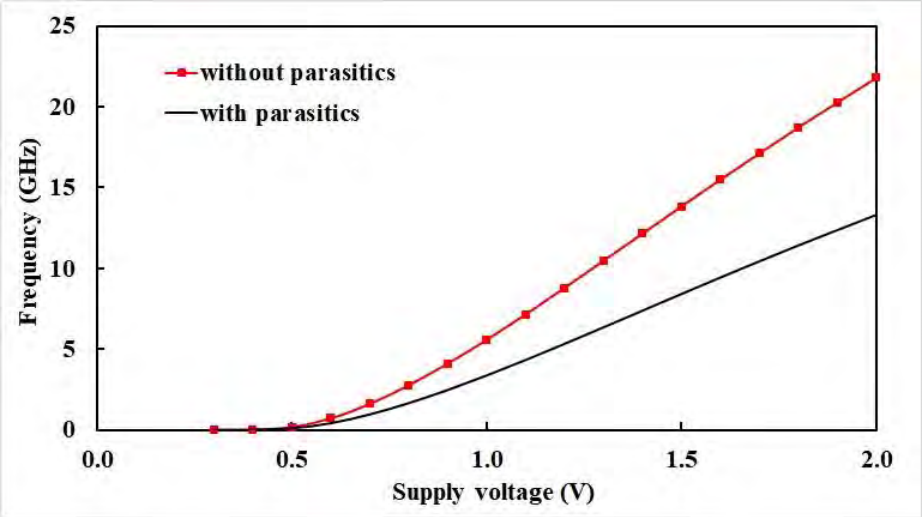


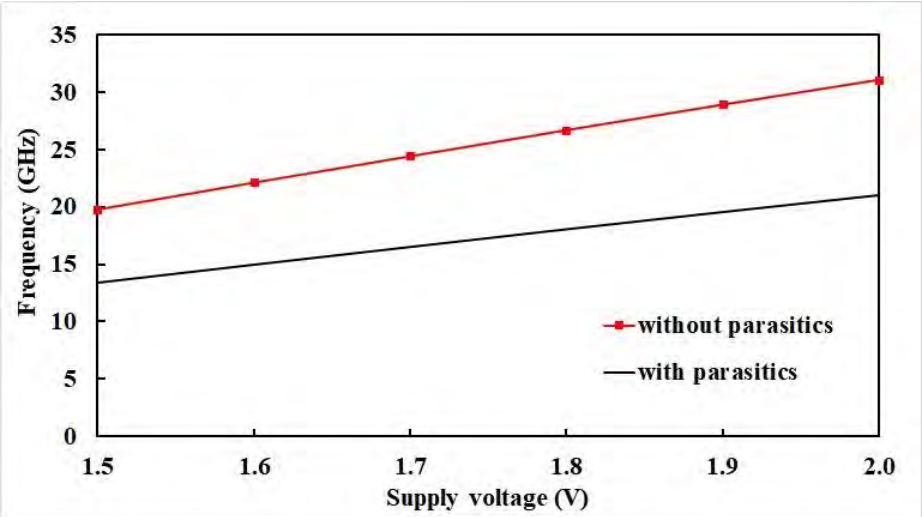
Fig. 3.4**:** Oscillator outputs of the three circuits at 2 V supply

Table 3.1**:** Load capacitance of the three oscillators

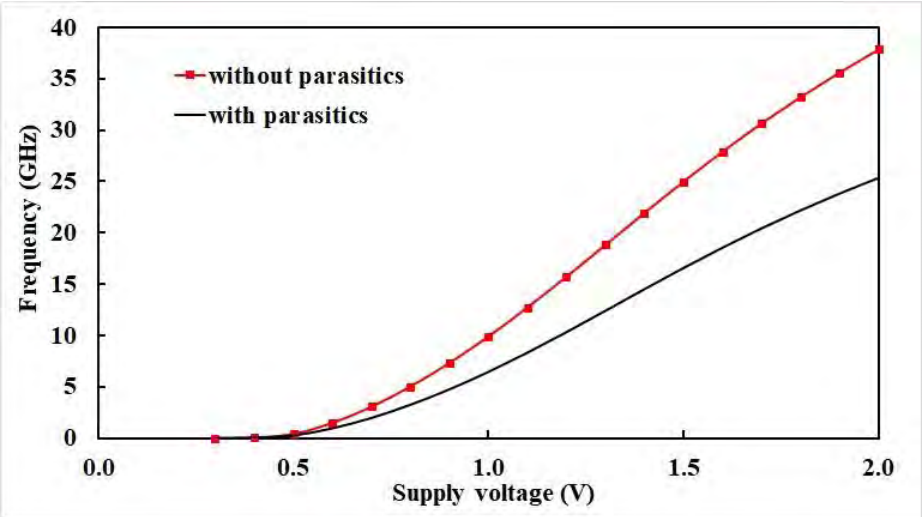
Circuit	**C_L (fF)**
Conventional SERO	0.662
SERO with active-load	0.447
Proposed SESLRO	0.518



(a)



(b)



(c)

Fig. 3.5: Parasitic effect on frequency-voltage characteristics for (a) conventional SERO, (b) SERO with active-load inverter, and (c) proposed SERO

3.4.2 Fine Tuning Frequency Response

The frequency response of the proposed RO in the fine tuning mode is shown in Fig. 3.6 for various supply (V_{DD}) magnitudes. Loss of oscillation occurs for higher fine tuning control voltage (V_{bias}) voltage values at supply voltages of 1.6 V and below. Furthermore, as the power rails decrease from 2 V, the frequency tends to a constant value in a quicker manner. The two tuning modes, coarse and fine, are compared together in Fig. 3.7. The auxiliary control voltage V_{DD} during fine tuning is set at 2 V, while V_{bias} during coarse tuning is set at 0 V. For the primary control voltage variation of 1 V (0.5 V to 1.5 V), approximate sensitivities of 3.37 GHz/V and 16.31 GHz/V are achieved for fine and coarse tuning, respectively.

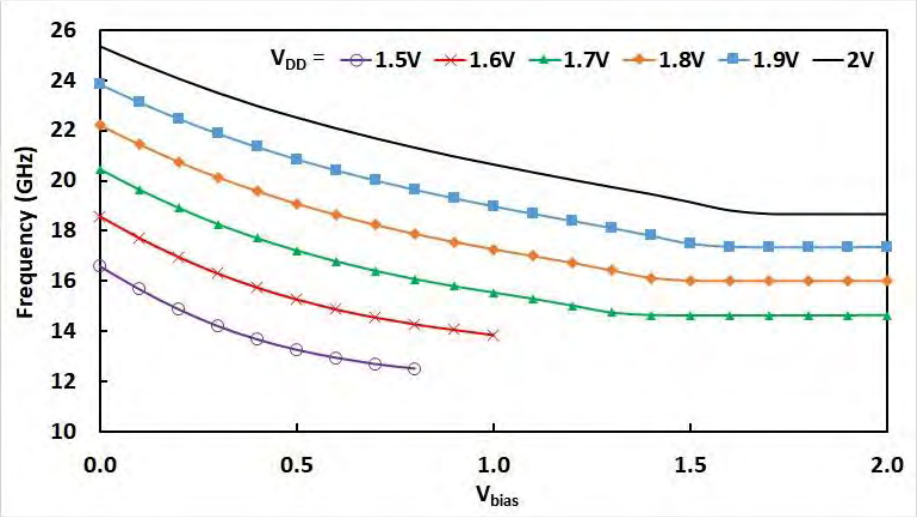


Fig. 3.6: Fine tuning frequency response of SESLRO

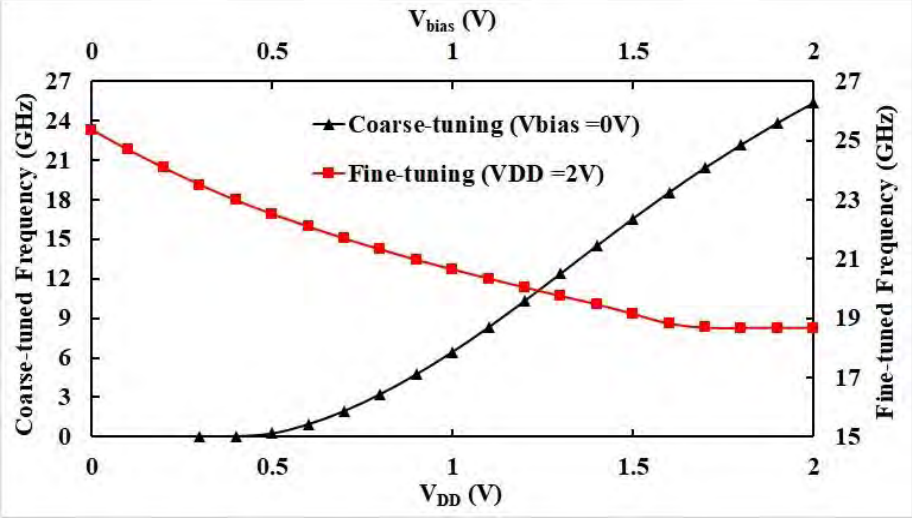


Fig. 3.7: Comparison of two tuning modes in SESLRO

The proposed SESLRO is then compared with other presented works in literature in terms of process node, supply voltage, operating-point, tuning range, power penalty and noise performances. Data presented in Table 3.2 shows the proposed architecture is able to manage higher frequency tuning range with considerably low power penalty.

Table 3.2: Comparison with other works

Architecture [Ref. No.]	**CMOS process (nm)**	**Supply voltage (V)**	**Center frequency (GHz)**	**Tuning range (GHz)**	**Power (mW)**	**PN (dBc/Hz) @ offset (MHz)**
Three-stage conventional [this work]	90	0.3 – 2	6.66	0.002 – 13.32	0.22 @ 2 V	-58.80 @ 1 (2 V)
Three-stage active-load inverter based [this work]	90	1.5 – 2	17.22	13.40 – 21.03	0.22 @ 2 V	-53.07 @ 1 (2 V)
Five-stage Current starved [31]	130	-	1.56	0.30 – 1.60	0.14	-90.68 @ 1
Five-stage Transmission gate based [31]	130	-	1.56	0.20 – 2.00	2.70	-95.17 @ 1
Three-stage RO using NMOS sinks [34]	180	0.6 – 2.5	3.024	0.34 – 5.68	0.60 @ 2.5 V	-117.00 @ 1 (2.5 V)
*Three-stage inductor peaking [40]	65	1.2	12.66	0.248 – 25.07	29.9	-95.6 @ 1
*Three-stage inductor peaking [40]	130	1.5	6.13	0.36 – 11.89	37.5	-103.3 @ 1
*Four-stage RO using series LC tanks [41]	45	0.9 – 1.1	3.82	2.66 – 4.97	8.5 – 16	-107.5 @ 1 (0.9 V)
Proposed circuit [this work]	90	0.3 – 2	12.67	0.004 – 25.34	0.63 @ 2 V	-53.61 @ 1 (2 V)

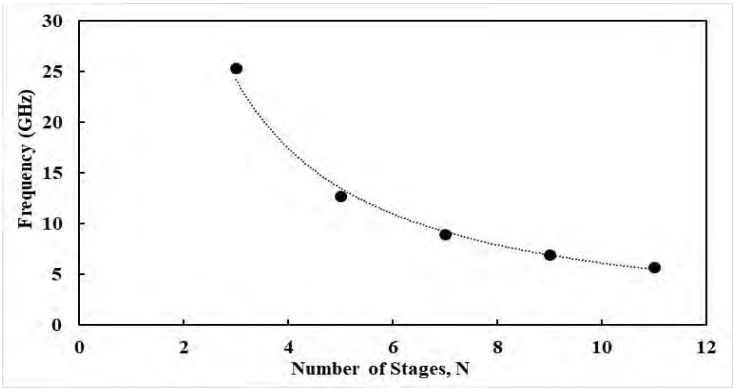
*Data include experimental result

3.4.3 Empirical Model of Operating-Point

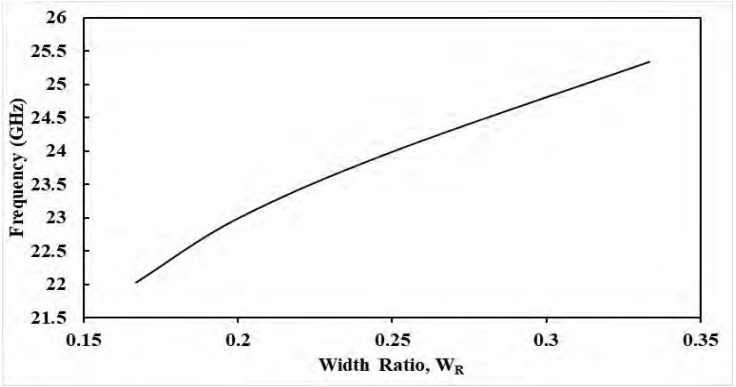
As discussed in section 2.8, the approximate operating-point models are based on the conventional inverter based RO and cannot be used as a practical formula by designers

for different architectures [53]. Additionally, simplifications are required in complex analytical derivations which reduce the accuracy of the equations. Therefore, a more accurate expression for the frequency of oscillation of the proposed SESLRO is obtained from simulation data which explicitly estimates the operating-point of the circuit for particular values of the controlling parameters. As a result, desired frequency of oscillation can also be set for specific applications such as SERO based fault testing, as discussed in the next section.

At first, the effective parameters which influence the operating-point of the oscillator are determined which are control voltage V_{bias}, supply voltage V_{DD}, number of stages N and load capacitance C_L. The load capacitance depends on the transistor size (length and width). Since simulation is carried out at fixed technology node, transistor length remains constant. Typically, the widths of PMOS and NMOS transistors are chosen as a ratio for the CMOS inverter. Let that width ratio be W_R. The frequency response as a function of N and W_R are shown in figures 3.8(a) and 3.8(b), respectively.



(a)



(b)

Fig. 3.8: Frequency versus (a) N and (b) W_R

The maximum value of W_R is 0.33 for the design. This is because any higher value weakens pull-down network compared to the pull-up network and oscillation is lost. Analyzing figures 3.7 and 3.8, the operating-point expressions with respect to each controlling parameter individually while other parameters are fixed can be estimated using (3.7)-(3.10), where $N = 2x + 3$ for $x \geq 0$ and integers. Root mean square error (RMSE) and R^2 values are calculated to determine the accuracy of the models. The RMSE is a square root of the variance of the residuals and indicates how close the observed data points are to the model's predicted values [54]. A smaller value indicates better accuracy of the model. The R^2 value indicates how successful the fit is in explaining the variation of the data and a value close to 1 is desired. While R^2 is a relative measure of fit, RMSE is an absolute measure. The coefficient values and accuracy of the models are given in Table 3.3.

$$f_{osc}(V_{DD}) = a_1 {V_{DD}}^3 + a_2 {V_{DD}}^2 + a_3 V_{DD} + a_4 \tag{3.7}$$

$$f_{osc}(V_{bias}) = b_1 e^{cV_{bias}} + b_2 e^{dV_{bias}} \tag{3.8}$$

$$f_{osc}(W_R) = c_1 {W_R}^2 + c_2 W_R + c_3 \tag{3.9}$$

$$f_{osc}(N) = d_1 N^{d_2} \tag{3.10}$$

Table 3.3: Coefficients and accuracies of the functions in the empirical model

Function	Coefficients	R^2	RMSE
$f_{osc}(V_{DD})$	a_1 = -6.90, a_2 = 29.00, a_3 = -18.00, a_4 = 3.10	1	0.05
$f_{osc}(V_{bias})$	b_1 = 23.70, b_2 = 1.59, c = -0.29, d = 0.62	0.99	0.11
$f_{osc}(W_R)$	c_1 = -46.18, c_2 = 43.00, c_3 = 16.17	0.99	0.087
$f_{osc}(N)$	d_1 = 94.67, d_2 = -1.2	0.99	0.57

However, the general expression of the operating-point as a function of all the parameters using linear regression technique can be defined by (3.11). The R^2 value of the model is 0.96 indicating acceptable accuracy. Figure 3.9 compares the simulated data with the predicted data from the empirical model of (3.11) indicating that the oscillating frequency can be well estimated using the equation. However, the accuracy of the model can be improved with greater number of observations.

$$\begin{aligned} &f_{osc}(N, W_R, V_{DD}, V_{bias}) \\ &= -4.01N + 16.61W_R + 18.28V_{DD} - 3.35V_{bias} - 5.01 \end{aligned} \tag{3.11}$$

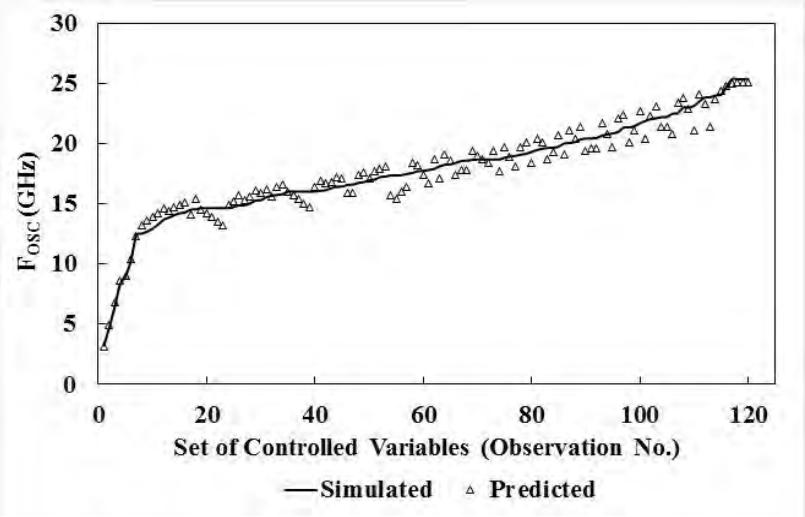


Fig. 3.9: Simulated data versus empirical model

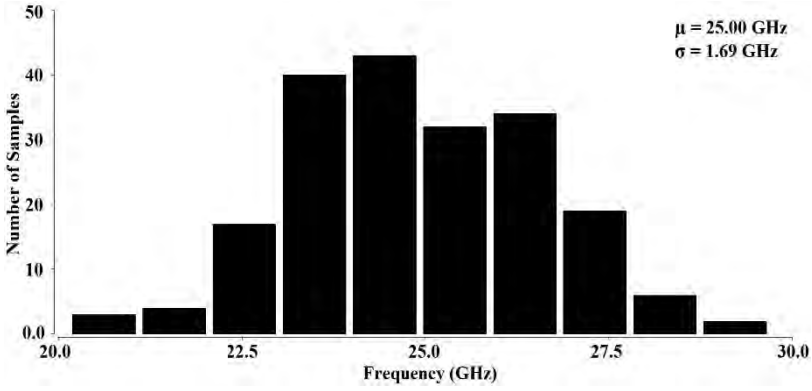
3.4.4 Impact of PVT Variations

The oscillation frequency is strongly dependent on the current through the transistors which is influenced by the supply voltage, and threshold voltage and geometric parameters of the device. On the other hand, threshold voltage and mobility are also temperature dependent. Hence any variation in the process parameters, voltage and temperature (PVT) would lead to variation in the oscillation frequency. The frequency response with respect to supply variation is already shown in Fig. 3.5, since it is used as one of the frequency tuning controls. A wide variation is desired in this case for wide frequency tuning range.

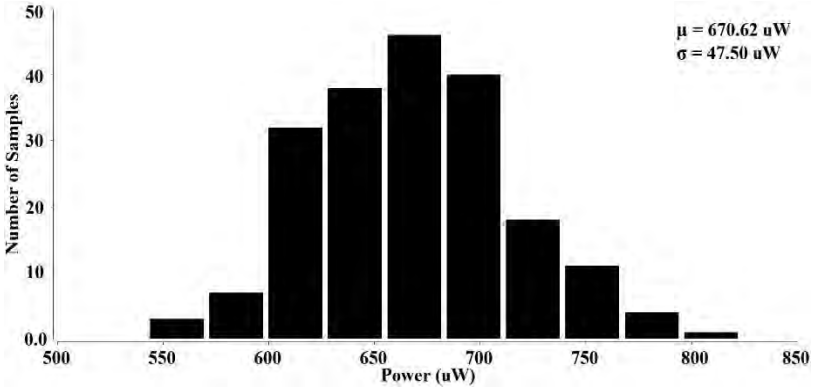
To observe the effect of process variations and device mismatch, Monte Carlo simulations are performed. Gaussian statistical distribution with maximum standard deviation σ of 10% of the mean μ is considered for the variation. Two hundred Monte Carlo runs are performed to observe the effect on oscillation frequency and power penalty for a supply voltage of 2 V, and both responses followed the Gaussian distribution as shown in Fig. 3.10. The standard deviation is less than 10% and the maximum and minimum values are within $\pm 3\sigma$ of the mean value.

Performance of the proposed oscillator is also evaluated at different technology nodes such as 16 nm and 45 nm. Predictive Technology Models (PTM) for low power applications are used for simulations while keeping the p-type to n-type device width ratio

same as before. Performance is evaluated in terms of frequency response, power penalty and phase noise and is presented in Table 3.4. At 45 nm technology, oscillation is obtained for the same range of supply regulation from 0.3 V to 2 V. Although maximum operating point is reduced, lower frequency bands are obtained in the kHz range and hence the percentage of tuning range remains equal. Meanwhile at 16 nm technology, oscillation frequency is significantly increased at the cost of reduced percentage of tuning range. Oscillation is obtained for supply regulation from 0.7 V to 1.4 V. Power penalty is reduced for both technology nodes, while phase noise performance degrades further.



(a)



(b)

Fig. 3.10: Impact of statistical variations of process parameters on (a) frequency, and (b) power penalty

Table 3.4: Performance of proposed oscillator at different technology nodes

Process (nm)	**Supply regulation (V)**	**Center frequency (GHz)**	**Tuning range (GHz)**	**Power consumption (mW)**	**Phase noise (dBc/Hz) @ offset (MHz)**
16	0.7 – 1.4	25.67	2.06 – 49.27	0.053 @ 1.4 V	-31.2 @ 1 (1.4V)
45	0.3 – 2.0	10.00	0.0007 – 19.99	0.301 @ 2 V	-46.18 @ 1 (2.0 V)

Figure 3.11 shows the effect of temperature variation, which is negligible, on the frequency versus supply characteristic curve. The maximum variation of oscillation frequency is 7.06% at 2 V supply for 100 degrees change in temperature. The power penalty variation is only 5.35% for the same environment. The increase in temperature causes threshold and mobility degradation, which directly influences the current. At higher supply voltages, the effect of mobility degradation is dominant, causing a decrease in the oscillation frequency.

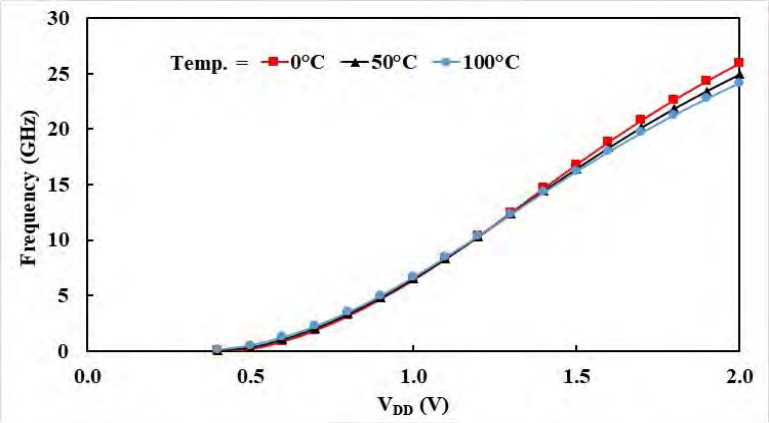


Fig. 3.11: Impact of temperature variation on frequency-voltage characteristic

3.4.5 Layout

The layout diagram of the proposed SESLRO is drawn using Cadence Virtuoso Layout Suite L editor and is shown in Fig. 3.12. The total calculated area of the circuit is only 8.02 um^2.

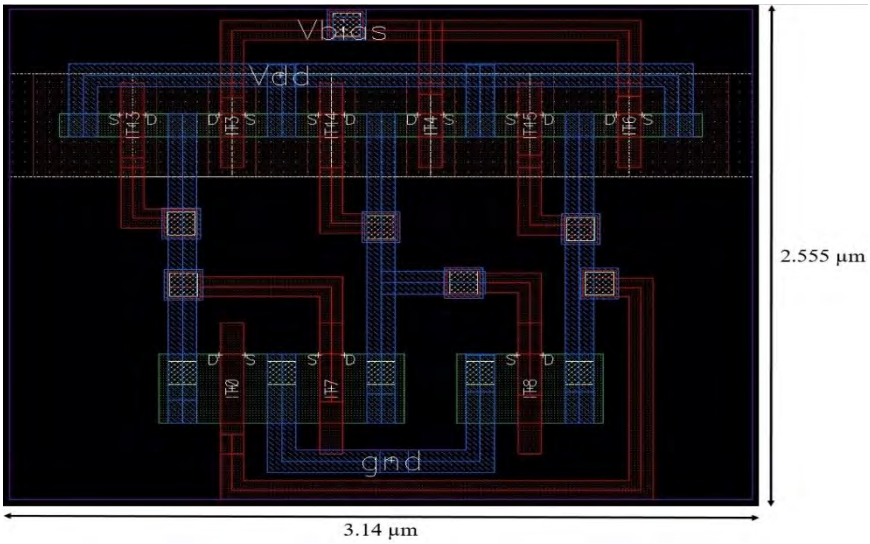


Fig. 3.12: Layout of proposed SESLRO

Chapter 4

Leakage Tolerant Transistor Stuck-ON Fault Detection using Ring Oscillators

This chapter initially discusses conventional fault detection methods with regard to error inducing events like TSON faults. After that, it introduces the proposed methodology of fault-testing schemes based on SEROs. Simulation results and analysis are then provided for conventional and proposed SERO fault-detecting architectures with focus on leakage tolerant TSON fault detection, adaptable threshold regulation and built-in current sensor performance. Finally, the scheme is validated by making comparison with testing methods in literature.

Testing is generally defined to be the process by which a fault or defect in the system, that may occur at the time of manufacturing or operation of the system, can be detected. The growing complications of electronic components and systems demand high quality, simple and low cost fault testing to ensure correct operations [55, 56]. These tests have become a difficult and time consuming task for the chips that contain a million or more transistors. Design for testability techniques are recommended to ease the testing burden. Many such techniques have been proposed which have the common aim of trying to abate the amount of time it takes to generate test vectors and apply them to the circuit under test (CUT) [57].

4.1 Transistor Stuck-ON (TSON) Fault

Transistor stuck-on (TSON) is a type of fault where the corresponding transistor is always on because the drain-source terminals are shorted. It is the kind of fault whose presence results in the circuit drawing current a few orders of magnitude greater than the normal leakage current [58]. During this fault in CMOS logic, a complete path between the supply voltage and ground is created that results in higher leakage current and an intermediate voltage at the output node which is difficult to interpret as either logic high or low. The intermediate voltage is based on the ratio of equivalent resistances of the pull-up and pull-down networks. Hence, the output voltage will vary for different input combinations and fault locations due to different equivalent resistances at one or both networks.

4.2 Conventional Fault Detection Methods

When a TSON fault is present in a circuit, it can be exposed as an incorrect logic value at the output node. This is the popular logic (voltage) testing method. However, observing the logic value at the voltage level is not the only method, and neither a reliable one, to always determine the occurrence of a fault. This is because certain locations of the fault sometimes can cause the circuit to draw excessively large amount of current for a corresponding test vector but not result in an incorrect logic value at the outputs.

In order to tackle the difficulties of logic test, an alternative method based on current monitoring is available which measures the steady state (or quiescent) current (I_{DDQ}) drawn by the circuit, and can ensure the detection of all stuck-on faults [59, 60]. Though I_{DDQ} testing is a well-accepted testing approach based on the observation of the quiescent current consumption, it consists of several drawbacks. Since a period of time needs to be considered for the current to reach the steady-state condition and be monitored, it is a slow process limiting the frequency of input vectors that can be fed to few kHz [61]. Furthermore, although built-in current sensing of CUTs is possible with this method [62], additional sensing equipment in the presented works in literature have high area overhead with complex circuitry. A major drawback of the method is that its effectiveness in deep

submicron technology may decline where the increased leakage current and fault current become indistinguishable from each other [63].

Several works discussed in [64-67] use SEROs to detect through silicon via (TSV) faults, which include shorts, opens, delay faults, incomplete fillings or presence of micro-voids in the via. For example, incomplete fillings or micro-voids cause changes in the capacitance of the TSV. The testing is based on the variation in frequency of the oscillator due to the change in capacitance which causes a change in delay. On the other hand, open faults result in loss of oscillation.

4.3 Fault Conditions and Test Vectors

The CUT investigated in this work for TSON fault detection is shown in Fig. 4.1. The output equation of the circuit is

$$F = \overline{AB + CD} \tag{4.1}$$

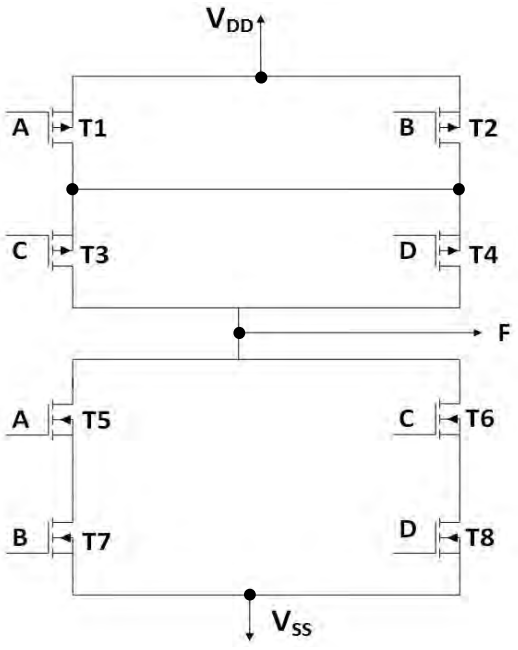


Fig. 4.1: Circuit under Test (CUT)

TSON faults are created at each transistor by shorting the drain and source terminals. The effect of the fault is observed at the output by switching OFF the corresponding faulty transistor. For a TSON fault in the pull-up network, the input to the gate of faulty transistor is set at logic high and input to other PMOS transistors are set such that no conducting path is created from V_{DD} to the output node F in a fault-free condition while

such a path is created during a faulty condition. Similarly for faults in the pull-down network, the corresponding faulty transistor is biased by setting the gate logic to 0 (low). The set of input combinations which creates two distinguished outputs for fault-free and faulty conditions is called a test vector (TV). Fault testing techniques can be divided into two categories: simulation before test and simulation after test [68]. In simulation before test method, test vectors are applied for a selected number of faults to observe the circuit response. For example, we consider a stuck-on fault in transistor T1. In order to test this fault, a test vector must be selected so that the circuit gives an output of logic 0 during fault-free condition but logic 1 during faulty condition due to the stuck-on transistor. The three possible test vectors are <1100>, <1101> and <1110>. All three test vectors ensure that the pull-down network is conducting to pass logic 0 to the output during fault-free condition through transistors T5 and T7. To propagate the effect of fault in T1 to the output, T2 must be off all the time so that during faulty condition the path is created through T1 and either T3 or T4. Hence, during fault-free condition the output logic remains 0, while in faulty condition a complete path is created from V_{DD} to V_{SS} which results in an intermediate voltage level to be observed at the output node. The intermediate voltage between logic 1 and 0 is based on voltage-divider rule due to the on-resistance of the conducting transistors. This voltage becomes difficult to be interpreted as logic high or low and so the fault detection using logic level is unsuitable. However, since a constant path is created between the two voltage rails, the static current of the circuit increases and the fault can be detected by measuring this quiescent current, I_{DDQ}. The I_{DDQ} current can vary depending on the test vector due to the total equivalent resistance of the conducting path from V_{DD} to V_{SS}. For example, the equivalent resistance for input combination <1100> is less than the other two test vectors and so the quiescent current is higher in this condition. Table 4.1 lists the possible test vectors for the CUT for differing TSON fault locations.

Table 4.1: TSON faults and corresponding test vectors

Network	TSON fault location	Test vectors
Pull-up network	T1 or T2	<1100>, <1101>, <1110>
	T3 or T4	<0011>, <0111>, <1011>
Pull-down network	T5	<0100>, <0101>, <0110>
	T6	<0001>, <0101>, <1001>
	T7	<1000>, <1001>, <1010>
	T8	<0010>, <0110>, <1010>

4.4 Proposed Methodology of Testing Methods

Problems of both logic test and I_{DDQ} test methods are discussed in section 4.2. In order to mitigate these disadvantages and obtain a simpler testing technique, ring oscillators are employed in this work to detect the TSON faults. In this method, when a stuck-on fault occurs in a transistor, oscillation is observed at the output of the appended ring circuit immediately after the current crosses a threshold value. The threshold value can be considered as the maximum leakage current in the network during fault-free state. Test vectors and fault locations can also be identified by observing the output of the SERO. The corresponding input combinations which generate oscillation can be matched with Table 4.1 to identify possible fault locations.

The two proposed methods are discussed in this section and the output results are presented. A review of different testing schemes is discussed in [69]. The proposed methods follow the measurement-based test methodology. In order to investigate the effectiveness of the two proposed techniques, a sequence of task is performed which is presented as a flowchart in Fig. 4.2. At first, one of the methods (method 1: SERO as current-controlled oscillator, or method 2: SERO as voltage-controlled oscillator) is selected for testing procedure. After the selection and integration of the SERO with the CUT, outputs of the test circuit and the oscillator are observed during fault-free state to verify correct operation. A TSON fault is then introduced in the CUT by shorting the drain and source terminals of a transistor and then oscillation is checked at corresponding test vectors. If no oscillation occurs, the selected method proves to be ineffective. In case of successful fault detection, both methods may be compared in terms of key features such as frequency of oscillation, area and power penalty overhead, and the effect on CUT output logic during fault-free state. In order to use the testing circuit as a built in current sensor (BICS) for on-chip testing, the SERO can be integrated with the CUT to form one single IC. The testing engineer can select the design which is more efficient in terms of the aforementioned features.

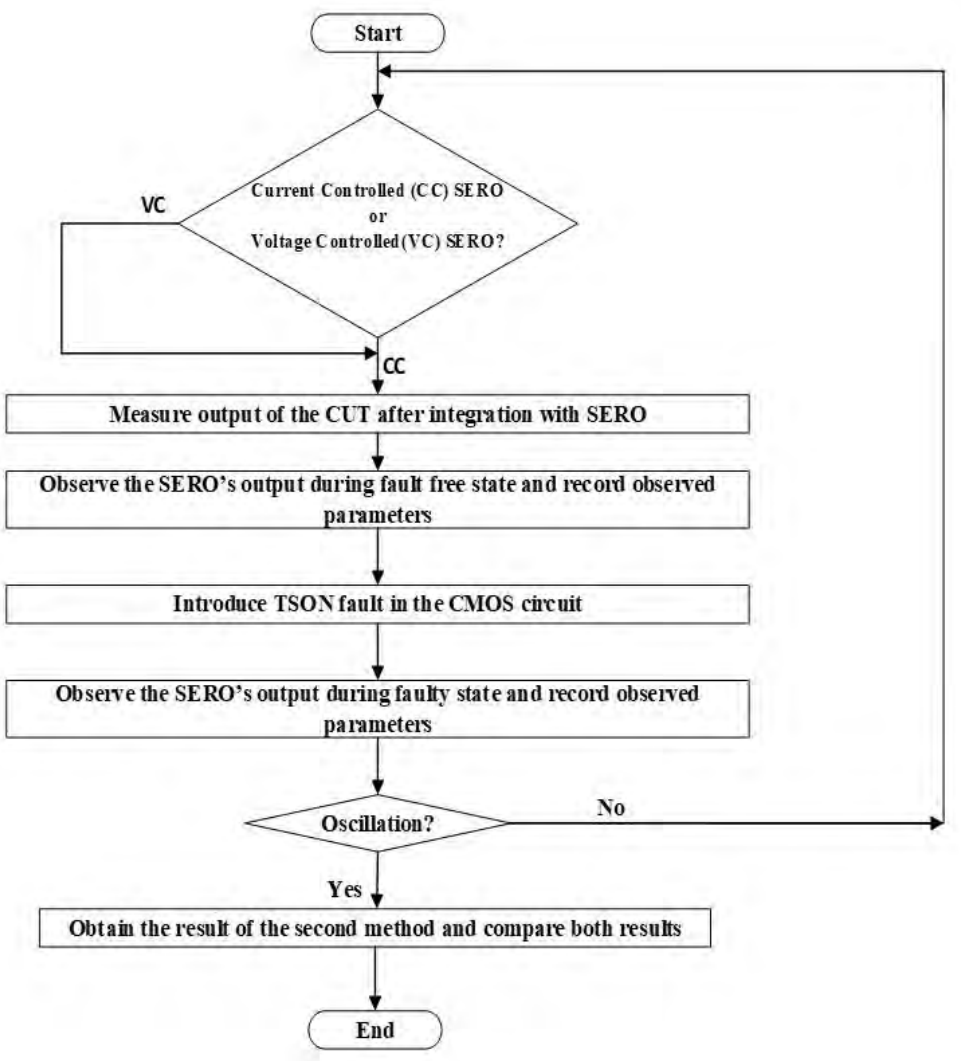


Fig. 4.2: Test method verification flowchart

4.5 Simulation Results and Analysis

4.5.1 Method 1: using Current-Controlled SERO

The first proposed technique uses a current controlled SERO. The architecture consists of the test circuit (CUT), a conventional inverter based ring oscillator (SERO) and a current mirror circuit (T_{P1} and T_{P2}) as shown in Fig. 4.3. The supply voltage to the ring oscillator and CUT is set at 1.2 V. The operating-point of the SERO is dependent on the current supplied to the oscillator as seen in section 2.8. The current through the CUT is mirrored into the SERO and hence the oscillation is dependent on the static current through the test circuit. During fault-free state, the static current through the CMOS

circuit is negligible and no oscillation is observed at the ring oscillator output. When a fault is present, the steady-state current of the test circuit increases significantly. This fault-modulated current triggers an oscillation at the output of the SERO.

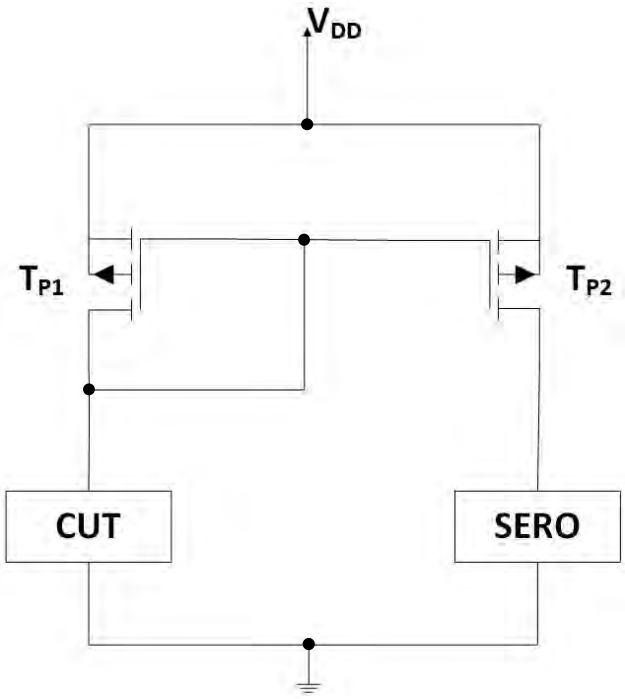


Fig. 4.3: TSON fault test using current-controlled SERO

The control signals of the standalone CUT are shown in Fig. 4.4. Figure 4.5 shows the performance of the integrated architecture during fault-free condition where the logic output of CUT, current through the CUT and oscillator output are shown. The CUT output logic is slightly deteriorated because of the integration of current mirror components but the logic levels can still be distinguished. The plot of current shows an absence of static current and hence no periodic oscillation is observed. For a TSON fault at a device in the pull-up network T_{PUN} (T1), the same output parameters are shown in Fig. 4.6. It can be observed that there is an increased steady-state current through the CUT and oscillation is obtained for the three corresponding test vectors indicating the presence of the fault. Meanwhile, the voltage output of the CUT has no significant change. The increase in current in the SERO integrated architecture is less compared to the CUT in isolated condition because of the extra PMOS element (mirror transistor) which increases overall resistance in the conducting path. The outputs for the fault in a pull-down network's transistor P_{TDN} (T6) are shown in Fig. 4.7. It shows that the fault is easily detected from the change in expected output logic for a stuck-on fault in the pull-down network. Due to

the presence of the fault, both pull-up and pull-down networks are conducting. An intermediate voltage is supposed to be obtained which cannot be assigned to any particular logic value. But the addition of the PMOS current mirror transistor makes the voltage drop across the pull-up network higher and the output voltage reaches closer to 0 V. Hence, the integration of the SERO also makes it easier for the fault to be detected through the logic testing method. However, the increase in current in this case is lower.

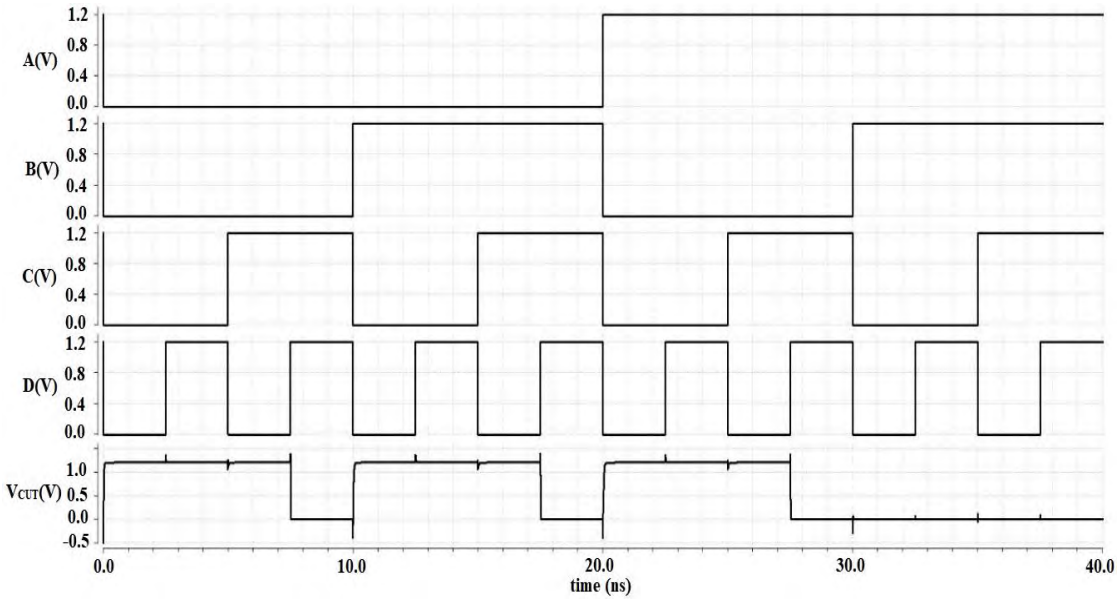


Fig. 4.4: Input control signals and output of the standalone CUT

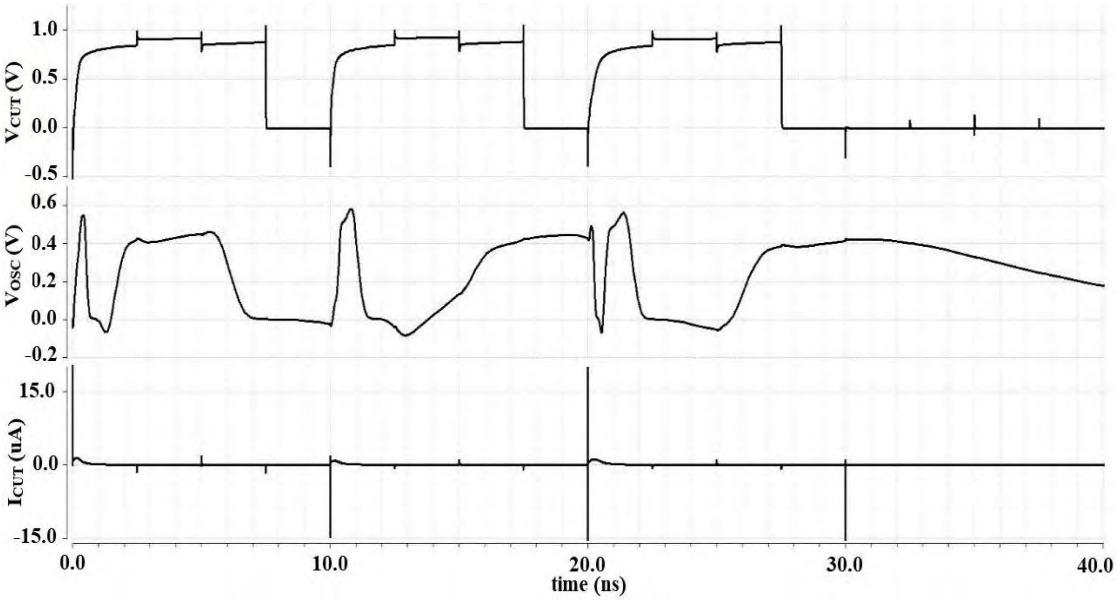


Fig. 4.5: Output logic of CUT, oscillator output and current through the CUT during fault-free state using Method 1

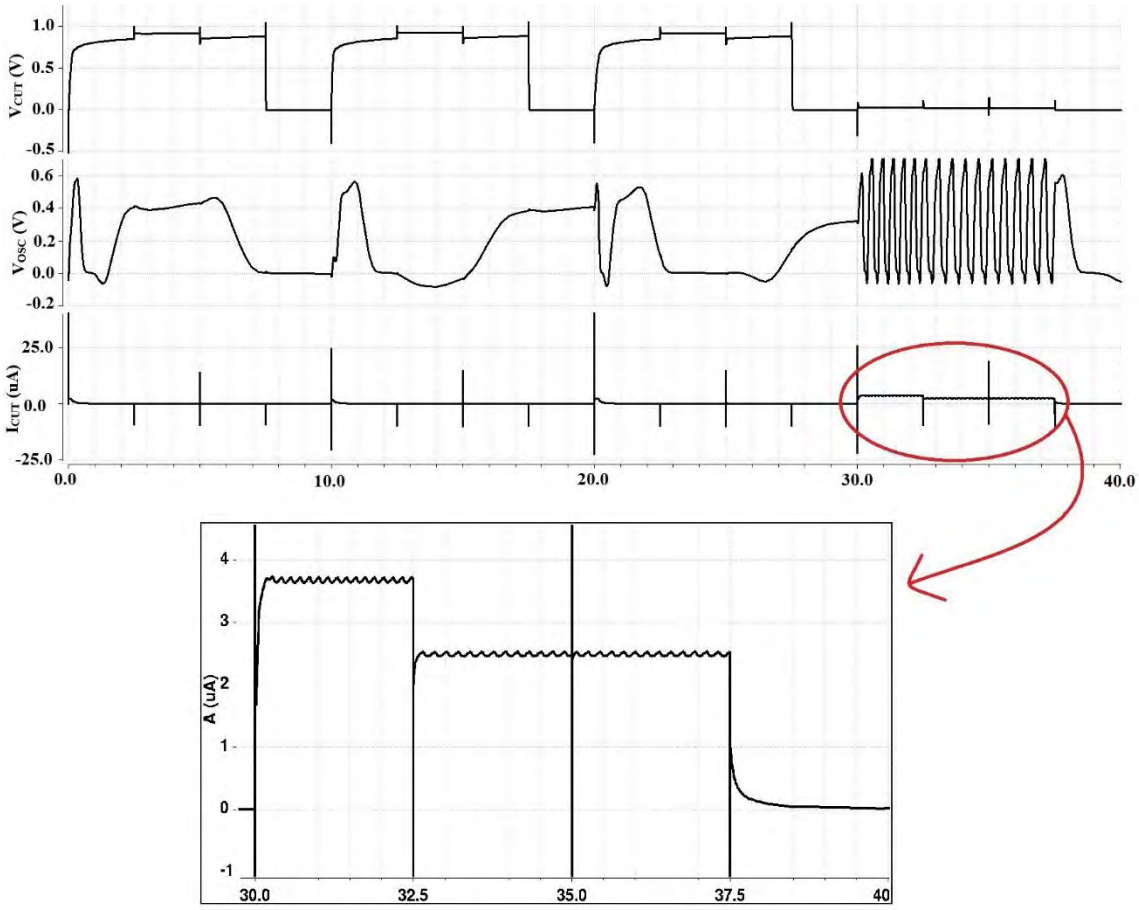


Fig. 4.6: Outputs for TSON fault at T_{PUN} (T1) using Method 1

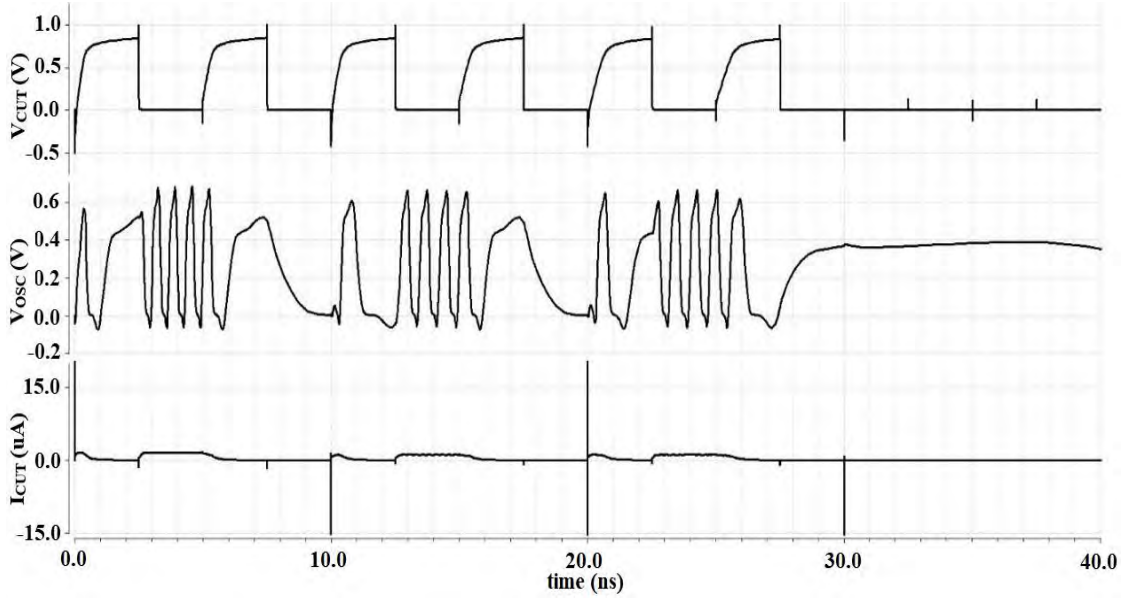


Fig. 4.7: Outputs for TSON fault at P_{TDN} (T6) using Method 1

4.5.2 Method 2: using Voltage-Controlled SERO

In the second proposed method, the SERO is used as a voltage controlled oscillator. An active load device (NMOS) is connected in series with the CUT and the voltage drop across this load, V_P is provided as the supply rail to the ring oscillator. The design structure is shown in Fig. 4.8. During a faulty condition, the increased steady-state current results in an increased potential at V_P which generates oscillation at the SERO output. The output resistance, R_O of NMOS should be sufficiently high in this case to cause the desired voltage drop at V_P. The resistance R_O for an NMOS in saturation region is given by the following equation [70]:

$$R_O = \frac{2L_n}{K_n W_n (V_{gs} - V_{thn})^2 \lambda} \tag{4.2}$$

where L_n is feature size, W_n is the width, K_n is a process parameter ($\mu_n C_{ox}$), V_{gs} is the gate-source voltage, V_{thn} is the threshold voltage of the NMOS and λ is the channel length modulation coefficient for short channel devices. In this case, V_{gs} is V_P. With L_n, K_n, V_{th} and λ fixed for a particular technology, and V_P depending on circuit operation, the width W_n is the only parameter that can be controlled by the designer. The width is kept minimum at 120 nm (minimum width allowed for 90 nm technology) for the desired resistance and output response. For any greater value, the oscillating frequency is too low for accurate detection.

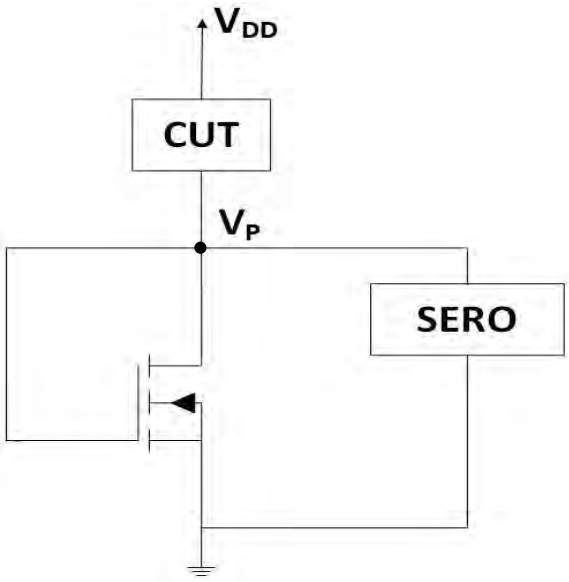


Fig. 4.8: TSON fault test using voltage-controlled SERO

All output voltages (logical output, V_P and oscillation) during fault-free conditions are shown in Fig. 4.9. Figure 4.10 shows the logical output, oscillator output and V_P during a TSON fault at T_{PUN} (T1) of the pull-up network. A constant voltage is obtained across the active load (due to the constant steady-state current) for the corresponding three fault detecting test vectors. The output logic is also high at this state since there is a significant voltage drop across the active load (approx. 0.55 V) because of the fault current. Therefore, the fault can also be detected from the voltage logic level in this situation. The oscillator output shows the desired oscillation at appropriate test vectors. A TSON fault at T_{PDN} (T6) was also created and the results are shown in Fig. 4.11. In this case, the fault cannot be detected from the voltage logic method since change in the output voltage of the CUT is minimal between fault-free and faulty conditions.

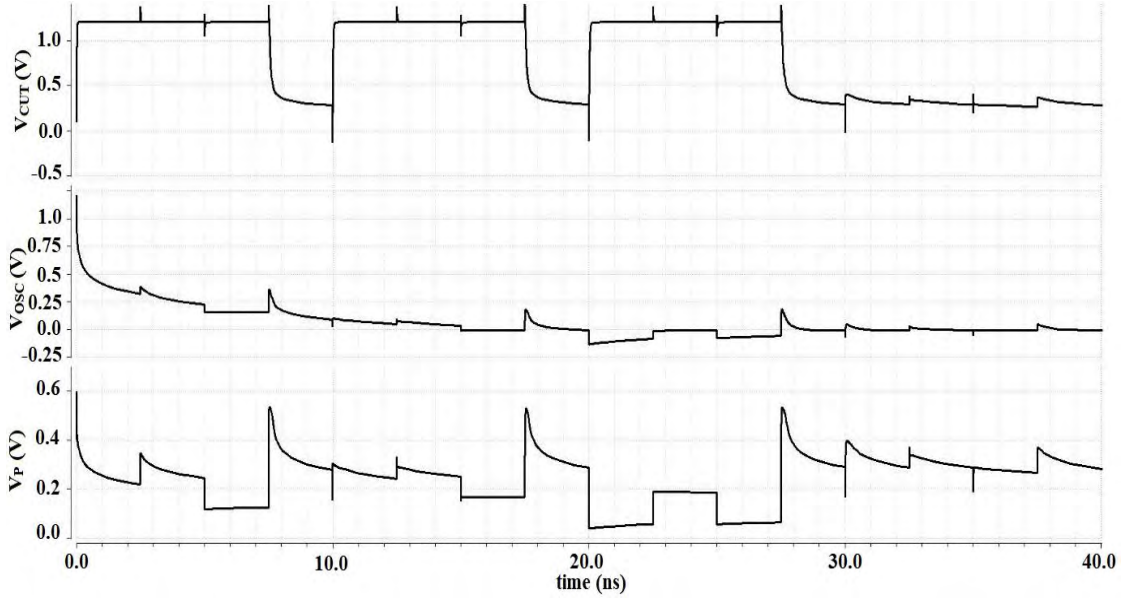


Fig. 4.9: Output logic of CUT, oscillator output and voltage V_P during fault-free state using Method 2

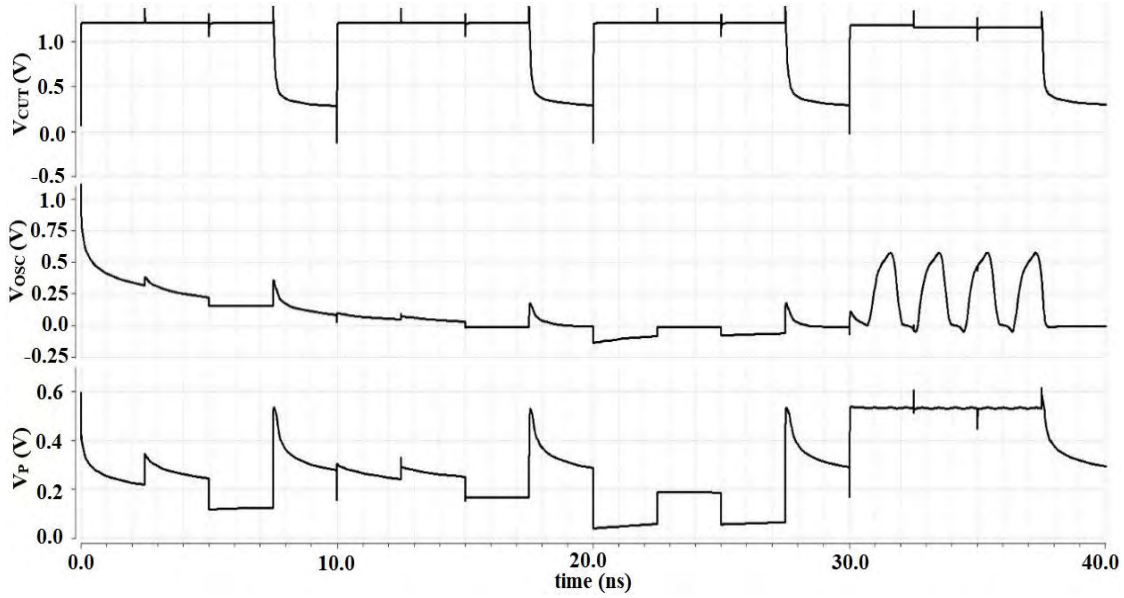


Fig. 4.10: Outputs for TSON fault at T_{PUN} (T1) using Method 2

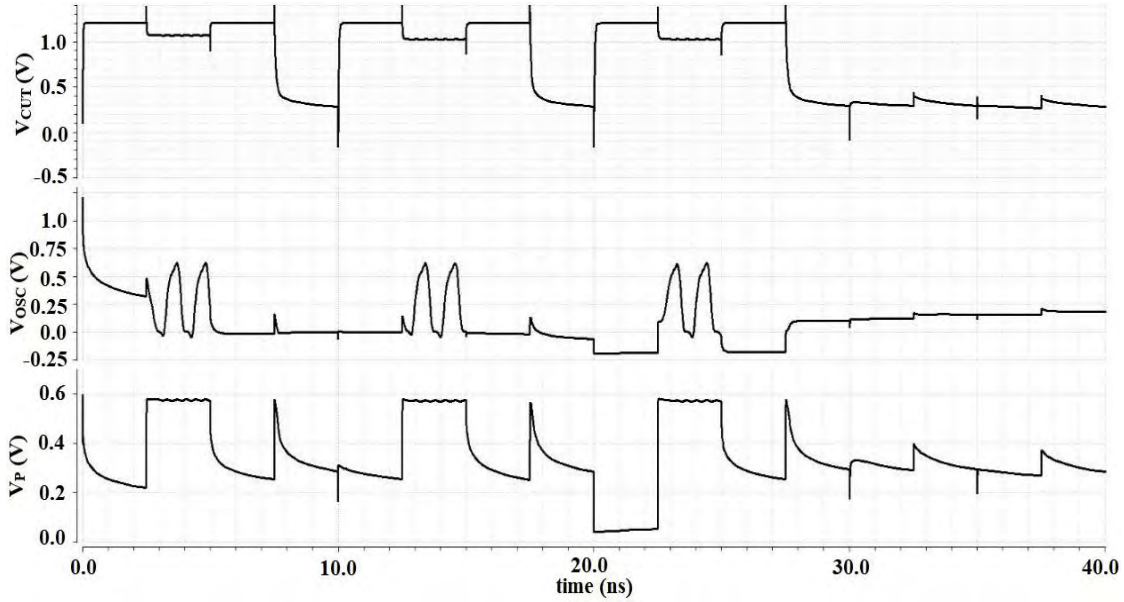


Fig. 4.11: Outputs for TSON fault at T_{PDN} (T6) using Method 2

4.6 Leakage Tolerant TSON Fault Detection

Once it has been verified through simulations that the two methods can successfully detect TSON faults, the conventional SERO is replaced with the proposed SESLRO structure. Figures 4.12 and 4.13 show the simulated results with method 1 for fault-free

and faulty conditions, respectively, for a fault in T_{PUN} (T1). Similarly, figures 4.14 and 4.15 show results for method 2. Figures show that the small difference between high leakage and fault current is sensed to trigger oscillation only during the fault at the corresponding test vectors. Any leakage-modulated oscillation can be eliminated for leakage tolerant testing through threshold regulation by the secondary tuning of the split-load oscillator, which will be further discussed in section 4.7.3. Figures 4.16 and 4.17 show the layout diagrams of the two methods using the SESLRO structure.

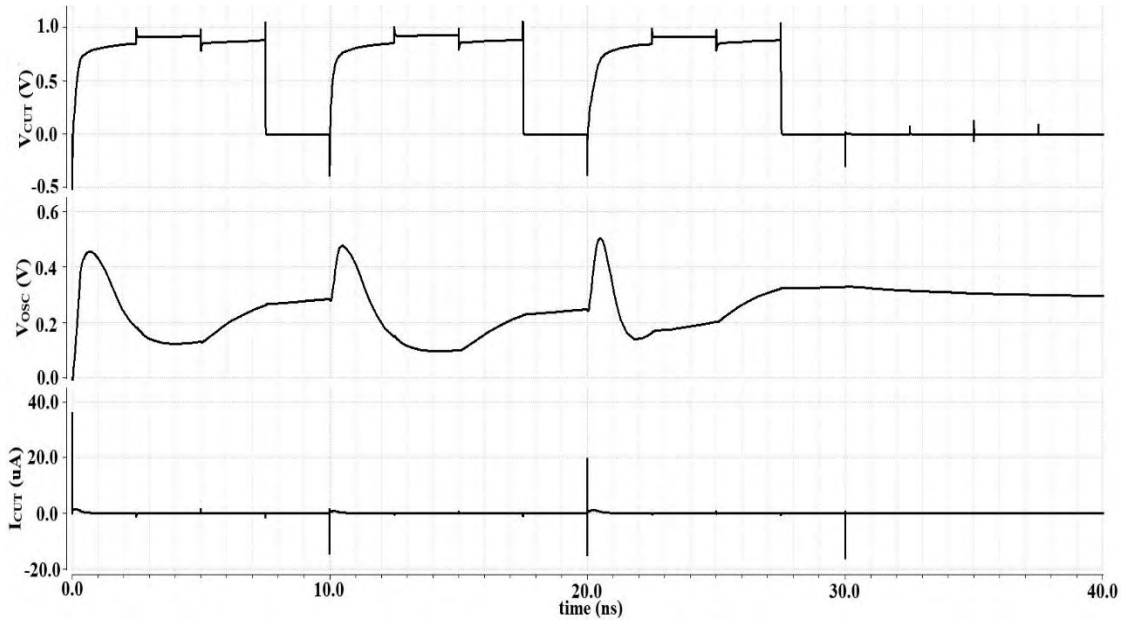


Fig. 4.12: Outputs of SESLRO-based Method 1 for fault-free state

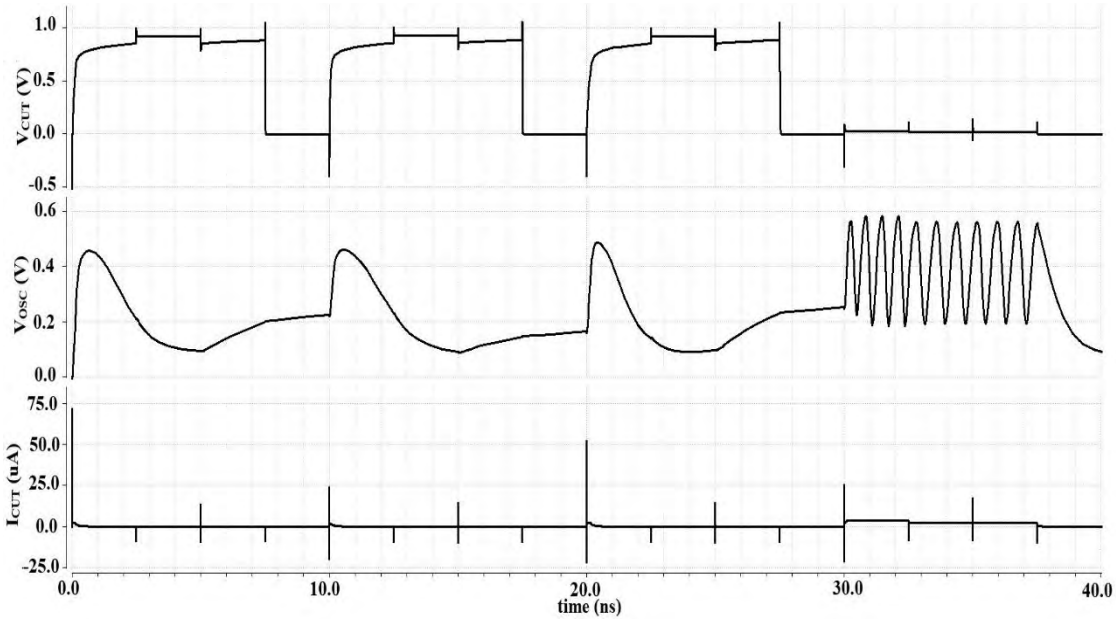


Fig. 4.13: Outputs of SESLRO-based Method 1 for fault in T_{PUN} (T1)

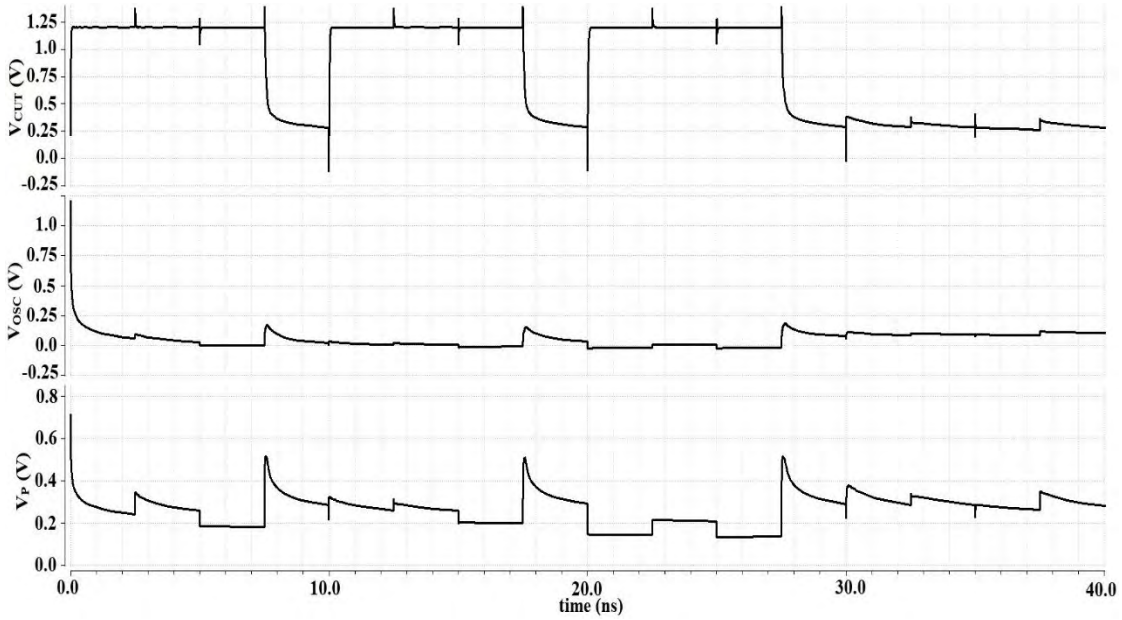


Fig. 4.14: Outputs of SESLRO-based Method 2 for fault-free state

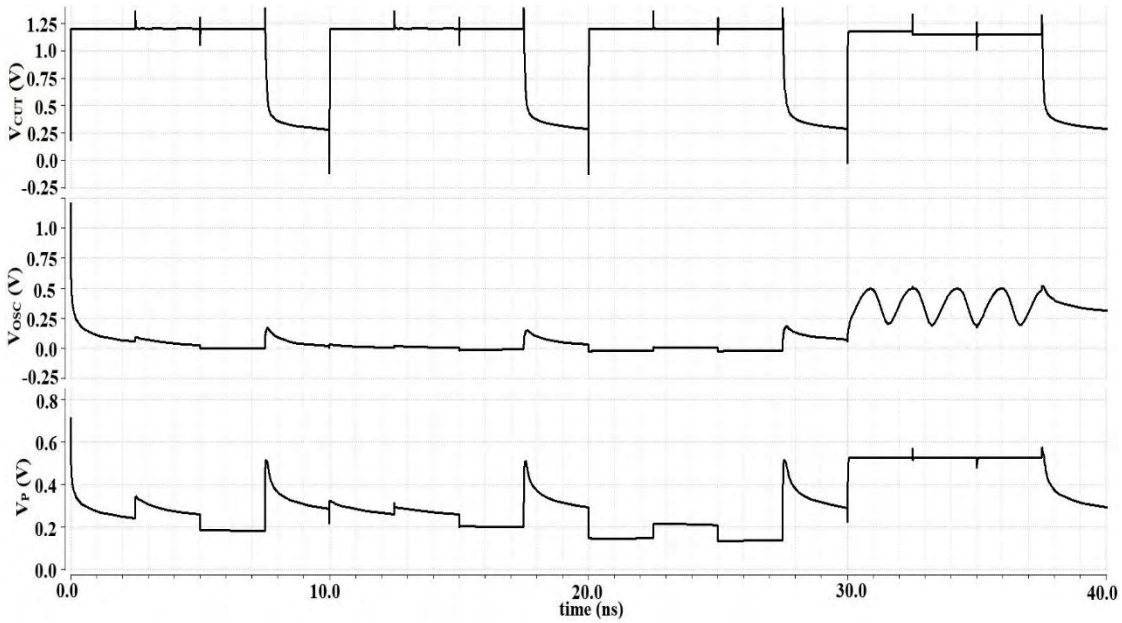


Fig. 4.15: Outputs of SESLRO-based Method 2 for fault in T_{PUN} (T1)

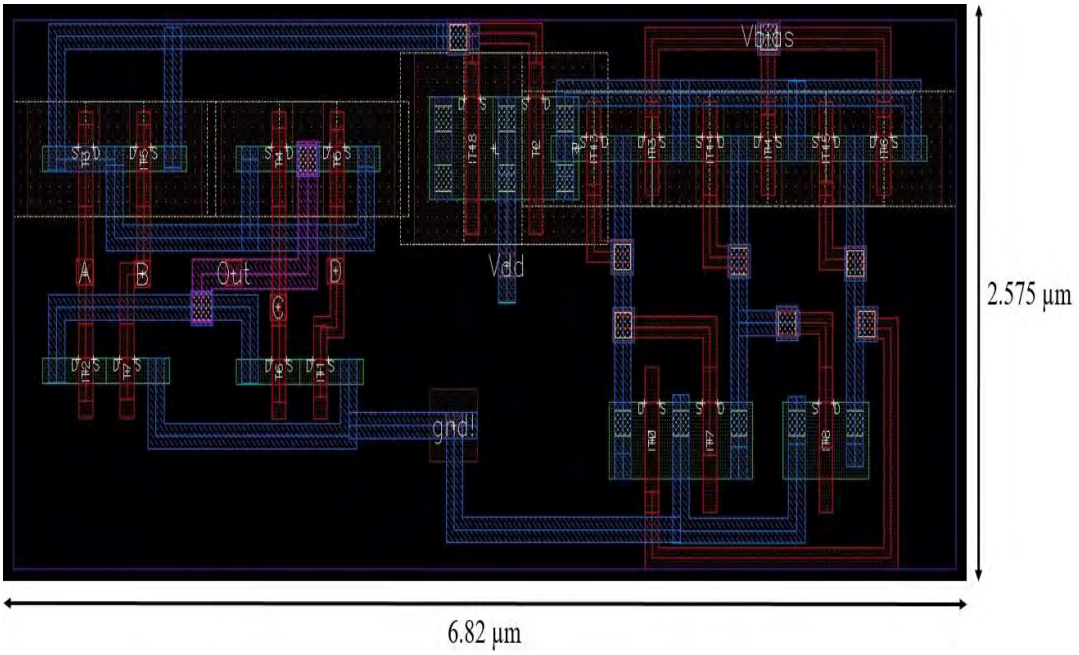


Fig. 4.16: Layout of SESLRO-based testing Method 1

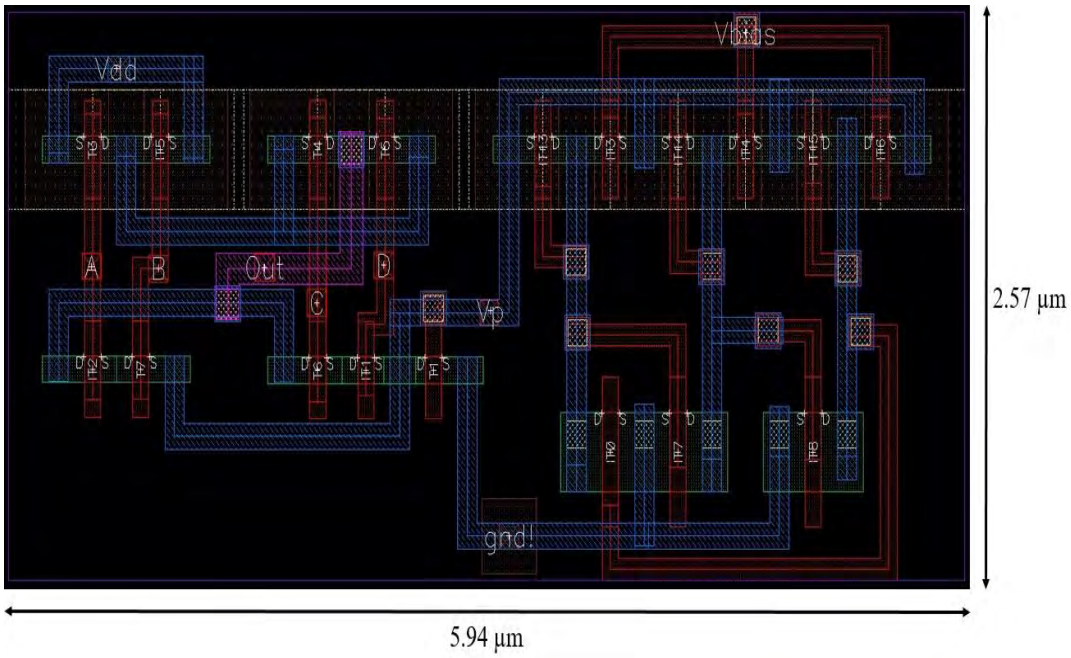


Fig. 4.17: Layout of SESLRO-based testing Method 2

4.6.1 Comparison between SESLRO-based Proposed Methods

The two proposed methods can be compared in terms of their influence on the output voltage level of the CUT, oscillator output curve at fault-free state, frequency of oscillation during faulty state and average power consumption during fault detection.

During the fault-free state in method 1, although the output logic level of the CUT remains detectable there is a slight degradation of the logic high voltage level as observed in Fig. 4.12. Whereas in method 2, no deterioration is observed for logic high after the integration of the active-load device (Fig. 4.14). However, the logic low voltage level in method 2 is degraded unlike in method 1. Comparing Fig. 4.13 and Fig. 4.15 for a TSON fault at T1, no significant change is obtained from the voltage output of the CUT in method 1, but in method 2 there is a clear fault detection from the voltage logic level.

In terms of oscillation at fault-free condition, it can be observed from Fig. 4.12 and Fig. 4.14 that the output of the oscillator is more stable in method 2 compared to method 1 where the output seldom tries to oscillate during transitions due to the current spikes. The frequency of oscillation and power penalty of the two methods may also be compared during faulty state. Average power consumption is measured during one complete cycle of inputs with the presence of a single fault. However, both the frequency and power dissipation are influenced by the location of the fault. A quantitative comparison is presented in Table 4.2. Rigorous simulation concludes that the corresponding data for faults in T1 and T6 in Table 4.2 represent any single TSON fault in the pull-up and pull-down networks, respectively. Variation in results for faults in other transistors of the same network is negligible.

Table 4.2: Comparison between the two testing methods

Method	**Output voltage of CUT in fault-free case (V)**	**Frequency of oscillation (GHz)**		**Power consumption (uW)**		**Area (um^2)**
		Fault in T_{PUN} (T1)	**Fault in T_{PDN} (T6)**	**Fault in T_{PUN} (T1)**	**Fault in T_{PDN} (T6)**	
1	Logic HIGH: 0.85-0.90 Logic LOW: 0	1.27	0.88	1.70	1.27	17.56
2	Logic HIGH: 1.20 Logic LOW: 0.35	0.61	0.97	1.06	1.68	15.27

4.7 Performance Assessment

Some important observations are discussed in this section which addresses the effects of integrating the multimode SESLRO with the CUT.

4.7.1 Power Penalty

Table 4.3 presents the power consumption overhead of the original test circuit for both fault-free and faulty conditions after integrating the test method using SESLRO. For the average power consumption measurement without the oscillator, the CUT is operated in its isolated state without the RO and additional transistors. The maximum recorded power penalty for each method is presented in the table. The power consumption overhead during fault-free state for method 1 is significantly high. On the other hand, the power consumption for method 2 is less than the standalone CUT. This is because the testing network is added in series with the CUT which increase the total impedance from supply to ground. In the fault-free state, one of the networks in the CUT is always non-conducting with a high impedance. Total power consumption after the integration of the oscillator is less than the isolated CUT during faulty condition due to the extra transistors in the CUT network which increases the equivalent resistance and, hence, reduce the overall current.

Table 4.3: Comparison of power penalty for CUT with and without integrated SERO

Fault-free condition		**Faulty condition**	
without SERO	**with SERO**	**without SERO**	**with SERO**
180.90 nW	309.50 nW (CCO, Method 1) 133.30 nW (VCO, Method 2)	4.07 μW	1.70 μW (CCO, Method 1) 1.68 μW (VCO, Method 2)

4.7.2 Behavior of Oscillator and CUT Outputs

In terms of the oscillation behavior of the oscillator, it can be observed from figures 4.5-4.7 and 4.12-4.13 that the use of current-controlled SERO causes some spurious oscillations. This phenomenon occurs every time the output of CUT rises from logic low to high. Although the spurious oscillation has a similar amplitude as the oscillation obtained during the presence of a fault, it is not a uniform and continuous oscillation throughout the period of the corresponding input vector. They include only one spike or an incomplete cycle with no measurable frequency. The user can verify that these are not caused due to a fault by applying a longer period of that corresponding input combination which will not continue the oscillation. In this way, the spurious oscillations are distinguishable from the high-frequency oscillations observed during the fault.

On the other hand, the use of voltage-controlled SESLRO causes degradation of the logic low level in the CUT for both fault-free and faulty conditions. The voltage V_P acts as a virtual ground and is not exactly at 0 V. Therefore, an approximate value of 350mV is obtained for logic low at the output of the CUT. Moreover, when the output voltage switches from logic high to low, there is a spike in the voltage level of V_P which slowly decreases to the value of 350 mV. This causes a delay in the output voltage when switching to logic low. Typically, for a voltage swing between 0 V and 1.2 V, the decision level for a logic value is the midpoint i.e. 0.6 V. Output voltage below 0.6 V can be considered logic low, while output signal above 0.6 V can be considered logic high. For a supply rail swing of 1.2 V, the difference between the two logic levels obtained were approximately 0.9 V for both methods. Moreover, some presented circuits in literature using carbon nanotube FET (CNTFET) obtained a lower output voltage swing. Therefore, the degradation in the output logic can be considered in the acceptable range and the voltage levels can be properly assigned to a particular logic level.

4.7.3 Adaptable Threshold Regulation

The proposed fault testing methods can be utilized as both off-chip and on-chip testing schemes for CMOS circuits with wide range of supply voltages. Each testing method may provide a better indication of the fault's presence than the other for specific fault locations, as shown in Table 4.2. The user will have the options between both test circuits for the off-chip testing method to effectively detect the fault. In the case of on-chip testing, the SESLRO and the additional transistors act as a BICS for the CUT.

In the high leakage regime, the increase in current due to faults is insignificant and is difficult to distinguish from the high quiescent current due to leakage. However, in the proposed methods, the increased current in the presence of a fault will be directly reflected at the oscillator's output through the presence of an oscillation. The SESLRO and current mirror devices can also be sized accordingly to detect the smallest possible increase in current due to a fault. This makes the proposed methods more effective in deep submicron technology compared to the conventional I_{DDQ} method. Moreover, the proposed RO architecture with its load adaptation provides regulation of the threshold current for

different supply voltages through the gate bias voltage (V_{bias}) of the split-load, which will trigger oscillation.

Figure 4.18 shows the oscillator response for a fault in transistor T1 at a higher supply rating of 2 V. Three observations can be perceived from this output response. First, the proposed testing method is still successful in detecting the fault through increased frequency of oscillation at the corresponding test vectors. Next, the scenario of high leakage current is produced by increasing the supply which creates undesired oscillations for different input vectors. This means that the SERO will also generate oscillation during fault-free state. In such circumstances, the threshold regulation through the V_{bias} voltage of the proposed split-load technique eliminates the oscillation at input pattern other than the test vectors. Finally, the spurious oscillations of Method 1 can be reduced through similar fashion.

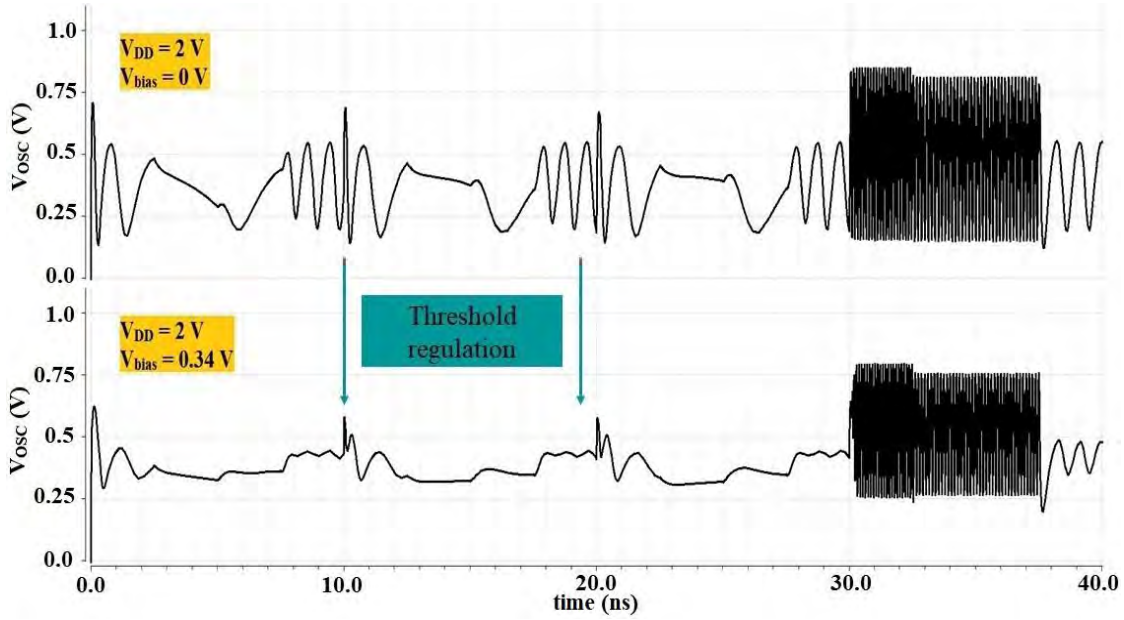


Fig. 4.18: Threshold regulation at increased supply rating reflecting high leakage

4.7.4 Built-in Current Sensor (BICS) Performance and Comparison with Literature

Several built-in current sensor (BICS) circuits are presented in the literature [62, 71-73] which are more complex in circuitry and operation and use a higher number of transistors compared to the proposed design in this work. Nuernbergk *et. al.* [62] proposes

a hugely complex circuit with capacitors, resistors, comparators, data converters and switches. Passive elements require more die area and are difficult to fabricate which increases the cost of production. The proposed method, therefore, provides improved area and cost-effectiveness. The circuit in [71] uses two types of active devices (MOSFETs and BJTs) and a separate reference voltage is required, while the circuit in [72] requires a diode and a separate reference current. Whereas, the proposed method with current-controlled RO uses the same supply voltage as the CUT. Bastos *et. al.* present several BICS circuits which are connected to the bulk terminals of the PMOS and NMOS transistors [73]. As a result, separate BICS circuits are required for the pull-up and pull-down networks of the CUT. Based on the circuitry of the existing architectures, it can be estimated that the proposed methods will have lower power and area overhead. A brief comparison of the proposed methods with few other existing works including BICS are presented in Tables 4.4 and 4.5 for oscillation based and I_{DDQ} based detection, respectively. Some data which are unavailable in the reference are blank. The use of BICS, however, results in performance degradation of the CUT in normal operation. In order to mitigate these issues, an auxiliary control mechanism with a circuit partitioning technique may be used, which simultaneously increases circuit complexity, power penalty and area requirement significantly.

Table 4.4: Comparison with existing BICS circuits for oscillation based detection

Test Method	[64]	[65]	[67]	Proposed Method
Process (nm)	65	250	65	90
Supply (V)	1.0	3.3	1.0	1.2
Area (μm^2)	-	-	69,300	17.56 (method 1) 15.27 (method 2)
Fault-free Frequency (GHz)	0.47	1.37	0.29	No oscillation
Frequency during fault (GHz)	0.46 (leakage) 0.48 (open)	0.66	0.41	1.27 (method 1) 0.97 (method 2)
Elements in BICS	multiplexers, buffers	Counters, latch, logic gates	Controller circuit, JTAG interface, counter, comparator, logic gates	11 transistors (method 1) 10 transistors (method 2)
Fault detected	Leakage and open	Delay	Micro-voids or incomplete filling	Transistor stuck-on

Table 4.5: Comparison with existing BICS circuits for I_{DDQ} based detection

Test Method	[74]	[75]	[76]	Proposed Method
Process (nm)	100	180	800	90
Supply (V)	1.2	1.5	2.5	1.2
Power (µW)	11.32	1300	-	1.70 (method 1) 1.68 (method 2)
Elements in BICS	27 transistors	9 transistors	14 transistors + 2 reference current sources	11 transistors (method 1) 10 transistors (method 2)
Fault detected	Single event upset (current injection)	Bridging and open	Transient	Transistor stuck-on

Chapter 5

Conclusions and Future Scopes

In this chapter, we conclude about the proposed multi-mode SESLRO structure with wide tuning benefits and its application in TSON fault detection in CMOS circuits. Finally, we discuss the possible scope of future work to improve the performance of the architecture and extend its application for detection of other types of faults.

5.1 Summary

Design of ROs with wide frequency band is crucial for communication systems as it enables maximum utilization of the frequency spectrum. On that basis, a CMOS ring VCO is designed in 90 nm technology with a wide frequency tuning property while maintain a cap on the power penalty. For a supply voltage variation of 0.3 V – 2 V, a frequency range of 3.93 MHz – 25.34 GHz is obtained while addressing the parasitic effects, which is the highest tuning range when compared with state-of-the-art architectures. The proposed SESLRO structure offers fine-tuning of the frequency in addition to coarse-tuning for greater coverage and more precise regulation of the frequency band. The split-load technique simultaneously reduces the parasitic capacitance and increases the current driving capability of the delay structure, and hence,

improves the operating-point of the oscillator. The maximum power consumption of the circuit was only 0.63 mW for a supply voltage of 2 V. The frequency of the oscillator is expressed as a function of number of stages N, tuning voltages V_{DD} and V_{bias}, and width ratio W_R of NMOS to PMOS transistors separately. To ensure the accuracy of the relation, RMSE and R^2 values are calculated. A general expression in terms of all the controlling parameters is generated with a value close to 1 for the R^2 parameter. A comparison between the simulated data and empirical model implies the use of the model for estimation of the oscillating frequency.

For the TSON fault detection, the SESLRO is used as a current-controlled oscillator with additional current mirror transistors in one of the methods. In the second method, the oscillator is used as a voltage controlled oscillator with an additional NMOS load. Both methods successfully detect the presence of the stuck-on fault through the triggering of oscillation at the output node of the oscillator during faulty condition. Comparison between the two methods are made in terms of the impact they have on the output voltage of the CUT during fault-free condition. While the first method degrades the voltage level of logic '1', the second method degrades the level of logic '0'. However, the degradations are equal and considered acceptable as the total voltage swing remains significantly high for correct interpretation of the two logic levels. The methods are also compared in terms of oscillating frequency and power penalty during faulty condition, and total area requirement. Although different fault locations generate different values for frequency and power, method 1 has a higher average frequency and power consumption. Meanwhile, the second method is more area efficient. Both methods can be utilized in off-chip as well as on-chip testing schemes for CMOS circuits with wide range of supply voltages. When compared with state-of-the-art BICS architectures, the proposed methods eliminate device-heavy compound circuitry, has a higher frequency for oscillation-based testing, and lower area overhead.

5.2 Future Scopes

1. The SERO structure with its load adaptation in this work provides a wide frequency tuning range and low power penalty, but at the cost of poor phase noise performance. The impact of the different controlling parameters such as transistor size and tuning voltages on the phase noise can be investigated to improve the noise performance. Increasing the transistor's width will have an adverse effect on the power consumption so optimization will be required.
2. Hybrid SEROs combine different RO structures to obtain each of their benefits. Therefore, other techniques like negative-skewed, current-starved or LC elements can be introduced with the SESLRO structure to analyze the frequency response and explore the effect.
3. Another limitation of the proposed oscillator is the decreased output voltage swing which could be improved by employing level shifter circuits.
4. The presented fault detection faces output voltage degradation of the CUT. Application of auxiliary control circuits may be explored to switch connections between standalone and testing modes, while maintaining low area and power overhead.
5. In this work, SERO based testing methods are used to detect faults in CMOS digital circuits. The proposed methods can be investigated in future for efficient fault and excess current detection in digital circuits involving pass-transistor logic or transmission-gate logic.
6. The proposed testing schemes are used to detect TSON events. However, other types of faults such as stuck-open and bridging also frequently occur in CMOS circuits and performance of the presented test methods in their detection can be assessed.

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List of Publications

JOURNAL

1. S. M. I. Huq, A. Roy, M. Ahmed, and A. U. Mahin, "Efficient Detection of Transistor Stuck-ON Faults in CMOS Circuits using Low-Overhead Single-Ended Ring Oscillators," *Springer Journal of Computational Electronics*, vol. 19, no. 4, pp. 1685–1694, 2020.
2. S. M. I. Huq, and A. Roy, "Relative Design Merits and Trends in Single-Ended Ring Voltage Controlled Oscillators," *IETE Journal of Research*, Vol. 2019. DOI: 10.1080/03772063.2019.1656557

CONFERENCE PROCEEDING

1. S. M. I. Huq, and A. Roy, "Design of Linearized Split-Load Low Power Single-Ended Ring Oscillator with High Tuning Range," in Proceedings of *2nd International Conference on Innovation in Engineering and Technology (ICIET),* 2019, pp. 1-6.