BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2019-2020

Sub : **EEE 303** (Digital Electronics)

Full Marks : 210 Time : 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks.

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE** questions.

1. (a) Find the minimum-cost POS expression for the function $f(x_1, x_2, x_3\, x_4) = \sum_m (0, 2, 8, 9, 10, 15) + D(1, 3, 6, 7)$ using k-map. Implement the function using NOR gates only and determine the cost. Assume that the input variables are available in both uncomplemented and complemented forms. **(25)**

   (b) Write the vering code for behavioral specification of the function *f* in Question 1(a). **(10)**

2. (a) Perform the following operation involving four-bit 2′s complement numbers and indicate whether arithmetic overflow occurs. Check your answers by converting to decimal sign and magnitude representation. **(15)**

$$\begin{array}{r} 1010 \\ +1101 \\ \hline C_4\ s_3\ s_2\ s_1\ s_0 \end{array}$$

   (b) Draw a circuit to determine the arithmetic overflow using s_3 in question 2(a). **(10)**

   (c) Write the verilog code for an n–bit adder with the option to determine the arithmetic overflow using s_3 and other available signals. For simplicity, take n=4 as parameter. **(10)**

3. (a) For the function $f(w_1, w_2, w_3) = \Sigma_m(0, 4, 6, 7)$, use Shannon's expansion to derive an implementation using a 2 – to – 1 multiplexer with ω_3 as the selector of the multiplexer. Use other necessary gates as required. **(10)**

   (b) Implement the function $f(w_1, w_2, w_3) = \Sigma_m(0, 2, 5, 7)$ by using a 3 – to – 8 binary decoder and associated gates. **(5)**

   (c) Design and implement a 4 – to – 2 priority encoder which gives higher priority to lower order lines. The cost of the designed encoder should be minimum. **(10)**

   (d) Write verilog code for the 4 – to – 2 priority encoder in Question 3(c). **(10)**

4. (a) Write the verilog code for implementing the following ALU functions depending on the inputs $s_2\ s_1\ s_0$. **(12)**

Contd P/2

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Contd ... Q. No. 4(a)

Operation	Inputs (s_2 s_1 s_0)	Outputs (F)
Clear	000	0000
B – A	001	B – A
2 bit right shift	010	2 bit right shift of F
2 bit left shift	011	2 bit left shift of F
ADD	100	A+B
NOR	101	A NOR B
XNOR	110	A XNOR B
Preset	111	1111

(b) If P = 4′ b110 x, Q = 3′ b11x and *f* is a scalar then

Evaluate: **(12)**

(i) P & Q
(ii) P ∧ Q
(iii) f = P | Q
(iv) f = P && Q
(v) f = ∧ P
(vi) {2{P}, 2{Q}}

(c) With an example clearly describe the differences between blocking and non-blocking assignments for combinational circuits. **(6)**

(d) With an example clearly describe what is meant by implied memory in verilog? **(5)**

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Design a four-bit shift register with parallel load using D flip-flops. There are two control inputs: shift and load. When shift = 1, the content of the register is shifted by one position. New data are transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change. Draw the circuit diagram of your system and write the corresponding Verilog code to implement it. **(15)**

(b) A digital system has a clock generator that produces pulses at a frequency of 80 MHz. Design a circuit that provides a clock with a cycle time of 100 ns. **(10)**

(c) Design a modulo-7 counter, which counts in the sequence 0, 1, 2, 3, 4, 5, 6, 0, 1.... The counter counts the clock pulses if the enable input w, is equal to 1. Use D flip-flops in your circuit. **(10)**

6. (a) Design a Mealy-type FSM 3-bit sequence detector that would have input, w and output, z. If a 3-bit sequence detected equals to 000 or 111, the output z will be 1, otherwise z will be 0. Draw the state diagram, write the state table, and minimize the states. Write the excitation table and implement the detector with a circuit diagram. **(15)**

(b) A sequential circuit has three flip-flops A, B, C; one input x_in; and one output y_out. The state diagram is shown in Fig. for Q 6(b). The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states. **(10)**

Contd P/3

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Contd ... Q. No. 6(b)

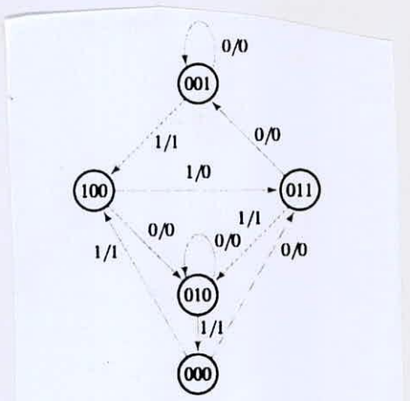

Fig. for Q 6(b).

(c) Design a sequential circuit with two JK flip-flops A and B and two inputs E and F. If E = 0, the circuit remains in the same state regardless of the value of F. When E = 1 and F = 1, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When E = 1 and F =0, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats. **(10)**

7. (a) The 32 * 6 ROM, together with the 20 line, as shown in Fig. for Q 7(a), converts a six-bit binary number to its corresponding two-digit BCD number. For example, binary 100001 converts to BCD 0011 0011 (decimal 33). Write the truth table for the ROM. **(10)**

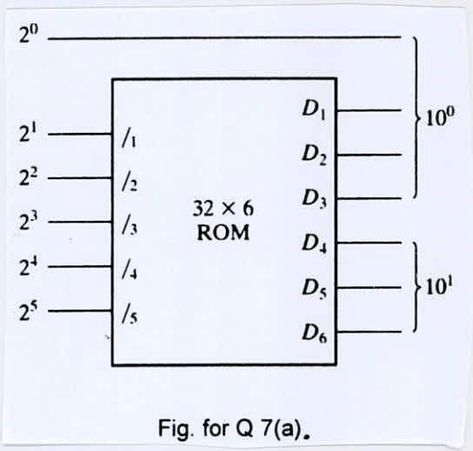

Fig. for Q 7(a).

(b) Using 64 * 8 ROM chips with an enable input, construct a 512*8 ROM with eight chips and a decoder. **(10)**

(c) Give the truth table for the CMOS circuit in Fig. for Q 7(c). Derive the simplest sum-of-products expression for the truth table. **(10)**

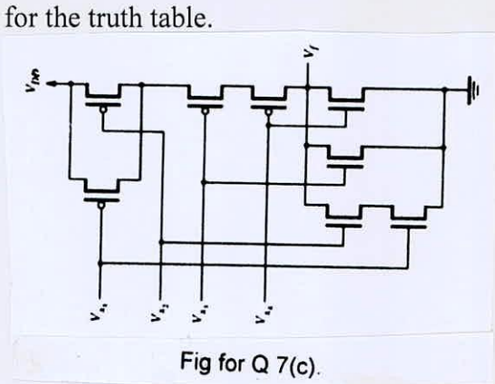

Fig for Q 7(c).

Contd P/4

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Contd ... Q. No. 7

(d) Fig for Q 7(d) shows half of a CMOS circuit. Derive the other half that contains the NMOS transistors. **(5)**

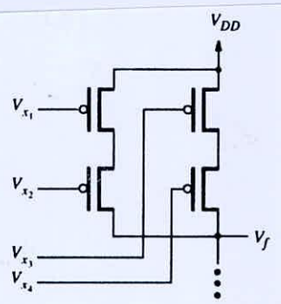

Fig for Q 7(d).

8. (a) Derive the minimal Moore-type flow table specifies the same functional behavior as the flow table in Fig. for Q 8(a). Draw the state diagram for the system. **(20)**

Present state	Next state w_2w_1 = 00	01	10	11	Output z
A	(A)	B	C	–	0
B	K	(B)	–	H	0
C	F	–	(C)	M	0
D	(D)	E	J	–	1
E	A	(E)	–	M	0
F	(F)	L	J	–	0
G	D	(G)	–	H	0
H	–	G	J	(H)	1
J	F	–	(J)	H	0
K	(K)	L	C	–	1
L	A	(L)	–	H	0
M	–	G	C	(M)	1

Fig for Q 8(a).

(b) A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in Fig. for Q 8(b). Derive the state table and state diagram of the sequential circuit. Write a Verilog code to implement the circuit. **(15)**

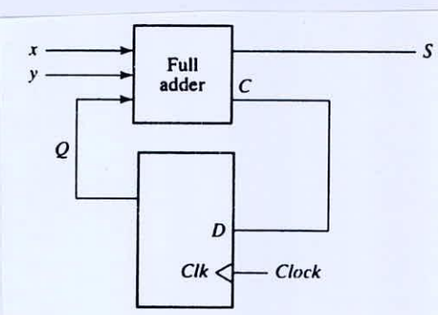

Fig for Q 8(b)

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L-3/T-2 B. Sc. Engineering Examinations 2019-2020

Sub: **EEE 313** (Solid State Devices)

Full Marks: 210 Time: 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks

The symbols have their usual meanings. Assume reasonable values for any missing data.

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE** questions.

Question ONE (1) is Compulsory.

1. (a) A 100 μm long Si bar at room temperature in steady state has the energy band diagram indicated in Fig. for Q(1). Assuming $E_{Fp} = E_F$, answer the following with explanation. **(25)**

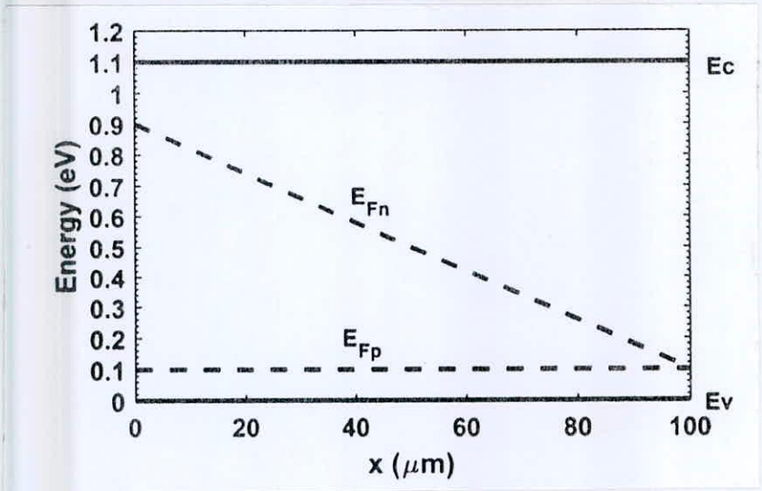

Fig. for Q(1)

i. Is the sample-
- In thermal equilibrium/ out of equilibrium
- Uniformly doped/ nonuniformly doped
- n type / p type
- Intrinsic/extrinsic
- Excited with low-level / high-level injection

ii. Estimate the electron and hole diffusion current densities at x = 0.

iii. Estimate the hole drift current density at x = 0.

iv. Quantitatively sketch all the current components and the total current as a function of x.

(b) In a silicon sample doped with 10^{17} cm^{-3} of phosphorus atoms, what fraction of the donors are not ionized if the donor level is located at 45 meV below the conduction band. (Assume $N_c = 2.8 \times 10^{19}$ cm^{-3} and donor degeneracy factor = 2.) **(10)**

Contd P/2

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2. (a)

N-type	P-type
$N_d = 5 \times 10^{17}$ cm^{-3}	$N_a = 10^{17}$ cm^{-3}
$D_p = 12$ cm^2/s	$D_n = 36.4$ cm^2/s
$\tau_p = 1$ μs	$\tau_n = 2$ μs

A 0.6 V forward bias is applied to the Si diode. (a) What are the diffusion lengths on the N side and the P side? (b) What are the injected excess minority carrier concentrations at the junction edge? (c) What is the majority carrier profile on the N side? (d) Sketch the excess carrier densities. (e) Sketch the energy diagram, including $E_{Fp}(x)$ and $E_{Fn}(x)$ (the quasi-Fermi levels). **(20)**

(b) Consider an n-type silicon sample doped with $N_D = 10^{17}$ cm^{-3}. **(15)**

i. Find the location of the equilibrium Fermi level.

ii. Find the quasi Fermi levels when excess carriers are introduced such that $\delta_n = \delta_p = 10^{15}$ cm^{-3}.

(Assume $N_C = 2.8 \times 10^{19}$ cm^{-3} and $N_V = 1.04 \times 10^{19}$ cm^{-3}.)

3. (a) The slope of $1/C^2$ vs. V_R characteristic for a Si p-n junction is 2×10^{23} F^{-2}V^{-1} and the intercept on the x-axis is at -0.84 V. The area of the junction is 1 μm^2. There is no way to determine whether the lightly/heavily doped side is the n or p side. However, one can determine the doping values for both sides. Find the heavier and lighter doping concentrations. **(20)**

(b) A Si p+n junction has $N_A = 10^{20}$ cm^{-3} and $N_D = 10^{17}$ cm^{-3}. What is **(15)**

i. the built-in potential?

ii. the total depletion width?

iii. the extension of the depletion region in p-side?

iv. the extension of the depletion region in n-side?

4. (a) Consider an ideal silicon pn junction diode with the doping concentrations $N_A = 5 \times 10^{16}$ cm^{-3} and $N_D = 1.5 \times 10^{16}$ cm^{-3}, and the minority carrier lifetimes $\tau_{n0} = 2 \times 10^{-7}$ s and $\tau_{p0} = 8 \times 10^{-8}$ s. The cross-sectional area is $A = 5 \times 10^4$ cm^2. Calculate (a) the ideal reverse-saturation current due to holes, (b) the ideal reverse-saturation current due to electrons, (c) the hole concentration at $x = x_n$ for $V_a = 0.8V_{bi}$, (d) the electron current at $x = x_n$ for $V_a = 0.8\ V_{bi}$, and (e) the electron current at $x = x_n + (1/2)\ L_p$ for $V_a = 0.8V_{bi}$. (Assume $D_p = 10$ cm^2/sec and $D_n = 25$ cm^2/sec.) **(20)**

Contd P/3

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Contd... Q. No. 4

(b) Assume that an n-type semiconductor is uniformly illuminated, producing a uniform excess generation rate g'. Show that in steady state the change in the semiconductor conductivity is given by **(15)**

$$\Delta\sigma = e(\mu_n + \mu_p)\tau_{p0}g'.$$

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. Find the donor concentration and barrier height of the W-GaAs Schottky barrier diode shown in Fig. for Ques. No. 5. Compare the barrier height with that obtained from the saturation current density of 5×10^{16} A/cm^2. For n-type GaAs, A* = 8 A/K^2–cm^2. For a reverse bias of -1 V, calculate the depletion-layer width W, the maximum field, and the capacitance. **(35)**

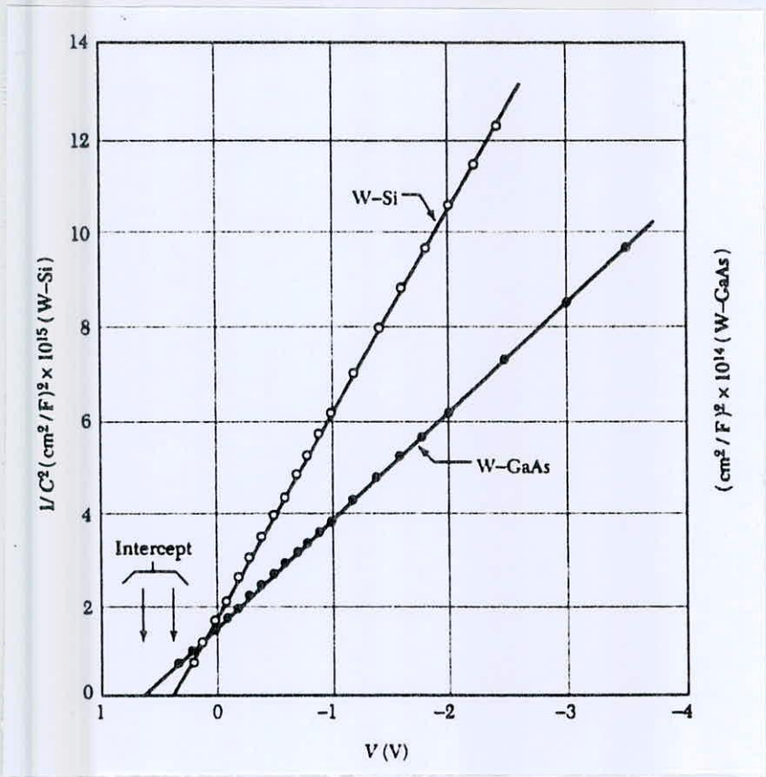

Fig. for Ques. No. 5

6. Consider a uniformly doped silicon npn bipolar transistor at T = 300 K. The device is biased in the forward-active mode with the B-C junction reverse biased by 3 V. The metallurgical base width is 1.1 μm. The doping concentrations are $N_E = 10^{17}$ /cm^3, $N_B = 10^{16}$ /cm^3, and $N_C = 10^{15}$ / cm^3. Determine the B-E voltage such that minority carrier election concentration, at x = 0 is 10 percent of the majority carrier hole concentration. At this bias, determine the minority carrier hole concentration at x′ = 0. Determine the neutral base width for this bias. **(35)**

Contd P/4

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7. (a) Consider an MOS device with the following parameters: p^+ polysilicon gate, n-type substrate, t_{ox} = 220 Å, and $Q'_{ss} = 10^{10}$ /cm^2. Use Fig. for ques. No. 7. Determine the n-type doping concentration such that threshold voltage is in the range

$$-0.50 < V_{TP} < -0.30 \text{ V}.$$ **(25)**

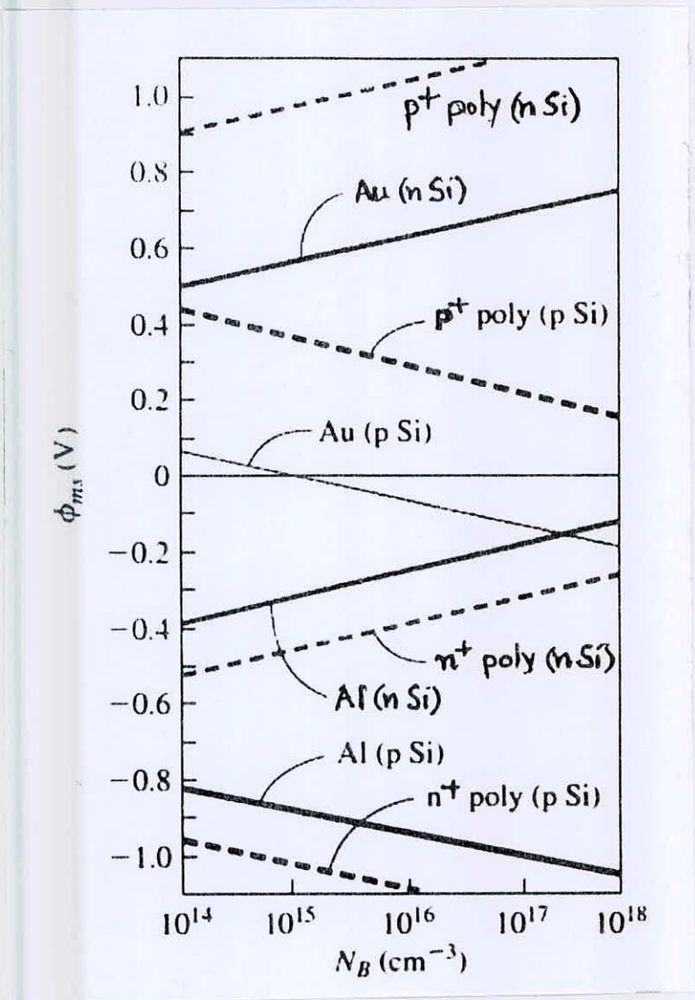

Fig. for Ques. No. 7

(b) Consider an MOS structure with a p-type semiconductor substrate doped to $N_a = 10^{16}$ /cm^3, a silicon dioxide insulator with a thickness of t_{ox} = 200 Å and an oxide charge of $Q'_{ss} = 8 \times 10^{10}$ /cm^2, calculate the flat-band voltage. Use Fig. for Ques. No. 7. **(10)**

8. (a) For a metal-SiO_2–Si capacitor having $N_a = 5 \times 10^{16}$ /cm^3 and t_{ox} = 8 nm, calculate the minimum capacitance, oxide capacitance, and flat-band capacitance on the C-V curve. **(25)**

(b) Draw the structure of a FinFET and compare its performance with a MOSFET. **(10)**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2019-2020

Sub: **EEE 315** (Power Electronics)

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks

USE SEPARATE SCRIPTS FOR EACH SECTION

All the symbols and notations used bear their usual meanings.

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE** questions.

1. (a) Explain the operating principal of an SCR using the two-transistor model. **(10)**

   (b) Describe how 'natural commutation' and 'forced commutation' happen with at least 1 static power semiconductor device for each type. **(12)**

   (c) Based on the I/O voltage levels, classify DC choppers or DC-DC converters. Draw necessary circuit diagrams and waveforms for each class. **(13)**

2. (a) What is the fundamental difference between a chopper and a DC voltage regulator? **(5)**

   (b) Draw a step-down chopper circuit with resistive load and prove that the rms value of output voltage is $V_0 = \sqrt{D}V_S$ where D = duty cycle and V_S = input DC voltage. **(12)**

   (c) The DC converter in **Fig. for Q. No. 2(c)** has a resistive load, R = 15 Ω and input voltage, V_S = 240 V When the converter remains on, its voltage drop is V_H = 1.75 V and chopping frequency is f = 15 kHz. If the duty cycle is 90%, determine- **(18)**

   (i) the average output voltage V_a, (ii) the rms output voltage V_o, (iii) the converter efficiency, (iv) the effective input resistance R_i, and (v) the rms value of the fundamental component of harmonics on the output voltage.

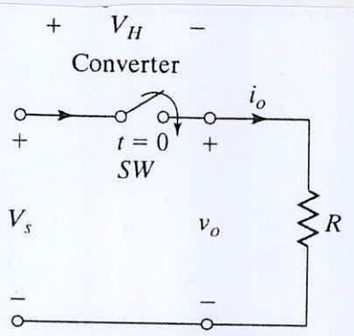

Fig. for Q. No. 2(c).

EEE 315

3. (a) For a three-phase bidirectional AC voltage controller, draw the (i) circuit diagram (ii) waveforms for input phase voltages, Thyristor gate pulses, and output phase voltage (for $\alpha = 60°$) **(16)**

(b) For the single-phase full-wave AC voltage controller circuit shown in the **Fig. for Q. No. 3(b)**, $v_s = \sqrt{2}V_s \sin(\omega t)$ is the input voltage, and the delay angles of thyristors T_1 and T_2 are equal $(\alpha_2 = \pi + \alpha_1)$. Drive the rms output voltage V_o. What will be the range of V_o? **(12)**

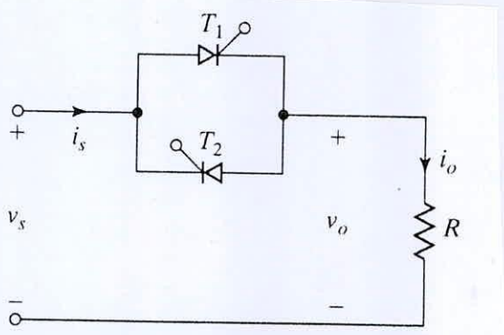

Fig. for Q. No. 3(b).

(c) For the circuit shown in the **Fig. for Q. No. 3(b)**. $R = 10\,\Omega$, $V_{rms} = 230$ V, 50 Hz. The delay angles of thyristors T_1 and T_2 are: $\alpha_1 = \alpha_2 = \alpha = \pi/2$. Determine the rms output voltage V_o. **(7)**

4. (a) What is the basic difference between an AC voltage controller and a cycloconverter? **(5)**

(b) The input voltage to the cycloconverter shown in the **Fig. for Q. No. 4(b)** is 120 V (rms), 60 Hz. The load resistance is 5 Ω and the load inductance is L = 40 mH. The frequency of the output voltage is 20 Hz. If the converters are operated as semiconverters such that $0 \le \alpha \le \pi$ and the delay angle is $\alpha_p = 2\pi/3$, determine (i) the rms value of output voltage V_o, (ii) the rms current of each thyristor I_R, and (iii) the input power factor. **(15)**

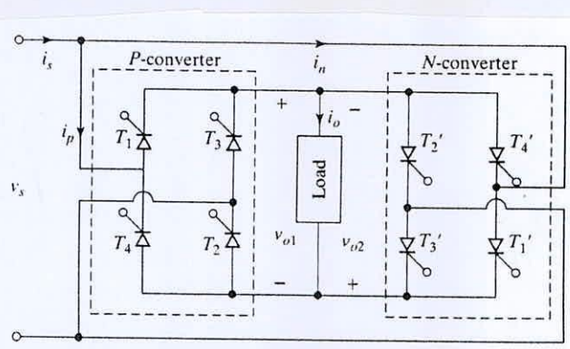

Fig. for Q. No. 4(b).

(c) Draw the (i) circuit diagram, (ii) line voltages, (iii) output voltage, and the (iv) conduction periods for P and N converters of a 3-phase/1-phase cycloconverter. Again, draw the circuit diagram of a 3-phase/3-phase cycloconverter. **(15)**

Contd P/3

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SECTION – B

There are **FOUR** questions in this section. Answer any **THREE** questions.

5. (a) Draw the circuit diagram of a single-phase full-wave AC-DC converter with R–L load and derive the expression of the rms and average current of a thyristor and output. **(17)**

(b) The Y-connected three-phase full wave AC-DC converter has a load of L = 1.5 mH, R = 1.5 Ω, and E = 0 V. The line-to-line input voltage is V_{ab} = 208 V (rms), 60 Hz. The delay angle is $\alpha = \pi/6$. Determine (i) the steady-state load current I_1 at $\omega t = (\pi/6 + \alpha)$, (ii) the rms output current I_{rms}, and (iii) the average output current I_{dc}. **(18)**

6. (a) The three-phase inverter operating in 180° conduction mode has star-connected resistive load. Derive the expression of line-to-line rms voltage and the DC supply current. **(17)**

(b) The three-phase inverter operating in 180° conduction mode has a Y-connected load of R = 10 Ω and L = 15 mH. The inverter frequency is f_0 = 50 Hz and the dc input voltage is V_s = 220 V. Calculate (i) the THD, (ii) the Distortion factor (DF), (iii) the Harmonic factor (HF) and DF of the Lowest order harmonic (LOH), and (iv) the load power P_o. **(18)**

7. (a) Classify inverters. Explain the performance parameters of inverters. **(3+12=15)**

(b) What is space vector modulation (SVM)? With a block diagram explain how the switching time for a three-phase inverter is calculated in each state in SVM. **(20)**

8. (a) Write short notes on different Types of HVDC Links and HVDC systems. Draw the schematic diagram of a typical HVDC Transmission Station and point out the main components. **(12+8=20)**

(b) Describe the advantages and disadvantages of Variable Speed Drives. **(15)**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2019-2020

Sub: **EEE 317** (Control System I)

Full Marks: 250 Time: 3 Hours

The figures in the margin indicate full marks

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE** questions.

All the symbols have their usual meanings. Assume reasonable values for missing data.

1. (a) Using the Routh-Hurwitz criterion and the unity feedback system of Fig. for Q. N. 1(a) with **(20)**

$$G(s) = \frac{K}{s(s+1)(s+2)(s+5)}$$

(i) Find the range of K for stability

(ii) Find the value of K for marginal stability

(iii) Find the actual location of the closed-loop poles when the system is marginally stable.

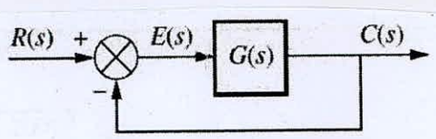
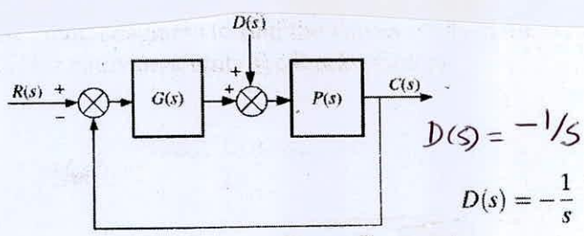


Fig. for Q. No. 1(a)

(b) For the system in Fig. for Q. N. 1(b), find the total steady-state error due to a command input R(s) and disturbance D(s) applied simultaneously. **(15)**



$R(s) = \frac{3}{s}$ $D(s) = -\frac{1}{s}$

$G(s) = 5$ and $P(s) = \frac{7}{s+2}$.

Fig. for Q. No. 1(b)

2. (a) For the system represented by Fig. for Q. N. 2(a), find the transfer function T(s), where, $T(s) = C(s)/R(s)$. **(17)**

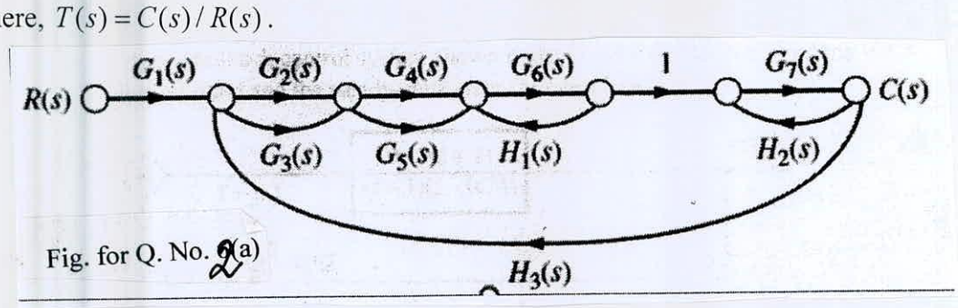


Fig. for Q. No. 2(a)

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Contd... Q. No.2

(b) For the system shown in Fig. for Q. N. 2(b), find the gain margin and phase margin if the value of K is 100. **(18)**

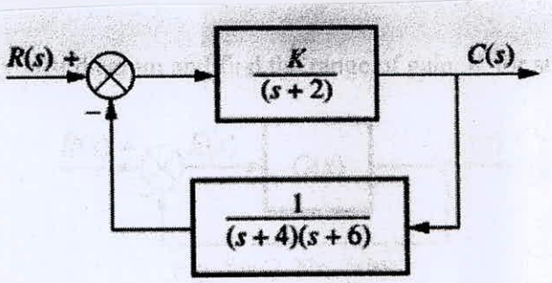

Fig. for Q. No. 2(b)

3. (a) For a unity feedback system with **(20)**

$$G(s) = \frac{100K}{s(s+36)(s+100)},$$

using the frequency response method, design a Lead Compensator to yield a 20% overshoot and $K_v = 44$ with a peak time of 0.1 second.

(b) Explain how to use Bode Diagrams to find the values of the static error constants (Kp, Kv, Ka) for equivalent unity feedback systems. **(15)**

4. (a) For the feedback control system shown in Fig. for Q. N. 4(a), find the static error constant and the steady-state error for ramp input **(18)**

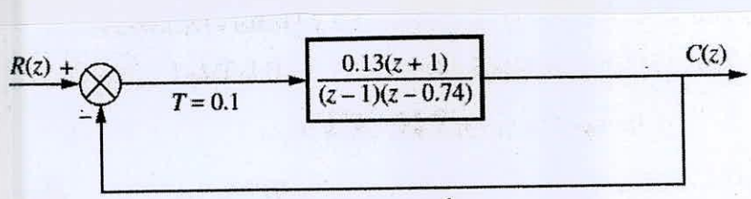

Fig. for Q. No. 4(a)

(b) For the system shown in Fig. for Q. N. 4(b), where **(17)**

$$G(s) = \frac{K}{(s+2)(s+4)(s+6)}$$

Plot the Nyquist diagram and find the range of gain, K for stability.

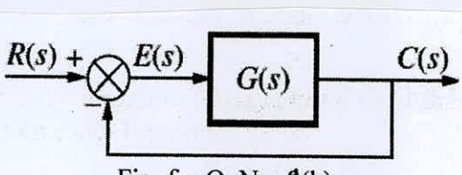

Fig. for Q. No. 4(b)

Contd P/3

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SECTION – B

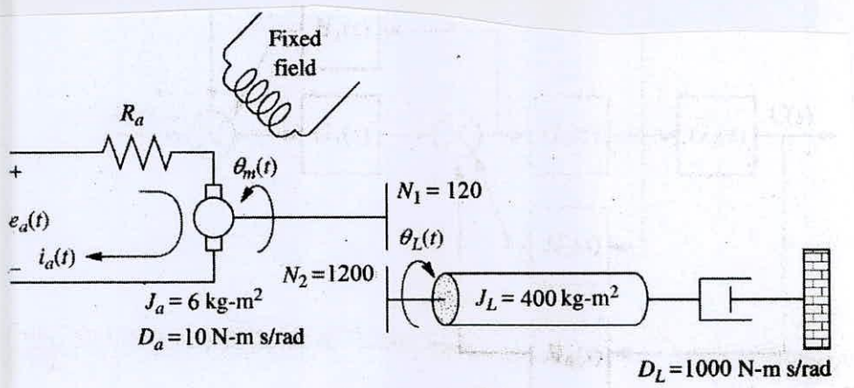
There are **FOUR** questions in this section. Answer any **THREE** questions.

All the symbols have their usual meanings. Assume reasonable values for missing data.

5. (a) Draw a functional block diagram showing clearly the different blocks necessary for antenna azimuth position control system. **(8)**

(b) For a second order system, the settling time T_s is found twice of the peak time T_p (i.e. $T_s = 2\ T_p$). Find the percentage overshoot. By changing the pole locations, if the percentage overshoot is doubled, find the new ratio of T_s and T_p. Also find the new pole locations if the peak time is now 0.33 sec. **(12)**

(c) For the DC motor control system shown in Fig. for Q. 5(c), motor torque constant $K_T = 5\ R_a$ and back emf constant $K_b = 2$. Find the overall transfer function $\frac{\theta_m(s)}{E_a(s)}$. **(15)**



Fog. For Q. 5(c)

6. (a) Represent the following transfer function is state space **(10)**

$$G(s) = \frac{(s^2 + 3s + 8)}{(s+1)(s^2 + 5s + 5)}$$

(b) Find the state-space representation from the block diagram shown in Fig. for Q. 6(b). Here x_1, x_2 and x_3 are state variables. **(10)**

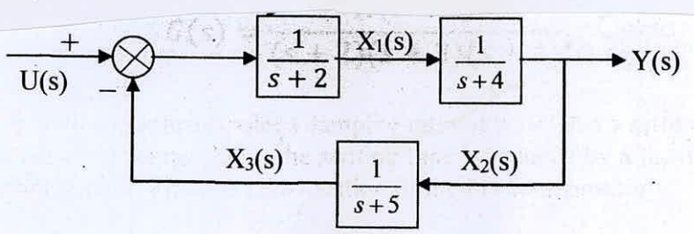


Fig. for Q. 6(b)

(c) From the state space representation shown below find the poles of the system and the state-transition matrix. **(15)**

$$\dot{\mathbf{x}} = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}\mathbf{x} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u(t)$$

$$y = \begin{bmatrix} 3 & 4 \end{bmatrix}\mathbf{x};\ \mathbf{x}(0) = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

Contd P/4

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7. (a) A negative unity feedback system has the following open-loop transfer function **(12)**

$$G(s) = \frac{K(s+6)}{(s+2)(s+3)(s+4)}$$

It is operating with two dominant-poles, a damping ratio of 0.707 and a settling time of T_s = 1.893. By using a PD compensator, the settling time is reduced by a factor of 2 keeping the same damping ratio. Find the zero location of the PD compensator.

(b) For a negative unity feedback system, the open-loop transfer function G(s) is given by **(23)**

$$G(s) = \frac{K(s-1)(s-2)}{s(s+1)}$$

Sketch the root locus indicating break-away, break-in and imaginary axis crossing points. Also find the range of gain to keep the system stable.

8. (a) Reduce the block diagram shown in Fig. for Q. 8(a) to a single block connecting the input R(s) and output C(s) by explicitly presenting the step-by-step reductions. Find the transfer function T(s) = C(s)/R(s) considering $G_1(s) = G_2(s) = G_3(s) = 1/s$, $H_1(s) = H_2(s) = s$ and $H_3(s) = H_4(s) = s^2$. **(12)**

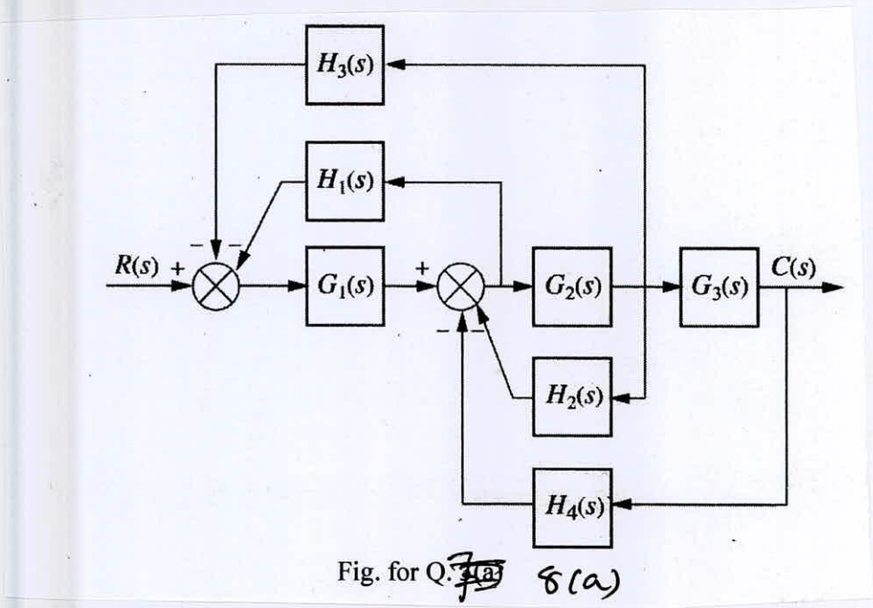

Fig. for Q. ~~7(a)~~ 8(a)

(b) Open-loop transfer function of a negative unity feedback system is given by **(23)**

$$G(s) = \frac{K}{s(s+4)(s+11)}$$

The uncompensated system is operating with 30% overshoot and peak time T_p = 0.953 sec. Design a lag-lead compensator with a compensating zero located at -4 that will decrease the peak time by a factor of 2, decrease the percent overshoot by a factor of 2, and improve the steady-state error by a factor of 30.

L-3/T-2/EEE **Date: 02/04/2022**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2019-2020

Sub: **IPE 493** (Industrial Management)

Full Marks: 210 Time: 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks

Assume reasonable value for missing data, IF ANY.

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE** questions.

1. (a) The Following tasks must be performed on an assembly line in the sequence and times specified in Table 1. **(10+5+20=35)**

Table 1 for Question 1.

Task	Task Time (Seconds)	Tasks That Must Precede other Tasks
A	50	---
B	40	---
C	20	A
D	45	C
E	20	C
F	25	D
G	10	E
H	35	B, F, G

(a) Draw the precedence diagram.

(b) What is the theoretical minimum number of stations required to meet a forecast demand of 400 units per eight-hour day?

(c) Use the longest-task-time rule (primary rule) and maximum number of following tasks rule (Secondary rule) and balance the line in the minimum number of stations.

2. (a) A company makes bicycles. It produces 450 bicycles a month. It buys the tires for bicycles from a supplier at a cost of $20 per tire. The company's inventory carrying cost is estimated to be 15% of cost and the ordering is $50 per order. Compute the economic order quantity (EOQ). Also calculate the cycle length in days. **(20)**

(b) Expected cash flows from an investment are as follows. Given the bank interest rate (cost of capital) of 13%, should you invest in this project by taking loans from the bank? Make your decision based on evaluating the internal rate of return (IRR). Show all the required calculations. **(15)**

Contd P/2

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Contd... Q. No. 2(b)

Table 2 for Question 2(b).

Year	Cash Flow ($)
0	-250,000
1	50,000
2	100,000
3	200,000

3. (a) The production scheduler for XYZ Machine Shop has six jobs ready to be processed that can each be assigned to any of six different workstations. Due to the characteristics of each job and the different equipment and skills at the workstations, the time to complete a job depends on the station it is assigned to. Table 3 shows the data on the jobs and the time it would take to do each job at each workstation. **(25)**

Table 3 for Question 3(a).

	Job Completion Time at Workstation (hours)					
Job	1	2	3	4	5	6
A	3.2	3.5	2.9	3	4	3.6
B	2.7	2.9	2.3	3	3.1	3.7
C	3.8	4	4.3	4.5	4.1	3.6
D	2.8	2.1	2.9	2.5	3	2.2
E	6.1	6.5	6.7	7	6	6.2
F	1.5	1.3	1.9	2.9	4	3.6

Required:

Using the Hungarian method, assign each job to a machine to minimize total processing time.

(b) Suppose you are a safety manager of a plastic manufacturing company. You are asked to find the possible root causes of electrical fire at the factory. How can you apply the idea of the Fishbone diagram to examine the root causes? **(10)**

4. (a) A company that operates 10 hours a day manufacturers three products on three processes. Table 4 summarizes the data. **(27)**

Table 4 for Question 4(a).

	Minutes per unit			
Product	Process 1	Process 2	Process 3	Unit price
1	10	6	8	$4.50
2	5	8	10	$5.00
3	6	9	12	$4.00

Required:

Using the Simplex method, determine the optimal product mix to maximize the profit.

Contd P/3

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Contd... Q. No. 4

(b) What is a product structure tree? Provide examples. **(8)**

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE** questions.

5. (a) According to Henry Fayol, what are the different skills that managers need to possess? Explain their variations at different Managerial levels with necessary example. **(6)**

(b) List the 14 management principles identified by Henry Fayol with necessary examples. **(14)**

(c) Discuss the contributions of Frank and Lillian Gilbreth. **(7)**

(d) Elaborate Hawthorne experiment. What are the insights obtained from it? **(8)**

6. (a) Discuss the origin of the 'Management Science School'. Explain how wars like World War II and Vietnam war influenced this school. **(13)**

(b) Explain Maslow's need theory with necessary example. **(7)**

(c) Elaborate Matrix type organizational structure. What are its advantages and disadvantages? **(8)**

(d) Briefly explain 'Task technology approach' of organizational design. **(7)**

7. (a) Discuss five bases of power with necessary examples. **(10)**

(b) Explain the advantages of delegation. What are the Steps of Delegation? **(10)**

(c) A company has the following actual demands in units over the 12 months period in 2021. Forecast their demand on January 2022. Use exponential smoothing technique to forecast. Assume the smoothing constant value to be 0.15. Also calculate the corresponding MAD, MAPE and TS. **(15)**

Months in 2021	1	2	3	4	5	6	7	8	9	10	11	12
Actual Demand	40	39	42	43	36	45	38	40	35	38	42	44

Contd P/4

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8. (a) Discuss 'Reinforcement theory' with necessary examples. **(8)**

(b) Discuss different types of formal team. What are the stages of team development? **(8+7=15)**

(c) For a certain industry worker, working in a factory, the following data is given. Guaranteed base rate = Tk 35 per hour. Total piece to be produced = 500 pieces. Standard Task = 200 pieces/hour, Low task would be 75% of the standard task. The worker took 3 hours to complete the job. Percentage of the workers' share in the gain of above task is 35%. Now, calculate the rate of incentive per hour for that worker- **(12)**

i. If the company follows Halsey's plan

ii. If the company follows Rowan's plan
