L-3/T-1/CSE **Date: 24/09/2022**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2020-2021

Sub: **CSE 305** (Computer Architecture)

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **NINE** questions in this section. Answer any **SEVEN** questions.

1. You have surely learnt about the eight big ideas of computer architecture. They are again mentioned below to brush up your memory: **(15)**

   - Design for Moore's Law
   - Use abstraction to simplify design
   - Make the common case fast
   - Performance via parallelism
   - Performance via pipelining
   - Performance via prediction
   - Hierarchy of memories
   - Dependability via redundancy

   Now identify the statements below best relate to which of the above ideas. Each statement should relate to a single idea. Elaborate the justification behind your answer.

   (a) Code reordering is done to avoid the use of load result in the next instruction.

   (b) Different caches for data and memory can effectively increase bandwidth.

   (c) As CPUs have hit their physical performance barrier due to power limit issues, GPUs have started gaining increased popularity among the programming community.

2. What is your most favorite topic learnt from processor, memory hierarchy, and multiprocessors? Describe briefly. **(15)**

3. A full datapath with a control unit is given in Figure 1. Highlight the datapath elements that will be active for the `ori $t1, 100($t2)` instruction. Also, mention which control bits will be set. [You may highlight the given figure and attach it to your answer script.] **(15)**

4. Suppose you are maintaining a 5-stage pipeline in a MIPS datapath. You are given the following code snippet to execute. Identify all the data hazards that can occur using a multi-cycle pipeline diagram and mark where there is a need for forwarding. Also

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Contd.... for Q. No. 4

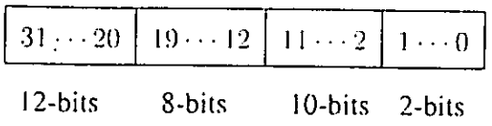
write down the forwarding conditions to mitigate the hazards. Can all of the hazards in this snippet be addressed using forwarding? Defend your position. Also write down the forwarding conditions to mitigate the hazards. Can all of the hazards in this snippet be addressed using forwarding? Defend your position. **(15)**

```
lw  $t0, 0($t1)
add $t0, $t0, $t1
add $t0, $t2, $t0
add $t0, $t0, $t3
sub $t1, $t2, $t3
and $t4, $t5, $t6
sw  $t0, 0($t6)
```

5. You are given the following code snippet and have been tasked to run multiple issues in parallel for faster execution. Refactor the code so that IPC is maximized. Also compute the effective IPC. [Hint: you do not have to limit the code to two issues.] **(15)**

```
Loop: lw   $t0, 0($s0)
      lw   $t1, 0($s1)
      addu $t0, $t0, $t1
      sw   $t0, 0($s1)
      addi $s0, $s0, -4
      addi $s1, $s1, -4
      bne  $s1, $zero, Loop
```

6. Answer the questions below for the following memory address subdivision and a 2-way set associate LRU cache: **(15)**



(a) How many distinct blocks of data can there be in the cache?

(b) In which cache index will the decimal address 24092022 map to?

(c) If a cache index is valid, what is the probability that one of its elements will have to be replaced in the next request? Assume each memory address has equal likelihood of being requested and each element in a cache index has equal likelihood of being filled.

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7. Suppose in a memory hierarchy there are four types of memories: **(15)**

Cache → RAM → SSD → HDD . Their local miss rates are 5%, 15%, 25%, and 0% respectively. Their access times are 1, 10, 100, and 1,000 cycles respectively. Now answer the following questions:

(a) What is the probability that a data will be fetched from the SSD?

(b) What is the expected time of a fetch?

(c) If the cache is separated into an I-cache and a D-cache, what will the miss rate of the I-cache be for a program that accesses data elements in 10% of its instructions if the overall miss rate remains constant (i.e., 5%) and the D-cache miss rate is 10%?

8. Suppose you have implemented an approximate LRU page replacement scheme using a reference bit for each page table entry. Your virtual memory has eight and page table has four entries. After every four time-steps, the reference bits are cleared. Assuming a fully set associative page table, simulate your page replacement scheme for the virtual memory reference below: **(15)**

0, 0, 2, 7, 0, 6, 1, 2, 6, 7, 1, 1, 7, 1, 4, 1

You have to print the page table after each page table reference. You also have to mention whether or not it is a hit or miss.

9. You want to perform two sums in a program: one is a sum of 8 scalar variables and another is a matrix sum of a pair of two-dimensional arrays of size 8 by 8. Assume you are doing these sums with 8 processors. **(15)**

(a) Assume only the matrix sum is parallelizable, what speed-up will you get with 8 versus 16 processors?

(b) Again assuming only the matrix sum is parallelizable, calculate the speed-up when the matrices grow to 16 by 16.

(c) Devise a recursive algorithm to speed-up the scalar sum and calculate the new speed-up.

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE** questions.

10. (a) Briefly explain the eight great ideas in Computer Architecture. **(12)**

(b) Suppose you want to design a 4-bit ALU where the inputs to the ALU are A $(A_3A_2A_1A_0)$ and B $(B_3B_2B_1B_0)$, and the selection variables are S_3, S_2, S_1 and S_0. Also, consider X_i, Y_i and Z_i as the inputs to the i-th parallel adder of the ALU. The

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Contd.... for Q. No. 10

ALU must satisfy the following functional design specification (given in Table 10b) that has to be realized through the parallel adders. Your task is to derive the input equations (X_i, Y_i and Z_i) for the parallel adders of the ALU. You must design using the least possible number of gates. **(18)**

S_3	S_2	S_1	S_0	Required Functions
0	0	0	0	$F = A$
0	0	0	1	$F = A - 1$
0	0	1	0	$F = A + B + 1$
0	0	1	1	$F = A + B$
0	1	0	0	$F = A - B$
0	1	0	1	$F = A - B - 1$
0	1	1	0	$F = A + 1$
0	1	1	1	$F = A$
1	0	0	X	$F = A'$
1	0	1	X	$F = AB'$
1	1	0	X	$F = A \odot B$ [XNOR]
1	1	1	X	$F = A \vee B$ [OR]

Table 10(b): Required functional design specification

(c) Briefly describe how to perform a signed multiplication operation. **(5)**

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11. (a) Suppose a hypothetical performance benchmark SPECBM101 runs on a computing system and the following data is obtained. **(10)**

Description	Execution Time (seconds)	Reference Time (seconds)
Program 1	?	9770
Program 2	527	10490
Program 3	586	12100
Program 4	109	20720
Program 5	470	7020
Program 6	275	6900

If the geometric mean of the benchmark is 28.74 seconds, what is the execution time of Program 1?

(b) Consider the following figure (Figure 11b) of a processor unit employing a scratchpad memory. How many micro operations does it require to complete an addition operation with two operands, and store the result? Which changes and constraints are required to reduce the number of micro operations to only one? **(2+6=8)**

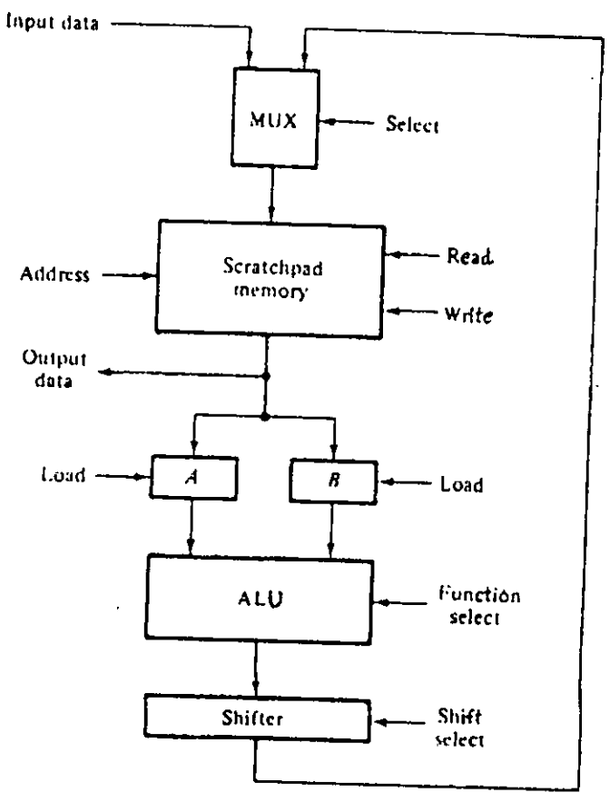

Figure 11(b): Processor unit employing a scratchpad memory

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Contd.... for Q. No. 11

(c) Write the equivalent efficiency sequence of MIPS instructions for the following C code fragment. **(12)**

```
int testFunc (int a, int b, int c)
{
  int i=0, result=0;
    do
    {
       if(i>b)
          result += c;
       i++;
    }while (i<a)

  return result;
}
```

Assume, $s1 and $s2 will carry the values of variable *i* and variable *result*, respectively.

(d) Provide an illustrative example for showing how MIPS architecture follows the design principle: "Good design demands good compromises." **(5)**

12. (a) The data for the two programs A and B are given below. **(8)**

Instruction Type	Clock Cycle per Instruction (CPI)	Instruction Count in Program A	Instruction Count in Program B
Multiplication	3	2	3
Addition	1	1	2
Subtraction	2	4	3
Division	4	2	2

Which program has the higher average clock cycle per instruction?

(b) Consider the following MIPS code: **(10)**

```
L1: bne $t0, $t1, L3
L2: j LX
L3: addi $t0, $t1, 1
```

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Contd.... for Q. No. 12(b)

Now, if the opcode of *j*, *bne* and *addi* are 2, 5 and 8 respectively, the register *$t0* and *$t1* are indicated by register values 8 and 9 respectively, and the addresses are

L1 → 1000

L2 → 1004

L3 →1008

LX → 131072

then, write down the instruction format name and the instruction values for each of the above-mentioned instructions. The following example is provided as a hint.

Example: Consider the following MIPS instruction:

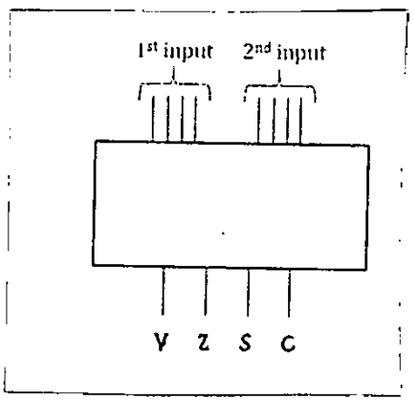
add $s1, $s2, $s3

The instruction format is R-format and instruction values should be:

Address	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
0400	0	18	19	17	0	0

(c) Briefly explain the importance of guard digit, round digit, and sticky bit during rounding an intermediate floating point number. **(9)**

(d) Consider the following module. **(8)**



This module takes two 4-bit inputs, and shows only the four status bits (V: Overflow, Z: Zero, S: Sign and C: Carry) considering the subtraction operation of the second input from the first input. If the first 4-bit input is expressed by A and second 4-bit input is expressed by B, draw the diagram of the complete circuit that can determine whether A>B, A=B, or A<B.

Contd P/8

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13. (a) Consider a 32-bit system where 24 bits are reserved for fraction, one bit for sign, and the rest for exponent. Answer the following questions. **(4×4=16)**

(i) Why is bias used during the floating point representation?

(ii) What should be the value of the bias for this system? Why?

(iii) What are the smallest and the largest absolute values that can be stored in this system?

(iv) What is the smallest denormalized number that can be stored using this system?

(b) How is address calculation performed in PC-relative addressing? **(7)**

(c) Write the equivalent efficient sequence of MIPS instructions for the following C code fragment. Assume appropriate registers for each of the variables. **(7)**

```
float a, b, c;
double w, x, y, z;
if (a+b>c)
    x=(y*z)/w;
```

(d) What are the main differences between x86 architecture and MIPS architecture? **(5)**

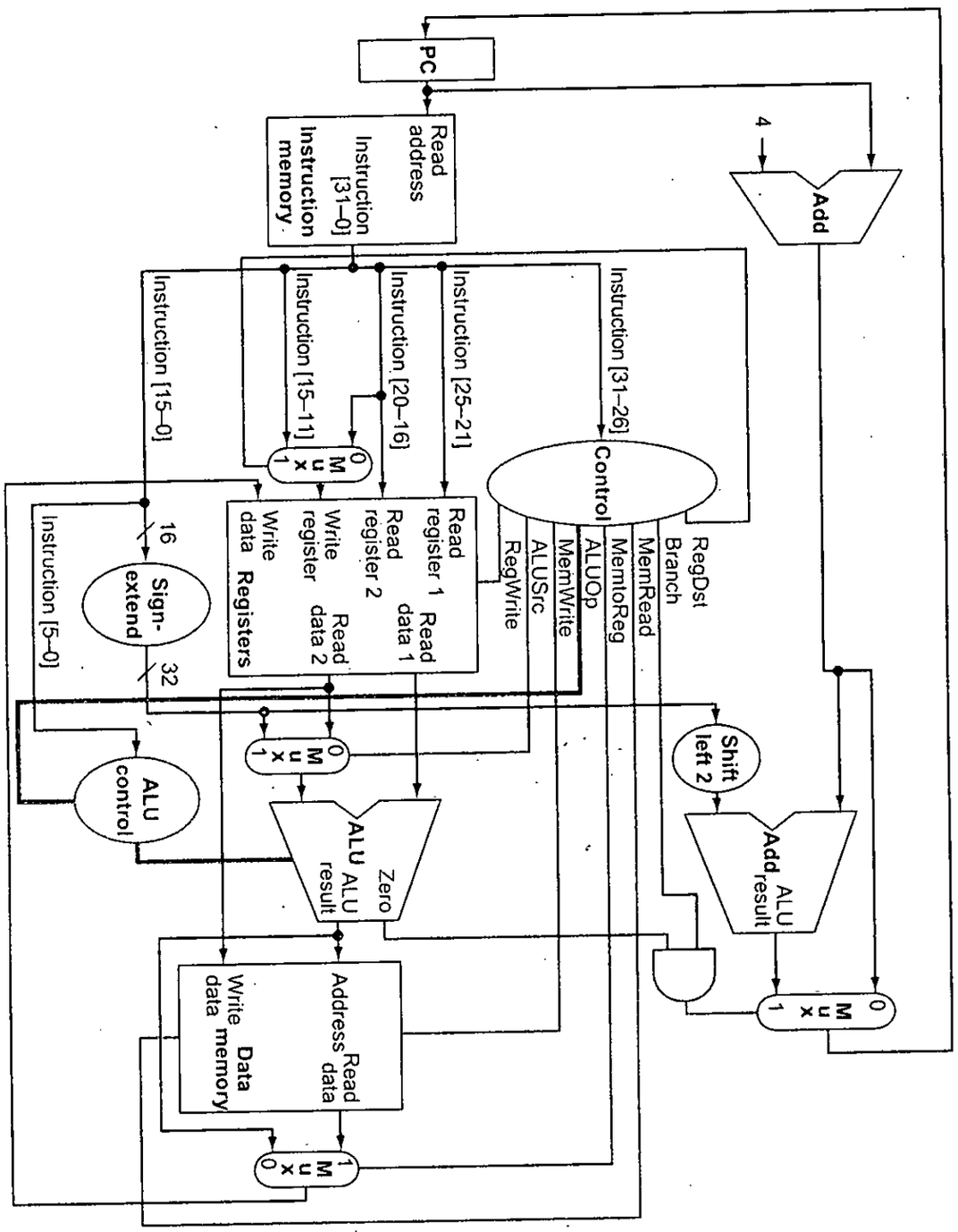

Figure 1: MIPS Datapath

This Figure can be detached from the question paper and attached to the answer script of Section-A

L-3/T-1/CSE **Date: 19/10/2022**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2020-2021

Sub: **CSE 307** (Soft Engineering)

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks

The structure of design patterns are supplied in the attached sheet

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE** questions.

1. (a) Consider a burger shop selling burger, appetizer and drinks. The following points describe the services provided to the customer. **(28)**

   (1) Three different types of pizza are being sold: Veggi, Beef and Chicken.

   (2) There are provisions to add extra cheese on those pizza.

   (3) There are provisions of different types of drinks: Coffee, Water and Coke. The prices of these different types of drinks are different. The customer can select one or more drinks in an order.

   (4) Onion Rings and French Fries are two different types of appetizers available.

   (5) A customer can order a meal which consists of an appetizer, a pizza with necessary cheese and drinks.

   Construct a class indicating the following using three different patterns:

   (1) Beef pizza with French fry and cheese

   (2) Chicken Pizza with onion rings and Bottle of Water

   (3) A combo meal with Veggi pizza, French Fry and two bottles of Coke

   (4) A combo meal with Veggi pizza, Onion Rings, Coffee and Water

   In each of the cases determine the price of the options shown above as a method of the class to be created.

   (b) Discuss the relative advantages and disadvantages of using different patterns in constructing the class in the problem 1(a). **(7)**

2. (a) Consider a web-based system where users will select a mobile phone talk time scheme and the cost associated with the scheme will be displayed to the users. New schemes are added frequently. Demonstrate how you can decouple the programmers of the user interface from the classes implementing the schemes. **(10)**

   (b) There are three sorting routines implementing selection, insertion and quicksort algorithm. Demonstrate the use of strategy pattern for using these routines for sorting. **(10)**

   (c) There is a list of student IDs with their obtained marks. You are to find the corresponding grades of the students. You must prepare a merit list for the students who get the highest grade. Provide a suitable solution using a design pattern. Write necessary code to demonstrate the solution. You can assume any grading scheme in this problem. **(15)**

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3. (a) You are to implement the hierarchy of the employees of the company. An employee may be under a boss and he or she might have one or more subordinates. The level of hierarchy is not fixed, and it varies any time. You can add a subordinate employee under an employee or you can remove an already included subordinate employee in the hierarchy. The employees listed in the subordinate list is considered as direct subordinate. The subordinate of subordinates is called indirect subordinate. The list of all subordinates (direct or indirect up to leaf) with detailed information will be available through a method of the class representing an employee. Show necessary implementation of the classes using appropriate design patterns. **(15)**

(b) Consider a dashboard that shows the maximum temperature and average temperature of the last one year. The temperature of the day is entered at the end of day. This triggers updating the temperature in the dashboard. You have to demonstrate the solution using appropriate software design pattern. **(10)**

(c) Describe COCOMO II model for estimation with necessary examples. **(10)**

4. (a) Consider a project for result processing system which is scheduled to prepare the results of SSC 2022. The software is being developed for education boards of the country. The project manager has to consider issues related to natural calamities like flood. Identify five risks while planning this software development project. Discuss the impact and exposure of the risks with proper justification. Briefly describe the risk mitigation plans for the identified risks. **(10)**

(b) What are the factors in selecting the team members for developing a Bangla Spell Checker? Explain in details. **(15)**

(c) Titas Gas Transmission and Distribution Company is trying to have a new billing software. There are several alternatives to implement that. The first one is to acquire a ready made billing software from a software development company with the cost of Tk. 1 crore. It might require 20 additional changes/reports to customize the software for the use of the company. The cost of each easy, moderately difficult or extremely difficult change/report is Tk. 50K, Tk. 70K or Tk. 100K. The probability of the changes/reports are easy and moderately difficult are 0.30 or 0.25 respectively. The other option is to reuse an open source billing software by an in house team of 10 members. The average salary of the in house team members are Tk. 75K. It will take 12 months to develop the system if the development is straight forward with the probability of 0.60. Otherwise it will take 18 months to develop the system if the development is complex. Which one would be best strategy for developing the billing software? **(10)**

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SECTION – B

There are **FOUR** questions in this section. Answer any **THREE** questions.

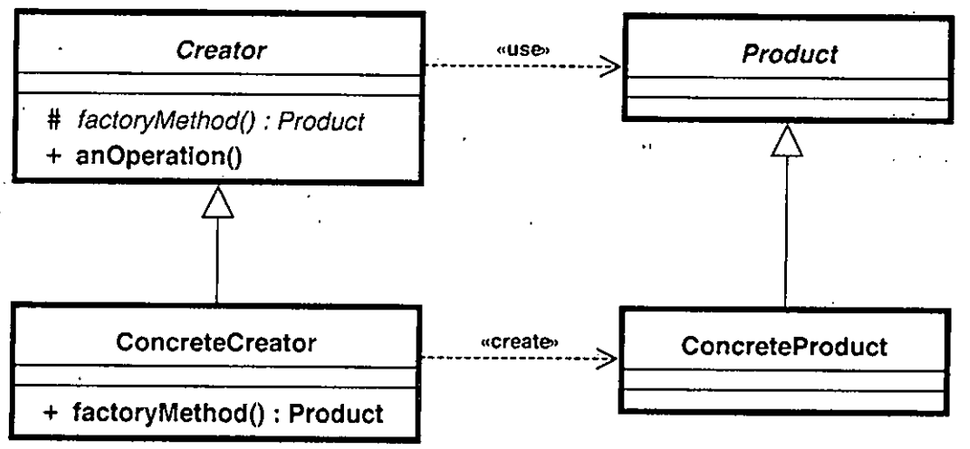
5. (a) A media agency is responsible to order advertisements at different newspapers. Each newspaper has a standard rate for unit size (1 column-inch) for each page which may change over time. Different newspaper gives different discounts over this rate to the agency. The agency has a database of expected readership for each page of each newspaper. An employee of the agency prepares a media plan for a product by selecting different positions for the ad (page, size, date and newspaper) to achieve maximum readership for a given budget. This plan is approved by client and then another employee generates Release Order from this plan. The Release Order mentions a number of ads to display with their positions, date to publish and cost. **(16)**
Design a Class diagram to implement the scenario described above.
(b) What do you understand by Equivalence Partitioning in the context of test data generation? Create test input set to test if the cost of Release Order is computed properly considering the scenario of Q 5(a). **(12)**
(c) What do you understand by Non-repudiation? Given an example considering the scenario of Q 5(a). **(7)**

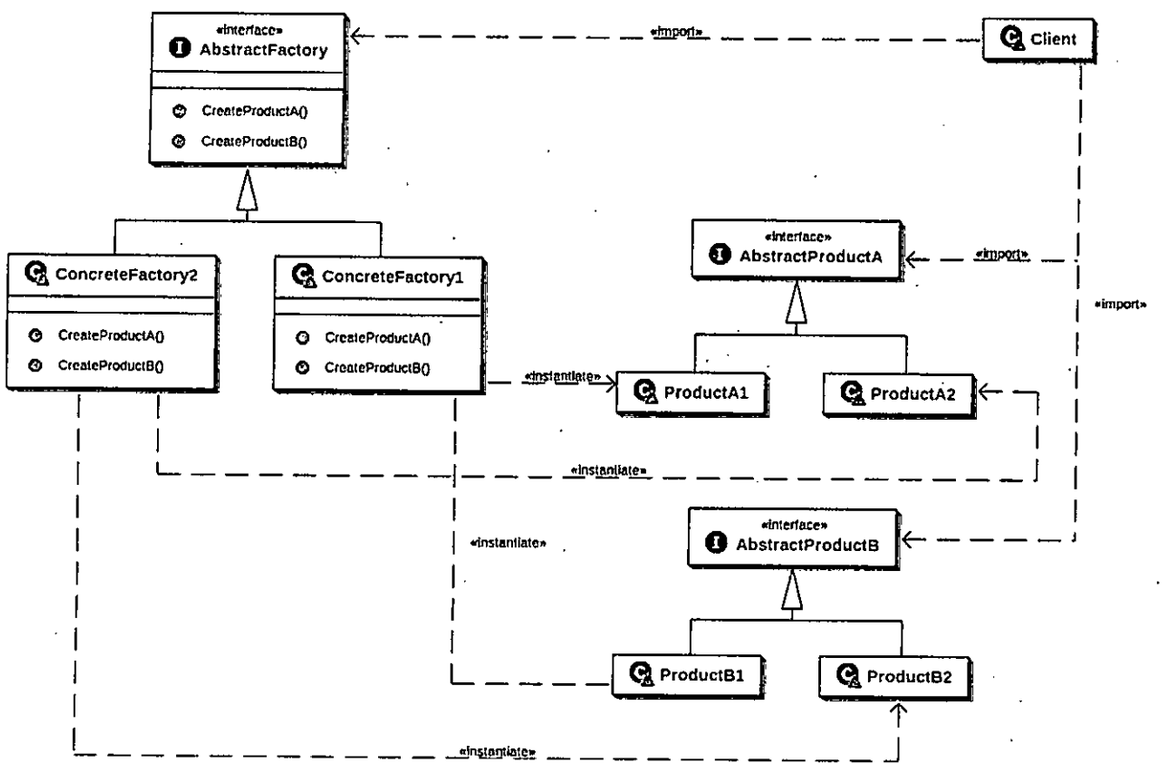
6. (a) To purchase books, the sites like Amazon.com or Rokomari.com are widely used. Draw an architecture to design such a system following Microservice architecture. **(12)**
(b) Give an example test execution ensuring method, branch and condition coverage. What are the characteristics of good unit testing? **(15)**
(c) What are the issues commonly identified during Code review? **(8)**

7. (a) A general manager of an office is entitled to have a laptop and two mobile phones per year. The laptop requisition process is implemented in a software application. Give examples of positive and negative testing in the context of testing the software process. **(10)**
(b) You have chosen write-through/read-through when you actually should be using write-around/read-through to implement cache in your system. Discuss an example scenario where such mistake may happen. What will be the consequence? **(16)**
(c) Give three example scenarios where Data-Centered software architecture is appropriate. **(9)**

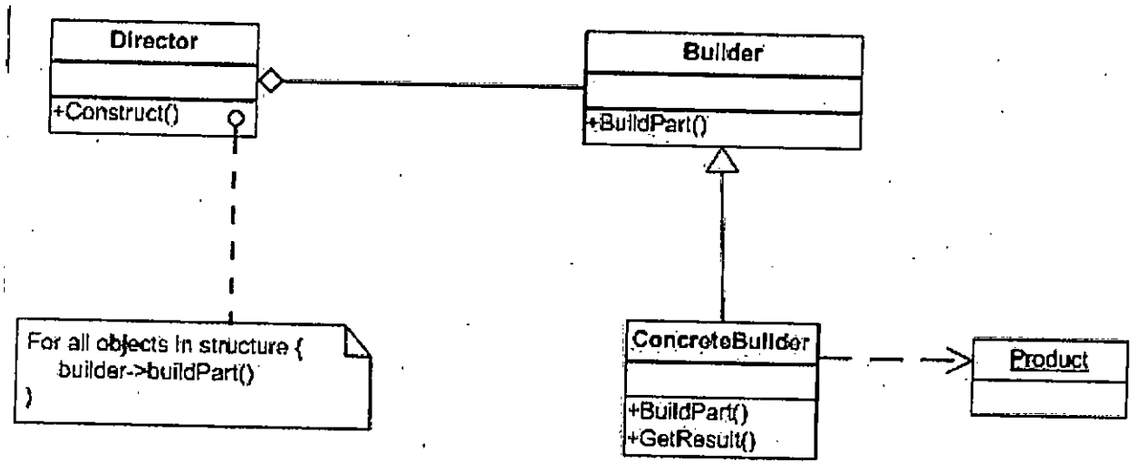
8. (a) What are the benefits of using Message Queue? What are the good practices recommended to ensure Confidentiality in software application? **(15)**
(b) Discuss Continuous Integration and Containerization in brief in the context of DevOps engineering. **(12)**
(c) What is the difference between Smoke and Regression testing? Discuss with an example. **(8)**

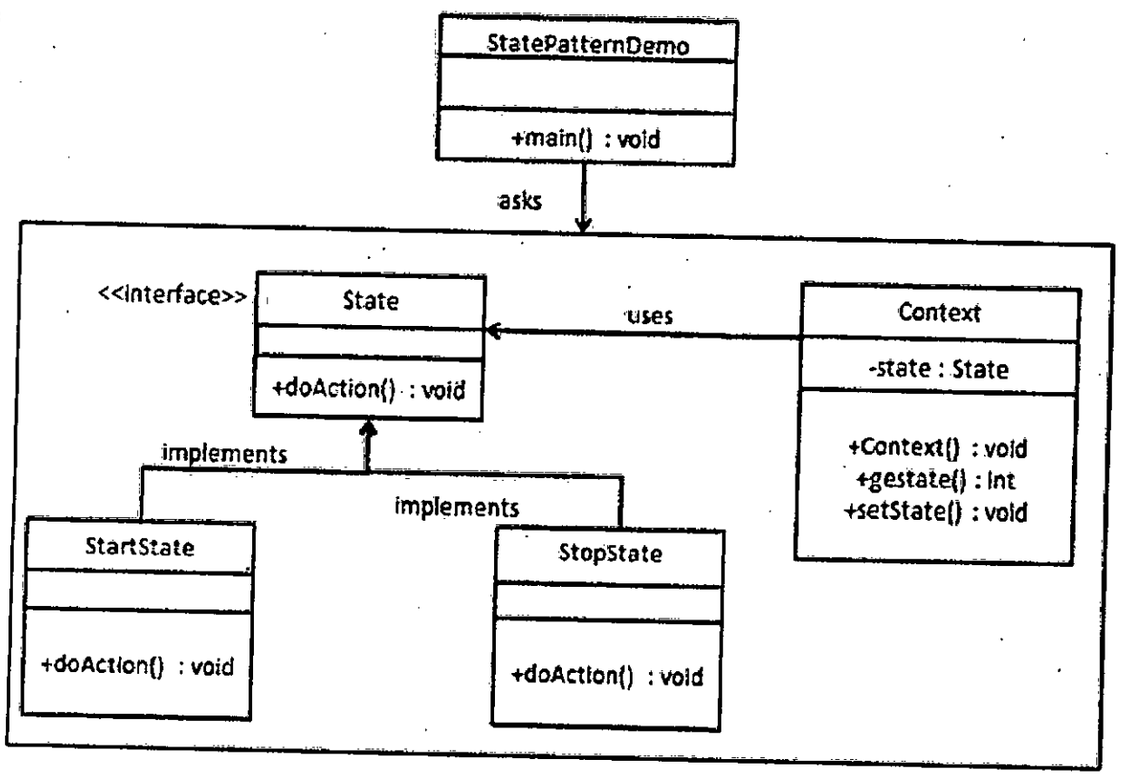
Annex : 1


Creator
factoryMethod() : Product
+ anOperation()
«use»
Product
ConcreteCreator
+ factoryMethod() : Product
«create»
ConcreteProduct

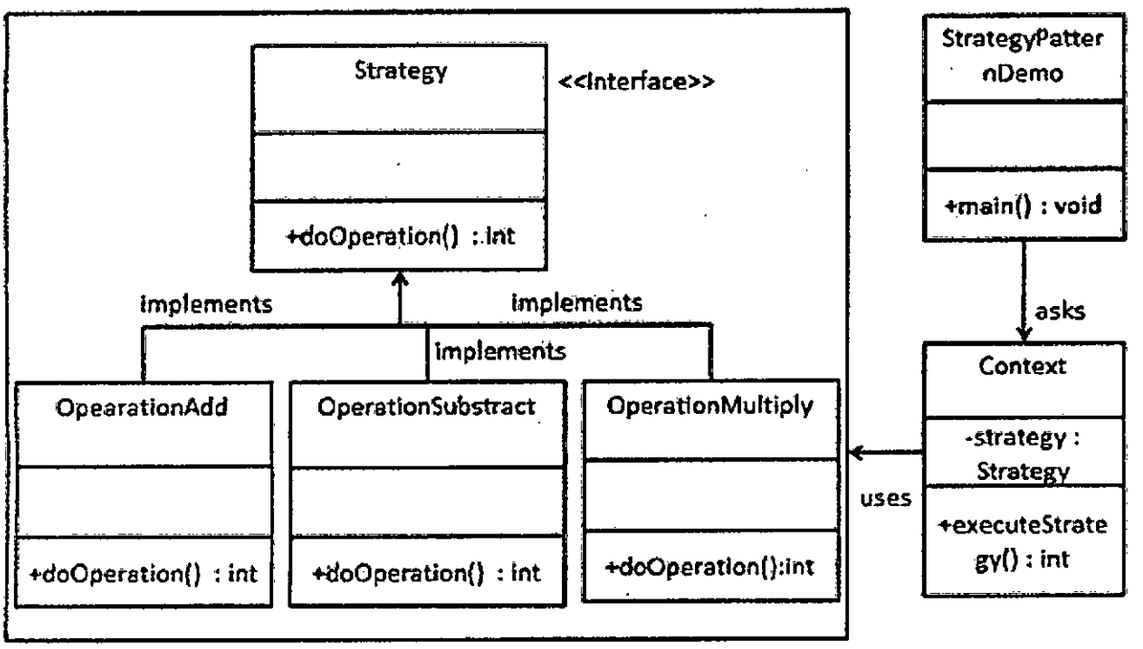

«interface»
AbstractFactory
CreateProductA()
CreateProductB()
«import»
Client
ConcreteFactory2
CreateProductA()
CreateProductB()
ConcreteFactory1
CreateProductA()
CreateProductB()
«instantiate»
«interface»
AbstractProductA
«import»
«import»
ProductA1
ProductA2
«instantiate»
«instantiate»
«interface»
AbstractProductB
ProductB1
ProductB2
«instantiate»

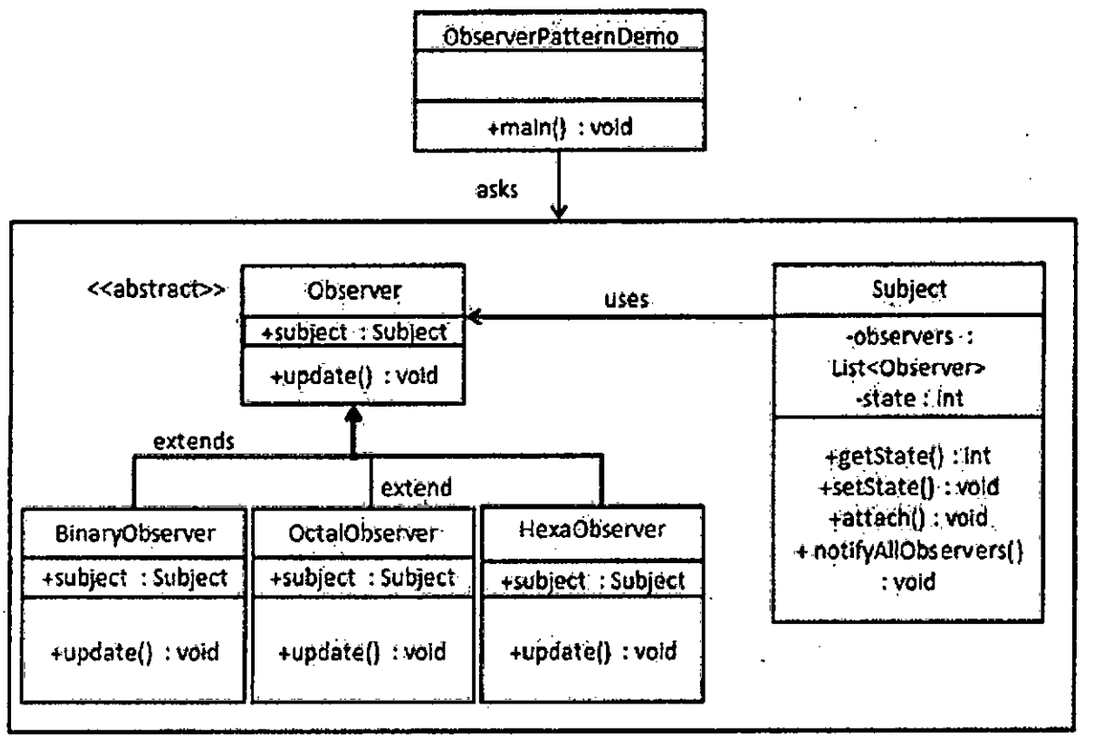
Anexa : 2


Director
+Construct()
Builder
+BuildPart()
For all objects in structure {
builder->buildPart()
}
ConcreteBuilder
+BuildPart()
+GetResult()
Product


StatePatternDemo
+main() : void
asks
<<Interface>>
State
+doAction() : void
uses
Context
-state : State
+Context() : void
+gestate() : int
+setState() : void
implements
implements
StartState
+doAction() : void
StopState
+doAction() : void

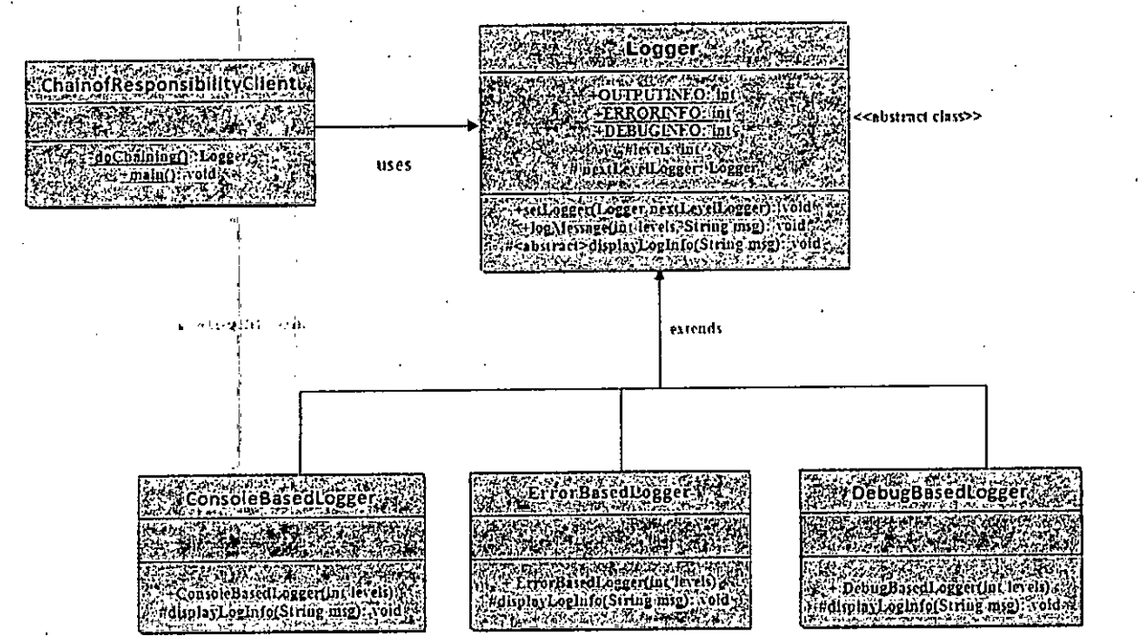
Ans : 3

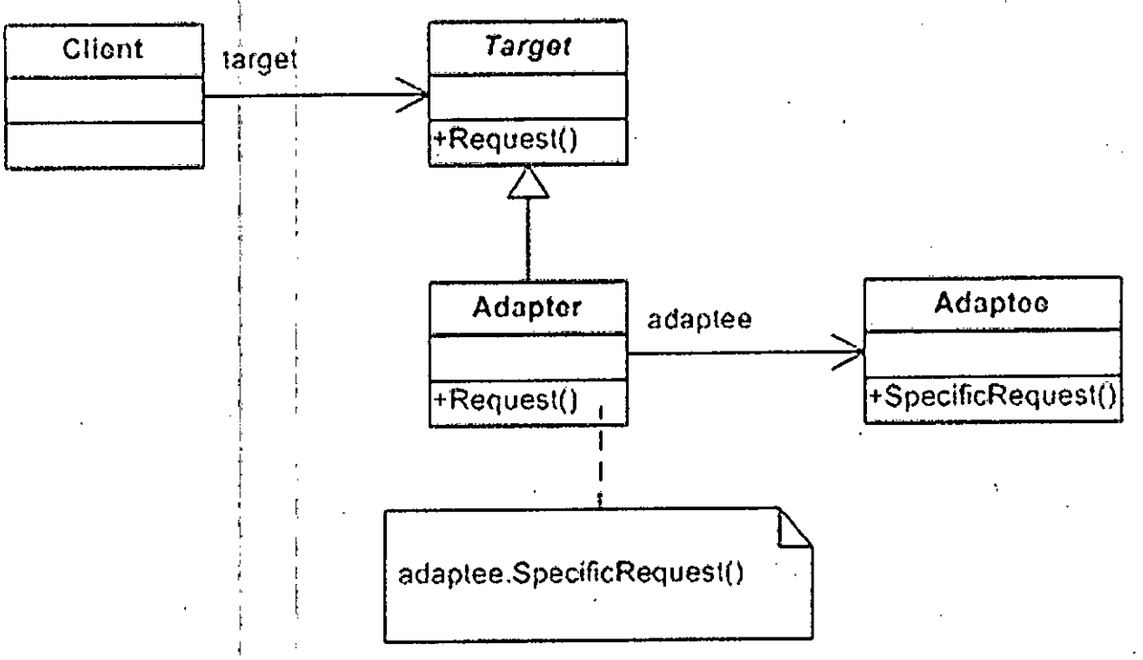

Strategy
<<Interface>>
+doOperation() : int
StrategyPatternDemo
+main() : void
asks
implements
implements
implements
OpearationAdd
+doOperation() : int
OperationSubstract
+doOperation() : int
OperationMultiply
+doOperation():int
uses
Context
-strategy : Strategy
+executeStrategy() : int


ObserverPatternDemo
+main() : void
asks
<<abstract>>
Observer
+subject : Subject
+update() : void
uses
Subject
-observers : List<Observer>
-state : int
+getState() : int
+setState() : void
+attach() : void
+notifyAllObservers() : void
extends
extend
BinaryObserver
+subject : Subject
+update() : void
OctalObserver
+subject : Subject
+update() : void
HexaObserver
+subject : Subject
+update() : void

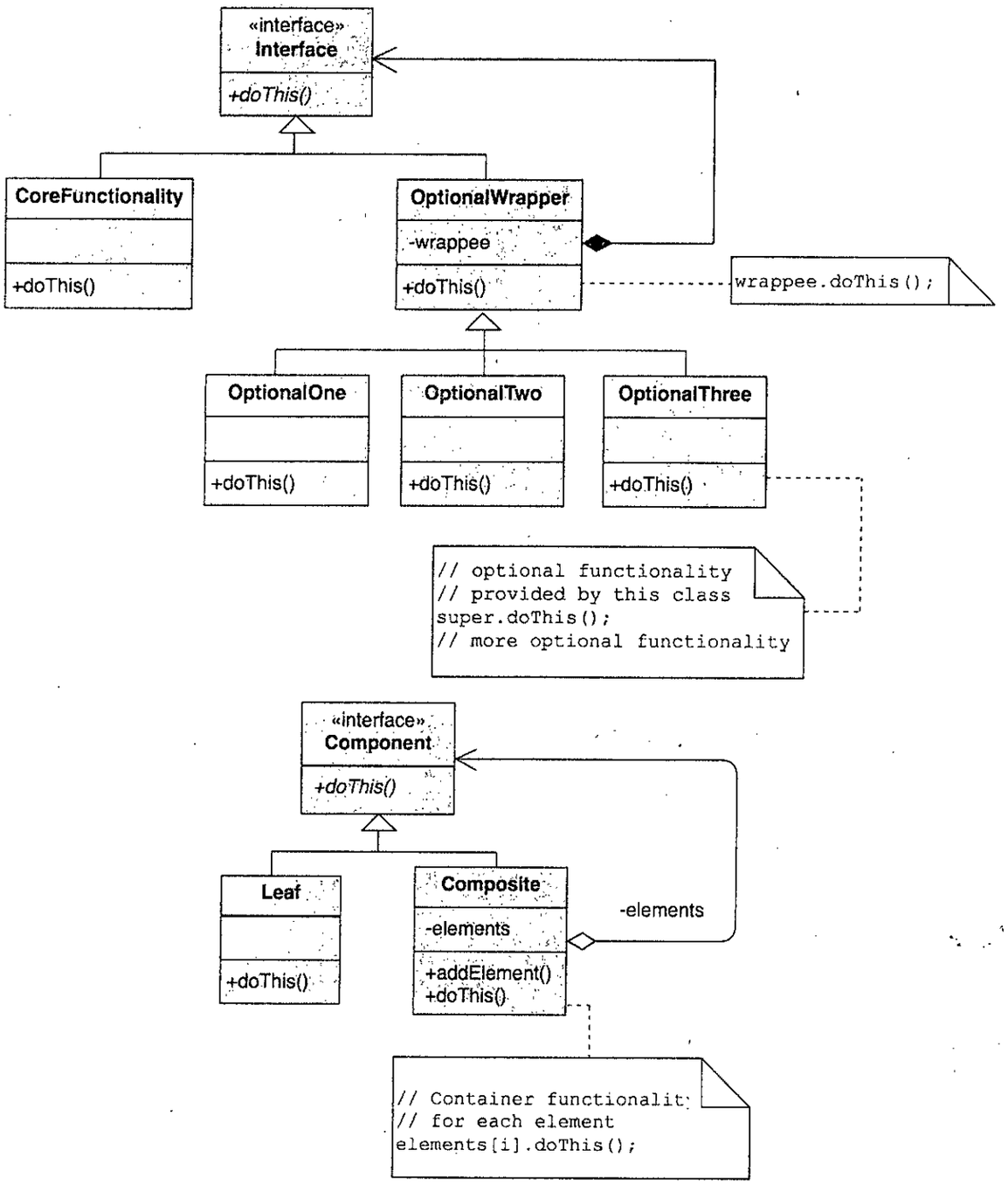
Ans - 4

UML for Chain of Responsibility Pattern:





Annex - 5


«interface»
Interface
+doThis()
CoreFunctionality
+doThis()
OptionalWrapper
-wrappee
+doThis()
wrappee.doThis();
OptionalOne
+doThis()
OptionalTwo
+doThis()
OptionalThree
+doThis()
// optional functionality
// provided by this class
super.doThis();
// more optional functionality
«interface»
Component
+doThis()
Leaf
+doThis()
Composite
-elements
+addElement()
+doThis()
-elements
// Container functionalit
// for each element
elements[i].doThis();

L-3/T-1/CSE **Date: 25/10/2022**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2020-2021

Sub: **CSE 309** (Compiler)

Full Marks: 210 Time: 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

All the symbols have their usual meanings in the context of compilers unless explicitly mentioned.

1. The following grammar generates a list numbers of the form- **(12)**

$\{num_1, num_2, num_3, \ldots, num_n\}$

where the terminal **num** represents any constant integer number.

$L \rightarrow$ '{' N '}'

$N \rightarrow$ N ',' **num|num**

(a) Design a syntax-directed definition (SDD) based on this grammar, which will compute and print for a given list of numbers –

(i) the index of the maximum number and

(ii) the count of numbers whose values are greater than their indices.

Assume the leftmost number has the index **0**.

For examples, for the input {3, 6, 1, 2, 5}, (i) the index of the maximum number is **1**, and (ii) the count of numbers whose values are greater than their indices is **3**.

(b) For the SDD you have designed in the answer to Question 1(a), draw the annotated parse tree for the list- {3, 6, 1, 2, 5} **(6)**

(c) Convert the SDD you have designed in the answer to Question 1(a) to an SDT. Can the SDT be implemented during top-down parsing? If not, transform the SDT such that it is implementable during top-down parsing. **(8)**

(d) Define Postfix SDT. Briefly des how Postfix SDT's can be implemented during LR parsing. **(9)**

2. (a) What is an Intermediate Representation (IR)? What are the advantages of using an IR? Give two examples of IR. **(8)**

(b) Write syntax-directed definition (SDD) for the following flow-of-control statement corresponding to a **for** loop in 'C'. **(9)**

$S \rightarrow$ **for** $(S_1; B; S_2)\ S_3$

Assume S has an inherited attribute *next* that represents a label assigned to the next statement following S. The non-terminal B represents a Boolean expression.

Contd P/2

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Contd... Q. No. 2

(c) Write down a translation scheme for generating code using *backpatching* for the flow-of-control statements yielded by the following productions. You may add market symbols in the productions as required. Make other justified assumptions as required. **(12)**

(i) $S \rightarrow$ **if** (B) S_1 **else** S_2

(ii) $\rightarrow$ **while** (B) S_1

(d) translate the following if-else statement to three-address code avoiding redundant gotos. Assume &&, || are left associative and && has higher precedence than ||. **(6)**

if ((x! = y || x > 20) && x < 10) flag = 0; else flag = 1;

3. (a) The baker's mark-and-sweep algorithm for garbage collection moves objects among four lists: *Free*, *Unreached*, *Unscanned*, and *Scanned*. Illustrate how Baker's mark-and-sweep algorithm garbage collector works using the example network below when the pointer A $\rightarrow$ D is deleted. Assume X and Y are members of the root set. What is the time and space complexity of the algorithm? **(15)**

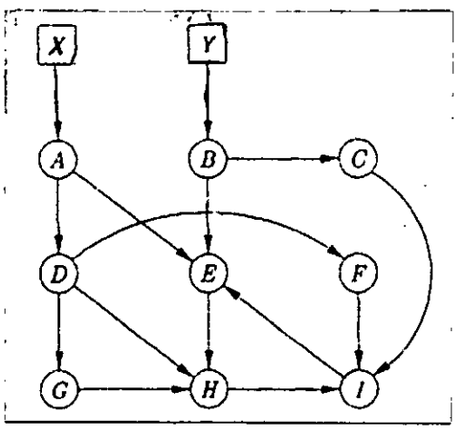

Figure for Question 3(a)

(b) Explain why register allocation and assignment is a critical issue during code generation? While generating code for a basic block, a function is used to select registers for each memory location associated with a three-address instruction *I*. Assume the function is called *getReg(I)*. For an instruction of the form, *I*: $x = y + z$, what rules are used by the function *getReg(I)* while selecting registers for each of the variables, x, y, and z. **(5+15=20)**

4. (a) Consider the three-address code below and answer the following questions.

(i) Identify the basic blocks and construct the flow graph for the given code. Give each block an identifier and replace the label references in the statements with the corresponding identifiers. Also, find and list the loops in the flow graph. **(14)**

Contd P/3

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Contd... Q. No. 4(a)

(ii) Optimize the code by using all possible semantic preserving transformations. For each of the transformations used, specify the name of the transformation. **(14)**

```
1     L1: i = 0
2     L3: t1 = n - 1
3         iffalse i < t1 goto L2
4     L4: j = i + 1
5     L5: iffalse j < n goto L6
6     L7: t2 = i * 8
7         t3 = a [ t2 ]
8         t4 = j * 8
9         t5 = a [ t4 ]
10        iffalse t3 > t5 goto L8
11    L9: t6 = i * 8
12        p = a [ t6 ]
13    L10:    t7 = i * 8
14        t8 = j * 8
15        t9 = a [ t8 ]
16        a [ t7 ] = t9
17    L11:    t10 = j * 8
18        a [ t10 ] = p
19    L8: j = j + 1
20        goto L5
21    L6: i = i + 1
22        goto L3
23    L2:
```

(b) Consider a 'C' code fragment and the corresponding assembly code generated by some 'gcc' compiler using -O2 optimization switch. Now, identify the optimizations that have been performed by the compiler for the given 'C' code. Write an equivalent 'C' program for the optimized code. **(7)**

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Contd... Q. No. 4(b)

Program written in C	Assembly code generated by gcc

`#include<stdio.h>`
`int fact(int n)`
`{`
`  if (n == 0)  return 1;`
`  return n*fact(n-1);`
`}`
`int main(){`
`  int i=fact(5);`
`  printf("%d",i);`
`}`
	`fact(int):`
	`  mov eax, 1`
	`  test edi, edi`
	`  je .L1`
	`.L2:`
	`  imul eax, edi`
	`  sub edi, 1`
	`  jne .L2`
	`.L1:`
	`  ret`
	`.LC0:`
	`  .string "%d"`
	`main:`
	`  sub rsp, 8`
	`  mov esi, 120`
	`  mov edi, OFFSET FLAT:.LC0`
	`  xor eax, eax`
	`  call printf`
	`  xor eax, eax`
	`  add rsp, 8`
	`  ret`

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Describe the working principal of the language processor used by Java Programming Language? **(10)**

(b) Suppose you want to run a company that will produce compilers for different programming languages. If you need to build compilers for 10 programming languages, then which approach you will follow to build the front-end and back-end? Give a high-level overview of your design. **(15)**

[Your design must be efficient]

(c) In C programming language special keywords fall under the category of identifiers. Explain how lexical analyzer differentiates special keywords from identifiers. **(10)**

6. (a) Perform left factoring for the following grammar. **(5)**

$S \rightarrow abA \mid abcS$

$A \rightarrow aA \mid \in$

Contd P/5

CSE 309
Contd... Q. No. 6

(b) Briefly describe the following questions. **(5+8+7=20)**

i. Is it possible to eliminate lexical analyzer step from compilation?
(just write Yes or No)

ii. Why lexical analyzer uses buffer pair instead of single buffer?

iii. What does it mean by 'Panic Mode' in the context of lexical analyzer?

(c) Does lexical analyzer will find errors from the following code snippet? If you think lexical analyzer will find some errors then explain them properly. **(10)**

```
int arr[] = {1, 2, 3, 5};
int i = 0;
do {
    if (arr[i] %2 == 0)
        print("EVEN\n");
    else
        print("ODD\n");
    i++;
 } while (index < 4);
```

7. (a) Explain the difference among the following regular expressions in the context of Lex lexical analyzer generator. **(14)**

i. {mytoken}

ii. [mytoken]

iii. mytoken

iv. (mytoken)+

v. mytoken +

vi. (mytoken)*

vii. mytoken*

(b) Perform left recursion elimination from the following grammar. **(21)**

$S \rightarrow Sa \mid Tb \mid Uc \mid a$

$T \rightarrow Sc \mid Ta \mid Ub \mid b$

$U \rightarrow Sb \mid Tc \mid Ua \mid c$

8. (a) Compute FIRST and FOLLOW for the following grammar. **(5+10=15)**

$T \rightarrow S\$$

$S \rightarrow DbE$

$D \rightarrow VD \mid \epsilon$

$V \rightarrow cdE \mid acdE$

$E \rightarrow c \mid \epsilon$

Contd P/6

CSE 309

Contd... Q. No. 8

(b) Consider the following grammar. **(20)**

$E \rightarrow TE'$

$E' \rightarrow +TE' \mid \in$

$T \rightarrow FT'$

$T' \rightarrow *FT' \mid \in$

$F \rightarrow (E) \mid id$

On input id + id * id, construct a table by showing the moves that will be made by the non-recursive predictive parser algorithm.

L-3/T-1/CSE **Date : 15/10/2022**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2020-2021

Sub : **CSE 311** (Data Communication)

Full Marks : 210 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) Define DC component problem in a line coding scheme. How does it cause problem while transmitting a signal through a communication channel? With appropriate examples show that both NRZ-L and NRZ-I exhibit the DC component problem. Why don't AMI and pseudo-ternary line coding schemes have this problem despite the existence of long sequence of 1'0 or 0's in a data stream? **(25)**

   (b) Can we foretell the future events of a signal from its past samples? Justify. **(10)**

2. (a) With necessary mathematical analysis, show that the receiver in differential pulse code modulation (DPCM) is able to produce the original message signal pulse the quantization noise. How does the signal-to-noise ratio (SNR) improve here though there is quantization noise? **(18)**

   (b) Calculate the coefficients of the exponential Fourier Series (FS) expansion of the signals $\sin 2\pi t$ and $\cos 2\pi t$. Comment on the characteristics of these signals and their corresponding coefficients in FS expansion. Do we need to integrate the signals over their complete cycles while calculating their coefficients in FS expansion? Justify. **(17)**

3. (a) A practical signal cannot be fully recovered from its sampled values no matter how much we increase the sampling frequency. Justify the statement. Which phenomenon causes this problem and how does it distort the signal? What do we do to minimize this distortion? **(24)**

   (b) State the Dirichlet condition for the existence of Fourier Transform (FT) of a signal. Is it a necessary condition of the existence of the FT of a signal? Justify with an appropriate example. **(11)**

4. (a) State the characteristics of distortionless transmission. With appropriate examples give physical interpretation of these characteristics. What happens if these characteristics are not satisfied? **(20)**

Contd P/2

CSE 311

Contd ... Q. No. 4

(b) In a hypothetical telemetry system, there are five analog signals. The bandwidth of the first one is 5.0 kHz, but for each of the remaining signals it is 2.5 kHz. These signals are to be sampled at rates no less than their respective Nyquist rates and no more than the Nyquist rate of the first one and are to be word-by-word multiplexed. This can be achieved by multiplexing the PAM samples of the five signals and then binary coding the multiplexed samples (as in the case of the PCM T1 carrier mentioned in your text book). **Suggest and draw** a suitable multiplexing scheme for this purpose. Note: In this case, you may have to sample some signal(s) at rates higher than their Nyquist rate(s). **What is the commutator frequency** (in rotations per second)? If the samples are quantized into 1024 levels, **determine the binary pulse rate** (bits per second) of the composite binary-coded signal, and **the minimum bandwidth** (in kHz) required to transmit this signal. **(15)**

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Max wants to design a 4-ary FSK scheme. He wants B/W consumption to be as small as possible while keeping the FSK signals orthogonal to each other in T_b. Derive the most appropriate frequency increment, δf, among signals which would fulfill Max's requirements. Finally, specify a set of FSK signals suited to the task when T_b = 10 ms. **(11+4=15)**

(b) Consider the scheme designed in 5(a). Explain with necessary block diagram how the transmitted FSK signals can be detected at the receiver's end using Noncoherent and Coherent techniques. **(5+5=10)**

(c) Sketch the PM wave corresponding to the modulating signal shown in Figure 5.1, given f_c = 10 MHz and $k_p = 5\pi$. **(10)**

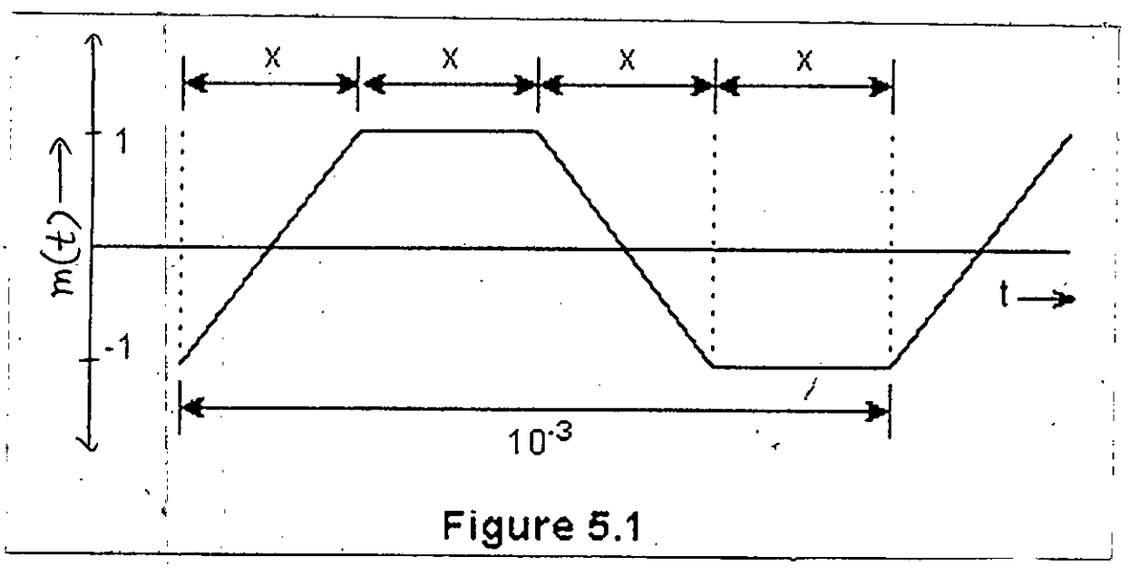

Figure 5.1

CSE 311

6. (a) Rank the following digital modulation schemes in terms of probability of error. Provide necessary figures/diagrams, and explanations to support your claim. **(3×6=18)**

   (i) Binary ASK

   (ii) Binary PSK

   (iii) Binary FSK

   (b) Briefly explain when and why the value of $k_p m(t)$ has to be restricted within $(-\pi, \pi)$ during Phase Modulation. **(5)**

   (c) Suppose you want to design a DSB-SC modulator, where you simply multiply the modulating signal $m(t)$ with a carrier. But unfortunately, you do not have any multiplier at your disposal. Propose an alternate solution to achieve modulation. Show necessary diagrams. **(12)**

7. (a) Compute the estimated bandwidth of Wide Band FM signal using staircase approximation. Provide necessary figures. **(15)**

   (b) Explain why envelope detection does not work for PSK. Propose an alternate approach/modification to PSK so that envelope detection can be used during demodulation. **(4+8=12)**

   (c) Draw a block diagram for SSB modulation (Lower sideband only). **(8)**

8. (a) Suppose you want to transmit 4 bits of data at a time using M-ary PSK. Specify a set of PSK signals suited to the task. **(4+8=12)**

   Also compute the distance between two consecutive points in the signal space diagram, showing detailed steps.

   (b) Draw the block diagram for an NBFM modulator using a DSB-SC modulator. **(10)**

   (c) Explain how Offset-QPSK deals with the high phase shift problem of QPSK. **(7)**

   (d) Describe how a Frequency Modulated signal can be demodulated using Envelope Detection. **(6)**

L-3/T-1/CSE **Date: 29/09/2022**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2020-2021

Sub: **CSE 315** (Microprocessors, Microcontrollers, and Embedded System)

Full Marks: 210 Time: 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE** questions.

Assume system clock frequency 1MHz if not given.

List of registers and necessary diagrams are at the end of the question.

If configuration for any required register/control-word/bit is missing, just assume a configuration and clearly show the assumed configuration.

1. (a) Draw a timing diagram showing Serial Peripheral Interface (SPI) data transfer when leading (falling) edge is setup edge and trailing (rising) edge is sample edge. Clearly show with respect to clock pulse when the data is sampled and when relevant pins are changed. **(10)**

   (b) Suppose you are taking analog input using ATmega32. Here, ADMUX = 11010000, ADC0 is connected to 2V and ADC1 is connected to 1V. Determine the value of ADCL and ADCH after a conversion ends. **(10)**

   (c) Suppose you are to design a Fire Alarm System. There is a smoke sensor (S) and a temperature sensor (T) connected to ATmega32. The S sensor provides 0V if there is no smoke and jumps to 5V when it detects any smoke. The T sensor provides voltage in the range of 0V to 5V in proportional to the temperature between 0°C to 100°C. **(15)**

   If there is smoke and the temperature is above 70°C, you are to light up an LED connected to the ATmega32.

   i) Draw a circuit diagram showing the connection among S, T, LED and ATmega32

   ii) Write a C code for the system

   Your system should avoid unnecessary computation to be energy efficient.

2. (a) Write two advantages of using microcontroller compared to using a microprocessor. **(5)**

   (b) Analyze the pattern of analog reading if we always read ADCH before ADCL? **(5)**

   (c) Explain quantization error in terms of Analog-to Digital conversion? **(5)**

   (d) Three SPI Slave (S1, S2 and S3) is connected to a SPI Master (M) as shown in Figure 2(d). Initially, each device has eight bits of data in their shift registers as shown in corresponding dotted box. Each device is also configured to transmit the MSB first. **(10)**

Contd P/2

CSE 315

Contd... Q. No. 2

Determine the contents of the shift registers of four devices after

(i) 4 clock pulses

(ii) 16 clock pulses

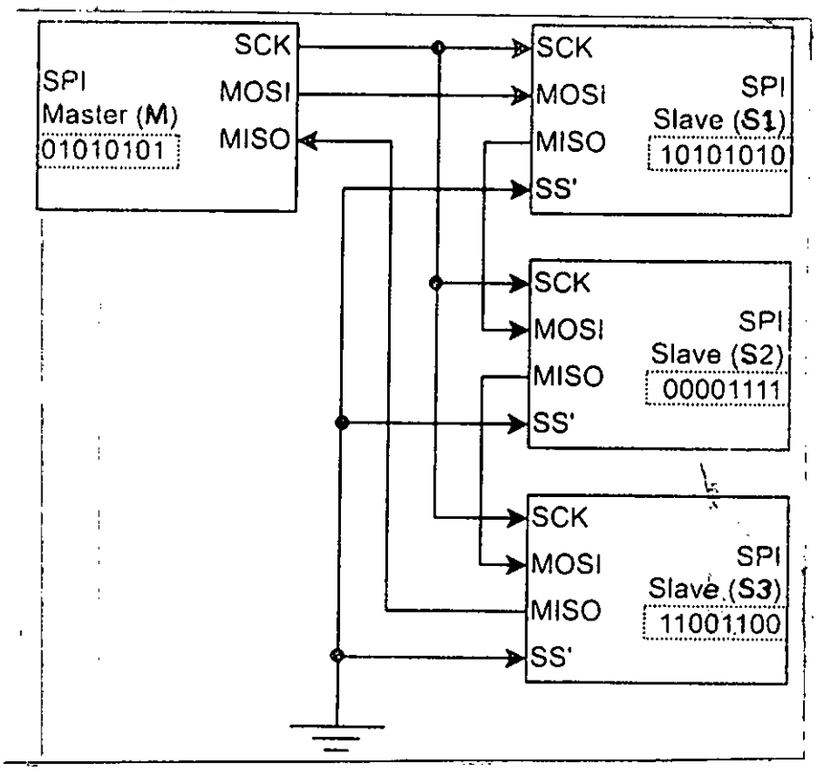

Figure 2(d)

(e) Write a C code to measure elapsed time of a code segment using TIMER1. TIMER1 must operate under normal model (0000), and counter must increment after every eight internal clock pulses. Measure the elapsed time in microseconds and store it in a variable named "elapsed_time". **(10)**

3. (a) Describe the procedure to enable nested interrupts in ATmega32. **(5)**

(b) Write a function named UART_init to initialize a USART communication configured for double speed, only transmission, asynchronous mode, even parity, 2 stop bits, 7 data bits and 3800 bps baud rate. **(10)**

(c) Suppose TIMER1 of ATmega32 is operating in mode WGM = 1010 (Table 2). Prescaler is 64. Values of ICR1 is 1000 and OCR1B is 200. OC1A is configured to be clear on compare match when up-counting and set on compare match when down-counting. Calculate the duty cycle and frequency of OC1A.

(d) Suppose TIMER1 of ATmega32 is operating in mode WGM = 1111 (Table 2). Prescaler is 8. Value of OCR1A is 1999 and OCR1B is 199. OC1B is configured to be set on compare match and clear at BOTTOM. Calculate the duty cycle and frequency of OC1B. **(10)**

Contd P/3

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4. (a) Explain the stop bit detection process in USART. **(5)**

(b) You are to design a Fibonacci counter using ATmega32. An active-low switch is connected to PD2. When the switch is pressed, the counter will increase. The counter is an 8-bit number. It starts from 0 and increases like the following sequence: 1, 1, 2, 3, 5, 8 ....When the counter overflows, it goes back to zero. The current value of the counter will be displayed in eight LEDs connected to PORTA. Write a C program to implement this counter using external interrupt. **(10)**

(c) Briefly describe three motivations for serial communication and 2 motivations for parallel communication. **(10)**

(d) A switch S is connected to ATmega32 as shown in Figure 4(d). To perform as expected, you need to choose the resistence of R carefully. Explain the issues if the resistence of R is chosen to be too high or too low. **(10)**

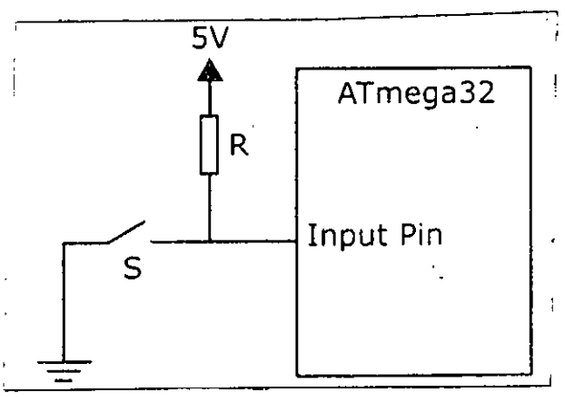

Figure 4(d)

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Determine the first five (5) and last five (5) of the logical addresses in segment:offset form for the physical address 2A3B4h. Write the address in HEXADECIMAL format i.e. AAAAh:BBBBh. **(10)**

(b) While studying memory organization of different intel microprocessors, Jake came to know about the following two methods of bank selection: **(5+10=15)**

i) separate write signal to select a write to each bank

ii) separate decoders are used for each bank

Explain the pros and cons of the above-mentioned two methods.

Now Jack is trying the first methods with an 80486 which has 32-bit address bus. Draw the logic circuit to generate the separate write signals $(\overline{WR0}, \overline{WR1}, ...)$ from the bank selection signals $\overline{BE3}$, $\overline{BE2}$, $\overline{BE1}$, $\overline{BE0}$, and write signal to 80486 $\overline{MWTC}$.

Contd P/4

CSE 315

Contd... Q. No. 5

(c) Explain the memory access mechanism of the DRAM architecture shown in figure 5(c). **(10)**

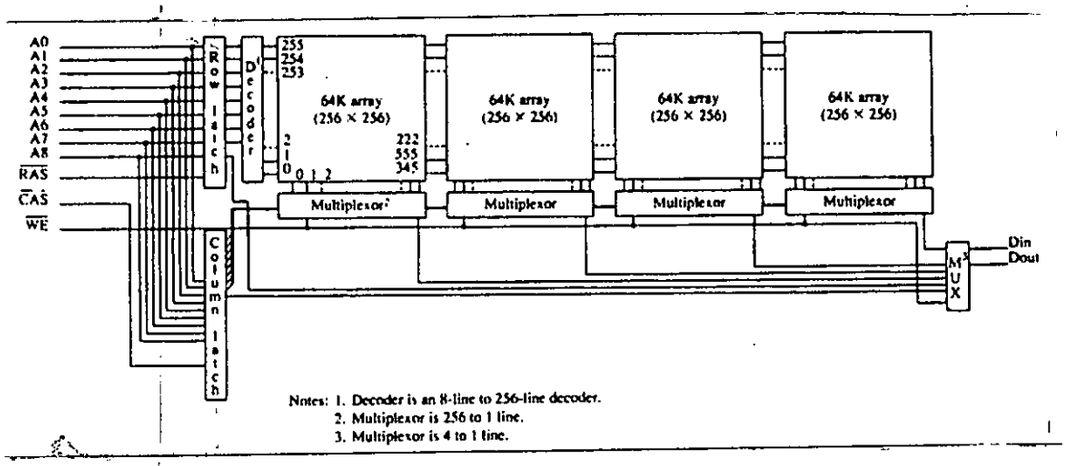

Figure for Question 5(c)

6. (a) John is designing a system with an 81212 microprocessor, a DAC, and a clock generator (8284A). For his system he needs to feed the microprocessor with 10 MHz clock signal and the DAC with 15 MHz clock signal. To ensure it, John applies 30 MHz crystal in between X1 and X2, and another 15 MHz signal to EFI of the 8284A. He feeds the microprocessor with CLK signal and the DAC with PCLK signal from the clock generator as shown in figure 6(a). **(20)**

Now, you need to answer the following (with other necessary diagrams)-

i. Does the microprocessor get the intended clock signal? If so, then you need to explain how it is getting the clock signal at the clock input of the microprocessor from corresponding input to the clock generator. If not, then you need to explain why the two clock inputs to the clock generator are not enough or appropriate in supplying the intended clock signal to the microprocessor.

ii. Does the DAC get the intended clock signal? If so, then you need to explain how it is getting the clock signal from corresponding input to the clock generator to the clock input of the DAC. If not, then you need to explain why the two clock inputs to the clock generator are not enough or appropriate in supplying the intended clock signal to the a DAC.

Contd P/5

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Contd... Q. No. 6(a)

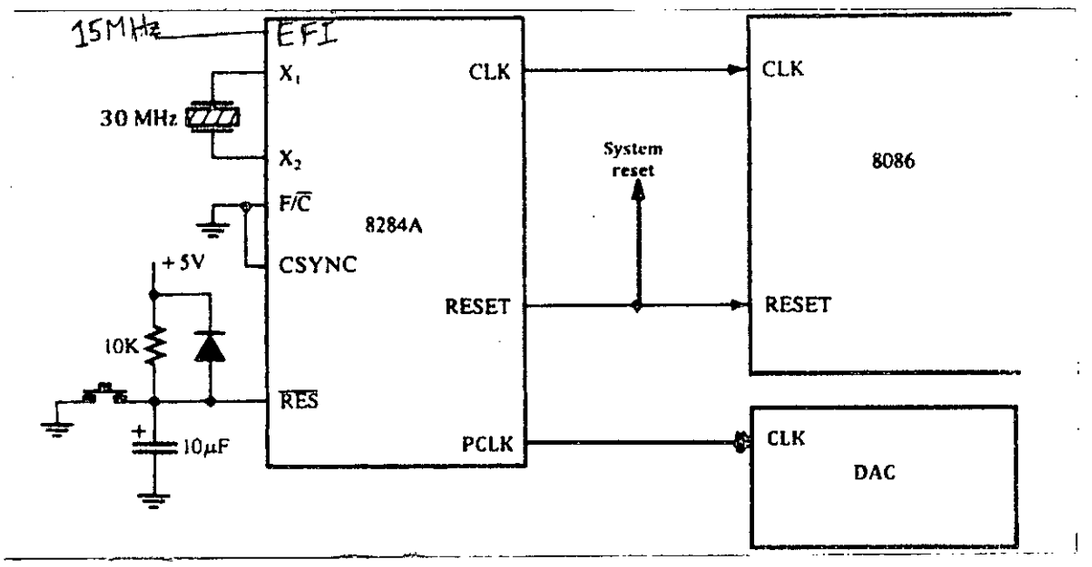


Figure for Question 6(a)

(b) The circuit in Figure 6(b) is intended for a buffered system of 8086, where all address, control, and data buses are fully buffered. Do you think that the circuit is enough or appropriate for the purpose of fully buffered system of 8086? If so, then explain how it serves the purpose. If not, then present necessary correction(s) or enhancement(s) needed to be made in the circuit. **(15)**

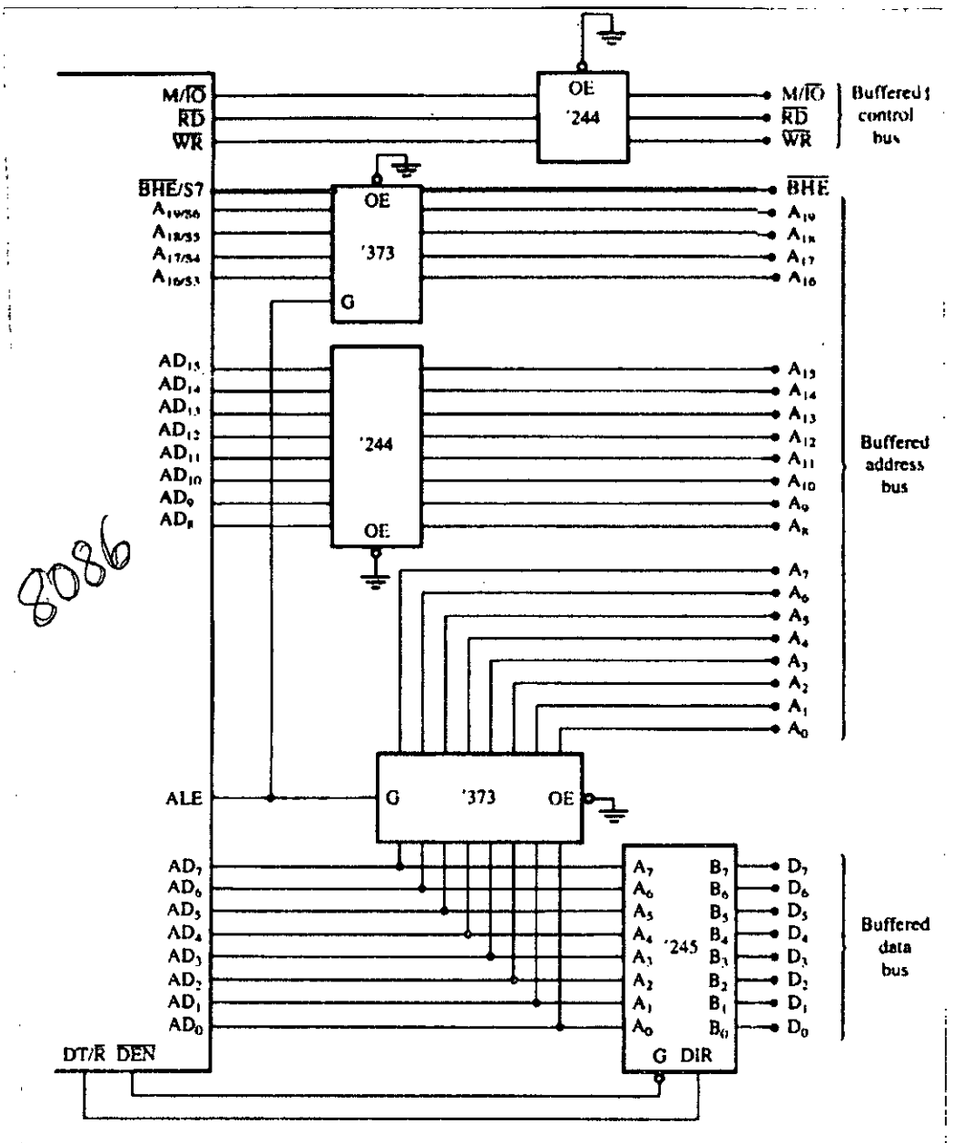


Figure for Question 6(b)

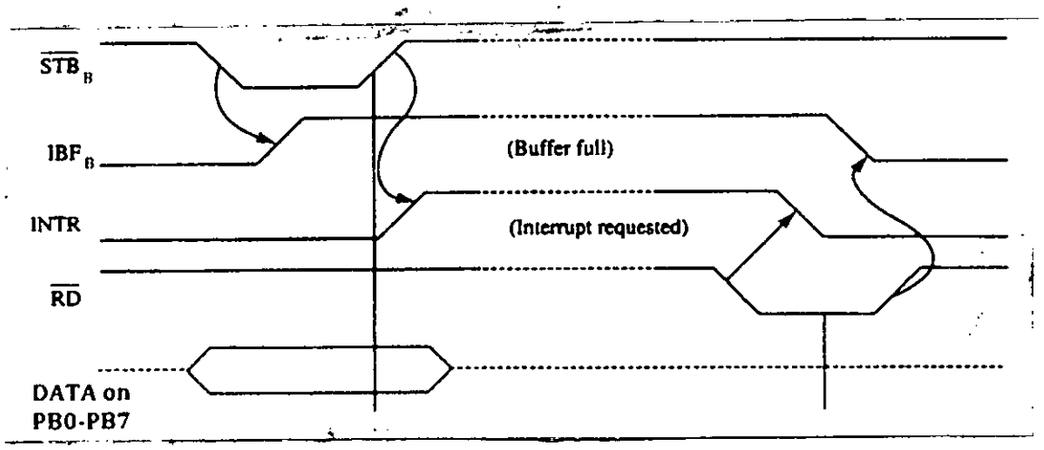
Contd P/6

CSE 315

7. (a) What are the differences between 8086 and 8088? **(7)**

(b) Suppose an 8086 system is connected to a printer and an array of switches via an 8255 PPI. The printer is connected to PORT A and operates in single handshake mode. The array is connected to PORT B and operates in simple I/O mode. Clearly specify the control word to support the above-mentioned configurations. **(10)**

(c) Suppose 8086 is reading data bytes from a typewriter through PORT B of the 8255 using strobed input mode (mode 1). The timing diagram for one byte of data transfer is given below: **(18)**



Now redraw the same timing diagram in your answer script and mark the first occurrence of each of the following events with the corresponding even ID surrounded by a circle on the timing diagram.

Event ID	Event Description
1	8255 loads Data into its input latch
2	The typewriter indicates that data is no more valid
3	The typewriter sends data to port's data line
4	8255 forbids the typewriter to send next data
5	8255 prevents a second interrupt for the same data
6	CPU starts reading the data
7	Data Transfer complete
8	8255 informs CPU about the data by generating interrupt signal
9	Read complete

Contd P/7

CSE 315

8. (a) Ralph is using the circuit in Figure 8(a) for interrupt expansion for his term project. **(15)**

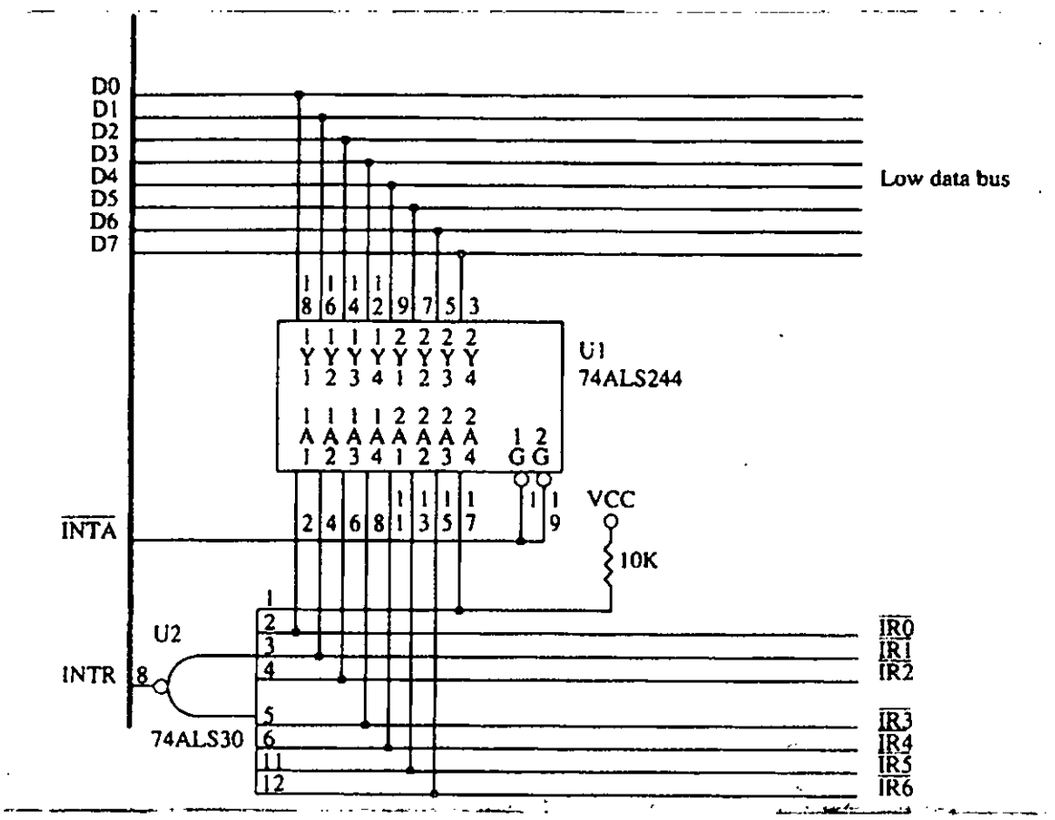


Figure for Question 8(a)

The interrupt vectors and their corresponding vector addresses for single trigger of any one interrupt are shown in the following table:

$\overline{IR6}$	$\overline{IR5}$	$\overline{IR4}$	$\overline{IR3}$	$\overline{IR2}$	$\overline{IR1}$	$\overline{IR0}$	Vector	Vector Address
1	1	1	1	1	1	0	FEH	1F342H
1	1	1	1	1	0	1	FDH	4C215H
1	1	1	1	0	1	1	FBH	32E54H
1	1	1	0	1	1	1	F7H	987B4H
1	1	0	1	1	1	1	EFH	C3E42H
1	0	1	1	1	1	1	DFH	13D2BH
0	1	1	1	1	1	1	BFH	F3E4AH

For simultaneous trigger of multiple interrupts, priority is resolved in following order:

$\overline{IR3}$, $\overline{IR5}$, $\overline{IR2}$, $\overline{IR6}$, $\overline{IR1}$, $\overline{IR4}$, $\overline{IR0}$.

Now determine the values for ***K, L, M, N, O, P, Q, R, S, T, U,*** and ***V*** from the following table. The first row is filled up for you.

Contd P/8

CSE 315

Contd... Q. No. 8(a)

$\overline{IR6}$	$\overline{IR5}$	$\overline{IR4}$	$\overline{IR3}$	$\overline{IR2}$	$\overline{IR1}$	$\overline{IR0}$	Vector	Vector Address
1	1	1	0	1	1	0	F6H	987B4H
1	0	1	1	0	0	1	***K***	***L***
M							AFH	***N***
0	1	1	1	0	1	1	***O***	***P***
Q							C5H	***R***
1	1	0	1	1	0	0	***S***	***T***
U							BBH	***V***

(b) Describe three (3) ways of interfacing DMA controller with microprocessor, I/O devices, and memory with diagrams. **(15)**

(c) Write a short note on membrane key switches. **(5)**

CSE 315

Figures for Section A

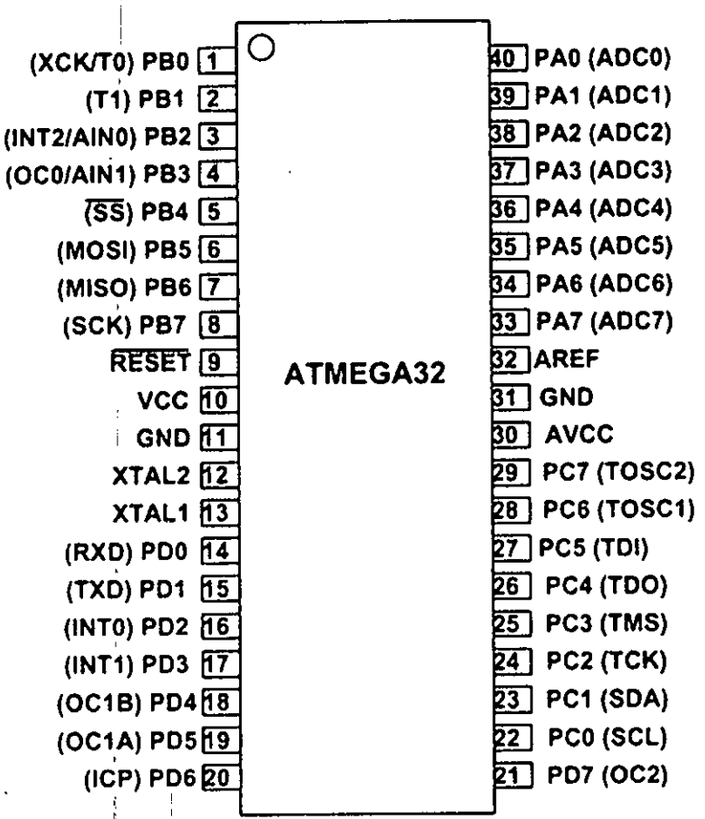


Figure: Atmega32 MCU Pinout

CSE 315

Table 1: Register Configurations of ATmega32

Name	Configuration							
GICR	INT1	INT0	INT2	-	-	-	IVSEL	IVCE
MCUCR	-	-	-	-	ISC11	ISC10	ISC01	ISC00
	Trigger codes: 00 → low level, 01 → any logical change, 10 → falling, 11 → rising							
ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0
	REFS1, REFS0: 00 → AREF, 01 → AVCC, 11 → Internal 2.56, ADLAR: 0 → Left							
	MUX4...0	Single Ended	Positive Differential	Negative Differential	Gain			
	00001	ADC1						
	01000		ADC0	ADC0	10x			
	01001		ADC1	ADC0	10x			
ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM
UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8
UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL
	UCSZ2, UCSZ1, UCSZ0: 000 → 5-bit, 001 → 6-bit, 010 → 7-bit, 011 → 8-bit, 111 → 9-bit							
	UPM1,UPM0: 00 → No parity, 10 → even parity, 11 → odd parity							
	USBS: 0 → 1 stop bit, 1 → 2 stop bits							
TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10
TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10
	CS12, CS11, CS10: 001 → No prescaling, 010 → clk/8, 011 → clk/64, 100 → clk/256							
TIMSK	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0

Table 2: Wave Generation Modes of TIMER1

WGM	Timer/Counter Mode of Operation	TOP	Update of OCR1X	TOV1 Flag Set on
1110	Fast PWM	ICR1	BOTTOM	TOP
1111	Fast PWM	OCR1A	BOTTOM	TOP
1010	Phase Correct PWM	ICR1	TOP	BOTTOM