BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2020-2021

Sub: **EEE 303** (Digital Electronics)

Full Marks: 210 Time: 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE** questions.

Symbols have their usual meanings.

1. (a) Draw the circuit to implement the function $f = \overline{x_1 + x_2.x_3}$ in switch level representation. **(10)**

   (b) Write the Verilog code for the function in Question 1(a). **(6)**

   (c) Convert $5432|_6$ into octal, hexadecimal and binary numbers. **(9)**

   (d) With a simple example explain what is glitch and how it can be solved. **(10)**

2. (a) Implement the function f= (A+B) $(C.\overline{D} + \overline{E})$ using NAND gates only. **(7)**

   (b) Design the minimum cost circuit that implements the function $f(x_1, x_2, x_3) = \sum_m (1, 3, 4, 6, 7)$. Determine the cost. Assume that input variables are available both in complemented and uncomplemented forms. **(8)**

   (c) Binary variables A, B, C, D are used to represent a decimal digit where A is the MSB and D is the LSB. Derive a SOP expression for segment b of a 7-segment display using the variables A,B,C,D and then minimize the expression using a K-map. The 7-segment display is shown in Fig. for Question 2(c). **(10)**

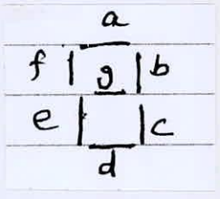

Fig. for Question 2(c).

   (d) Write the Verilog code for the implementation of a 7-segment display. **(10)**

3. (a) Draw the circuit of a 64 bit ALU with Negative, Zero, Carry out and Overflow flags. The ALU receives a 2-bit control signal ALU $\text{Control}_{1:0}$ and performs the functions shown in Table for Question 3(a). **(18)**

Contd P/2

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Contd... Q. No. 3(a)

Table for Question 3(a)

ALU Control$_{1:0}$	Function
00	Add
01	Subtract
10	AND
11	OR

(b) Write the verilog code for the ALU defined in Question 3(a). **(17)**

4. (a) Implement the function $f(x_1, x_2, x_3) = \sum_m (1, 3, 5, 7)$ using a 1-to-8 demultiplexer. **(7)**

(b) Design and implement an 8-to-1 multiplexer using a 3-to-8 decoder. **(8)**

(c) Write the verilog code for the 8-to-1 multiplexer that you designed in Question 4(b) using a 3-to-8 decoder. **(10)**

(d) Why address multiplexing is done for accessing memory? With a neat timing diagram, explain how address multiplexing is performed for memory access. **(10)**

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Draw a circuit diagram for a 5 bit ring counter using S-R flip-flops. Briefly explain with truth table, how your circuit operates. Write a Verilog module for module for implementing a 5 bit ring counter **(15)**

(b) Design a modulo-9 counter using T-flip-flops and basic gates. Draw the complete digital circuit diagram of your design. **(10)**

(c) Using D-flipflop and 2-to-1 MUX, design a 4 bit parallel-load universal shift register (that can selectively left shift or right shift the stored data). With truth table, briefly explain how your design works. **(10)**

6. (a) A synchronous FSM takes two inputs, A and B, and generates one output, Z. The output in cycle n, Z_n, is either the Boolean AND or OR of the corresponding input A_n and the previous input A_{n-1}, depending on the other input, B_n. **(20)**

$Z_n = A_n A_{n-1}$ if $B_n = 0$,

$Z_n = A_n + A_{n-1}$ if $B_n = 1$.

Contd P/3

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Contd... Q. No. 6(a)

(i) Design the FSM with the given characteristics. Show the state transition diagram, encoded state transition table, next state and output equations, and schematic using D flipflops and logic gates.

(ii) For a particular case, if CLK, A and B has the waveshapes given in Fig. for Q6 (a), and x axis denotes time, neatly sketch the output waveform Z.

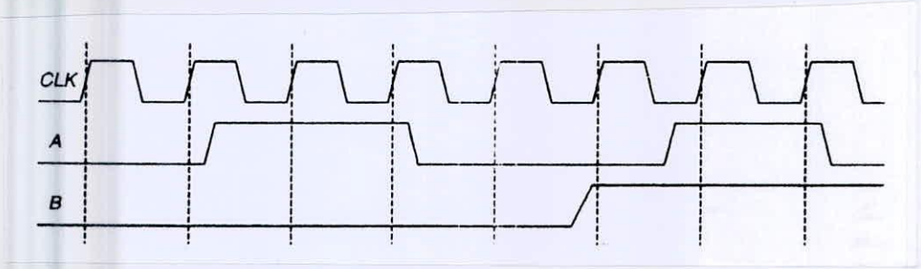

Fig. for Q6(a)

(b) The State Transition Diagram of a Finite State Machine is given in the Fig. for Q6(b). Minimize the states using partitioning with brief written description of each minimization steps. Write a Verilog code to implement the FSM. **(15)**

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	B	C	0	0
B	D	–	0	0
C	F	E	0	1
D	B	G	0	0
E	F	C	0	1
F	E	D	0	1
G	F	–	0	1

Fig. for Q6(b)

7. (a) Design an Asynchronous Sequential Circuit with an input w and output z, such that when pulses are applied to w, the output z is equal to 1 if the number of previously applied pulses is even, and z is equal to 0 if the number of pulses is odd. Write the State Transition Diagram, Flow Table, and using the appropriate state assignment, derive the logic expressions for the output. Implement the Asynchronous Sequential Circuit with basic gates. **(15)**

(b) The table in Fig. for Q7(b) shows the relation between scaling different parameters and their effect on circuit speed, performance and power. In each case of Full Scaling and General Scaling, derive the value of S and U for reducing the transistor area to half. Also, find out the power density in each case. **(10)**

Contd P/4

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Contd... Q. No. 7(b)

Parameter	Relation	Full Scaling	General Scaling	Fixed-Voltage Scaling
W, L, t_{ox}		$1/S$	$1/S$	$1/S$
V_{DD} V_T		$1/S$	$1/U$	1
N_{SUB}	V/W_{dep}^2	S	S^3/U	S^2
Area/Device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_{gate}	$C_{ox}WL$	$1/S$	$1/S$	$1/S$
k_n, k_p	$C_{ox}W/L$	S	S	S
I_{sat}	$C_{ox}WV$	$1/S$	$1/U$	1
Current Density	I_{sat}/Area	S	S^3/U	S^2
Ron	V/I_{sat}	1	1	1
Intrinsic Delay	$R_{on}C_{gate}$	$1/S$	$1/S$	$1/S$
P	$I_{sat}V$	$1/S^2$	$1/U^2$	1
Power Density	P/Area	1	S^3/U^2	S^2

Fig. for Q7(b).

(c) Sketch neat circuit diagrams to implement the logic function AB+CD using (i) Pass Transistor Logic (ii) CMOS Transmission Gates and (iii) CMOS technology. **(10)**

8. (a) Fig. for Q8(a) shows the block diagram of an SAP-1 computer. Briefly describe the 6 machine states for the LDA command. Derive the value of the CON control word for 6 machine cycles of executing the LDA command. **(15)**

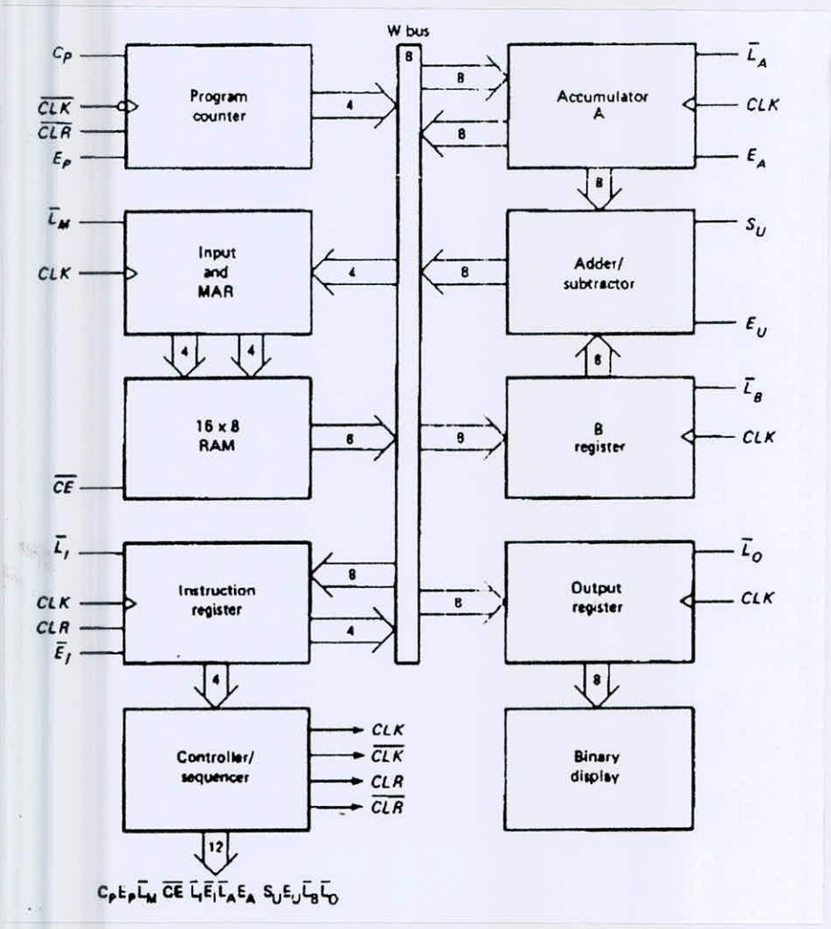

Fig. for Q8(a)

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Contd... Q. No. 8

(b) The given program is written for a SAP -2 computer with 8-bit data and 16 bit address bus, running at 10 kHz clock frequency. Fig. for Q8(b) shows the information for the relevant instructions used in the program. **(15)**

Label	Mnemonic
	MVI C, 78H
LOOP:	DCR C
	NOP
	JNZ LOOP
	HLT

i) Find out how long would it take to execute the program in the SAP-2 computer.
ii) Modify the program (by adding / changing instructions) so that it now takes as close to 1s execution time as possible. Write your modified code, and calculate the new execution time.

Instruction	**Op Code**	***T* States**	**Flags**	**Addressing**	**Bytes**
NOP	00	4	None	–	1
JNZ address	C2	10/7	None	Immediate	3
MVI C, byte	0E	7	None	Immediate	2
DCR C	0D	4	S, Z	Register	1
HLT	76	5	None	–	1

Fig. for Q8(b)

(c) What does PCB stand for? Briefly describe the steps of a PCB Design. **(5)**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2020-2021

Sub: **EEE 313** (Solid State Devices)

Full Marks: 210 Time: 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks

SECTION – A

There are **FOUR** questions in this section.

Answer any **THREE** question including Question No. 1.

1. (a) The Figure for Question no. 1 shows the metal-semiconductor work function difference versus doping concentration for aluminum, gold, n^+ and p^+ polysilicon gates. For a p-type silicon substrate having doping concentration of 10^{15} cm^{-3}, you have to design a MOSFET which will operate as a depletion mode device. Suppose there are 10^{10} cm^{-2}trap charges in the 12 mm thick gate oxide layer. The relative permittivity of the gate oxide material and silicon are 3.9 and 11.7, respectively, and the intrinsic carrier concentration of silicon is 1.5×10^{10} cm^{-3}. **(35)**

i. With necessary calculations, suggest the appropriate choice of gate metal to design the depletion mode MOSFET. Draw the energy band diagram of the MOSFET under zero-bias condition.

ii. Calculate the threshold voltage and flat-band voltage of your designed MOSFET.

iii. What would be your choice of metal if you were asked to design an enhancement mode MOSFET? Show necessary calculations to justify your answer.

iv. Suppose you have finalized the design of the MOSFET. Now suggest a technique of changing the threshold voltage of the MOSFET by external means. Write down necessary equation(s) to support your answer.

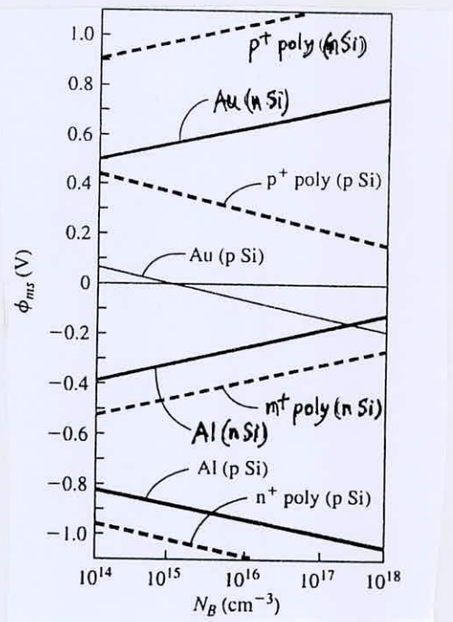

Figure for Question no. 1

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2. (a) Consider a p-n-p BJT operating in the active mode. Derive the expression of emitter injection efficiency for this BJT. Based on your derivation, decide whether the emitter or the base should have a higher doping concentration to obtain a high common-emitter gain. **(18)**

(b) Consider a p-type semiconductor having a bandgap of 1 eV and an electron affinity of 4 eV. The doping concentration of the semiconductor is 10^{17} cm^{-3} and the effective density of states in the valence band of the semiconductor is 10^{19} cm^{-3}. **(17)**

i. With necessary calculations, chose a metal from the Table for Question no. 2(b) to design a Schottky junction so that the built-in voltage of the device is as large as possible.

ii. Calculate the space charge width and the maximum electric field of your designed Schottky junction for zero applied bias.

iii. Draw the energy band diagram of your designed metal semiconductor junction for a positive bias applied at the metal side.

Element	Work function, ϕ_m(eV)
Ag, silver	4.26
Al, aluminum	4.28
Au, gold	5.1
Cr, chromium	4.5
Mo, molybdenum	4.6
Ni, nickel	5.15
Pd, palladium	5.12

Table for Question no. 2(b)

3. (a) Consider the high-frequency C-V curve plot shown in the Figure for Question 3(a). **(18)**

i. Is this C-V characteristics curve of a p-MOS or n-MOS? Why?

ii. Draw the energy band diagram for each point 1, 2, 3, 4, 5 labelled on this plot.

iii. Suppose, from measurements, the following results are obtained:

- At point 5, capacitance performance unit area = 20×10^{-8} F/cm^2
- At point 4, capacitance performance unit area = 17×10^{-8} F/cm^2

If relative permittivity of the gate oxide and the channel material are 3.9 and 11.7, respectively, calculate the doping concentration of semiconductor.

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Contd... Q. No. 3(a)

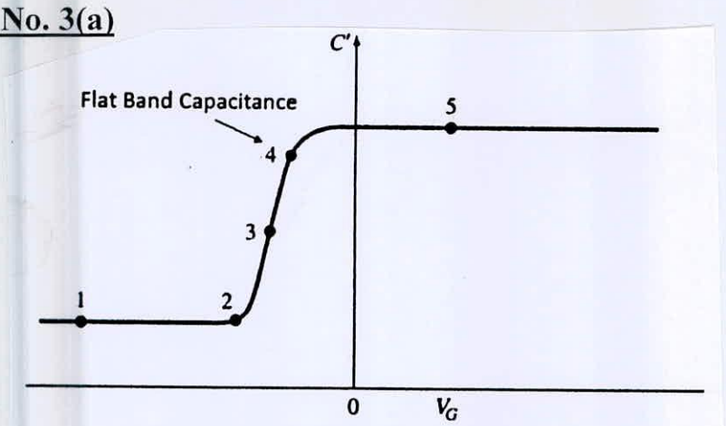

Figure for Question no. 3(a)

(b) With proper labelling, draw the excess minority carrier concentration profiles of an n-p-n BJT operating in the following modes: **(17)**

i. Reverse active mode

ii. Saturation mode

Write down the differential equations and boundary conditions required to obtain the expressions of minority carrier concentration profiles in the emitter, base, and collector regions of the device operating in saturation mode.

4. (a) Consider an n-MOS transistor operating in the triode region. If V_x denotes the potential drop at any point x in the channel, show that the drain to source current of the MOSFET is given by: **(18)**

$$I_x = -W\mu_n C_{ox} \frac{dV_x}{dx}\left[(V_{GS} - V_x) - V_T\right].$$

Mention the assumptions you used in deriving the above expression.

(b) Consider a p-n junction diode with the following material parameters: **(17)**

$$N_a = 10^{18} cm^{-3} \qquad N_d = 10^{16} cm^{-3}$$
$$D_p = 10 cm^2/s \qquad D_n = 25 cm^2/s$$
$$\tau_{po} = 10^{-7} s \qquad \tau_{no} = 10^{-7} s$$

Intrinsic carrier concentration of the p-n junction diode's semiconductor material is 10^{10} cm^{-3}. For an application, you need 10 A/ cm^2 forward bias current. To achieve this current, you are asked to design a Schottky diode such that the forward bias voltage required for the diode is approximately half of the forward bias voltage required by the p-n junction diode.

i. Assuming the effective Richardson constant to be 114 A/K^2- cm^2, calculate the Schottky barrier height of your proposed diode.

ii. Based on the experimental data given in Figure for Question no. 4(b), suggest the combination of metal-semiconductor which best satisfies your design.

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Contd... Q. No. 4(b)

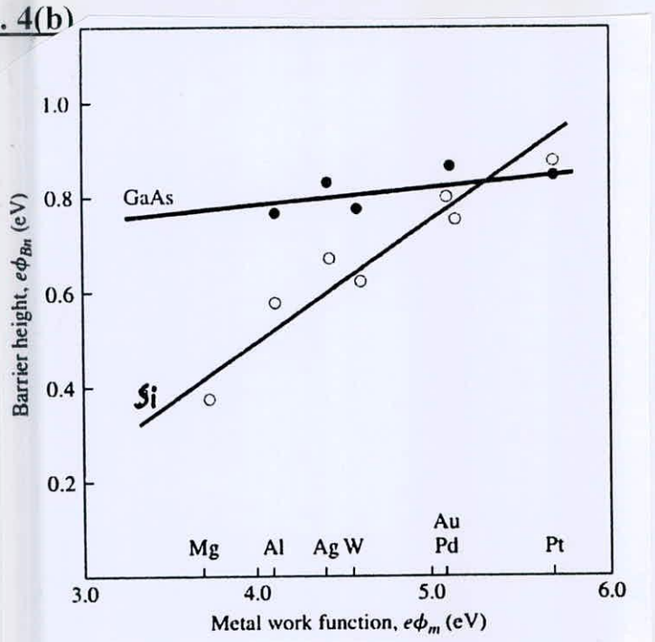

Figure for Question no. 4(b)

List of relevant Equations (the symbols have their usual meanings)

$$W = x_n = \left[\frac{2\epsilon_s(V_{bi} + V_R)}{eN_d}\right]^{1/2}$$

$$J = \left[A^* T^2 \exp\left(\frac{-e\phi_{Bn}}{kT}\right)\right]\left[\exp\left(\frac{eV_a}{kT}\right) - 1\right]$$

$$\delta n_B(x) = \frac{n_{B0}\left\{\left[\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right]\sinh\left(\frac{x_B - x}{L_B}\right) - \sinh\left(\frac{x}{L_B}\right)\right\}}{\sinh\left(\frac{x_B}{L_B}\right)}$$

$$\delta p_E(x') = \frac{p_{E0}\left[\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right]\sinh\left(\frac{x_E - x'}{L_E}\right)}{\sinh\left(\frac{x_E}{L_E}\right)}$$

$$\phi_{ms} \equiv \left[\phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right]$$

$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} - \phi_{fn}\right)$$

$$V_{TN} = \left(|Q'_{SD}(\max)| - Q'_{ss}\right)\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2\phi_{fp}$$

$$V_{TP} = \left(-|Q'_{SD}(\max)| - Q'_{ss}\right)\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} - 2\phi_{fn}$$

$$x_{dT} = \left\{\frac{4\epsilon_s\phi_{fn}}{eN_d}\right\}^{1/2}$$

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\left(\frac{kT}{e}\right)\left(\frac{\epsilon_s}{eN_a}\right)}}$$

$$C'_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)x_{dT}}$$

$$\Delta Q'_{SD} = -\sqrt{2e\epsilon_s N_a}\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

Contd P/5

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SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

Question Five (5) is compulsory.

All the Symbols have their usual meanings, List of relevant equations are attached.
Assume reasonable values for missing data.

5. In this problem, we will design a Si diode to attain specific built-in potential and electric field profile. The diode has four regions. Each region is 1 μm long. The doping profile of the device is given by:

$$N(x) = \begin{cases} N_D - N_A = -N_{d0}, -2 \le x \le -1 \\ N_D - N_A = N_{d0}x, -1 \le x \le 1 \\ N_D - N_A = N_{d0}, \quad 1 \le x \le 2 \end{cases}$$

Where N_{d0} is a constant and x is in μm. $N(x) < 0$ implies p-type doping and $N(x) > 0$ implies n-type doping. The build-in potential of the diode from x = -2μm to x = 2μm is 0.596 V. Both the acceptor and donor energy levels are such that only 20% of the dopants are activated.

i. Determine the energy levels of the acceptor and donor atom with respect to the Fermi level for the above case.

ii. Find the doping concentration N_{d0} and draw the doping profile of the device.

iii. Draw the Energy band diagram of the device with proper leveling of the energy levels.

iv. If the thermal equilibrium depletion widths on both sides are $|x_N| = |x_P| = 0.25$ μm, draw the charge density in the space charge region. Also, determine and plot the electric field in the depletion region.

v. Now a bias voltage V_R is applied to this diode and it is found that the depletion widths on both sides are $|x_N| = |x_P| = 1$ μm. Without any mathematical derivation, qualitatively plot the electric field in the depletion region. **(6+5+5+12+7=35)**

6. (a) A p-type semiconductor sample of length $6L$ with doping concentration N_A is illustrate at two location as shown in Fig. for Question 6(a). The illustration rates are G0 and $2G_0$ at x = $-L$ and $x = L$, respectively. Assume low-level injection and zero applied electric field in the sample. The right and left contacts of the semiconductor device are ohmic, i.e., the excess minority carrier hole concentration is zero at those points. μ_n is the electron mobility, τ_{no} is the minority carrier lifetime, and D_n is the finite electron diffusion coefficient. **(5+4+10+6=25)**

Contd P/6

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Contd... Q. No. 7

(b) The critical field for breakdown of Si is 4×10^5 Vcm^{-1}. Draw the $1/C^2$ vs. V_R characteristics of an abrupt p^+n diode for breakdown voltage 30V and 60V assuming the critical field does not change with doping concentration. From these two curves, comment on the relation between the slope of $1/C^2$ vs. V_R characteristic and breakdown voltage of the diode. Dielectric constant of silicon is 11.7. **(12)**

8. (a) Consider a non-degenerate semiconductor in thermal equilibrium at 300 K with the following material parameters: **(8+10=18)**

$\mu_n = 1000\ cm^2V^{-1}s^{-1}$, $\mu_p = 350\ cm^2V^{-1}s^{-1}$, $N_c = 2.78 \times 10^{19}\ cm^{-3}$,

$N_v = 9.84 \times 10^{18}\ cm^{-3}$, $n_i = 1.5 \times 10^{10}\ cm^{-3}$,

$E_g = 1.1$ eV, $m_e^* = 0.26m_0$ and $m_h^* = 0.8m_0$.

i) If the material is doped with doping concentration $N_d = 10^{17}\ cm^{-3}$, the mobility dcreases to $600\ cm^{-3}V^{-1}s^{-1}$. Compute the relaxation time due to ionized impurity scattering if the activation of the donors is 50% at 300K.

ii) Using the data given above, find the maximum, minimum and undoped conductivity for material. Comment on the result.

(b) Consider an n-type semiconductor in equilibrium with spatially varying doping profile $N_D(x)$. The induced electric field $E(x)$ due to nonuniform doping is given by $E(x) = \dfrac{2k_BTx}{eL^2}$ where L is the length of the device. **(3+6+8=17)**

i) Find the potential difference between x = 0 and x = L.

ii) Find and draw the doping profile $N_D(x)$. Assume the $N_D(0) = N_0$.

iii_ Draw the qualitative Energy band diagram of the semiconductor showing E_C, E_F, E_{Fi}, and E_v.

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Contd... Q. No. 6(a)

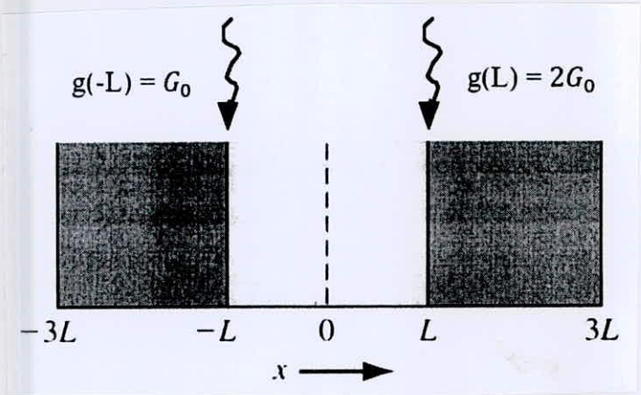

Fig. for Question 6(a)

i) Explain briefly why a single Fermi leel cannot be used to represent the band diagram of the semiconductor device in Fig. for Question 6(a) under illumination.

ii) Write down the transport equation for the excess minority carriers for $-3L \leq x \leq 0$ and $0 \leq x \leq 3L$ with appropriate boundary conditions. Note that at any point inside the semiconductor sample, the excess minority carrier concentration is continuous and the diffusion current is finite.

iii) Determine and plot the spatial dependence of the steady state excess minority carrier concentration of the deice using the assumption $L_e \rightarrow \infty$ where L_e is the electron diffusion length.

iv) Plot the spatial dependence of the minority carrier diffusion current density inside the semiconductor.

(b) Describe briefly with necessary equations the ideal electron and hole components through a pn junction under forward bias. **(10)**

7. (a) Consider an n-type semiconductor with doping concentration N_D, electron, and hole effective masses m_e^* and m_h^*, respectively, and E_F is the Fermi level. **(7+11+5=23)**

i) Plot qualitatively electron concentration versus temperature curve for the semiconductor showing regions: Partial Ionization, Extrinsic and Intrinsic for doping concentration N_D and $10N_D$.

ii) We define intrinsic temperature T_{int} as the temperature at which the extrinsic semiconductor becomes intrinsic. Assuming the Boltzmann approximation is valid, determine the relation between T_{int} and material band gap E_g for a semiconductor with doping concentration N_D.

iii) Consider the intrinsic carrier concentration versus temperature curve shown in Fig. for Question 7(a) (iii). Which of the materials from GaN, GaAs, Si and Ge will be suitable for high temperature operation? Explain very briefly.

Contd P/7

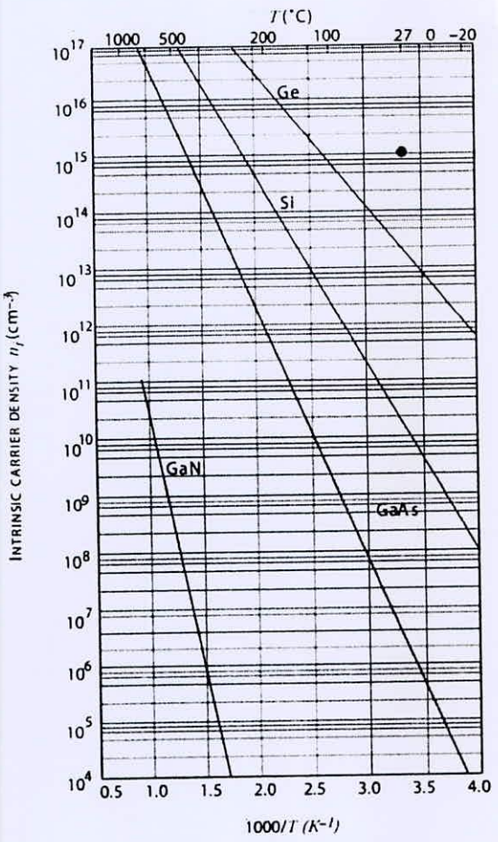

Fig. for Question 7 (a) (iii)

List of Equations

Symbols have their usual meaning.

1. $N_c = 2\left(\frac{2\pi m_n^* k_B T}{h^2}\right)^{\frac{3}{2}}$

2. $N_v = 2\left(\frac{2\pi m_p^* k_B T}{h^2}\right)^{\frac{3}{2}}$

3. $n_0 = N_c \exp\left(-\frac{E_c - E_F}{k_B T}\right)$

4. $n_d = \frac{N_d}{1+\frac{1}{2}\exp\left(\frac{E_d - E_F}{k_B T}\right)}$

5. $p_a = \frac{N_a}{1+\frac{1}{g}\exp\left(\frac{E_F - E_a}{k_B T}\right)}$

6. $J_{\text{drift}} = e(\mu_n n + \mu_p p)E$

7. $J_{\text{total}} = en\mu_n E + ep\mu_p E + eD_n \nabla n - eD_p \nabla p$

8. $E_x = -\left(\frac{k_B T}{e}\right)\frac{1}{N_d(x)}\frac{dN_d(x)}{dx}$

9. $D_n \frac{\partial^2(\delta n)}{\partial x^2} + \mu_n E \frac{\partial(\delta n)}{\partial x} + g' - \frac{\delta n}{\tau_{n0}} = \frac{\partial(\delta n)}{\partial t}$

10. $D_p \frac{\partial^2(\delta p)}{\partial x^2} + \mu_p E \frac{\partial(\delta p)}{\partial x} + g' - \frac{\delta p}{\tau_{n0}} = \frac{\partial(\delta p)}{\partial t}$

11. $x_n = \left\{\frac{2\epsilon_s V_{bi}}{e}\left[\frac{N_a}{N_d}\right]\left[\frac{1}{N_a + N_d}\right]\right\}^{\frac{1}{2}}$

12. $x_p = \left\{\frac{2\epsilon_s V_{bi}}{e}\left[\frac{N_d}{N_a}\right]\left[\frac{1}{N_a + N_d}\right]\right\}^{\frac{1}{2}}$

13. $E_{\max} = -\frac{eN_d x_n}{\epsilon_s}$

14. $V_B = \frac{\epsilon_s E_{\text{critical}}^2}{2eN_B}$

L-3/T-2/EEE **Date: 30/04/2023**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2020-2021

Sub: **EEE 315** (Power Electronics)

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE** questions.

All the symbols and notations used in this section bear their usual meanings.

1. (a) Classify converters depending on the following bases: (i) Output wave-shapes (ii) Number of input phases, and (iii) Operating zones (quadrants in the *i-v* characteristics). Provide illustrative examples where necessary. **(7)**

(b) Draw a single-phase full converter (controlled rectifier) with highly inductive load and derive the expression of average output voltage as a function of the firing angle α. **(11)**

(c) The three-phase controlled rectifier of Fig. for Q. No. 1(c) is directly supplied from a 4160-V rms line-to-line 50-Hz source connected in delta. The load is a 120-Ω resistor. (i) Determine the delay angle required to produce an average load current of 25 A. (ii) Estimate the amplitudes of the voltage harmonics V_6, V_{12}, and V_{18}. (iii)Sketch the currents in the load, S_1, S_4, and phase A of the AC source. **(17)**

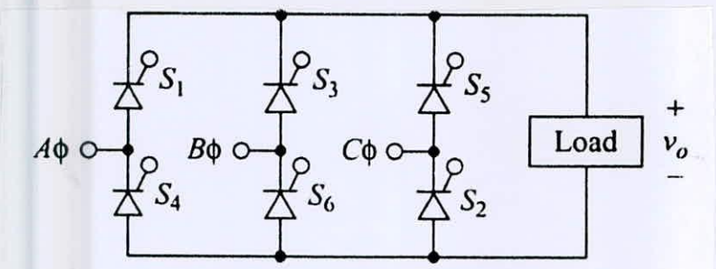

Fig. for Q. No. 1(c)

2. (a) Draw three-phase voltage-source inverters and with the help of switching states tables, explain their operating principles considering (i) 120-degree conduction (ii) 180 degree conduction. Compare the output parameters of these two cases. **(20)**

(b) For a full-bridge inverter, the DC source is 125 V, the load is a series *RL* connection with R = 10 Ω and L = 20 mH, and the switching frequency is 50 Hz. (i) Determine the THD of the load voltage, and (ii) If displacement power factor of the load is 0.9 lag, then what will be the "true" power factor? **(15)**

Contd P/2

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3. (a) Mention the four (4) types of Pulse-Width Modulation (PWM) techniques applied for voltage control of inverters. Illustrate the modified sinusoidal PWM technique and describe its advantages over other PWM techniques. **(15)**

(b) Draw and explain the block diagram that can be used for digital implementation of the Space Vector Modulation (SVM) algorithm to improve performance of inverters. **(10)**

(c) From applicational view point, mention some additional features of an AC power supply unit over an inverter. Also briefly describe the advantages of Variable Speed Drives (VFDs). **(10)**

4. (a) Classify the DC power supply units and given examples of suitable applications from each class. **(8)**

(b) Draw and explain the operation of a reversible phase-controlled induction motor drive. **(8)**

(c) Draw the block diagram of a PV solar-based power network including (i) Panel-MPPT, (ii) Charge Controller-Battery, and the (iii) Inverter-Grid. **(9)**

(d) For grid-connected wind turbine, is the use of a converter essential? Explain the reasons. Also prove that wind power is proportional to the cube of the wind velocity. **(10)**

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE** questions.
The symbols have their usual meaning. Assume reasonable values for any missing data.

5. The dc\dc converter of Fig. for Q. No. 5 below takes in a DC input current I_1, and drives a DC output voltage V_2

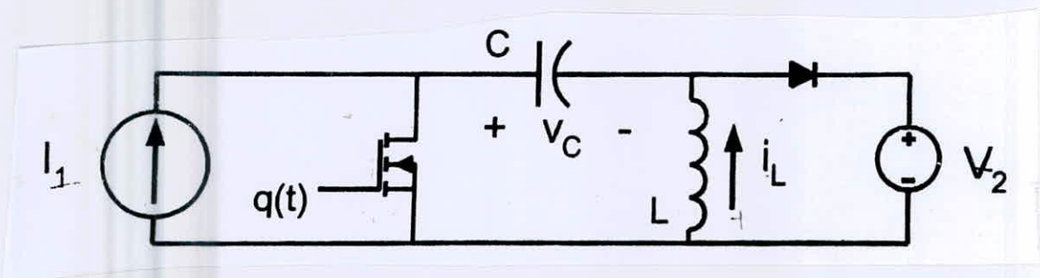

Fig. for Q. No. 5

(a) Find an expression for the DC inductor current I_L (in periodic steady state for continuous conduction mode operation) as a function of input current I_1 and switch duty ratio D. **(15)**

(b) Derive an averaged model for this converter in continuous conduction under duty ratio control (i.e. expression of V_2 as a function of I_1 and D). Assume that the ripple in i_L and v_C are small. **(20)**

Contd P/3

EEE 315

6. (a) Explain the operation of the following forced communication circuit with necessary waveforms. **(20)**

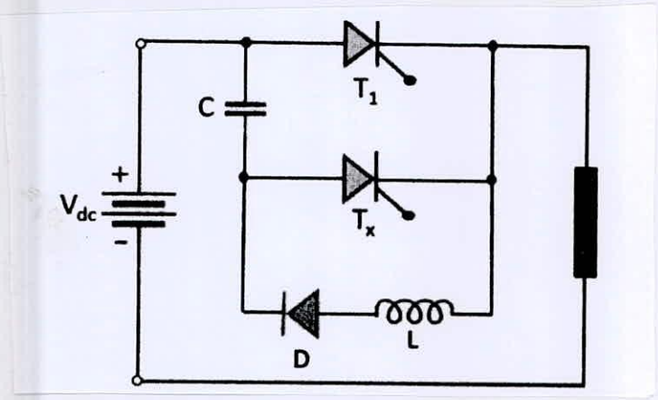

Fig. for Q. No. 6(a)

(b) Define latching current and holding current of a thyristor and label them in the I-V characteristics of a SCR. **(8)**

(c) Through a two-transistor model show that a high *dv/dt* across anode-cathode can cause the SCR to turn-on. **(7)**

7. (a) Draw the circuit diagram of a single phase cycloconverter. **(8)**

(b) Explain the necessary waveforms how the circuit drawn in Q. No. 7(a) can be used to generate 20 Hz (frequency down conversion) as well as 180 Hz (frequency up conversion) periodic signals from 60 Hz sine wave. **(20)**

(c) Draw the circuit diagram of a matrix converter and briefly explain its operation. **(7)**

8. (a) With neat sketches, explain the working principles and draw the i-v characteristics of (i) IGBT and (ii) GTO. **(20)**

(b) Draw the schematic diagram of a SEPIC type circuit arrangement and mention it's advantages. Also, define inverse of a SEPIC. **(15)**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2020-2021

Sub: **EEE 317** (Control system - I)

Full Marks: 210 Time: 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE** questions.

1. (a) For the following digital system find the range of sampling interval T to make the system stable. **(10)**

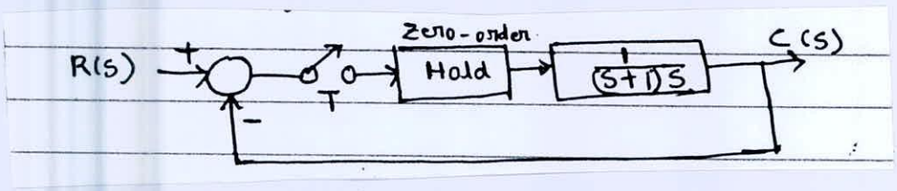

Fig. for Q. 1(a)

(b) Find the closed loop transfer function for the system shown in Fig. for Q. 1(b) in Z-domain. **(17)**

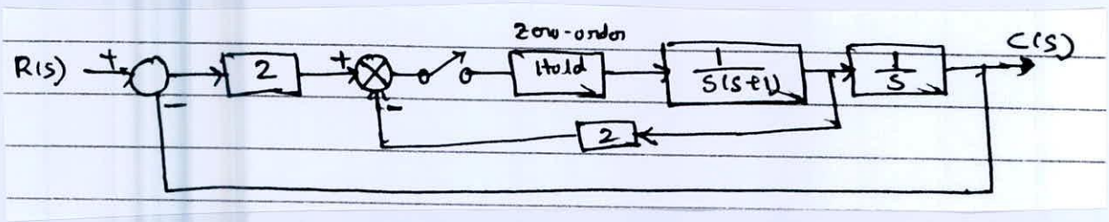

Fig. for Q. 1(b)

(c) For the feedback control system shown in Fig. for Q. 1(c), find static error constant and steady state error for unit step input. **(8)**

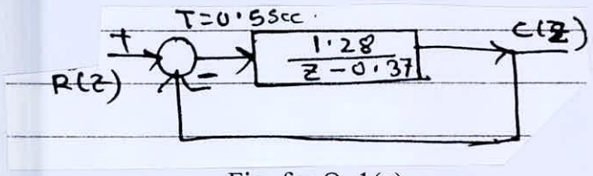

Fig. for Q. 1(c)

2. (a) A lead compensator has the following transfer function. **(10)**

$$G_c(S)=\frac{1}{\beta}\frac{S+\frac{1}{T}}{S+\frac{1}{\beta T}} \quad \text{where } \beta < 1.$$

Contd …… P/2

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Contd... Q. No. 2(a)

show that the angular frequency at which the maximum phase angle ϕ_{max} occurs is $w_{max} = \frac{1}{T\sqrt{\beta}}$ and ϕ_{max} can be expressed as $\phi_{max} = \tan^{-1}\frac{1-\beta}{2\sqrt{\beta}}$.

Also find the $|G_c(jw_{max})|$.

(b) Design a lead compensator of the form as mentioned in Q. No. 2(a) for a unity negative feedback control system with an open loop transfer function **(25)**

$$G(S) = \frac{k}{s(s+5)(s+20)}$$

The uncompensated system has about 55% overshoot and a peak time of 0.5 second when $K_u = 10$. Use frequency response method to design the lead compensator with a target to yield a percent overshoot of 10%. While keeping the peak time and steady state error about the same or less. Make required second order approximation.

3. (a) A feedback control system having the following open loop transfer function **(20)**

$$GH(jw) = \frac{10(1+j0.5w)}{(1+jw)\left[1+j0.5w+0.25(jw)^2\right]}$$

The log-magnitude and phase angle at different frequencies of GH(jw) is given in the following table.

w	dB	∠GH(jw)	w	dB	∠GH(jw)
0	20	0	6.0	-5.2	-170°
1.2	18.4	-65°	8.0	-10.0	-175°
1.6	17.8	-86°			
2.0	16.0	-108°			
2.8	10.5	-142°			
4.0	2.7	-161°			

Using Nichol's chart find (i) Gain margin, phase margin, phase - crossover frequency and gain cross- over frequency. (ii) peak value of the closed loop magnitude response and peak frequency. Is the system stable or unstable?

(Attach the used Nichol's chart along with your answer script).

(b) State and explain Nyquist stability criterion. For the following systems shown, in Figs 3(b) determine whether the system is stable or unstable by sketching the complete Nyquist diagram. **(15)**

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Contd... Q. No. 3(b)

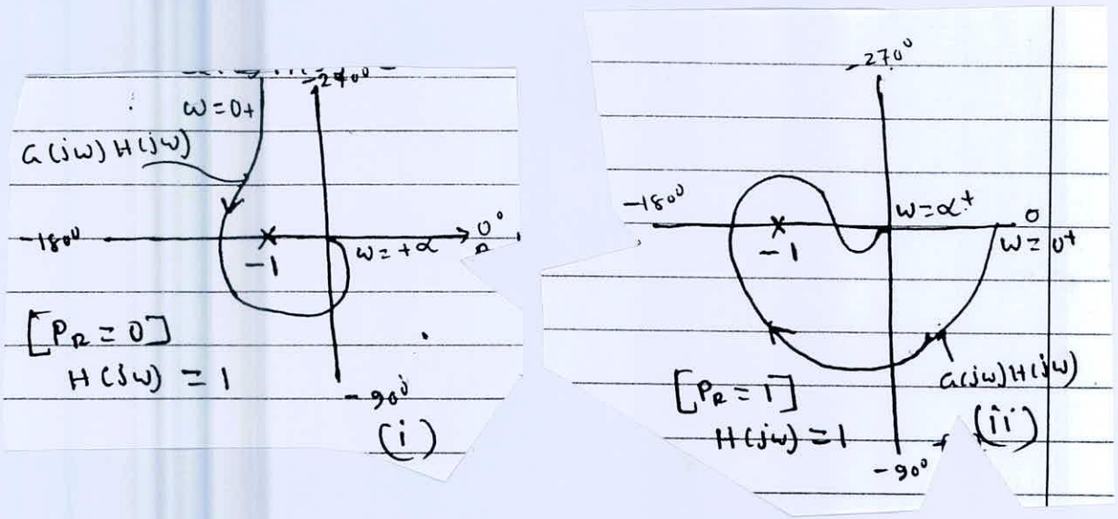

Fig. for Q. 3(b)

4. (a) Find the transfer function G(s) = Y(s)/R(s) for the following system represented in state space. **(12)**

$$\dot{x} = \begin{bmatrix} 2 & -3 & -8 \\ 0 & 5 & 3 \\ -3 & -5 & -4 \end{bmatrix} x + \begin{bmatrix} 1 \\ 0 \\ 6 \end{bmatrix} r$$

$$y = [1 \;\; 3 \;\; 6]x$$

(b) From the Bode plot as shown in Fig. 4(b) evaluate the transfer function. **(12)**

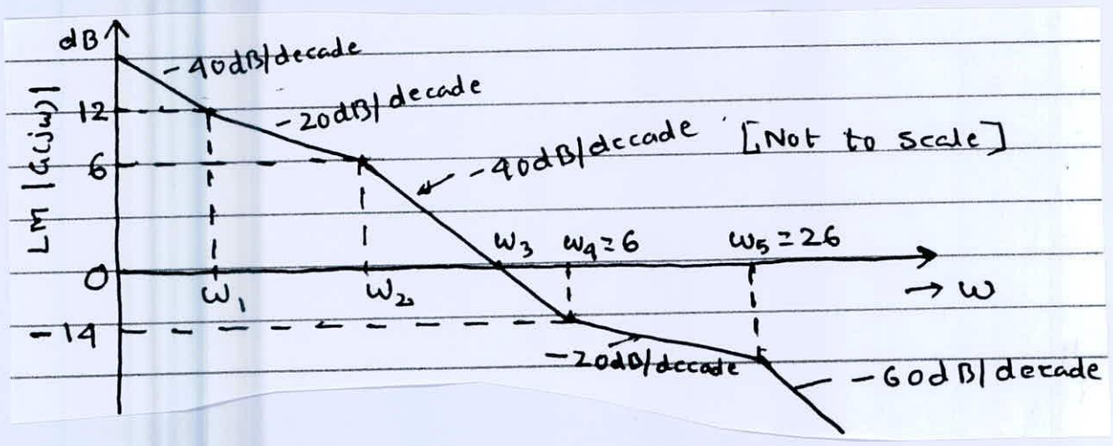

Fig. for Q. 4(b)

(c) From the block diagram obtain a state space model for the system shown in Figure 4(c). **(11)**

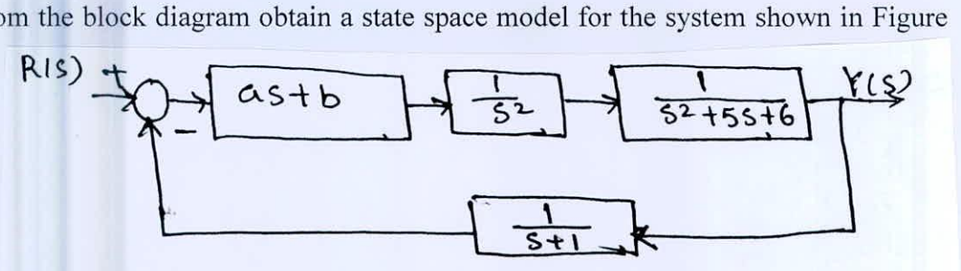

Fig. for Q. 4(c)

Contd P/4

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SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

All the Symbols have their usual meanings

5. (a) For the system shown in Fig. Q5(a), derive the expression for steady state error when both the input, R(s) and the disturbance, D(s) are present. **(15)**

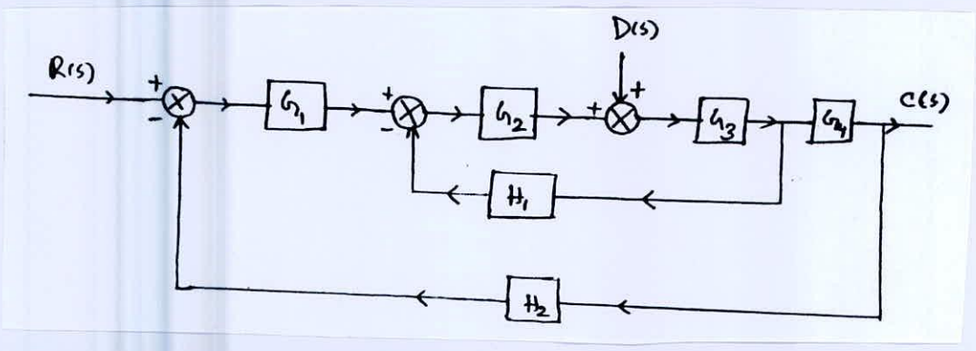

Fig. for Q. 5(a)

(b) Find the transfer function of the system shown in Fig. Q5(b). **(12)**

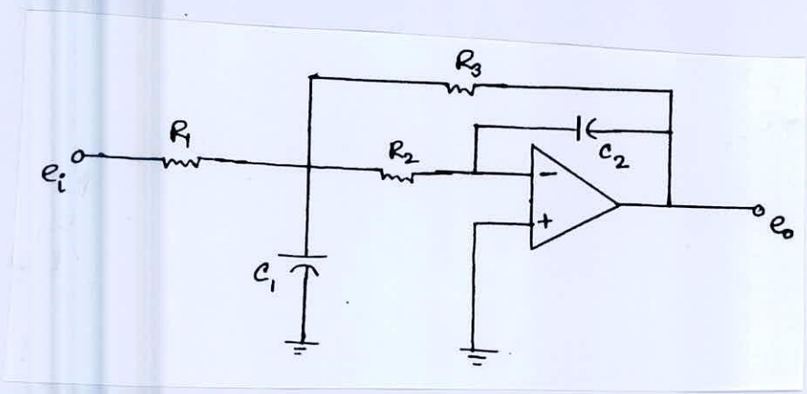

Fig. for Q. 5(b)

(c) Suppose, a second order system is operating with a damping ratio, ζ and a natural frequency, ω_n. A third pole at $-\alpha$ has been introduced into the system. With partial fraction method, determine the unit step response of the system after the addition of the pole. Also, explain how the position of the pole determines whether the system can be approximated as second-order or not. **(8)**

6. (a) For the unity gain negative feedback shown in Fig. Q6(a), determine the range of K for stability. **(12)**

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Contd... Q. No. 6(a)

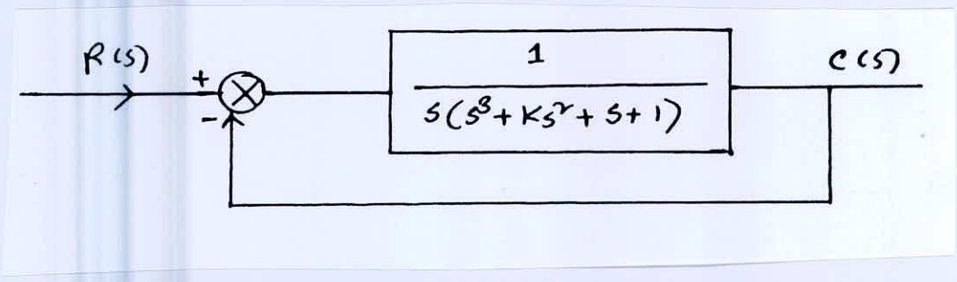

Fig. for Q. 6(a)

(b) For the system shown in Fig. Q(b), determine the following: **(13)**

i) The closed loop transfer function

ii) The steady state error for input 5u(t)

iii) The steady state error for input 5tu(t)

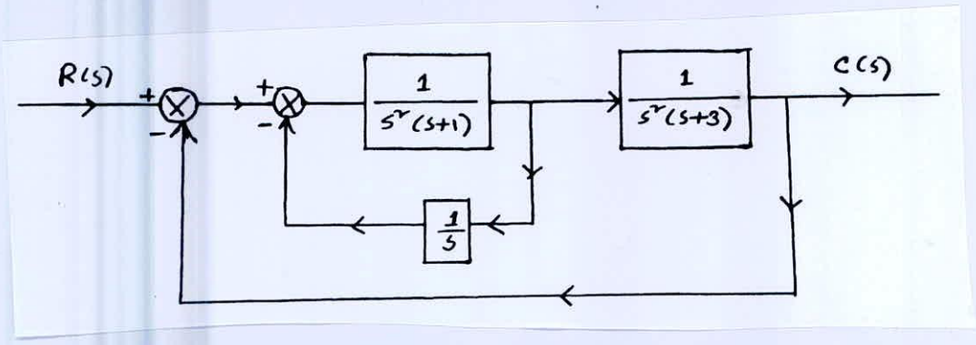

Fig. for Q. 6(b)

(c) Suppose, you have a negative feedback system as shown in Fig. Q6(c). If the forward path gain, G(s) increases by 10%, what is the percentage change in overall transfer function, T(s)? From your calculation, what comment can you make about negative feedback systems compared to open loop? **(10)**

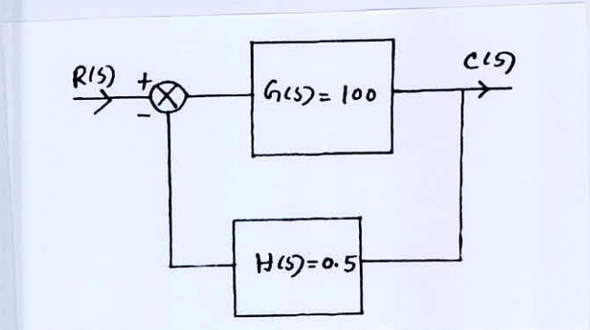

Fig. for Q. 6(c)

Contd P/6

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7. (a) Suppose, an open loop system has two negative and real poles at $s = -a$ and $s = -b$. Determine the analytical expression for settling time, Ts from the unit step response of the system. Assume that the system has settled when it reaches within ± 2% of its final value. **(15)**

(b) A schematic of a DC motor with mechanical loading is shown in Fig. Q 7(b). The input is the voltage, $e_a(t)$ and the output is the angular velocity $w_m(t)$. Draw a block diagram of the system and comment if there is any feedback. From the transfer function, $\frac{W_m(S)}{E_a(S)}$, sketch the root locus as the damping D_m is varied. K_t and K_b refer to the motor torque constant and back emf constant respectively. **(20)**

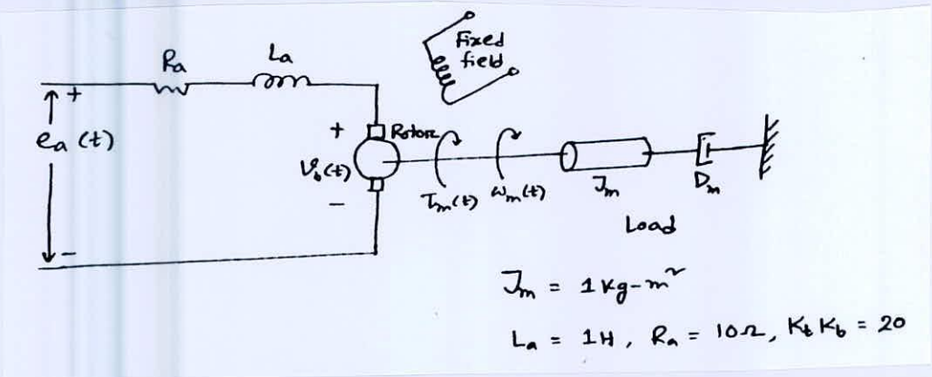

Fig. for Q. 7(b)

8. (a) A unity-gain negative feedback system having a forward path gain, G(s) has been compensated using a controller, $G_c(s)$ as shown in Fig. Q 8(a). The damping ratio of the dominant poles before and after compensation is 0.4. After compensation, the settling time is 0.5 seconds. Find the following: **(20)**

i) Location of the dominant poles
ii) Location of the zero of the compensator, z_c using root locus
iii) Required system gain
iv) The improvement in error after compensation (check if second-order approximate is valid)

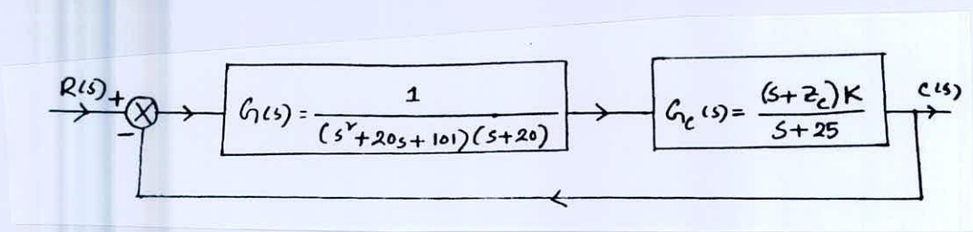

Fig. for Q. 8(a)

(b) A unity-gain negative feedback system with open loop transfer function, $G(s) = \frac{K}{(s+2)(s+6)}$ is operating with a peak time of 1.5 seconds. Perform the following: **(15)**

i) Find the operating gain of the system
ii) Design a lead compensator using root locus to provide a two-fold improvement on peak time
iii) Show a circuit realization for the designed lead compensator

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L-3/T-2/EEE **Date: 12/04/2023**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-2 B. Sc. Engineering Examinations 2020-2021

Sub: **IPE 493** (Industrial Management)

Full Marks: 210 Time: 3 Hours

USE SEPARATE SCRIPTS FOR EACH SECTION

The figures in the margin indicate full marks

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE** questions.

Assume any approximate values for missing data

1. (a) Define the following terms with an appropriate example: Direct cost, Indirect cost, Product cost and Period cost **(15)**

(b) Lamar Company is considering a project that would have a five-year life and require a $2,400,000 investment in equipment. At the end of five years, the project would terminate and the equipment would have no salvage value. The project would provide network operating income each year as follows: **(20)**

Sales		$3,200,000
Variable expenses		1,800,000
Contribution margin		1,400,000
Fixed expenses:		
Advertising, salaries, and other fixed out-of-pocket costs	$700,000	
Depreciation	300,000	
Total fixed expenses		1,000,000
Net operating income		$ 400,000

The company's discount rate is 12%.

Required:

1. Compute the annual net cash inflow from the project.
2. Compute the project's net present value. Is the project acceptable?
3. Compute the project's payback period.

2. (a) What do you understand by margin of safety and degree of operating leverage? If variable expense is increased keeping everything else constant, will the margin of safety and degree of operating leverage increase or decrease? Justify your answer. **(10)**

(b) Why aren't actual manufacturing overhead costs traced to jobs just as direct materials and direct labor costs are traced to jobs? Explain the process used to compute a predetermined overhead rate. **(10)**

(c) Lucido Products markets two computer games: Claimjumper and Makeover. A contribution format income statement for a recent month for the two games appears below: **(15)**

Contd P/2

IPE 493/EEE
Contd... Q. No. 4

	Claimjumper	Makeover	Total
Sales	$30,000	$70,000	$100,000
Variable expenses	20,000	50,000	70,000
Contribution margin	$10,000	$20,000	30,000
Fixed expenses			24,000
Net operating income			$ 6,000

Required:

1. Compute the overall contribution margin (CM) ratio for the company.
2. Compute the overall break-even point for the company in dollar sales.
3. Verify the overall break-even point for the company by constructing a contribution format income statement showing the appropriate levels of sales for the two products.

3. (a) Define Market Segmentation, Market Targeting, and Market positioning. **(10)**

(b) Explain 4 major geographic segmentation variables for consumer markets with appropriate examples. **(15)**

(c) The Lakeshore Hotel's guest-days of occupancy and custodial supplies expense over the last seven months were: **(10)**

Month	Guest-Days of Occupancy	Custodial Supplies Expense
March	4,000	$7,500
April	6,500	$8,250
May	8,000	$10,500
June	10,500	$12,000
July	12,000	$13,500
August	9,000	$10,750
September	7,500	$9,750

Guest-days is a measure of the overall activity at the hotel. For example, a guest who stays at the hotel for three days is counted as three guest-days.

Required:

1. Using the high-low method, estimate a cost formula for custodial supplies expense.
2. Using the cost formula you derived above, what amount of custodial supplies expense would you expect to be incurred at an occupancy level of 11,000 guest-days?

Contd P/3

4. (a) Let's say you work for a company that makes prepared breakfast cereals like corn flakes. Your company is planning to introduce a new hot breakfast product made from whole grains that would require some minimal preparation by the consumer. This would be a completely new product for the company. How would you propose forecasting initial demand for this product? **(08)**

(b) Demand for stereo headphones and MP3 players for joggers has caused Nina Industries to grow almost 50 percent over the past year. The number of joggers continues to expand, so Nina expects demand for headsets to also expend, because, as yet no safety laws have been passed to prevent joggers from wearing them. Demand for the players for last year was as follows: **(17)**

Month	Demand (units)	Month	Demand (units)
January	4,200	July	5,300
February	4,300	August	4,900
March	4,000	September	5,400
April	4,400	October	5,700
May	5,000	November	6,300
June	4,700	December	6,000

Using linear regression analysis, what would you estimate demand for the first four months of the next year?

(c) Demand for an item is constant at 200 units a month. The item can be made at a constant rate of 400 units a month. Unit cost is $50, batch set-up cost is $650, and holding costs is 30 per cent of value a year. Form the production, the stock is replenished gradually. What is the optimal batch size for the item? If production set-up time is 2 weeks, when should this be started? **(10)**

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Explain the universal need for management concept. Does it still hold true in todays world? Why or why not? **(10)**

(b) Discuss Hersey and Blanchard's Situational Leadership Theory model. How do you think follower readiness changes according to this theory? **(15)**

(c) Explain the contingency factors that affect organizational design. **(10)**

IPE 493/EEE
Contd... Q. No. 4

6. (a) Draw the managerial grid and explain the different categories of managerial styles. **(12)**

(b) Discuss the advantages and disadvantages of different performance appraisal methods. **(15)**

(c) Write down Taylor's Scientific Management Principles. **(8)**

7. (a) How is Maslow's Hierarchy of Needs related to motivation in a organization? Discuss the limitations of this theory. **(12)**

(b) Differentiate between traditional and contemporary organization. **(8)**

(c) Atlas is a computer hardware company. A recent survey revealed that the employees have developed a practices of coming late to work. How can you apply reinforcement theory of motivation to change this behavior? **(7)**

(d) Discuss the elements of the process of delegation. Briefly explain the principles of delegation of authority. **(8)**

8. (a) A construction project is broken down into the following 10 activities: **(15)**

Activity	Immediate Predecessor	Time (weeks)
1	----	4
2	1	2
3	1	4
4	1	3
5	2, 3	5
6	3	6
7	4	2
8	5	3
9	6, 7	5
10	8, 9	7

Answer the following questions:

i. Draw the network diagram.

ii. Find the critical path.

(b) Some tasks and the order in which they must be performed according to their assembly requirement are shown in the following table. These are to be combined into workstations to create an assembly line. The assembly line operates 7 $\frac{1}{2}$ hours per day. The output requirement is 1,000 units per day. **(20)**

Contd P/5

IPE 493/EEE

Contd... Q. No. 8(b)

Task	Preceding Tasks	Time (Seconds)
A	---	15
B	A	24
C	A	6
D	B	12
E	B	18
F	C	7
G	C	11
H	D	9
I	E	14
J	F, G	7
K	H, I	15
L	J, K	10

Answer the following questions:

i. What is the workstation cycle time required to produce 1,000 units per day?

ii. Balance the line using the longest task time based on the 1,000-unit forecast, stating which tasks would be done in each workstation.

iii. What is the efficiency of the line?
