ANALYTICAL MODELING OF THRESHOLD VOLTAGE AND DRAIN CURRENT OF GATE AND CHANNEL ENGINEERED DOUBLE GATE MOSFET

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MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

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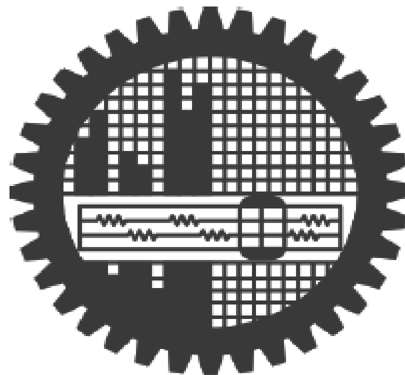

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

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DECLARATION

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

(Md. Arafat Mahmud)

DEDICATION

I would like to dedicate this work to my parents who have always been caring and supportive to me.

APPROVAL CERTIFICATE

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LIST OF SYMBOLS

Symbol	Meaning
Φ_{m1}, Φ_{m2} and Φ_{m3}	Work functions of the three materials in the gate electrode
L	Channel length
L_1, L_2, L_3, L_4 and L_5	Length of the five channel regions 1,2,3,4 and 5
t_{eff}	Effective oxide thickness
t_{sio2}	SiO_2 layer thickness
t_{Hfo2}	HfO_2 layer thickness
$\in_{sio2}$	Permittivity of SiO_2
$\in_{Hfo2}$	Permittivity of HfO_2
N_{Am}	Halo doping concentration near drain and source region
N_{As}	Substrate doping concentration
N_{eff}	Average doping concentration for uniform doping concentration profile
$N_{eff, linear}$	Average doping concentration for linear doping concentration profile
$N_{eff, gaussian}$	Average doping concentration for gaussian doping concentration profile
C_1	Outer fringing capacitance component on each side of front and back gate between gate and source or gate and drain elect
C_2	Direct overlap capacitance between gate and source or gate and drain junction

C_3	Inner fringing capacitance between gate and source side junction or gate and drain side junction
C_F	Maximum value of inner fringing capacitance
t_{gate}	Gate electrode thickness
W	Channel width
α	Slanting angle
X_j	Source/drain junction depth
Q_{DF}	Charge induced at drain end at each side of the front and back gate due to inner fringing capacitance
Q_{SF}	Charge induced at source end at each side of the front and back gate due to inner fringing capacitance
$V_{DS,eff}$	Effective drain to source voltage
V_{fb}	Flat band voltage
V_{th}	Threshold voltage
φ_F	Fermi potential
V_T	Thermal voltage
n_i	Intrinsic carrier concentration
V_{FD}	Fringing potential at drain end
V_{FS}	Fringing potential at source end
Ψ	Channel potential
χ_{si}	Electron affinity of Si
$E_{g_{si}}$	Energy band gap of Si

q	Electron charge
Q_0	Effective surface charge
V_{bi}	Built-in potential
N_{DS}	Doping concentration at drain and source region
t_{si}	Silicon channel thickness
λ	Characteristic length
Ψ_c	Mid-channel potential
Ψ_S	Surface potential
$\Psi_{s,min}$	Minimum surface potential
r_{oc}	Ratio of gate oxide capacitance to channel capacitance
V_{thL}	Long channel threshold voltage
μ	Electron mobility
Q_I	Inversion layer charge
I_{DRIFT}	Drift current component in drain to source current
I_{DIFF}	Diffusion currentcomponent in drain to source current
μ_0	Low carrier mobility
E_c	Critical electric field
Q_s	Surface charge
Q_D	Depletion layer charge
T	Temperature

$I_{DS,tot}$	Drain to source current without CLM effect
$I_{DS,CLM}$	Drain to source current with CLM effect
V_{DP}	Pinch-off voltage
V_A	Early voltage
$V_{roll\text{-}off}$	Threshold voltage roll-off

LIST OF ABBREVIATIONS

Abbreviation	Full Form
SCE	Short Channel Effect
HCE	Hot Carrier Effect
DIBL	Drain Induced Barrier Lowering
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOI MOSFET	Silicon on Insulator MOSFET
SON MOSFET	Silicon on Nothing MOSFET
SM MOSFET	Single Material MOSFET
DM MOSFET	Double Material MOSFET
TM MOSFET	Triple Material MOSFET
SG MOSFET	Single Gate MOSFET
DG MOSFET	Double Gate MOSFET
TM-DG MOSFET	Triple Material Double Gate MOSFET
SM-DG MOSFET	Single Material Double Gate MOSFET
TM-DG-DH-GS MOSFET	Triple Material Double Gate Double Halo Gate Stack MOSFET
EOT	Effective Oxide Thickness
CLM	Channel Length Modulation

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ABSTRACT

Advancement of technology exerts enormous pressure on scaling of devices with a view of improved performance. The scaling of device technology faces significant challenges to control the short channel effects (SCE) and limits the further shrinkage of device size. A number of new architectures have been reported to mitigate these effects. Double gate MOSFET is a promising candidate because of its SCE handling capability. The gate electrodes with more than one material with the different work functions have better control over SCEs. In a Triple Material Double Gate MOSFET, both gate electrodes are composed of three different materials which screen the effect of drain on the source-channel barrier and suppress DIBL (Drain Induced Barrier Lowering). In device of sub-100 nm regime, charge sharing and DIBL effect become very severe. To overcome this issue, halo doping is used i.e., substrate doping is increased selectively near the depletion region. To deal with leakage current, inclusion of high k dielectric has been proved effective. The combined advantages of gate and channel engineering techniques can be achieved in symmetric halo doped gate stacked triple material double gate MOSFET. In this work, a two dimensional analytical model of channel potential, threshold voltage and drain to source current of a triple material double gate double halo gate stacked MOSFET has been developed. Two dimensional Poisson's equations with proper boundary conditions have been solved to obtain the channel potential considering parabolic approximation. For accurate modeling of the device, bias dependent inner fringing capacitance and effective surface charge have been considered. Basic drift-diffusion equation has been used to model the drain to source current. Mid-channel potential of the device has been used instead of surface potential in the current modeling considering the fact that the punch-through current is not confined only to the surface in a fully depleted MOSFET. Thus, an expression of pinch-off voltage has been derived for modeling the drain current in saturation region accurately. Channel length modulation effect has also been included in the model which lifts up the positive slope in the current voltage characteristics in the pinch off region of a MOS device in deep submicron level. The device performance has been analyzed with the variation in device parameters, such as channel length,

channel thickness, doping profile etc. Various short channel effects like drain induced barrier lowering, gate leakage, threshold voltage roll-off have also been investigated. This structure shows excellent ability in suppressing various short channel effects. The analytical model of the device will give a deeper insight of the device physics and characteristics. Finally, the proposed model results have been validated against the data obtained from a commercially available numerical device simulator.

CHAPTER ONE

INTRODUCTION

Continuous scaling of device technology originates significant difficulties and challenges to control the short channel effects (SCE) and hinders the further shrinkage of device size. A number of new architectures have been reported to mitigate these effects and improve device performance. Double gate (DG) MOSFET is advantageous over the traditional single gate (SG) structure because of its higher drive current capability and transconductance, lower off-current, better scaling capability, better Drain induced barrier lowering (DIBL) and effective SCE handling capability [1-9] as two gates control the channel from both sides.

Efficient gate as well as channel engineering contributes significantly to minimize various SCEs [5-8]. The gate electrodes with multiple materials with the different work functions can mitigate the effects of SCE. Some studies have dealt with dual material [10]-[14] and triple material [15]-[17] gate MOSFET. In a symmetric tripe material double gate (TM-DG) MOSFET, both the front and back gate electrodes are composed of three materials with different work functions and the material close to the source has the highest work function while that close to drain has the lowest (n-channel MOSFET).It gives a two-step surface potential profile that screens the effect of drain on the source-channel barrier and suppresses DIBL effectively. This gate engineering also allows to have the same threshold voltage for the device with a reduced doping concentration in the channel region resulting in better immunity against mobility degradation and hence higher transconductance. Some theoretical and experimental works on the TM gates have already been published.

To struggle against leakage associated with continual scaling of gate oxide, inclusion of high k dielectric over the traditional gate oxide (SiO_2) layer has been reported to be beneficial in the literatures [18-19]. The gate stack structure also improves SCEs, DIBL, hot carrier effects and channel length modulation.

In device of sub-100 nm regime, source and drain depletion region tend to approach each other and charge sharing effect becomes very severe. In addition, drain induced barrier lowering effect worsens the situation [20]. Therefore, depletion region width in a short-channel device must be restricted. But increasing substrate doping concentration everywhere is not a suitable solution to this problem, since this will increase the body effect co-efficient. Large value of body effect co-efficient will cause large variation of threshold voltages with change in substrate bias which causes complication in circuit design. To overcome these effects, as a form of channel engineering, double halo doping is used i.e. substrate doping is increased selectively using ion implantation around source and drain region, where depletion region occurs. Triple material double gate double halo gate stacked (TM-DG-DH-GS) MOSFET incorporates the combined advantage of the gate engineering and the channel engineering techniques and is expected to provide further improvement in the performance with enhanced suppression of short channel effects.

1.1 Literature Review

Analytical and simulation works on double gate MOSFET have already been presented in some literatures [1]-[9]. Ernst *et al.* [1] have lifted up the superiority of DG MOSFETs compared to SG MOSFETs in terms of better subthreshold swing and improved transconductance. Quantum calculations have been combined with classical models in it to show the comparison. Suzuki *et al.* [2] have established a scaling theory for DG SOI MOSFET suggesting that a device can be designed with a gate length of less than 0.1 μm while maintaining the ideal subthreshold factor. Lu *et al.* [3] have presented an analytic potential model for long-channel symmetric and asymmetric double-gate MOSFETs. The model is derived rigorously from the exact solution to Poisson's and current continuity equation without the charge-sheet approximation. The resulting analytic expressions of the drain-current, terminal charges, and capacitances for long-channel DG MOSFETs in [3] are continuous in all operation regions, i.e., linear, saturation, and subthreshold, making it suitable for compact modeling. Ieong *et al.* [4] have explored the advantageous flexibility in a DG MOSFET by individual control of the two gates for low-power and mixed-signal applications. Chen *et al.* [5] have presented a compact, physical, short-channel

threshold voltage model for undoped symmetric double-gate MOSFETs based on an analytical solution of the two-dimensional (2-D) Poisson equation with the mobile charge term included. Taur *et al.* [6] and Tsormpatzoglou *et al.* [7] have put efforts on developing analytical model for undoped symmetrical DG MOSFETs, while Cerdeira *et al.* [8] have presented the analytical model for doped symmetrical DG MOSFETs. Young *et al.* [9] have investigated the conduction phenomena in fully depleted SOI DG MOSFET.

The advantages associated with gate engineering in the form of using multiple materials in the gate electrode in dealing with SCEs have been reported in some previous research works [10]-[17]. Among these works, some works [10]-[14] have dealt with dual material (DM) MOSFETs while the rest of them had their focus on triple material (TM) MOSFETs. Reddy *et al.* [10] have presented the analytical modeling of an asymmetrical DM-DG SOI MOSFET and it has been shown that SCEs in this structure are suppressed because of the perceivable step in the surface-potential profile, which screens the drain potential. It has been further demonstrated that the DM-DG structure provides a simultaneous increase in the transconductance and a decrease in the drain conductance when compared with the DG structure. Sarkhel *et al.* [11] have lifted up the enhancement in the device scalability in a DM-DG SON MOSFET compared to a SM-DG SON MOSFET by means of the threshold control with multiple material electrode. Pal *et al.* [12] and Li *et al.* [13] have reported the role of double material in suppressing SCEs in a surrounding gate DM MOSFET. Sarker *et al.* [14] have developed an analytical subthreshold surface potential model of asymmetric pocket-implanted Double-Halo DM-SG-DH and DM-SG-SH MOSFET. The model is derived using the pseudo-2D analysis by applying the Gauss's law to an elementary rectangular box in the channel depletion region, considering the surface potential variation with the channel depletion layer depth. The asymmetric pocket-implanted model in this work takes into account the effective doping concentration of the two linear pocket profiles at the source and the drain ends. The inner fringing field capacitances are also considered in the model for accurate estimation of the subthreshold surface potential at the two ends of the MOSFET. Dhanaselvama *et al.* [15] presented a simulation based work on TM-DG MOSFET

and showed the improvement of SCEs such as DIBL, HCE and CLM effects compared to DM-DG MOSFET and Conventional DG MOSFET.

Razavi *et al.* [16] have developed an analytical model for the threshold voltage of fully depleted short-channel TM-DG MOSFET. In this work, lightly doped channel has been taken to enhance the device performance in terms of higher carrier mobility and minimum dopant fluctuation. The improved hot carrier effects over the double-material DG MOSFETs have been demonstrated. Different length ratios of three channel regions related to different gate materials have been optimized to minimize SCEs. However, it has not considered the inclusion of High-k dielectric for minimizing leakage current or halo doped channel for improved performance against DIBL. Besides, drain to source current model for the device structure has also not been developed in the work. Another limitation of the modeling of Razavi *et al.* [16] is that it has not considered effective surface charge and bias dependent fringing phenomena in its modeling which can give more accurate expression of surface potential. Similarly, Tiwari *et al.* [17] have dealt with analytical modeling of a TM-MOSFET, but they had their focus on surrounding gate structures and it has been demonstrated that notable enhancement in device performance against SCE is observed with their proposed device structure.

The benefit of using a gate stack MOSFET architecture to deal with leakage associated with downscaling of device has been reported in some of the earlier works [18]-[19]. Inani *et al.* [18] have discussed on the practical implications of the high-k dielectric materials on the device performance of a deep submicron MOSFET. Cheng *et al.* [19] have presented the potential impact of high-κ gate dielectrics on device short-channel performance over a wide range of dielectric permittivities using a two-dimensional (2-D) simulator implemented with quantum mechanical models. It is shown in this work that the short-channel performance degradation is caused by the fringing fields from the gate to the source/drain regions which weaken the gate control. The gate stack architecture plays an important role in the determination of the device short-channel performance degradation. It is also presented in this work that using double-layer

gate stack structures and low-κ dielectric as spacer materials well confine the electric fields within the channel thereby minimizing short-channel performance degradation.

Tsividis [20] lifted up the charge sharing effect severely present in a short channel MOSFET and discusses in details on halo doping process as a form of channel engineering to mitigate the very effect.

Pradhan *et al.* [21] have presented a simulation based work on TM-DG-DH-GS MOSFET, but has not presented any analytical modeling of the device structure. As such, it provides very limited insight of the device physics and phenomena; However, it unleashes the promises of the device structure in dealing with SCE to some extent.

Bentrcia *et al.* [22] have studied the influence of hot-carrier degradation effects on the drain current of a DG-GS MOSFET device. The literature has used the idea of EOT (Effective Oxide Thickness) for modeling drain to source current. De et al. [23] have presented an quasi-Fermi potential based analytical subthreshold drain current model for linear and Gaussian doping profile based DHDMG MOSFET. Park *et al.* [24] have presented a charge sheet capacitance model for MOSFET. The bias dependent inner fringing phenomena have been included in this work. Young *et al.* [25] have dealt with the SCEs in a fully depleted SOI MOSFET and proposes the channel potential of such a MOSFET can be approximated by a 2nd order polynomial. The concept has been adopted in this work for modeling of channel potential and threshold voltage.

Yan *et al.* [26] explore an important fact regarding the calculation of characteristics length of a MOSFET. Characteristic length indicates how much electric field from drain region is penetrated into channel and hence how much it is controlled by drain. It has been reported at Yan *et al.* [26] that solving Poisson's equation at semiconductor-oxide interface does not give reasonable value of characteristic length and so cannot measure SCEs properly. Rather, solving Poisson's equation at mid-channel provides a better value of the parameter. This idea has been incorporated in this work.

Arora [27] indicates to the fact that for a fully-depleted DG MOSFET, the punch-through current is not confined only to surface. So, it is suggested in the work that the center potential should be considered instead of surface potential in drain to source current modeling for accurate values. Sodini *et al.* [28] and Akers *et al.* [29] have dealt with developing analytical expressions for low carrier mobility, electric field, critical electric field, surface charge and depletion layer charge of a fully depleted DG MOSFET. Merckel [30] has worked on CAD models of MOSFET. An empirical formula has been developed in his work for incorporating the CLM effect in drain to source current model.

Hamid *et al.* [31] and Kumar *et al.* [32] reveal the fact that QMEs (Quantum Mechanical Effects) become negligible for the channel thickness over 5nm. It is also reported that Ballistic transport is observed when the mean free path of the electron is longer than the dimension of the medium through which the electron travels [33]. Sverdrup *et al.* [34] report that it is known that at room temperature, the electron mean free path in heavily doped sample is~1-10 nm. The channel length used in this analytical modeling is 120nm. So, the ballistic transport effect has not been considered in this modeling.

1.2 Objectives of the Work

The Short Channel Effects (SCEs) are ever on the increase along with the advancement of the technology associated with super-shrunken device in deep submicron level for practical applications. Gate and Channel Engineering techniques can be efficiently applied in a downscaled device to mitigate SCEs. The advantages of gate as well as channel engineering technique can combinedly be incorporated in symmetric halo doped gate stacked triple material double gate MOSFET. To the best of our knowledge, no theoretical model of this device has been reported yet. Hence the purpose of the proposed work is to develop an analytical model of the device structure for having a deeper insight of the device physics and characteristics.

In this work, a two dimensional analytical model of channel potential, threshold voltage and drain to source current of a symmetric halo gate stacked triple material double gate MOSFET will be developed. The analytical model results will also be compared simultaneously with the

data from a commercially available numerical device simulator to validate the model. The expression of channel potential and surface potential of the device will be obtained by solving two dimensional Poisson's equations with appropriate boundary conditions with continuum of channel potential and electrical flux along the channel. Bias dependent inner fringing phenomena and oxide trapping phenomena will also be incorporated for better accuracy of the model. With a view of integrating these effects, inner fringing capacitance and effective surface charge will be included. The expression of drain to source current will be derived using basic drift-diffusion equations. Since the punch-through current is not confined only to the surface in a fully depleted MOSFET, center potential of the channel will be used instead of surface potential in the current modeling. Thus, an expression of pinch-off voltage will be deduced for modeling the drain current in saturation region accurately. However, in deep submicron level, the drain to source current actually does not become constant even after the pinch-off occurs. To depict this phenomenon through our modeling, the channel length modulation effect will also be included. The device performance will be examined with the variation in device parameters, such as channel length, channel thickness, doping profile etc. Several short channel effects like drain induced barrier lowering, leakage, threshold voltage roll-off will also be explored and compared with those of other already proposed device structures to point out the areas of improvement achieved through the application of gate and channel engineering in this device.

1.3 Thesis Outline

The thesis is organized as follows-

Chapter One introduces the topic of the thesis. The motivation behind this thesis work is written in this chapter. An outline of the specific objectives of the work is also included. It also lifts up the reviews of the related earlier literatures and how some of the concepts used in those literatures were adopted in our work.

Chapter Two presents the theoretical aspects of gate and channel engineered TM-DG-DS-DH MOSFET which are relevant to the device characteristics and device capability in dealing with

SCEs with continuous downscaling of device. The parameters which should be known to understand thestructure and performance of the device have been explained in this chapter.

Chapter Three explains the device structure and contains the development of the analytical modeling of channel potential, threshold voltage and drain to source current of the TM-DG-DH-GS MOSFET. Two dimensional Poisson's Equation with proper boundary conditions has been solved and basic drift-diffusion equation has been used to derive the mathematical expression of various device parameters and SCEs

Chapter Four lifts up the analysis and graphical representation of the results obtained from the proposed analytical model along with the simulation results extracted from professional 2D device simulator for model verification. Significant improvements in dealing with SCEs attained with TM-DG-DH-GS MOSFET compared to other device structures with no gate and channel engineering implemented in those, have also been presented in this chapter.

Chapter Five briefly summarizes the overall research work and suggests the scope of future work.

CHAPTER TWO

THEORETICAL BACKGROUND

Practical applications demand ever decreasing chip sizes, which leads to reduced length of the channel in MOS devices. However, as the channel length, L is reduced to increase both the operation speed and the number of components per chip, the short-channel effects arise. Short-channel effect is an effect whereby a MOSFET in which the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction, behaves differently from other MOSFETs. The threshold voltage is modified due to the shortening of channel length. Some of the common SCEs are : Drain Induced Barrier Lowering (DIBL), Hot Carrier Effect (HCE), Threshold Voltage Roll-off and Channel Length Modulation (CLM) Effect etc.

2.1 Drain Induced Barrier Lowering (DIBL) :

Drain-induced barrier lowering is a short-channel effect in MOSFETs refers originally to a reduction of threshold voltage of the transistor at higher drain voltages. In a classic planar field-effect transistor with long channel length, the bottleneck in channel formation occurs far enough from the drain contact and it is electrostatically shielded from the drain by the combination of the substrate and gate. Hence classically the threshold voltage of the long channel transistor is independent of drain voltage. In short-channel devices this phenomena is no longer true. The drain is close enough to gate the channel, and so a high drain voltage can open the bottleneck and turn on the transistor prematurely [20].

Normally, the combined charge in the depletion region of the device and that in the channel of the device are balanced by three electrode charges: the gate, the source and the drain. As drain voltage is increased, the depletion region of the p-n junction between the drain and body increases in size and extends under the gate, so the drain assumes a greater portion of the burden of balancing depletion region charge, leaving a smaller burden for the gate. As a result, the charge present on the gate retains charge balance by attracting more carriers into the channel, equivalent to lowering the threshold voltage of the device. In effect, the channel becomes more

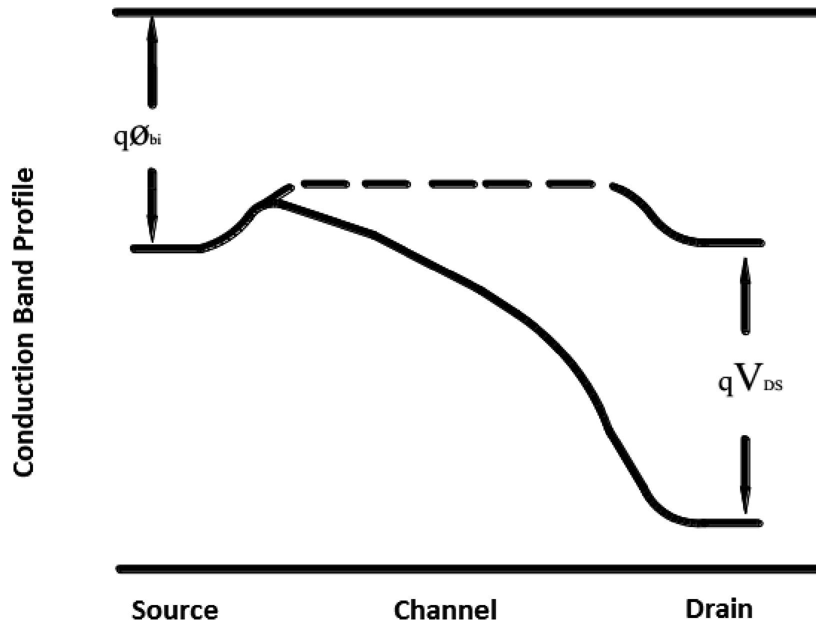


Fig. 2.1 Drain Induced Barrier Lowering phenomena in Short Channel MOSFET [20]

attractive for electrons. In other words, the potential energy barrier for electrons in the channel is lowered. Hence the term "barrier lowering" is used to describe these phenomena. Fig. 2.1 illustrates the DIBL effect with the conduction band profile in a short channel MOSFET. As the drain bias increases, fields emanating from the drain end up throughout the channel and the surface potential is raised. The electrons now find it easier to cross the barrier and their population in the channel increases. As a result, the threshold voltage is decreased and becomes a strong function of drain voltage in short channel device.

2.2 Hot Carrier Effect (HCE) :

Hot Carrier Effect is a phenomenon in solid-state electronic devices where an electron generated in the space charge region is attracted due to the electric field induced by a positive gate voltage and gains sufficient kinetic energy to overcome a potential barrier necessary to break an interface state. The term "hot" refers to the effective temperature used to model carrier density, not to the overall temperature of the device. Since the charge carriers can become trapped in the gate

dielectric of a MOS transistor, the switching characteristics of the transistor can be permanently changed. Hot-carrier injection is one of the mechanisms that adversely affects the reliability of semiconductors in solid-state devices [32].

2.3 Threshold Voltage Roll-off :

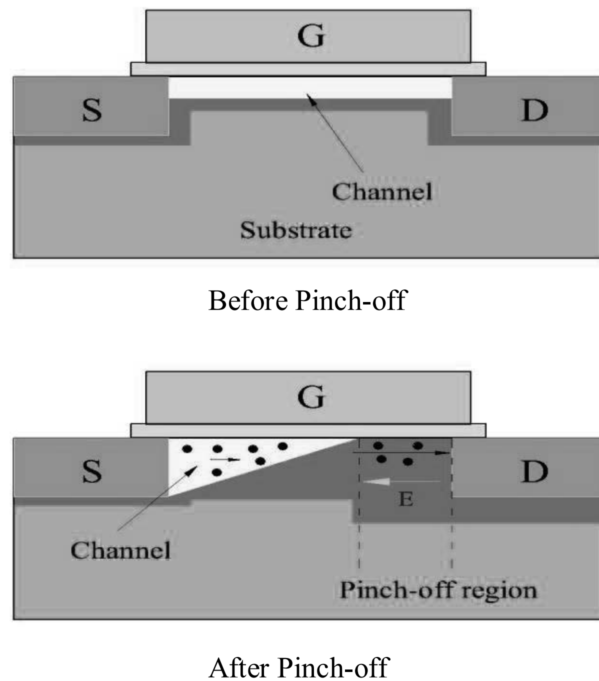
The decrease of threshold voltage with decrease in gate length is a well-known short channel effect called the "Threshold voltage roll-off". As the channel of the device is reduced to nanoscale region, the charge distribution in the channel is influenced by the field originating from the source/drain. Thus the value of threshold voltage in a short channel device decreases from the constant value maintained in a long channel device. Mathematically, threshold voltage roll-off is the difference between the threshold voltage of a short channel MOSFET and that of a long channel MOSFET.

2.4 Channel Length Modulation (CLM) Effect :

Channel Length Modulation (CLM) is a shortening of the length of the inverted channel region with increase in drain bias for large drain voltage. The result of CLM is an increase in current with drain bias and a reduction of output resistance.

CLM effect is closely associated with pinch-off phenomena in the MOS Device. The channel in a MOS device is formed by attraction of carriers to the gate, and the current drawn through the channel is nearly a constant, independent of drain voltage in saturation mode. However, near the drain, the gate and drain jointly determine the electric field pattern. Instead of flowing in a channel, beyond the pinch-off point the carriers flow in a subsurface pattern made possible because the drain and the gate both control the current. The channel becomes weaker as the drain is approached, leaving a gap of uninverted silicon between the end of the formed inversion layer and the drain (the pinch-off region) [20].

As the drain voltage increases, its control over current toward the source extends further and hence the uninverted region expands toward the source, shorten the length of the channel region.



Before Pinch-off

After Pinch-off

Fig. 2.2 Channel Length Modulation (CLM) Effect in MOSFET device

This effect is termed as channel-length modulation. Fig. 2.2 shows the channel-length modulation phenomena in a MOS device. Before the pinch-off phenomenon occurs, the channel is extended to the drain end. However, once the pinch-off occurs, the channel length is decreased towards the source. Since resistance is proportional to length, shortening the channel length decreases its resistance, causes an increase in current with increase in drain bias for a MOSFET operating in saturation. The effect is more pronounced with shorter source-to-drain separation, deeper drain junction, and thicker oxide insulator [20].

2.5 Gate Engineering:

Gate Engineering is applied to mitigate SCEs in a MOSFET device. One form of Gate Engineering is to use metals having different work functions in the gate electrode with the one close to source having the highest work function and the lowest work function material being adjacent to the drain. Since, the work function of the metal close to drain is the highest of the all, the minimum surface potential will be found in the channel region under that metal. So, the energy barrier level will be the highest in this region. The channel will not conduct until this highest barrier is lowered irrespective of drain bias applied. Threshold voltage condition of the device is thus effectively screened from drain bias and the Drain Induced Barrier Lowering (DIBL) effect will be less.

Another form of Gate Engineering is the inclusion of High-k dielectric material along with the conventional SiO_2 as gate oxide layer. With the continuous downscaling of the device, leakage current is ever on the increase. Including the High-k dielectric material in the gate oxide decreases leakage current effectively.

2.6 Channel Engineering:

Channel Engineering is applied in a MOSFET device in the form of Halo Doping. In the short channel MOSFET, the depletion regions associated with the source and the drain come into close proximity/contact with each other. It affects the device current-voltage characteristics adversely. The slope of $\log\left(I_{DS}\right)$ vs V_{GS} becomes very small and the device cannot be turned off adequately even if V_{DS} is decreased significantly [20]. This is called Punch through effect. For avoiding the phenomena, depletion region width must be limited. Using higher substrate doping can limit depletion region width, but it is not desirable to increase the substrate doping concentration everywhere in the channel, as it will increase the body effect co-efficient which will impede the optimum device performance in many applications. So, the substrate doping concentration is increased locally, around the source or drain or both region using ion implantation. This processis called Halo doping. If the halo implantation is done around both source and drain regions, it is called Double Halo doping and if it is done around any of the two regions, it is

called Single Halo doping. The length of the halo regions is assumed to be fixed, independent of the channel length.

2.7 Effective Oxide Thickness (EOT):

Effective oxide thickness is a number used to compare performance of high-k dielectric MOSFET gates with performance of SiO_2 based MOSFET gates [22]. It shows the thickness of SiO_2 gate oxide needed to obtain the same gate capacitance as the one obtained with thicker than SiO_2 dielectric featuring higher dielectric constant, K. For example, EOT of 1 nm would result from the use a 10 nm thick dielectric featuring k=39 (k of SiO_2 is 3.9). Mathematically, EOT can be represented as :

$$EOT = t_{sio2} + \frac{t_{High,k} \times \in_{sio2}}{\in_{High,k}}$$

Where, t_{sio2}, $t_{High,k}$, $\in_{sio2}$ and $\in_{High,k}$ denote SiO_2 and high-k dielectric layer thickness, permittivity of SiO_2 and high-k dielectric respectively.

CHAPTER THREE

ANALYTICAL MODELING OF PROPOSED DEVICE

3.1 Physical Device Structure and Dimensions:

A schematic structure of the proposed device is shown in Fig. 3.1. The x- and y- axes of the 2D device structure are considered to be along the front oxide-semiconductor interface and the source terminal-channel interface, respectively.The total channel length, L is divided into 5 regions. L_1 and L_5 ($L_1 = L_5$) denote the length of the regions with uniform halo doping near source and drain end, correspondingly. Doping concentration used in these regions is $N_{Am}=1.2x10^{18}$ cm^{-3}. Elsewhere in the channel, the doping concentration is $N_{As} = 10^{15}$ cm^{-3}. The doping concentration of drain and source region is $N_{DS}=10^{20}$ cm^{-3}. The front and the back gate electrodes of the device are symmetric and composed of three different materials having work functions of Φ_{m1}, Φ_{m2} and Φ_{m3} ($\Phi_{m1} > \Phi_{m2} > \Phi_{m3}$) deposited over lengths (L_1+L_2),L_3 and(L_4+L_5) respectively. The front and the back gate terminals are shorted to a fixed potential, V_{GS}. The drain bias is V_{DS} and the source terminal is grounded. Two layers of oxides have been used with both front and back gate terminals. The first layer of the oxide is HfO_2 having high dielectric constant, k_{HfO2} of 25 and the lower layer is SiO_2. So, the effective oxide thickness with equivalent permittivity of SiO_2 is given by $t_{eff} = t_{sio2} + \frac{t_{Hfo2} \times \in_{sio2}}{\in_{Hfo2}}$ [22], where, t_{sio2} , t_{Hfo2} , $\in_{sio2}$ and $\in_{Hfo2}$ denote SiO_2 and HfO_2 layer thickness, permittivity of SiO_2 and HfO_2 respectively.

3.2 Doping Concentration Profile:

Plot of doping profile along the channel is presented in Fig. 3.2. Doping concentration along the channel can be expressed as:

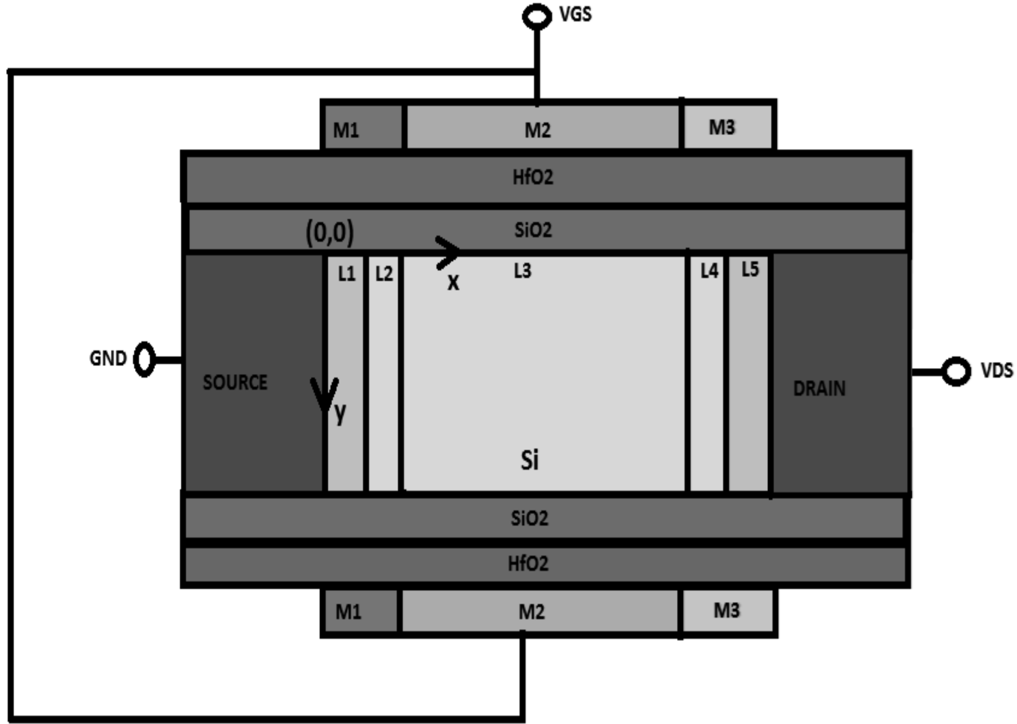


Fig. 3.1 Schematic cross sectional view of triple material double gate double halo gate stacked MOSFET

$$N(x) = \begin{cases} N_{Am}, 0 < x \le L_1 \\ N_{As}, L_1 < x \le (L - L_5) \\ N_{Am}, (L - L_5) < x \le L \end{cases} \tag{1}$$

Here, the halo doping concentration, N_{Am} has been used uniformly in the region L_1 and L_5. So, it has been named as uniform halo doping concentration profile. Since, there is a non-uniform doping profile along the channel; the average effective concentration [14] as well as local doping concentration have been considered in the analytical modeling for mathematical simplicity. The average effective doping concentration for the uniform halo doping concentration profile can be found by:

$$N_{eff} = N_{As} + \frac{2L_1\left(N_{Am} - N_{As}\right)}{L} \tag{2}$$

Unless otherwise stated, the abovementioned uniform halo doping profile has been used for result analysis in the work. We have also studied linear [14] and Gaussian [23] halo doping concentration profile in the work. For linear and Gaussian halo doping profile, the average effective doping concentration along the channel can be found by the following equations respectively:

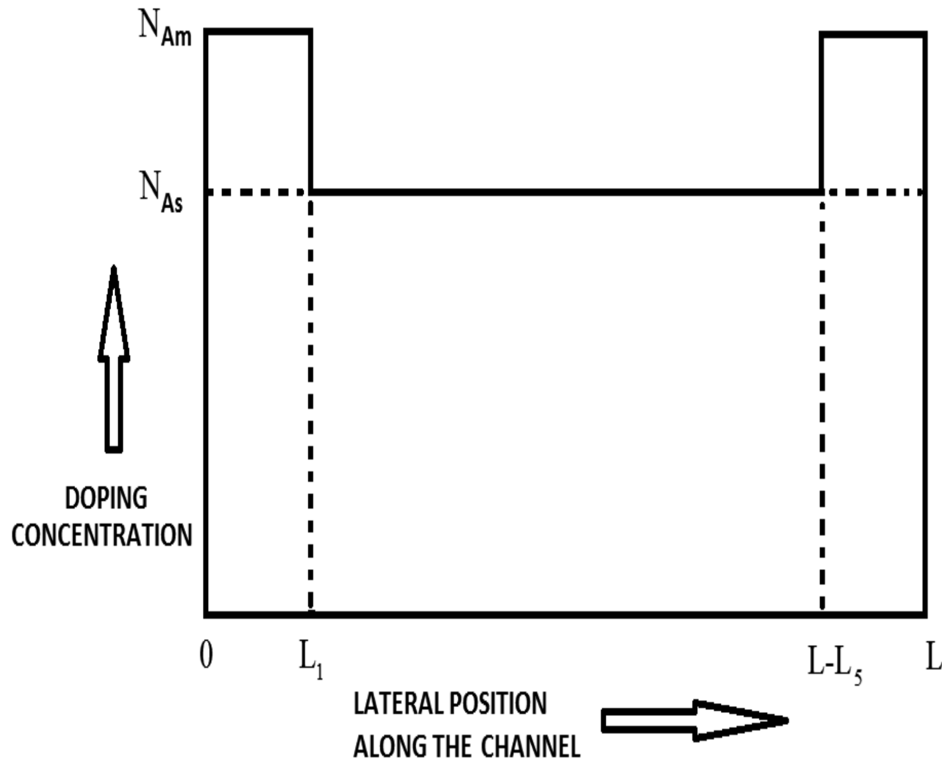


Fig. 3.2 Plot of doping concentration along the lateral position of the channel

$$N_{\text{eff, linear}} = N_{As} + \frac{L_1 \left(N_{Am} - N_{As} \right)}{L} \tag{3}$$

$$N_{\text{eff, gaussian}} = N_{As} + N_{Am} \left\{ \frac{\sqrt{\pi}\ \text{erf}\left(\frac{L}{L_1} \right)}{\left(\frac{L}{L_1} \right)} \right\} \tag{4}$$

3.3 Fringing Phenomena in Device:

The bias dependent inner fringing phenomena in the device have been considered in our model. All the fringing and the overlap capacitance components in the device have been shown in Fig. 3.3. C_1 is the outer fringing capacitance component on each side of front and back gate between gate and source or gate and drain electrode. C_2 is the direct overlap capacitance between gate and source or gate and drain junction. C_3 is the inner fringing capacitance between gate and source

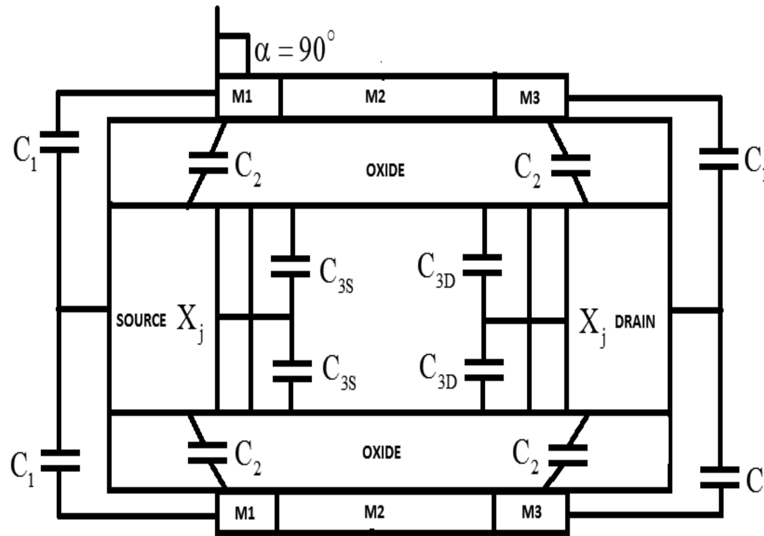


Fig. 3.3 Outer, inner and overlap fringing capacitance components

side junction or gate and drain side junction. C_F is the maximum value of inner fringing capacitance, C_3. The capacitors are modeled as:

$$C_1 = W\frac{\epsilon_{sio2}}{\alpha}\ln\left(1+\frac{t_{gate}}{t_{eff}}\right) \tag{3}$$

$$C_2 = W\frac{\epsilon_{sio2}}{t_{eff}}\left[0.5t_{eff}\left(\frac{1-\cos\alpha}{\sin\alpha}+\frac{1-\cos\delta}{\sin\delta}\right)\right] \tag{4}$$

$$C_F = W\frac{\epsilon_{sio2}}{\delta}\ln\left(1+\frac{X_j\sin\alpha}{t_{eff}}\right) \tag{5}$$

where $\delta = 0.5\pi\frac{\epsilon_{sio2}}{\epsilon_{si}}$ and t_{gate}, W, α and X_j are gate electrode thickness, channel width, slanting angle and source/drain junction depth, respectively.

The charge induced at drain and source end at each side of the front and back gate due to inner fringing capacitance are,

$$Q_{DF} = -C_F\frac{V_{DS}-V_{DS,eff}}{1+e^{-\frac{V_{GS}-V_{fb}}{30V_T}}} = -C_F V_{FD} \tag{6}$$

$$Q_{SF} = -C_F\frac{V_{th}+V_{fb}+2\varphi_F+\gamma\sqrt{2\varphi_F-V_{GS}}}{1+e^{-\frac{V_{GS}-V_{fb}}{30V_T}}} = -C_F V_{FS} \tag{7}$$

where, V_{fb} is flat band voltage, V_{th} is threshold voltage, $\varphi_F = V_T\ln\left(\frac{N_{eff}}{n_i}\right)$ is Fermi potential, n_i is intrinsic carrier concentration, $\gamma = \frac{\sqrt{2q\epsilon_{si}N_{eff}}}{C_{ox}}$ is body effect coefficient, V_T is thermal voltage and $C_{ox} = \frac{\epsilon_{sio2}}{t_{eff}}$ is oxide capacitance. The effective drain to source voltage, $V_{DS,eff}$ is given by Park et al. [24]. V_{FD} and V_{FS} are inner fringing potential at drain and source end, respectively.

3.4 Channel Potential :

Let $\Psi_j(x,y)$; j=1, 2,3,4,5 be the channel potential in the channel region 1, 2, 3, 4 and 5 respectively. We solve the two dimensional Poisson's equation to obtain the channel potential, $\Psi_j(x,y)$:

$$\frac{\partial^2\Psi_j(x,y)}{\partial x^2}+\frac{\partial^2\Psi_j(x,y)}{\partial y^2}=\frac{qN_{eff}}{\epsilon_{si}} \tag{8}$$

To solve the equation the boundary conditions of potential and electrical flux continuity at different interfaces are required. At front and back semiconductor-oxide interfaces, boundary conditions are given by:

$$\frac{\partial\Psi_j(x,y)}{\partial y}\Big|_{y=0}=\frac{\epsilon_{sio2}\left[\Psi_{sj}(x)-V_{GS}+V_{fbj}\right]}{\epsilon_{si}\ t_{eff}} \tag{9}$$

$$\frac{\partial\Psi_j(x,y)}{\partial y}\Big|_{y=t_{si}}=-\frac{\epsilon_{sio2}\left[\Psi_{sj}(x)-V_{GS}+V_{fbj}\right]}{\epsilon_{si}\ t_{eff}} \tag{10}$$

where, t_{si} is the channel thickness and V_{fbj} corresponds the flat band voltage of region 1,2,3,4 and 5 and is given by the expression :

$$V_{fbj}=\varphi_{mj}-\left[\chi_{si}+\frac{E_{g_{si}}}{2q}+\varphi_F\right]-\frac{Q_0}{C_{ox}};j=1,2,3,4,5 \tag{11}$$

here, $\chi_{si}, E_{g_{si}}, \varphi_F$ and Q_0 are electron affinity ,energy band gap of silicon, Fermi potential and effective surface charge, respectively. The value of effective surface charge, Q_0 is $1.6\text{x}10^{-8}$ C/m^2 .

Due to the continuous behavior of potential and electrical flux throughout the channel, potential and electrical flux are continuous functions, hence at the interface of region 1 and 2, region 2 and 3, region 3 and 4 and region 4 and 5 we get,

$$\Psi_1(L_1,0)=\Psi_2(L_1,0) \tag{12}$$

$$\frac{\partial \Psi_1}{\partial x}\Big|_{x=L_1} = \frac{\partial \Psi_2}{\partial x}\Big|_{x=L_1} \quad (13)$$

$$\Psi_2(L_1+L_2,0) = \Psi_3(L_1+L_2,0) \quad (14)$$

$$\frac{\partial \Psi_2}{\partial x}\Big|_{x=L_1+L_2} = \frac{\partial \Psi_3}{\partial x}\Big|_{x=L_1+L_2} \quad (15)$$

$$\Psi_3(L_1+L_2+L_3,0) = \Psi_4(L_1+L_2+L_3,0) \quad (16)$$

$$\frac{\partial \Psi_3}{\partial x}\Big|_{x=L_1+L_2+L_3} = \frac{\partial \Psi_4}{\partial x}\Big|_{x=L_1+L_2+L_3} \quad (17)$$

$$\Psi_4(L_1+L_2+L_3+L_4,0) = \Psi_5(L_1+L_2+L_3+L_4,0) \quad (18)$$

$$\frac{\partial \Psi_4}{\partial x}\Big|_{x=L_1+L_2+L_3+L_4} = \frac{\partial \Psi_5}{\partial x}\Big|_{x=L_1+L_2+L_3+L_4} \quad (19)$$

Potentials at source-channel and drain channel interface can be expressed as,

$$\Psi_1(0,0) = V_{bi} + V_{FS} \quad (20)$$

$$\Psi_5(L_1+L_2+L_3+L_4+L_5,0) = V_{bi} + V_{DS} + V_{FD} \quad (21)$$

where, V_{bi} is the built in potential and is given by:

$$V_{bi} = V_T \ln\left(\frac{N_{Am}N_{DS}}{n_i^{2}}\right) \quad (22)$$

here, N_{DS} is the doping concentration at drain and source region. From [25], the solution of Eq. (8) can be approximated by a 2nd order polynomial:

$$\Psi_j(x,y) = c_{j0}(x) + c_{j1}(x)y + c_{j2}(x)y^2,\ j=1,2,3,4,5 \quad (23)$$

where, $c_{j0}(x)$, $c_{j1}(x)$ and $c_{j2}(x)$ are arbitrary functions of x which can be solved using boundary conditions of Eqs. (9)-(21). Substituting y=0 in Eq. (23) we get

$$c_{j0}(x) = \Psi_j(x,0) = \Psi_{sj}(x) \quad (24)$$

Taking derivative of Eq. (23) and using Eqs. (9) and (10) we get,

$$c_{j1}(x) = \frac{\epsilon_{sio2}\left[\Psi_{sj}(x) - V_{GS} + V_{fbj}\right]}{\epsilon_{si}\ t_{eff}} \quad (25)$$

$$c_{j2}(x) = -\frac{\epsilon_{sio2}\left[\Psi_{sj}(x) - V_{GS} + V_{fbj}\right]}{\epsilon_{si}\ t_{eff} t_{si}} \tag{26}$$

So, Eq. (25) becomes,

$$\Psi_j(x,y) = \Psi_{sj}(x) + \frac{\epsilon_{sio2}\left[\Psi_{sj}(x) - V_{GS} + V_{fbj}\right]}{\epsilon_{si}\ t_{eff}} y - \frac{\epsilon_{sio2}\left[\Psi_{sj}(x) - V_{GS} + V_{fbj}\right]}{\epsilon_{si}\ t_{eff} t_{si}} y^2 \tag{27}$$

For more accurate modeling of channel potential we need to consider characteristic length, λ. It indicates how much electric field from drain region is penetrated into channel and hence how much it is controlled by drain.

But solving Poisson's equation at semiconductor-oxide interface does not give reasonable value of λ and so cannot measure short channel effects properly [26]. Rather, solving Poisson's equation at mid-channel provides a better value of λ [26] and λ is expressed as:

$$\lambda = \sqrt{\frac{t_{si}^{2}\left(1 + \frac{r_{oc}}{4}\right)}{2r_{oc}}}$$

Now, the mid-channel potential:

$$\Psi_{cj}(x) = \Psi_j(x,y)\Big|_{y=\frac{t_{si}}{2}} \tag{28}$$

From Eqs. (25)-(27),

$$\Psi_{cj}(x) = \Psi_{sj}(x)\left(1 + \frac{r_{oc}}{4}\right) - \frac{r_{oc}}{4}\left(V_{GS} - V_{fbj}\right) \tag{29}$$

here, r_{oc} is the ratio of gate oxide capacitance to channel capacitance and is given by:

$$r_{oc} = \frac{\epsilon_{sio2}\ t_{si}}{\epsilon_{si}\ t_{eff}}$$

Differential equation for solving Eq. (8) at mid-channel:

$$\frac{\partial^2 \Psi_{cj}(x)}{\partial x^2} - \frac{\Psi_{cj}(x)}{\lambda^2} = \frac{qN_{eff}}{\epsilon_{si}} - \left(\frac{V_{GS} - V_{fbj}}{\lambda^2}\right) \tag{30}$$

General solution for Eq. (30) can be written as

$$\Psi_{cj}(x) = G_j e^{\tau x} + H_j e^{-\tau x} - \frac{\alpha_j}{\tau^2} \tag{31}$$

where,

$$\alpha_j = \frac{qN_{eff}}{\epsilon_{si}} - \left(\frac{V_{GS}\text{-}V_{fbj}}{\lambda^2}\right) \tag{32}$$

$$\tau = \frac{1}{\lambda} \tag{33}$$

The coefficients G_j and H_j (j=1,2,3,4,5) can be found using boundary conditions of Eqs. (9)-(21). Solving, we get,

$$G_1 = \frac{1}{2\sinh(\tau L)}[V_{FD} + V_{bi} + V_{DS} + \frac{\alpha_5}{\tau^2} - \left(V_{bi} + V_{FS} + \frac{\alpha_1}{\tau^2}\right)e^{-\tau L} + \left(\frac{\alpha_1 - \alpha_2}{\tau^2}\right)\cosh\{\tau(L_2 + L_3 + L_4 + L_5)\} + \left(\frac{\alpha_2 - \alpha_3}{\tau^2}\right)\cosh\{\tau(L_3 + L_4 + L_5)\} + \left(\frac{\alpha_3 - \alpha_4}{\tau^2}\right)\cosh\{\tau(L_4 + L_5)\} + \left(\frac{\alpha_4 - \alpha_5}{\tau^2}\right)\cosh(\tau L_5)] \tag{34}$$

$$G_2 = G_1 - \left(\frac{\alpha_1 - \alpha_2}{2\tau^2}\right)e^{-\tau L_1} \tag{35}$$

$$G_3 = G_1 - \left(\frac{\alpha_1 - \alpha_2}{2\tau^2}\right)e^{-\tau L_1} - \left(\frac{\alpha_2 - \alpha_3}{2\tau^2}\right)e^{-\tau(L_1 + L_2)} \tag{36}$$

$$G_4 = G_1 - \left(\frac{\alpha_1 - \alpha_2}{2\tau^2}\right)e^{-\tau L_1} - \left(\frac{\alpha_2 - \alpha_3}{2\tau^2}\right)e^{-\tau(L_1 + L_2)} - \left(\frac{\alpha_3 - \alpha_4}{2\tau^2}\right)e^{-\tau(L_1 + L_2 + L_3)} \tag{37}$$

$$G_5 = G_1 - \left(\frac{\alpha_1 - \alpha_2}{2\tau^2}\right)e^{-\tau L_1} - \left(\frac{\alpha_2 - \alpha_3}{2\tau^2}\right)e^{-\tau(L_1 + L_2)} - \left(\frac{\alpha_3 - \alpha_4}{2\tau^2}\right)e^{-\tau(L_1 + L_2 + L_3)} - \left(\frac{\alpha_4 - \alpha_5}{2\tau^2}\right)e^{-\tau(L_1 + L_2 + L_3 + L_4)} \tag{38}$$

$$H_1 = V_{bi} - G_1 + \frac{\alpha_1}{\tau^2} + V_{FS} \tag{39}$$

$$H_2 = H_1 - \left(\frac{\alpha_1 - \alpha_2}{2\tau^2}\right)e^{\tau L_1} \tag{40}$$

$$H_3 = H_1 - \left(\frac{\alpha_1 - \alpha_2}{2\tau^2}\right)e^{\tau L_1} - \left(\frac{\alpha_2 - \alpha_3}{2\tau^2}\right)e^{\tau(L_1+L_2)} \tag{41}$$

$$H_4 = H_1 - \left(\frac{\alpha_1 - \alpha_2}{2\tau^2}\right)e^{\tau L_1} - \left(\frac{\alpha_2 - \alpha_3}{2\tau^2}\right)e^{\tau(L_1+L_2)} - \left(\frac{\alpha_3 - \alpha_4}{2\tau^2}\right)e^{\tau(L_1+L_2+L_3)} \tag{42}$$

$$H_5 = H_1 - \left(\frac{\alpha_1 - \alpha_2}{2\tau^2}\right)e^{\tau L_1} - \left(\frac{\alpha_2 - \alpha_3}{2\tau^2}\right)e^{\tau(L_1+L_2)} - \left(\frac{\alpha_3 - \alpha_4}{2\tau^2}\right)e^{\tau(L_1+L_2+L_3)} - \left(\frac{\alpha_4 - \alpha_5}{2\tau^2}\right)e^{\tau(L_1+L_2+L_3+L_4)} \tag{43}$$

Using Eqs. (27), (29) and (31) and Eqs. (34)-(43), the channel potential equation is:

$$\Psi_j(x,y) = \left[\frac{G_j e^{\tau x} + H_j e^{-\tau x} - \frac{\alpha_j}{\tau^2} + \frac{r_{oc}}{4}\left(V_{GS}\text{-}V_{fbj}\right)}{\left(1+\frac{r_{oc}}{4}\right)}\right] \times \left(1 + \frac{r_{oc}}{t_{si}}y - \frac{r_{oc}}{t_{si}^2}y^2\right) - \frac{r_{oc}}{t_{si}}\left(V_{GS}\text{-}V_{fbj}\right)y + \frac{r_{oc}}{t_{si}^2}\left(V_{GS}\text{-}V_{fbj}\right)y^2; j = 1,2,3,4,5 \tag{44}$$

Expression of surface potential can be found as :

$$\Psi_{sj}(x) = \frac{G_j e^{\tau x} + H_j e^{-\tau x} - \frac{\alpha_j}{\tau^2} + \frac{r_{oc}}{4}\left(V_{GS}\text{-}V_{fbj}\right)}{\left(1+\frac{r_{oc}}{4}\right)} \tag{45}$$

3.5 Threshold Voltage :

The channel region is under three different material gate electrodes. Since, the work function of metal 1, φ_{m1} is the highest of the three, from Eqs. (14) and (45), the minimum surface potential will be found in the channel region under metal 1. So, the energy barrier level will be the highest in this region [16]. That is why the channel will not conduct until this highest barrier is lowered. Threshold voltage condition of the device is thus dependent on this channel region.

Since, the flatband voltage in region 1 and 2 are same (since they are under same metal),taking derivative of Eq. (45) for region 2 and equating it to zero, we find the channel position x_{min} where, the surface potential is minimum and it is given by :

$$x_{min} = 0.5\lambda \ln \frac{H_2}{G_2} \tag{46}$$

And the minimum surface potential can be found using Eq. (45):

$$\Psi_{s,min} = 2\sqrt{G_2 H_2} - \frac{qN_{eff}}{\epsilon_{si}\ \tau^2} + \left(V_{GS}\text{-}V_{fb2}\right) \tag{47}$$

For threshold condition,

$$\Psi_{s,min} = 2\varphi_F \tag{48}$$

$$V_{GS} = V_{th} \tag{49}$$

usingEqs. (47)-(49), we can write for threshold condition,

$$2\sqrt{G_2{}^{th} H_2{}^{th}} - \frac{qN_{eff}}{\epsilon_{si}\ \tau^2} + \left(V_{th}\text{-}V_{fb2}\right) = 2\varphi_F \tag{50}$$

where, $G_2{}^{th} = G_2$ at $V_{GS} = V_{th}$ and $H_2{}^{th} = H_2$ at $V_{GS} = V_{th}$

Now, using Eq. (50), a quadratic equation of threshold voltage, V_{th} can be approximated as:

$$AV_{th}{}^2 + BV_{th} + C = 0 \tag{51}$$

where,

$$A = 1 + 4\left(U_2 + \sqrt{U_2}\right) - U_7 - U_8 \tag{52}$$

$$B = -2V_{thL} - 4U_1 - U_6 - 2U_5U_7 - U_5U_8 \tag{53}$$

$$C = V_{thL}{}^2 - 4U_3 - U_4 - U_5U_6 - U_5{}^2U_7 \tag{54}$$

$$V_{thL} = \frac{qN_{eff}}{\epsilon_{si}\ \tau^2} + V_{fb2} + 2\varphi_F \tag{55}$$

$$U_1 = \frac{V_1\left(e^{-\tau L} - 1\right)}{2\sinh\left(\tau L\right)} - \frac{V_6\left(e^{-\tau L} - 1\right)}{\sinh\left(\tau L\right)} - V_6 - \frac{V_{FD}{}^{th}\left(e^{-\tau L} - 1\right)}{2\left\{\sinh\left(\tau L\right)\right\}^2} - \frac{V_{FD}{}^{th}}{2\sinh\left(\tau L\right)} \tag{56}$$

$$U_2 = \left\{\frac{\left(e^{-\tau L} - 1\right)}{2\sinh\left(\tau L\right)}\right\}^2 \tag{57}$$

$$U_3 = V_1V_6 - V_6{}^2 \tag{58}$$

$$U_4 = \frac{2V_1 V_{FD}{}^{th}}{\sinh(\tau L)} + 4\left[\left\{\frac{V_{FD}{}^{th}}{2\sinh(\tau L)}\right\}^2 + \frac{V_6 V_{FD}{}^{th}}{\sinh(\tau L)}\right] \tag{59}$$

$$U_5 = V_{fb1} + 2\varphi_F + \gamma\sqrt{2\varphi_F} \tag{60}$$

$$U_6 = \frac{2V_{FD}{}^{th} e^{-\tau L}}{\{\sinh(\tau L)\}^2} - \frac{4V_6 e^{-\tau L}}{\sinh(\tau L)} - \frac{2V_1 e^{-\tau L}}{\sinh(\tau L)} \tag{61}$$

$$U_7 = \left\{\frac{e^{-\tau L}}{\sinh(\tau L)}\right\}^2 \tag{62}$$

$$U_8 = \frac{2e^{-\tau L}\left(e^{-\tau L} - 1\right)}{\{\sinh(\tau L)\}^2} + \frac{2e^{-\tau L}}{\sinh(\tau L)} \tag{63}$$

where, $V_{FD}{}^{th} = V_{FD}$ at $V_{GS} = V_{th}$ and V_{thL} is the long channel threshold voltage which is independent of channel length.

$$V_j = V_{bi} + \frac{qN_{eff}}{\epsilon_{si}\,\tau^2} + V_{fbj}\ ;\ j = 1,2,3,4,5 \tag{64}$$

$$V_6 = \frac{1}{2\sinh(\tau L)}[V_{DS} + V_5 - V_1\ e^{-\tau L} + (V_1 - V_2)\cosh\{\tau(L_2 + L_3 + L_4 + L_5)\}$$
$$+ (V_2 - V_3)\cosh\{\tau(L_3 + L_4 + L_5)\} + (V_3 - V_4)\cosh\{\tau(L_4 + L_5)\} + (V_4 - V_5)\cosh(\tau L_5)] \tag{65}$$

Using Eqs. (51)-(65), the expression of the threshold voltage is given by:

$$V_{th} = \frac{-B + \sqrt{\left(B^2 - 4AC\right)}}{2A} \tag{66}$$

3.6 Drain to Source Current :

For modeling of drain to source current, mid-channel potential has been considered instead of surface potential in basic drift and diffusion current equation, because considering surface potential in this case assumes punch-through current to flow only at surface [2], which is invalid

for double gate fully depleted MOSFET [27]. Thus the inclusion of center potential in current equation provides better result in measuring short channel effects.

Drain to source current can be expressed as a combination of drift and diffusion current [20] for all the regions which can be given as:

$$I_{DRIFT_j} = W \cdot \mu_j(x) \cdot Q_{Ij}(x) \frac{d\Psi_{cj}(x)}{dx} \tag{67}$$

$$I_{DIFF_j} = W \cdot \mu_j(x) \cdot V_T \frac{dQ_{Ij}(x)}{dx} \tag{68}$$

where, $W, V_T, \mu_j(x)$ and $Q_{Ij}(x)$ are channel width, thermal voltage, carrier mobility and inversion layer charge, respectively for j=1,2,3,4,5 and are given by:

$$\mu_j(x) = \frac{\mu_0}{\sqrt{\left[1+\left\{\frac{E_j(x)}{E_c}\right\}^2\right]}} \tag{69}$$

$$Q_{Ij}(x) = 2\left\{Q_{sj}(x) - Q_{Dj}\right\} \tag{70}$$

where, $\mu_0, E_j(x), E_c, Q_{sj}(x)$ and Q_{Dj} are low carrier mobility, electric field, critical electric field, surface charge and depletion layer charge, respectively [28]-[29] and are given by:

$$E_j(x) = \frac{C_{ox}\left[\Psi_{cj}(x) - V_{GS} + V_{fbj}\right]}{\epsilon_{si}} \tag{71}$$

$$E_c = 6.01\times10^2 \cdot T^{\frac{3}{2}} \tag{72}$$

$$Q_{sj}(x) = -C_{ox}\left[V_{GS} - V_{fbj} - \Psi_{cj}(x)\right] \tag{73}$$

$$Q_{Dj} = C_{ox}\left(\varphi_F - V_{th} + V_{fbj}\right) \tag{74}$$

The model has been developed considering constant room temperature (300K) and the value of low carrier mobility, μ_0 at this temperature is 1350 $cm^2/V\text{-}s$.

Now, integrating both sides of the Eq. (67) and using Eqs. (69), (70), (73) and (74),

$$\int_{L^*_{j-1}}^{L^*_j} I_{DRIFT_j} dx = \int_{\Psi_{cj-1}}^{\Psi_{cj}} \frac{W\mu_0 \left[-2C_{ox} \left\{ V_{GS} - \Psi_{cj}(x) + \varphi_F - V_{th} \right\} \right]}{\sqrt{\left[1 + \left\{ \frac{E_j(x)}{E_c} \right\}^2 \right]}} d\Psi_{cj} \tag{75}$$

where,

$$\begin{cases} L^*_0 = 0, \\ L^*_1 = L_1, \\ L^*_2 = L_1 + L_2, \\ L^*_3 = L_1 + L_2 + L_3, \\ L^*_4 = L_1 + L_2 + L_3 + L_4, \\ L^*_5 = L_1 + L_2 + L_3 + L_4 + L_5 \end{cases}$$

and

$$\begin{cases} \Psi_{c0} = \Psi_{cj}(x)\big|_{x=L^*_0} \\ \Psi_{c1} = \Psi_{cj}(x)\big|_{x=L^*_1} \\ \Psi_{c2} = \Psi_{cj}(x)\big|_{x=L^*_2} \\ \Psi_{c3} = \Psi_{cj}(x)\big|_{x=L^*_3} \\ \Psi_{c4} = \Psi_{cj}(x)\big|_{x=L^*_4} \\ \Psi_{c5} = \Psi_{cj}(x)\big|_{x=L^*_5} \end{cases}$$

and j=1,2,3,4,5

From Eqs.(71), (73) and (75), we get,

$$I_{DRIFT_j} = \frac{S_4}{L_j - L_{j-1}} [(S_1 + S_3) \ln \left\{ \frac{\left(S_3 + \Psi_{cj}\right) + \sqrt{S_2^2 + \left(S_3 + \Psi_{cj}\right)^2}}{\left(S_3 + \Psi_{cj-1}\right) + \sqrt{S_2^2 + \left(S_3 + \Psi_{cj-1}\right)^2}} \right\} - \left\{ \sqrt{S_2^2 + \left(S_3 + \Psi_{cj}\right)^2} - \sqrt{S_2^2 + \left(S_3 + \Psi_{cj-1}\right)^2} \right\}] \tag{76}$$

where,

$$S_1 = V_{GS} + \varphi_F - V_{th} \tag{77}$$

$$S_2 = \frac{\in_{si} E_c}{C_{ox}} \tag{78}$$

$$S_3 = V_{fbj} - V_{GS} \tag{79}$$

$$S_4 = -2 \in_{si} \mu_0 W E_c \tag{80}$$

Now, integrating both sides of the Eq. (68) and using Eqs.(69), (70), (71) and (72),

$$\int_{L^*_{j-1}}^{L^*_j} I_{DIFF_j} dx = \int_{Q_{Ij-1}}^{Q_{Ij}} \frac{W\mu_0 V_T}{\sqrt{\left[1 + \left\{\frac{E_j(x)}{E_c}\right\}^2\right]}} dQ_{Ij} \tag{81}$$

where,

$$\begin{cases} Q_{I0} = Q_{Ij}(x)\big|_{x=L^*_0} \\ Q_{I1} = Q_{Ij}(x)\big|_{x=L^*_1} \\ Q_{I2} = Q_{Ij}(x)\big|_{x=L^*_2} \\ Q_{I3} = Q_{Ij}(x)\big|_{x=L^*_3} \\ Q_{I4} = Q_{Ij}(x)\big|_{x=L^*_4} \\ Q_{I5} = Q_{Ij}(x)\big|_{x=L^*_5} \end{cases}$$

and j=1,2,3,4,5

From Eqs.(70), (71), (72) and (81), we get,

$$I_{DIFF_j} = \frac{S_7}{L_j - L_{j-1}} \left[\ln \left\{ \frac{\left(S_5 + Q_{Ij}\right) + \sqrt{S_6^{\,2} + \left(S_5 + Q_{Ij}\right)^2}}{\left(S_5 + Q_{Ij-1}\right) + \sqrt{S_6^{\,2} + \left(S_5 + Q_{Ij-1}\right)^2}} \right\} \right] \tag{82}$$

where,

$$S_5 = 2C_{ox}\left[V_{fbj} + \varphi_F - V_{th}\right] \tag{83}$$

$$S_6 = 2 \in_{si} E_c \tag{84}$$

$$S_7 = S_6 W V_T \mu_0 \quad (85)$$

So, the drain to source current can be expressed as,

$$I_{DS} = \sum_{j=1}^{5} \left[I_{DRIFT_j} + I_{DIFF_j} \right] \quad (86)$$

Now, the expression in Eq. (86) is valid for all values of drain to source voltage below pinch off. As the drain to source voltage, V_{DS} is increased gradually, at a certain value of V_{DS}pinch off occurs at drain end of the channel i.e. the inversion layer charge becomes zero at drain end. This value of drain to source voltage is called pinch off voltage, V_{DP}. Above V_{DP}, the drain to source current remains constant. The expression of V_{DP} can be obtained by equating inversion layer charge expression in Eq. (70) at L^*_5 to zero and using Eqs. (31)- (33) and (70), (73), (74) and (77):

$$V_{DP} = V_{GS} - V_{th} + \varphi_F + \frac{\alpha_5}{\tau^2} - G^*_5 e^{\tau L^*_5} - H^*_5 e^{-\tau L^*_5} \quad (87)$$

where, G^*_j and H^*_j are not functions of V_{DP} and expressed as:

$$G^*_j = G_j - \frac{V_{DP}}{2\sinh(\tau L)} \quad (88)$$

$$H^*_j = H_j + \frac{V_{DP}}{2\sinh(\tau L)} \quad (89)$$

So, $V_{DS} \geq V_{DP}$, drift current component,

$$I^*_{DRIFT_j} = \frac{S_4}{L_j - L_{j-1}} [(\Psi_{c5} + S_3) \ln \left\{ \frac{(S_3 + \Psi^*_{cj}) + \sqrt{S_2^2 + (S_3 + \Psi^*_{cj})^2}}{(S_3 + \Psi^*_{cj-1}) + \sqrt{S_2^2 + (S_3 + \Psi^*_{cj-1})^2}} \right\}$$

$$- \left\{ \sqrt{S_2^2 + (S_3 + \Psi^*_{cj})^2} - \sqrt{S_2^2 + (S_3 + \Psi^*_{cj-1})^2} \right\}] \quad (90)$$

where,

$$\Psi^*_{cj} = G^*_j e^{\tau L^*_j} + H^*_j e^{-\tau L^*_j} - \frac{\alpha_j}{\tau^2} + V_{DP} \quad (91)$$

$$\Psi^{*}_{cj\text{-}1} = G^{*}_{j} e^{\tau L^{*}_{j\text{-}1}} + H^{*}_{j} e^{-\tau L^{*}_{j\text{-}1}} - \frac{\alpha_j}{\tau^2} + V_{DP} \tag{92}$$

Also, for for $V_{DS} \geq V_{DP}$, diffusion current component,

$$I^{*}_{DIFF_j} = \begin{cases} \frac{S_7}{L_j - L_{j\text{-}1}} \left[\ln \left\{ \frac{\left(S_5 + Q^{*}_{Ij}\right) + \sqrt{S_6^{\,2} + \left(S_5 + Q^{*}_{Ij}\right)^2}}{\left(S_5 + Q^{*}_{Ij\text{-}1}\right) + \sqrt{S_6^{\,2} + \left(S_5 + Q^{*}_{Ij\text{-}1}\right)^2}} \right\} \right]; j=1,2,3,4 \\ \frac{S_7}{L_j - L_{j\text{-}1}} \left[\ln \left\{ \frac{S_5 + \sqrt{S_6^{\,2} + S_5^{\,2}}}{\left(S_5 + Q^{*}_{I4}\right) + \sqrt{S_6^{\,2} + \left(S_5 + Q^{*}_{I4}\right)^2}} \right\} \right]; j=5 \end{cases} \tag{93}$$

where,

$$Q^{*}_{Ij} = -2C_{ox}\left(S_1 - \Psi^{*}_{cj}\right) \tag{94}$$

$$Q^{*}_{Ij\text{-}1} = -2C_{ox}\left(S_1 - \Psi^{*}_{cj\text{-}1}\right) \tag{95}$$

So, for $V_{DS} \geq V_{DP}$, drain to source current can be expressed as:

$$I^{*}_{DS} = \sum_{j=1}^{5} \left[I^{*}_{DRIFT_j} + I^{*}_{DIFF_j} \right] \tag{96}$$

So, the drain to source current can be expressed as :

$$I_{DS,tot} = \begin{cases} I_{DS}; V_{DS} < V_{DP} \\ I^{*}_{DS}; V_{DS} \geq V_{DP} \end{cases} \tag{97}$$

But, in the deep submicron level, drain to source current effectively does not remain constant after the pinch off voltage. Because of the channel length modulation effect present in the device, a positive slope is observed in the current-voltage characteristics in the pinch-off region. Channel length modulation effect can be included in the current equation of the device using an empirical formula used in [30]:

$$I_{DS,CLM} = I_{DS,tot}\left(1 + \frac{V_{DS} - V_{DP}}{V_A + V_{DP}}\right) \quad (98)$$

$$V_A = CL\sqrt{N_{eff}} \quad (99)$$

where, $I_{DS,CLM}$, C, L and V_A are drain to source current with channel length modulation effect, a constant ($2x10^{-3}$ V. $cm^{1/2}$) [30], total channel length and early voltage respectively.

3.7 Threshold Voltage Roll-off :

Threshold voltage roll-off is the difference between the threshold voltage of a short channel MOSFET and that of a long channel MOSFET. Expression of threshold voltage roll-off can be given by:

$$V_{roll\text{-}off} = V_{th} - V_{thL} \quad (100)$$

where, V_{thL} is the long channel threshold voltage that is the threshold voltage with infinite channel length; the term is independent of channel length and it is given by the expression in Eq. 55.

3.8 Drain Induced Barrier Lowering :

Drain induced barrier lowering is defined as the ratio of the change in threshold voltage to the change in drain voltage. Expression of Drain induced barrier lowering (DIBL) can be given by:

$$DIBL = \frac{V_{th1} - V_{th2}}{V_{DS1} - V_{DS2}} \quad (101)$$

where, V_{th1} and V_{th2} are threshold voltage of the device at drain voltages V_{DS1} and V_{DS2} respectively.

CHAPTER FOUR

RESULTS AND DISCUSSION

In this chapter, the results obtained from the proposed model have been represented graphically and compared with the simulated characteristics obtained by using professional 2D device simulator to verify the model. Total channel length, L of the device has been considered to be 120 nm with the lengths of the channel region with halo doping, L_1 and L_5 being 20 nm each. Ratio of the length of the channel regions, L_1: L_2: L_3: L_4: L_5 has been kept 1:1:2:1:1. In our analysis, channel thickness, t_{si} has been considered 20 nm. It is reported that the QMEs (Quantum Mechanical Effects) become negligible for the channel thickness over 5nm [31]-[32]. Hence, we have ignored QME in our modeling. Again, it is well-known that Ballistic transport is observed when the mean free path of the electron is longer than the dimension of the medium through which the electron travels [33]. At room temperature, the electron mean free path in heavily doped sample is 1-10 nm [34] whereas the channel length used in our analytical modeling is 120nm. So, the ballistic transport effect has not been considered in our modeling. Work functions of the gate materials, used in this analysis, are φ_{m1} = 4.8eV, φ_{m2} = 4.6eV and φ_{m3} = 4.4eV and effective oxide thickness, t_{eff} is kept 3.5nm. In our device simulator, Gold, Tungsten and Titanium have been used as the gate electrode materials. In the subsequent sections of this chapter the attained results from model and device simulator have been analyzed.

4.1 Surface Potential along the Channel: Variation with Drain and Gate Bias

Fig. 4.1 shows the variation of surface potential with lateral position of the channel from source to drain. From the figure, it is obvious that there is a two-step profile in the surface potential due to gate engineering used in the device and the lowest surface potential is always at a channel position under metal 1, material with higher work function, irrespective of drain potential. It is in agreement with our assumption considered in the modeling of the threshold voltage of the device. The energy barrier height would be highest at this position and channel would not be

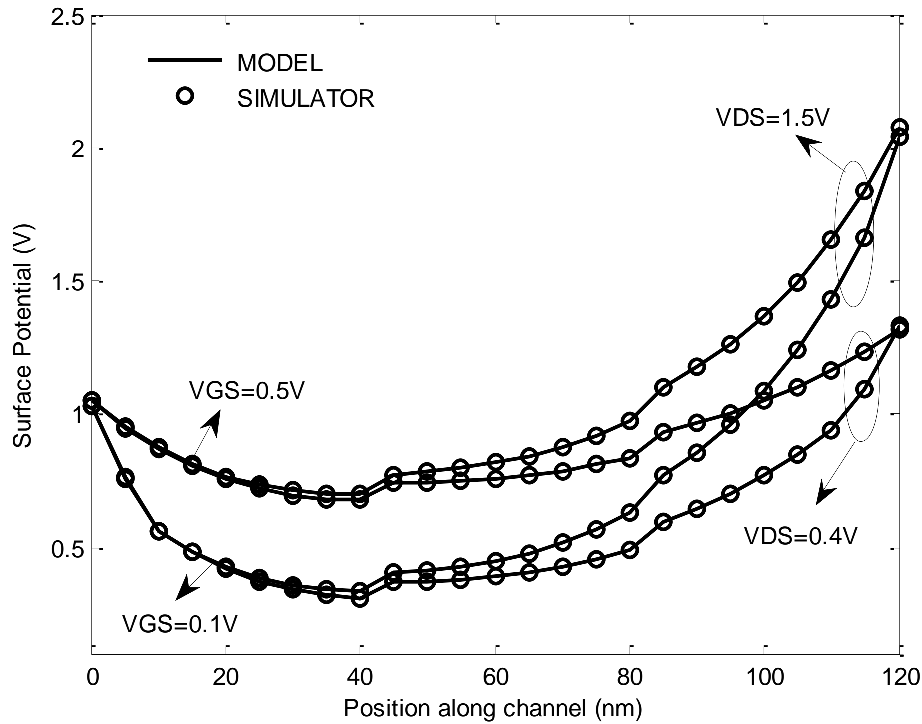


Fig. 4.1 Surface potential variation with lateral position along channel from source to drain for V_{GS}=0.1V, 0.5V and V_{DS}=0.4V, 1.5V

turned on unless this barrier is lowered. Thus, the drain to source voltage has a very little impact on channel and DIBL is not significant.

4.2 Electric Field along the Channel: Comparison among Various Device Structures

Fig. 4.2 shows the plot of electric field along the lateral position of the channel for Triple Material Double Gate Double Halo Gate Stack (TM-DG-DH-GS) MOSFET, Triple Material Double Gate (TM-DG) MOSFET and Single Material Dual Gate (SM-DG) MOSFET. The electric field has been calculated by taking the first spatial derivative of surface potential. It is clear from the figure that for TM-DG-DH-GS MOSFET, the electric field peak at the drain side is 0.223 MV/cm which is 20.74 times less compared to that (4.625 MV/cm) of SM-DG

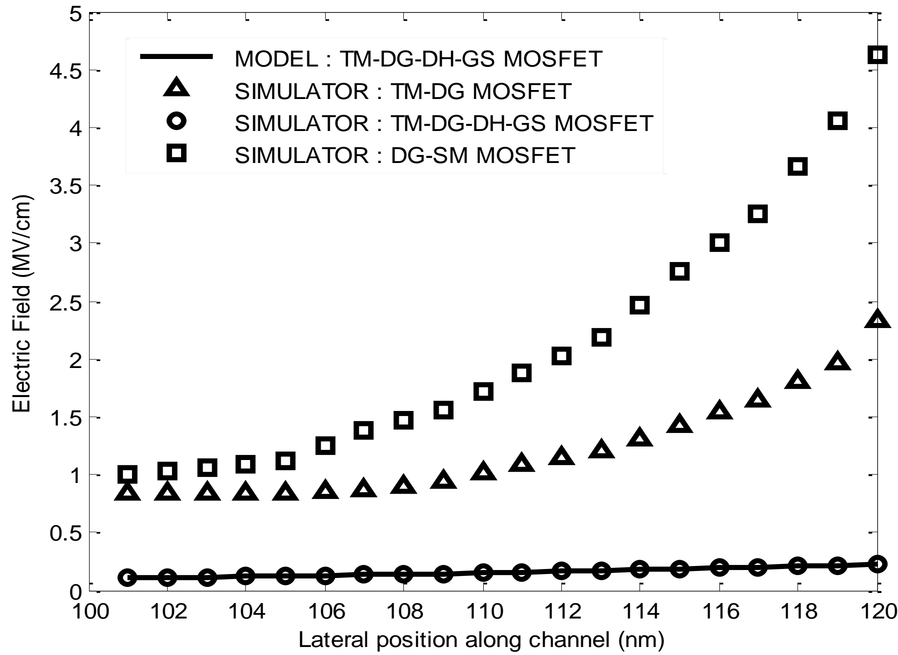


Fig. 4.2 Variation in electric field with lateral position along channel(100-120nm) for TM- DG-DH-GS MOSFET, TM-DG MOSFET and SM-DG MOSFET with V_{GS}=0.1V and V_{DS}=0.1V

MOSFET structure and 10.45 times less compared to that (2.33 MV/cm) of TM-DG MOSFET structure. So, gate and channel engineering in TM-DG-DH-GS MOSFET ensure less Hot Carrier Effect (HCE).

4.3 Threshold Voltage: Changes with Different Channel Lengths and Substrate Doping Concentrations

Fig. 4.3 presents the threshold voltage as a function of channel length with two different substrate doping concentrations. As the channel length is decreased, in both cases, the two halo regions approach each other, and the average channel doping increases. So, the threshold voltage is increased with the decrease in channel. But charge sharing effect becomes dominant with further decrease in channel length and as a result, there is a decrease in threshold voltage. It is

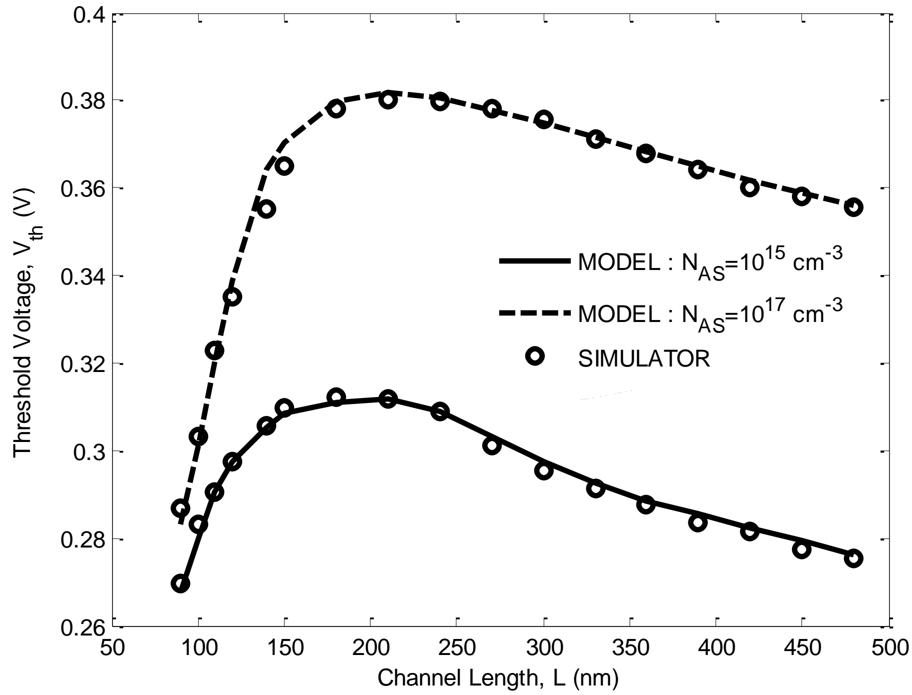


Fig. 4.3 Threshold voltage of the device along the channel length for $N_{Am} = 1.2x10^{18}/cm^3$, $N_{As} = 10^{15}/cm^3$ and $10^{17}/cm^3$ with $V_{DS} = 0.5V$

also observed from Fig. 4.3 that, the higher substrate doping concentration gives higher values of threshold voltage. Higher substrate doping requires greater gate bias to invert the channel and increases the threshold voltage likewise.

4.4 Threshold Voltage Roll-off: Comparison among Various Device Structures

Fig. 4.4 shows threshold voltage roll-off for TM-DG-DH-GS MOSFET, TM-DG MOSFET and SM-DG MOSFET for a drain voltage of 0.05V. The roll-off is lowest for TM-DG-DH-GS MOSFET, followed by TM-DG and SM-DG MOSFET structure for channel lengths below 150nm and this short channel effect (SCE) is least for TM-DG-DH-GS MOSFET likewise.

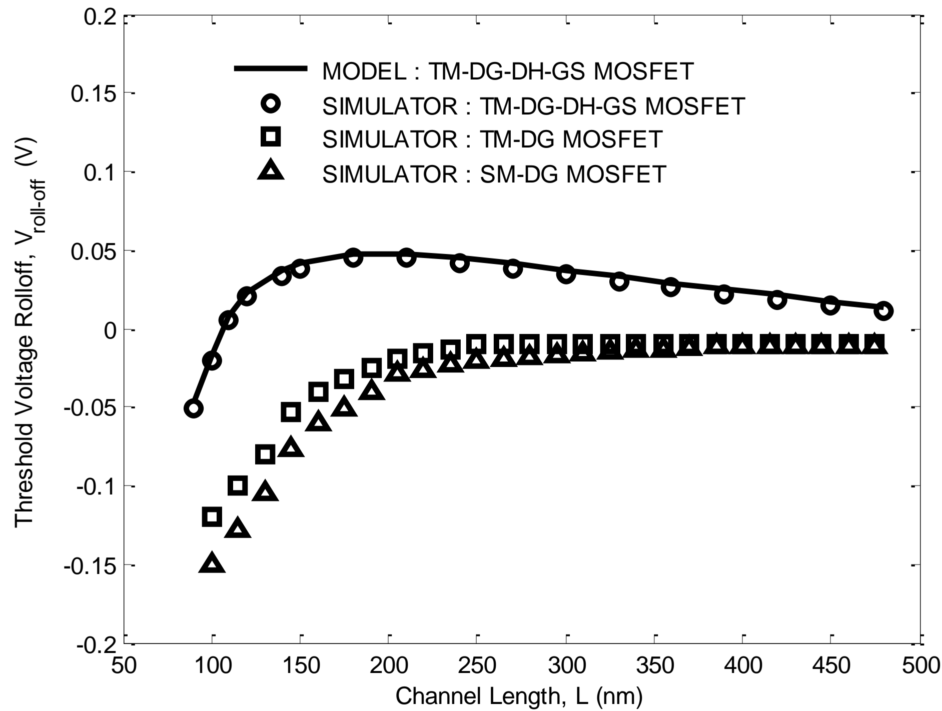


Fig. 4.4 Threshold voltage roll-off along the channel length for TM-DG-DH-GS MOSFET, TM-DG MOSFET and SM-DG MOSFET for $V_{DS} = 0.05V$

4.5 Threshold Voltage Roll-off: Effect of Drain Bias

Fig 4.5 lifts up the plot of threshold voltage roll-off for two different drain bias. It is obvious form the plot that higher drain bias results in higher SCE and larger value of threshold voltage roll-off likewise. It is because of the fact that high drain bias establishes more control over the channel than the gate bias and DIBL becomes dominant.

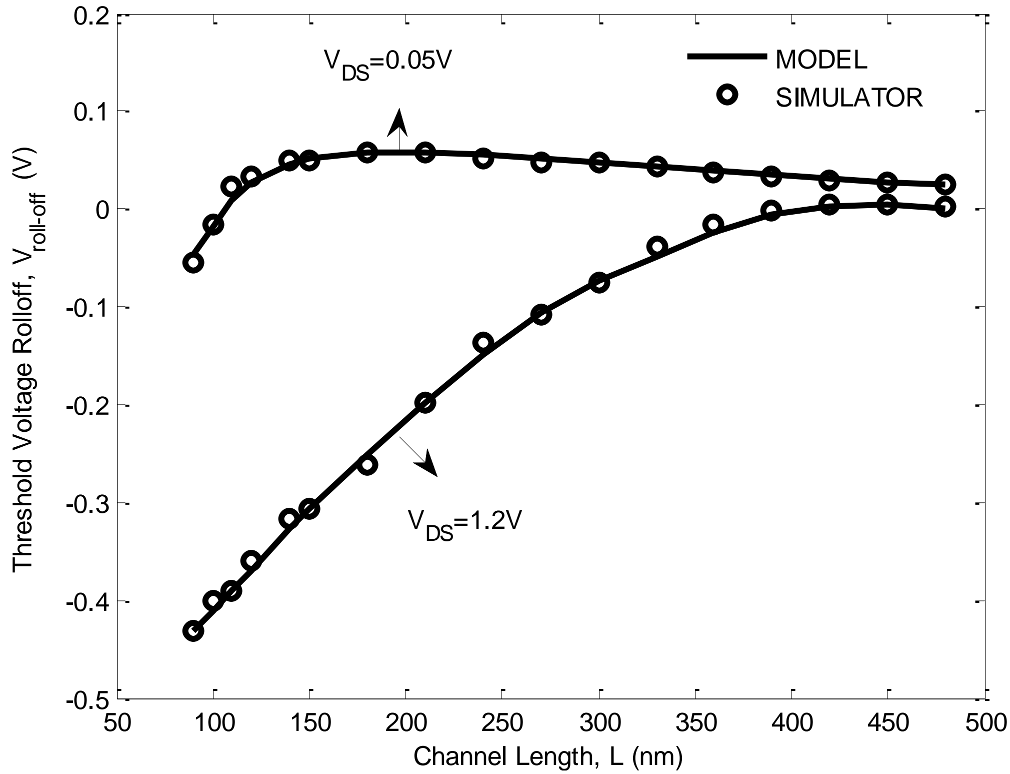


Fig. 4.5 Plot of threshold voltage roll-off vs channel length for $N_{Am} = 1.2x10^{18}/cm^3$ and $N_{As} = 10^{15}/cm^3$ for $V_{DS} = 0.05V$ and 1.2V

4.6 Drain Induced Barrier Lowering (DIBL): Comparison among Various Device Structures

It is obvious from Fig. 4.6 that DIBL effect is less for TM-DG-DH-GS MOSFET compared to TM-DG and SM-DG MOSFET structure. So, TM-DG-DH-GS MOSFET has better performance in dealing with DIBL compared to other device structures like TM-DG and SM-DG MOSFET. In our analysis, V_{DS1} and V_{DS2} are taken to be 0.1V and 2V, respectively.

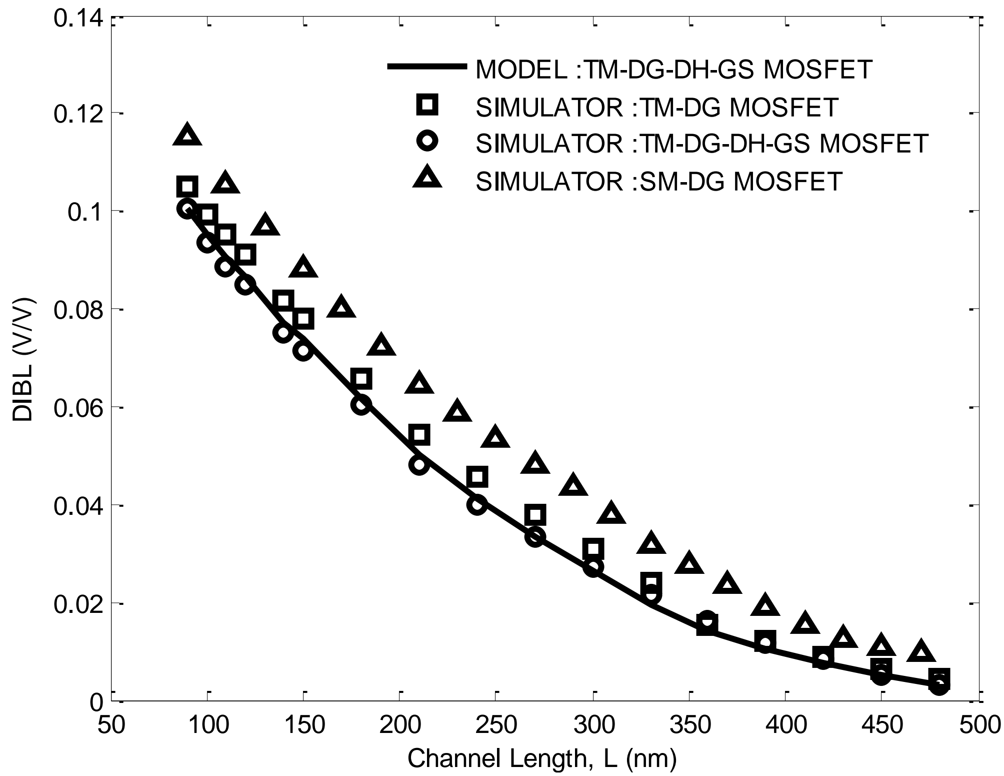


Fig. 4.6 Drain induced barrier lowering (DIBL) variation with channel length for TM-DG-DH-GS MOSFET, TM-DG MOSFET and SM-DG MOSFET

4.7 Drain Induced Barrier Lowering (DIBL): Effect of Halo Doping Concentration

Fig. 4.7 illustrates the advantage of using halo doping in the channel in dealing with DIBL. The plot displays that DIBL value is lower when higher halo doping concentration is used in the channel. Higher doping concentrations around the drain and source region restrict depletion regions to come into close proximity and thus mitigate the charge sharing effect. DIBL effect is minimized likewise with higher value of halo doping concentration.

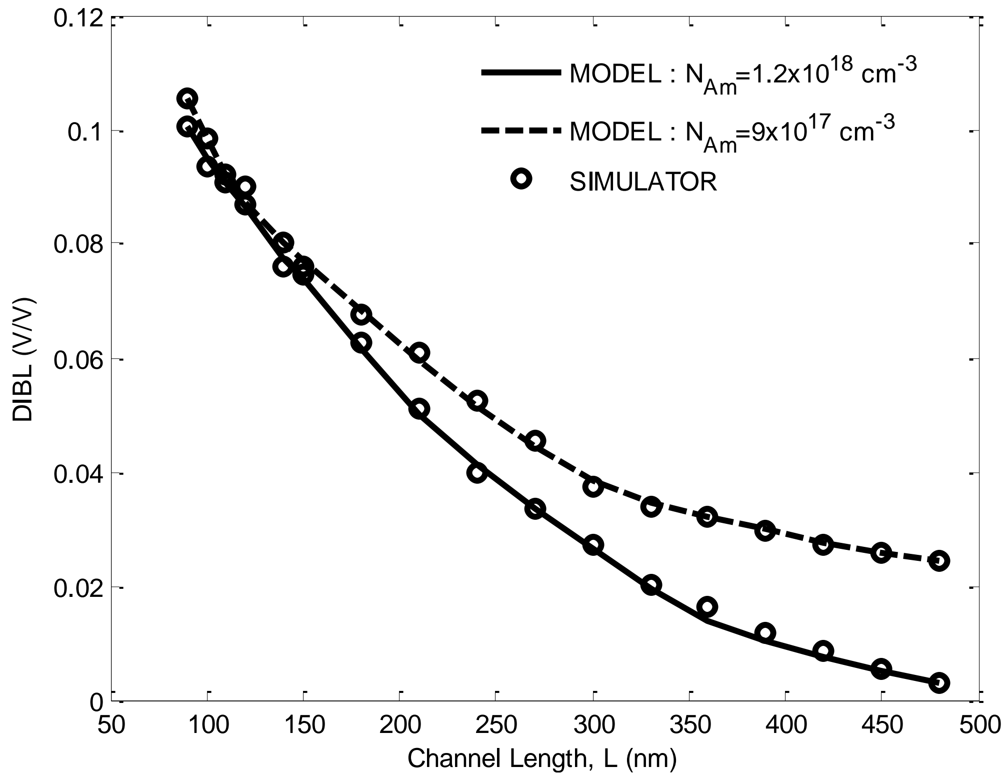


Fig. 4.7 Plot of Drain induced barrier lowering(DIBL) vs channel length, L for N_{Am} = $1.2x10^{18}/cm^3$, $9x10^{17}/cm^3$ and $N_{As}=10^{15}/cm^3$

4.8 Drain to Source Current: Variation with Gate Voltage for Different Drain Bias

Fig. 4.8 presents the drain to source current with varying gate voltages for three different drain voltages both including and excluding CLM effect. In the subthreshold region, negligible leakage current flows through the channel. Once the threshold voltage is achieved, the device is turned on and drain to source current increases with increasing gate voltage.

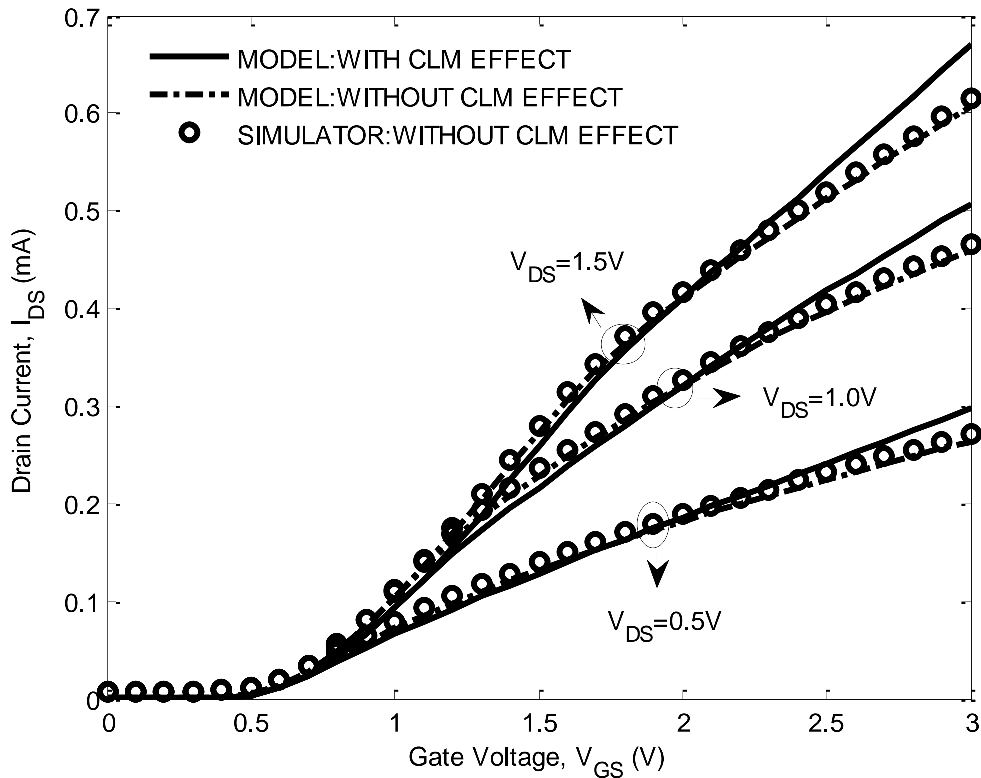


Fig. 4.8 Drain to source current, with and without Channel Length Modulation (CLM) effect, as a function of gate voltage for V_{DS}=0.5V, 1V and 1.5V

4.9 Drain to Source Current: Variation with Drain Voltage for Different Gate Bias

In Fig. 4.9, the drain current is plotted as a function of drain voltage for three different values of gate voltage. It is obvious from the figure that, in the model excluding the channel modulation effect, at a certain value of V_{DS} (pinch off voltage, V_{DP}), pinch off occurs at the drain end and current remains constant with further increase of drain bias. This means, in the saturation region, the slope of the curves become zero giving a zero output conductance. The locus of pinch off voltage shifts with the increase of gate voltage. However, owing to the CLM effect, as the drain voltage increases, depletion region at the drain terminal extends laterally into the channel and

hence the uninverted region expands toward the source. It shortens the length of the channel region i.e. Channel Length Modulation occurs. Since resistance is proportional to length, channel length shortening causes an increase in current with increase in drain bias for a MOSFET operating in saturation. Thus, a positive slope is observed in the I_{DS}-V_{DS} characteristics even at saturation, giving rise to a finite output conductance. If the drain current curves for different biases are extrapolated to zero drain current, the curves intersect the voltage axis at a point named Early voltage, V_A. Hence early voltage actually is caused due to CLM effect. For higher value of Early voltage, the positive slope in the I_{DS}-V_{DS} characteristics curve and the output conductance of the MOS device will be lower and vice versa. Thus the model with CLM effect included in it lifts up the real device phenomenon in deep submicron level. For both cases, it is also prominent that the magnitude of drain current increases with increasing gate voltage as it crosses the threshold value.

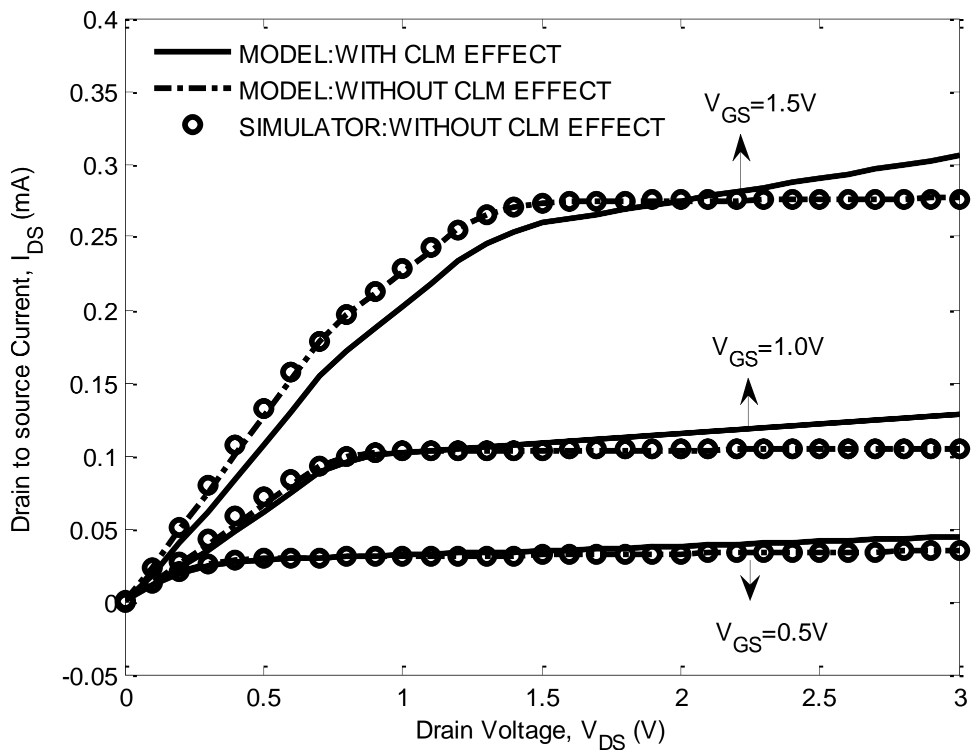


Fig. 4.9 Plot of Drain to source current, with and without Channel Length Modulation (CLM) effect, as a function of drain voltage for V_{GS}=0.5 V, 1V and 1.5V

4.10 Leakage Current: Contrast among Various Device Structures

Fig. 4.10 shows the plot of leakage current for low range drain voltages with V_{GS} =0V for a TM-DG-DH-GS MOSFET where both SiO_2 and HfO_2 have been used as gate oxide and also for a TM-DG-DH MOSFET with a layer of SiO_2 only as gate oxide. In both the cases, effective oxide thickness is kept 3.5 nm. It is evident from the figure that gate stack structure exhibits lower leakage current due to high-k i.e. gate stack used in TM-DG-DH-GS MOSFET structure reduces leakage current too.

So, the analytical model results, as a whole, show good agreement with simulation results from the 2D device simulator and prove the validity of our model.

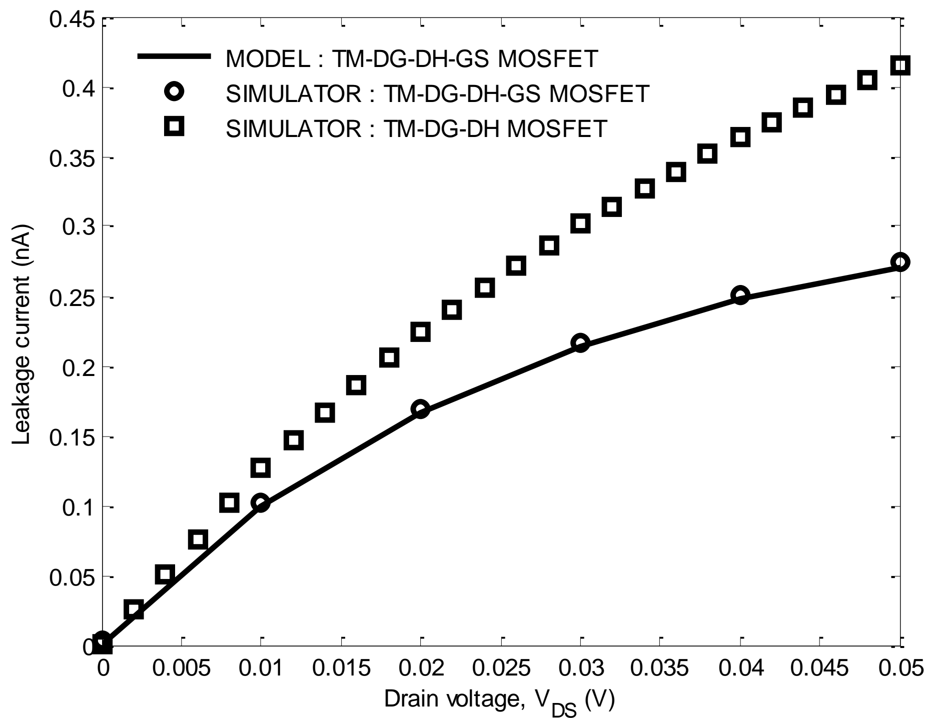


Fig. 4.10 Leakage current in TM-DG-DH-GS MOSFET and TM-DG-DH MOSFET as a function of drain voltage with t_{eff}=3.5nm and V_{GS} = 0V

4.11 Body Potential and Pseudo Flat Band Point (Crossover Point)

Fig. 4.11 presents the body potential of the device at x=30nm along with varied gate voltages at three different vertical position of channel (y=0, $t_{si}/2$ and $t_{si}/8$). The corresponding body potentials are termed as surface potential, mid channel potential and potential at 1/8th of the channel thickness. It is noticeable from Fig. 4.11 that all the three potential curves pass through a common point for a particular gate voltage. This point is called "Crossover Point" and the particular gate voltage can be termed as "Pseudo Flat Band Voltage", since there is no potential drop along the vertical direction of the channel from mid position to the surface of the channel. As the potential variation prevails along the lateral position even at this state, so it is called Pseudo Flat Band Condition.

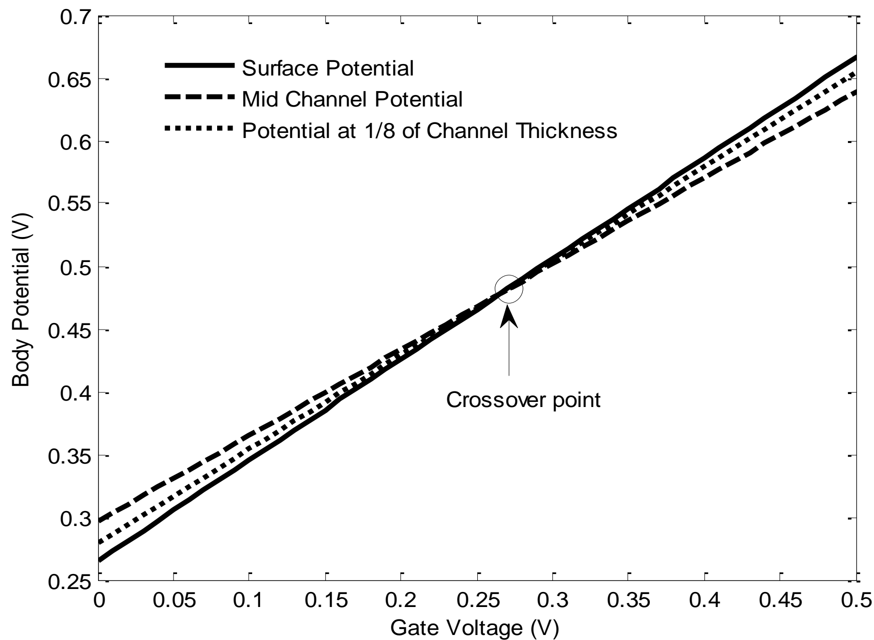


Fig. 4.11 Plot of body potential at x=30nm along with gate voltage with V_{DS} = 0.1V for t_{si}= 25nm

4.12 Surface Potential along the Channel: Variation with Effective Oxide Thickness

Fig. 4.12 depicts variation in the surface potential along the lateral position of the channel with changes in effective oxide thickness of the device. It is obvious from the plot that thicker oxide layer causes smaller values of surface potential. Thicker oxide layer contributes to weaker control of gate over the channel which leads to an increase in energy barrier height. This attributes to the fact that the surface potential is at some lower value, being inadequate to keep the energy barrier lower. So, the lowest value of surface potential is observed with t_{eff} = 4.5nm while the highest with t_{eff} = 2.5nm.

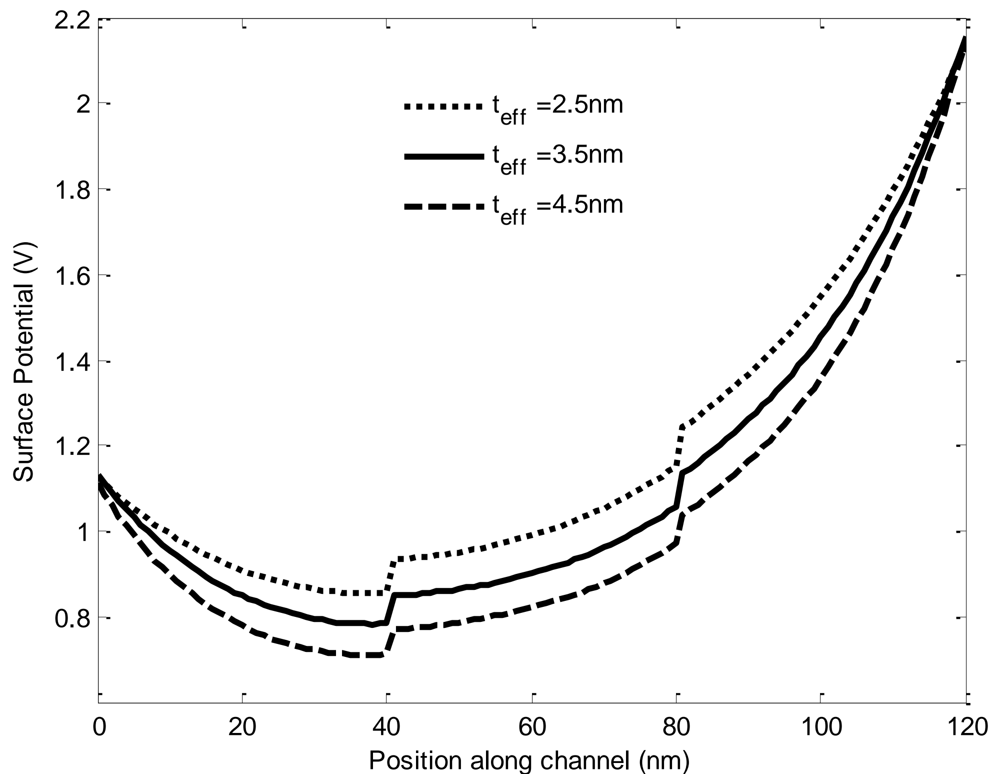


Fig. 4.12 Surface potential variation with lateral position along channel from source to drain for effective oxide thickness, t_{eff}= 2.5nm, 3.5nm and 4.5nm with V_{GS}=0.5V and V_{DS}=1.5V

4.13 Surface Potential along the Channel: Effect of Doping Concentration Profile

Fig. 4.13 lifts up the changing trend of surface potential along the channel owing to the variation in doping concentration profile. With lower effective doping concentration value, inversion layer formation is easier because of higher electron mobility and less impurity scattering. This indicates the surface potential value is high enough to keep the energy barrier height more lowered compared to the case with higher effective doping concentration. Eqs. (2)-(4) suggest that the effective doping concentration is the highest for the uniform doping concentration profile and the lowest for the linear doping concentration profile. As a result, highest value of surface potential is observed with linear doping profile concentration and lowest with uniform doping profile.

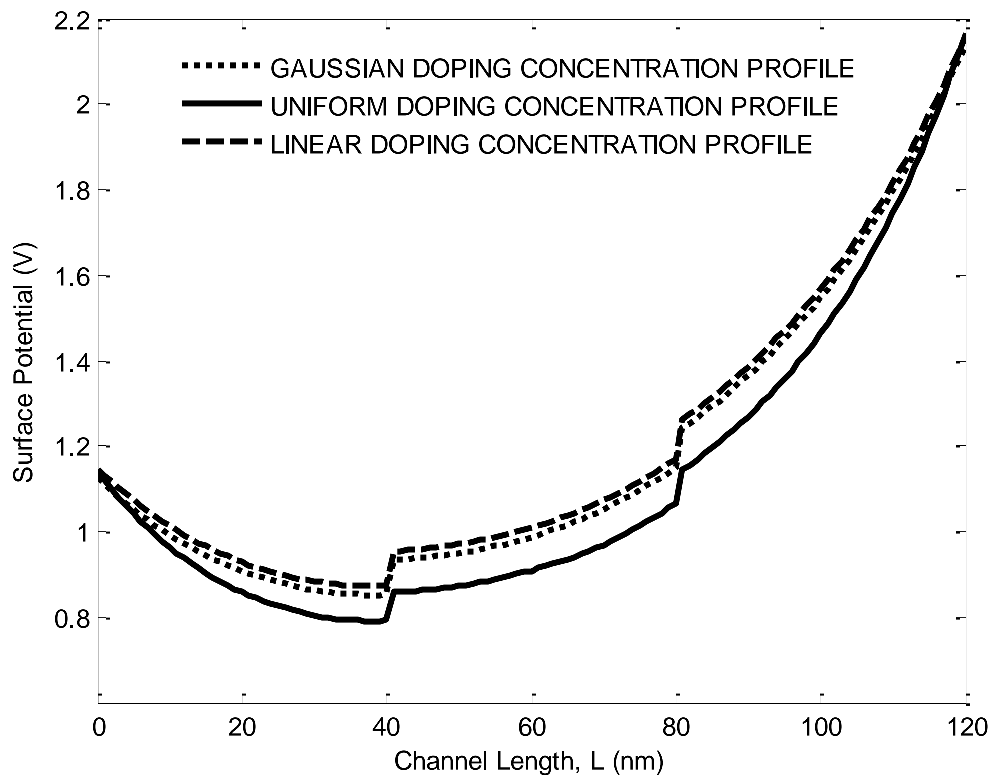


Fig. 4.13 Surface potential variation with lateral position along channel from source to drain for Gaussian, Uniform and Linear doping profile concentration with V_{GS} =0.5V and V_{DS} =1.5V

4.14 Surface Potential along the Channel: Variation with Silicon Channel Thickness

Fig. 4.14 illustrates the effect of silicon channel thickness on the surface potential along the lateral position of the channel. It is easily visible from the plot that surface potential is higher with thicker channel. The semiconductor channel with larger thickness benefits from more readily available charge carriers for inversion layer formation. Thus, the energy barrier height is smaller and the surface potential remains at a higher value. Accordingly, the highest value of surface potential distribution along the channel is observed with t_{si} = 25nm and the lowest with t_{si} = 15nm.

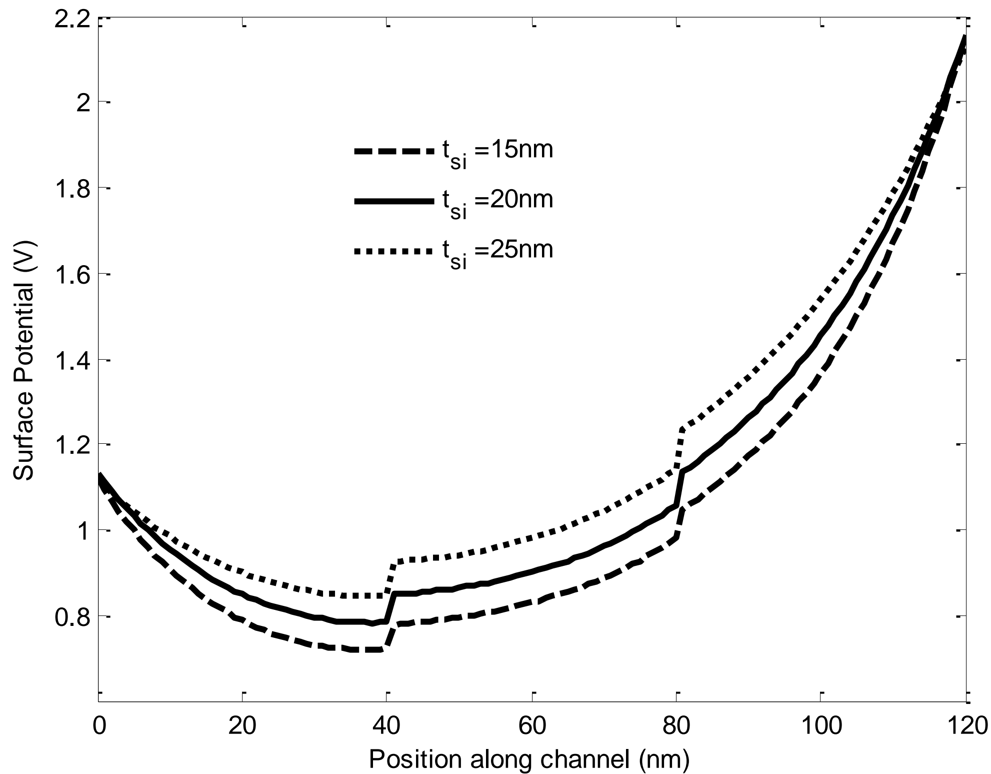


Fig. 4.14 Surface potential variation with lateral position along channel from source to drain for channel thickness, t_{si} = 15nm, 20nm and 25nm with V_{GS} =0.5V and V_{DS} =1.5V

4.15 Threshold Voltage: Effect of Effective Oxide Thickness

Fig. 4.15 shows the changing pattern of threshold voltage along with the changes in effective oxide thickness for different channel lengths. The influence of gate voltage, being less on the MOS channel with a thick oxide layer, the amount of gate bias required to turn on such a device is higher. So, the threshold voltage is higher with a thicker gate oxide layer. Consequently, the highest value of threshold value has been found with thickest oxide layer and vice versa.

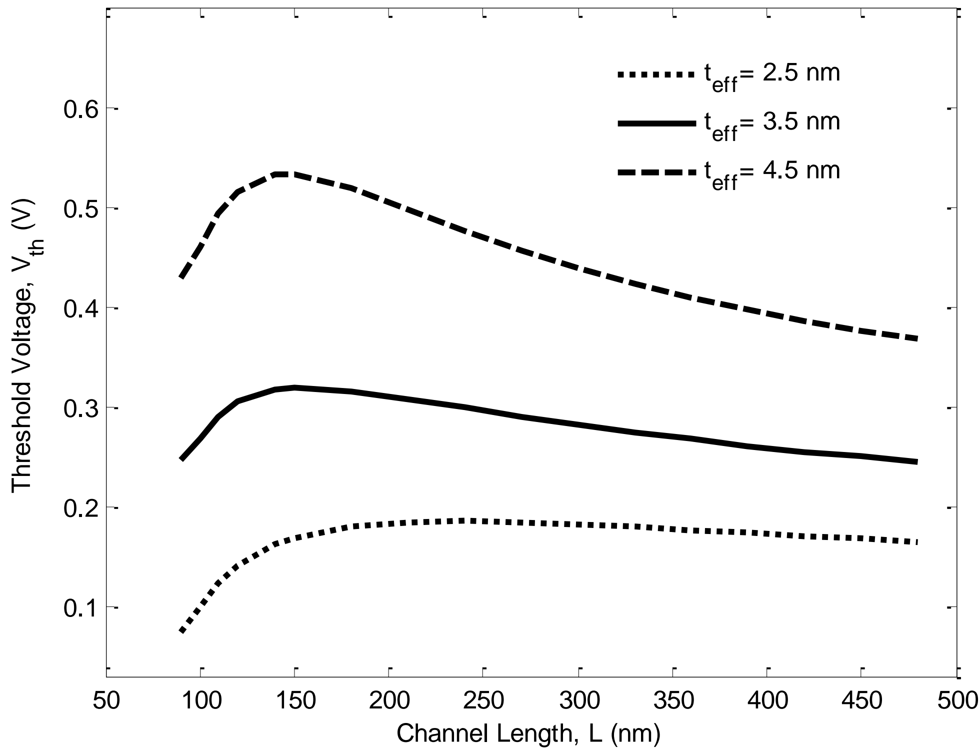


Fig. 4.15 Threshold voltage of the device along the channel length for effective oxide thickness, t_{eff}= 4.5nm, 3.5nm and 2.5nm with V_{DS}=1.5V

4.16 Threshold Voltage: Effect of Drain Bias

Fig. 4.16 shows the plot of the threshold voltage with varying drain voltages. It is observed that with increase in the drain voltage, there is a decrease in threshold voltage, as DIBL becomes

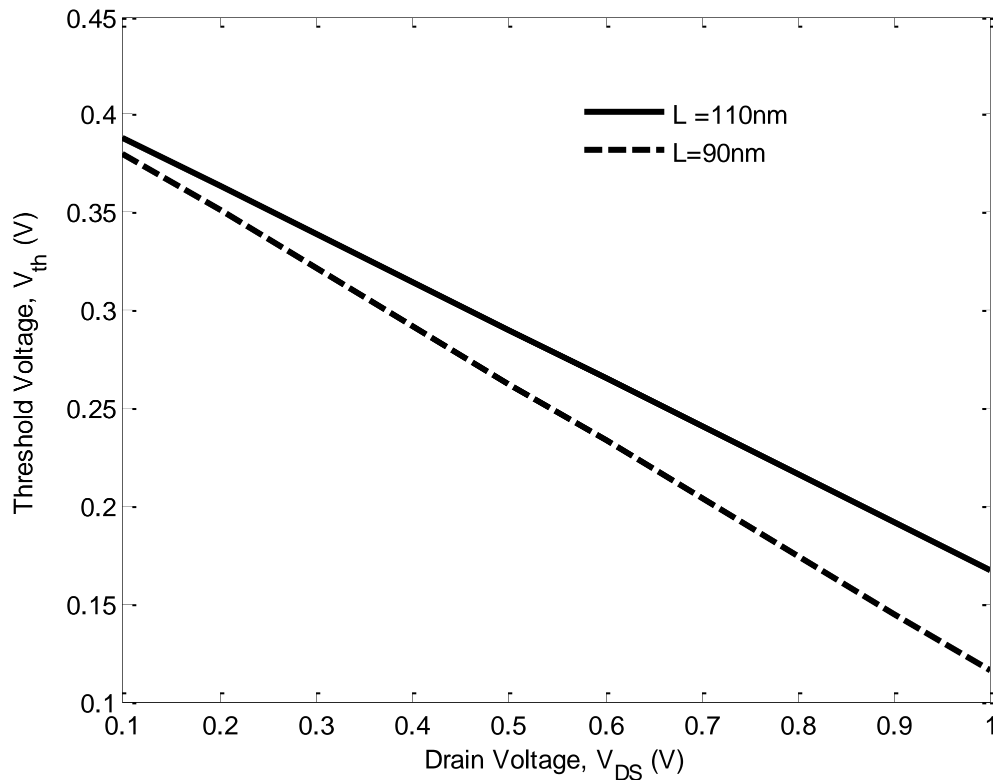


Fig. 4.16 Plot of threshold voltage vs drain voltage for Channel length, L=120nm and 90nm

significant with increasing drain potential. Also, a sharper decline in threshold voltage is observed with narrower channel length as the charge sharing effect is more acute.

4.17 Threshold Voltage: Variation with Channel Thickness

Fig. 4.17 holds a pictorial representation of the variation in threshold voltage as a function of channel length owing to different channel thickness. It is obvious from the figure that the threshold voltage is higher for thicker silicon channel. This phenomenon is attributed to the fact that the charge carriers are more abundant in a thicker channel device and the energy barrier height is lower likewise. Accordingly, the threshold voltage is lower in a device with higher channel thickness.

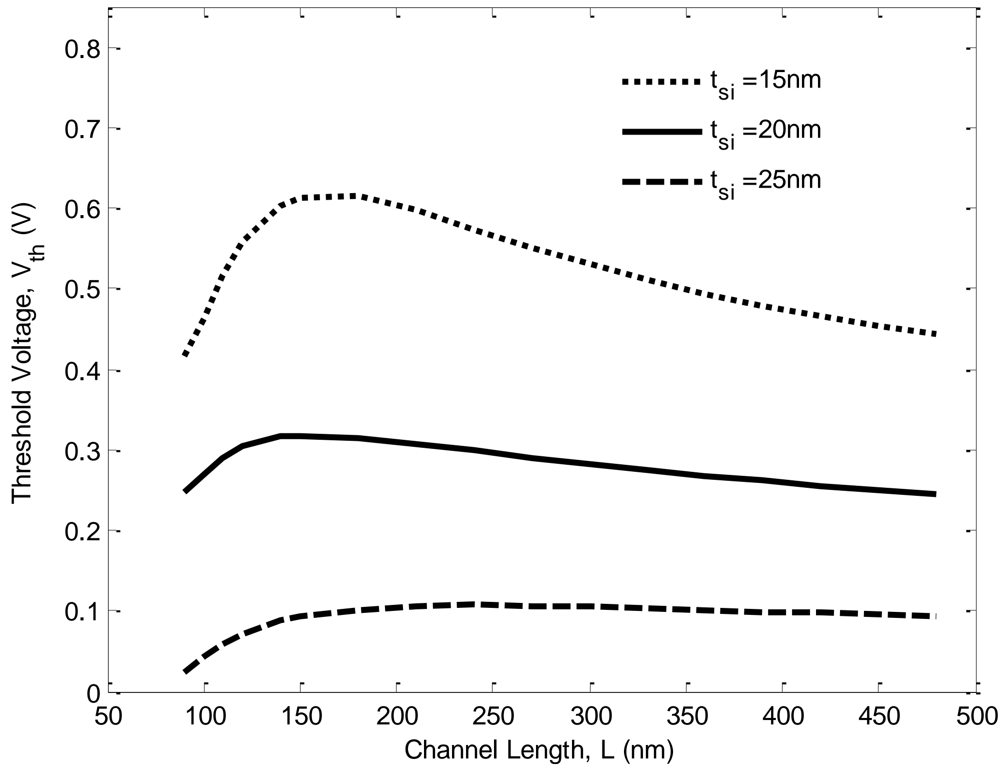


Fig. 4.17 Threshold voltage of the device along the channel length for channel thickness, t_{si} = 15nm, 20nm and 25nm with V_{DS} =1.5V

4.18 Threshold Voltage: Effect of Doping Concentration Profile

Fig. 4.18 demonstrates the changing pattern of threshold voltage with the variation of doping concentration profile for a set of channel lengths. High doping concentration causes abundance of impurity atoms which leads to a rise in energy barrier height for conduction and increased threshold voltage thereby. Since, uniform doping profile concentration renders the highest value of effective doping concentration among the profiles used; threshold voltage is highest with this concentration profile.

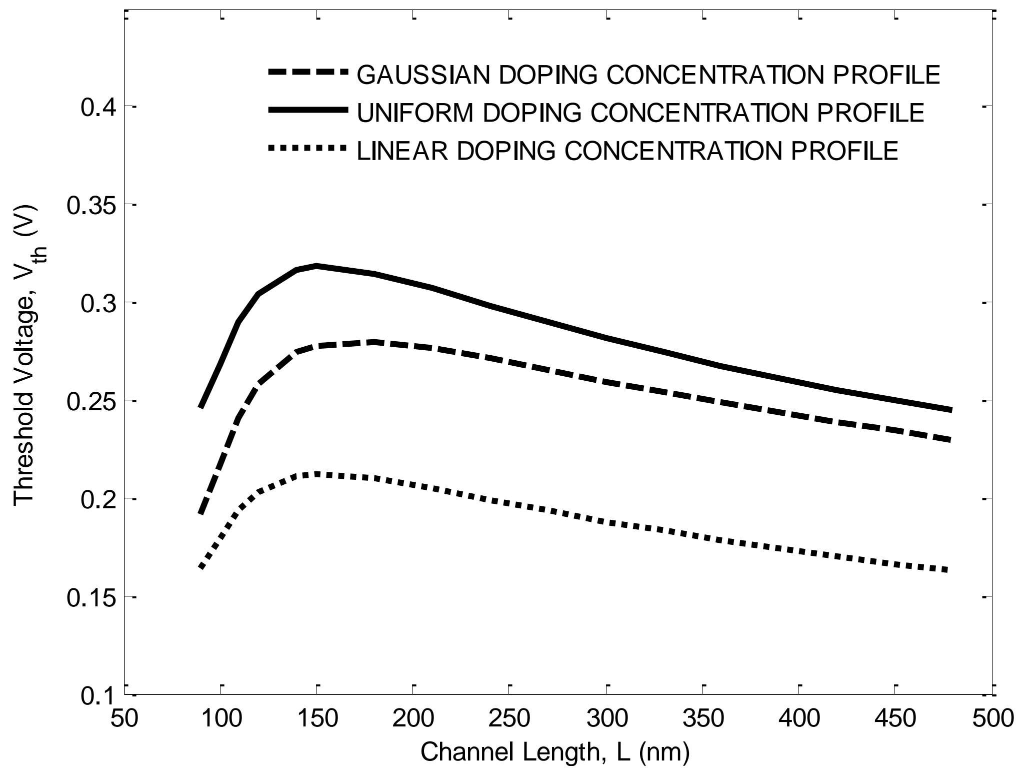
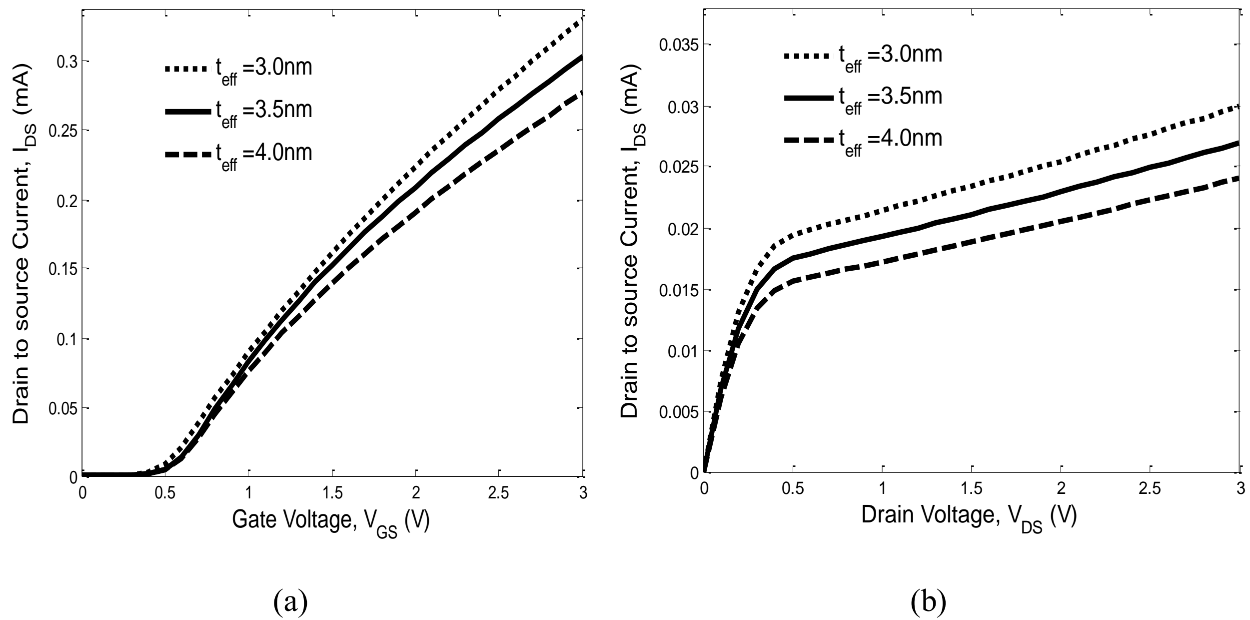


Fig. 4.18 Threshold voltage of the device along the channel length Gaussian, Uniform and Linear doping profile concentration with V_{DS}=1.5V

4.19 Drain to Source Current: Effect of Effective Oxide Thickness with Different Gate and Drain Bias

Fig. 4.19 shows the plot of drain to source current with changing gate and drain voltages for various effective oxide thickness. Channel length modulation has also been considered in these plots. A positive slope in the current vs drain voltage characteristics confirms the inclusion. Since, a thick oxide layer passivates the control of gate over channel, inversion layer formation becomes harder. Consequently, the magnitude of drain to source current with a thicker channel is lower.

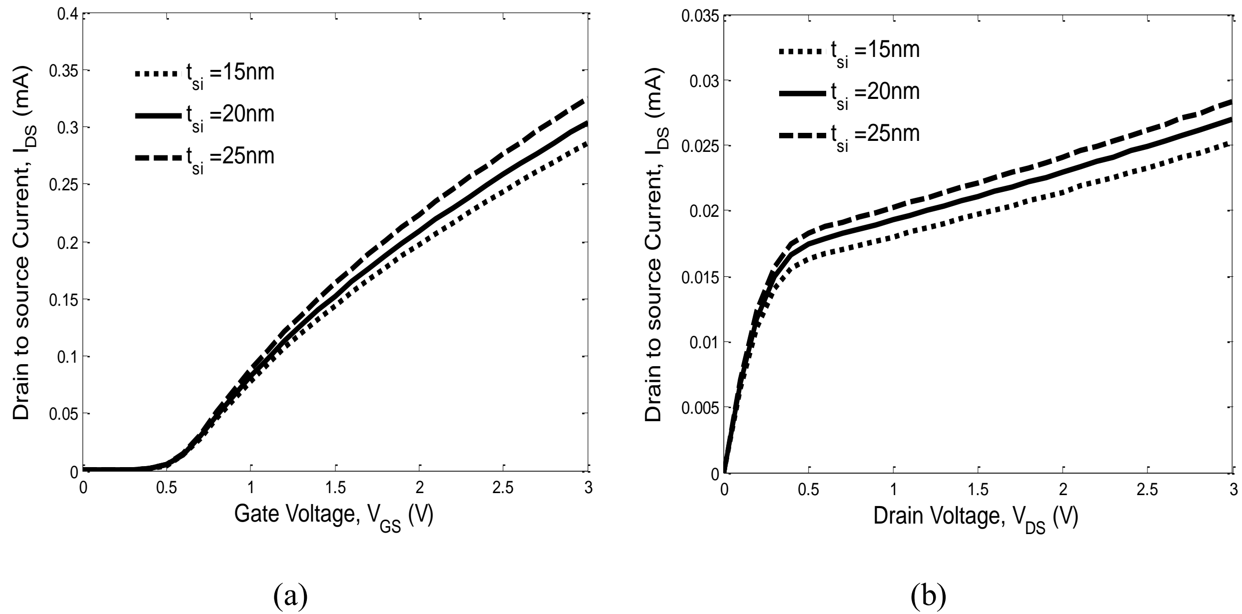


(a) (b)

Fig. 4.19 Plot of drain to source current, with Channel Length Modulation (CLM) effect for effective channel thickness, t_{eff} =3.0nm, 3.5nm and 4.0nm as a function of (a) gate voltage for V_{DS}=0.5V and of (b) drain voltage for V_{GS}=0.5V

4.20 Drain to Source Current: Effect of Silicon Channel Thickness with Different Gate and Drain Bias

Fig. 4.20 illustrates the effect of channel thickness on the drain to source current with various gate and drain bias. Thick channel contains plentiful of charge carriers which makes it easier to reduce the energy barrier height and gives a rise in current magnitude. In accordance with that, the highest current value has been observed with t_{si} =25nm and the lowest with t_{si} =15nm.

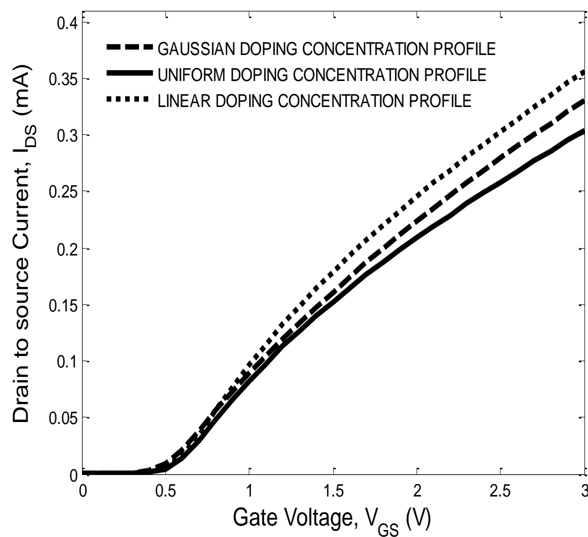


(a) (b)

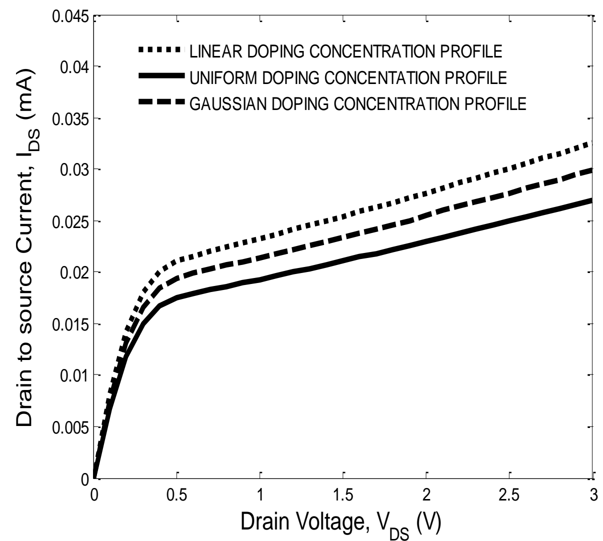
Fig. 4.20 Plot of drain to source current, with Channel Length Modulation (CLM) effect for channel thickness, t_{si} =15nm, 20nm and 25nm as a function of (a) gate voltage for V_{DS}=0.5V and of (b) drain voltage for V_{GS}=0.5V

4.21 Drain to Source Current: Variation with Doping Concentration Profile

Fig. 4.21 shows the changing trend in drain to source current with various doping concentration profile. The highest value of current is observed with linear doping concentration profile and the lowest with the uniform doping profile. Uniform doping concentration profile renders highest value of effective doping concentration along the channel which leads to more impurity scattering and less available inversion charge at the surface causing the lowest value of drain to source current. Likewise, the magnitude of highest current is with linear doping profile concentration giving rise to lowest effective doping concentration along the channel.



(a)



(b)

Fig. 4.21 Plot of drain to source current, with Channel Length Modulation (CLM) effect for uniform, gaussian and linear doping concentration profile as a function of (a) gate voltage for V_{DS}=0.5V and of (b) drain voltage for V_{GS}=0.5V

CHAPTER FIVE

CONCLUSION

5.1 Conclusion:

A two dimensional analytical model of triple material double gate double halo doped channel MOSFET has been presented in this work. The device structure incorporates the combined effects of gate and channel engineering in effective mitigations of SCEs. Gate engineering has been incorporated by the lateral assembling of multiple materials in the gate electrodes and by the inclusion of gate stack architecture in the oxide layers. Double halo doping has been used as a mean of channel engineering to deal with severe charge sharing effects present in a short channel MOSFET. The expression of channel potential has been derived considering parabolic approximation by means of solving Poisson's equations with suitable boundary conditions. To depict the bias dependent inner fringing phenomena, inner fringing potentials at both the drain and source side have been incorporated in the boundary condition equations. Oxide trapping phenomena have been included in the model by the inclusion of effective surface charge into the flat band voltage model. Thus a precise model of channel potential has been developed. It becomes prominent from the two-step profile of the surface potential that multiple materials in the gate electrodes ensure effective screening of channel from drain potential and suppresses DIBL effect likewise. Taking the first order spatial derivative of the surface potential, the expression of electric field has been derived. It has also been observed in this study that electric field value at the drain side is much lower in this MOS device compared to those obtained from some other device structures indicating the hot carrier effect is effectively minimized in this structure. The gate and channel engineering used in this device also render a suppressed threshold voltage roll-off. Channel length modulation effect has been considered in the drain to source current model. The drain to source current expression has been derived using basic drift diffusion equations. Mid channel potential has been used for the derivation of current expression in lieu of surface potential, since in a fully depleted MOSFET it is necessary to incorporate the body punch through phenomenon along with that of surface. In the model, leakage current with

zero gate bias and minimal drain voltage has also been studied. It is found out that the inclusion of a high-k dielectric oxide along with the conventional SiO_2 layer ensures the reduction of leakage current in contrast with other devices without considering gate stack technology. Thus, the proposed device structure has been found out to be suitable in this study to deal with SCEs associated with downscaling of latest devices. Besides lifting up the areas of improvement obtained with the MOS structure, the changes in various device characteristics have been studied along with the variations in device dimensions like oxide thickness, channel length, substrate doping concentrations etc. and with varied doping concentration profiles along the channel region as well. Among the doping concentration profiles used in this work, the uniform doping profile renders highest energy barrier and the most effective screening of channel from the drain. Thus the DIBL effect is the least with uniform doping concentration profile. In this work, Quantum Mechanical Effect and Ballistic Transport have not been included, since the device dimensions assumed for the modeling are long enough not to cause such effects in a practical device of similar dimensions. There remain some challenges regarding the fabrication issue of TM-DG-DH-GS MOSFET, since it is difficult to deposit three different adjacent metals on short length gates; however this work lifts up the promises of the device in future nanotechnology. The accuracy of the proposed model has been verified by comparing the results with the numerical simulations. A good agreement is achieved with a reasonable accuracy over a wide range of device parameter.

5.2 Scope of Future Works:

The possible future extensions of the existing work have been listed below:

- The two dimensional Poission’s equation has been solved in this model using effective average concentration for model simplicity. The work can be extended by solving the Poission’s equations areawise considering different doping concentrations at different regions. This will definitely increase the model complexity, but will give more precise expressions of the device parameters.

- Quantum Mechanical Effects (QME) have not been considered in our model as the Si channel thickness was above 5 nm. However, it will be interesting to explore the QME phenomena in the TM-DG-DH-GS device structure with channel thickness below 5 nm.

- Ballistic transport phenomena have not been considered in our present model since the channel length considered in the model was 120nm. Including Ballistic transport phenomena in our model for sub 10 nm device structure will, therefore, be an important future work.

PUBLICATIONS BASED ON THE THESIS WORK

1. **"A Two Dimensional Analytical Modeling of Threshold Voltage and Drain Current of a Triple Material Double Gate Double Halo Gate Stacked MOSFET",** by Md. Arafat Mahmud and Samia Subrina. (SST: 100951, Under review at Semiconductor Science and Technology, Journal, IOPscience in 2014).

2. **"A Two Dimensional Analytical Modeling of Drain Current and Subthreshold Slope of a Triple Material Double Gate MOSFET",** by Md. Arafat Mahmud and Samia Subrina., Accepted at 8th International Conference on Electrical & Computer Engineering (ICECE), IEEE in 2014.

3. **"Two Dimensional Analytical Modeling of Subthreshold Slope and Channel Conductance of a Gate and Channel Engineered Double Gate MOSFET",** by Md. Arafat Mahmud and Samia Subrina (To be Submitted)

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