

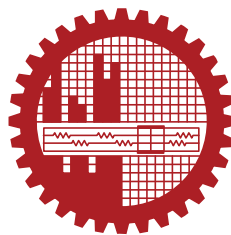
# VARIABILITY AND SELF-HEATING ANALYSIS OF SPIN TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY DEVICES

by

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MASTER OF SCIENCE  
IN  
ELECTRICAL AND ELECTRONIC ENGINEERING



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May 06, 2023

The thesis titled, "VARIABILITY AND SELF-HEATING ANALYSIS OF SPIN TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY DEVICES", submitted by Bejoy Sikder, Roll No.: 0419062224, Session: April 2019, has been accepted as satisfactory in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Electronic Engineering on May 06, 2023.

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# DECLARATION

This is to certify that the work presented in this thesis paper, titled, “VARIABILITY AND SELF-HEATING ANALYSIS OF SPIN TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY DEVICES”, is the outcome of the investigation and research carried out by BEJOY SIKDER under the supervision of Dr. Md. Zunaid Baten, Associate Professor, Department of Electrical and Electronic Engineering (EEE), Bangladesh University of Engineering and Technology (BUET).

It is also declared that neither this thesis book nor any part thereof has been submitted anywhere else for the award of any degree, diploma or other qualifications.

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May 06, 2023

# ACKNOWLEDGEMENT

I am thankful to Almighty for His blessings for the successful completion of my thesis. My heartiest gratitude, profound indebtedness, and deep respect go to our supervisor, Dr. Md. Zunaid Baten, Associate Professor, Department of Electrical and Electronic Engineering (EEE), Bangladesh University of Engineering and Technology for his constant supervision, affectionate guidance, and great encouragement and motivation. His keen interest in the topic and valuable advice throughout the study were of great help in completing the thesis.

I am especially grateful to Dr. Md. Aynal Haque, Dr. Anwarul Abedin, Dr. Samia Subrina, and Dr. Orchi Hassan for their consent to be on my board of examiners. I would also like to thank my collaborators Uday Kamal, Mondal Anik Kumar, Dr. Jia Hao Lim, Joel Tan, Dr. Nagarajan Raghavan, Dr. Kin-Leong Pey, Dr. Andrea Padovani, and Dr. Luca Larcher for providing their assistance in my research papers published from this thesis work. I appreciate the support from the Department of Electrical and Electrical Engineering (EEE) of Bangladesh University of Engineering and Technology (BUET) during my M.Sc. courses and thesis work. Finally, I would like to thank my family members, especially my mother, Provati Sikder, and sister, Projecta Sikder, for supporting me through many sleepless nights during my academic career. I extend my appreciation to Brishty Karmakar for her consistent and invaluable assistance over the past several years. My sincere thanks to Mr. Shahnewaz Ahmed for his useful suggestions and helps regarding simulation work.

# ABSTRACT

Spin Transfer Torque Magnetic Random Access Memories (STT-MRAMs) are promising candidates for next-generation data storage due to their non-volatility, fast access times, scalability, low power consumption, and compatibility with conventional CMOS technologies. The primary building block of an STT MRAM is the Magnetic Tunnel Junction (MTJ), which consists of two ferromagnetic layers separated by an insulating layer. However, owing to the small dimensionalities, STT-MRAMs are significantly prone to device-to-device and cycle-to-cycle variations. Moreover, the high current density required to program the MTJ invariably leads to self-heating, which significantly influences the device's performance and may even cause the breakdown of the insulating layer, thereby significantly limiting their reliability. In this thesis, a simulation framework for studying the device-to-device variability along with the self-heating analysis capability of the STT MRAM device has been developed. The proposed framework has been validated against reported experimental results in the literature. Within this framework, device-to-device variability of CoFeB/MgO-based STT-MRAMs is studied, considering the influence of interface quality, temperature variation, and device dimensionality. Metal-induced gap states resulting from electron transfer at the ferromagnet-tunnel barrier interface significantly influence these devices' effective energy barrier height, irrespective of their diameters. Switching voltage and parallel-antiparallel resistance values vary by as much as 43% and 30%, respectively, for about 13% variation of the energy barrier, whereas the tunneling magnetoresistance remains typically unaffected. WRITE cycles of highly scaled STT-MRAMs are, therefore, more susceptible to device-to-device variations resulting from microscopic variations in the interface quality rather than the READ cycles. Such variations are observed to be independent of temperature as well as the spatial distribution of the defects. Moreover, in this thesis, our proposed simulation framework has been extended to present a theoretical study of self-heating, taking into account the magnetic switching dynamics and three-dimensional heat transfer characteristics of STT MRAM devices. The impact of self-heating has been explored for different dimensions, geometrical aspects, and bias conditions of the device. The temperature rise of the MTJ stack is observed to be strongly dependent on the choice of the encapsulating material and top metal layer thickness. Because of the asymmetry of the stack, device-to-device self-heating variability is expected to be more prominent in undercut structures than in overcut ones. From transient analysis, it is observed that during both unipolar and bipolar pulsing conditions, MRAM switching is accompanied by an abrupt temperature change of around 25-30 K. The results of this work suggest that consideration of magnetic switching dynamics is essential to accurately estimate self-heating during transient and steady-state operations of STT-based MTJ devices.

# TABLE OF CONTENTS

|   |            |
|---|------------|
| <b>Certification</b>                                      | <b>i</b>   |
| <b>Declaration</b>  | <b>ii</b>  |
| <b><i>ACKNOWLEDGEMENT</i></b>                             | <b>iii</b> |
| <b><i>ABSTRACT</i></b>                                    | <b>iv</b>  |
| <b>TABLE OF CONTENTS</b>                                  | <b>v</b>   |
| <b>LIST OF FIGURES</b>                                    | <b>x</b>   |
| <b>LIST OF TABLES</b>                                     | <b>xi</b>  |
| <b>LIST OF ABBREVIATION</b>                               | <b>1</b>   |
| <b>1 Introduction</b>                                     | <b>2</b>   |
| 1.1 Introduction . . . . .                                | 2          |
| 1.1.1 Spin Transfer Torque MRAM (STT-MRAM) . . . . .      | 4          |
| 1.2 Literature Review . . . . .                           | 5          |
| 1.3 Motivation of the Work . . . . .                      | 9          |
| 1.4 Objectives of the Work . . . . .                      | 9          |
| 1.5 Thesis Outline . . . . .                              | 10         |
| <b>2 Theory of Magnetic Tunnel Junction</b>               | <b>11</b>  |
| 2.1 Introduction to Spintronics . . . . .                 | 11         |
| 2.2 Historical Advances in Spintronics Research . . . . . | 11         |
| 2.3 Basic Concepts of Spintronics . . . . .               | 13         |
| 2.4 MTJ Working Principle . . . . .                       | 13         |
| 2.5 MTJ Switching Mechanisms . . . . .                    | 16         |

|          |  |           |
|----------|--|-----------|
| 2.6      | Modeling of MTJ . . . . .  | 19        |
| 2.6.1    | Magnetization Dynamics: LLGS Equation . . . . .                  | 20        |
| 2.6.2    | Effective Magnetic Field . . . . .                               | 21        |
| 2.6.3    | Demagnetization Field . . . . .                                  | 21        |
| 2.6.4    | Voltage Controlled Magnetic Anisotropy . . . . .                 | 22        |
| 2.6.5    | Resistance Calculation . . . . .                                 | 23        |
| 2.6.6    | Trap Assisted Tunneling (TAT) . . . . .                          | 24        |
| <b>3</b> | <b>Device-to-Device Variability in STT-MRAM</b>                  | <b>27</b> |
| 3.1      | Description of the Simulation Framework . . . . .                | 28        |
| 3.2      | Results and Discussions . . . . .                                | 28        |
| 3.2.1    | Experimental Reports on Device-to-Device Variability . . . . .   | 28        |
| 3.2.2    | Analysis of Origin of the Device-to-Device Variability . . . . . | 29        |
| <b>4</b> | <b>Variability of Self-Heating in STT MRAM</b>                   | <b>38</b> |
| 4.1      | STT MRAM Stack and Self-Heating Model . . . . .                  | 39        |
| 4.2      | Undercut and Overcut structures . . . . .                        | 40        |
| 4.3      | Results and Discussions . . . . .                                | 42        |
| 4.3.1    | Spatial and Temporal Heat Distribution of MRAM Stack . . . . .   | 42        |
| 4.3.2    | Impact of Size Variations . . . . .                              | 43        |
| 4.3.3    | Impact of Shape Variation . . . . .                              | 45        |
| 4.3.4    | Impact of Variation of Encapsulation . . . . .                   | 45        |
| 4.3.5    | Self-Heating under different pulsed operations . . . . .         | 46        |
| <b>5</b> | <b>Conclusions</b>   | <b>51</b> |
| 5.1      | Summary of the Present Work . . . . .                            | 51        |
| 5.2      | Suggestions for Future Works . . . . .                           | 52        |
|          | <b>REFERENCES</b>  | <b>53</b> |

# LIST OF FIGURES

|     |  |    |
|-----|--|----|
| 1.1 | Memory hierarchy in a conventional computer architecture [1]. . . . .  | 3  |
| 1.2 | Processor Memory Performance Gap [5]. . . . .  | 3  |
| 1.3 | MJT cell of an STT-MRAM [6]. . . . .   | 4  |
|     |  |    |
| 2.1 | Spin-dependent tunneling of electrons in an MTJ while the magnetization directions in two FM layers are parallel (bottom left) and anti-parallel (bottom right) [52]. . . . .  | 15 |
| 2.2 | MTJ consists of three layers: two FM layer separated by an oxide barrier. The device resistance ( $R_P$ and $R_{AP}$ ) depends on the corresponding state of the magnetization of the two FM layers, Parallel(P) or Anti-parallel (AP). The MTJ state can be switched by modulating the magnetic field [53]. . . . . | 16 |
| 2.3 | MTJ Switching Regimes [57]. . . . .  | 17 |
| 2.4 | Spin Transfer torque switching mechanism from anti-parallel (AP) to parallel (P) configuration [61]. . . . .   | 18 |
| 2.5 | Illustration of different terms in LLGS equation . . . . .   | 19 |
| 2.6 | Tunneling processes in a MOS transistor [75]. . . . .  | 24 |
| 2.7 | Inelastic phonon emission model of trap assisted tunneling. Electrons, after being captured from the cathode, are relaxed to the trap energy level by phonon emission and then emitted to the anode [75,81]. . . . .   | 25 |
|     |  |    |
| 3.1 | Flowchart of the developed simulation framework . . . . .  | 28 |
| 3.2 | Schematic illustration of considered MTJ pillar. . . . .   | 29 |
| 3.3 | Measured R-V loops of $d = 60$ nm devices fabricated on the same wafer [94]. . . . .   | 30 |
| 3.4 | Schematic of the definition of Oxide Barrier Height. . . . .   | 30 |
| 3.5 | a) Proposed Band diagram of the MTJ device involving MIGS. b)-c) Reported Ab-initio calculations showing the density of states (DOS) in CoFeB/MgO/CoFeB [94, 102]. . . . .   | 31 |



|      |   |    |
|------|---|----|
| 3.6  | Measured (symbols) and simulated (lines) results of (a) R-V loops and (b) I-V loops (c) TMR vs. voltage characteristics and (d) R-V loops at different temperature for $d = 70$ nm. . . . .   | 32 |
| 3.7  | Measured (symbols) and simulated (lines) R-V loops for highest and lowest resistance values of each diameter. . . . .   | 33 |
| 3.8  | Effect of $\phi$ on TMR of the device; inset shows $R_m$ obtained for multiple READ cycles during TDDB measurements where $V_R$ and $V_S$ refer to normalized READ and stress voltages respectively. . . . .  | 34 |
| 3.9  | Effect of operating temperature variation on R-V loops corresponding to extracted values of (i) $\phi = 1.35$ - $1.36$ eV and (ii) $\phi = 1.20$ - $1.23$ eV . . . . .  | 35 |
| 3.10 | Comparison of spin (solid lines) and trap current (dashed lines) densities for different concentrations of bulk defects (effect on R-V loop shown as inset). . . . .  | 35 |
| 3.11 | Trap currents calculated from linear (dashed lines) and statistical (solid lines) variation of $\phi$ ; inset shows energy band diagram illustrating the physical significance of $\phi$ . . . . .  | 36 |
| 3.12 | CDF plot of zero-bias $R_P$ considering the statistical variation of $t_{ox}$ (experimental results shown as symbols whereas dashed lines show fits with a fixed value of $\phi = 1.25$ eV for all devices) . . . . .   | 37 |
| 3.13 | CDF plot of zero-bias $R_{AP}$ considering the statistical variation of $t_{ox}$ (experimental results are shown as symbols whereas dashed lines show fits with a fixed values of $\phi = 1.25$ eV and continuous line shows fit with corresponding values of $\phi$ for all devices) . . . . .   | 37 |
| 4.1  | 2D schematic of the STT-MRAM stacks considered in this study for self-heating analysis. . . . .   | 40 |
| 4.2  | 2D Schematic of a) Overcut and b) Undercut Structures. Here $D$ is the nominal diameter, and $d$ is the diameter of the upper (lower) layer for overcut(undercut) structure. $D-d$ is the amount of overcut or undercut. . . . .  | 41 |
| 4.3  | a) Spatial temperature distribution of the whole STT-MRAM Stack along with the electrodes and encapsulation and b) temperature distribution of the MTJ stack along the z-x plane under the application of $-0.8$ V pulse for $5 \mu s$ . The diameter of the cylindrical MTJ is $70$ nm. From the distribution, it is evident that most of the heating occurs at the MgO layer, and it reaches up to $450$ K temperature. . . . . | 42 |

|      |  |    |
|------|--|----|
| 4.4  | a) Temporal Temperature profile for 70 nm MTJ under the application of -0.8V for 5 $\mu$ s. b) Temperature Rise $\Delta T$ vs. Applied negative bias voltage (UNI-) curve for MTJ with 70 nm diameter. The curve resembles a parabola. Fitting this curve to the equation $\Delta T = R_{th} \frac{V^2}{R_{MTJ}}$ , we can obtain $R_{th}$ . . . . .   | 43 |
| 4.5  | Variation of the steady-state temperature with the thickness of TiN and TaN layers. In both cases, the steady-state temperature increases with the thickness of the TiN and TaN layers. But in the case of the TiN layer, the change is more prominent than the TaN layer. . . . .   | 44 |
| 4.6  | a) The temporal temperature profile of MTJ stack with diameter 60, 70, and 80 nm under the application of -0.8 V pulse for 5 $\mu$ s. b) steady-state temperature rise $\Delta T$ vs bias voltage (V). Here the bias voltage is UNI- as per our convention. . . . .  | 44 |
| 4.7  | Temporal temperature profile for undercut, overcut, and original structure for the nominal diameter of 70 nm. . . . .  | 45 |
| 4.8  | Steady-state temperature for a) different upper diameter for Overcut and b) different lower diameter for Undercut structure. The temperature rise is always lower in the case of the undercut. However, the range of the temperature rise is larger for the undercut than the overcut structure for the same diameter values. . . . .  | 46 |
| 4.9  | a)Effect of encapsulation on the temporal temperature profile of an MTJ. Temperature increases more for lower thermal conductivity encapsulation, i.e. SiCOH than SiO2 b) Steady-state Temperature vs thermal conductivity ( $\kappa$ ) of encapsulation. c) Steady-state temperature for different encapsulation dimensions which shows an upward but very gradual rise. The initial and boundary temperatures for all cases are 298 K, as shown in the figure. . . . .   | 47 |
| 4.10 | a) Applied ramped positive voltage pulse with period 4 $\mu$ s and duty cycle 40%. Here only one period is shown. b) The corresponding resistance state of MTJ. Around 2 $\mu$ s, i.e. at 0.5V, there is a change in resistance values which indicates the switching of MTJ from $R_P$ to $R_{AP}$ . c) Temperature vs. time curve for ramped positive bias. The spike around 2 $\mu$ s corresponds to the switching of MTJ. Also, the temperature initially increases with the bias, but after switching, it gets decreased as the resistance after switching is higher ( $R_{AP}$ ), which results in lower heat and lower temperature before switching. . . . . | 48 |

|      |   |    |
|------|---|----|
| 4.11 | Steady state temperature under the application of a) positive ramped pulses and b) negative ramped pulses for different diameters. According to our convention, positive ramped pulses switch MTJ from $R_P$ to $R_{AP}$ , and so a discontinuity in Figure a) is observed. Also, due to the higher resistance of smaller devices, the temperature rise is lowest for 60 nm diameter. . . . .   | 48 |
| 4.12 | a) Applied bipolar voltage pulse with magnitude 0.8 V with period 310 ns. Here two periods are shown. b) The corresponding resistance state of MTJ. Three distinct resistance states are evident from this figure. The lowest one is the RP state (marked by I), the middle one is the resistance in the AP state at 0.8V (marked by II), and the highest one is the resistance in the AP state at 0V (marked by III). c) Temperature vs. time curve for the application of the bipolar pulse. The spikes correspond to the switching between different R states of MTJ, as mentioned in Fig. 4b). d) Steady-state temperature rise for the application of bipolar ramped pulse from -1V to 1V. . . . . | 50 |

# LIST OF TABLES

|     |  |    |
|-----|--|----|
| 1.1 | Comparison of existing, prototypical, and emerging embedded memory technologies . *Energy only refers to single cell, without considering the bit lines and peripheral circuits [7]. . . . . | 5  |
| 1.2 | Different types of defects in STT-MRAM [36,37,43]. . . . .   | 9  |
| 2.1 | Historical Advances in Spintronics Research [47] . . . . .   | 12 |
| 2.2 | Defect parameters used to calculate trap current and comparison with ab-initio calculations and experiments. . . . .   | 26 |
| 3.1 | Average Barrier Height Used to calculate $R_p$ and comparison with ab-initio calculations and experiments . . . . .  | 32 |
| 3.2 | Extracted values of $\phi$ , and measured percentage (%) variation and percentage standard deviation (% $\sigma$ ) of $R_p$ and $R_{AP}$ . . . . .   | 33 |
| 4.1 | Material Parameters used for Simulation . . . . .  | 41 |
| 4.2 | Extracted $R_{th}$ for different diameters . . . . .   | 44 |

# LIST OF ABBREVIATIONS

|             |  |
|-------------|--|
| <b>AMR</b>  | Anisotropic Magnetoresistance          |
| <b>DRAM</b> | Dynamic Random Access Memory           |
| <b>FL</b>   | Free Layer                             |
| <b>FM</b>   | Ferromagnetic                          |
| <b>HDD</b>  | Hard Disk Drive                        |
| <b>LLG</b>  | Landau Lifshitz Gilbert                |
| <b>LLGS</b> | Landau Lifshitz Gilbert Sloczewski     |
| <b>MIGS</b> | Metal Induced Gap States               |
| <b>MRAM</b> | Magnetic Random Access Memory          |
| <b>MTJ</b>  | Magnetic Tunnel Junction               |
| <b>NEGF</b> | Non-equilibrium Green's Function       |
| <b>PDOS</b> | Projected Density of States            |
| <b>RL</b>   | Reference Layer                        |
| <b>SAF</b>  | Synthetic Anti-Ferromagnetic           |
| <b>SH</b>   | Self-Heating                           |
| <b>SOT</b>  | Spin Orbit Torque                      |
| <b>SRAM</b> | Static Random Access Memory            |
| <b>STT</b>  | Spin Transfer Torque                   |
| <b>TAS</b>  | Thermally Assisted Switching           |
| <b>TAT</b>  | Trap Assisted Tunneling                |
| <b>TDDB</b> | Time Dependent Dielectric Breakdown    |
| <b>TMR</b>  | Tunnel Magnetoresistance               |
| <b>VCMA</b> | Voltage Controlled Magnetic Anisotropy |

# CHAPTER 1

## INTRODUCTION

### 1.1 Introduction

Conventional memory architecture consists of different types of memory technologies, each having its own performance attributes. The memory hierarchy is shown in Fig. 1.1. Computers usually store a small amount of frequently used data in the fast SRAM caches, while a large amount of seldom used data are stored in the slow hard disk drive (HDD). Thus conventional architectures combine the high speed of the cache memory and the low cost of the HDD. The memory devices used in traditional devices can largely be categorized as: i) Volatile and ii) Non-volatile Memory. Volatile memories cannot retain their data after the power is cut. On the other hand, non-volatile memories can retain their data for a long period of time, even after the power is off. Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) are two of the most notable examples of volatile memory. On the other hand, Flash, EPROM, HDD, etc., are non-volatile ones.

SRAMs are usually used as CPU registers and cache (L1-L3) and store data statistically. On the other hand, DRAMs are usually used as the main working memory and require a periodical refresh. Flash is used as portable and integrated storage for consumer electronics and magnetic hard disks. Every memory device has its own pros and cons. SRAM has a lower access time, so it is fast. However, SRAM requires a constant power supply and so consumes higher static power. The circuitry required for SRAM is also very complex and costly. On the other hand, DRAM is slower than SRAM. But it offers reduced power consumption and requires small internal circuitry. It also has a high packaging density. On the other side of the spectrum, flash and HDD are non-volatile memory, but they have much lower access speeds and larger energy consumption for memory operations. But both of them have low cost and high density. However, during the last few decades, electronic device usage has increased immensely, ranging from computing devices to wearable ones. The major drive behind this growth is the ever-increasing logic computational capabilities which result in doubling computer chip transistor density every 18 months, popularly known as Moore's law. Despite the tremendous development of logic units in an electronic devices, the memory performance has not been on the same par. This created the

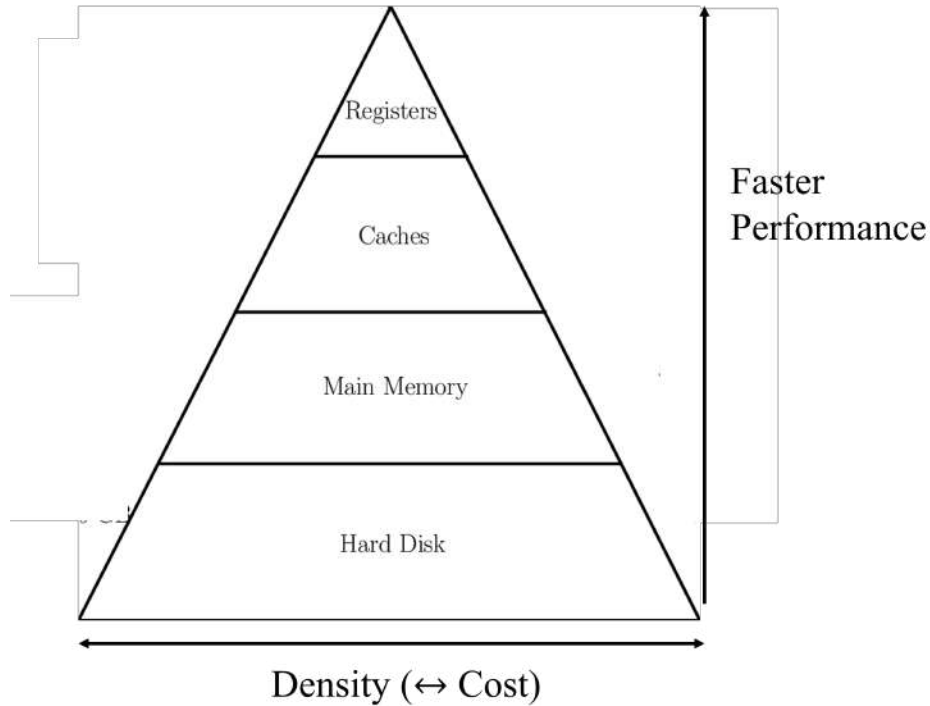


Figure 1.1: Memory hierarchy in a conventional computer architecture [1].

processor-memory gap, memory wall, or memory bottleneck, as shown in Fig. 1.2. Existing electronic memory devices cannot provide high speed, bandwidth, and less power consumption simultaneously. Various physical mechanisms have been proposed to resolve this memory wall issue. Several emerging non-volatile memory (NVM) technologies have been explored to improve speed, bandwidth, and power consumption. Magnetic Random Access Memory (MRAM) is one of the most promising candidates for this purpose. Spin Transfer Torque MRAM (STT-MRAM) is a type of MRAM considered universal memory owing to high endurance, faster access time, low power consumption, and CMOS compatibility [2–4].

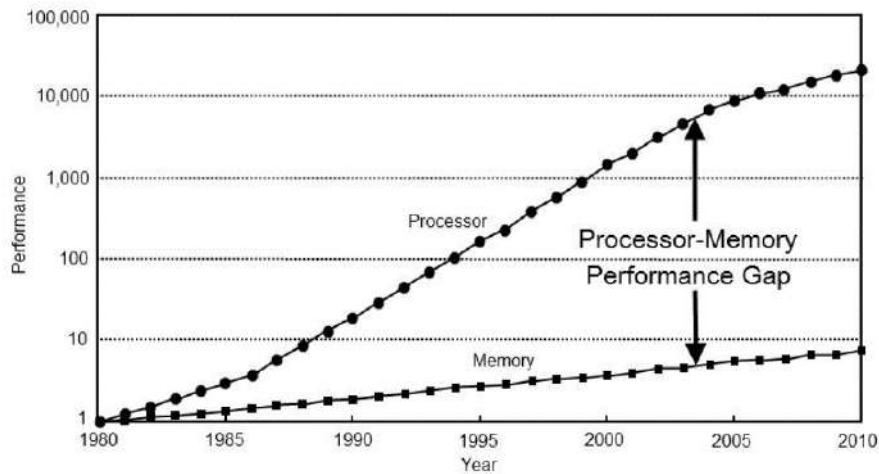


Figure 1.2: Processor Memory Performance Gap [5].

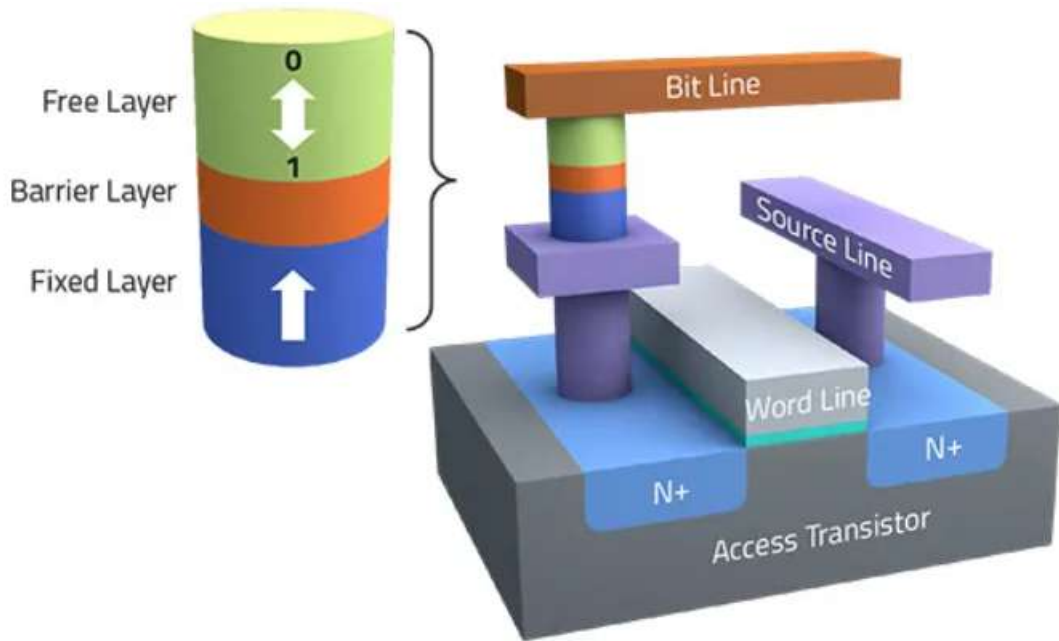


Figure 1.3: MJT cell of an STT-MRAM [6].

### 1.1.1 Spin Transfer Torque MRAM (STT-MRAM)

Spin Transfer Torque MRAM is a type of non-volatile memory that is considered to be one of the most significant inventions of spintronics. An STT-MRAM device with its primary component Magnetic Tunnel Junction (MTJ) along with Bit Line, Source Line and Write Line is shown in Fig. 1.3. Prior to STT-MRAM, spintronic devices were solely controlled by magnetic fields, which was a hindrance to the scaling of spintronics devices. In STT-MRAM, the spin-polarized current is used to apply spin transfer torque on the electron spins of a magnetic material which causes the device to switch between two states. STT-MRAM can replace embedded Flash, lower SRAM cache (L2-L3), and can be used in neuromorphic computing and Internet-of-things (IoT) due to its low power consumption. The comparison between different memory devices is given in Table 1.1.

The primary element in the MRAM technology is the magnetic tunnel junction (MTJ). In MTJ, two ferromagnetic layers are separated by an insulating layer which is called the tunnel barrier. One of the ferromagnetic layers is called the reference layer (RL) whose magnetization orientation is kept fixed and the other one's magnetization can vary in space which is called free layer (FL). For ensuring the stability of RL, other layers such as SAF (Synthetic Anti-Ferromagnetic) layer, Hard Layer etc. are used. These layers are described in detail in chapter 4. MTJ can have two stable orientations: i) when both magnetization vectors of RL and FL are in parallel and ii) when they are in anti-parallel orientations. Depending on these two orientations, the MTJ can have



Table 1.1: Comparison of existing, prototypical, and emerging embedded memory technologies .\*Energy only refers to single cell, without considering the bit lines and peripheral circuits [7].

|                                     | Existing        | Emerging             | Existing         | Prototype        |
|-------------------------------------|-----------------|----------------------|------------------|------------------|
| Technology                          | e Flash         | eReRAM               | eDRAM            | STT-MRAM         |
| Endurance (Cycles)                  | 10 <sup>5</sup> | 10 <sup>5</sup>      | 10 <sup>15</sup> | 10 <sup>15</sup> |
| Read Time (ns)                      | 10              | 3-10                 | 1-2              | 1-5              |
| Write/Erase Time (ns)               | 25 $\mu$ s/2ms  | 500/100 $\mu$ s      | 1-2              | 5-10             |
| Cell Size (area in F <sup>2</sup> ) | 40-100          | 15-30                | 40-100           | 40-50            |
| Bit Density (Gb/cm <sup>2</sup> )   | 0.5-1           | 1.5-3                | 0.5-1            | 1                |
| Read Energy/Bit (fJ)                | 10 <sup>6</sup> | 1000                 | 100              | 10-20            |
| Write/Erase Energy/bit (fJ)         | 10 <sup>6</sup> | 1000/10 <sup>6</sup> | 1000             | 100-200          |
| Non Volatile                        | Yes             | Yes                  | No               | Yes              |
| Standby Power                       | None            | None                 | Refresh          | None             |

two resistance states. Switching from one state to another is possible by the application of current or external bias fields. In STT-MRAM, spin transfer torque switching mechanism is used. Detailed theoretical backgrounds are provided in Chapter 2 of this thesis.

## 1.2 Literature Review

STT-MRAM is one of the most promising devices Spintronics has offered. Over the last few years, there has been several research works focusing on the modeling and device physics-related aspects of MTJ and STT-MRAM. Although this work does not include the neuromorphic application of these devices, a lot of research focus has been on this particular application field. Overall, STT-MRAM has been an active field of research in recent years. An accurate physics-based device model for the MTJ is required to investigate its electrical behavior along with stochastic switching and device-to-device variability. There exist two types of models for MTJ: static and dynamic.

Static models explain the switching of an MTJ with the concept of a threshold current or switching time. It utilizes the Julliere model to determine the stable state depending on whether switching has been occurred or not. W. Zhao et al. proposed a macro-model implemented in Verilog-A, which utilizes a combination of the Juliere model and Brinkman’s model to determine the bias-dependent conductance of different MTJ states [8]. They derived a simplified expression using Slonczweski for switching current based on which the different states of MTJ are determined [9,10]. But this model only considers switching due to thermal fluctuations and constant current amplitude.

Also, it does not consider the temperature dependence of different parameters and the stochastic switching nature of MTJ. S.S. Mukherjee et al. proposed a SPICE micro static model utilizing the hysteresis behavior of MTJ [11]. However, this model fails to capture the transient behavior and stochastic switching of MTJ. Another SPICE model proposed by J.D. Harms includes a decision circuit [12]. Based on its decision, MTJ switches for a given bias and its duration. Switching of MTJ is accomplished by utilizing the charging time of a capacitor for a given constant current. However, such a simplified model based on capacitor charging is inadequate to capture the magnetization dynamics in an MTJ.

The static models fail to capture the dynamics of the magnetization of an MTJ upon the application of bias. To solve this issue, several dynamic models have been proposed. L. Faber et al. [13] proposed an extended and modified version of the static model developed by W.Zhao [8], which includes heating effect and stochastic switching behavior. The model captures the dynamic nature of magnetization by considering two regions. When the applied current is lower than the critical current, the switching time is calculated by Neel-Brown Model [14]:

$$\tau_1 = \tau_0 \exp \left\{ \left( \frac{\Delta E}{k_B T} \left( 1 - \frac{I}{I_{C0}} \right) \right) \right\} \quad (1.1)$$

where  $T$  is the temperature,  $k_B$  is the Boltzmann constant,  $1/\tau_0$  is the attempt frequency and  $\Delta E$  is the energy barrier. For higher bias current, the model utilizes Sun's proposed model to compute the switching time:

$$\tau_2 = \frac{1}{\alpha \mu_0 \gamma M_s} \frac{I_{C0}}{I - I_{C0}} \ln \frac{\pi}{2\theta_0} \quad (1.2)$$

where  $\theta_0$  is the initial angle of the magnetization vector from the easy axis. This model also includes the heating effect by calculating temperature rise and fall, considering voltage across MTJ, current amplitude, and material thermal conductivity. This model utilizes equation 1.1 and 1.2, which are derived from the LLGS equation using some assumptions [15]. It assumes the small deviation of the initial angle  $\theta_0$  from the easy axis and constant amplitude for the applied current pulse, which are not always the case. As a result, this model fails to capture the transient behavior of MTJ switching under STT. M. Madec et al. [16–18] developed an improved dynamic model which incorporates both magnetic and non-linear electronic transport phenomena. LLGS equation is used to model the magnetic dynamics. The conductance is calculated using Julliere and Brinkmann's formalism, taking the bias dependence of conductance  $G$  and TMR into account. This model is implemented in VHDL. The self-heating effect is not considered in this work.

A. Nigam et al. [19] proposed a SPICE model that solved the LLG equation and ob-

tained the transient behaviors of MTJ. To capture the steady state properties, the Simmons tunnel current model is used [20]. Transmission probabilities of the carrier tunneling through the barrier and the available density of states are used to compute the I-V characteristics. The models discussed so far considered MTJ with in-plane magnetic anisotropy only. Zhang et al. [21] developed a device model of an MTJ with perpendicular magnetic anisotropy (p-MTJ) switched by STTs for the first time. MTJ conductances were calculated using Brinkman’s model along with the voltage-dependent TMR model. Switching behavior is captured by utilizing a threshold current and average switching time obtained from the approximated solution of LLG equation [22, 23].

C. Augustine et al. [24] presented a coupled Non-equilibrium Green’s Function (NEGF) and LLG framework for the numerical analysis of STT MTJ stacks for 1T-1R memory arrays. The authors utilized a set of experimentally calibrated MTJ parameters to obtain the charge and spin current density using NEGF. The STT is calculated from the differences of spin currents in the free layer of MTJ and used to solve LLG. The model was capable of predicting switching current density, TMR, etc., and electrical properties of MTJ. In the initial stages of the model described here, they were only simulating the static and dynamic behavior of an MTJ switched by STT. Later several models were proposed or modified to include the variability study of the devices. G. Panagopoulous et al. [25] modified the coupled LLG+NEGF model proposed in [24] to simulate time-dependent dielectric breakdown following the analysis developed for MOSFET gate dielectric models. In this work, the soft breakdown is modeled as a voltage-dependent current source parallel to the MTJ. The percolation current is assumed to be independent of the MTJ state and following a power law [25]. This model is able to model the TMR, switching performance, and lifetime degradation of STT MRAM due to breakdown. Later the same group published several papers to explore the device performance and analysis under geometrical, process, and CMOS parameter variations along with design space and scalability analysis of the device [26–28]. All these frameworks are implemented in SPICE, and the components include several bias-dependent sources and other passive elements.

In [29], the authors proposed a physics-based statistical model that evaluates the TDDB impact of device performances considering oxide thickness. The percolation model is used for statistical analysis of breakdown behavior. In [30], the reliability and variability of STT-MRAM cell are studied under the fabrication and aging-induced process, supply voltage, and operating temperature (PVT) variation. Bit-cells with different thermal stability coefficients are analyzed for stochastic thermal effect. A. Chintaluri et al. [31] presented a systematic analysis of all possible defect and fault models. Process-induced variability study is carried out in this work considering the variation of MTJ material parameters such as magnetic anisotropy,  $H_k$ , saturation

magnetization,  $M_s$ , TMR, etc., transistor electrical parameters such as threshold voltage, lithographic variation, and thermal fluctuations. In this work, both inter and intra-cell defects and faults are modeled by resistive shorts and open. Interconnect faults are also included. Few other papers also focused on the device performances of an STT-MRAM under process, material parameters, and operational condition-induced variations by utilizing Monte-Carlo or other statistical frameworks [32, 33]. Defect analysis is very crucial for the variability and reliability study of STT-MRAM. In an STT-MRAM, several defects can be present such as manufacturing defects, material defects, the presence of oxygen vacancies, traps, etc. Different types of defects and their origins are given in table 1.2. Conventionally, spot defects in STT-MRAM are modeled as a linear resistor whose resistance value represents defect strength [34–36]. Typically, open, short, and bridge resistors are used for modeling defects.

In [37], the authors proposed a methodology for physical defect modeling by considering the modification of the affected technology parameters of the MTJ. Their methodology includes extraction of the defect-free and defective device parameters such as resistance-area (RA) product, TMR, barrier height,  $H_k$ ,  $M_s$ , etc. The affected experimentally obtained parameters are then used to calculate the electrical properties such as resistance, switching current, and R-V hysteresis loop of an MTJ. The simulation framework is validated against the experimental results. However, the existing models fail to consider the impact of traps, material defects, and the interface between oxide and ferromagnetic materials on the device-to-device variability of an STT-based MTJ device. Modeling and influences of such effects constitute the first part of the thesis.

Self-heating (SH) is another factor that controls the reliability of a device. Due to the small dimensions of an MTJ, direct experimental measurement of the temperature rise due to SH is a pretty difficult task. As a result, a simulation framework is required. Early works modeled the temperature rise by modeling the phenomenon by circuit elements such as resistors and capacitors [28, 38]. Indirect measurements of temperature rise are reported by studying the TDDB and reliability of an MTJ [39, 40]. Van Beek presented a simulation-based study of temperature rise and the impact of different parameters on SH [41]. Hadáček et al. [42] developed a 3D simulation model for solving the heat diffusion equation in an STT-MRAM stack coupled with the LLG equation. However, a theoretical study that reconciles the switching dynamics of the STT-MRAM with the heat transfer characteristics of the entire stack is currently missing. Moreover, it remains to be seen how an STT-MRAM’s heat transfer characteristics will be influenced by its shape, size, surrounding, and biasing scheme. These aspects are considered in detail in the second part of the thesis.

Table 1.2: Different types of defects in STT-MRAM [36, 37, 43].

| FEOL (Front End of Line)  | BEOL (Back End of Line)   |  |
|---|---|--|
| Transistor  | Interconnect  | MTJ Device   |
| Material and Crystal defects,<br>Pinholes in gate oxide,<br>variation in dopants' position etc. | Open contacts,<br>Shape irregularities,<br>Presence of small particles etc. | Pinholes in Tunnel Barrier,<br>MTJ Sidewall redepositions,<br>Magnetization flipping in reference Layer,<br>Backhopping,<br>Material parameter variations,<br>MgO/CoFeB interface roughness etc. |

### 1.3 Motivation of the Work

Variability and reliability studies of STT-MRAMs are essential to fully understand the utility of these devices for future memory and neuromorphic applications. Previous studies on STT-MRAM variability primarily focused on variations arising from process, operating temperature, and operating conditions in MRAM circuits or arrays. Though significant insights on the variability and reliability of STT-MRAMs have been obtained from these studies, the ongoing drive towards utilizing highly-scaled variants of these devices for memory and neuromorphic applications necessitates variability analysis from a microscopic point of view. In particular, aspects related to the role of interface quality and defects on device-to-device variation need to be investigated to have a better understanding of the source of variability in these devices. Moreover, a detailed analysis of self-heating, taking into account the magnetization dynamics of STT-MRAMs, is currently missing in the literature. To better understand the phenomenon, a coupled simulation framework is required, which may correlate the heat transfer with the switching dynamics of these devices under static and pulsed operations.

### 1.4 Objectives of the Work

The main objectives of the work are:

1. To gain insight into the origin of the variability of STT-MRAMs by analyzing the impact of device and materials parameters on the static and dynamic performances of these devices.
2. To evaluate the impact of interface quality and defects on the device-to-device variability of STT-MRAMs.
3. To analyze self-heating in STT-MRAMs taking into account the magnetization dynamics of these devices under both steady-state and transient conditions.
4. To investigate self-heating considering device-to-device variability of STT-MRAMs.

## 1.5 Thesis Outline

The rest of this thesis is organized as follows: Chapter 2 begins with a brief discussion of the history and origin of Spintronics. Then the fundamental theory of a magnetic tunnel junction, along with different spin transport and switching mechanisms, has been explained. Finally, the governing equations required to model an MTJ with STT switching effect are described along with the theory of trap-assisted transport mechanism.

Chapter 3 describes the simulation framework developed in this work to investigate the device-to-device variability of an STT-MRAM. Then the reported experimental results on device variability have been discussed. Finally, the impact of barrier height at the interface of oxide and ferromagnetic materials have been elucidated.

Chapter 4 reports the modeling and results of the variability of self-heating in an STT-MRAM stack due to size, shape, and different pulsed switching mechanisms. First, the necessary equations required to determine the self-heating resulting temperature rise are explained with necessary material parameters and boundary conditions. Finally, the sources and their impact on the self-heating variability of STT-MRAM have been investigated.

Chapter 5 concludes the work. It summarizes the work presented herein and highlights the possible impact of this thesis in future studies. A brief discussion on future scopes of experimental and theoretical research in this direction is presented as well.

# CHAPTER 2

## THEORY OF MAGNETIC TUNNEL JUNCTION

The focus of this chapter is to introduce the basic concept related to the Magnetic Tunnel Junction device (MTJ) and the field of spintronics. The first section briefly details the spintronics—its history and fundamental physical operation. The second section of this chapter covers the characteristics and unique properties of the MTJ device. In the third section, we shall discuss the governing equations of an MTJ and how to use them to model this device's electrical behavior under applied bias.

### 2.1 Introduction to Spintronics

The word "Spintronics" is the amalgamation of the words "spin" and "electronics." According to the Oxford Dictionary, "Spintronics is the field of electronics in which electron spin is manipulated to yield the desired outcome." In conventional electronic devices, information processing works on the principle of control over the flow of charge through a material. On the contrary, spintronics involves the control and manipulation of both electron spin and charge in solid-state electronics [44, 45]. Large-scale non-volatile memories (e.g., hard disk drives or HDDs) exploit ferromagnetism to store information by controlling the spin alignment of the electrons applying external means of the magnetic field [46].

### 2.2 Historical Advances in Spintronics Research

Table 2.1 shows the key milestones in spintronics research classified into the following four categories: discoveries, key experiments, device concept proposals, and chip-level demonstrations. At first, the electron was discovered in 1897 by J.J. Thomson. An electron has both charge and spin. The electron charge was measured with perfection by R. Millikan. Spin is an intrinsic conserved property of elementary particles with no classical electron counterpart. Owing to having spin properties, electrons possess a magnetic moment akin to a rotating charged body in classical electrodynamics. This fact was discovered in 1922 by Otto Stern and Walther Gerlach, famously known as the Stern-Gerlach experiment. The resulting intrinsic magnetic moment  $\mu$  of electron

Table 2.1: Historical Advances in Spintronics Research [47]

|                                      | 1970   | 1980                            | 1990  | 2000   | 2010   |
|--------------------------------------|--|---------------------------------|---|--|--|
| <b>Discovery of Phenomena/Theory</b> | 1971 SHE<br>1975 TMR   | 1985 Spin injection<br>1988 GMR | 1992 GMR based two current model<br>1996 Spin torque transfer                       | 2001 MgO based MTJ<br>2007 Magnetoelectric effect  |  |
| <b>Lab Experiments</b>               |  |                                 | 1991 GMR at room temp. (1 <sup>st</sup> spin valve)<br>1995 TMR at room temp.       | 2000 STT switching at room temp.<br>2002 Perpendicular MTJ<br>2004 STT switching in MgO-MTJ<br>2007 Spin injection into spin channel<br>2008 Lateral spin valve switching  | 2010 Interfacial perpendicular MTJ<br>2010 Multi-level MTJ<br>2012 Voltage-assisted switching, Giant SHE switching |
| <b>Device Concept Proposal</b>       |  |                                 | 1990 Spin transistor<br>1997 GMR-MRAM<br>1998 TMR-MRAM                              | 2000 Nano magnet logic<br>2003 Spin oscillator<br>2008 Racetrack domain wall memory  | 2010 All spin logic<br>2012 Domain wall logic<br>2013 Spin random number generator                                 |
| <b>Circuit/Chip Demonstration</b>    | <p>* Acronyms<br/>SHE: Spin Hall Effect<br/>TMR: Tunnel Magneto Resistance<br/>GMR: Giant Magneto Resistance<br/>MTJ: Magnetic Tunnel Junction</p> |                                 | 1994 GMR field sensor (1 <sup>st</sup> GMR product), GMR Hard Disk Drive (HDD) head | 2003 0.6 $\mu$ m 1Mb 1T-1MTJ field-based MRAM<br>2005 1 <sup>st</sup> commercial MRAM, 180nm 4Kb STT-MRAM<br>2007 MgO-TMR HDD head<br>2009 45nm 32Mb STT-MRAM, 4Kb DW-MRAM | 2012 64Mb DDR3 STT-MRAM (Everspin)   |

Year  $\rightarrow$

having spin angular momentum  $\mathbf{S}$  is:

$$\boldsymbol{\mu} = \frac{g_s q}{2m} \mathbf{S} \quad (2.1)$$

where  $g_s$  is a dimensionless quantity called the  $g$ -factor. Later it was found that, like charge, spin is also quantized. The allowed values of  $\mathbf{S}$  are:

$$S = \frac{\hbar}{2} \sqrt{n(n+2)} \quad (2.2)$$

where  $\hbar$  is the reduced Planck constant and  $n$  is an integer. Wolfgang Pauli provided the theory of spin in 1927 by using the basic foundations of quantum mechanics. Spin states in quantum mechanics are represented by "Pauli Matrices" given by the following representations:

$$\begin{aligned} \sigma_x &= \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \\ \sigma_y &= \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix} \\ \sigma_z &= \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix} \end{aligned} \quad (2.3)$$

In the early 1970s, a study on spin polarization tunneling on ferromagnet/insulator/superconducting aluminum junction was conducted [48]. This study showed that electron spin remains conserved in electron tunneling through insulators. This result created the possibility of spin-sensitive tunneling between two ferromagnetic films.

Later, Mikhail D'yakonov and Vladimir Petel' predicted the spin Hall effect in 1971- a spin flow perpendicular to the current flow direction. In 1975, Julliere gave his famous



formula for calculating the Tunneling Magnetoresistance (TMR) ratio in terms of polarization of the two ferromagnetic layers of Fe/Ge/Co stack [49]. At that time, a ten % increase in anti-parallel state resistance was observed at 4.2K temperature. The next big thing came after a long time in the mid-to-late 1980s. Room temperature TMR effects were discovered. Anisotropic magnetoresistive (AMR) layers were first used to construct AMR-MRAM to replace bulky and heavy plated-wire radiation-hard memories [50]. With the discovery of Giant Magnetoresistance (GMR) in 1988, this AMR-MRAM became obsolete. After that, electron spin became a significant basis of almost all electronic information storage. The main difference between TMR and GMR is that in TMR, an insulator is used to transmit current by tunneling, while GMR uses a metallic layer. Generally, TMR shows a more considerable impedance change between parallel and anti-parallel states than GMR. In 1996, Slonzewski at IBM gave a theoretical prediction that the magnetization of a free layer can be toggled using spin-polarized current rather than an external magnetic field. This effect is termed spin transfer torque (STT). This has been verified by experiments and proven to consume low power and simplify the memory cell design compared to field-based switching [9].

### 2.3 Basic Concepts of Spintronics

An electron can have two possible values of spin quantum number:  $+\frac{\hbar}{2}$  and  $-\frac{\hbar}{2}$  which are conventionally termed as *up* and *down* spin. Information is coded as one of these two possible spin orientations in a conventional spintronic circuit. In traditional electronic circuits, electrons carry their spins along the wire, but the difference between up and down spin cannot be distinguished. On the other hand, spintronic circuits usually have two current channels: one for spin up electrons and one for spin down electrons. This can be obtained by utilizing a magnetic material with appropriate magnetic moment orientations.

### 2.4 MTJ Working Principle

In a magnetic tunnel junction, a thin non-magnetic insulating material is sandwiched between two ferromagnetic (FM) layers. The phenomenon can be microscopically explained by band structure. In any FM layer, the number of spin-up (majority) and spin-down (minority) electrons are not the same giving rise to net spin polarization. Spin polarization,  $P$  is defined as:

$$P = \frac{n \uparrow - n \downarrow}{n \uparrow + n \downarrow} \quad (2.4)$$

where  $n_{\uparrow}$  and  $n_{\downarrow}$  are the numbers of spin-up and spin-down electrons, respectively. In FM materials, the number of spin-up and spin-down electrons are different at the Fermi energy level. Consequently, the available density of states is also different for each [51]. The net magnetization depends on the difference,  $\delta n = n_{\uparrow} - n_{\downarrow}$  of two spin electrons. The more the difference, the stronger the magnetic moment. As the numbers differ in an FM layer, the material is magnetized due to the net magnetic moment generated by this non-equilibrium.  $\delta n$  near the Fermi level is important because these electrons act as carriers during transport. Electrons, while tunneling through the non-magnetic insulating barrier, follow the spin-state conservation principle. For example, a spin-up electron will tunnel if there is an available spin-up state for it in the Fermi level of the other FM layer. Therefore, the tunneling probability and hence current will depend on the relative orientation of the two FM layers. If the two layers are magnetized in the same direction, i.e., parallel state (P), then all the spin-up electrons can easily find a corresponding state after tunneling through the barrier because the band structures, as a rule, of the two FM layers are almost the same. However, if the two FM layers have antiparallel (AP) magnetization, only partial electrons can act as carriers for the tunneling current. For this reason, conductance (resistance) remains high (low) in the P-state and low (high) in AP-state. In other words, the resistance of the trilayer stack depends on the orientation of the magnetization of the FM layers. This is illustrated in Fig. 2.1.

This idea is implemented in Magnetic Tunnel Junction (MTJ). Fig. 2.2 shows a typical structure of an MTJ stack. As previously stated, the MTJ block has three layers: a thin insulator (usually oxide barriers such as  $Al_xO_y$  and MgO) sandwiched by two ferromagnetic layers. The spin magnetization configuration of the two ferromagnetic layers is different. Spin magnetization of one layer is fixed, and the other one can switch between two spin magnetization states, i.e., either parallel or antiparallel to the fixed layers. This layer is called the free layer, storage layer, or switching layer. Parallel (P) and antiparallel (AP) are usually used to indicate the two possible states of the free layer. The characteristics of the MTJ block can be tuned by changing the state of this free layer. And this can be achieved by applying an external magnetic field having a value greater than a certain threshold with an opposite directions. When the two FM layers are in parallel states, current passes through the MTJ block undisturbed, indicating a low resistance state ( $R_P$ ). However, in the antiparallel state, the other layer will block the current generated by the first layer indicating a high resistance state  $R_{AP}$ . The TMR ratio is one of the most important parameters which determines the performance of an MTJ device. It is defined as:

$$\text{TMR} = \frac{R_{AP} - R_P}{R_P} \quad (2.5)$$

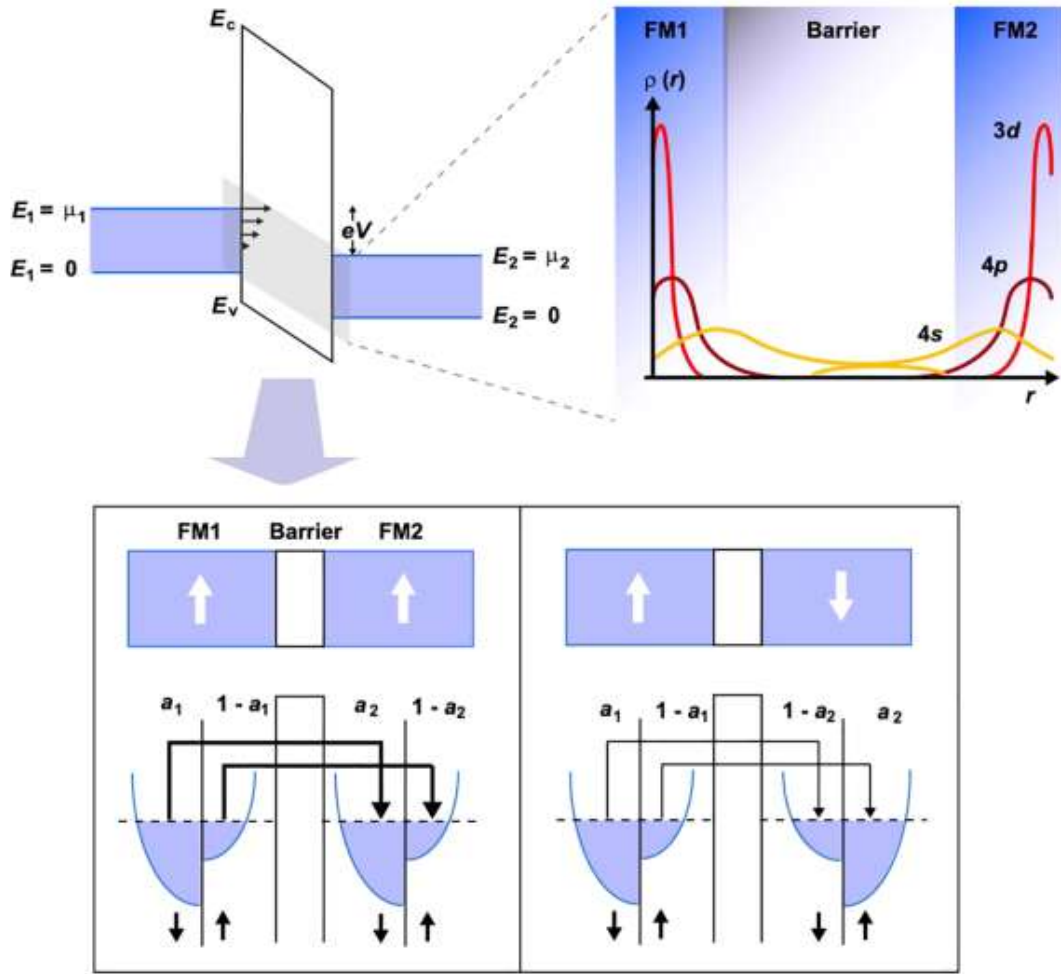


Figure 2.1: Spin-dependent tunneling of electrons in an MTJ while the magnetization directions in two FM layers are parallel (bottom left) and anti-parallel (bottom right) [52].

TMR is also defined in terms of polarization of the two FM layers as follows:

$$\text{TMR} = \frac{2P_1P_2}{1 - P_1P_2} \quad (2.6)$$

where  $P_1$  and  $P_2$  are the spin polarization of the two FM layers. They can be calculated from equation (2.4)(2.4). Increasing the value of TMR and the effect of defects on TMR has been a great research interest in recent years. The more the value of TMR, the more efficiently the two states of the MTJ block at any given voltage can be distinguished.

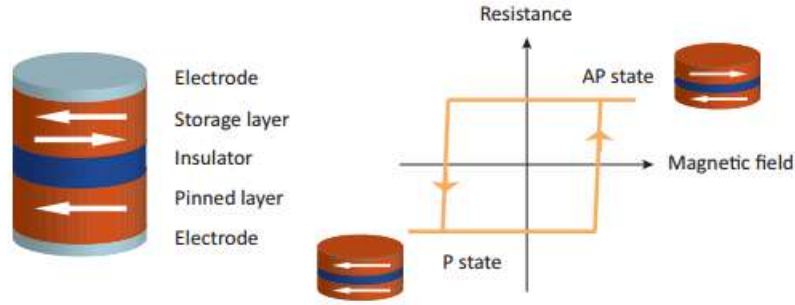


Figure 2.2: MTJ consists of three layers: two FM layer separated by an oxide barrier. The device resistance ( $R_P$  and  $R_{AP}$ ) depends on the corresponding state of the magnetization of the two FM layers, Parallel(P) or Anti-parallel (AP). The MTJ state can be switched by modulating the magnetic field [53].

## 2.5 MTJ Switching Mechanisms

The switching of the MTJ state can be realized by changing the spin magnetization orientation of the free layer. Several switching approaches have been proposed since the appearance of MTJ. For example:

- Field-induced magnetic switching (FIMS)
- Thermally assisted switching (TAS)
- Spin Transfer Torque (STT)
- Spin-Orbit Torque (SOT)

There are various versions of STT switching, like Spin Hall effect spin transfer torque, etc. However, in this thesis, we're discussing only Spin Transfer Torque MRAM (STT-MRAM), so we'll discuss the basic STT switching mechanism. In 1996 both Berger and Slonczewski independently predicted Spin Transfer Torque (STT) [9, 54]. STT switching mechanism is superior to other mechanisms like FIMS and TAS in case of better energy efficiency and scalability. STT switching method only requires a bidirectional current  $I$  higher than the threshold current to change the state of MTJ.

In MTJs, two types of magnetic switching occur due to spin transfer torque: precessional and thermally activated switching [14] [55]. Precessional switching occurs on a nanosecond time scale, while thermally activated switching occurs at a much larger time scale [56]. The transition between these two switching regions lies between 1 and 10 ns which is depicted in Fig.2.3. It was observed that a spin-polarized current injected perpendicularly to the plane transfers spin angular momentum to a local magnetization of the FM layer. Thus a large torque known as 'Spin Transfer Torque' is generated. This torque efficiently facilitates the magnetic manipulations of FM layers

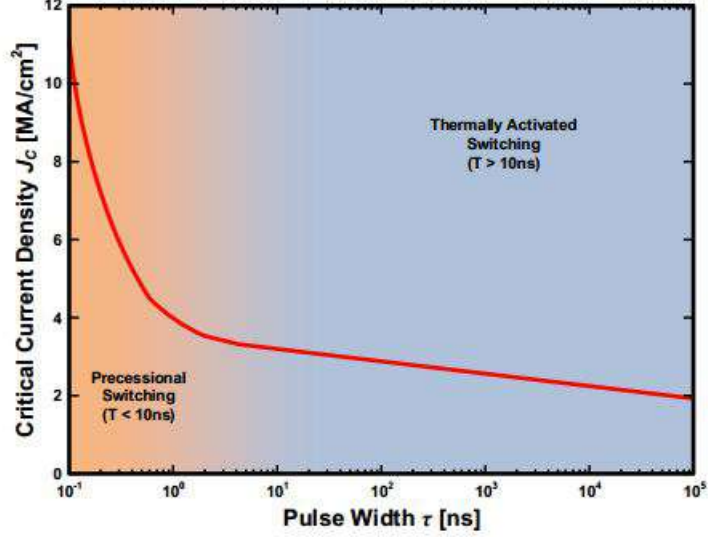


Figure 2.3: MTJ Switching Regimes [57].

in MTJ. If the current density is greater than the threshold value, the torque applied by the spin-polarized current will alter the magnetization of the free layer (FL) of MTJ [58].

In STT switching-based MTJ, the electrons injected into the pinned layer (PL) become spin polarized according to the spin of PL. Then these electrons tunnel through the oxide barrier. Then they transfer their angular momentum by applying a torque on the magnetization of FL as shown in Fig.2.4. To describe the switching of MTJ from an antiparallel configuration to a parallel configuration, a current is passed from the free layer to the fixed layer, which results in electrons flowing from the fixed layer to the free layer. The electrons in the fixed layer experience a torque, causing their spin magnetic moments to align with the magnetization of the fixed layer. Consequently, the current becomes spin-polarized along the direction of the fixed layer's magnetization. The magnetization of the fixed layer experiences an equal and opposite torque according to Newton's third law, but due to its rigidity, its magnetization is not significantly altered. The spin-polarized current then passes through the oxide barrier and enters the free layer. Next, the current's polarization encounters a torque that aligns it with the magnetization of the free layer. Concurrently, the magnetization of the free layer experiences an equal and opposite torque, which aligns it with the direction of the fixed layer. This process involves torque transfer between spins, and the torque experienced by the free layer due to the spin-polarized current is referred to as spin-transfer torque (STT).

To switch from a parallel configuration to an antiparallel configuration, the polarity of the voltage source must be reversed so that the now current flows from the fixed layer to the free layer, implying the electrons flow from the free layer to the fixed layer. When the electrons enter the free layer, their spins align with the magnetization of

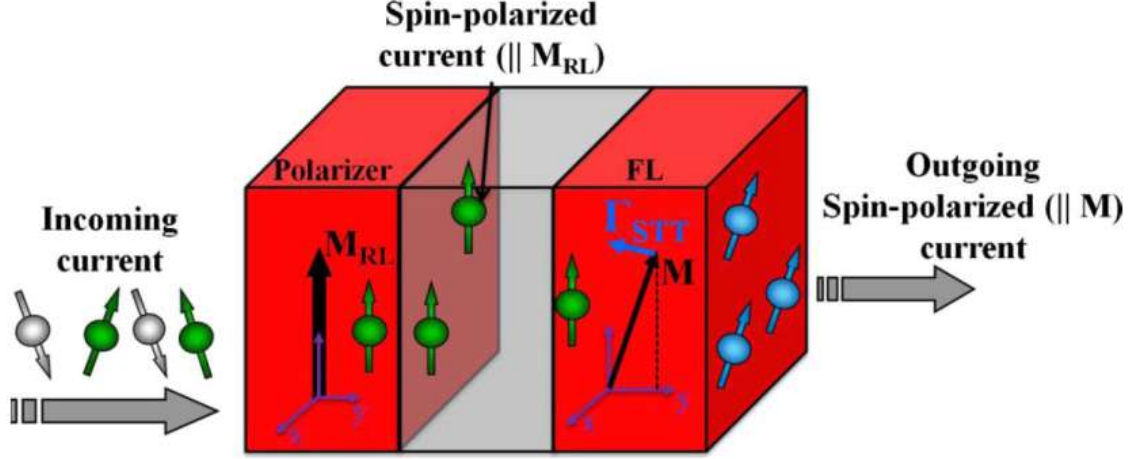


Figure 2.4: Spin Transfer torque switching mechanism from anti-parallel (AP) to parallel (P) configuration [61].

the free layer. They then traverse the oxide barrier before entering the fixed layer. Due to the fixed nature of the magnetization in this layer, the torque exerted by the spin-polarized current on the layer has no appreciable effect on the magnetization of the layer. Instead, a torque equal and opposite to the torque required to polarize the current acts on the free layer, eventually flipping the magnetization of the free layer and resulting in the two layers becoming antiparallel to one another [59,60]. The basic idea of STT devices can be described in a single domain model, which assumes that the layers are uniformly magnetized [15] [62]. The dynamics of the magnetization of FL can be described by a Landau-Lifshitz-Gilbert (LLG) equation, including the spin transfer torque term [63] [64] as the following equation:

$$\frac{\partial \vec{m}}{\partial t} = -\gamma \mu_0 \vec{m} \times H_{eff} + \alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t} - \beta J \vec{m} \times (\vec{m} \times \vec{m}_r) \quad (2.7)$$

The detail of this equation will be discussed in the modeling section. However, here the meaning of the equation will be discussed through a picture in Fig. 2.5. On the right-hand side of the equation, the first term represents the precession of the field-induced magnetization, and the second describes the intrinsic Gilbert damping torque, which reduces the precessional angle as a function of time and leads to the relaxation of the precession. The last term is the STT term with the opposite direction of the damping vector, which induces the switching of magnetization momentum. In such a current-induced magnetization switching of MTJ, the switching is determined by the competition between damping and STT term. For instance, if the STT term generated by a small current is relatively weaker than the damping term, then the magnetization direction remains unaltered. On the other hand, if the STT term generated by a higher current is stronger than the damping term, resulting in larger precessional angles and

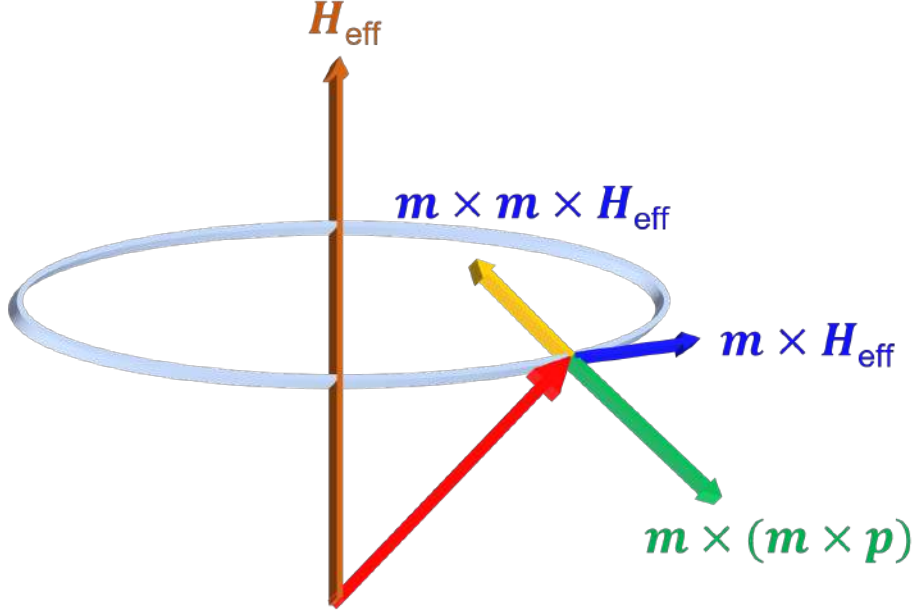


Figure 2.5: Illustration of different terms in LLGS equation

eventual state switching. The two regimes are distinguished by the threshold current, which is commonly known as critical switching current  $I_{c0}$ .

Switching occurs on a much longer time scale when the current through the MTJ is less than the critical switching current [14]. In the thermally activated regime, the switching current is a function of pulse duration  $\tau$ :

$$I_C = I_{C0} \left[ 1 - \frac{\ln(\tau/\tau_0)}{\Delta} \right] \quad (2.8)$$

where  $\Delta$  is the thermal stability of the MTJ,  $\tau_0$  is the natural time constant.

## 2.6 Modeling of MTJ

Small dimensionalities, in addition to the intrinsically stochastic switching properties of STT-MRAMs, make them highly susceptible to device-to-device and cycle-to-cycle variations. In order to study the origin of these variations, a physics model is required to capture the overall effects of the metal-insulator interface, defects, device dimension, and operating temperature. In this section, a physics-based model of MTJ considering the impact of interface and defects has been developed. The effect of current-induced joule heating, i.e., self-heating, is considered in chapter 4. First, the magnetization dynamics are captured by solving the Landau–Lifshitz–Gilbert–Slonczewski equation numerically, considering spin transfer torque (STT). Then the magnetization is used to compute the electrical property of the MTJ, such as resistance, current, etc., under

the application of bias voltage.

### 2.6.1 Magnetization Dynamics: LLGS Equation

As mentioned earlier, an MTJ consists of two ferromagnetic materials (free layer and reference layer) with an insulator in between them. The magnetization  $\vec{M}$  in a ferromagnet might change internally due to thermal excitation or external torque, but its magnitude is always equal to the saturation magnetization  $M_s$ . The precessional motion of magnetization  $\vec{M}$  of the free layer (FL) of an MTJ, in the presence of an external magnetic field  $\vec{H}_{\text{eff}}$ , can be very accurately modeled by the LLGS equation [9,38,65,66]. Initially, the equation was named LLG (Landau–Lifshitz–Gilbert) equation which predicts the dynamics of magnetization vector in the presence of torque. Later in 1996, John Slonczewski included an additional term to account for the spin transfer torque. The conventional way of writing the LLGS equation is as follows:

$$\dot{\mathbf{m}} = -\gamma \mathbf{m} \times \mathbf{H}_{\text{eff}} + \alpha \mathbf{m} \times \dot{\mathbf{m}} + \tau_{\parallel} \frac{\mathbf{m} \times (\mathbf{p} \times \mathbf{m})}{|\mathbf{p} \times \mathbf{m}|} + \tau_{\perp} \frac{\mathbf{p} \times \mathbf{m}}{|\mathbf{p} \times \mathbf{m}|} \quad (2.9)$$

where  $\mathbf{m} = \mathbf{M}/M_s$  is the unit vector of  $\mathbf{M}$ ,  $\mathbf{H}_{\text{eff}}$  is the effective magnetic field,  $\alpha$  is the dimensionless damping term,  $\tau_{\parallel}$  and  $\tau_{\perp}$  are the in-plane and perpendicular component of STT and  $\mathbf{p}$  is the unit vector along the polarization of the current [9]. To obtain a physical model, a modified version of eq. 2.9 is used:

$$(1 + \alpha^2) \dot{\mathbf{m}} = -\gamma (\mathbf{m} \times \mathbf{H}_{\text{eff}}) - \alpha \gamma (\mathbf{m} \times (\mathbf{m} \times \mathbf{H}_{\text{eff}})) - \frac{\eta \hbar J_e}{2et_{\text{FL}} M_s} ((\mathbf{m} \times (\mathbf{m} \times \mathbf{p}) - \alpha (\mathbf{m} \times \mathbf{p})) \quad (2.10)$$

The first term on the right-hand side of eq. 2.10 represents the magnetization precession around the effective magnetic field. The second term is the intrinsic Gilbert damping term which causes the magnetization to be relaxed in the state of minimum energy, i.e., parallel to the effective field, and also to keep the magnitude of the magnetization vector constant. The final two-term is included in the equation to describe the STT switching phenomenon. As the damping parameter  $\alpha$  is usually very small, the last term in eq. 2.10 is ignored. In order to switch the MTJ by utilizing the STT effect, the in-plane torque contributes more significantly than the perpendicular torque. So the equation used in this thesis is as follows:

$$(1 + \alpha^2) \dot{\mathbf{m}} = -\gamma (\mathbf{m} \times \mathbf{H}_{\text{eff}}) - \alpha \gamma (\mathbf{m} \times (\mathbf{m} \times \mathbf{H}_{\text{eff}})) - \frac{\eta \hbar J_e}{2et_{\text{FL}} M_s} (\mathbf{m} \times (\mathbf{m} \times \mathbf{p})) \quad (2.11)$$

The definitions of the variables used in eq. 2.11 are as follows:

- $\mathbf{m}$  is the unit Magnetization vector of the free layer



- $\mathbf{p}$  is the unit Magnetization vector of the pinned or reference layer. It is also the spin-polarization direction.
- $\mathbf{H}_{\text{eff}}$  is the effective magnetic field. Its different components are discussed in later sections.
- $\gamma$  is the gyromagnetic ratio
- $\eta$  is the torque efficiency factor and is defined by:  $\eta = \frac{P^2}{2(1+P^2 \cos \theta)}$  where  $\theta$  is angle between  $\mathbf{m}$  and  $\mathbf{p}$  and  $P$  is the polarization factor and  $M_s$  is the saturation magnetization
- $J_e$  is the device current density
- $t_{\text{FL}}$  is the thickness of Free layer
- $e$  is electron charge and  $\hbar$  is the reduced Planck's constant.

The different terms of the eq. 2.11 are shown in Fig. 2.5.

### 2.6.2 Effective Magnetic Field

The effective magnetic field  $\mathbf{H}_{\text{eff}}$  is given by:

$$\mathbf{H}_{\text{eff}} = \mathbf{H}_{\text{ext}} + \mathbf{H}_{\text{dem}} + \mathbf{H}_{\text{an}} - \mathbf{H}_{\text{VCMA}} + \mathbf{H}_{\text{th}} \quad (2.12)$$

where,

$\mathbf{H}_{\text{ext}}$  is the external applied magnetic field

$\mathbf{H}_{\text{an}}$  is the magnetocrystalline anisotropy field

$\mathbf{H}_{\text{dem}}$  is the demagnetization field

$\mathbf{H}_{\text{VCMA}}$  is the voltage controlled magnetic anisotropy field

$\mathbf{H}_{\text{th}}$  is the effective contribution of thermal noise.

### 2.6.3 Demagnetization Field

The demagnetization field (shape anisotropy) varies with the geometry of the free layer and is modeled as  $\vec{H}_{\text{dem}} = N\vec{M}$ . If the free layer is assumed to be a very flat ellipsoid,

the factors of the demagnetization tensor  $N$  (which was calculated by Osborn) [67] are:

$$\begin{aligned}
N_x &= \frac{d}{L} (1 - e^2)^{1/2} \frac{K - E}{e^2} \\
N_Y &= \frac{d}{L} \frac{K - (1 - e^2) E}{e^2 (1 - e^2)^{1/2}} \\
N_z &= 1 - \frac{d}{L} \frac{E}{(1 - e^2)^{1/2}} \\
e &= \left( 1 - \frac{W^2}{L^2} \right)^{1/2}
\end{aligned} \tag{2.13}$$

where  $K$  and  $E$  are the complete elliptic integrals of the first and second kinds whose argument is  $e$ .

#### 2.6.4 Voltage Controlled Magnetic Anisotropy

In the case of STT-MRAM, the effect of  $\vec{H}_{VCMA}$  is very insignificant in case of STT-MRAM. However, the equation for  $\vec{H}_{VCMA}$  is given by:

$$\vec{H}_{VCMA} = \frac{2\zeta V}{\mu_0 M_s t_{ox} d} m_z \hat{z} \tag{2.14}$$

$$\vec{H}_{an} = \frac{2K_i}{d\mu_0 M_s} m_z \hat{z} \tag{2.15}$$

$K_i$  is the perpendicular magnetic anisotropy constant,  $\zeta$  is the VCMA constant,  $V$  is the voltage across the MTJ, and  $t_{ox}$  is the thickness of the oxide layer. Both the terms are in the  $z$ -direction, and their strength is proportional to  $m_z$ , and the VCMA term subtracts from the PMA term in  $\vec{H}_{eff}$ .

##### 2.6.4.1 Thermal Noise

The final component of the effective magnetic field is the thermal noise  $\vec{H}_{th}$ , which causes random fluctuations in the free layer magnetization. It is given by:

$$\vec{H}_{th} = \vec{\sigma} \sqrt{\frac{2\alpha k_B T}{\mu_0 M_s \gamma V \delta t}} \tag{2.16}$$

where,  $k_B$  is Boltzmann's constant,  $T$  is the absolute temperature in K,  $V$  is the volume of the free layer, and  $\delta t$  is the simulation time setup.  $\vec{\sigma}$  is a unit vector whose  $x$ ,  $y$ , and  $z$  components are uncorrelated Gaussian random variables with zero mean

and unity standard deviation. Due to this thermal noise-induced field, the switching phenomenon in MTJ becomes probabilistic, which enables the utilization of MTJ in probabilistic and neuromorphic computing.

### 2.6.5 Resistance Calculation

As previously mentioned in Chapter 1, an MTJ can act as a low and high resistance depending on the relative orientation of the free layer and reference layer. The parallel resistance ( $R_P$ ) of an MTJ is independent of the bias voltage and is given by the following formula [68, 69]:

$$R_P = \frac{t_{\text{ox}}}{F \times \bar{\phi}^{1/2} \times A} \times \exp\left(\frac{2t_{\text{ox}}(2me\bar{\phi})^{1/2}}{\hbar}\right) \quad (2.17)$$

where  $t_{\text{ox}}$  is the thickness of oxide layer,  $\bar{\phi}$  is the oxide barrier height  $F$  is the fitting parameter,  $A$  is the area of the device,  $m$  and  $e$  are the electron mass and charge respectively. For a fixed barrier height and fixed oxide thickness the right hand side of the eq. 2.17 is constant and this is the  $RA$  product of an MTJ. Usually an MTJ is specified by its  $RA$  product and its  $TMR$ . So for a fixed oxide thickness and fixed barrier height,  $R_P$  can be obtained by the  $RA$  product and its area. The anti-parallel resistance ( $R_{AP}$ ) is bias-dependent through the TMR. The bias-dependent TMR is given by [70]:

$$TMR(V) = \frac{TMR(0)}{1 + (V/V_h)^2} \quad (2.18)$$

where  $TMR(0)$  is the TMR at zero bias and  $V_h$  is the voltage at which the  $TMR(V)$  is equal to the half of  $TMR(0)$ . The bias dependent resistance  $R_{MTJ}$  as a function of voltage and magnetization orientation is given by [69]:

$$R_{MTJ}(V_b) = R_P \frac{1 + (V_b/V_h)^2 + TMR(0)}{1 + (V_b/V_h)^2 + TMR(0)[0.5(1 + \cos \theta)]} \quad (2.19)$$

where  $\theta$  is the angle between  $\mathbf{m}$  and  $\mathbf{p}$  vectors. To capture the self-heating effect, a 3D heat diffusion equation is solved with proper boundary conditions. The details are described in chapter 4. In the theoretical framework described above, which is based on the Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation, a key assumption is that the free layer (FL) and fixed layer (RL) can be treated as monodomain magnets. This can be justified due to the smaller dimension of the layers. Any magnet with a dimension below 100 nm can be assumed to be a monodomain magnet. In our simulation, the considered FL and RL have diameters ranging from 60 to 80 nm. So the LLGS based formalism is justified.

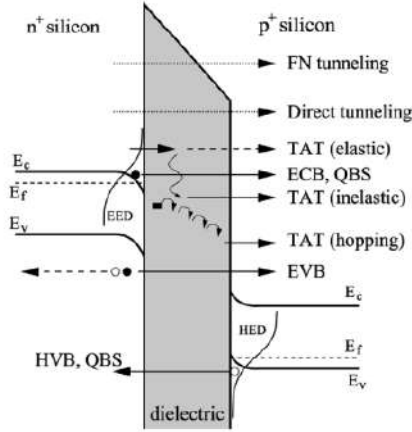


Figure 2.6: Tunneling processes in a MOS transistor [75].

### 2.6.6 Trap Assisted Tunneling (TAT)

To obtain the trap-assisted current, it is assumed that the traps are non-magnetic and invariant under spin transport. Here, I'll briefly discuss the theory of trap-assisted tunneling. Important parameters that play pivotal roles in trap-assisted tunneling are: i) Energy barrier that the charge carriers need to overcome, ii) trap occupancy dynamics, and iii) trap density and distribution [71–75]. Trap-assisted tunneling (TAT) is usually a two or more-step process. These traps are generally assumed to be in the insulating layer. Traps usually provide a discrete energy level in the forbidden band gap region of a material which leads not only to non-radiative recombination but also the passage of carriers through an energy barrier. Hopping, elastic and inelastic types of TATs are usually considered in various models. In the elastic process, the carriers tunnel through the barrier, maintaining the same energy level. On the other hand, in an inelastic process, the tunneling is assisted by emitting a phonon. So the energy of the trap is lower than the carrier. Different types of tunneling processes are shown in Fig. 2.6.

#### 2.6.6.1 Different Models of TAT

Chang et al. proposed a generalized TAT model which formulates TAT current density as follows [76, 77]:

$$J = q \int_0^{t_{diel}} AN_T(x) \frac{P_1(x)P_2(x)}{P_1(x) + P_2(x)} dx \quad (2.20)$$

where  $A$  denotes a fitting constant,  $N_T(x)$  is the spatial trap concentration, and  $P_1$  and  $P_2$  are the transmission coefficients of electrons captured and emitted by traps.

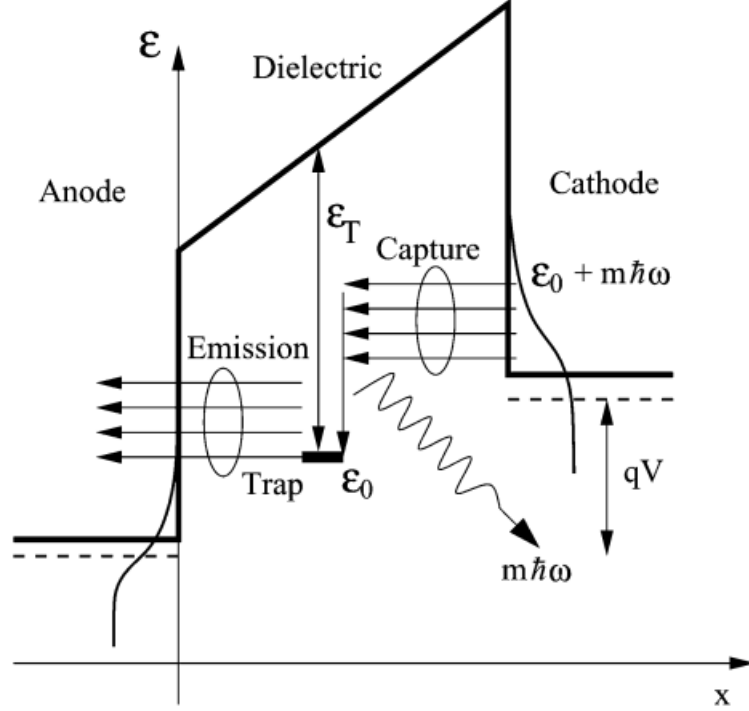


Figure 2.7: Inelastic phonon emission model of trap assisted tunneling. Electrons, after being captured from the cathode, are relaxed to the trap energy level by phonon emission and then emitted to the anode [75,81].

Generally, TAT models combine the idea of carrier capture and emission phenomena with tunneling. Ielmini et al. proposed a model that combines inelastic TAT and hopping conduction [78,79] whose formula is given by:

$$J = \int_0^{t_{\text{diel}}} dx \int_{E_{\text{min}}}^{E_{\text{max}}} \tilde{J}(E_T, x) dE \quad (2.21)$$

where  $\tilde{J}$  is the net current flowing through the dielectric, which is the difference between capture and emission currents through the left and right sides of the barrier.

$$\begin{aligned} \tilde{J}(E_T, x) &= J_{\text{cl}} - J_{\text{el}} = J_{\text{er}} - J_{\text{cr}} \\ &= qN_T W_c \left( 1 - \frac{f_T(E_T, x)}{f_1(E_T, x)} \right) \end{aligned} \quad (2.22)$$

where  $f_T$  is the trap occupancy,  $E_T$  is the trap energy,  $W_c$  capture rate and  $f_1$  is the energy distribution function at the left interface. In Ginestra<sup>TM</sup> [80], a multiphonon-emission trap-assisted tunneling model is used. This model has been proposed by Herrmann and Schenk [81]. The process is shown in Fig. 2.7. In this process, electrons lose energy after capturing from the cathode and emit phonons with energy  $m\hbar\omega$ . Hence, they relax to the energy of the trap and then are emitted to the anode. The TAT current is given by:

$$J_t = q \int_0^{t^{\text{diel}}} \frac{N_T(x)}{\tau_c(x) + \tau_e(x)} dx \quad (2.23)$$

where  $N_T(x)$  is the trap concentration and  $\tau_c(x)$  and  $\tau_e(x)$  denote the capture and emission times calculated from

$$\begin{aligned} \tau_c^{-1}(z) &= \int_{\mathcal{E}_0}^{\infty} c_n(\mathcal{E}, x) T_l(\mathcal{E}) f_l(\mathcal{E}) d\mathcal{E} \\ \tau_e^{-1}(z) &= \int_{\mathcal{E}_0}^{\infty} e_n(\mathcal{E}, x) T_r(\mathcal{E}) (1 - f_r(\mathcal{E})) d\mathcal{E}. \end{aligned} \quad (2.24)$$

Here,  $c_n$  and  $e_n$  are the capture and emission rates respectively,  $f_l$  and  $f_r$  denote the Fermi distributions,  $T_l$  and  $T_r$  are the transmission coefficients from the left and right side of the dielectric. TAT current is computed in Ginestra<sup>TM</sup> in the framework of

Table 2.2: Defect parameters used to calculate trap current and comparison with ab-initio calculations and experiments.

| Parameters       | Value Used | Ab-initio Calculations/Experimental Results |
|------------------|------------|---|
| $E_T$            | 3.2 eV     | 3.3 eV (F <sup>+</sup> *) [82]              |
|                  |            | 3.2 eV (F <sup>+</sup> *) [83]              |
|                  |            | 3.4 eV (Bulk F <sup>0</sup> ) [84]          |
| $E_{\text{rel}}$ | 1 eV       | 0.9 eV [84]                                 |

the multiphonon TAT theory [80, 85–88]. The Kinetic Monte Carlo method is used to generate the random distribution of traps in the insulating layer. Additionally, the TAT model considers the displacements of lattice atoms that surround the defect sites due to charge trapping and emission. This process is inherent to the atomistic structure of the traps. The relaxation energy  $E_{\text{rel}}$  controls the charge capture and emission processes and the thermal dependence of TAT [89, 90]. In this work, neutral (F<sup>0</sup>) and singly charged (F<sup>+</sup>\*) oxygen vacancies are considered as traps/defects in the oxide layer. The considered relaxation energy  $E_{\text{rel}}$  and thermal ionization energy  $E_T$  of considered defects are given in table 2.2.

# CHAPTER 3

## DEVICE-TO-DEVICE VARIABILITY IN

### STT-MRAM

Small dimensionalities and inherently stochastic switching properties of STT-MRAMs make them substantially more susceptible to fluctuations from one device to another and from cycle to cycle. The majority of earlier research on STT-MRAM variability concentrated on process, temperature, and operating conditions in magnetic tunneling junction (MTJ)/CMOS circuits or arrays [30–33, 91–93]. Even though significant insights on the variability and reliability of STT-MRAMs have been obtained from these studies, the ongoing drive towards utilizing highly scaled variants of these devices for memory, as well as neuromorphic applications, necessitates variability analysis from a microscopic point of view.

In particular, there are facets relating to the role of interface quality and defects on the device-to-device variation that needs to be investigated in detail to have a better understanding of the source of variability in these devices. This will allow for a better understanding of the source of variability in these devices.

In this chapter, we present a simulation framework validated by the experimental results reported in the literature for analyzing and investigating the variability of standalone CoFeB/MgO MTJs taking into account the role of defects, interface quality, operating temperature, and dimensions of the devices. In contrast to previous studies, which incorporated defects as resistive shorts or opens in equivalent circuit models of STT-MRAMs [31], [37], this work employs multiscale simulation and ab-initio calculations which relate microscopic/atomistic properties of a device to its spintronic output characteristics. The results of this work indicate that WRITE cycles of STT-MRAMs are more susceptible to variations induced by interface quality than READ cycles. This work also correlates effective energy barrier height with the interface quality of these devices and shows that it can be exploited to predict device-to-device variabilities of STT-MRAM devices.

### 3.1 Description of the Simulation Framework

Based on the equations presented in chapter 2, a simulation framework has been developed to capture the behavior of an MTJ. The model has been validated with the experimental data presented in [94]. The details of the experimental setup are beyond the scope of this thesis. The overall simulation framework is given in Fig. 3.1. As previously mentioned in chapter 2, the LLGS equation is solved to calculate spin-dependent direct tunneling current ( $I_{\text{spin}}$ ), taking into account temperature and voltage dependence of tunneling magnetoresistance (TMR). Trap-assisted tunneling current ( $I_{\text{trap}}$ ) is calculated using Ginestra<sup>TM</sup>, which performs statistical simulation by randomly generating every device and its constituent oxygen vacancies in the MgO layer, and applies the Kinetic Monte Carlo simulation technique to account for the stochastic nature of charge transport. The total current ( $I_{\text{total}}$ ) resulting from  $I_{\text{spin}}$  and  $I_{\text{trap}}$  in effect influences the overall magnetic switching characteristics, thereby creating a self-consistent loop.

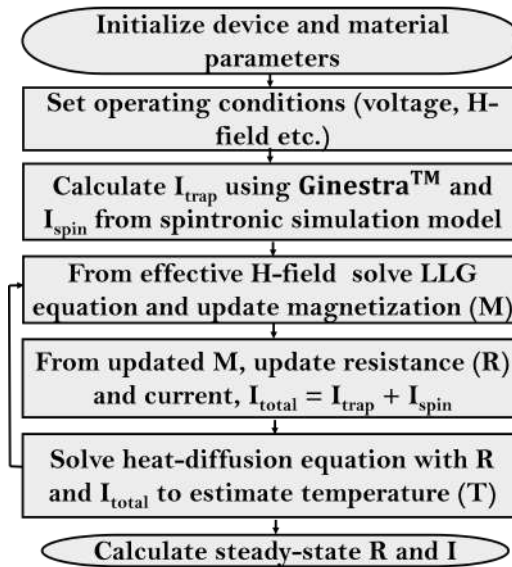


Figure 3.1: Flowchart of the developed simulation framework

## 3.2 Results and Discussions

### 3.2.1 Experimental Reports on Device-to-Device Variability

Several researches reported on the variability of electrical characteristics of STT-MRAM such as R-V loop, R-H loop, and TMR-voltage curve for different operational conditions [26, 32, 33, 91]. The experimental results reported in [94] are considered in



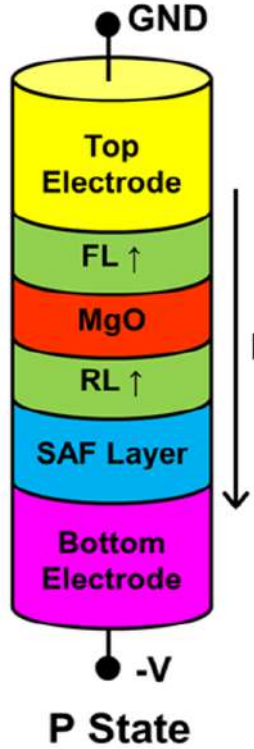


Figure 3.2: Schematic illustration of considered MTJ pillar.

this thesis for the variability study of MgO based STT-MRAM stack. CoFeB/MgO STT-MRAM stack was deposited by magnetron sputtering on 300 mm Si wafers. The MTJ pillars tested had circular cross-sections with nominal diameters of 60, 70, and 80 nm, as shown in Fig. 3.2. MgO thickness was around 1 nm. The device cross-sectional area was about 15 to 20 times larger than the MgO sidewall area, which ensured that the influence of sidewall on device variability was negligible. For the variability study, 15-20 devices of each diameter were fabricated on the same wafer. Variation in the measured R-V characteristics was observed (percentage standard deviation ranging from 5-7%). Also, the considered devices were located in the central dies of the wafer, and RA non-uniformity is expected to be small-typically within  $\pm 0.2\Omega - \mu\text{m}^2$ . The device-to-device variabilities in the measured R-V loops for devices with 60 nm diameter are shown in Fig. 3.3. Similar variations are observed for devices of 70 and 80nm diameters as well.

### 3.2.2 Analysis of Origin of the Device-to-Device Variability

Now we'll look into the possible origins of device-to-device variability of STT-MRAMs. The factors which come into the analysis of the experimental results can be broadly categorized as:

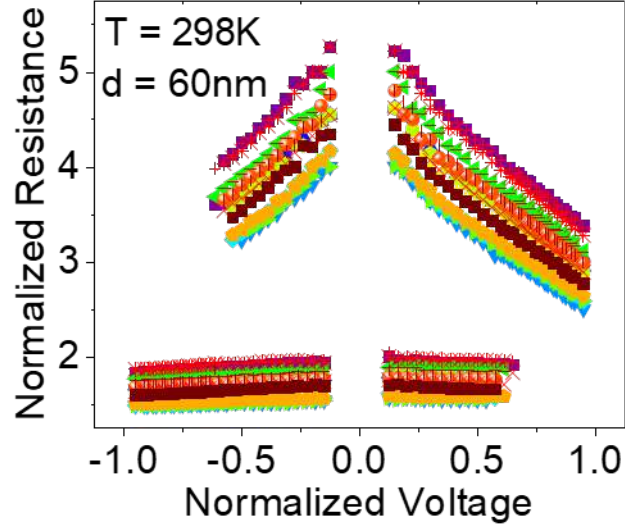


Figure 3.3: Measured R-V loops of  $d = 60$  nm devices fabricated on the same wafer [94].

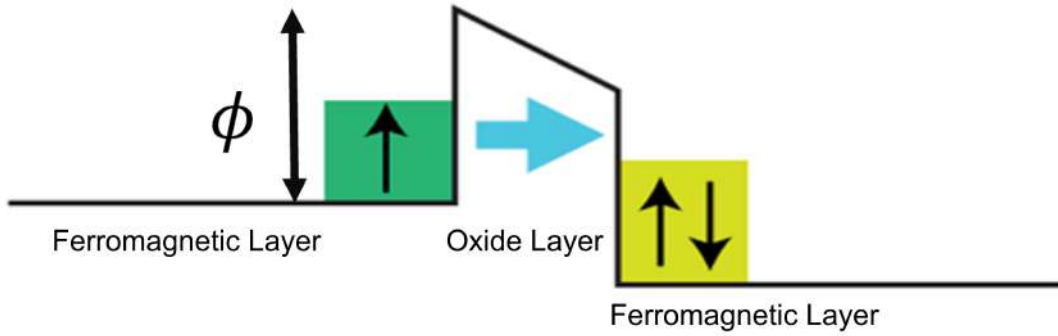


Figure 3.4: Schematic of the definition of Oxide Barrier Height.

- Material Parameters
- Geometrical Parameters
- Fitting Parameters

### 3.2.2.1 Effect of Oxide Barrier Height

A parameter fundamental to the estimation of parallel spin-state resistance of an STT-MRAM is the oxide barrier height,  $\phi$ , as included in eq. 2.17 and shown in 3.4. For MgO-based MTJ devices, the reported energy barrier heights range from 0.39-1.2eV [82,95–97], even though the ideal barrier height of bulk MgO is 3.7eV [98]. Such deviation of  $\phi$  from the ideal value hints towards the significant influence of interface quality on the electronic properties of ultra-thin MgO tunnel barriers in MTJs. In fact, ab-initio calculations and experimental results suggest that spatial penetration

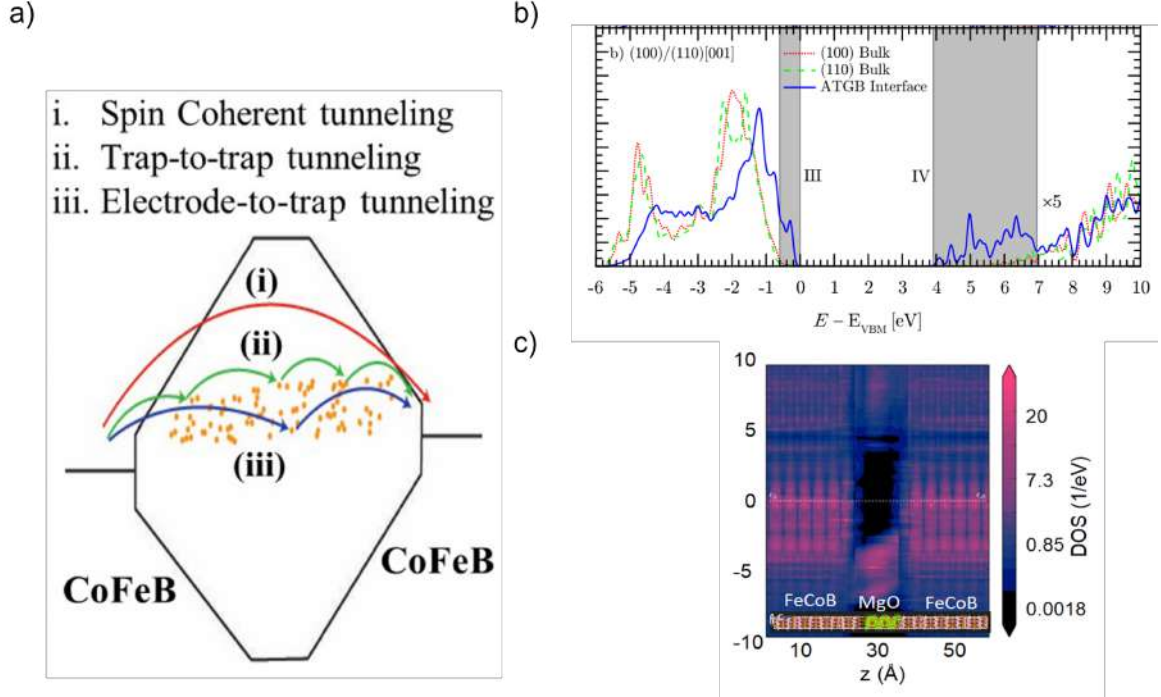


Figure 3.5: a) Proposed Band diagram of the MTJ device involving MIGS. b)-c) Reported Ab-initio calculations showing the density of states (DOS) in CoFeB/MgO/CoFeB [94, 102].

of metal wave functions as well as hybridization of electronic states arising from the defects may lead to the formation of gap states in the tunnel barrier. Such states, which are known as metal-induced gap states (MIGS), effectively reduce the MgO bandgap at the CoFeB/MgO interface [99–101]. To incorporate the effect of MIGS, the present simulation framework considers a gradually varying energy band profile (Fig. 3.5 a)). This is in accordance with previous spectroscopic and first principle calculation-based reports [102–104], which suggest gradual as well as local change of MgO bandgap because of intermixing and interdiffusion between tunnel barrier and magnetic contact layers.

In fact, Jonathan et al. [102] reported from first principle calculations using HSE06 exchange functionals that there exists a wide band of states in the 2 eV window below the bulk conduction band minimum, which effectively reduces the band gap at the grain boundaries of CoFeB/MgO interface. To look into this, the reported Projected Density of states (PDOS) of the CoFeB/MgO/CoFeB interface is shown in Fig. 3.5 [94, 102](b) and (c) [94, 102]. This shows the existence of energy states within the barrier height of the bulk MgO. Good agreement between numerical simulations and experimental results are obtained for all three diameters of the STT-MRAMs considering such band profiles (Figs. 3.6(a)-(c)). The effective value of average  $\phi$  extracted for these devices is 1.25eV. A comparison of these values with ab-initio simulation results is shown in table 3.1. To look into the impact of microscopic barrier height on device-to-device

Table 3.1: Average Barrier Height Used to calculate  $R_p$  and comparison with ab-initio calculations and experiments

| Parameter | Value Used | Ab-initio/Experimental Values                     |
|-----------|------------|---|
| $\phi$    | 1.25 eV    | 1.1-1.7 eV (CoFe/Fe/MgO/CoFe, CoFe/MgO/CoFe) [96] |
|           |            | 0.39 eV (Fe/MgO/Fe) [95]                          |
|           |            | 0.45-0.49 eV (CoFeB/MgO/CoFeB) [97]               |
|           |            | 1.2 (P) - 0.8 (AP) eV (CoFeB/MgO/CoFeB) [82]      |

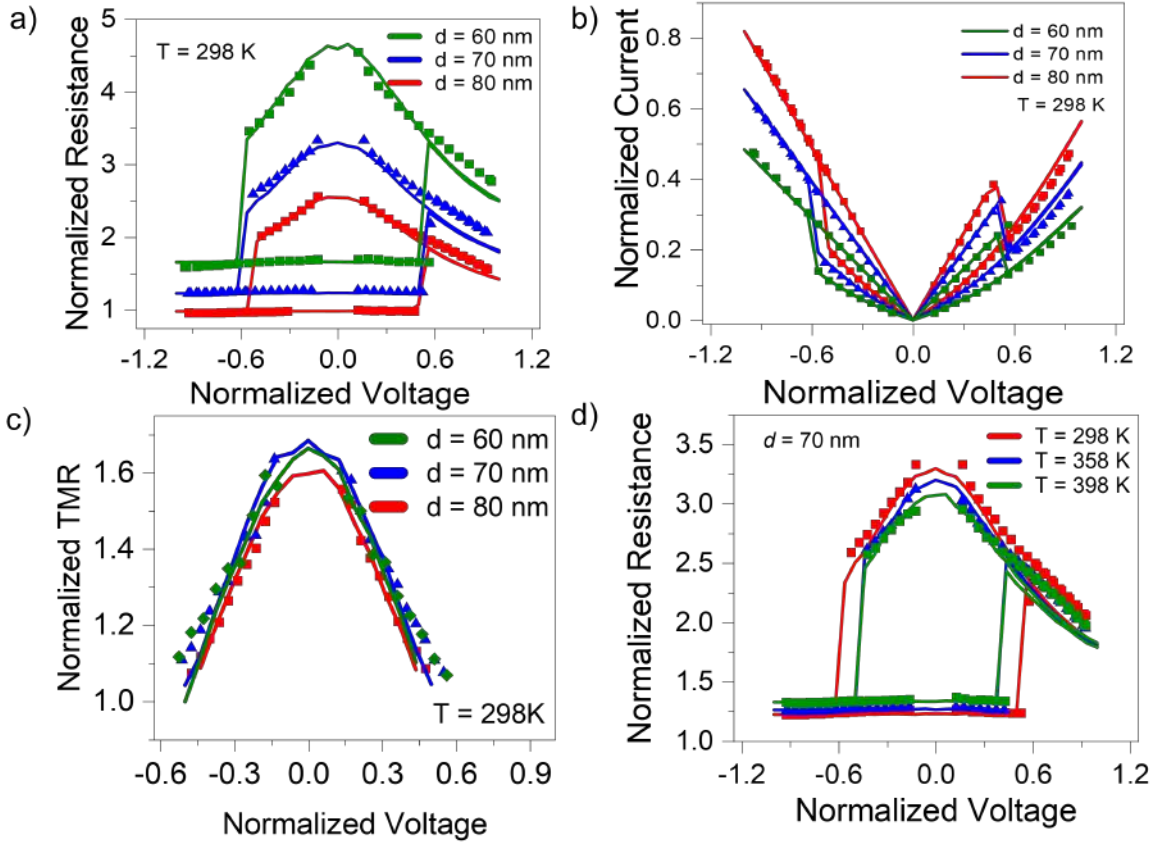


Figure 3.6: Measured (symbols) and simulated (lines) results of (a) R-V loops and (b) I-V loops (c) TMR vs. voltage characteristics and (d) R-V loops at different temperature for  $d = 70$  nm.

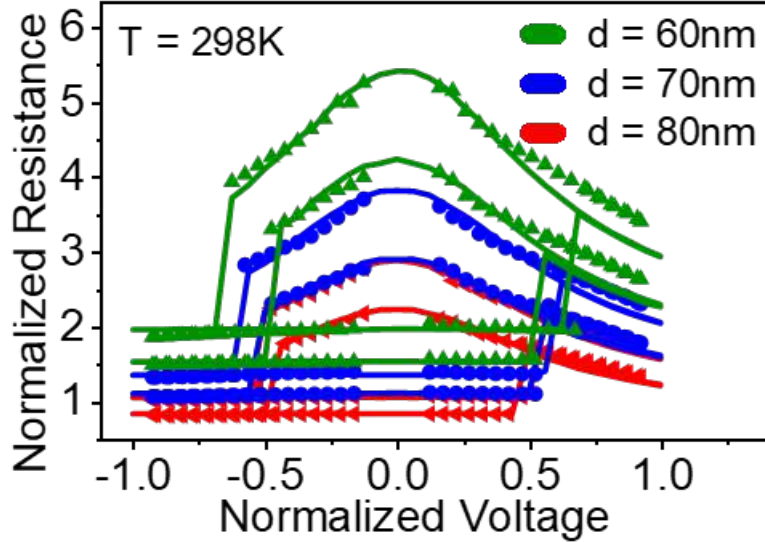


Figure 3.7: Measured (symbols) and simulated (lines) R-V loops for highest and lowest resistance values of each diameter.

Table 3.2: Extracted values of  $\phi$ , and measured percentage (%) variation and percentage standard deviation ( $\% \sigma$ ) of  $R_p$  and  $R_{AP}$ .

| Diameter, d (nm) | Extracted $\phi$ (eV) | % Variation of $\phi$ | % Variation of |          | % $\sigma$ of |          |
|------------------|-----------------------|-----------------------|----------------|----------|---------------|----------|
|                  |                       |                       | $R_p$          | $R_{AP}$ | $R_p$         | $R_{AP}$ |
| 60               | 1.20-1.35             | 12.5                  | 28.4           | 27.8     | 8.5           | 8.3      |
| 70               | 1.19-1.31             | 10.1                  | 21.7           | 31.8     | 7.5           | 8.4      |
| 80               | 1.17-1.32             | 12.8                  | 26.4           | 29.5     | 6.3           | 6.9      |

variability, R-V loops with the highest and lowest resistance values for each diameter of the devices are analyzed as shown in Fig. 3.7. The extracted values of  $\phi$  for these devices with extreme R-V loops for different diameters are given in table 3.2.

From the extracted values of  $\phi$ , we see that the range of  $\phi$  is almost the same for different diameters, and the values do not show any specific monotonic behavior. This hints at any uncorrelated relation of  $\phi$  with diameters. However, it is noteworthy that the parallel ( $R_p$ ) and anti-parallel ( $R_{AP}$ ) resistances vary up to about 28% and 32% respectively, over this extracted range of  $\phi$ . In fact, both  $R_p$  and  $R_{AP}$  exhibit increasing behavior with  $\phi$ . This is evident from table 3.2 and also from equation 2.17. Also, Fig. 3.8 shows that the switching voltage is positively correlated to  $\phi$  such that 0.2eV variation of  $\phi$  results in about 43% variation of switching voltage. However, the TMR of these devices however essentially remains constant over this range of  $\phi$ .

TMR is a significant parameter of an STT-MRAM which indicates how well the two states of the device can be distinguished during the read cycle. The read voltage of STT-MRAMs is typically within 0.01-0.20V, and for such small voltages, the devices

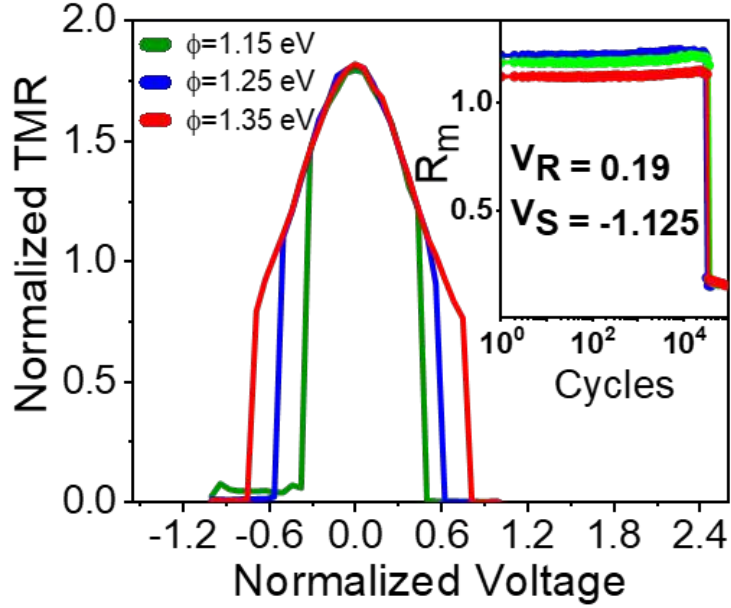


Figure 3.8: Effect of  $\phi$  on TMR of the device; inset shows  $R_m$  obtained for multiple READ cycles during TDDB measurements where  $V_R$  and  $V_S$  refer to normalized READ and stress voltages respectively.

show similar resistance values after multiple READ cycles. This is further illustrated in the inset of Fig. 3.8, which shows as an inset the minimum value of normalized parallel resistance ( $R_m$ ) obtained from consecutive READ cycles during TDDB measurement of three devices having identical diameters [40, 94, 105]. Even in the presence of a stress voltage much higher than the READ voltage, a %  $\sigma$  variation of only about 0.7% is obtained for  $R_m$ . Such variation corresponds to a change of energy barrier height by only about 20 meV. This, along with the constant behavior of TMR with different  $\phi$  indicates that variation of energy barrier height has minimal effect on READ cycles. To investigate the impact of operating temperature on the variability of  $\phi$ , R-V loops of different operating temperatures and the corresponding extracted  $\phi$  values are analyzed. The extracted values of  $\phi$  suggest that for a 100° C change of temperature, the energy barrier height changes only by about 10-20meV. Consequently, temperature variation over such a range has a negligible effect on the variability of these devices, as shown in Fig. 3.9.

### 3.2.2.2 Effect of Trap Assisted Current on R-V Loops

To understand whether device-to-device variability in MTJs is governed more by the density and distribution of defects rather than by the slight change of energy barrier height resulting from material and interfacial properties, trap-assisted tunneling currents have been calculated considering different density and spatial distributions of bulk defects. However, it is observed from Fig. 3.10 that for all defect densities,  $I_{\text{trap}}$



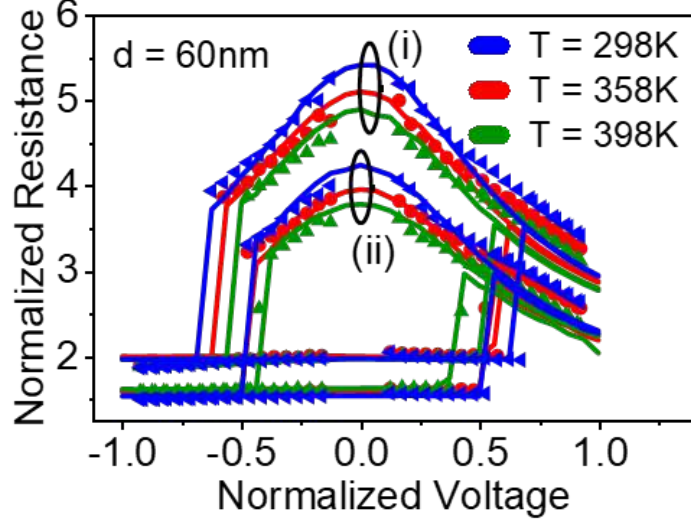


Figure 3.9: Effect of operating temperature variation on R-V loops corresponding to extracted values of (i)  $\phi = 1.35\text{-}1.36\text{ eV}$  and (ii)  $\phi = 1.20\text{-}1.23\text{ eV}$

remains about two orders of magnitude smaller than  $I_{\text{spin}}$ , thereby having minimal effect on the R-V characteristics.

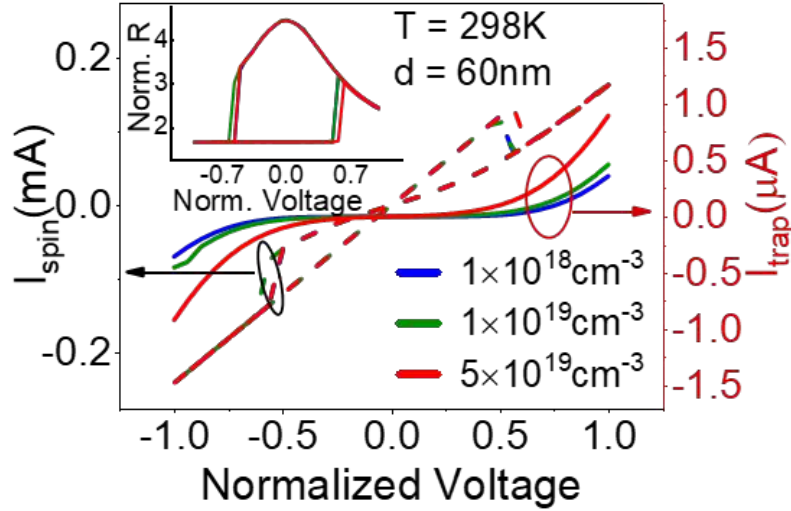


Figure 3.10: Comparison of spin (solid lines) and trap current (dashed lines) densities for different concentrations of bulk defects (effect on R-V loop shown as inset).

Therefore, variability in these devices primarily arises from interface quality, which manifests itself in the MIGS-induced lowering of  $\phi$ . To further elucidate this aspect, a statistical simulation of 25 devices is performed in Ginestra<sup>TM</sup> considering the uniform spread of the spatially varying bandgap of MgO. As shown in Fig. 3.11, the results of the statistical simulation are well within the range of trap current calculated using the extracted values of  $\phi$ . These results further validate the use of an effective barrier to correctly represent the gradually varying band profile.

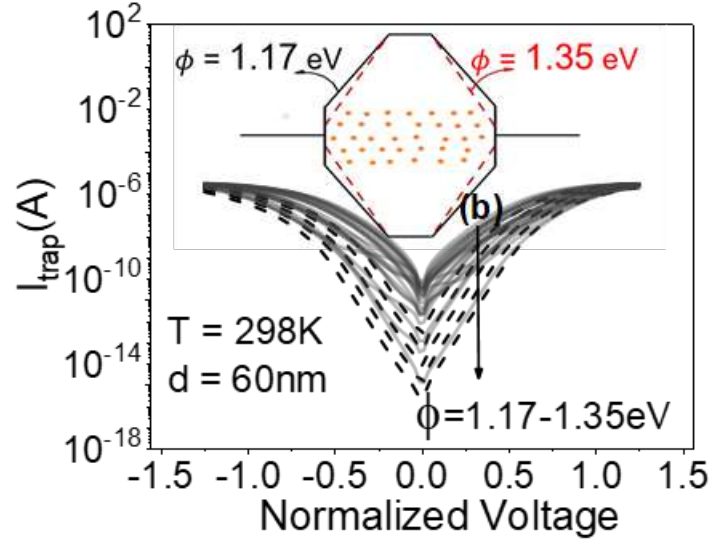


Figure 3.11: Trap currents calculated from linear (dashed lines) and statistical (solid lines) variation of  $\phi$ ; inset shows energy band diagram illustrating the physical significance of  $\phi$ .

### 3.2.2.3 Effect of Oxide thickness on Device Variability

Due to process variation and other fabrication artifacts, it's not possible to fabricate devices with the exact oxide thickness of 1 nm. So oxide thickness variability is another source of variation that can give rise to device-to-device variability for fixed-diameter devices. To look into whether the oxide thickness variation is the primary and sole source of variation of these devices, the cumulative distribution function (CDF) of  $R_P$  and  $R_{AP}$  of the corresponding devices is calculated. Fig. 3.12 and 3.13 show the CDF plot of zero-bias  $R_P$  and  $R_{AP}$  considering statistical variation of  $t_{ox}$ . In the case of  $R_P$ , all the devices have the same  $\phi$  values, and for  $R_{AP}$ , the corresponding  $\phi$  values are shown in the figure. These figure show that statistical variation of oxide thickness ( $t_{ox}$ ) alone cannot accurately predict device-to-device variability if a fixed value of  $\phi$  is considered for all devices.

However, as shown by solid lines, experimental results for all three diameters of the devices fit well with statistical analysis of energy barrier heights of corresponding devices are duly considered. These results establish the significance of effective barrier height as a figure of merit of the interface quality of ultra-scaled STT-MRAMs and provide evidence that it can be utilized to predict WRITE cycle device-to-device variability.



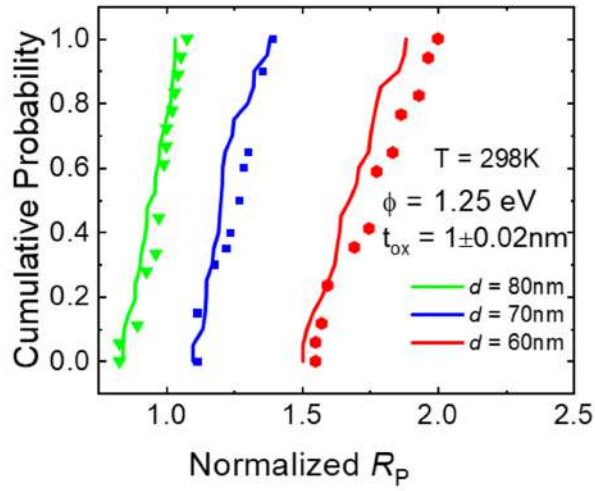


Figure 3.12: CDF plot of zero-bias  $R_p$  considering the statistical variation of  $t_{ox}$  (experimental results shown as symbols whereas dashed lines show fits with a fixed value of  $\phi = 1.25$  eV for all devices)

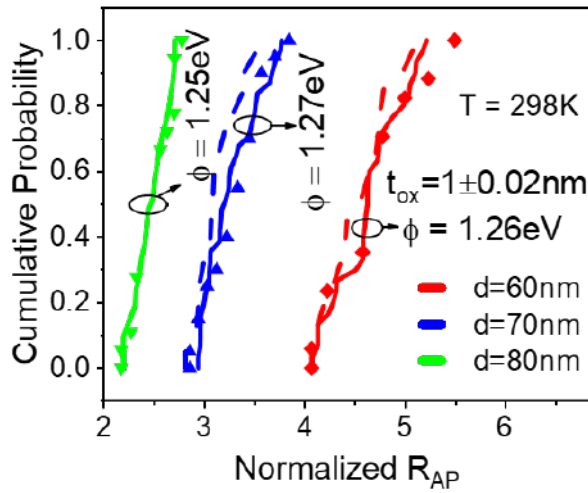


Figure 3.13: CDF plot of zero-bias  $R_{AP}$  considering the statistical variation of  $t_{ox}$  (experimental results are shown as symbols whereas dashed lines show fits with a fixed values of  $\phi = 1.25$  eV and continuous line shows fit with corresponding values of  $\phi$  for all devices)

# CHAPTER 4

## VARIABILITY OF SELF-HEATING IN STT MRAM

As previously mentioned, a current density of  $1 \text{ MA/cm}^2$  or higher is required in order to flip the magnetization of the MTJ from parallel to antiparallel or vice-versa. Application of such high current density results in substantial self-heating which invariably influences the overall performance and reliability of the device [39, 106]. Also, self-heating ramps up breakdown and hence has an impact on device endurance [107, 108]. In this chapter, based on the numerical solution of the Landau–Lifshitz–Gilbert–Slonczewski (LLGS) equation and three-dimensional (3D) heat transfer equation, we present a theoretical analysis of STT-MRAM self-heating with appropriate boundary conditions and material parameters. Temperature rise in the device has been investigated under steady-state and transient conditions. The model developed in this chapter is used to investigate the variability of self-heating.

The major sources of variability of self-heating in an MTJ are mostly the geometric and material parameters of FL, RL, and the oxide layer. However, in an STT MRAM stack, there are a few additional layers required to provide magnetic and mechanical stability to the MTJ. All these layers govern the heating in the oxide layer. Material property-related and geometric variations of these layers, along with the surroundings, control the overall heating of the device. In this chapter, applying the simulation framework elaborated in the previous chapter, we'll investigate the effects of the variability of different layers on the heating behavior of an STT MRAM. Firstly, in section 4.3.1, we'll look into the spatial and temporal heat distribution of an STT MRAM stack under the application of DC bias. Later in section 4.3.2, the effects of geometric variations are investigated. The dimensions of different layers and device diameters are varied to observe the impact on transient and steady-state behavior of the temperature in the device. Then in chapter 4.3.3, the effects of shape variation, i.e., undercut and overcut structure on self-heating, are analyzed. Lastly, in chapter 4.3.4, we look into how the variations in the material properties of the surrounding metal stacks and enclosure lead to the variation of steady-state temperature.

## 4.1 STT MRAM Stack and Self-Heating Model

The self-heating model consists of two parts: one is solving the 3D Fourier Heat Transfer equation along with the LLGS equation. The latter is used to incorporate the switching dynamics of MTJ under different pulse schemes. The details of the LLGS equation are described in Chapter 2, and we'll restrict our discussions on the 3D Fourier Heat Transfer equation in this chapter.

Before going into the details of the heat transfer equation, we'll describe the STT MRAM stack considered in this work. The perpendicular MTJ-stack studied in this work is schematically shown in Fig. 4.1. This device structure is representative of a standard MgO-based STT-MRAM [42, 109]. The reference layer (RL) and free layer (FL) of the device are CoFeB ferromagnets. MgO sandwiched between RL and FL acts as the insulator increasing the TMR of the device. The RL is pinned with a synthetic anti-ferromagnet (SAF) layer, which consists of alternating Co/Pt layers. The SAF layer is required to provide stability to the RL. The SAF layer is also termed a Hard Layer (HL) in literature. The rest of the structure comprises of TiN hard mask (HM), TaN/Tungsten (W) bottom electrode (BE), Cu-top electrode (TE), and a SiO<sub>2</sub> encapsulation. The TiN hard mask is used for mechanical support and to withstand the MTJ etching process. The thicknesses of these layers have been chosen based on practical MRAM stacks reported in [41]. The MTJ device considered here is cylindrical in shape. In accordance with the values reported in [41], RA product of  $10\Omega - \mu m^2$  are considered in this study. For high-density memory and neuromorphic applications, STT-MRAMs having diameters ranging from 40 nm to 100 nm have been experimentally reported [109]. Based on this observation, we have considered devices of 60, 70, and 80 nm diameters in our study.

As current flows through MTJ, Joule heating ( $I^2R$ ) occurs in the MgO layer due to its high resistivity. This results in an increase in temperature. Time-dependent three-dimensional (3D) Fourier heat conduction equation of the following form has been solved with appropriate material parameters (given in Table 4.1) and boundary conditions.

$$\rho c \frac{\partial T}{\partial t} = \nabla \cdot (k \nabla T) + \frac{I^2 R}{V} \quad (4.1)$$

Here  $\rho$  is the material density,  $c$  is the specific heat capacity,  $k$  is the thermal conductivity,  $I$  is the current through the MTJ,  $R$  is the resistance, and  $V$  is the volume of the device. Device resistance under the application of different input voltages has been obtained by solving the LLGS equation.

As shown in Fig. 4.1, the TE of the device is grounded, and DC/AC bias is applied at BE. According to this polarity convention, a positive bias switches the MTJ resistance from RP to RAP, and a negative voltage switches it from RAP to RP.

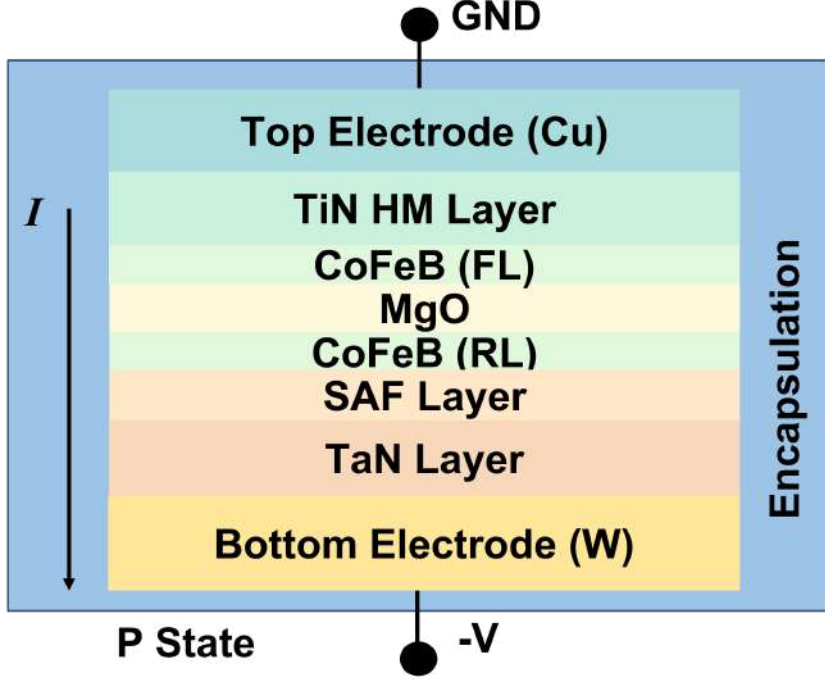


Figure 4.1: 2D schematic of the STT-MRAM stacks considered in this study for self-heating analysis.

Eq. 4.1 is solved using Finite Element Method (FEM). The exterior side of the encapsulation has been used as a thermal boundary kept at fixed  $T_0 = 298$  K. The Dirichlet boundary condition is used. Also, the initial condition is assumed to be  $T_0 = 298$  K. A useful quantity that can be obtained from the temperature rise vs bias voltage curve is the **thermal resistance** ( $R_{th}$ ), which characterizes the increase of temperature for given input power. The larger  $R_{th}$  of a system, the higher temperature rise will occur at a particular bias. It can be obtained by assuming that  $\Delta T$  due to SH is proportional to input power, i.e.  $I^2 R$  or  $\frac{V^2}{R}$ . This proportionality constant is  $R_{th}$ .

$$\Delta T_{SH} = \frac{V_{MTJ}^2}{R} R_{th} \quad (4.2)$$

So by fitting  $\Delta T$  vs  $V$  curve to the equation given in 4.2, one can obtain  $R_{th}$  under different conditions. This parameter heavily depends on the local material stack environment surrounding the MgO layer.

## 4.2 Undercut and Overcut structures

To observe the shape variation, we have used two different types of structures, as shown in Fig. 4.2a) and b). The structures are named ‘overcut’ and ‘undercut’ structures,

Table 4.1: Material Parameters used for Simulation

| Material | k (WmK) | c (JkgK) | p(kgm3) |
|----------|---------|----------|---------|
| Cu       | 401     | 390      | 8940    |
| TiN      | 11      | 380      | 5400    |
| CoFeB    | 87      | 440      | 7700    |
| MgO      | 48      | 940      | 3580    |
| Co       | 100     | 420      | 8900    |
| Pt       | 71.6    | 133      | 21450   |
| TaN      | 3       | 210      | 13800   |
| SiCOH    | 0.59    | 636      | 1400    |
| SiO2     | 1.4     | 703      | 2320    |
| W        | 40      | 134      | 19300   |

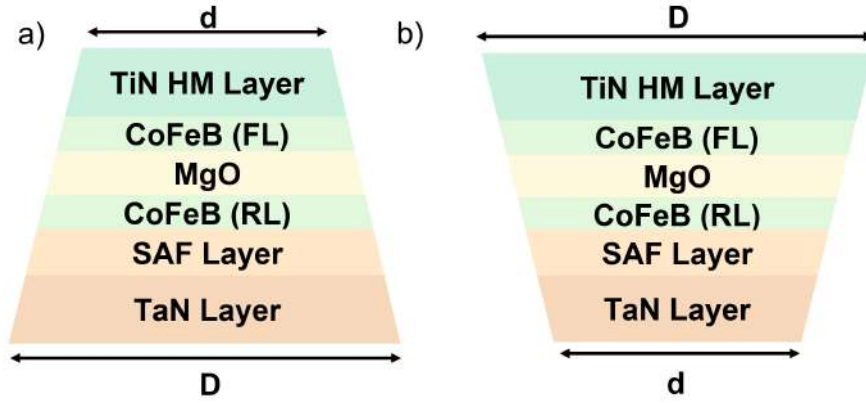


Figure 4.2: 2D Schematic of a) Overcut and b) Undercut Structures. Here  $D$  is the nominal diameter, and  $d$  is the diameter of the upper (lower) layer for overcut(undercut) structure.  $D-d$  is the amount of overcut or undercut.

respectively. Overcut structure is one in which the upper diameter is less than the nominal diameter, and for undercut structure, the lower diameter is less than the nominal one. For comparison purposes, the nominal diameter has been considered to be 70 nm in this thesis. Also  $d$  is the diameter of the upper (lower) layer for overcut (undercut) structure. We define  $D-d$  as the amount of overcut or undercut.

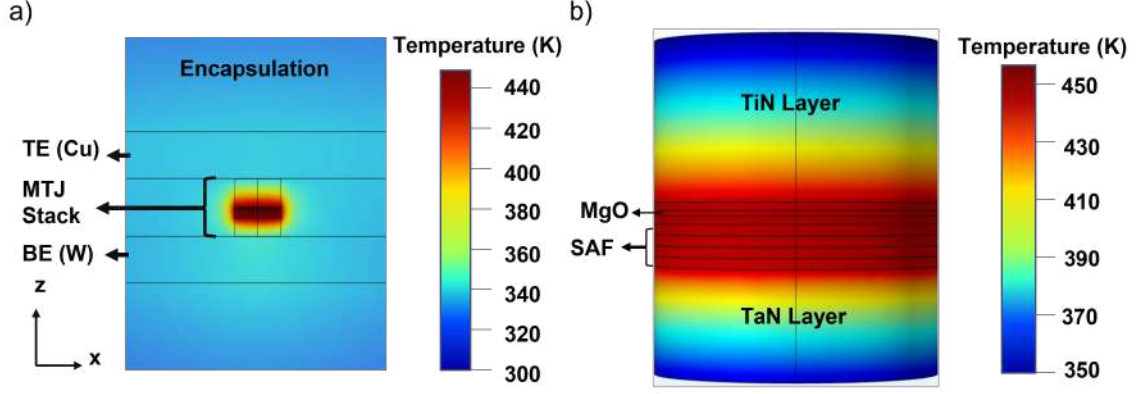


Figure 4.3: a) Spatial temperature distribution of the whole STT-MRAM Stack along with the electrodes and encapsulation and b) temperature distribution of the MTJ stack along the z-x plane under the application of  $-0.8$  V pulse for  $5 \mu s$ . The diameter of the cylindrical MTJ is  $70$  nm. From the distribution, it is evident that most of the heating occurs at the MgO layer, and it reaches up to  $450$  K temperature.

## 4.3 Results and Discussions

### 4.3.1 Spatial and Temporal Heat Distribution of MRAM Stack

As previously mentioned, to obtain the temperature rise in an STT MRAM stack due to self-heating, the Fourier Heat equation 4.1 is solved. The spatial thermal distribution of the STT-MRAM, under the application of a negative bias of  $0.8$  V for  $5 \mu s$ , is shown in Fig. 4.3b) and c). As observed, the temperature rises mostly in the MgO and the adjacent layers. The temporal temperature profile for this device is shown in Fig. 4.4a). It is evident from this figure that initially, the temperature rises rapidly, and after that, the rate of rise decreases, and finally, the temperature reaches saturation or steady state value. The initial fast heating component followed by the slow one has been observed previously as well [39, 41, 110]. The origin of these two regions can be attributed to the difference in thermal conductivities of different layers of the MTJ stack. The CoFeB/MgO/CoFeB MTJ is surrounded by poor thermal conductive materials such as TiN, TaN and encapsulated by SiO<sub>2</sub>, which impede the escape of generated heat from the MgO layer. As a result, initially, the generated heat cannot escape from the MgO layer, and so the temperature rise increases faster. However, after the heat reaches good thermal conductive material like Cu, W it can get away from the device, and hence the rate of temperature rise decreases. The steady-state temperature rise for different negative (UNI-) bias voltage for  $70$  nm device is shown in 4.4b). The curve follows a parabolic shape exhibiting the  $\Delta T \propto V^2$  relation.

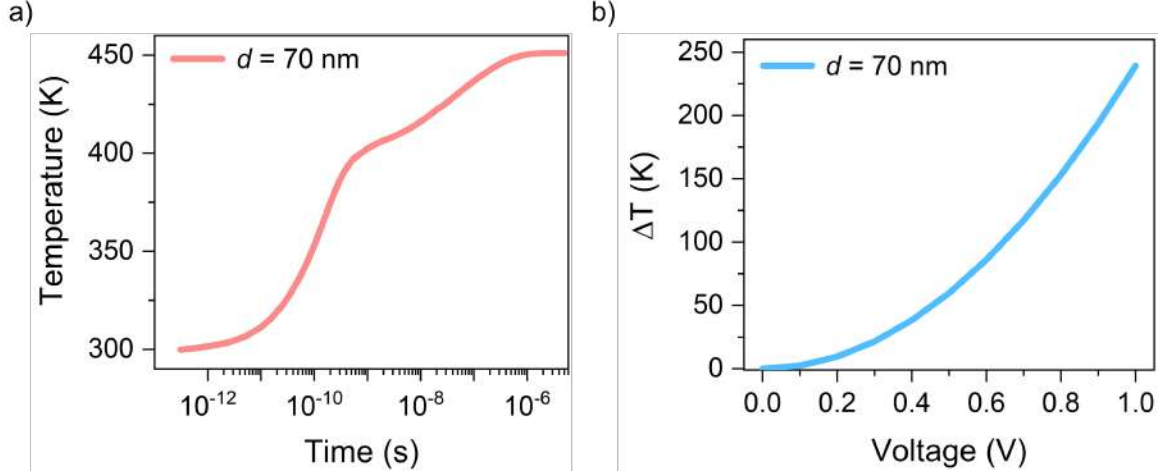


Figure 4.4: a) Temporal Temperature profile for 70 nm MTJ under the application of  $-0.8\text{V}$  for  $5\mu\text{s}$ . b) Temperature Rise  $\Delta T$  vs. Applied negative bias voltage (UNI-) curve for MTJ with 70 nm diameter. The curve resembles a parabola. Fitting this curve to the equation  $\Delta T = R_{\text{th}} \frac{V^2}{R_{\text{MTJ}}}$ , we can obtain  $R_{\text{th}}$ .

### 4.3.2 Impact of Size Variations

In Fig. 4.1, the considered STT MRAM stack is given. At first, we'll investigate the effect of the thickness of the TaN and TiN layer on the steady state temperature of the device. We vary the thickness from 20 nm to 70 nm and observe the steady-state temperature under the application of constant bias voltage 0.8V. The result is shown in Fig. 4.5. It is evident that the final temperature ( $T_f$ ) increases with increasing TiN layer thickness near the top electrode. The same trend is observed if the TaN layer thickness of the bottom electrode is increased. However, the increase appears to be more prominent for the TiN layer near the TE, which suggests that this layer thickness contributes more to the temperature rise than does the ultrasmooth BE (TaN) layer. Next, we look into the variation of diameter of the MTJ with fixed  $RA$  product of ( $11\Omega - \mu\text{m}^2$ ) and having diameters 60 nm, 70 nm, and 80 nm. The temporal profiles of temperature under the application of a constant negative bias of 0.8V for  $5\mu\text{s}$  with different diameters are shown in Fig. 4.6a). It can be seen that with increasing diameter, the temperature rise also increases. The steady-state temperature rises  $\Delta T$  vs. bias voltage ( $V$ ) (UNI-) is shown in Fig. 4.6b) also exhibits this trend. The calculated  $R_{\text{th}}$  for different diameters are also in table 4.2. The calculated  $R_{\text{th}}$  exhibits decreasing behavior with increasing diameter. Smaller devices have higher  $R_{\text{th}}$  as they have smaller cross-sectional area contacts with the top and bottom electrodes for heat dissipation [111].

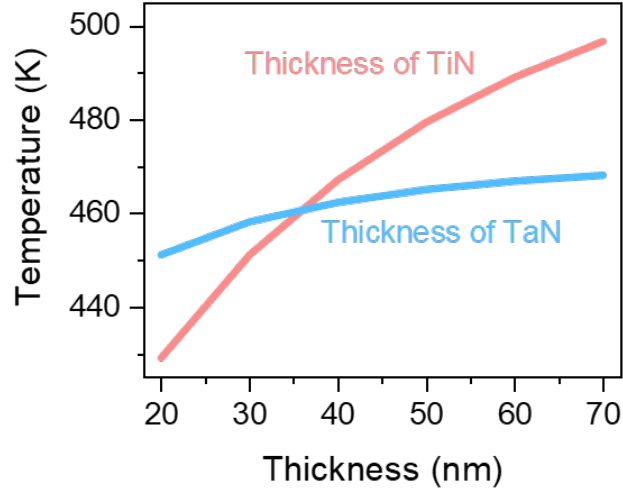


Figure 4.5: Variation of the steady-state temperature with the thickness of TiN and TaN layers. In both cases, the steady-state temperature increases with the thickness of the TiN and TaN layers. But in the case of the TiN layer, the change is more prominent than the TaN layer.

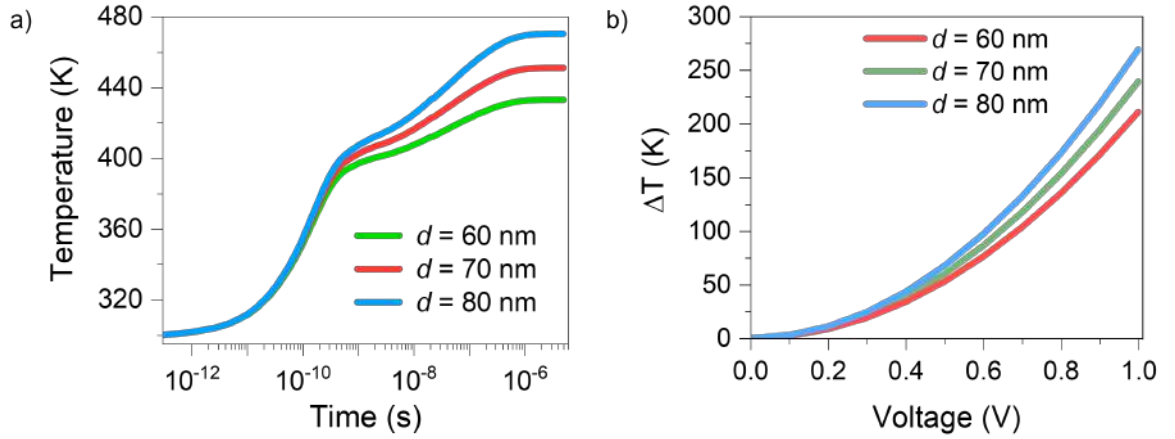


Figure 4.6: a) The temporal temperature profile of MTJ stack with diameter 60, 70, and 80 nm under the application of  $-0.8$  V pulse for  $5 \mu\text{s}$ . b) steady-state temperature rise  $\Delta T$  vs bias voltage (V). Here the bias voltage is UNI- as per our convention.

Table 4.2: Extracted  $R_{\text{th}}$  for different diameters

| Diameter (nm) | $R_{\text{th}}$ ( $^{\circ}\text{C}/\mu\text{W}$ ) |
|---------------|--|
| 60            | 0.74614  |
| 70            | 0.62149  |
| 80            | 0.53567  |



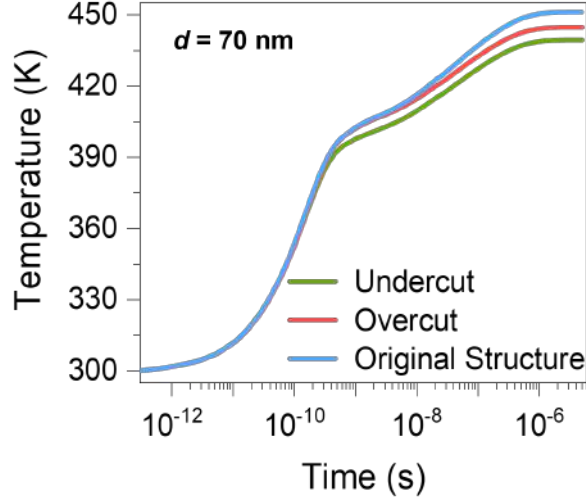


Figure 4.7: Temporal temperature profile for undercut, overcut, and original structure for the nominal diameter of 70 nm.

### 4.3.3 Impact of Shape Variation

In this section, we'll investigate the effect of overcut and undercut structures (as shown in Fig. 4.2 on the self-heating of STT MRAM. The temporal temperature profiles of the overcut and undercut structures are shown in Fig. 4.7. It is interesting to see that compared to the original, symmetric structure, the temperature rise decreases in both overcut and undercut structures. This is owing to the reduced average diameter of the MTJ, which ultimately results in a larger electrical resistance for a fixed RA product of the MTJ. It is also noteworthy that the undercut structure exhibits a smaller temperature rise compared to the overcut structure. This is due to the asymmetry of the MTJ below and above the MgO barrier layer.

To look into this aspect in further detail, steady state temperatures for different upper (lower) diameters of the overcut (undercut) structure have been calculated. The results, shown in Fig. 4.8a) and 4.8b), suggest that the final temperature is always slightly higher for the overcut structure. However, whereas the range of temperature rise is 30 K for the undercut structure, for overcut structure, the value is 15 K. Hence device-to-device temperature variability is expected to be larger in undercut structures than in overcut ones.

### 4.3.4 Impact of Variation of Encapsulation

Encapsulation is used as a boundary between the environment and the STT-MRAM stack. Throughout our simulation, we used SiO<sub>2</sub> as encapsulation. Both the dimension and the thermal conductivity of encapsulation can exert effects on the steady-state temperature of the device. Fig. 4.9(a) shows the temporal profile of temperature for

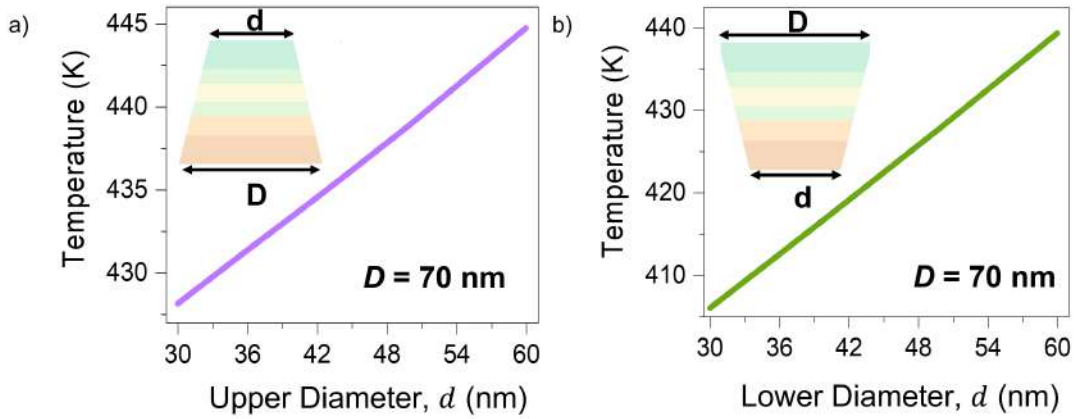


Figure 4.8: Steady-state temperature for a) different upper diameter for Overcut and b) different lower diameter for Undercut structure. The temperature rise is always lower in the case of the undercut. However, the range of the temperature rise is larger for the undercut than the overcut structure for the same diameter values.

two different encapsulations: one is for  $\text{SiO}_2$ , and another one is for  $\text{SiCOH}$  encapsulation. Due to the lower thermal conductivity of  $\text{SiCOH}$  ( $0.59 \text{ Wm}^{-1}\text{K}^{-1}$  than  $\text{SiO}_2$ ), the temperature increase is higher in the former case. Lower thermal conductivity encapsulation will trap more heat, and so the final temperature rise will be higher. This is evident from Fig. 4.9(b), which shows the decreasing steady-state temperature with respect to the thermal conductivity ( $\kappa$ ) of the encapsulation. To observe the effect of encapsulation dimension on the steady-state behavior of temperature, the dimension of cubic shape encapsulation of  $\text{SiO}_2$  is varied from  $1.5 \mu\text{m}$  to  $5 \mu\text{m}$ , and the steady-state temperature is calculated. The result presented in Fig. 4.9(c) shows that with increasing encapsulation dimension, the final temperature increases, but the rate of change is very slow. From the figure, it can be seen that increasing the dimension by around five times makes the temperature rise about 12 K only.

#### 4.3.5 Self-Heating under different pulsed operations

To understand the transient characteristics related to self-heating, both unipolar and bipolar pulses are considered. For such pulsing, MTJ state will change from RP to RAP or RAP to RP, depending on the initial state of the MTJ. In this study, the device is initially considered to be in a parallel state. A positive ramp voltage having 40% duty cycle and  $4 \mu\text{s}$  period is taken as the first case of pulsed input (Fig. 4.10(a)), and the corresponding resistance values are shown in Fig. 4.10(b). At around  $2 \mu\text{s}$  and  $0.5\text{V}$  input voltage, the current density is large enough to switch the MTJ from RP to RAP state. Because  $R_{\text{AP}} > R_{\text{P}}$ , the change of resistance state is accompanied

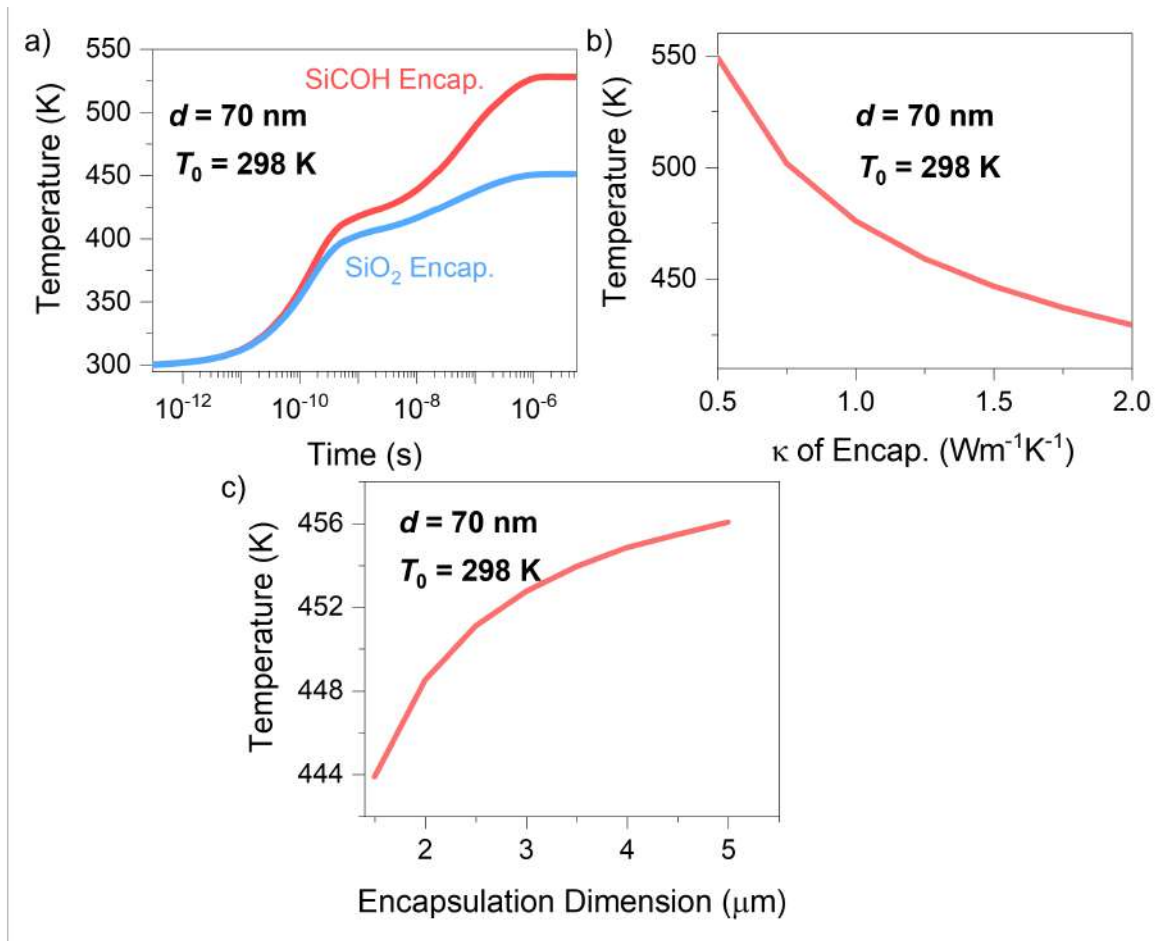


Figure 4.9: a) Effect of encapsulation on the temporal temperature profile of an MTJ. Temperature increases more for lower thermal conductivity encapsulation, i.e. SiCOH than SiO<sub>2</sub> b) Steady-state Temperature vs thermal conductivity ( $\kappa$ ) of encapsulation. c) Steady-state temperature for different encapsulation dimensions which shows an upward but very gradual rise. The initial and boundary temperatures for all cases are 298 K, as shown in the figure.

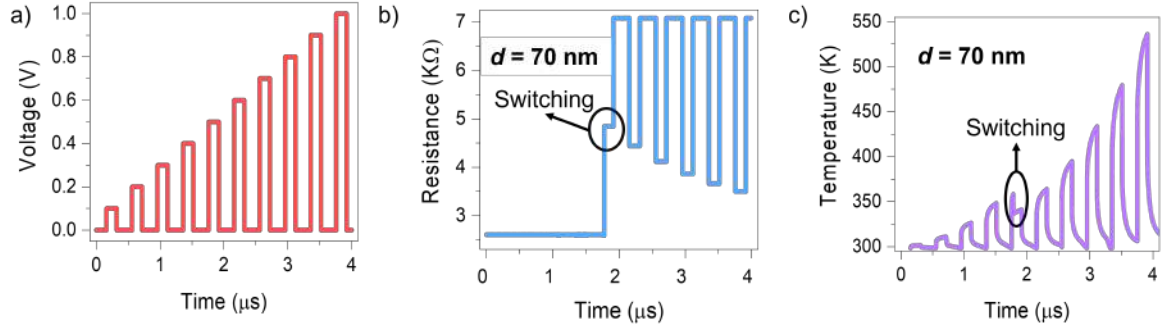


Figure 4.10: a) Applied ramped positive voltage pulse with period  $4 \mu\text{s}$  and duty cycle 40%. Here only one period is shown. b) The corresponding resistance state of MTJ. Around  $2\mu\text{s}$ , i.e. at  $0.5\text{V}$ , there is a change in resistance values which indicates the switching of MTJ from  $R_P$  to  $R_{AP}$ . c) Temperature vs. time curve for ramped positive bias. The spike around  $2\mu\text{s}$  corresponds to the switching of MTJ. Also, the temperature initially increases with the bias, but after switching, it gets decreased as the resistance after switching is higher ( $R_{AP}$ ), which results in lower heat and lower temperature before switching.

by a rapid decrease in temperature. This is confirmed by the spike in the temperature vs. time plot shown in Fig. 4.10(c).

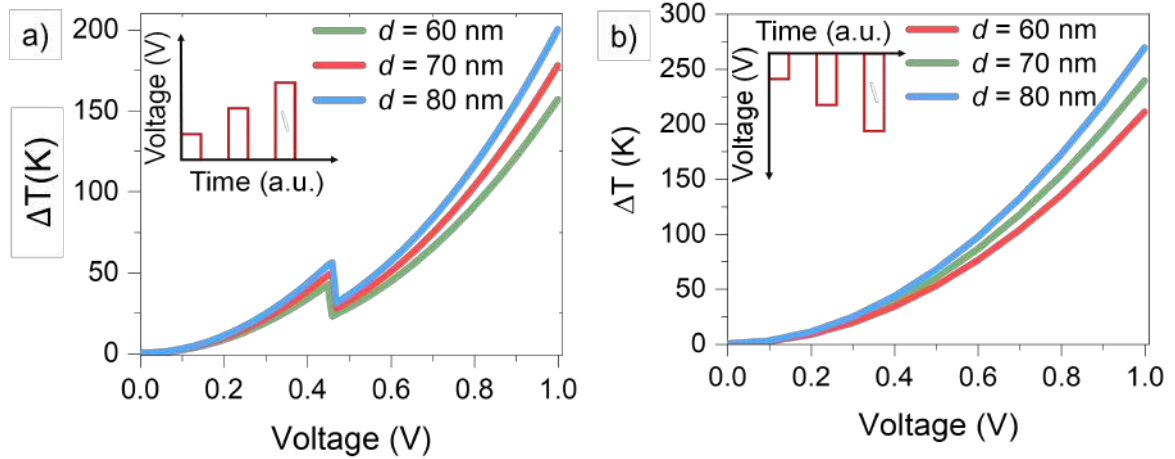


Figure 4.11: Steady state temperature under the application of a) positive ramped pulses and b) negative ramped pulses for different diameters. According to our convention, positive ramped pulses switch MTJ from  $R_P$  to  $R_{AP}$ , and so a discontinuity in Figure a) is observed. Also, due to the higher resistance of smaller devices, the temperature rise is lowest for 60 nm diameter.

As the input voltage is unipolar, after the first period, the device remains in  $R_{AP}$  state, and hence there are no further spikes in the temperature profile. In Fig. 4.11(d), the steady-state temperature rise ( $\Delta T$ ) is shown as a function of input voltage for this positive ramp. The abrupt change of temperature near the switching voltage becomes evident from this plot. In the case of the ramped negative voltage, as the device was already in  $R_P$  state, no switching occurs, and hence the temperature vs. voltage curve

appears parabolic (Fig. 4.11(b)). The temperature rise is greater in this case as the MTJ remains in a low resistance state for all values of the negative bias.

The case of a bipolar input pulse of magnitude 0.8V, period 390 ns is shown in Fig. 4.12(a). Three distinct states can be identified from the resistance vs. time plot (Fig. 4.12(b)) obtained for this input. The lowest resistance state (denoted as I) corresponds to the  $R_P$  state, the middle transition (denoted as II) corresponds to  $R_{AP}$  state at 0.8V, and the highest resistance state (labeled III) is the  $R_{AP}$  at zero bias. The results here are in accordance with the voltage dependence of the anti-parallel state of an STT-MRAM. The resulting temperature vs. time curve is shown in Fig. 4.12(c), which clearly exhibits the transition from I to II states mentioned in Fig. 4.12(b). Because of the small duty cycle of the input pulse, the device reaches ambient temperature before the negative cycle. For negative bias, the device transits to a parallel-state and stays therein. Hence no spike is observed in the switching characteristics in this case. Fig. 4.12 shows the steady-state temperature rise under the application of a bipolar pulse which ramps from -1V up to 1V in each period. This is clearly a combination of UNI- and UNI+ pulse cases. In UNI- case, there is now switching. In the UNI+ case, the switching occurs in the initial period. Afterward, there will be no switching as the device will be in a higher resistance state for the subsequent UNI+ pulses. However, in ramped bipolar case, as there will be both positive and negative pulses in each period, there will always be switching, and there will always be a discontinuity in the temperature profile. This hints at the more effects of self-heating on STT-MRAM's reliability and breakdown behavior in bipolar stress than UNI+ and UNI- stress cases as detailed shown in [111].

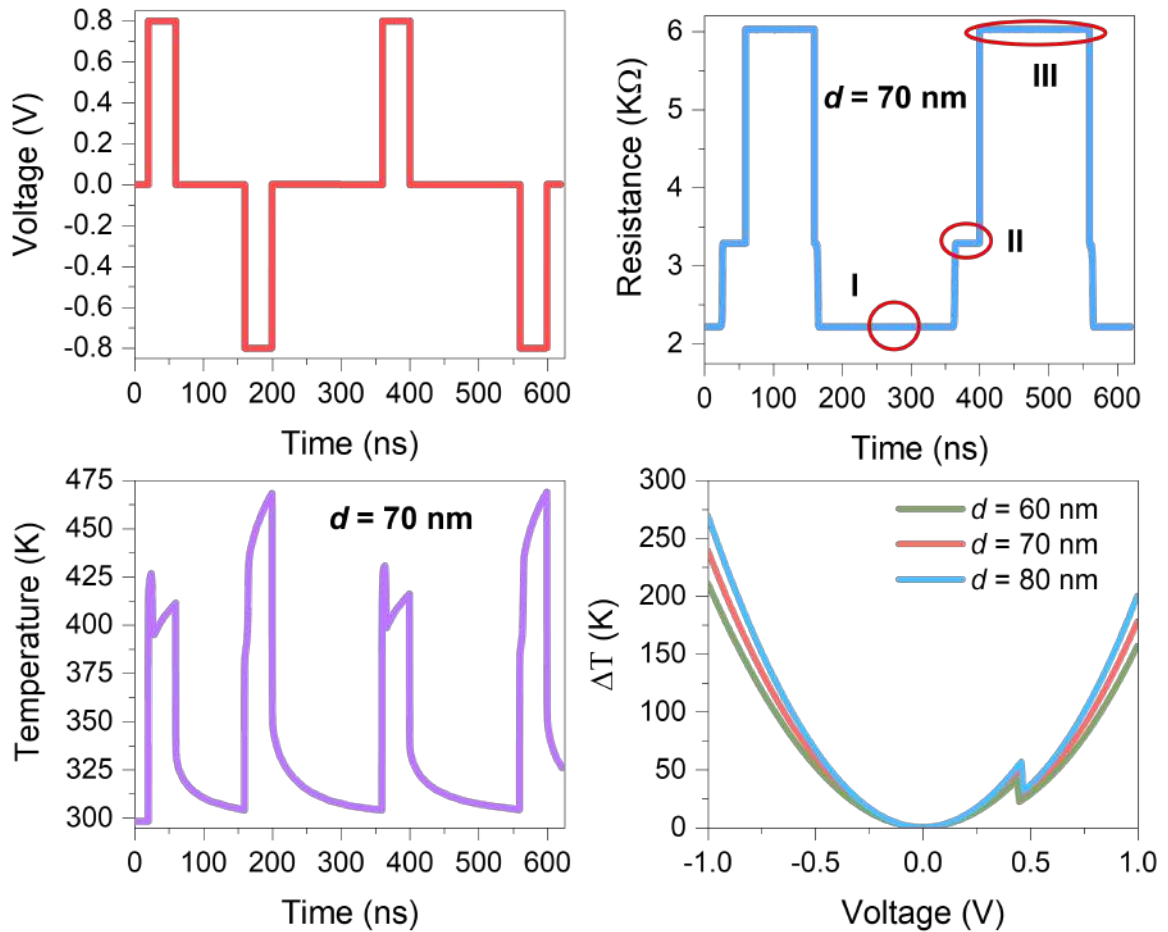


Figure 4.12: a) Applied bipolar voltage pulse with magnitude 0.8 V with period 310 ns. Here two periods are shown. b) The corresponding resistance state of MTJ. Three distinct resistance states are evident from this figure. The lowest one is the RP state (marked by I), the middle one is the resistance in the AP state at 0.8V (marked by II), and the highest one is the resistance in the AP state at 0V (marked by III). c) Temperature vs. time curve for the application of the bipolar pulse. The spikes correspond to the switching between different R states of MTJ, as mentioned in Fig. 4b). d) Steady-state temperature rise for the application of bipolar ramped pulse from -1V to 1V.

# CHAPTER 5

## CONCLUSIONS

### 5.1 Summary of the Present Work

In the present work, to incorporate the effect of interface quality, temperature variation, device dimensionality, and defects on device-to-device variability and the impact of geometrical shape, size, and different pulsed operations on self-heating of an STT MRAM, a simulation framework has been developed. The framework consists of solving the LLG equation numerically along with the 3D heat diffusion equation. At first, the proposed model has been validated using the experimental results reported in several literature. Then the impact of various parameters on device-to-device variability has been explored. In order to include the effect of metal-induced gap states in the insulating oxide layer, a gradually varying energy band profile of the oxide barrier has been proposed with an average effective barrier height. Good agreement between simulation and experimental results is obtained for all devices irrespective of diameters if such band profiles are considered. Thus the effective energy barrier height can serve as a figure of merit of the interface quality of MTJs. This interface barrier height can significantly influence the variability of these devices. It has been shown that Switching voltage and parallel-antiparallel resistance values vary by as much as 43% and 30%, respectively, for about 13% variation of the energy barrier, whereas the tunneling magnetoresistance remains typically unaltered. This barrier height can also be utilized to predict WRITE cycle variability. Bulk defect density and distribution, as well as temperature, are observed to have minimal effect on such variabilities of STT-MRAMs.

To model the temperature rise in an STT-MRAM stack due to self-heating resulting from the high current density, the 3D Fourier Heat equation is solved, taking into account the spin-transfer torque-based switching dynamics. The results of the theoretical self-heating analysis show that the thickness of the heavy metal layer near the top electrode and the encapsulation have a significant impact on the temperature rise in these devices. Also, undercut structures are expected to be more susceptible to device-to-device temperature variability. The results of this work also show that spintronic switching dynamics deserve careful consideration for an accurate estimate of the temperature rise of STT-MRAMs, especially during their transient operations.

As the impact of self-heating on device endurance and TDDB breakdown has been reported in several papers [39, 41, 108, 111], the temperature rise due to self-heating observed in this work can be used to investigate the Time Dependent Dielectric Breakdown (TDDB) in STT MRAM by duly taking into account the spatial and temporal distribution of temperature rise in the MTJ stack. The analysis technique applied here and the insights obtained from this work may also provide guidelines for improving the reliability and endurance of STT MRAMs by proper selection of materials and geometric structures.

## 5.2 Suggestions for Future Works

There are a lot of opportunities for further research. The considered ones related to the thesis are:

- While discussing MIGS, a gradually varying band profile has been proposed. But due to brevity and lack of computational resources, an ab-initio study has not been possible to verify such proposals. A rigorous ab-initio study can be done to verify the barrier height lowering of the oxide layer due to MIGS.
- Spin scattering from the defects inside the oxide layer has been neglected for the simplification of analysis. A Monte Carlo simulation framework to study how such scattering can affect spin transport in the presence of defects can be studied.
- The impact of interface quality on device-to-device variability can further be extended by investigating how different oxide layers contribute to it. However, for this, a combination of both new experiments and simulations is required. Carrying out any new experimental work is beyond the scope of this thesis work.
- A Time-Dependent Dielectric Breakdown (TDDB) experimental study for unipolar and bipolar pulsing stress can be carried out, including the self-heating analysis presented in this thesis. This will enable us to explain the underlying physical mechanisms of breakdown under different pulsing schemes.
- Experimental validation of the tapered shape devices can be done in the context of self-healing. As our simulation suggests, undercut and overcut structures exhibit lower temperature rise compared to the original structure. Experiments can be designed to look into the performances of such tapered-shaped devices to obtain design space for temperature rise and performance improvement.



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