L-4/T-2/EEE **Date: 25/03/2024**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-4/T-2 B. Sc. Engineering Examinations 2021-2022

Sub: **EEE 415** (Microprocessor and Embedded System)

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks.

The corresponding Course Outcomes (COs) of each part of Question 1 and 5 are mentioned on the right most column. The COs of the Course are mentioned at the end of the question paper.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer to **Question No. 1 is compulsory.**

Answer any TWO questions from Questions 2-4.

1. (a) Based on ARMv7 architecture, you have to design a single-cycle microprocessor which is also capable of executing three special instructions **ADDXOR, ADDNOR** and **SUBAND**. These instructions are described as follows: **(20)** (CO1)

`ADDXOR Rd, Rn, Src2`	First adds Rn with Src2, then performs an XOR operation between the obtained summation and Rn, and finally stores the result in Rd
`ADDNOR Rd, Rn, Src2`	First adds Rn with Src2, then performs a NOR operation between the obtained summation and Rn, and finally stores the result in Rd
`SUBAND Rd, Rn, Src2`	First subtracts Src2 from Rn, then performs an AND operation between the obtained subtraction and Rn, and finally stores the result in Rd

(i) Draw the complete datapath of the single-cycle processor capable of executing the mentioned special instructions, in addition to the regular instruction set of Armv7.

(ii) Based on your design, calculate the time required for execution of **ADDXOR, ADDNOR** and **SUBAND** instructions. Refer to Table for Question No. 1(a) for timing delays of different components of the microprocessor. Also assume that introduction of any new logic gate in the datapath introduces a propagation delay of 25 ps.

Contd P/2

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Contd... Q. No. 1(a)

Element	Parameter	Delay (ps)
Register clk-to-Q	t_{pcq}	40
Register setup	t_{setup}	50
Multiplexer	t_{mux}	25
ALU	t_{ALU}	120
Decoder	t_{dec}	70
Memory read	t_{mem}	200
Register file read	t_{RFread}	100
Register file setup	$t_{RFsetup}$	60

Table for Question no. 1(a)

(b) Based on your knowledge and understanding of current trends and development in ARM and RISC-V processor architectures, list their major similarities and differences, as well as their advantages and disadvantages. **(15)** (CO3)

2. (a) Consider the datapath of the pipelined processor shown in the Figure for Question No. 2(a). There is an error in the datapath which needs to be addressed for pipelining to occur properly. **(20)**

   (i) Identify the error and make necessary corrections to the datapath.

   (ii) Suggest a modification to the datapath to optimize the usage of the Program Counter logic.

   (iii) Now suppose you are executing the following assembly instructions in your modified pipelined processor. What kind of hazard would happen during the execution of these instructions?

Make necessary modifications to your design to address the hazard.

```
ADD R1, R4, R5
ORR R8, R1, R3
AND R9, R6, R1
SUB R10, R1, R7
```

(b) A cache has the following parameters: **(15)**

- Block size given in number of words: b
- Number of sets: S
- Number of ways: N
- Number of address bits: A

Contd P/3

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Contd... Q. No. 2(b)

Obtain the following:

(i) The capacity of the cache in units of words.

(ii) The total number of bits required to store tag bits.

(iii) The number of sets if the cache is direct mapped.

(iv) The number ways if the cache is fully associative.

3. (a) Consider the multi-cycled processor shown in the Figure for Question No. 3(a). Show the complete Finite State Machine (FSM) for the control signal corresponding to the following assembly instructions. **(20)**

```
STR R1, [R4, #4]
ORR R8, R1, R3
B LABEL
```

Note that in your FSM diagram, if you need to show any control signal that appears inside the control unit, show the corresponding signal that appear in the Figure for Question No. 3(a).

If the above instruction set is used as a benchmark, what will be the clocks per instruction (CPI) according to your FSM?

(b) Consider the following high level code which adds '5' with the array named '**runs**': (15)

```
int i;
int runs[22];
for (i=0; i <22; i=i+1)
        runs[i]=runs[i]+10;
```

It is mentioned that all values stored in the array '**runs**' are within the range of 0 to 100.

Write down the ARM assembly code for the above high level code such that the assembly code makes optimum utilization of memory space.

4. (a) Suppose, you have to run the following assembly instruction set comprising of Branch instruction: **(20)**

```
MOV R0, #4
MOV R1, #0
LOOP CMP R0,#0
BEQ FINISH
LDR R2, [R1, #0x44]
LDR R3, [R1, #0X24]
SUB R0, R0, #1
B LOOP
FINISH
```

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Contd... Q. No. 4(a)

(i) Considering the 8-word direct mapped cache shown in the Figure for Question No. 4(a), calculate the hit rate. Show all entries of the direct mapped cache after the end of execution of the above assembly code.

(ii) Using the concept of termporal locality, make necessary modifications to the 8-word cache so that miss rate is reduced. Calculate the miss rate for your suggested design and show all entries of your designed cache after the end of execution of the assembly code.

(iii) If you were asked to exploit spatial locality instead of temporal locality in order to improve hit rate, what modifications would you do? Calculate the miss rate for your suggested design and show all entries of your designed cache after the end of execution of the assembly code.

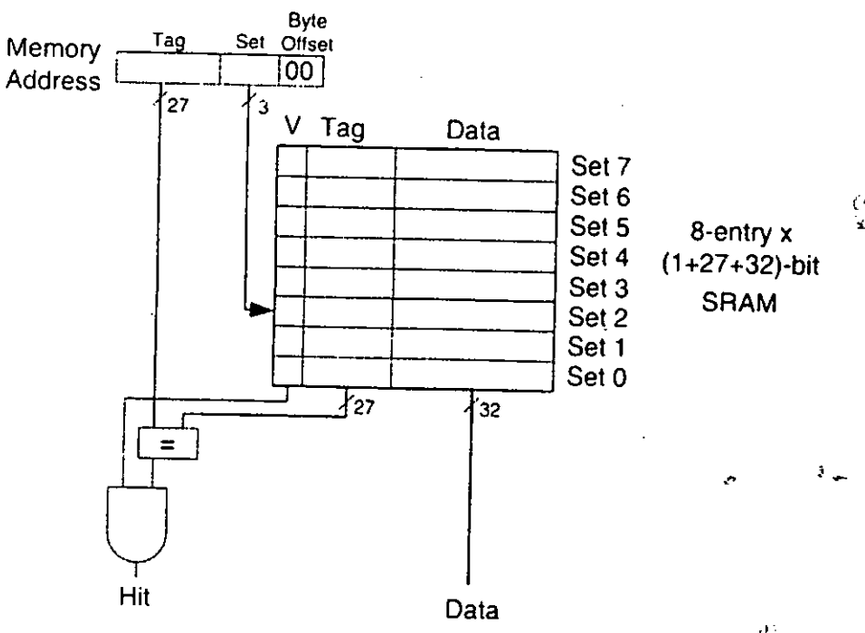

Figure for Question no. 4(a)

(b) Based on the information given in the Appendix for Question No. 4(b), translate the following assembly language statements into machine language: **(15)**

```
STR R10, [R3],#-13
MOV R1, 5
SUB R2, 12
ADD R3, R4
```

Contd P/5

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Contd... Q. No. 4(b)

Also translate the following machine language code into assembly language based on the information given in Appendix for Question No. 4(b):

```
0xE3A02045
0xE1510002
0xE0475001
0xE5949010
```

SECTION – B

There are **FOUR** questions in this section. Answer to **Question No. 5 is compulsory.**

Answer any TWO questions from Questions 6-8.

5. Suppose, you want to automate and parking lot, so that it can warm the incoming drivers when all the parking spaces are full. The parking lot has two gates - an entrance and an exit. You connected two InfraRed (IR) detectors (one at each gate) and a red LED with an STM32L4 board as shown in Fig. for Q. No. 5(i). When connected to VDD and GND as shown, the middle pin of the IR detector gives a signal that is 3.3 V when an object is detected in front of it, and 0 V otherwise. The total number of parking spaces is known to you (included in the code as #define capacity 10).

(a) Compare the push-pull and open-drain mode of driving a GPIO pin. Which mode will you use for pin 5 of GPIO port A (PA5)? **(5)** (CO2)

(b) Compare Interrupt and polling method. Which method will be more appropriate for monitoring both gates simultaneously? Write a function that initializes the PC13 and PC 14 pins and connect them to suitable external interrupts. Related registers are described in Fig. for Q. No. 5(ii). **(15)** (CO2)

(c) Write the handler EXTI15_10_IRQHandler() that performs the following functionality - increase the count if a car is detected at the entrance. But if count is greater than or equal capacity, the warning LED turns on, and count does not become more than capacity. Else if a car is detected at exit, the count decreases by one. **(15)** (CO2)

Contd P/6

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Contd... Q. No. 4(a)

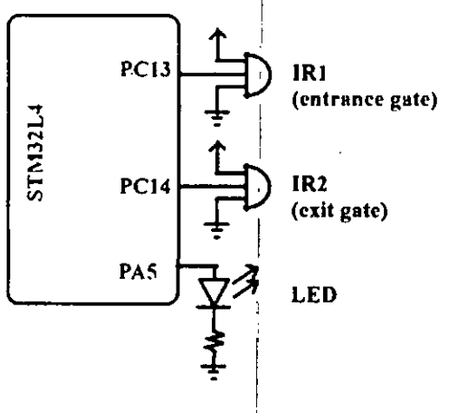

Fig. for Q. No. 5(i)

GPIO:
MODER: 2 bits per pin, 32 bits for 16 pins are sequentially located.
00 = digital input, 01 = digital output, 10 = alternate function, 11 = analog (default)
OTYPER: 1 bits/pin, sequentially located. 0 = push-pull, 1 = open-drain
OSPEEDR: 2 bits/pin, sequentially located.
00 = low speed, 01 = medium 10 = Fast speed, 11 = High Speed
PUPDR: 2 bits/pin, sequentially located.
00 = no pull-up, no pull-down, 01 = pull up, 10 = pull down, 11 = reserved
IDR, ODR: input and output data register, 1 bits/pin, sequentially located.
SYSCFGN:
EXTICR:
can connect each of the 16 EXTI to a Port between A (0000) and H (1111). There are four EXTICR ([0] to [3]) that handles EXTI 0 to 15, each register contains 4 EXTI, sequentially.
EXTI:
RTSR, FTSR, IMR, PR: 1 bit for each EXTI.

Fig. for Q. No. 5(ii)

6. A common way to convert DC to AC is Sinusoidal Pulse Width Modulation, which can be generated by comparing a sinusoidal modulation wave to a triangular/sawtooth carrier, as shown in Fig. for Q. No. 6. Observe that -

- The waveforms that the output frequency is dependent on the modulation wave frequency
- The resolution of the output is dependent on the ratio of the frequency of the carrier and sine wave, as one pulse is generated at each sawtooth period.

You have to generate the output PWM signal shown in Fig. for Q. No. 6(i) at PE8 pin, which is connected to TIM1_CH1N as AF1, with the following requirements -

- The system frequency is 4MHz, Output PWM frequency 100 Hz
- There must be 10 output pulses in each period of the sine wave.
- The modulation sine wave is being implemented by updating the timer compare value (CCR) from a lookup array (cmp_val) at regular intervals by the SysTick interrupt.

Contd P/7

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Contd... Q. No. 6

Now-

(a) Compute the ARR value of TIM1, if PSC is 39. **(10)**

(b) Which PWM mode will you choose for the timer if the counting direction is UP? Write the code to initialise the timer. **(15)**

- You don't have to initialise PE 8.
- Some important timer registers and their relevant bit fields are included in Fig. for Q. No. 6(ii).

(c) Suppose, the lookup arrary cmp_val contains 12 CCR values for one period (360°) of the sine wave. The SysTick Interrupt is using cmp_val to generate the 100 Hz modulation signal. If SysTick is using the same clock as the system calculate the SysTick period and the LOAD register value. **(10)**

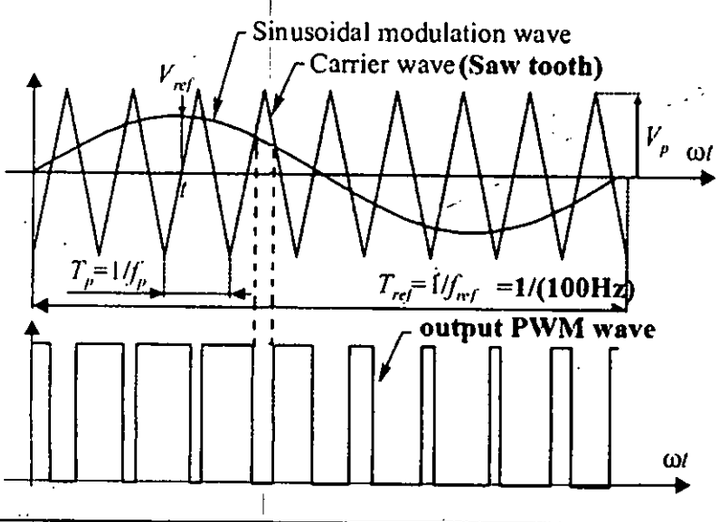

Fig. for Q. No. 6(i)

CR1:
DIR bit 4: 0 Up, 1 DOWN
CEN bit 0: 0 disable, 1 enable

PSC, ARR, CCR

CCMR1:
OC1M bit 4~6: PWM mode 1 is 110, PWM mode 2 is 111

CCER:
CC1NE bit 2: 0 disable, 1 enable
CC1NP bit 3: 0 active high, 1 active low

BDTR:
MOE bit 15: 0 disable, 1 enable

Fig. for Q. No. 6(ii)

7. (a) Draw the block diagram of a successive-appropriation (SAR) ADC. Explain its operation with the following example: The ADC is 3 bit, with reference voltage (Vref) of 3.3 V. What is the converted digital value when input is 1.8 V? **(15)**

(b) The City Corporation has given you the responsibility to automate the street lights in your locality so that the lamps are turned on at sun set or low light conditions. You decided to use Light Dependent Resistors (LDR), which have resistance as high as several MΩ in dark, but in the light, the resistance drops as low as a few hundred ohms. After some testing, you found the LDR has resistance ~15 KΩ at sun set condition. You connected the LDR to the STM microcontroller as shown in Fig. for Q. No. 7(b)(i). PA3 is connected to ADC1 as channel 8. **(20)**

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Contd... Q. No. 7(b)

(i) If the ADC is running in default 12 bit conversion mode, what is the condition on the value read at PA3 to turn on the street light?

(ii) Complete the code snippet given in Fig. for Q. No. 7(b)(ii), which is using single channel single conversion mode. Related registers are given in Fig. for Q. No. 7(b)(iii)

```
static void configure_ADC(){
        PA3_Init();
        /* This function sets up PA3 in Analogue mode
        You don't have to write this */
        //setup ADC1 with the following -
        //Enable ADC clock;
        //Choose Software Trigger
        //Select conversion length
        //Set up conversion sequence
        //Enable ADC
}

int main(void){

        enable_HSI(); // You don't have to write this
        configure_ADC();

        while(1)
                {
                /* Start a conversion and
                Read Data valid data */
                /* Call the function turn_on_light() if
                the Sun set is detected. You don't have
                to write the turn_on_light() function */
        }
}
```

Fig. for Q. No. 7(b)(ii)

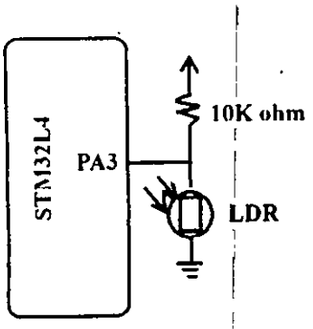

Fig. for Q. No. 7(b)(i)

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC_ISR																						JQOVF	AWD3	AWD2	AWD1	JEOS	JEOC	OVR	EOS	EOC	EOSMP	ADRDY
Reset value																						0	0	0	0	0	0	0	0	0	0	0
ADC_CR	ADCAL	ADCALDIF	DEEPPWD	ADVREGEN																							JADSTP	ADSTP	JADSTART	ADSTART	ADDIS	ADEN
Reset value	0	0	1	0																							0	0	0	0	0	0
ADC_SQR1				SQ4[4:0]						SQ3[4:0]						SQ2[4:0]						SQ1[4:0]								L[3:0]	
Reset value				0	0	0	0	0		0	0	0	0	0		0	0	0	0	0		0	0	0	0	0				0	0	0	0
ADC_DR																regular RDATA[15:0]																
Reset value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Fig. for Q. No. 7(b)(iii)

Fig. for Q. No. 7(b)(i)	Fig. for Q. No. 7(b)(ii)

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8. (a) For UART communication, draw the frame for transmitting the data 0xAB (LSB first) under the following conditions: 1 start bit, 8 data bits, 2 stop bits, no parity bit. If the Baud rate is 9600, how much time will be required to transmit 1 Kilo Byte data? **(15)**

(b) Suppose you want to measure the pulse width of an active high signal which is connected to the PB 6 pin. The CH1 of TIM4 is connected to PB 6 as AF2. The system frequency is 16 MHz. You configured the timer in input capture mode and enabled the timer Interrupt at both edges. The prescaler is set to 15999 so that the pulse width is measured in milliseconds. **(20)**

(i) Which interrupts of TIM4 will do enable if you want to measure delays accurately even if the timer counter overflows?

(ii) The ARR is 0xFFFF. Complete the code snippet shown in Fig. for Q. No. 8(b)(i). Assume the signal is 0 at the beginning. You may declare additional variables. The timer SR register is shown in Fig. for Q. No. 8(b)(ii).

```
volatile int overflow = 0;
volatile int time = 0; // put the pulse width in ms here

void TIM4_IRQHandler(void) {

}
```

Fig. for Q. No. 8(b)(i)

TIMx status register (TIMx_SR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			CC4OF	CC3OF	CC2OF	CC1OF			TIF		CC4IF	CC3IF	CC2IF	CC1IF	UIF
			rc_w0	rc_w0	rc_w0	rc_w0			rc_w0		rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Fig. for Q. No. 8(b)(ii)

Course Outcomes of EEE 415:

CO1	**Explain** the architecture, instruction set, memory and input/output interface of a ARM Microprocessor
CO2	**Design** Embedded Systems solutions with relevant appropriate consideration
CO3	**Illustrate** emerging technologies and trends in Microprocessor design to recognize the need to always learn the state-of-the art

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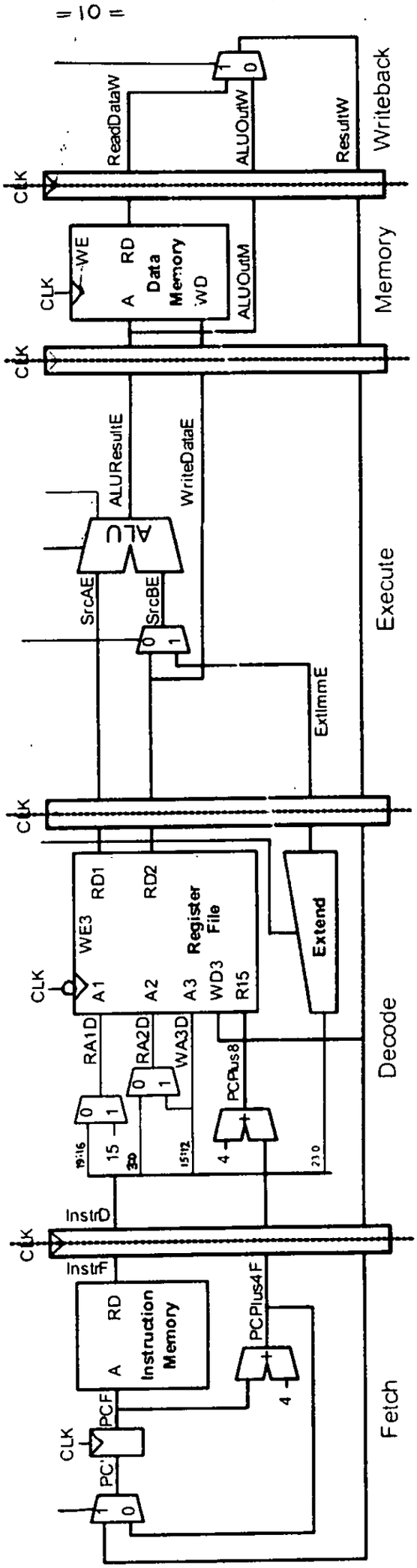

Figure for Question no. 2(a)

Contd. --- P/11

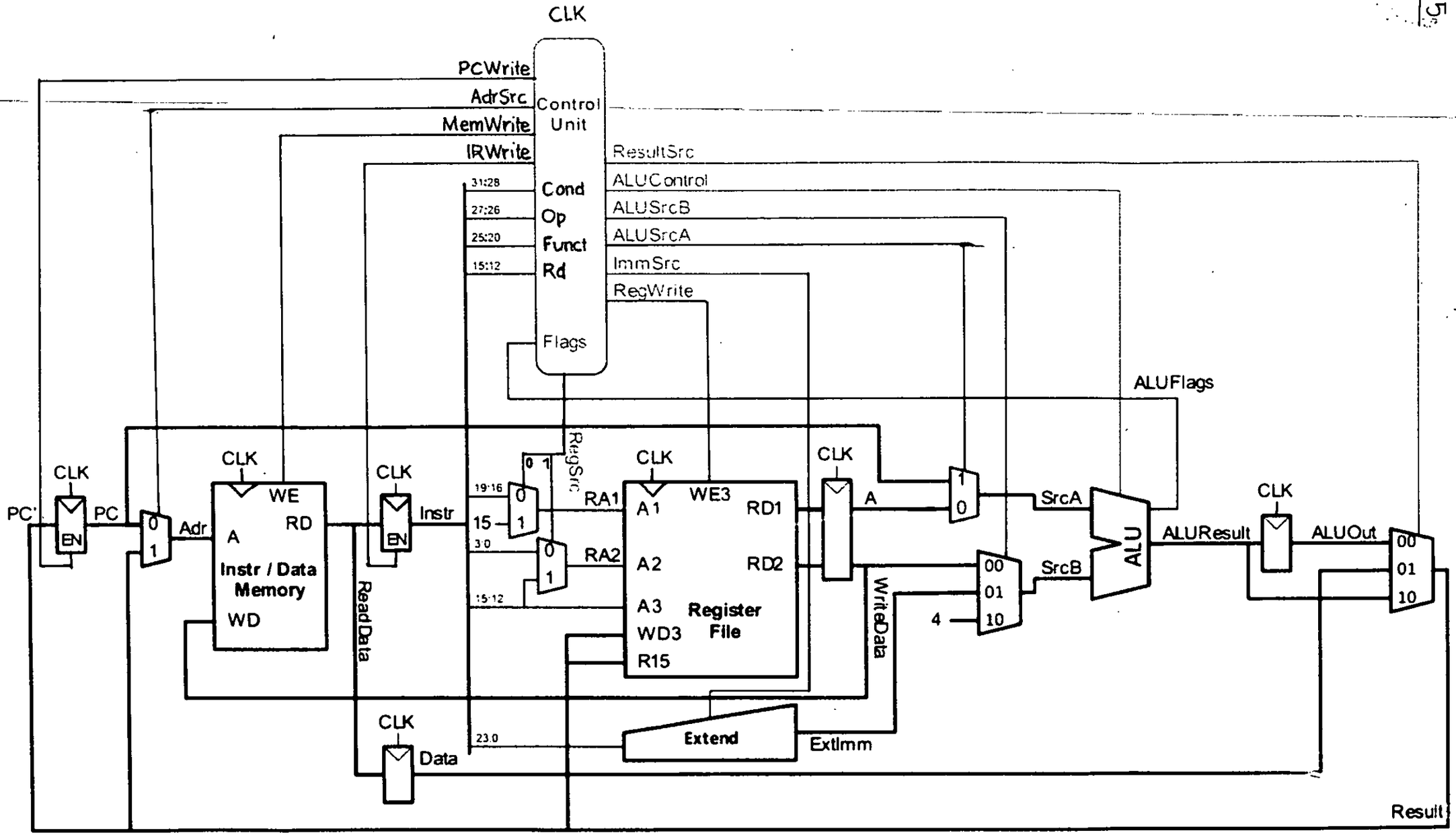

Figure for Question no. 3(a)

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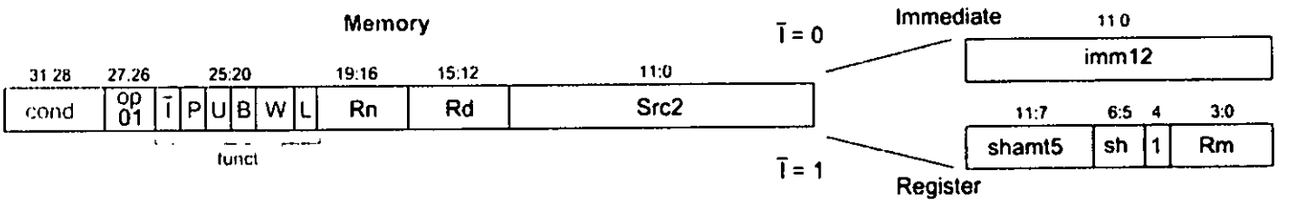
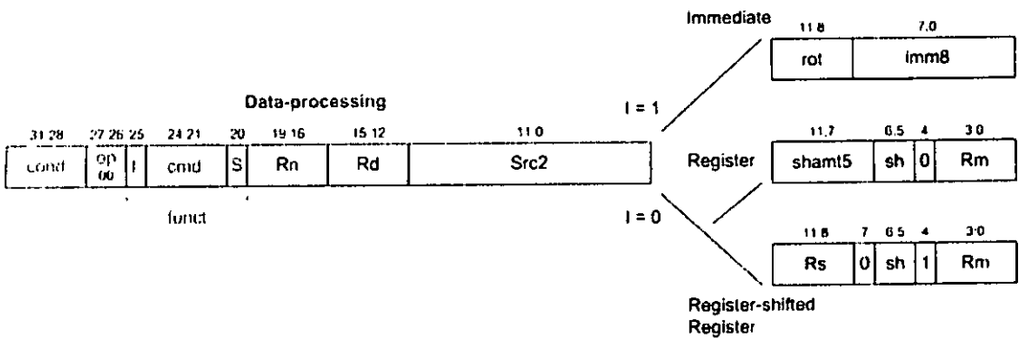
Appendix for Question no 4(b)





P	W	Index Mode
0	0	Post-index
0	1	Not supported
1	0	Offset
1	1	Pre-index

L	B	Instruction
0	0	STR
0	1	STRB
1	0	LDR
1	1	LDRB

Instruction	sh
LSL	00_2
LSR	01_2
ASR	10_2
ROR	11_2

cmd	Name
0000	AND Rd, Rn, Src2
0001	EOR Rd, Rn, Src2
0010	SUB Rd, Rn, Src2
0011	RSB Rd, Rn, Src2
0100	ADD Rd, Rn, Src2
0101	ADC Rd, Rn, Src2
0110	SBC Rd, Rn, Src2
0111	RSC Rd, Rn, Src2
1000 ($S = 1$)	TST Rd, Rn, Src2
1001 ($S = 1$)	TEQ Rd, Rn, Src2
1010 ($S = 1$)	CMP Rn, Src2
1011 ($S = 1$)	CMN Rn, Src2
1100	ORR Rd, Rn, Src2
1101	Shifts:
$I = 1$ OR ($\text{instr}_{11:4} = 0$)	MOV Rd, Src2
$I = 0$ AND ($sh = 00$; $\text{instr}_{11:4} \neq 0$)	LSL Rd, Rm, Rs/shamt5
$I = 0$ AND ($sh = 01$)	LSR Rd, Rm, Rs/shamt5

cond	Mnemonic
0000	EQ
0001	NE
0010	CS/HS
0011	CC/LO
0100	MI
0101	PL
0110	VS
0111	VC
1000	HI
1001	LS
1010	GE
1011	LT
1100	GT
1101	LE
1110	AL (or none)

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-4/T-2 B.Sc. Engineering Examinations 2021-2022

Sub: **EEE 433 (Microwave Engineering)**

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks

USE SEPARATE SCRIPTS FOR EACH SECTION

Corresponding Course Outcomes (COs) of each part of Question 1 and 5 are mentioned on the right most column. The COs of the Course are mentioned at the end of the question paper.

SECTION – A

There are **FOUR** questions in this section. Answer to Question no 1 is compulsory.

Answer any 2 questions from questions 2-4.

1. (a) Consider the circuit shown in Fig. for Q. 1(a). Determine the scattering parameters of the circuit. **(12)** **(CO3)**

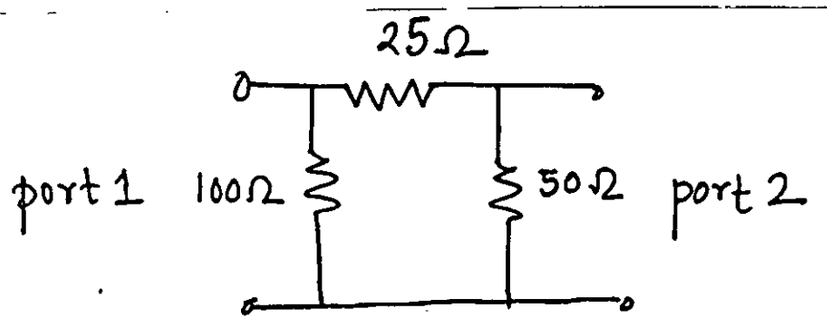


Fig. for Q. 1(a)

b) A four-port network has the scattering matrix is given by: **(8)** **(CO3)**

$$[S] = \begin{bmatrix} 0.2\angle 50° & 0 & 0 & 0.4\angle -45° \\ 0 & 0.6\angle 45° & 0.7\angle -45° & 0 \\ 0 & 0.7\angle -45° & 0.6\angle 45° & 0 \\ 0.4\angle -45° & 0 & 0 & 0.5\angle 45° \end{bmatrix}$$

(i) Is this network lossless?

(ii) Is this network reciprocal?

(iii) What is the return loss at port 1 when all other ports are terminated with matched loads?

(c) Two four-element antenna arrays are shown in Fig. for Q. 1 (c). Determine sketch and compare the group patterns of the antenna arrangements. **(15)** **(CO4)**

Contd P/2

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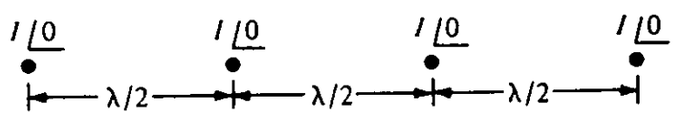
Contd... Q. No. 1(c)



(a)

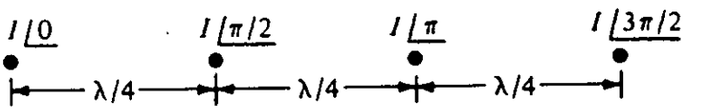


Fig. for Q. 1 (c)

2. a) Derive the expression for Q of a TE_{mmm} mode in a cube a=b=d. Show that Q increases as m increases for a given dielectric and resonant frequency. Comment on the result. The field expressions of TE_{mnp} mode for an $a \times b \times d$ rectangular resonator are given below: **(20)**

$$H_z = C\cos\left(\frac{m\pi x}{a}\right)\cos\left(\frac{n\pi y}{b}\right)\sin\left(\frac{p\pi z}{d}\right)$$

$$H_x = -\frac{C}{k_c^2}\left(\frac{p\pi}{d}\right)\left(\frac{m\pi}{a}\right)\sin\left(\frac{m\pi x}{a}\right)\cos\left(\frac{n\pi y}{b}\right)\cos\left(\frac{p\pi z}{d}\right)$$

$$H_y = -\frac{C}{k_c^2}\left(\frac{p\pi}{d}\right)\left(\frac{m\pi}{b}\right)\cos\left(\frac{m\pi x}{a}\right)\sin\left(\frac{n\pi y}{b}\right)\sin\left(\frac{p\pi z}{d}\right)$$

$$E_x = \frac{j\omega\mu C}{k_c^2}\left(\frac{n\pi}{b}\right)\cos\left(\frac{m\pi x}{a}\right)\sin\left(\frac{n\pi y}{b}\right)\sin\left(\frac{p\pi z}{d}\right)$$

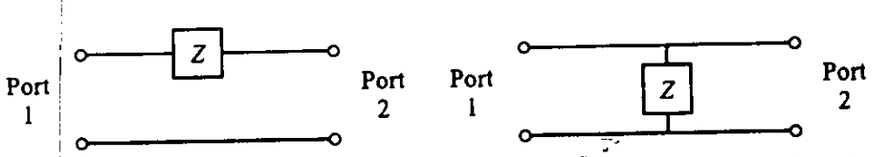
$$E_y = -\frac{j\omega\mu C}{k_c^2}\left(\frac{m\pi}{a}\right)\sin\left(\frac{m\pi x}{a}\right)\cos\left(\frac{n\pi y}{b}\right)\sin\left(\frac{p\pi z}{d}\right)$$

$$E_z = 0$$

Assume that the surface resistivity $R_s = 1\ \Omega$ and the resonator is filled with air.

b) Find the scattering parameters for the series and shunt loads shown in Fig. for Q. 2(b). **(15)**

Show that, $S_{12} = 1 - S_{11}$ for the series case, and that $S_{12} = 1 + S_{11}$ for the shunt case. Assume the characteristic impedance is given by Z_0.



3. a) For a half-wave dipole antenna, the magnetic vector potential due to $I = I_0\cos(\beta z)$ current distribution is given by: **(20)**

$$A_{zs} = \frac{\mu I_0 e^{-j\beta r}\cos\left(\frac{\pi}{2}\cos\theta\right)}{2\pi r\beta\sin^2\theta}, A_{\phi s} = 0 \text{ and } A_{\theta s} = 0$$

Show that the magnetic field at far-field is given by:

$$H_{\phi s} = j\frac{I_0 e^{j\beta r}\cos\left(\frac{\pi}{2}\cos(\theta)\right)}{2\pi r\sin\theta}$$

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Contd... Q. No. 3

b) A magnetic field strength of $5\mu A/m$ is required at a point on $\theta = \frac{\pi}{2}$, 2 km from an antenna in air. Neglecting ohmic loss, how much power must the antenna transmit if it is **(10)**

(i.) Hertzian Dipole of length $\lambda/25$?

(ii.) A half-wave dipole?

c) Explain the term "Directive Gain" with necessary equations. **(5)**

4. a) The transmitting and receiving antennas are separated by a distance of 200λ and have directive gains of 25 and 18 dB respectively. If 5 mW of power is to be received, calculate the minimum transmitted power. **(10)**

b) The radiation intensity of a certain antenna is given by: **(13)**

$U(\theta, \phi) = 10\cos^2\theta \sin^2\frac{\phi}{2}, 0 < \theta < \pi, 0 < \phi < \frac{\pi}{2}$

Determine the directive gain and directivity.

c) In free space, an antenna radiates a field, **(12)**

$$E_{\phi s} = \frac{0.2\cos^2\theta}{4\pi r} e^{-j\beta r} \text{ kV/m}$$

at far field. Determine the total radiated power and directive gain at $\theta = 60°$.

List of relevant Equations (The symbols have their usual meanings)

$$\begin{bmatrix} A_r \\ A_\theta \\ A_\phi \end{bmatrix} = \begin{bmatrix} \sin\theta\cos\phi & \sin\theta\sin\phi & \cos\theta \\ \cos\theta\cos\phi & \cos\theta\sin\phi & -\sin\theta \\ -\sin\phi & \cos\phi & 0 \end{bmatrix} \begin{bmatrix} A_x \\ A_y \\ A_z \end{bmatrix}$$

$$\nabla \times \mathbf{A} = \frac{1}{r^2\sin\theta}\begin{vmatrix} \mathbf{a}_r & r\mathbf{a}_\theta & (r\sin\theta)\,\mathbf{a}_\phi \\ \frac{\partial}{\partial r} & \frac{\partial}{\partial\theta} & \frac{\partial}{\partial\phi} \\ A_r & rA_\theta & (r\sin\theta)\,A_\phi \end{vmatrix}$$

$$= \frac{1}{r\sin\theta}\left[\frac{\partial}{\partial\theta}(A_\phi\sin\theta) - \frac{\partial A_\theta}{\partial\phi}\right]\mathbf{a}_r + \frac{1}{r}\left[\frac{1}{\sin\theta}\frac{\partial A_r}{\partial\phi} - \frac{\partial}{\partial r}(rA_\phi)\right]\mathbf{a}_\theta$$

$$+ \frac{1}{r}\left[\frac{\partial}{\partial r}(rA_\theta) - \frac{\partial A_r}{\partial\theta}\right]\mathbf{a}_\phi$$

Contd P/4

EEE 433

SECTION – B

There are **FOUR** questions in this section. Answer to Question no 5 is compulsory.

Answer any 2 questions from questions 6-8.

5 (a) Derive the equations of constant resistance and constant reactance circle of a Smith's chart. **(15)**

(CO1)

(b) For a rectangular waveguide with dimension a and b, show that for TE_{mn} mode, H_z component is given by: **(15+5=20)**

(CO2)

$$H_z(x,y,z) = A_{mn}\cos\left(\frac{m\pi x}{a}\right)\cos\left(\frac{n\pi x}{b}\right)e^{-j\beta z}$$

Also determine the expression of the cut-off frequency corresponding to the TE_{mn} mode. The symbols have their usual meaning.

6. (a) Drawing the lumped equivalent circuit, derive the general solutions for voltage and current on a two-conductor lossless transmission line. **(18)**

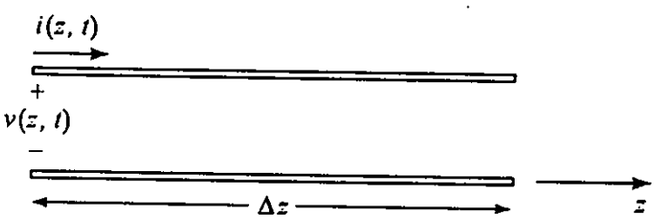

Fig. Q6 (a)

(b) A lossless transmission line of electrical length $\ell = 0.3\lambda$ and $Z_0 = 75\,\Omega$ is terminated with a complex load impedance $Z_L = 30 - j20\,\Omega$. Find the reflection coefficient at the load, the SWR on the line, the reflection coefficient at the input of the line, and the input impedance to the line. **(17)**

7. (a) Starting from Maxwell's curl equations, prove that for a source free lossless waveguide, **(13)**

$$H_x = \frac{j}{k^2 - \beta^2}\left(\omega\epsilon\frac{\partial E_z}{\partial y} - \beta\frac{\partial H_z}{\partial x}\right)$$

where symbols have their usual meaning. Then re-write the equation for lossy propagation.

(b) For a rectangular plate waveguide with dimensions a and b, the field components of TE_{10} mode are given by: **(15)**

Contd P/5

Contd... Q. No. 5(b)

$$H_z = A_{10}\cos\frac{\pi x}{a}e^{-j\beta z},$$

$$E_y = \frac{-j\omega\mu a}{\pi}A_{10}\sin\frac{\pi x}{a}e^{-j\beta z},$$

$$H_x = \frac{j\beta a}{\pi}A_{10}\sin\frac{\pi x}{a}e^{-j\beta z},$$

$$E_x = E_z = H_y = 0.$$

Determine the net power flow in the direction of propagation for $f > f_c$ and $f < f_c$ where f_c is the cut off frequency.

(c) Define TE, TM and TEM modes in context of a parallel plate waveguide. **(7)**

8. (a) What is single-stub tuning in the context of transmission line. For shunt stub, derive the expression for optimal stub length and stub position. **(10)**

(b) Design a single-section quarter-wave matching transformer to match a 12 Ω load to a 60 Ω transmission line at $f_0 = 30$ GHz. Determine the percent bandwidth for which the SWR ≤ 1.5. **(15)**

(c) A TE_{11} wave is propagating through a circular waveguide. The diameter of the waveguide is 10cm, and the waveguide is air-filled. Use table 8(c) if necessary. **(10)**

i. Find the cut-off frequency.

ii. Find the wavelength λ_g in the guide for a frequency of 3GHz.

iii. Determine the wave impedance in the guide.

Table 8(c): Values of p'_{mn} for TE Modes of a Circular Waveguide

n	p'_{n1}	p'_{n2}	p'_{n3}
0	3.832	7.016	10.174
1	1.841	5.331	8.536
2	3.054	6.706	9.970

Course Outcomes of EEE 433

COs	CO Statement
CO1	Explain the circuit model and different aspects of lossless and lossy transmission lines.
CO2	Employ electromagnetic theory to understand wave propagation in different waveguide structures.
CO3	Explain the techniques of solving microwave networks.
CO4	Design different types of antennas with specific radiation properties and antenna parameters.

L-4/T-2/EEE **Date : 24/03/2024**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-4/T-2 B. Sc. Engineering Examinations 2021-2022

Sub : **EEE 437** (Wireless Communications)

Full Marks : 210 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer to Question no 1 is compulsory. Answer any 2 questions from Questions 2-4. The corresponding Course Outcomes (COs) of each part of Question 1 are mentioned on the right most column below the marks. The COs of the Course are mentioned at the end of the question paper. The symbols have their usual meanings.

1. (a) Consider a 4x3 flat-fading MIMO channel where only the receiver knows CSI. There are three possible states of the channel-**H1, H2** and **H3** with probabilities 0.3, 0.45, 0.25, respectively. The diagonal elements of diagonal matrix by Eigen decomposition of channel matrices **H1, H2** and **H3** are found to be {4, 3, 2}, {4.5, 3.5, 2.5} and {4.5, 3, 2.8}, respectively. Determine the ergodic capacity of the channel in bps/Hz if the average SNR of each receiver antenna, E_s/N_0 is 10 dB. **(17)** *(CO2)*

   (b) Assuming that the average SNR per branch is 11 dB, design a SC diversity system to meet the following criteria- **(18)** *(CO2)*

   (i) the average received SNR ≥ 15 dB and

   (ii) outage probability ≤ 0.02 with the requited SNR threshold to be 12 dB.

2. (a) Explain the reasons of popularity of OFDM communication in wireless broadband communications. Also compare among FDM, OFDM and OFDMA systems. **(10)**

   (b) Explain the operation of baseband transmission using OFDM transmitter and receiver. **(15)**

   (c) Explain how to design block length and cyclic prefix length in OFDM for increasing the power efficiency of OFDM Syatem. **(10)**

3. (a) Show that a static MIMO channel can be presented as *r* SISO channels when both the transmitter and receiver know CSI. Also explain how the capacity of the system can be maximized by Water-Filling Algorithm. **(18)**

   (b) Starting from the voltage signal, derive the expression of average SNR for MRC of *M* branches each with average SNR of Γ. **(17)**

Contd P/2

EEE 437

4. (a) Explain the functions of e-NodeB, P-GW, S-GW and MME in LTE Communications. **(12)**

   (b) Explain the duplexing method in LTE System including the arrangement of duplexing flexibility. **(11)**

   (c) Describe the operation of Linear Decorrelator Detector and mention its advantages and disadvantages. **(12)**

SECTION – B

There are **FOUR** questions in this section. Answer any to Question No 5 is compulsory.

Answer any two from Question 6-8.

All the symbols have their usual meanings. Assume reasonable value for missing data.

5. (a) Write down the challenges associated with wireless channel. Describe log distance path loss model with log normal shadowing. Calculate the received power at a distance of 3 km from the transmitter if the path-loss exponent is 4. Assume the transmitting power of 4 W at 1800 MHz, a shadow effect of 10.5 dB, and the power at reference distance (d_0 = 100m) of -32dBm. What is the allowable path loss? **(18)** *(CO2)*

   (b) Consider a wideband channel with multiple intensity profile as **(9)** *(CO3)*

$$A_c(\tau) = \begin{cases} e^{-3\tau}, & 0 \le \tau \le 15\,\mu\text{sec} \\ 0, & else \end{cases}$$

   Find the mean and rms delay spreads of the channel and find the maximum symbol period such that a linearly modulated signal transmitted though this channel does not experience ISI.

   (c) Define coherence time and coherence bandwidth of a channel. **(4)** *(CO3)*

   (d) Write down the factors that influence the small scale fading. **(4)** *(CO1)*

6. (a) Define channel capacity. The joint probability of a system is given in the following. Find marginal entropies, joint entropy, conditional entropies, mutual information, channel capacity. **(18)**

$$p(x,y) = \begin{matrix} x_1 \\ x_2 \\ x_3 \end{matrix} \begin{bmatrix} 0.3 & 0.2 \\ 0.1 & 0.1 \\ 0.15 & 0.15 \end{bmatrix}$$

   (b) Consider a wireless channel where power falloff with distance follows the formula $P_r(d) = P_t(d_0/d)^3$ for d_0 = 20 m. Assume the channel has bandwidth B = 500 kHz and AWGN with noise power spectral density of $N_0 = 10^{-9}$ W/Hz. For a transmit power of 15W, find the capacity of this channel for a transmit-receive distance of 1.0 km, and 1.5 km. **(17)**

Contd P/3

EEE 437

7. (a) Consider a flat-fading channel with i.i.d. channel gain g[i] which can take on three possible values: sqrt(gl) = 0.55 with probability p1 = 0.1, sqrt(g2) = 0.75 with probability p2 = 0.1, and sqrt(g3) = 0.95 with probability p3 = 0.8. The transmit power is 100 mW, the noise spectral density is $N_0 = 10^{-9}$ W/Hz, and the channel bandwidth is 200 KHz. Assume the receiver has knowledge of the instantaneous value of g[i], but the transmitter does not. Find the Shanon capacity of this channel and compare with the capacity of an AWGN channel with the same average SNR. **(18)**

   (b) Derive symbol error rate (SER) for MQAM for AWGN channel. Draw bit error rate (BER) versus E_b/N_0 for different M and explain the variation with respect to M, E_b/N_0. **(17)**

8. (a) Comment on the bit error rate (BER) for BPSK and QPSK systems and explain briefly. Draw the block diagram of QPSK transmitter and receiver systems. **(18)**

   (b) Derive the average bit error rate (BER) for BPSK in Rayleigh fading channel. Draw the average BER versus average SNR curve for AWGN channel and Rayleigh fading channel and explain. **(17)**

Course Outcomes of EEE 437

COs	CO Statement
CO1	**Understand** the radio wave propagation and apply the knowledge of physics, mathematics, and engineering to model wireless channel
CO2	**Understand** the various transmission schemes for wireless communications, **apply** the knowledge of mathematics as well as propagation models, and **analysis** and **evaluation** of the performances of various transmission schemes
CO3	**Design** the parameters of wireless communication system so that certain requirements are satisfied

L-4/T-2/EEE **Date: 22/04/2024**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-4/T-2 B.Sc. Engineering Examinations 2021-2022

Sub: **EEE 443 (Radar and Satellite Communication)**

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks

The corresponding Course Outcomes (COs) of each part of Question 1 and 5 mentioned on the right most column. The (COs) of the Course are mentioned at the end of the question paper.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are FOUR questions in this section. Answer to Question No. 1 is compulsory.

Answer any TWO questions from Questions 2-4.

Assume reasonable values for any missing data only if necessary. Symbols carry their usual meanings

Answer in brief and to the point.

1. (a) Name 6 factors that affect radar performance. Mention, with brief statements, the basic principle of operation of radar. Define monostatic and bi-static radars. **(6+9)**

Write down the expression for the power density at a distance R form a directive antenna transmitting a power of P_t Watts. Assuming a monostatic radar, derive the ultimate received power, P_r at the receiving antenna form a target at a distance R, in terms of the relevant parameters, G. A_e and σ. (CO3)

(b) Draw the common repetitive train of short-duration pulses to be used as radar transmitter signal and show the typical values of peak power, pulse width, target return power, average power, PRI and f_p, and it duty cycle. What would be the duty cycle corresponding to a continuous wave (CW) radar? **(5+5)** (CO3)

Define the maximum unambiguous range, and hence derive its equation. Using the derived equation, polt the maximum unambiguous range versus the pulse repetition frequency, f_p (Use the three specific values, of f_p = 500Hz, 1000Hz and 1500Hz and a linear scale).

(c) Why is power amplification accomplished in multiple stages? Mention the use of a magnetron transmitter in radar applications and mention its limitations. **(4+6)**

With a neat sketch, describe the basic operation of a Klystron transmitter in brief and mention where it is used. Can solid-state transmitters be used instead of TWTs? (CO3)

2. (a) Comment on the power requirements and resolution of a radar system. Why is it hard to get a good average power and better resolution at the same time in pulsed continuous wave radar? **(6+7)**

Explain, with neat sketches, how the pulse compression technique allows a radar to simultaneously achieve the energy of a long pulse and the resolution of a short pulse.

Contd..... Page/2

EEE 443

(b What is a standard dipole? Show its dimension in a sketch in terms of λ. What is its output impedance? What is the impedance of free space? If a dipole is used for radiation in free space, can it ensure maximum power transfer? Explain why or why not. **(5+7)**

Define antenna pattern. Write down the equation for the gain of a standard dipole antenna and draw its antenna pattern in a polar plot. Determine the maximum gain in dBi.

(c) With neat sketches, define a phased array antenna and mention its advantages over the reflection antennas in radar applications.

Distinguish between a passive- and an active phased array radar. Mention the specifications of the **PAVE PAWS** radar that is used by the US military. **(5+5)**

3. (a) Answer the following questions in brief. **(5 x 4=20)**

(i) Write down the track- and search-radar range equations separately and elaborate the terms used.

(ii) State the functions of an Airport Surveillance Radar (ASR)? Mention its frequency of operation and average power.

(iii) State the principle of detecting the flight of a moving target by a modern radar. How can this principle be used to detect clutter?

(iv) State the main features of a ground probing radar.

(b) Define a Polarimetric radar. With neat sketches, show the single polarized and fully polarized (dual-pol) radars. For a linearly polarized radar system, write down the equation for the scattering-or S-matrix and explain the terms. **(6+9)**

The principle of a TDM MIMO radar is depicted in **Fig. for Q. No. 3(b)** with 3 Tx and 3 Rx antennas. Using standard procedure, determine and draw the equivalent virtual array and formulate the corresponding S-matrix. Use $\eta = k \,.\, e_d$ with e_d being the unit vector in the direction of the Rx array elements, and k is the unit vector in the direction of wave propagation.

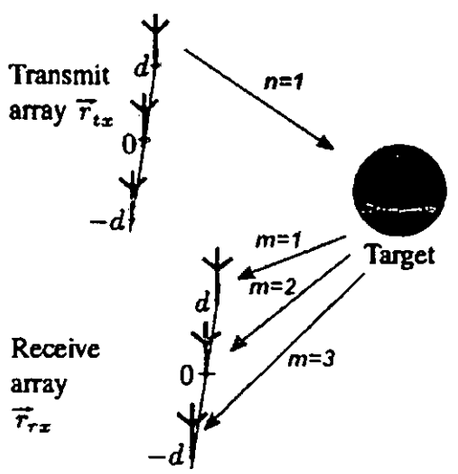

Fig. for Q. No. 3(b).

Contd..... Page/3

EEE 443

4. (a) *" A GPS receiver monitors multiple satellites and solves equations to determine the precise position of the receiver and its deviation form true time."* - Explain the statement and briefly clarify how the GPS receiver calculates its precise position on or above the earth. **(10)**

(b) Draw a simplified block diagram of the coarse acquisition (C/A) code generator used on GPS satellites and mention how a code is generated for specific satellite. Describe the characteristic of such a code along with the timing and modulation technique used for the navigation signal. **(12)**

(c) The received power level for a typical C/A signal from an early GPS satellite is given by the downlink budget in Table 1. The C/A code is transmitted at a bit rate of 1.023Mcps using BPSK modulation. The receiver IF noise bandwidth is assumed to be 2MHz, and T=273^{0}K. **(13)**

Table 1: Downlink budget for GPS C/A code.

Satellite EIRP	26.8 dBW
Path loss	186.8 dB
Receiving antenna gain	0 dB
Received Power, P_r	−160.0 dBW (0.1×10^{-15} W)

(i) Calculate the interference, ***I*** form **nine** interfering satellite spread spectrum **signals** of equal power for the C/A code.

(ii) Calculate the thermal noise N_t.

(iii) Calculate the **CNR** = $C/(N_t+I)$ in dB.

(iv) Compute the ***theoretical coding gain*** for a 1023 chip code sequence in dB.

(v) Obtain the ***overall SNR*** in dB.

(vi) Calculate the final ***effective SNR*** in dB by adding 13 dB processing gain for using a reduced bandwidth toward 50Hz.

Also, comment on the ***bit error rate.***

SECTION – B

There are FOUR questions in this section. Answer to Question No. 5 is compulsory.

Answer any TWO questions from Questions 6-8.

5. (a) Write the names of the different sub-systems in Space Segment and Grond Segment of a satellite communication system. Also explain the functions of the sub-systems for effective communication. **(18)** (CO1)

(b) Consider a geostationary satellite system at KU-band. The uplink and downlink parameters are given below. Design the transmitter antenna at ground station and receiver antenna at earth station assuming aperture efficiency of 0.6. Assume, the distance between ground station to satellite as well as satellite to earth station is 38500 km. **(17)**

Contd..... Page/4

EEE 443

(Continuation to Q. No. 5(b)

Uplink Parameters (Ground Station to Satellite)

Transponder noise temperature= 500K

Receiver noise bandwidth= 43.2MHz

Required uplink carrier to noise ratio, C/N= 30 dB

Uplink Carrier frequency= 14.15 GHz

Satellite receiver antenna gain= 31 dB

Other Losses= 3 dB

Transmit Power= 30 dBW

Downlink Parameters (Satellite to Earth Stations):

Overall carrier to noise ratio, C/N= 17 dB

Satellite transponder output power= 18 dBW

Receiving system noise temperature = 140K

Receiver noise bandwidth = 43.2 MHz

Downlink Carrier frequency= 11.45 GHz

Other losses= 4dB

Satellite antenna gain= 31 dB

6. (a) Describe the different types of orbital satellites with characteristics, brief operation mechanism, advantages, disadvantages and applications. **(17)**

(b) Explain the effects of rain in satellite communication. Mention how the effects of rain are mitigated in satellite communications. **(10)**

(c) Explain Kepler's Third Law and show how the radius of a circular orbit is measured. **(8)**

7. (a) Explain the function and operation of IDEMUX and HPA in satellite transponder. **(10)**

(b) How antennas are used in practice in satellite? Also explain how multiple beams are generated by satellite antennas? **(12)**

(c) With necessary diagrams explain the operation of a earth station receiver. **(13)**

8. (a) Describe the operation of mobile satellite communications. **(12)**

(b) Write down the operation, advantages and disadvantages of VSAT Polling Network Configuration. **(12)**

(c) Explain the operation of Orthogonal Polarization Multiple Access Technique. **(11)**

EEE 443

Course Outcomes of EEE 443

COs	CO Statement
CO1	**Understand** the underlying technology of satellite communications and networking.
CO2	**Design** appropriate link parameters, orbit, and modulation schemes for satellite communications.
CO3	**Understand** the essential concepts of radar systems.

L-4/T-2/EEE **Date: 22/04/2024**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-4/T-2 B.Sc. Engineering Examinations 2021-2022

Sub: **EEE 461 (Semiconductor and Nano Device)**

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks

The corresponding Course Outcomes (COs) of each part of Question 1 and 5 mentioned on the right most column. The (COs) of the Course are mentioned at the end of the question paper.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are FOUR questions in this section. Answer to Question No. 1 is compulsory.

Answer any TWO questions from Questions 2-4.

1. (a) Assume a junction between semi-infinite GaAs and A1GaAs materials with a step potential of 0.34 eV at the junction. Find the T-matrix for the step potential. (Consider electron's mass = 9.109×10^{-31} kg and Planck's constant = 6.626×10^{-34} J-s). Discuss how the elements of the matrix vary with the variation of the electron energy. **(20)** (CO2)

   (b) What is the condition for ballistic transport in a device? How can you design a transistor to achieve ballistic transport between the source and drain? **(15)** (CO3)

2. (a) How does interface roughness impact carrier transport through a material? Explain. **(15)**

   (b) What are the differences between electron scattering mechanisms due to phonons and photons? **(10)**

   (c) What assumptions were made when calculating the electron scattering rate due to phonon interactions? **(10)**

3. (a) How does temperature affect the electron scattering rate due to phonons? **(10)**

   (b) Can quasi-elastic approximation be applied to electron scattering due to longitudinal optical phonons? Explain. **(10)**

   (c) How does the electron distribution in two energy levels impact the scattering rate between them due to photons? What will determine whether electrons will scatter form a Lower energy level to a higher one and vice versa due to interaction with photons? **(15)**

4. (a) Classically derive the expression of the total power dissipated from a material when a harmonic light wave is incident on it. Use this expression to find the quantum-mechanical expression of the photo-induced conductivity. **(20)**

   (b) How is the data stored in flash memory device? How should you choose the dielectric layer thickness between the floating gate and the channel between the drain and the source in a flash memory device? **(15)**

Contd..... Page/2

EEE 461

SECTION – B

There are FOUR questions in this section. Answer to Question No. 5 is compulsory.

Answer any TWO questions from Questions 6-8.

5. (a) For a 1D monatomic lattice, show that **(20)**

(CO1)

$$\omega = \sqrt{\frac{4C}{m}}\left|\sin\frac{ka}{2}\right|$$

From there, demonstrate that at long wavelength propagation is dispersionless, and the phase velocity and group velocity both are equal to,

$$v_0 = a\sqrt{\frac{C}{m}}$$

In both equations, the symbols have their usual meaning.

(b) Consider an 1-D chain of atoms where the lattice vibration is characterized by an elastic constant of $2.2\times10^5\, gm/s^2$. The lattice constant and mass of the atoms are 5.4 angstrom and 28 amu. In the dispersion less propagation regime, what is the velocity of the wave propagation in the medium? Also calculate the cutoff frequency. **(15)**

[1 amu $=1.665\times10^{-27}\, kg$] (CO1)

6. (a) For a di-atomic molecule with masses m and M, the dispersion relation is - **(20)**

$$\omega^2 = \frac{C(m+M)}{mM}\left[1\pm\sqrt{1-\frac{4mM\sin^2 ka}{(m+M)^2}}\right]$$

Where all the symbols have their usual meaning. Determine the optical and acoustic branch frequencies at the edge of the Brilloin zone (k=0 and $\pm\pi/2a$).

(b) What happens to the energy of attenuated waves above cutoff frequency? Illustrate your answer with an example of the frequency 1% above the cut off. **(15)**

7. (a) Based on the harmonic oscillations model, derive the expression of internal energy and specific heat of a material. Also define Einstein's temperature based on your derivation and comment on the validity of the model in low and high temperature limits. **(20)**

(b) Define Reststrahlen peak. Between NaCl and GaAs, in which material do you expect the Reststrahlen effect to be stronger? Why? **(15)**

8. (a) Based on the tight-binding model, show with necessary equations how bringing a pair of wells of identical atoms causes the energy level to split into two levels. **(20)**

(b) "Effective mass of a particle can change depending on the crystal/material, and even be negative" - explain with suitable equations. **(15)**

Course Outcomes of EEE 461:

CO1	**apply** the physics-based knowledge to solve problems relevant to the electrical properties of materials
CO2	**analyse** the charge carrier transport through semiconductor and nano devices based on the underlying physics
CO3	**design** electronic and optoelectronic devices such that specified performance characteristics are attained

L-4/T-2/EEE **Date: 24/03/2024**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-4/T-2 B. Sc. Engineering Examinations 2021-2022

Sub: **EEE 467** (VLSI Circuits and Design)

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks.

The corresponding Course Outcomes (COs) of each part of Question 1 and 5 are mentioned on the right most column. The COs of the Course are mentioned at the end of the question paper.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer to **Question No. 1 is compulsory.**

Answer any TWO questions from Questions 2-4.

1. (a) A 64 bit adder will be implemented in CMOS with one bit full adder as a basic building block. You have to **design** the sum circuit of the one bit full adder which is realized with the following Boolean equation to achieve minimum number of transistor counts. **(20)** (CO1, CO3)

$$S_i = A_iB_iC_i + \overline{C_{i-1}}(A_i + B_i + C_i)$$

Your design goal is to achieve the highest speed in a given process node. The following process and design related data are given:

Mobility of electron is 3 times faster than mobility of hole, the slowest input signal is $\overline{C_{i-1}}$ followed by C_i. Apply as much design consideration as you can and explain why your design will achieve higher speed.

(b) To reduce critical path delay of multiplier, a designer uses of Wallace tree type of multiplier using [4:2] compressor. Show the dot diagram of the above [4:2] binary tree multiplier summing 16 partial products and show that to sum N partial product require $[\log_2(N/2)]$ levels of (4,2) counters to reduce N inputs down to two carry-save redundant form outputs. **(15)** (CO2)

2. (a) Fig. for Q. 2(a) shows the self-bypass paths for six separate ALUs of a microprocessor. The path for one of the ALUs begins at registers containing the inputs to an adder, as shown in the Figure. The adder must compute the sum. A result multiplexer chooses between this sum, the output of the logic unit, and the output of the shifter. Then a series of bypass multiplexers selects the inputs to the ALU for the next cycle. The early bypass multiplexer chooses among results of ALUs from previous cycles and is not on the critical path. The 8:1 middle bypass multiplexer chooses a result from any of the six ALUs, the early bypass mux, or the register file.

Contd P/2

EEE 467

Contd... Q. No. 2(a)

The 4:1 late bypass multiplexer chooses a result from either of two results returning from the data cache (Dc1. Dc2), the middle bypass mux result (Bypass), or the immediate operand (Imm) specified by the next instruction. The late bypass mux output is driven back to the ALU to use on the next cycle. Because the six ALUs and the bypass multiplexers occupy a significant amount of area, the critical path also involves 2 mm wires from the result mux to middle bypass mux and from the middle bypass mux and from the middle bypass mux back to the late bypass mux. The propagation delays and contamination delays of the path are given in Table 1. **(21)**

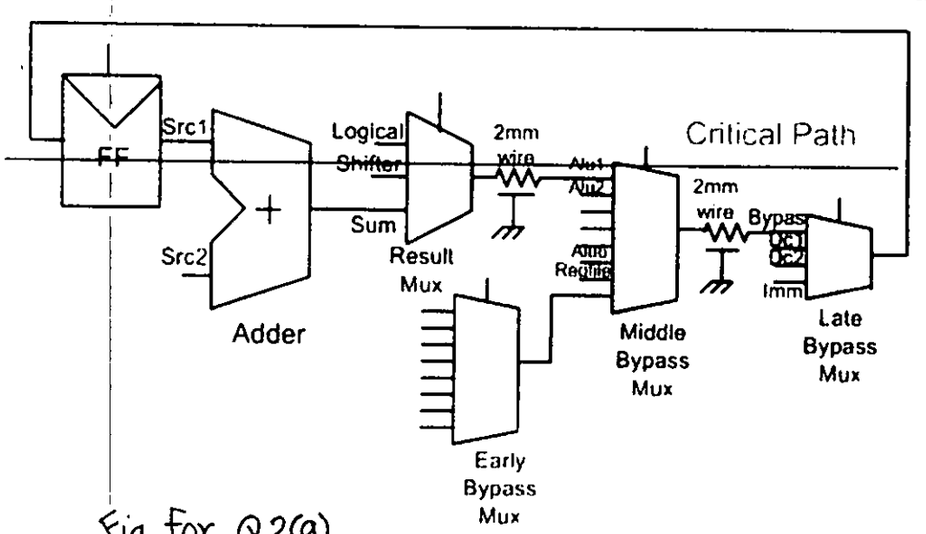

Fig for Q2(a)

Table 1

Elemetn	Propagation delay	Contamination delay
Adder	590 ps	100 ps
Result Mux	60 ps	35 ps
Early Bypass Mux	110 ps	95 ps
Middle Bypass Mux	80 ps	55 ps
Late By pass Mux	70 ps	45 ps
2mm wire	100 ps	65 ps

(i) Suppose the registers are built from flip-flops with a setup time of 62 ps, hold time of –10 ps, propagation delay of 90 ps, and contamination delay of 75 ps. Calculate the minimum cycle time Tc at which the ALU self-bypass path will operate correctly.

(ii) If the earliest input to the Late bypass multiplexer is the Imm value coming from another flip-flop, will this path experience any hold time failure?

(iii) If the ALU self-bypass path uses pulsed latches in place of flip-flops, will it have any hold time problems? How the hold time problem, if it exist, can be eliminated. The pulsed latch has a pulse width of 150 ps, a setup time of 40 ps, a hold time of 5 ps, a clock to Q propagation delay of 82 ps and a clock to Q contamination delay of 52 ps, and a D-to-Q propagation delay of 92 ps.

Contd P/3

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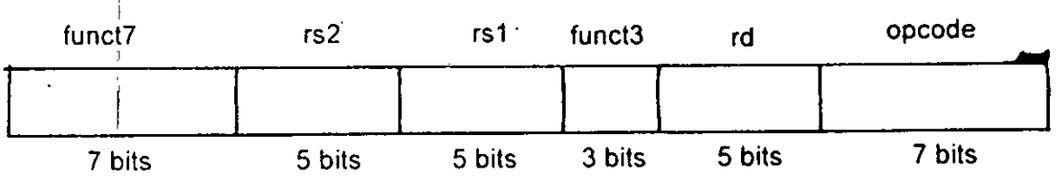
Contd... Q. No. 2

(b) What is 'clock Skew'? Explain how clock skew affect the setup time and hold time of a flip-flop based system. **(14)**

3. (a) Consider the R-type assembly code 'add x1, x2, x3' to be executed in a single cycle RISC-V processor.

(i) Show the 32 bit machine language code corresponding to the above assembly code in the box below: **(6)**



(ii) Show the schematic of the datapath along with the control lines necessary for execution of the above R-type instructions. Show the operation of the datapath for the above instruction identifying sequentially which hardwares are in operation. **(20)**

(iii) The Verilog code of the above datapath is written by someone in your company and you are required to verify the code. You are asked to build a layer testbench of the datapath. Show the schematic view of the full testbench with all the layers. Explain how you will execute the verification. **(9)**

4. (a) Consider an interface written as follows: **(15)**

```
interface my_if (input bit clk);
  bit write;
  bit [15:0] data_in;
  bit [7:0] address;
  logic [15:0] data_out;
endinterface
```

For the above interface add the following code

(i) A clocking block that is sensitive to the negative edge of the clock, and all I/O that are synchronous to the clock

(ii) A modport for the testbench called *master* and a modport for the DUB called *slave*

(iii) Use the clocking block in the I/O list for the master modport.

(b) A counter counts 0, 1, 3, 5, 7, 0,1 and so on. **(20)**

Write System Verilog code of a self checking testbench of the counter finite state machine.

Contd P/4

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SECTION – B

There are **FOUR** questions in this section. Answer to **Question No. 5 is compulsory.**

Answer any TWO questions from Questions 6-8.

5. (a) For the n-MOS inverter shown in Fig for Q 5(a), $\mu_n C_{ox} = 120\,\mu A/V^2, V_{tno} = 1V,$ $\gamma = 0.8\,V^{\frac{1}{2}}, L_1 = L_2 = 1\,\mu m,$ and $W_1 = 10\,\mu m.$ **(20)** (CO1)

(i) Find the ratio of W_2/W_1, so that for $V_I = 5\,V, V_O = 0.2\,V.$

(ii) Suppose that a CMOS inverter is designed by replacing M_2 with a p-MOS with $\mu_p C_{ox} = 60\,\mu A/V_2$, $V_{tpo} = 1V$ and the same W_2/L_2 as M_2, with its gate connected to input V_I and body connected to the $+5V$ supply. The input and output capacitances are: $C_{in} = 2pF$, $C_{out} = 1$pF. If this inverter is driving 100 identical inverters, find the rise time, fall time, and propagation delay at the node V_o.

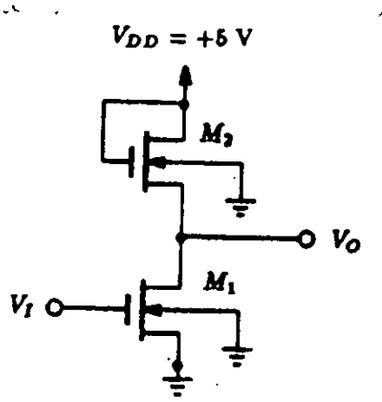

Fig for Q 5(a)

(b) (i) Implement a CMOS circuit to obtain the output $F = \overline{A(B+CD)}$, where A, B, C, D are inputs of the circuit. **(15)** (CO3)

(ii) Choose transistor widths to achieve effective rise and fall resistance equal to that of a unit inverter. Assume, $\mu_n = 2\mu_p$

(iii) Sketch equivalent R-C circuits for worst case falling and worst-case rising output transition. Assume there is not sharing or merging of diffusion nodes.

Contd P/5

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6. (a) In Fig. for Q 6(a), find al the node voltages V_1, V_2, V_3 if the nMOS parameters are $V_{to} = 1V$ and $\gamma = 0.4\, V^{\frac{1}{2}}$. Assume that the initial voltage was 0 in all the above nodes. **(15)**

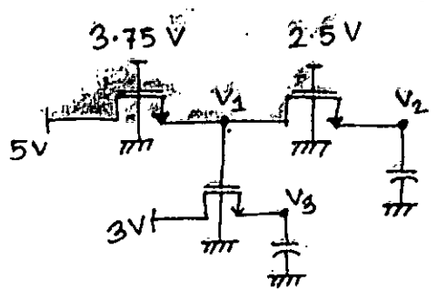

Fig. for Q 6(a)

(b) Draw the circuit diagram of an 8-to-1 MUX with nMOS pass transistor logic. **(13)**

(c) What is a domino gate? Draw the circuit diagram of a domino OR gate. **(7)**

7. (a) In Fig. for Q 7(a), estimate the minimum delay of the path from A to B (shown using dashed line) and choose transistor sizes to achieve this delay. The initial NAND2 gate may present a load of 16λ of transistor width. [For a n-input NAND gate, logical effort is (n+2)/3 and parasitic delay is n. For an n-input NOR gate, logical effort is (2n + 1)/3 and parasitic delay is n.] **(18)**

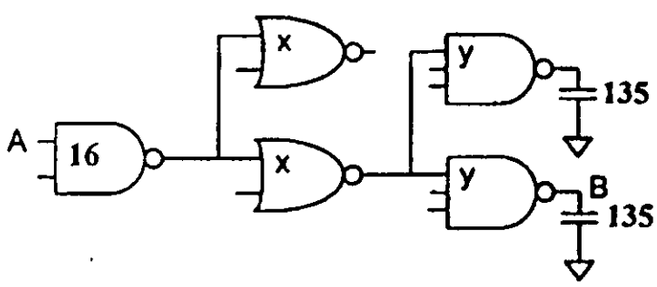

Fig. for Q 7(a)

(b) An 81-bit data path is to be driven by a unit inverter with C_{in} = 0.1 pF and C_{out} = 0.1 pF. Design a buffer chain and determine the number of stages that will achieve minimum delay. **(10)**

(c) A 31-stage ring oscillator is fabricated in a 0.6 μm process with τ = 60 ps. Find the oscillator frequency. **(7)**

Contd P/6

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8. (a) Draw the transistor level circuit diagram of a 4×4 bit NAND ROM which stores the following data: **(10)**

	B3	B2	B1	B0
W0	1	0	1	0
W1	0	1	0	0
W2	0	0	1	1
W3	1	0	0	1

(b) Draw the transistor level circuit diagram of a 6 transistor SRAM with pre-charging mechanism and briefly explain the read and write operations. **(18)**

(c) A NAND based decoder circuit is used as a 12-to-4096 row decoder of a memory block. Calculate the number of transistors required if CMOS circuit is used with 2-bit pre-decoding. Assume that the inverted forms of all input bits are available. **(7)**

Course Outcomes of EEE 467

CO No.	CO Statement	Corresponding PO(s)*
CO1	Apply the physics-based mathematical models of Semiconductor device to design digital circuit to do useful operation.	PO1
CO2	Synthesis Digital circuits based on specific operational requirements.	PO2
CO3	Design digital system based on specific requirements and design constraints such as power, speed, size etc.	PO3, PO4
CO4	Apply circuit simulation tools to verify theoretical prediction of circuit performance using very complex but realistic device model.	PO5

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-4/T-2 B. Sc. Engineering Examinations 2021-2022

Sub : **EEE 477** (Power System Protection)

Full Marks : 210 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

The corresponding Course Outcomes (COs) of each part of Question 1 and 5 are mentioned on the right most column. The COs of the Course are mentioned at the end of the question paper.

SECTION – A

There are FOUR questions in this section. Answer to Question No 1 is compulsory.

Answer any 2 questions from Questions 2-4.

1. (a) In Fig. 1(a), for the following cases where was the short circuit, and was there any failure of relaying, including breakers, and if so what failed? **(9)** *(CO1)*

Case	Breaker tripped
A	4,5,8
B	3,4,5,6
C	4,5,6

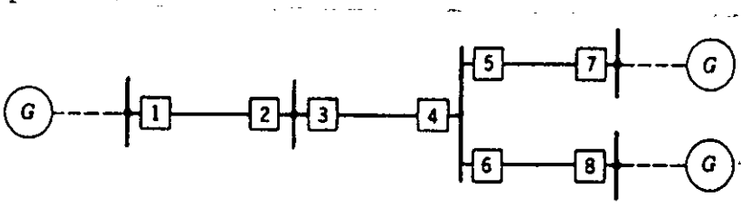

Fig. 1(a) Simple power system with circuit breaker positionings

(b) Write down your observations on Fig. 1(b). **(5)** *(CO1)*

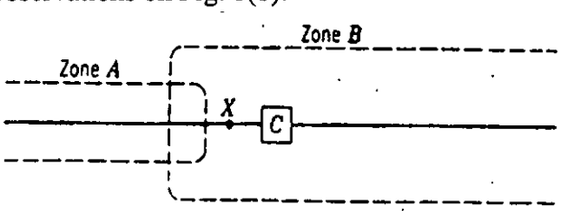

Fig. 1(b) Zones of protection

(c) "The protection of generators involves the consideration of more possible abnormal operating conditions than the protection of any other system element protection"- what are those 'abnormal operating conditions'? **(12)** *(CO2)*

(d) Discuss how errors may creep in due to poor transient performance of CTs. **(9)** *(CO3)*

Contd P/2

EEE 477
Contd ... Q. No. 2(a)

2. (a) With reference to Fig. 2(a) discuss the operating characteristics of a current-voltage directional relay. **(20)**

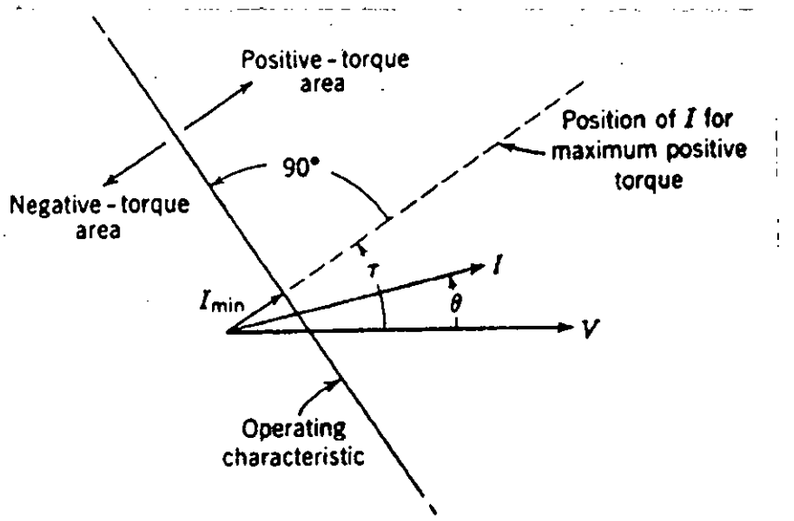

Fig. 2(a) Directional relay characteristics

(b) Present the operating principle of reactance type distance relay. What are its limitations? **(15)**

3. (a) Explain how coordination of inverse-time-overcurrent relays is achieved. **(20)**

(b) With reference to Fig. 3(b) discuss the effect of intermediate current source on distance relay operation. **(15)**

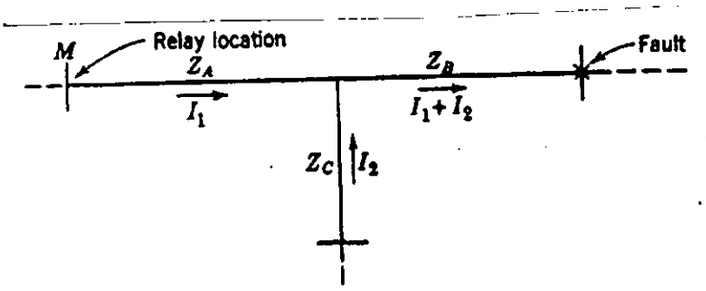

Fig. 3(b) Effect of intermediate current sources on distance-relay operation

4. (a) Why large generators need overfluxing protection? Why almost all overfluxing events occur during generator start-up? **(15)**

(b) What is pole-slip event in a generator? With reference to Fig. 4(b), discuss a technique for detecting pole slipping. **(20)**

Contd P/3

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Contd ... Q. No. 4(b)

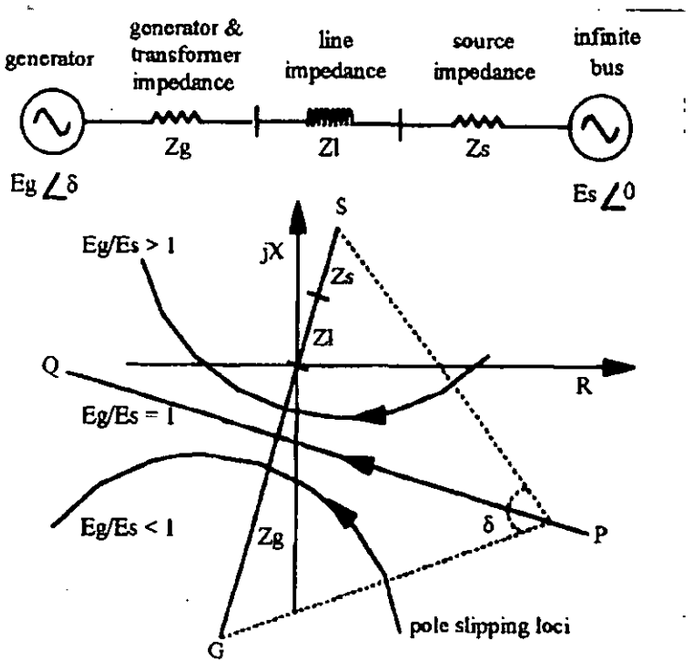

Fig. 4(b) Generator pole slipping loci

SECTION – B

There are **FOUR** questions in this section. **Answer to Question No 5 is compulsory.**

Answer any 2 questions from Questions 6-8.

5. (a) What are the 'rule of thumb' and basic requirements of CT connection for differential relays? With neat diagram, show the step-by-step procedure for CT connection for differential relays. **(20)** (*CO1*, *CO4*)

   (b) What are the methods to prevent tripping of relays when a transformer is energized? Briefly explain using diagrams. **(15)** (*CO4*)

6. (a) Write short notes on the followings for fault detection in power systems: **(16)**

   (i) magnitude comparison

   (ii) phase angle comparison

   (iii) harmonic content

   (iv) frequency sensing

   (b) With the help of connection and vector diagram using phase-to-phase voltage, describe the operating mechanism for power relays. **(10)**

   (c) Explain continuous, short-time and contact rating for relays. **(9)**

Contd P/4

EEE 477

7. (a) Mention the causes of bus faults. What are the desirable features of bus protection? **(15)**

   (b) What is current differential relaying? Explain its operating principle. Also, mention its disadvantages. **(20)**

8. (a) Explain the various methods of arc extinction in a circuit breaker. **(12)**

   (b) Based on IEC 62271-100 and IEC 62271-1, what are the parameters that determine the ratings of circuit breakers? Explain how the following rating values are selected for CBs: rated short circuit breaking current, transient recovery voltage, rated voltage. **(15)**

   (c) In a neat sketch, show the voltage and current waveforms with respect to time during fault clearing. **(8)**

Course Outcomes of EEE 477

COs	CO Statements	Corresponding Pos
CO1	Understand the fundamental philosophy of protective relaying, explain the relay and circuit breaker operating principles and functional characteristics.	PO1
CO2	Understand the different origins of power system equipment faults and analyze the equipment fault characteristics.	PO1, PO2
CO3	Understand the characteristics of current and voltage transformers and solve the problems of measurement errors in protective relaying.	PO1, PO2, PO3
CO4	Design basic protection schemes for transformer, rotating machinery, transmission line and specify their protection requirements.	PO2, PO3, PO4

L-4/T-2/EEE **Date: 22/04/2024**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-4/T-2 B.Sc. Engineering Examinations 2021-2022

Sub: **EEE 489 (Smart Grid)**

Full Marks: 210 Time: 3 Hours

The figures in the margin indicate full marks

The corresponding Course Outcomes (COs) of each part of Question 1 and 5 mentioned on the right most column. The (COs) of the Course are mentioned at the end of the question paper.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are FOUR questions in this section. Answer to Question No. 1 is compulsory.

Answer any TWO questions from Questions 2-4.

1. (a) Explain how data communication speed for smart metering is affected by the choice of the communication technology and the protocol? **(12)** (CO3)

   (b) Explain the impacts of DERs on the grid. **(12)** (CO2)

   (c) Explain how can a smart grid contribute to grid resilience? **(11)** (CO5)

2. (a) Describe the communication architecture to interface smart meters with server, and the functions of the data concentration unit and meter data management system. **(15)**

   (b) What types of communication technology and protocols may be used for smart metering. In our country which one is used? **(8)**

   (c) What are the factors for assessing protocols to be used for smart metering? **(12)**

3. (a) Discuss applications of IEC 62056 and ANSI C12.22 protocols for smart meter communication system. **(9)**

   (b) Discuss he functions of transport layers in ISO/OSI and TCP/IP protocols? **(10)**

   (c) Discuss dedicated, star, ring and multi-drop communication networks as applied in a power system or a substation. **(16)**

4. (a) Describe the control strategy for a roof top photovoltaic source tied with low voltage grid. **(20)**

   (b) Explain SAIFI, SAIDI and ASAI. How can these be improved using smart grid? **(15)**

Contd..... Page/2

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SECTION – B

There are FOUR questions in this section. Answer to Question No. 5 is compulsory.

Answer any TWO questions from Questions 6-8.

5. (a) Give an overview of the technologies required for the smart grid. **(16)** (CO4)

   (b) Describe various kinds of implementation of incentive based DSI schemes. **(10)** (CO6)

   (c) Mention the key motives behind the implementation of smart grid. **(9)** (CO1)

6. (a) Mention the major differences between Smart prepayment maters and AMI interfaced smart meter. **(10)**

   (b) What is AMI? Explain briefly how AMI combined with customer technologies participate in management of demand side consumption. **(10)**

   (c) Demand side resources can provide various services to power systems by modifying load consumption patterns. Give a description of such type services with suitable examples. **(15)**

7. (a) What are the major reasons for placing a microgrid in island mode? Describe briefly about the islanding process. Also describe the operating principle of a microgrid in island mode. **(11)**

Contd..... Page/3

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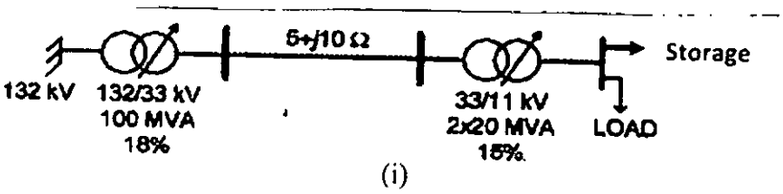
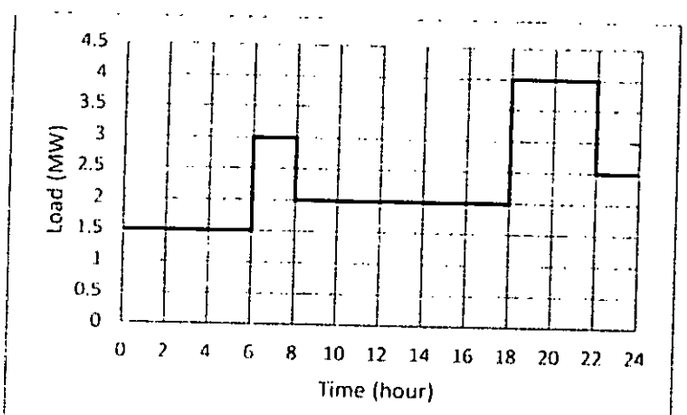
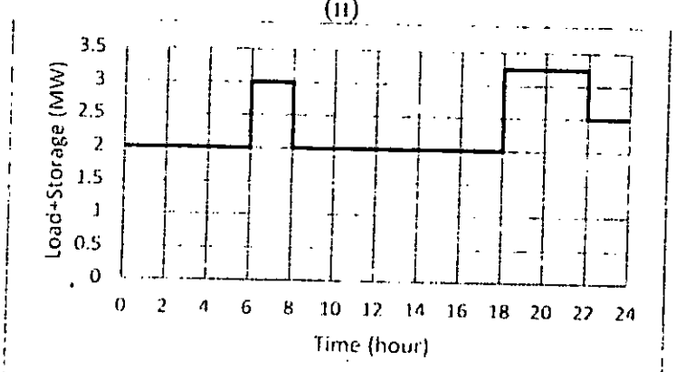
(b) Consider the circuit shown in Fig. for Q. 7(b)-(i). The 33/11 kV transformer has an on-load tap changer which maintains the load voltage at 11 kV. Load curve throughout the day is shown in Fig. for Q. 7(b)-(ii). Valley filling shown in Fig. for Q. 7(b)-(iii) is managed using a storage system for the 1st 6 hours and all the stored energy is used during peak load. Ignore the 33/11 kV transformer losses and unity power factor. **(18)**



(i)



(ii)



(iii)

Fig. for Q. 7(b)

i) Determine the peak demand for combined load and storage system.
ii) Calculate the percentage reduction in energy loss in the 33 kV line due to valley filling.

(c) What are the major obstacles to implement smart grid in Bangladesh? **(6)**

8. (a) Give a brief description of hierarchical control of a microgrid and explain how master controllers contribute to the hierarchical control. **(13)**

(b) What is HAN? Give a brief description of the services provided by HAN. **(7)**

(c) Why may the following issues create a challenge for normal operation of a conventional grid? Explain briefly. **(15)**

i. Ageing assets and lack of circuit capacity ii. Thermal constraints and iii. Operational constraints (voltage and frequency limits).

What are the solutions provided by a smart grid for the mentioned issues.

Contd..... Page/4

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COs	CO Statement
CO1	Understand the motives behind smart grid
CO2	Identity the needs and features of a smart grid
CO3	Learn the way a conventional power system (grid system) can be transformed into a smart grid
CO4	Know smart grid gadgets
CO5	Know the operational strategies of smart grid
CO6	Learn how the demand can be shaped to match available generation