HIGH PERFORMANCE NVRAM CIRCUIT DESIGN USING MEMRISTOR-MOS HYBRID ARCHITECTURE

A thesis submitted to
the Department of Electrical and Electronic Engineering
of
Bangladesh University of Engineering and Technology
in partial fulfillment of the requirements
for the degree of

MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

by,

Syed Shakib Sarwar
Student ID: 0412062230

Department of Electrical and Electronic Engineering

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY

May 2014

DECLARATION

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

(Syed Shakib Sarwar)

APPROVAL CERTIFICATE

The thesis titled "High Performance NVRAM Circuit Design Using Memristor-MOS Hybrid Architecture" submitted by Syed Shakib Sarwar, Student ID: 0412062230, Session: April 2012 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on May, 2014.

BOARD OF EXAMINERS

1.

______________________________ Chairman (Supervisor)

Dr. A.B.M. Harun-ur Rashid
Professor,
Department of EEE, BUET,
Dhaka-1000, Bangladesh

2.

______________________________ Member (Ex-Officio)

Dr. Pran Kanai Saha
Professor and Head,
Department of EEE, BUET,
Dhaka-1000, Bangladesh

3.

______________________________ Member

Dr. Md. Ziaur Rahman Khan
Professor,
Department of EEE, BUET,
Dhaka-1000, Bangladesh

4.

______________________________ Member

Dr. Zahid Hasan Mahmood
Professor, Department of Applied Physics, Electronics and Communication Engineering,
University of Dhaka.

CONTENTS

TITLE		***Page no:***
Declaration		ii
Approval Certificate		iii
Table of Contents		iv
List of Figures		vi
List of Tables		vii
Acknowledgement		viii
Abstract		ix
Chapter 01	**Introduction**	1
1.1	Memristor	1
1.2	SRAM	3
1.3	Motivation of our work	4
1.4	Thesis Outline	6
Chapter 02	**Memristor Basics**	7
2.1	A Single Memristor	7
2.2	Practical Memristor: Model of Non-Linear Dopant Drift	12
2.3	SPICE Model of Memristor with Non-Linear Dopant Drift	14
Chapter 03	**SRAM Basics**	18
3.1	SRAM	18
3.2	Conventional SRAM Types	20
3.2.1	4T-SRAM	20
3.2.2	6T-SRAM	21
3.2.3	4T2M-SRAM	23
3.2.4	3T-2M SRAM	24
Chapter 04	**Memristor Based SRAM Cell**	25
4.1	Memristor as A Memory Component	25
4.2.1	Two-Transistor Two-Memristor Memory Cell	28
4.2.2	Simulation of 2×2 Array Of Memory	32
4.3.1	Residual Voltage Effect	34

4.3.2	Contamination of Stored Data Due to Leakage	36
4.3.3	Change of Stored Data Due to Consecutive Read Operations	37
4.4	Proposed 2-T 2-M SRAM	38
4.4.1	Leaf Cell Connected with Peripheral Circuit with Complete Source Isolation	38
4.4.2	Array Structure	39
4.5	Simulation and Analysis	40
4.5.1	Functional Verification of 16×16 Array Structure	41
4.5.1.1	Write and Read Different Cells and Observe The Effect on a Single Cell	42
4.5.1.2	Write and Read Different Cells and Check the Output Values	44
4.5.2	SRAM Array with Sense Amplifier	45
4.5.2.1	Sense Amplifier	45
4.5.2.2	Array with Sense Amplifier	46
4.5.3	Non-Volatility	49
Chapter 05	**ANALYSIS AND COMPARISON**	50
5.1	Timing Analysis	50
5.2	Power Analysis	52
5.3	Layout	55
Chapter 06	**CONCLUSION AND FUTURE WORK**	57
6.1	Conclusion	57
6.2	Future Work	58
Chapter 07	**REFERENCES**	60
Appendix A:	Simulation Codes	63
Appendix B:	Memristor Modeling in MATLAB	111
Appendix C:	Exporting Data from PSPICE to MATLAB	113
Appendix D:	SPICE Convergence Problem Elimination Techniques	114
Appendix E:	Related publication	116

List of Figures

Figure no		*Page*
Figure 1.1	Relations between four variables of basic electrical circuit theory	3
Figure 2.1	A single memristor with the definition of R_{ON} and R_{OFF}	7
Figure 2.2	Theoretical i-v characteristics of a memristor with applied voltage	11
Figure 2.3	Theoretical i-v curves for a memristor with (realistic) dopant drift modeled by window functions	13
Figure 2.4	Block diagram of the memristor model	15
Figure 2.5	Structure of the SPICE model	16
Figure 2.6	Memristor with the parameters R_{ON}=100 Ω, p=10, driven by a voltage	17
Figure 3.1	Conventional SRAM cell	19
Figure 3.2	4T SRAM	21
Figure 3.3	6T SRAM	22
Figure 3.4	Structure of Non-volatile 4T SRAM cell with memristors	23
Figure 3.5	3T-2M SRAM	24
Figure 4.1	A pulsed source applied across a memristor	26
Figure 4.2	V vs Time and Rmem vs Time plot	26
Figure 4.3	V vs Time and Rmem vs Time plot with new memristor parameters	27
Figure 4.4	The 2-Memristor 2-Transistor SRAM cell	28
Figure 4.5	(a) circuit when rd=0, comb=1 (b) circuit when rd=1, comb=1	28
Figure 4.6	A CMOS pass gate is introduced for simulation	29
Figure 4.7	After writing ‘1’ (WD=1, COMB=1,RD=0), VD was read as 0.619V (COMB =1,RD=1) and After writing ‘0’ (WD=0, COMB =1,RD=0), VD was read as 0.5727V (COMB =1,RD=1)	31
Figure 4.8	(a) basic building block of a single cell (b) 2x2 array of memory	32
Figure 4.9	Plot of the read-write cycles in 2x2 array	33
Figure 4.10	‘0’ written on cell0 and read. Then ‘1’ was written on cell1 and cell0 was read. This time cell0 gives 0.9478 V much larger than ‘0’ should give due to addition of the residual voltage.	34
Figure 4.11	A NMOS controlled by Vdump signal is used to create a path to the ground for discharging the wordlines.	35
Figure 4.12	‘0’ written on cell0 and after using Vdump for 0.3ns cell0 is read. Then ‘1’ was written on cell1 and after using Vdump for 0.3ns cell0 was read. This time cell0 gives 0.5588 V which is equivalent to ‘0’.	35
Figure 4.13	(a) Series leakage path due to MOS leakage in a single cell. (b) Intra cell leakage path.	36
Figure 4.14	Leaf cell connected with peripheral circuit containing complete source isolation option	37
Figure 4.15	16×16 Array Structure of the proposed memristor based SRAM	39

Figure 4.16	Write and read different cells and observe the effect on a single cell	42
Figure 4.17	write and read different cells and check the output values	44
Figure 4.18	A simple voltage comparator	45
Figure 4.19	Comparator design specification	45
Figure 4.20	CMOS comparator with PMOS input drivers.	46
Figure 4.21	16×16 Array Structure of the proposed memristor based SRAM with sense amplifier	46
Figure 4.22	Functionality test of sense amplifier in the SRAM array circuit	48
Figure 4.23	Evidence of non-volatility of the Memristor SRAM cell	49
Figure 5.1	Timing Analysis	51
Figure 5.2	Simulation for Power Analysis	53
Figure 5.3	Layout of the SRAM cell	55

List of Tables

Table no.		***Page no.***
Table 5.1	Write and spread cycle time comparison	51
Table 5.2	Write and read cycle average energy estimation	54
Table 5.3	Write-read cycle average power comparison	54
Table 5.4	Write-read cycle average energy comparison	54
Table 5.5	Area estimation and comparison for 180nm process	56
Table 5.6	Area estimation and comparison for 45nm process	56

ACKNOWLEDGEMENT

First of all, I would like to thank the Almighty Allah for bringing me to the position where I am at this moment.

A huge amount of gratitude goes to my thesis supervisor Dr. A.B.M Harun-ur Rashid for his never ending support and guidance. His vast knowledge and expertise in the field of research always inspired me when I needed to lift my spirit. He always encouraged me to look for new technologies and scopes. He was inspirational in making me come up with the idea of my thesis work on memristor based memory element. I consider myself very lucky to have a thesis supervisor like Dr. A.B.M Harun-Ur-Rashid. And I earnestly hope to maintain an active relation with him for our future research works in the days to come.

Then, I would like to express my gratitude to my teachers and classmates who helped me along the way last one year. I would also like to thank my parents for their love and support. They always provided me with proper guidance and also gave me the freedom to choose what interested me the most.

Finally, I have tried my best to represent this thesis dissertation as appropriate as possible. I am feeling myself fortunate to finish the thesis on such an interesting topic which is really a great experience.

ABSTRACT

Scaling conventional SRAM technologies with respect to number of transistors is a big challenge and volatile memory nature of this technology is one of the biggest deficiencies. A new Memristor-MOS hybrid architecture based RAM structure has been proposed in this thesis which consumes less power and achieves nonvolatile operation (NVRAM) with less number of transistors. The thesis contains the operating procedure and the simulated results of proposed two transistors and two memristors NVRAM using TSMC 180nm CMOS technology simulated in ORCAD PSPICE 9.2. Memristors cover very little area and with only two transistors as opposed to six transistors of conventional SRAMs, the area is substantially reduced by 20.5 times. The proposed NVRAM operated with energy per cycle which is ~40 times smaller than conventional SRAMs. Though the write cycle time is higher but is still comparable, and the read cycle time is slightly lower than the conventional 6T SRAM cell. Again memristors give the circuit non-volatility which is a vital characteristic for any memory circuit. With these advantages our proposed cell can prove to have a very promising future in the field of computer memory.

Chapter 1

INTRODUCTION

Greater need for larger cache memories is growing very fast. Till date SRAM satisfies this need almost exclusively. Conventional SRAM technologies have reached a certain point where it is impossible to decrease the area of the memory in terms of number of transistors. SRAMS are also volatile in nature, they lose what was stored in them if the power is turned off. This thesis work focuses on studying a novel circuit structure for Memristor-MOS hybrid architecture NVRAM to enhance the read/write speed, reduce power consumption and minimize area.

1.1 MEMRISTOR

The properties of basic electrical circuits, constructed from three ideal elements, a resistor, a capacitor, an inductor, and an ideal voltage source v(t), are integral part of physics and engineering courses. These circuits show a wide variety of phenomena such as the exponential charging and discharging of a resistor-capacitor (RC) circuit with time constant τ_{RC} = RC, the exponential rise and decay of the current in a resistor-inductor (RL) circuit with time constant τ_{RL} = L/R, the non-dissipative oscillations in an inductor-capacitor (LC) circuit with frequency $\omega_{LC} = \frac{1}{\sqrt{LC}}$, as well as resonant oscillations in a resistor-capacitor- inductor (RCL) circuit induced by an alternating-current (AC) voltage source with frequency $\omega \sim \omega_{LC}$ [1,2,3,4] The behavior of these ideal circuits is determined by Kirchoff's current law and Kirchoff's voltage law. As Kirchoff's voltage law follows from Maxwell's second equation only when the time-dependence of the magnetic field created by the current in the circuit is ignored, $\oint E \, . \, dl = 0$ where the line integral of the electric field E is taken over any closed loop in the circuit [5] The study of elementary circuits with ideal elements provides us with a recipe to understand real-world circuits where every capacitor has a finite resistance, every battery has an internal resistance, and every resistor has an inductive component. We assume that the real-world circuits can be modeled using only the three ideal elements and an ideal

voltage source. An ideal capacitor is defined by the single-valued relationship between the charge q(t) and the voltage v(t) via *dq* = *Cdv*. Similarly, an ideal resistor is defined by a single valued relationship between the current i(t) and the voltage v(t) via *dv = Rdi*, and an ideal inductor is defined by a single-valued relationship between the magnetic flux ϕ(t) and the current i(t) via *dφ = Ldi*. These three definitions provide three relations between the four fundamental constituents of the circuit theory, namely the charge q, current i, voltage v, and magnetic flux ϕ (See Figure 1). The definition of current, i = *dq/dt*, and the Lenz's law, v = +*dφ/dt*, give two more relations between the four constituents. (We define the flux such that the sign in the Lenz's law is positive). These five relations, shown in Fig. 1, raise a natural question: Why is an element relating the charge q(t) and magnetic flux ϕ(t) missing? Based on this symmetry argument, in 1971 Leon Chua postulated that a new ideal element defined by the single-valued relationship *dφ = Mdq* must exist. He called this element memristor M, a short for memory-resistor [6]. This ground-breaking hypothesis meant that the trio of ideal circuit elements (R,C,L) were not sufficient to model a basic real-world circuit (that may have a memristive component as well). In 1976, Leon Chua and Sung Kang extended the analysis further to memristive systems [7,8]. These seminal articles studied the properties of a memristor, the fourth ideal circuit element, and showed that diverse systems such as thermistors, Josephson junctions, and ionic transport in neurons, are special cases of memristive systems [6,7,8]. Despite the simplicity and the soundness of the symmetry argument that predicts the existence of the fourth ideal element, experimental realization of a quasi-ideal memristor-defined by the single-valued relationship *dφ = Mdq* - remained elusive [9,10]. Early in 2009, Strukov and co-workers [11,12] created, using a nano-scale thin-film device, the first realization of a memristor. They presented an elegant physical model in which the memristor is equivalent to a time-dependent resistor whose value at time *t* is linearly proportional to the amount of charge *q* that has passed through it before. This equivalence follows from the memristor's definition and Lenz's law, *dφ = Mdq* ⇔ v = M(q)i. It also implies that the memristor value - memristance - is measured in the same units as the resistance.

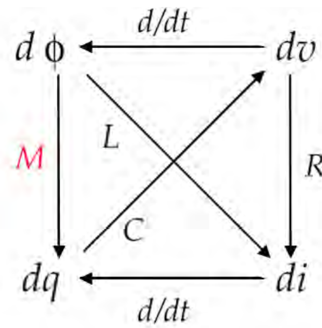


Figure 1.1: Relations between four variables of basic electrical circuit theory: the charge q, current i, voltage v and the magnetic flux ϕ. Three well-known ideal circuit elements R, C and L are associated with pairs (*dv, di*), (*dq, dv*) and (*dφ, di*) respectively. The top (bottom) horizontal pair is related by Lenz's law (definition). This leaves the pair (*dφ, dq*) unrelated. Leon Chua postulated that, due to symmetry, a fourth ideal element (memristor) that relates this pair, $d\varphi = Mdq$, must exist.

1.2 SRAM

One of the main features of computers these days is their capability to store data. Computer memory or storage refers to the physical device that stores data or programs on a temporary or permanent basis. Typically computer memory refers to RAM (Random Access Memory) where data is accessed with minimal amount of delay. RAMs can be of two types. Firstly DRAM (Dynamic Random Access Memory) where the data is stored using a transistor and a capacitance. Since capacitors leak charge, there is a need for refreshing the data periodically. Secondly there is SRAM (Static Random Access Memory), where data to be stored is latched in using cross-coupled inverters. As no capacitance is used to store data in SRAM, there is no necessity of refreshing. And it is for this reason mainly that SRAM is preferred over DRAM in many operations even though SRAM has a more complex structure and is more costly. Another advantage of SRAM over DRAM is its speed. SRAM is nearly five times faster than DRAM as it does not need any delays between accesses. But SRAMs are much more costly than DRAM due to their complex structure. So till now, SRAMs are only used in cache memory where high speed of operation is needed and a relatively small sized memory will suffice. Although SRAMs are free from the need of refreshing periodically, they are still volatile, as in they lose the stored data if or when the power supply is turned off. Conventional SRAM cells use four to six transistors. So space is also a concern for a large array of SRAM cells.

Scientists and researchers are striving for the invention of a static memory system that will be as fast as SRAM, but will be non-volatile and require less space. If these features can be combined, then it will be possible to attain a large static memory with small area which will hold data even without the power supply. So that memory will be perfectly suitable to be used as cache memory as well as flash memory for storing large amount of data. Our target was to design a new type of memory containing these advantages.

1.3 MOTIVATION OF OUR WORK

Both DRAM and SRAM must have continual power supply to hold their data. As soon as they lose power, their data are gone. One alternative approach would be to use flash memory. But it has a limited number of read-write cycles it could sustain. This characteristic clearly is not suited for random access memory (RAM) because a huge number of read-write cycles occur on them regularly. Besides, flash memory consumes a great amount of power whereas DRAM and SRAM are low power devices. Many research works have already been done on non-volatile random access memory or NVRAM. Most notable NVRAMs are Ferroelectric RAM (FeRAM), Magnetoresistive RAM (MRAM), Phase-change RAM (PRAM). Some of them broke into the market but neither of them was able to last long. There was always a concern of dimension, speed and power consumption which left conventional volatile DRAM and SRAM technology a better choice. There are also some differences between DRAM and SRAM. DRAM requires the data to be refreshed periodically in order to retain the data. SRAM does not need to be refreshed as the transistors inside would continue to hold the data as long as the power supply is not cut off. This behavior leads to a few advantages, such as much faster speed that data can be written and read. The additional circuitry and timing needed to introduce the refresh creates some complications that make DRAM memory slower and less desirable than SRAM. One complication is the much higher power used by DRAM memory. This difference is very significant in battery powered devices. SRAM modules are also much simpler compared to DRAM, which makes it easier for most people to create an interface to access the memory. This makes it easier to work with for hobbyists and even for prototyping.

Structurally, SRAM needs a lot more transistors in order to store a certain amount of memory. A DRAM module only needs a transistor and a capacitor for every bit of data where SRAM needs 6 transistors. Because the number of transistors in a memory module determines its capacity, a DRAM module can have almost 6 times more capacity with a similar transistor count to an SRAM module. This ultimately boils down to price, which is what most buyers are really concerned with. Because of its lower price, DRAM has become the mainstream in computer main memory despite being slower and more power hungry compared to SRAM. SRAM memory is still used in a lot of devices where speed is more crucial than capacity. The most prominent use of SRAM is in the cache memory of processors where speed is very essential, and the low power consumption translates to less heat that needs to be dissipated. So to fight against DRAM to be the computer main memory, SRAM needs to be smaller in area i.e. reduction in the number of transistors in a single cell. Recent emergence of memristor and their capability of storing non-volatile memory have given a boost to the researchers. In some memristor symposiums, it has been hypothesized that memristor in a crossbar structure can hold enormous amount of data in a small area. This devices is very small, could be less than 10nm of length. Some works on crossbar structure have already been done [13,14]. It can also be implemented with conventional CMOS technology which is called Memristor-CMOS Hybrid circuits. In 2010, Kamran Eshraghian *et. al.* successfully implemented memristor-mos content addressable memory [15]. So, it might be possible to design SRAM cells with memristor as memory element and MOS which might need fewer transistors than conventional SRAM cell and also possess the non-volatility characteristic.

1.4 THESIS ORGANIZATION

This thesis proposes a SRAM structure for retaining the feature of needlessness of periodic refreshing and combining with it the features of less area and non-volatility. The thesis paper has been organized in the following manner:

Chapter 2: Gives an idea of the memristor basics, mentions the model of non-linear dopant drift in practical memristors, shows the SPICE modeling of a memristor,

Chapter 3: Introduces the SRAM, different structures of conventional SRAM systems and Memristor based SRAM systems.

Chapter 4: First introduces initially proposed SRAM cell with two transistors and two memristors, then shows the residual voltage problem and leakage problem in array structure, and describes how the problems were overcome in final proposed structure. Then introduces sense amplifier, shows the non-volatility characteristics of the memory circuit, and verifies and explains the final array structure with simulation results.

Chapter 5: Gives the timing analysis, power analysis, area estimation from layout of leaf cell and finally compares the obtained results with conventional SRAM cell characteristics.

Chapter 6: Summarizes the outcome of our proposed non-volatile SRAM cell and discusses the future improvements or works to be done on this circuit.

Chapter 2

MEMRISTOR BASICS

Memristors have been studied intensively among many researchers because of their possibilities, especially as a strong candidate for future memories. Non-volatile property and high packing density in a crossbar array particularly excites the researchers.

2.1 A SINGLE MEMRISTOR

We start this chapter with the elegant model of a memristor presented in Ref 11 and 12. It consisted of a thin film (5 nm thick) with one layer of insulating TiO_2 and one layer of oxygen-poor TiO_{2-x}, each sandwiched between platinum contacts. The oxygen vacancies in the second layer behave as charge +2 mobile dopants. These dopants create a doped TiO_2 region, whose resistance is significantly lower than the resistance of the undoped region. The boundary between the doped and undoped regions, and therefore the effective resistance of the thin film, depends on the position of these dopants. It, in turn, is determined by their mobility μ_v (~10^{-10} $cm^2/V.s$) and the electric field across the doped region [2] Figure 2.1 shows a schematic of a memristor of size D (D~10 nm) modeled as two resistors in series, the doped region with size w and the undoped region with size (D−w).

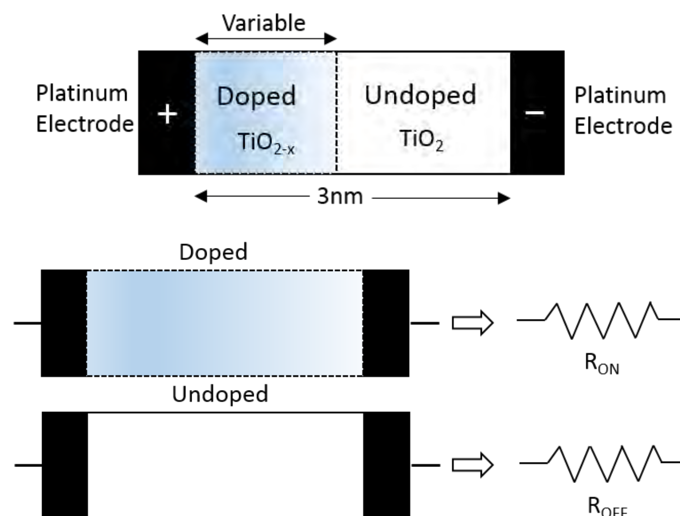


Figure 2.1: A single memristor with the definition of R_{ON} and R_{OFF}

The effective resistance of such a device is

$$\mathrm{M}(w) = \mathrm{R_{ON}}\frac{\mathrm{w}}{\mathrm{D}} + \mathrm{R_{OFF}}\left(1 - \frac{\mathrm{w}}{\mathrm{D}}\right) \qquad (2.1)$$

where R_{ON} (~1k) is the resistance of the memristor if it is completely doped, and R_{OFF} is its resistance if it is undoped. Although Eq.(2.1) is valid for arbitrary values of R_{ON} and R_{OFF}, experimentally, the resistance of the doped TiO_2 film is significantly smaller than the undoped film, $R_{OFF}/R_{ON} \sim 10^2 \gg 1$ and therefore $\Delta R = (R_{OFF} - R_{ON}) \approx R_{OFF}$. In the presence of a voltage v(t) the current in the memristor is determined by Kirchoff's voltage law v(t) = M(w)i(t). The memristive behavior of this system is reflected in the time-dependence of size of the doped region w(t). In the simplest model - the linear-drift model - the boundary between the doped and the undoped regions drifts at a constant speed v_D given by

$$\mathrm{v}_D = \frac{dw}{dt} = \eta\frac{\mu_D R_{ON}}{D}i(t) \qquad (2.2)$$

where we have used the fact that a current i(t) corresponds to a uniform electric field $R_{ON}i(t)/D$ across the doped region. Since the (oxygen vacancy) dopant drift can either expand or contract the doped region, we characterize the "polarity" of a memristor by η = ±1, where η = +1 corresponds to the expansion of the doped region. We note that "switching the memristor polarity" means reversing the battery terminals, or the ± plates of a capacitor (in an MC circuit) or reversing the direction of the initial current (in an ML circuit). Equations (2.1), (2.2) are used to determine the i-v characteristics of a memristor. Integration of Eq.(2.2) gives

$$w(t) = w_0 + \eta\frac{\mu_D R_{ON}}{D}q(t) = w_0 + \eta\frac{D}{Q_0}q(t) \quad (2.3)$$

where w_0 is the initial size of the doped region. Thus, the width of the doped region w(t) changes linearly with the amount of charge that has passed through it $Q_0 = D^2/\mu_D R_{ON}$ is the charge that is required to pass through the memristor for the dopant boundary to move through distance D (typical parameters [11,12] imply $Q_0 \sim 10^{-2}$ C). It provides the natural scale for charge in a memristive circuit. Using this result in Eq.(2.1) gives

$$M(q) = R_0 + \eta \frac{\Delta R q}{Q_0} \qquad (2.4)$$

where, $R_0 = R_{ON}(w_0/D)+R_{OFF}(1-w_0/D)$ is the effective resistance (memristance) at time t = 0. Eq.(2.4) shows explicitly that the memristance M(q) depends purely on the charge q that has passed through it. Combined with v(t) = M(q)i(t), Eq.(2.4) implies that the model presented here is an ideal memristor. (We recall that v = M(q)i is equivalent to *dφ = Mdq*). The factor of the q-dependent term is proportional to $1/D^2$ and becomes increasingly important when D is small. In addition, for a given D, the memristive effects become important only when $\Delta R \gg R0$. Now that we have discussed the memristor model from Ref. 2.1, in the following paragraphs we obtain analytical results for its i-v characteristics. For an ideal circuit with a single memristor and a voltage supply, Kirchoff's voltage law implies

$$(R_0 + \eta \frac{\Delta R q(t)}{Q_0}) \frac{dq}{dt} = \frac{d}{dt}\left(R_0 q + \eta \frac{\Delta R q^2}{2Q_0}\right) = v(t) \qquad (2.5)$$

The solution of this equation, subject to the boundary condition q(0) = 0 is,

$$q(t) = \frac{Q_0 R_0}{\Delta R}\left[1 - \sqrt{1 - \eta \frac{2\Delta R}{Q_0 R_0^2}\phi(t)}\right] \qquad (2.6)$$

$$q(t) = \frac{v(t)}{R_0} \frac{1}{\sqrt{1 - 2\eta \Delta R \phi(t)/Q_0 R_0^2}} = \frac{v(t)}{M(q(t))} \qquad (2.7)$$

where $\phi(t) = \int_0^t d\tau v(\tau)$ is the magnetic flux associated with the voltage v(t). Equations (2.6)-(2.7) provide analytical results for i-v characteristics of an ideal memristor circuit. Eq.(2.6) shows that the charge is an invertible function of the magnetic flux [6,7] consistent with the defining equation *dφ = M(q)dq*. Eq.(2.7) shows that a memristor does not introduce a phase-shift between the current and the voltage, i = 0 if and only if v = 0. Therefore, unlike an ideal capacitor or an inductor, is a purely dissipative element [16]. For an AC voltage $v(t) = v_0 \sin(\omega t)$,

the magnetic flux is $\phi(t) = v_0[1 - \cos(\omega t)]/\omega$. Note that although $v(\pi/\omega - t) = v(t)$, $\phi(\pi/\omega - t) \neq \phi(t)$. Therefore, it follows from Eq.(2.7) that the current i(v) will be a multivalued function of the voltage v. It also follows that since $\phi \propto 1/\omega$, the memristive behavior is dominant only at low frequencies $\omega \ll \omega_0 = 2\pi/t_0$. Here $t_0 = D^2/\mu_D v_0$ is the time that the dopants need to travel distance D under a constant voltage v_0. t_0 and ω_0 provide the natural time and frequency scales for a memristive circuit (typical parameters [11,12] imply t_0~0.1 ms and ω_0 ~ 50 KHz). We emphasize that Eq.(2.6) is based on the linear-drift model, Eq.(2.2), and is valid [2] only when the charge flowing through the memristor is less than $q_{max}(t) = Q_0(1-w_0/D)$ when $\eta = +1$ or $q_{max}(t) = Q_0 w_0/D$ when $\eta = -1$. It is easy to obtain a diversity of i-v characteristics using Eqns.(2.6) and (2.7), including those presented in Ref. 2.1 and 2.2 by choosing appropriate functional forms of v(t). Figure 3 shows the theoretical i-v curves for $v(t) = v_0 \sin(\omega t)$ for $\omega = 0.5\omega_0$ (red solid), $\omega = \omega_0$ (green dashed), and $\omega = 5\omega_0$ (blue dotted). In each case, the high initial resistance R_0 leads to the small slope of the i-v curves at the beginning. For $\omega \leq \omega_0$ as the voltage increases, the size of the doped region increases and the memristance decreases. Therefore, the slope of the i-v curve on the return sweep is large creating a hysteresis loop. The size of this loop varies inversely with the frequency ω. At high frequencies, $\omega = 5\omega_0$, the size of the doped region barely changes before the applied voltage begins the return sweep. Hence the memristance remains essentially unchanged and the hysteretic behavior is suppressed. The inset in Fig. 2.2 shows the theoretical q-ϕ curve for $\omega = 0.5\omega_0$ that follows from Eq.(2.6). Thus, a single memristor shows a wide variety of i-v characteristics based on the frequency of the applied voltage. Since the mobility of the (oxygen vacancy) dopants is low, memristive effects are appreciable only when the memristor size is nano-scale. Now, we consider an ideal circuit with two memristors in series (Fig. 2.1). It follows from Kirchoff's laws that if two memristors M1 and M2 have the same polarity, $\eta_1 = \eta_2$, they add like regular resistors, $M(q) = (R_{01} + R_{02}) - \eta(\Delta R_1 + \Delta R_2)q(t)/Q_0$ whereas when they have opposite polarities, $\eta_1\eta_2 = -1$, the q-dependent component is suppressed, $M(q) = (R_{01} + R_{02}) - \eta(\Delta R_1 - \Delta R_2)q(t)/Q_0$. The fact that memristors with same polarities add in series leads to the possibility of a superlattice of memristors with micron dimensions instead of the nanoscale dimensions. We emphasize that a single memristor cannot be scaled up without losing the memristive effect

because the relative change in the size of the doped region decreases with scaling. A superlattice(large chain of series connected memristors) of nano-scale memristors, on the other hand, will show the same memristive effect when scaled up.

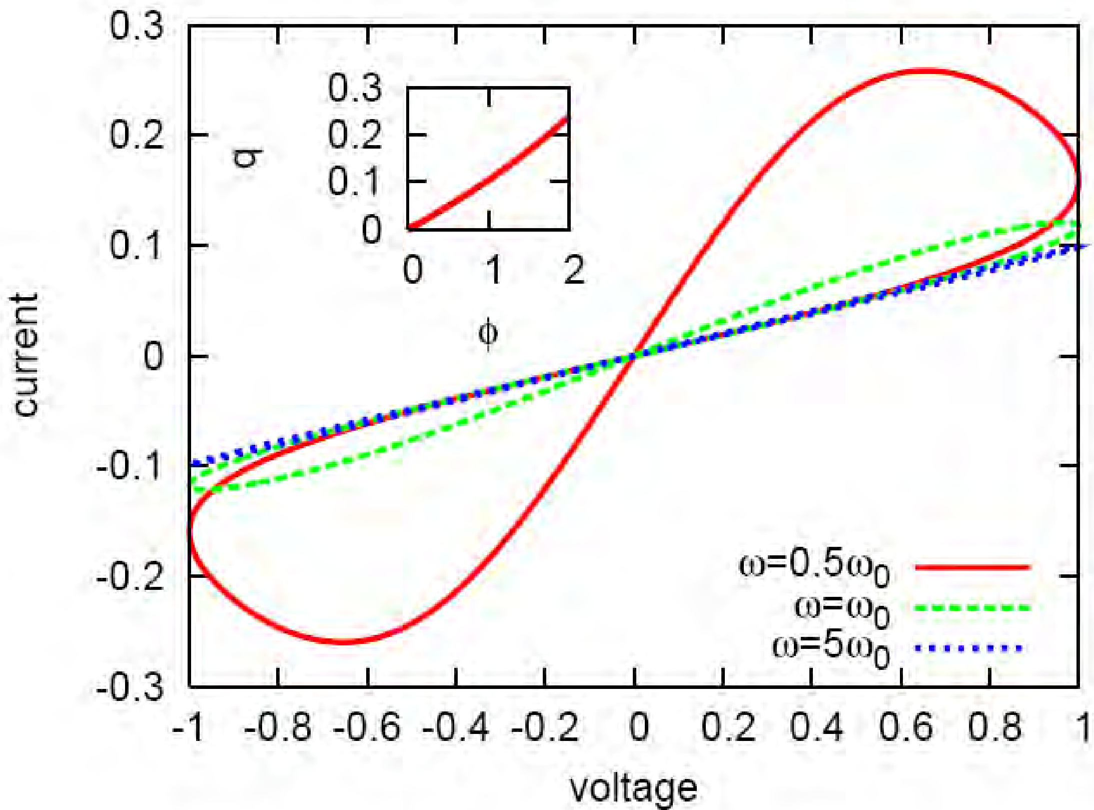


Figure 2.2: Theoretical i-v characteristics of a memristor with applied voltage $v(t) = v_0 \sin(\omega t)$ for $\omega = 0.5\ \omega_0$ (red solid), $\omega = \omega_0$ (green dashed), and $\omega = 5\ \omega_0$ (blue dotted). The memristor parameters are $w_0/D = 0.5$ and $R_{OFF}/R_{ON} = 20$. The unit of resistance is RON, the unit of voltage is v_0, and the unit of current is $I_0 = Q_0/t_0$. We see that the hysteresis is pronounced for $\omega \leq \omega_0$ and suppressed when $\omega \gg \omega_0$. The inset is a typical q- ϕ graph showing that the charge q is an invertible function of the flux ϕ. The unit of flux $\phi_0 = v_0 t_0 = D^2/\mu_D$ is determined by the memristor properties alone (typical parameters imply $\phi_0 = 10^{-2}$ Wb).[2]

2.2 PRACTICAL MEMRISTOR: MODEL OF NON-LINEAR DOPANT DRIFT

The linear-drift model used in preceding sections captures the majority of salient features of a memristor. The linear drift model suffers from one serious drawback: it does not take into account the boundary effects. Qualitatively, the boundary between the doped and undoped regions moves with speed v_D in the bulk of the memristor, but that speed is strongly suppressed when it approaches either edge, w ~ 0 or w ~ D. We modify Eq.(2.2) to reflect this suppression as follows Ref. 11

$$\frac{dw}{dt} = \eta \frac{\mu_D R_{ON}}{D} i(t) F\left(\frac{w}{D}\right) \qquad (2.8)$$

The window function F(x) satisfies F(0) = F(1) = 0 to ensure no drift at the boundaries. The function F(x) is symmetric about x = 1/2 and monotonically increasing over the interval $0 \le x \le 1/2$, $0 \le F(x) \le 1 = F(x = 1/2)$. These properties guarantee that the difference between this model and the linear-drift model, Eq.(2.2), vanishes in the bulk of the memristor as w → D/2. Motivated by this physical picture, we consider a family of window functions parameterized by a positive integer p, $F_p(x) = 1 - (2x - 1)^{2p}$. Note that Fp(x) satisfies all the constraints for any p. The equation $F_p(x) = 0$ has 2 real roots at x = ±1, and 2(p−1) complex roots that occur in conjugate pairs. As p increases $F_p(x)$ is approximately constant over an increasing interval around x = 1/2 and as p → ∞, $F_p(x) = 1$ for all x except at x = 0, 1.

Thus, $F_p(x)$ with large p provides an excellent non-linear generalization of the linear-drift model without suffering from its limitations. We note that at finite p Eq.(2.8) describes a memristive system [7,11] that is equivalent to an ideal memristor [11,6] when p →∞ or when the linear-drift approximation is applicable. It is instructive to compare the results for large p with those for p = 1, $F_{p=1}(x) = 4x(1 - x)$, when the window function imposes a non-linear drift over the entire region $0 \le w \le D$ [11]. For p = 1 it is possible to integrate Eq.(2.8) analytically and we obtain

$$w_{p=1}(q) = w_0 \frac{D\, exp\left(\frac{4\eta q(t)}{Q_0}\right)}{D + w_0\left[exp\left(\frac{4\eta q(t)}{Q_0}\right) - 1\right]} \qquad (2.9)$$

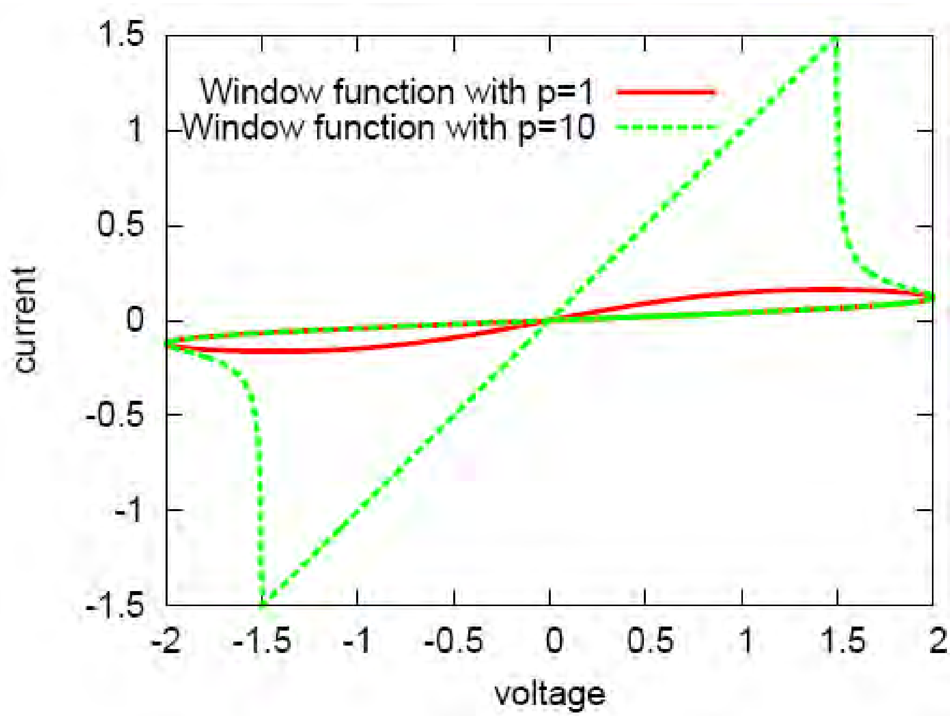


Figure 2.3: Theoretical i-v curves for a memristor with (realistic) dopant drift modeled by window functions $F_p(x) = 1-(2x-1)^{2p}$ with p = 1 (red solid) and p = 10 (green dashed), in the presence of an external voltage $v(t) = 2v_0 \sin(\omega_0 t/2)$. The memristor parameters are $w_0/D = 0.5$ and $R_{OFF}/R_{ON} = 50$.[2]

2.3 SPICE MODEL OF MEMRISTOR WITH NON-LINEAR DOPANT DRIFT:

Zdeněk BIOLEK et. al. showed an efficient technique of modeling the memristor with active circuit elements [16]. The Ohm's law relation is applicable between the memristor voltage and current:

$$v(t)=R_{MEM}(w)\, i(t) \qquad (2.10)$$

The speed of the movement of the boundary between the doped and undoped regions depends on the resistance of doped area, on the passing current, and on other factors according to the state equation

$$\frac{dx}{dt} = ki(t)f(x) \qquad (2.11)$$

Which can be found letting $x = \frac{w}{D}$ and $= \frac{\mu_D\, R_{ON}}{D^2}$. The window function is then

$$f(x) = 1 - (2x - 1)^{2p} \qquad (2.12)$$

State equation (2.10) and port equation (2.11) of the memristor can be modeled by the block oriented diagram in Fig. 2.4. The memory effect of the memristor is modeled via a feedback controlled integrator. With regard to the limiting boundary conditions, it stores the effects of the passing current, and controls the memristor resistance via modifying the boundary position. The nonlinear drift and the influence of the boundary conditions are modeled by the feedback via the nonlinear window function *f*( ).

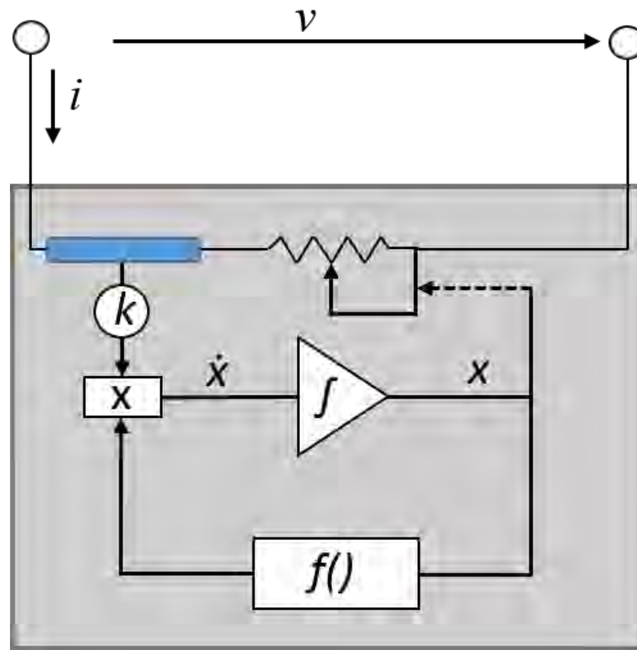


Figure 2.4: Block diagram of the memristor model

The structure of the SPICE model is shown in Fig. 2.5. The relation between the memristor voltage and current is modeled on the basis of the modified equation (2.11):

$$\mathrm{R_{MEM}}(x) = \mathrm{R_{OFF}} - \mathrm{x\Delta R} \quad (2.13)$$

In Fig. 2.5, equation (2.13) corresponds to the R_{OFF} resistor in series with the *E*-type voltage source whose terminal voltage is controlled according to the formula "-*x*Δ*R*". The normalized width *x* of the doped layer is modeled by the voltage *V*(*x*) of the capacitor C_x, which serves as an integrator of the quantities on the right side of state equation (2.11). The initial state of the normalized width of the doped layer x_0, which is modeled as initial voltage of the capacitor, is determined by the initial resistance R_{INIT} of the memristor according to the formula, derived from (2.13):

$$x_0 = \frac{R_{OFF}-R_{INIT}}{\Delta R} \quad (2.14)$$

The model is implemented as a SPICE subcircuit with parameters which can pass the following values into the subcircuit as arguments: the initial *RINIT* resistance, the *ROFF* and *RON* resistances, the width of the thin film *D*, the dopant mobility μ_v, and the exponent *p* of the window function. The list of the SPICE subcircuit mentioned below includes conventional model of the window function according to Joglekar [17], which is open to any modifications of the functions describing the nonlinear drift, including the import of experimentally acquired data. The SPICE model is also complemented with direct computation of the integral quantities which define the memristor, i.e. the time integrals of electrical voltage (flux) and of electric current (charge). These quantities belong to the results of the SPICE analysis, being available as voltages of the internal controlled sources E_{flux} and E_{charge}.

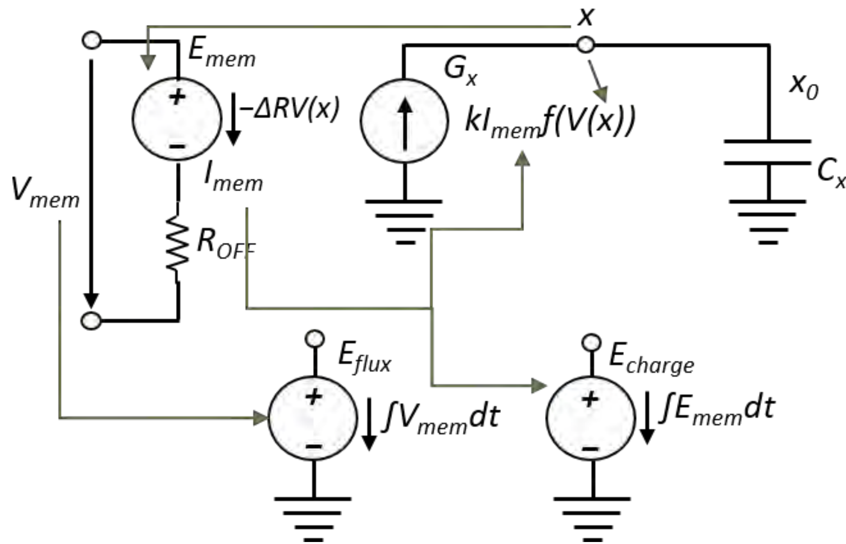


Figure 2.5: Structure of the SPICE model

According to the structure shown in Figure 2.5, a SPICE code was developed [16] as follows:

```
* HP Memristor SPICE Model
* For Transient Analysis only
* created by Zdenek and Dalibor Biolek
*************************
* Ron, Roff  - Resistance in ON / OFF States
* Rinit      - Resistance at T=0
* D          - Width of the thin film
* uv         - Migration coefficient
* p          - Parameter of the WINDOW-function
*              for modeling nonlinear boundary conditions
* x          - W/D Ratio, W is the actual width
*              of the doped area (from 0 to D)
*
.SUBCKT memristor Plus Minus PARAMS:
+ Ron=1K Roff=100K Rinit=80K D=10N uv=10F p=1
**********************************************
* DIFFERENTIAL EQUATION MODELING  *
**********************************************
Gx 0 x value={ I(Emem)*uv*Ron/D^2*f(V(x),p)}
Cx x 0 1 IC={(Roff-Rinit)/(Roff-Ron)}
Raux x 0 1T
* RESISTIVE PORT OF THE MEMRISTOR *
*******************************
Emem plus aux value={-I(Emem)*V(x)*(Roff-Ron)}
Roff aux minus {Roff}
**********************************************
*Flux computation*
**********************************************
Eflux flux 0 value={SDT(V(plus,minus))}
**********************************************
*Charge computation*
**********************************************
Echarge charge 0 value={SDT(I(Emem))}
**********************************************
* WINDOW FUNCTIONS
* FOR NONLINEAR DRIFT MODELING *
**********************************************
*window function, according to Joglekar
.func f(x,p)={1-(2*x-1)^(2*p)}
*proposed window function
;.func f(x,i,p)={1-(x-stp(-i))^(2*p)}
.ENDS memristor
```

Some simulation results are:

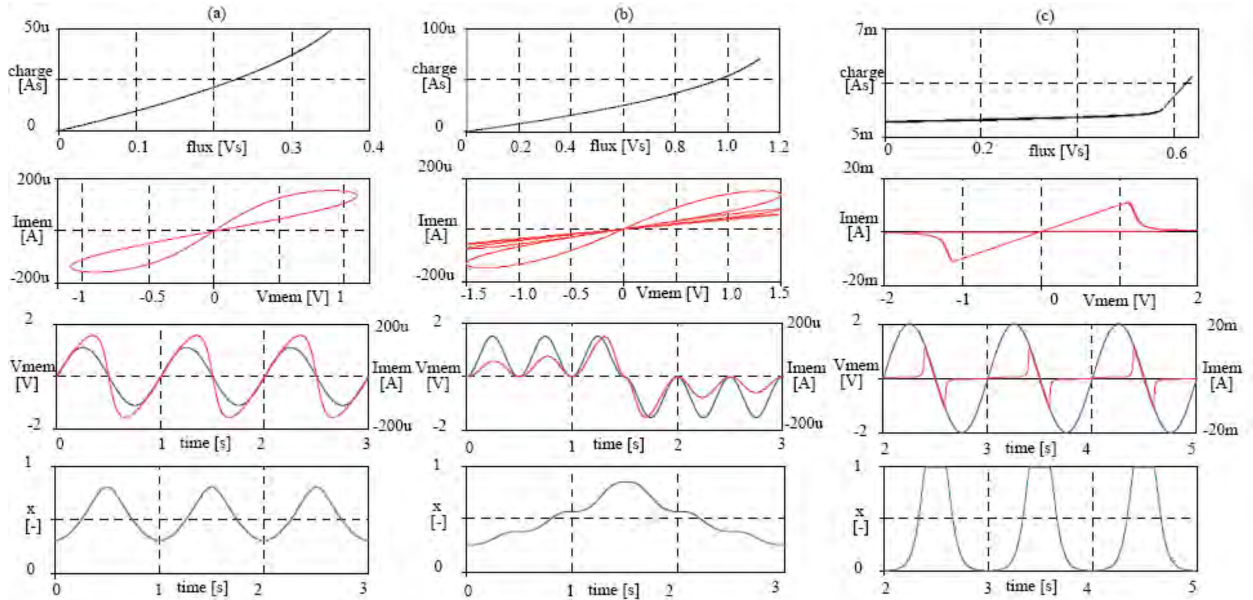


Figure 2.6: Memristor with the parameters R_{ON}=100 Ω, p=10, driven by a voltage: (a) harmonic with an amplitude of 1.2 V and a frequency of 1 Hz, (b) $\pm V_0 (\sin \omega_0 t)^2$ with V_0= 1.5 V and f_0=1 Hz, (c) harmonic with an amplitude of 2 V and a frequency of 1 Hz. Other parameters are: (a) R_{OFF}=16 kΩ, R_{INIT}=11 kΩ, (b) R_{OFF}=38 kΩ, R_{INIT}=28 kΩ, (c) R_{OFF}=5 kΩ, R_{INIT}=1 kΩ. Simulation in Fig. (c) confirms the hard switching effects[1]. [16]

Chapter 3

SRAM BASICS

Static Random Access Memory or SRAM is the most commonly used cache memory. SRAM is generally used in personal computers, workstations, routers and peripheral equipment: CPU register files, internal CPU caches and external burst mode SRAM caches, hard disk buffers, router buffers, etc. LCD screens and printers also normally employ static RAM to hold the image displayed.

3.1 SRAM

SRAM is a form of semiconductor memory widely used in electronics, microprocessor and general computing applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion, and does not need to be dynamically updated as in the case of DRAM (dynamic RAM) memory. While the data in the SRAM memory does not need to be refreshed dynamically, it is still volatile, meaning that when the power is removed from the memory device, the data is not held, and will disappear. SRAM is faster and more reliable than the DRAM. DRAM access times are few times higher than SRAM access times due to recharging necessity. In addition, its cycle time is much shorter than that of DRAM because it does not need to pause between accesses. Unfortunately, it is also much more expensive to produce than DRAM. Due to its high cost, SRAM is often used only as a memory cache.

SRAMs are used for specific applications within the PC, where their strengths outweigh their weaknesses compared to DRAM:

- Simplicity: SRAMs do not require external refresh circuitry or other work in order to keep stored data intact.
- Speed: SRAM is faster than DRAM.

In contrast, SRAMs have the following weaknesses, compared to DRAMs:

- Cost: SRAM is, byte for byte, several times more expensive than DRAM.
- Size: SRAMs take up much more space than DRAMs (which is part of why the cost is higher).

These advantages and disadvantages taken together obviously show that performance-wise, SRAM is superior to DRAM, and we would use it exclusively if only we could do so economically. Unfortunately, 32 MB of SRAM would be prohibitively large and costly, which is why DRAM is used for system memory. SRAMs are perfectly suitable for level 1 and level 2 cache memory as cache memory needs to be very fast, and not very large.

SRAM is manufactured in a way rather similar to how processors are: highly-integrated transistor patterns photo-etched into silicon. Each SRAM bit is comprised of between four and six transistors, which is why SRAM takes up much more space compared to DRAM, which uses only one (plus a capacitor). Because an SRAM chip is comprised of thousands or millions of identical cells, it is much easier to make than a CPU, which is a large die with a non-repetitive structure. This is one reason why RAM chips cost much less than processors do.

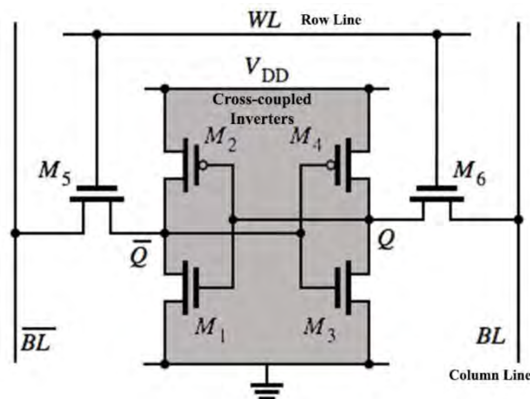


Figure 3.1: Conventional SRAM cell

The operation of the SRAM memory cell is relatively straightforward. When the cell is selected, the value to be written is stored in the cross-coupled inverters. The cells are arranged in a matrix, with each cell individually addressable. Most SRAM memories select an entire row of cells at a time, and read out the contents of all the cells in the row along the column lines. While it is not necessary to have two bit lines, using the signal and its inverse, this is normal practice which improves the noise margins and improves the data integrity. The

two bit lines are passed to two input ports on a comparator to enable the advantages of the differential data mode to be accessed, and the small voltage swings that are present can be more accurately detected. Access to the SRAM memory cell is enabled by the Word Line. This controls the two access control transistors which control whether the cell should be connected to the bit lines. These two lines are used to transfer data for both read and write operations.

3.2 Conventional SRAM Types:

There are different variations of SRAM. Most common are discussed here:

3.2.1 4T-SRAM:

4T-SRAM cell consists of four NMOS transistors plus two poly-load resistors. Two NMOS transistors are pass-transistors. These transistors have their gates tied to the word line and connect the cell to the columns. The two other NMOS transistors are the pull-downs of the flip-flop inverters. The loads of the inverters consist of a very high polysilicon resistor. This design is the most popular because of its size compared to a 6T cell. The cell needs room only for the four NMOS transistors. The poly loads are stacked above these transistors. Although the 4T SRAM cell may be smaller than the 6T cell, it is still about four times as large as the cell of a comparable generation DRAM cell. The complexity of the 4T cell is to make a resistor load high enough (in the range of giga-ohms) to minimize the current. However, this resistor must not be too high to guarantee good functionality. Despite its size advantage, the 4T cells have several limitations. These include the fact that each cell has current flowing in one resistor (i.e., the SRAM has a high standby current), the cell is sensitive to noise and soft error because the resistance is so high, and the cell is not as fast as the 6T cell.

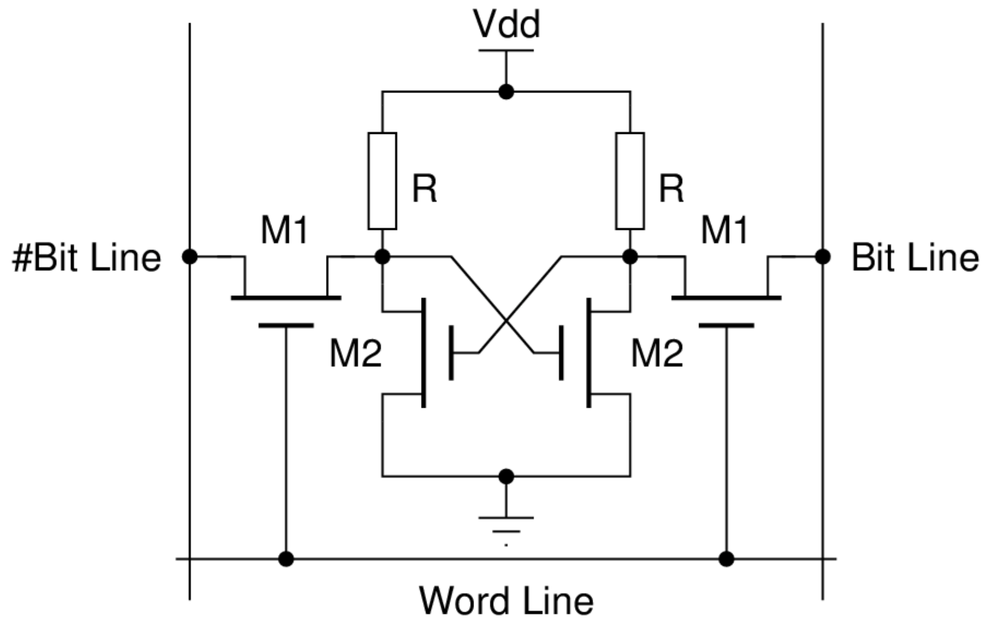


Figure 3.2: 4T SRAM

3.2.2 6T-SRAM

6T -SRAM is the most commonly used type of SRAM. This type SRAM cells are composed of six transistors, one NMOS transistor and one PMOS transistor for each inverter, plus two NMOS transistors connected to the row line. This configuration is called a 6T Cell. This cell offers better electrical performances (speed, noise immunity, standby current) than a 4T structure. The main disadvantage of this cell is its large size.

The four transistors in the center form two cross-coupled inverters. In actual devices, these transistors are made as small as possible to save chip-area, and are very weak. Due to the feedback structure, a low input value on the first inverter will generate a high value on the second inverter, which amplifies (and stores) the low value on the second inverter. Similarly, a high input value on the first inverter will generate a low input value on the second inverter, which feeds back the low input value onto the first inverter. Therefore, the two inverters will store their current logical value, whatever value that is.

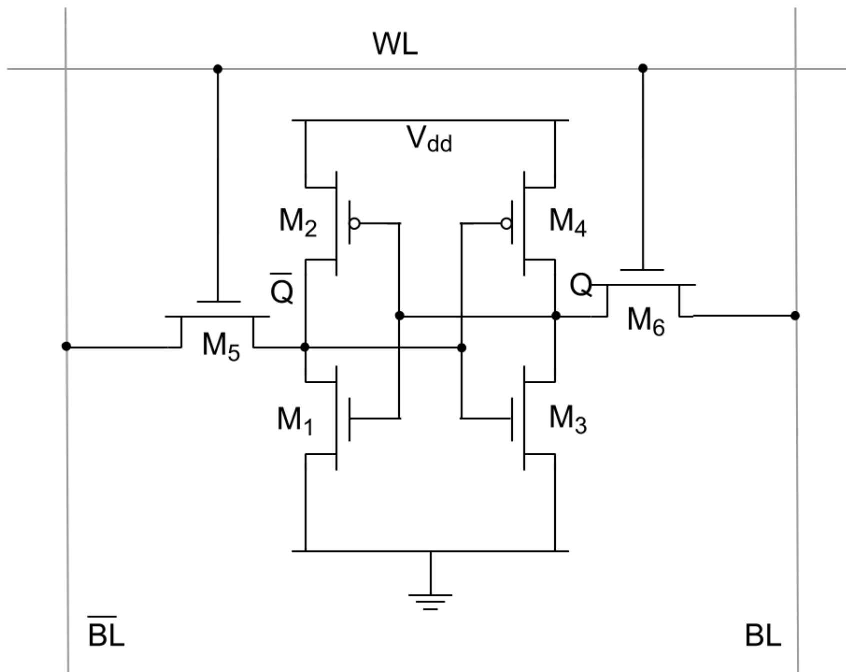


Figure 3.3: 6T SRAM

The two lines between the inverters are connected to two separate bitlines via two n-channel pass-transistors (left and right of the cell). The gates of those transistors are driven by a wordline. In a larger SRAM, the wordline is used to address and enable all bits of one memory word. As long as the wordline is kept low, the SRAM cell is disconnected from the bitlines. The inverters keep feeding themselves, and the SRAM stores its current value.

When the wordline is high, both n-channel transistors are conducting and connect the inverter inputs and outputs to the two vertical bitlines. That is, the two inverters drive the current data value stored inside the memory cell onto the bitline (left) and the inverted data value on the inverted-bitline (right). This data can then be amplified and generates the output value of the SRAM cell during a read operation.

To write new data into the memory, the wordline is activated, and the strong bitline input-drivers (on top of the schematics) are activated. Depending on the current value stored inside the SRAM cell there might be a short-circuit condition, and the value inside the SRAM cell is literally overwritten. This only works because the transistors inside the SRAM cell are very weak.

3.2.3 4T2M-SRAM [18]

The conventional SRAM cell is modified to implement the non-volatile functionality through replacement of the two pMOS load transistors in SRAM cell by memristors as illustrated in Fig. 3.4 SRAM cell when the power is turned off to save the data on the latch of the memristor device and two pull-down transistor and consists of two pass transistor.

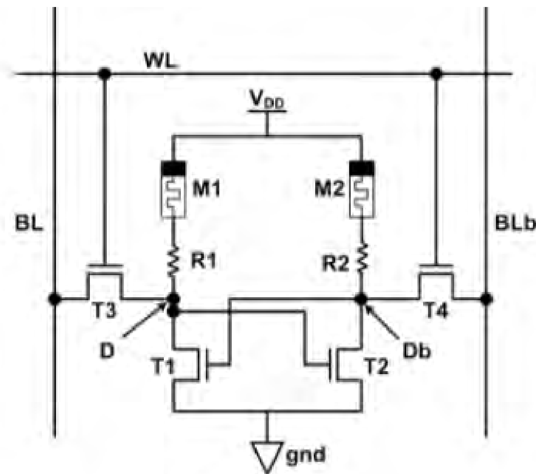


Figure 3.4: Structure of Non-volatile 4T SRAM cell with memristors

For the forward direction it has around 100K ohms: let this state correspond to the high bias condition. It is also about 50 ohms for the reverse direction: this is defined to be the low bias. Two load devices of a SRAM cell flow current in the forward direction making memristors in the high bias state. By making a cell discharge through power lines for power down events, one of the memristors will flow current in the reverse direction. The memristor will have the low bias state during the power off period. The resistivity mismatch between the two current paths is used for information storage. The mismatch will bring back the data stored just before the power down. When the power is on, the load device of the current path having the low bias state will have higher voltage than that of the other path having the high bias state. The latch mechanism of the SRAM cell instantly recovers the original data before the power down.

3.2.4 3T-2M SRAM [19]

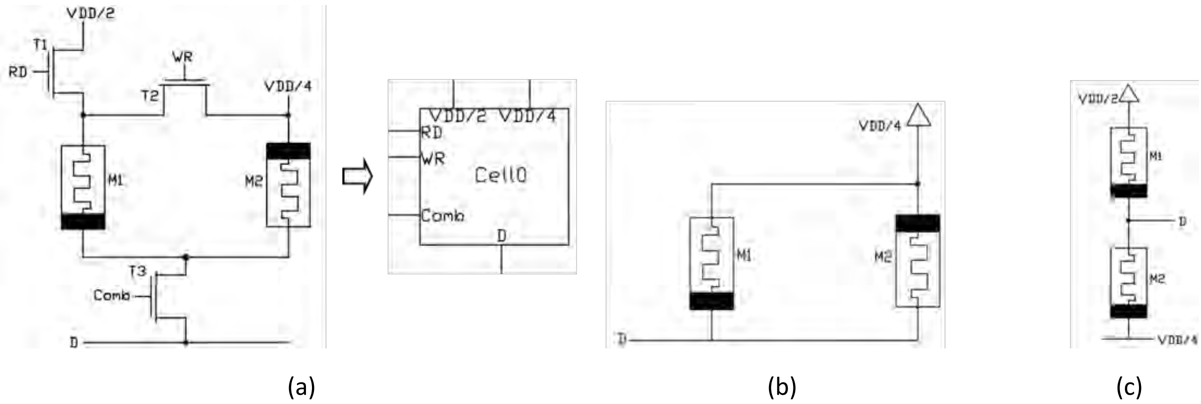


Figure 3.5: 3T-2M SRAM

A Memristor based SRAM cell is presented in ref 3.6. Electrical scheme of the 3T-2M leaf cell is shown in Fig. 3.5(a). Two memristors are used as memory element. The arrangement is in such a way that during write cycle, they are connected in parallel but in opposite polarity [Fig. 3.5 (b)] and during read cycle, they are connected in series [Fig. 3.5 (c)]. These connections are established by two NMOS pass transistors T1 and T2. A third transistor T3 is used to isolate a cell from other cells of the memory array during read and write operations. The gate input of T3 is the Comb signal which is the OR of RD and WR signals. If a bit is to be written, RD is taken to the LOW state and WR and Comb are taken to the HIGH state. As a result, circuit of Fig. 3.5 (b) is formed. The voltage across the memristors is (V_D−V_{DD}=4). Depending on the data, it can be positive (if D=1 i.e. V_D=V_{DD}) or negative (if D=0 i.e. V_D= 0 V). As polarities of the memristors are opposite, change of memristances (or resistances) will also take place in the opposite direction. Now if the data is to be read, RD and Comb are taken to the HIGH state and this forms the circuit shown in Fig. 3.4 (c). Voltage at D is now:

$$V_D = \left(\frac{V_{DD}}{2} - \frac{V_{DD}}{4}\right) \times \frac{R_2}{R_1+R_2} + \frac{V_{DD}}{4} \quad (5)$$

where, R1 and R2 are the resistances of M1 and M2 respectively. If ‘1’ was written during write cycle, R2 becomes significantly greater than R1 and then V_D is greater than V_{DD}=4. If ‘0’ was written, R1 becomes significantly greater than R2 which makes V_D to be as close as V_{DD}=4. A comparator can be used as a sense amplifier to interpret these voltages as HIGH or LOW correctly.

Chapter 4

MEMRISTOR BASED SRAM CELL

Non-volatile SRAMs, or NVSRAMs, have standard SRAM functionality, but they save the data when the power supply is lost, ensuring preservation of critical information. NVSRAMs are used in a wide range of situations—networking, aerospace, and medical, among many others — where the preservation of data is critical and where batteries are impractical. In our work memristor is used to give the non-volatile property to the memory circuit. In this chapter the development of proposed NVRAM is presented sequentially.

4.1 MEMRISTOR AS A MEMORY COMPONENT

Hysteresis in the *i-v* characteristic of memristor shown in the previous chapter (Figure 2.2, 2.3) suggests the property of keeping memory in the form of resistance. From Eq. 2.1, it can be seen that, effective resistance or memristance of a memristor depends on the diffusion length w. Again w is governed by the differential equation stated in Eq. 2.2 which led us the solution of w at any time t. It shows that the time dependent value of the diffusion length w depends on the time dependent charge q or in other word, current. So it can be concluded that the effective resistance is a function of current flowing through the memristor. Current flowing from positive to negative terminal of the memristor increases the diffusion length w and thereby decreases the effective resistance of the memristor (Eq. 2.1). Current flowing from the opposite direction causes increment of resistance. A quick simulation could demonstrate the scenario clearly. Figure 4.1 shows a memristor under application of pulses across it.

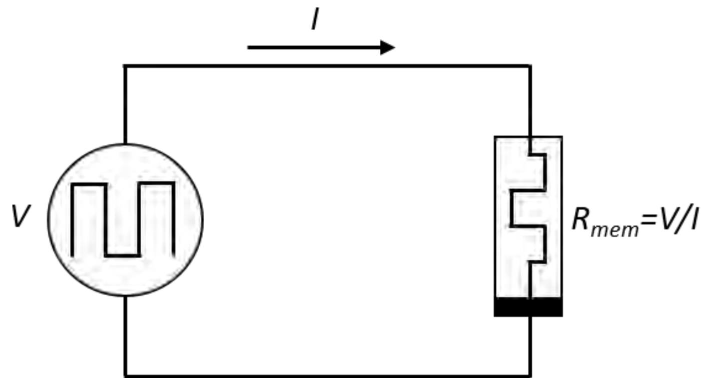


Figure 4.1: A pulsed source applied across a memristor

Simulation was done in PSPICE v9.2 with memristor parameters R_{OFF} = 10KΩ, R_{ON} = 100Ω, D=10nm, $\mu_D=10^{-9}$ $m^2/s/V$. Figure 4.2 shows the plot of the voltage and resistance of the memristor. Resistance is found by plotting V/I against time. The plot shows the decrement of resistance when applied a positive pulse and increment of resistance when applied a negative pulse.

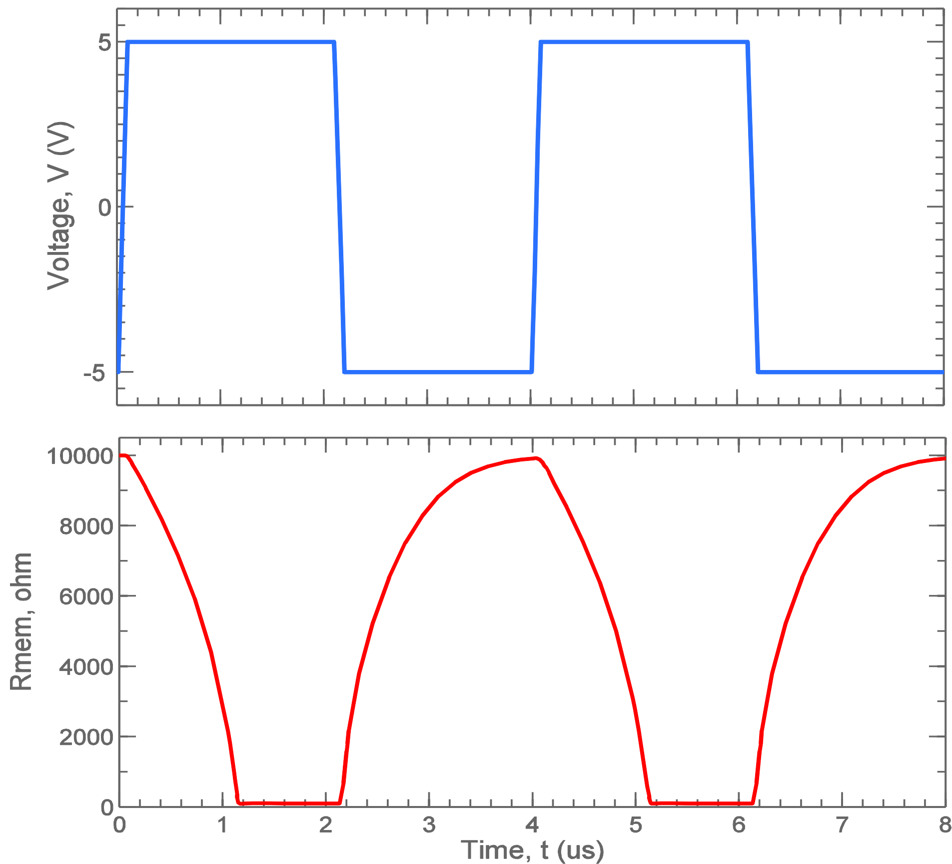


Figure 4.2: V vs Time and Rmem vs Time plot

This result clearly indicates that a memristor can hold memory in the form of resistance and a single memristor could be enough to hold 1-bit memory provided that both positive and negative pulses are available. However, generation of negative voltage can be a tough job in integrated circuits sometimes. To eliminate the need of negative source, we developed a good technique of using two different positive voltages connected with the memristor in opposite directions. Higher one is V_{DD} and the lower one is V_{DD}/x, where x>1. Also from recent developments we know that memristors can be as small as 3nm [20] and μ_D can be increased by 10~10^3 times. For example, simulation was done with memristor parameters R_{OFF} = 5KΩ, R_{ON} = 100Ω, D=3nm, $\mu_D=100\times10^{-9}$ m²/s/V and x=2. Figure 4.3 shows the plot of the voltage and resistance of the memristor.

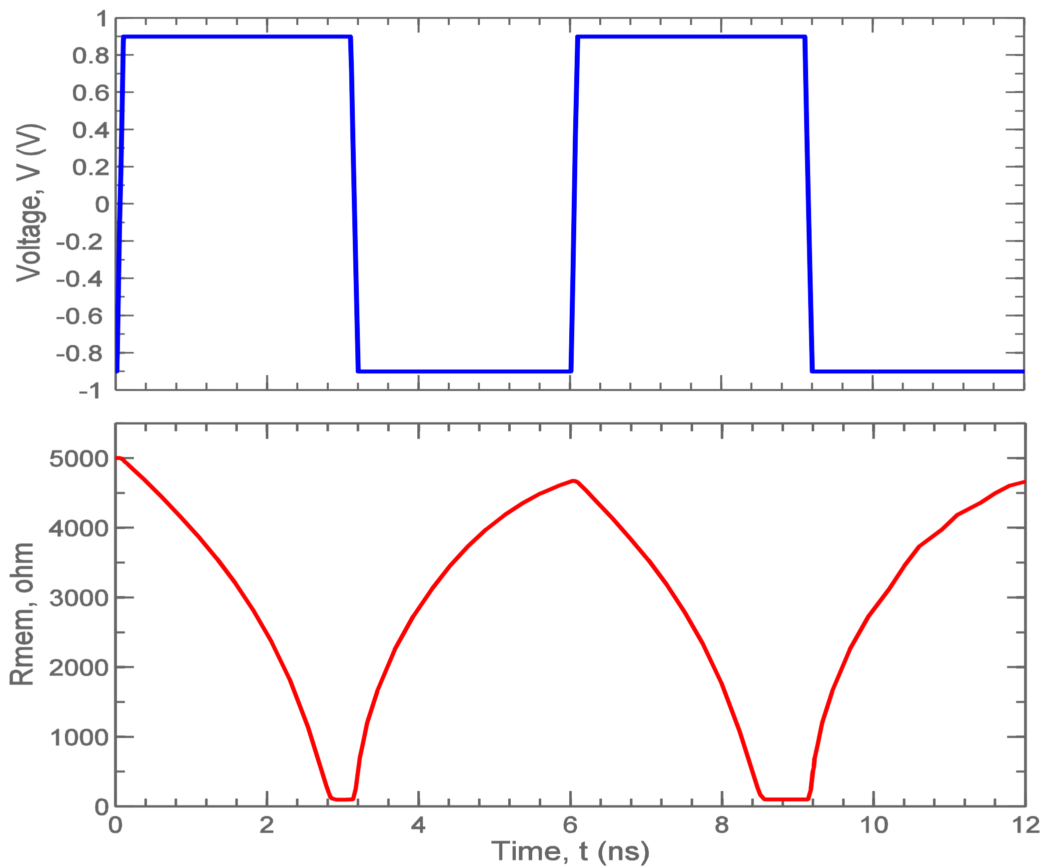


Figure 4.3: V vs Time and Rmem vs Time plot with new memristor parameters

This result also shows that the speed of change of resistance of a memristor is not same for current flow in either directions for same potential difference. To make the speed equal we had to use different potential differences for the two cases.

4.2.1 Two-Transistor Two-Memristor Memory Cell

As shown, one memristor can independently act as a memory element. It is sufficient for holding 1 bit memory. But to read it back, the resistance of the memristor have to be measured. To measure resistance, we have to apply a voltage across it and measure the current through it, which is very much inconvenient. A better approach is to use the voltage divider rule for which another resistive element is necessary. For this purpose another memristor can be used in reverse bias, whose memristance will never change and will act as fixed resistance. To control write and read operations our cell also needs two NMOSes. Transistors do the switching tasks to make different circuit combinations in reading and writing operation. Figure 4.4 shows our basic SRAM cell consisting of 2-NMOS and 2-memristor.

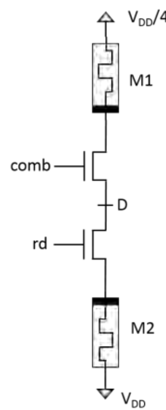


Figure 4.4: The 2-Memristor 2-Transistor SRAM cell

The arrangement is in such a way that during write cycle current will flow through only one memristor (Fig.4.5a) and during read cycle the memristors are connected in series (Fig.4.5b).These connections are established by two NMOS pass transistors T1 and T2.

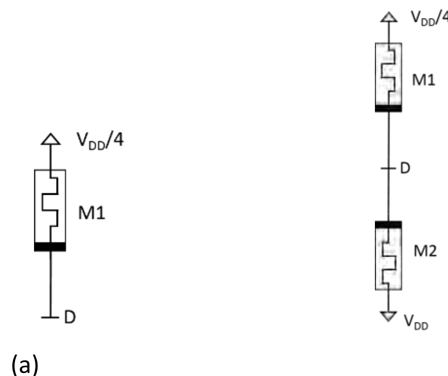


Figure 4.5: (a) circuit when rd=0, comb=1 (b) circuit when rd=1, comb=1

The COMB signal is logical ORed signal of WR(write) and RD(read) signal. If a bit is to be written, RD is taken to the LO state and COMB is taken to the HI state. As a result, circuit of Figure 4.5a is formed. The voltage across the memristors is (V_D-V_{DD}/4). Depending on the data, it can be positive (if D=1 i.e. V_D=V_{DD}) or negative (if D=0 i.e. VD=0V). According to 'write data' the polarity of the potential difference across M1 can be positive or negative, change of memristances (or resistances) will also take place in both way respectively. If D=1 i.e. V_D= V_{DD}, current will flow from V_D to V_{DD}/4 causing resistance of M1 to increase and vice versa. Period of the write cycle should be sufficient to make maximum resistance change in one direction. After completing the write cycle, COMB is taken to the LO state and the data will be stored encoded in the resistances of M1. Now if the data is to be read, RD and COMB both are taken to the HI state and this forms the circuit shown in Fig.4.5(b). Voltage at D is now:

$$V_D = \left(V_{DD} - \frac{V_{DD}}{4}\right) \times \frac{R1}{R1+R2} \qquad (4.1)$$

Where, R1 and R2 are the resistances of M1 and M2 respectively. If '0' was written, R2 was significantly greater than R1 and V_D was close to V_{DD}/4. If '1' was written during write cycle, R1 is significantly greater than R2 and V_D is greater than V_{DD}/4. But as V_D exceeds a certain value the source voltage of nMOS controlled by the READ signal becomes significantly high and moves the nMOS out of saturation. For this reason we don't get very high voltage at D node when we read '1'. To simulate the circuit, a CMOS transmission gate is used to make the READ and WRITE mutually exclusive on the data line D (figure 4.6).

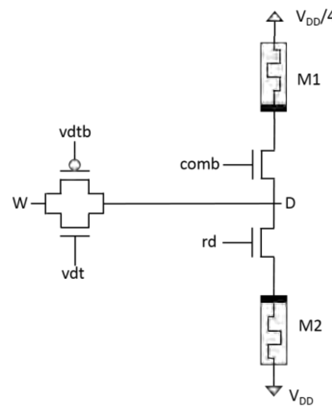


Figure 4.6: A CMOS pass gate is introduced for simulation

A pulse of 2 ns is applied to COMB for writing and a pulse of 0.8 ns is applied to RD and COMB for reading purpose. In the first read/write cycle, COMB=1 and RD=0 for 2ns. During this time, write data WD=1. After writing, COMB is made LO. Again COMB and RD are made high. Then the measured voltage at D is 0.619V (Figure 4.7). The read time here is 0.8ns. In the next cycle, a '0' is written making WD=0 during write cycle. After this, the measured voltage at D is 0.5727V (Figure 4.7). A comparator can be used as a sense amplifier to interpret these voltages as HI or LO correctly. Use of comparator is described later in section 4.5.2. The reference of the comparator should be tied to 0.59V. Simulations of the circuits are based on the following parameters: R_{ON} =100Ω, R_{OFF} =5kΩ, p =10, D =3nm and μ_v =100×10^{-9} m^2/s/V. SRAM cell has been implemented using CMOS 0.18µm technology. Using the above memristor parameters satisfactory operation of the SRAM cell was achieved at 1.8 Volts. We have referred to this voltage as the nominal voltage for the SRAM cell. Furthermore, the initial state of the memristors is determined by initial resistance, R_{INIT}.

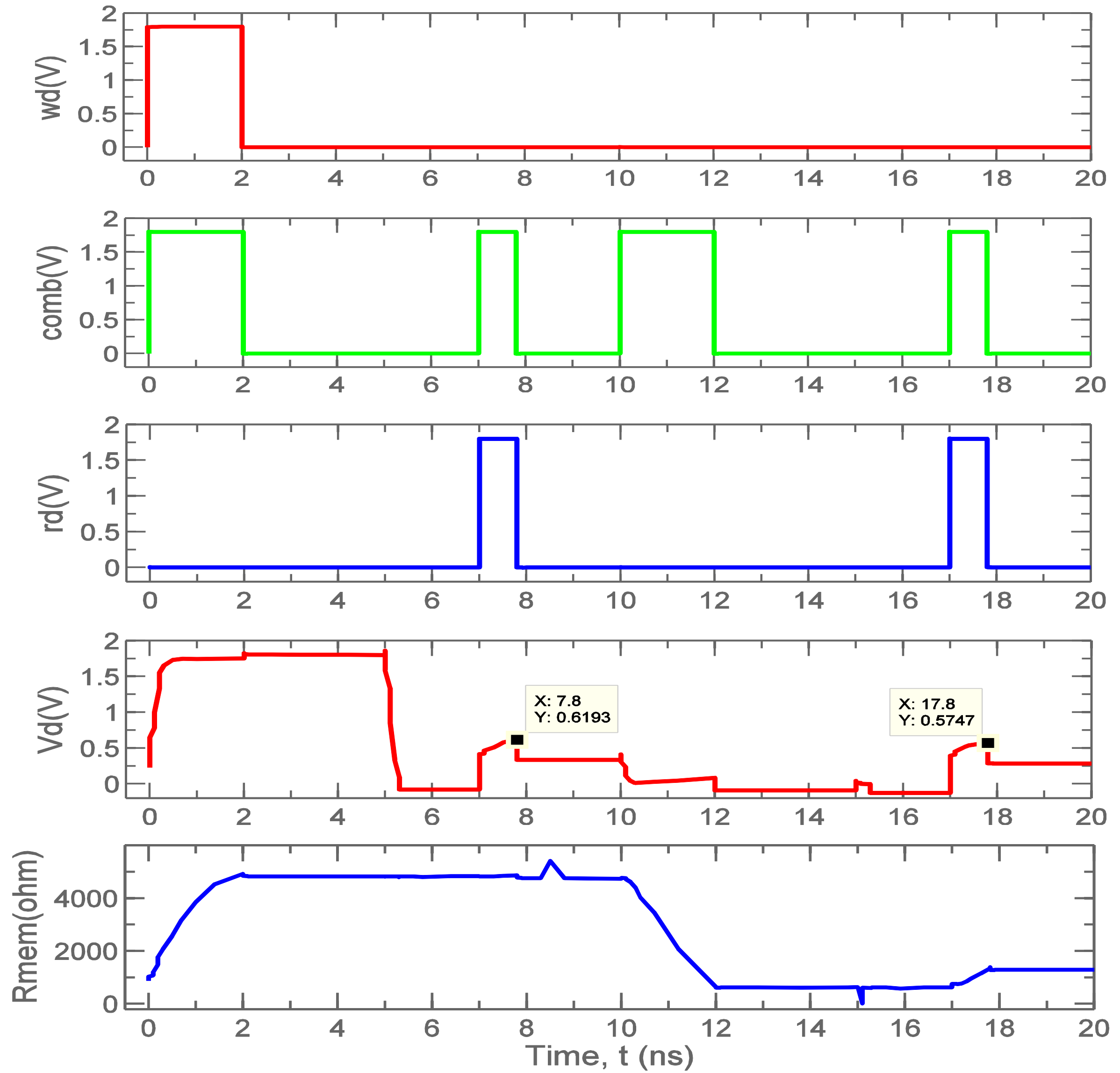


Figure 4.7: After writing '1' (WD=1, COMB=1,RD=0), V_D was read as 0.619V (COMB =1,RD=1) and After writing '0' (WD=0, COMB =1,RD=0), V_D was read as 0.5727V (COMB =1,RD=1)

4.2.2 SIMULATION OF 2×2 ARRAY OF MEMORY

In the previous section, we successfully demonstrated read and write operation of a single SRAM cell. For the implementation of SRAM array, it is equally important to build a memory architecture. For our cell, we have introduced a slightly different technique of organizing the memory in an array than it is conventionally done. Organization of 2x2 array is shown in figure 4.8(b). First, a little modification was needed for the single cell. It is shown in figure 4.8(a).

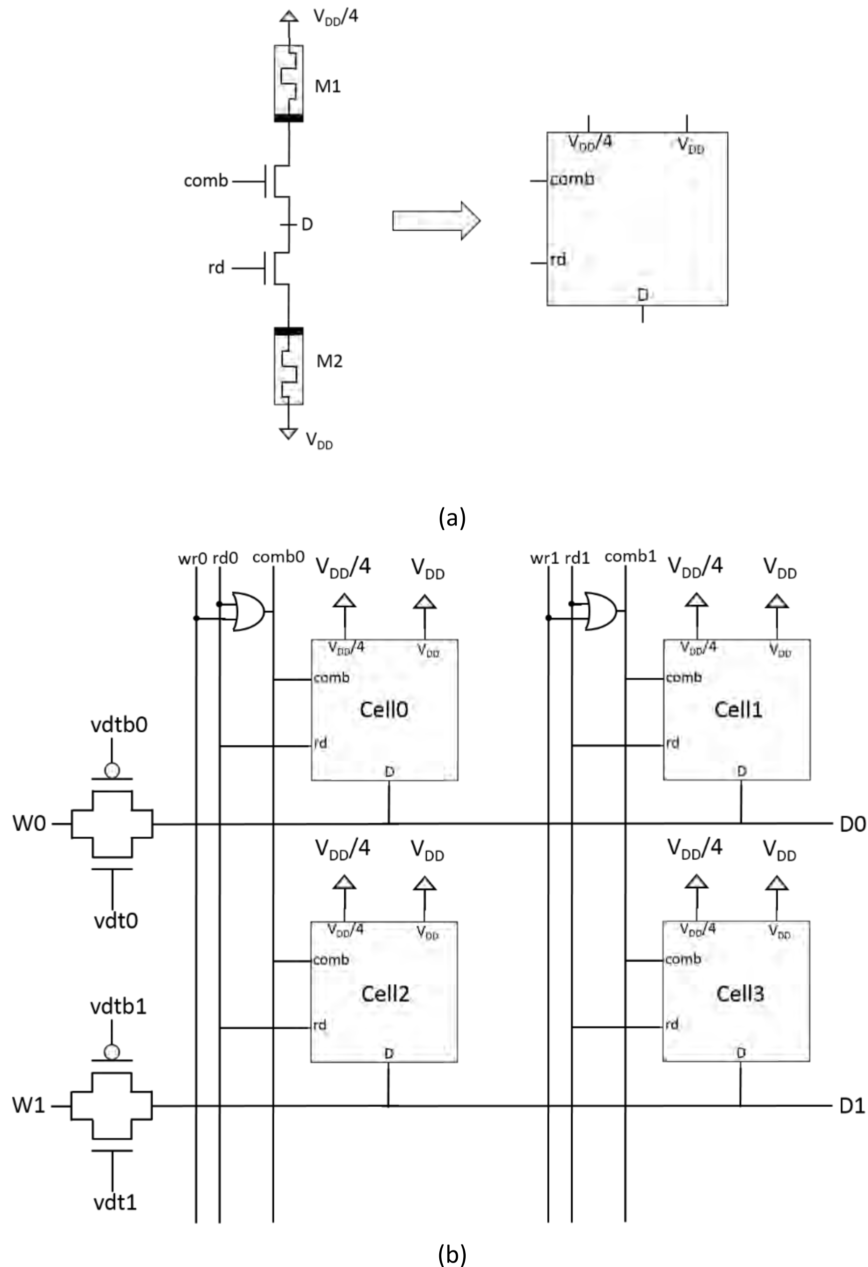


Figure 4.8 (a) basic building block of a single cell (b) 2x2 array of memory

Columns are selected by traditional read write encoder technique. $V_{DD}/4$ and V_{DD} pins are common in a column. Suppose we want to select row-1 column-0 cell. For this, RD0, COMB0 and Vdt1, Vdtb1 should be used. Data is read or written through D1 line. Simulation of this structure was done in PSPICE v9.2 with tsmc018 mos model. The nominal voltage is 1.8V and memristor parameters are R_{OFF} = 5KΩ, R_{ON} = 100Ω, D=3nm, $\mu_D=100\times10^{-9}$ $m^2/s/V$.

Four read-write cycles are shown in the plot. In the first cycle, '1' was written to cell0. Then it was read and found to be 0.6188 V and can be interpreted as HI with the aid of a sense amplifier. Then a '0' was written to the cell1 and read as 0.503 V (close to VDD/4). Again '0' was written on cell3 and cell0 was read as 0.6172 V. Finally '1' was written to the cell3 and found 0.6157V after reading. The write-read cycles are shown in figure 4.9.

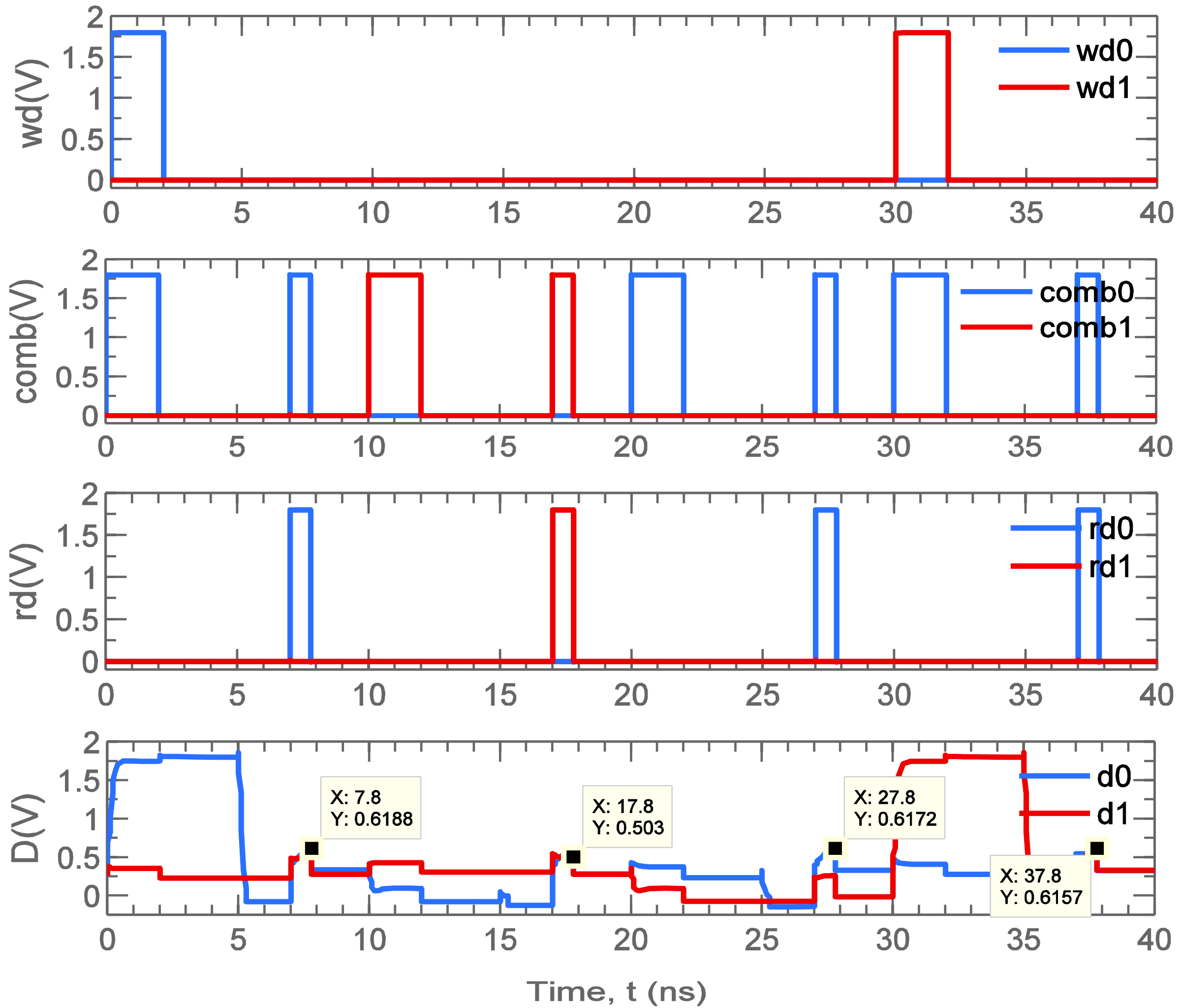


Figure 4.9: Plot of the read-write cycles in 2x2 array

4.3.1 Residual Voltage Effect

After writing '1' to a cell we have to disconnect the wordline. Some residual voltage remains in the wordline with no path to discharge. If we try to read '0' on a different cell which is on the same row, we would not be able to do it due the residual voltage. Figure 4.10 depicts the problem.

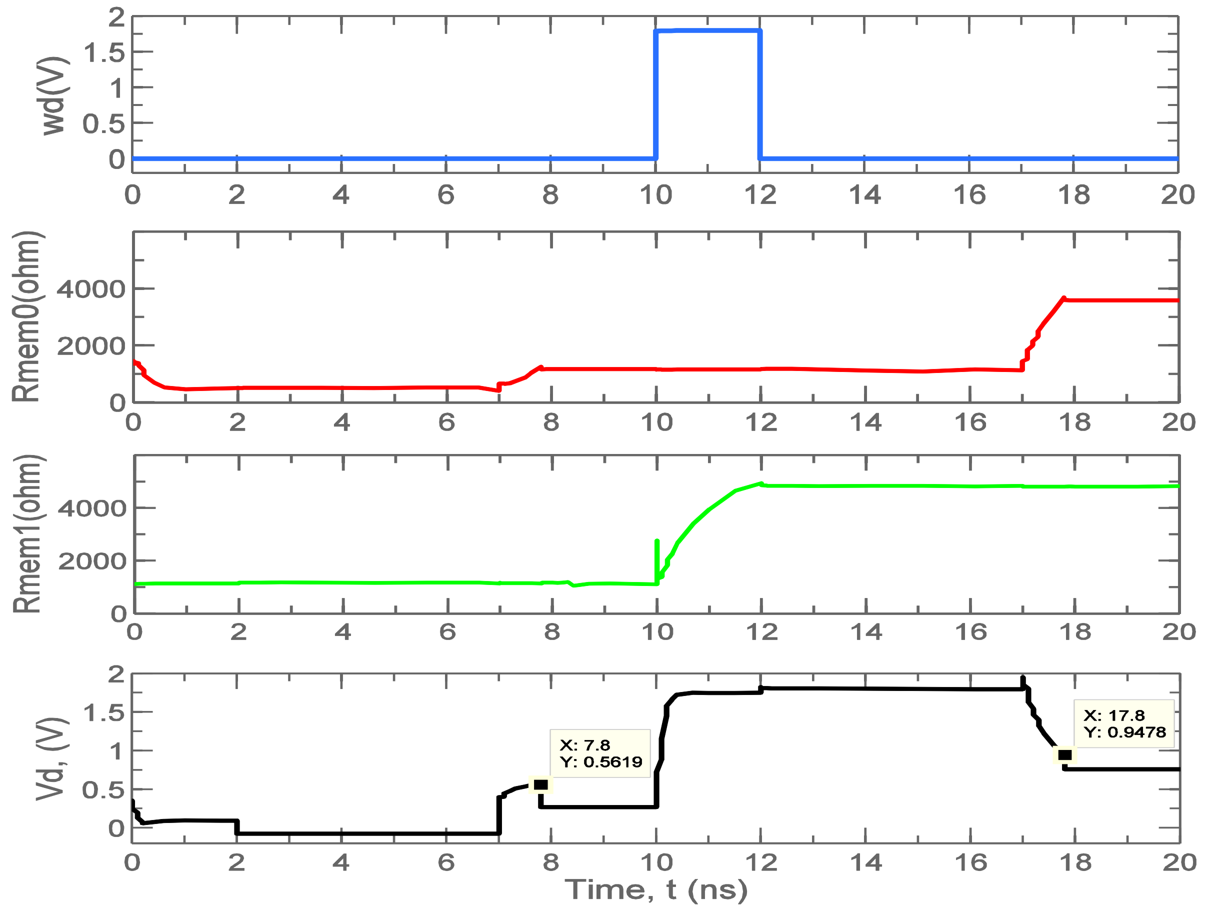


Figure 4.10: '0' written on cell0 and read. Then '1' was written on cell1 and cell0 was read. This time cell0 gives 0.9478 V much larger than '0' should give due to addition of the residual voltage.

This problem was not evident in single cell. But in array structure it shows severe discrepancy in reading cells. To solve this problem a new charge dumping technique (through resistor) was introduced.

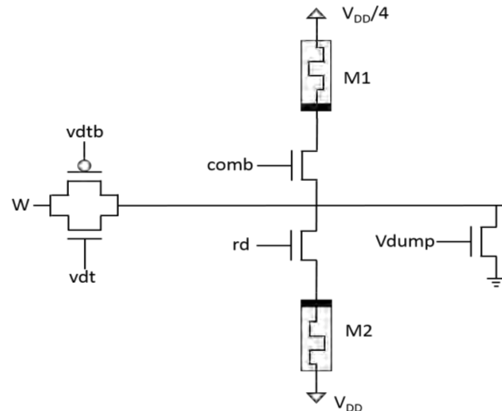


Figure 4.11: A NMOS controlled by Vdump signal is used to create a path to the ground for discharging the wordlines.

As shown in figure 4.11 a NMOS controlled by Vdump signal is introduced in the wordlines. Before every read operation Vdump signal turns the NMOS ON and a path to ground is created for 0.3 ns for the residual voltage to discharge completely. The effect is shown in figure 4.12

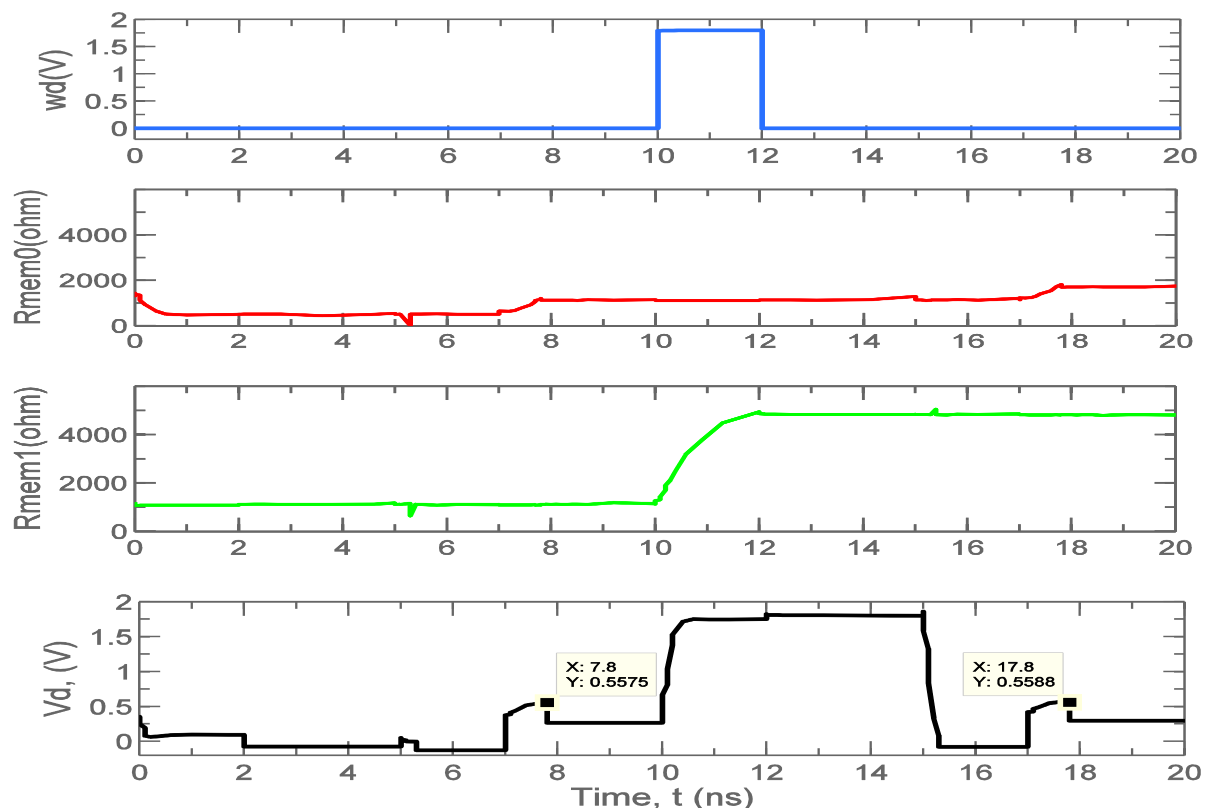


Figure 4.12: '0' written on cell0 and after using Vdump for 0.3ns cell0 is read. Then '1' was written on cell1 and after using Vdump for 0.3ns cell0 was read. This time cell0 gives 0.5588 V which is equivalent to '0'.

This solves the residual voltage problem but introduces 0.3 ns read time increase.

4.3.2 Contamination of Stored Data Due to Leakage

The above mentioned structure works well ideally. Unfortunately if we take practical conditions in consideration, data stored in that cell starts to distort because of a subtle leakage path. Current can flow through a series path (Fig 4.13a) while a cell is not active due to MOS leakage. Also current flows through other cells in time of reading or writing to a cell. This current changes the memristance of the memristors of other cells and changes the stored data. Change is negligible in a single cycle but can be severe if read/write takes place on the same cell for many consecutive cycles. Figure 4.13 shows the possible leakage paths created to the cell which is not under operation.

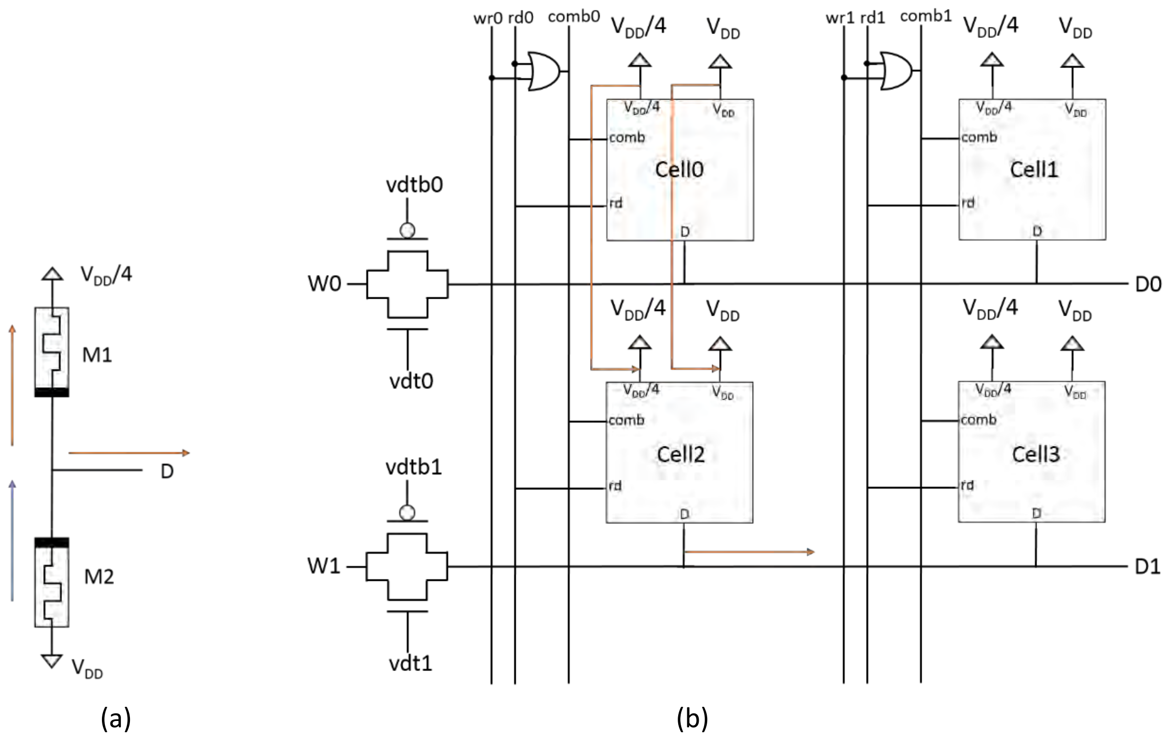


Figure 4.13 (a) Series leakage path due to MOS leakage in a single cell. (b) Intra cell leakage path.

Basically two types of contamination due to leakage can happen.

(a) Series leakage path due to MOS leakage in a single cell

(b) Intra cell leakage path.

4.3.3 Change of Stored Data Due to Consecutive Read Operations

To read back a cell data, the resistance of the memristor have to be measured. To measure resistance, we have to apply a voltage across it and measure the current through it, which is very much inconvenient. A better approach is to use the voltage divider rule. But in both cases Potential difference has to be applied across the memristor, which causes current flow through memristor and consequently change of memristance. This change depends on direction of current flow and duration of the operation. So every time we read a cell data, it causes a slight change in the memristance. In our proposed scheme it happens only if we try to read '0'. For the case of reading '1', memristance is at highest value for the direction of read current, hence no change occurs. Proposed circuit can tolerate 4-5 consecutive read operations on a single cell.

Till now no other suitable way of measuring memristance is discovered. The solution to this problem is making the read cycle minimum, so that almost zero current flows through the Memristors during read operation. But the read time is mostly dependent on sense amplifier's sensitivity and responsiveness. For this ultra-sensitive sense amplifier with really fast response have to be designed.

4.4 Proposed 2-T 2-M SRAM

4.4.1 Leaf Cell Connected with Peripheral Circuit with Complete Source Isolation:

The leaf cell of our proposed SRAM contains two transistors and two memristors. Two transistors and 2 memristors are arranged following the basic 2T2M structure described in section 4.2.1 and two more transistors are added in every row to tackle the series leakage in single cell and intra cell leakage problem in the array structure.

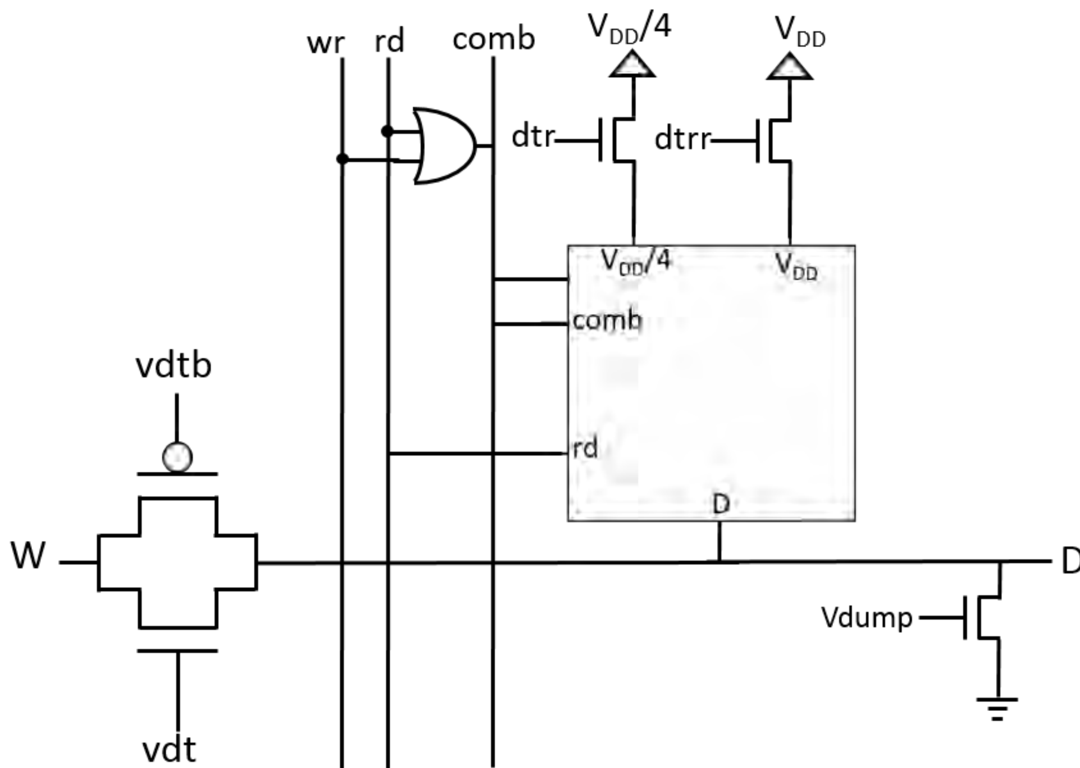


Figure 4.14: leaf cell connected with peripheral circuit containing complete source isolation option

Complete source isolation is achieved through two NMOSes controlled by signals Vdtr and Vdtrr. As a cell is completely isolated from sources V_{DD} and $V_{DD}/4$ and thus leakage path is blocked when a cell is inactive.

4.4.2 ARRAY STRUCTURE:

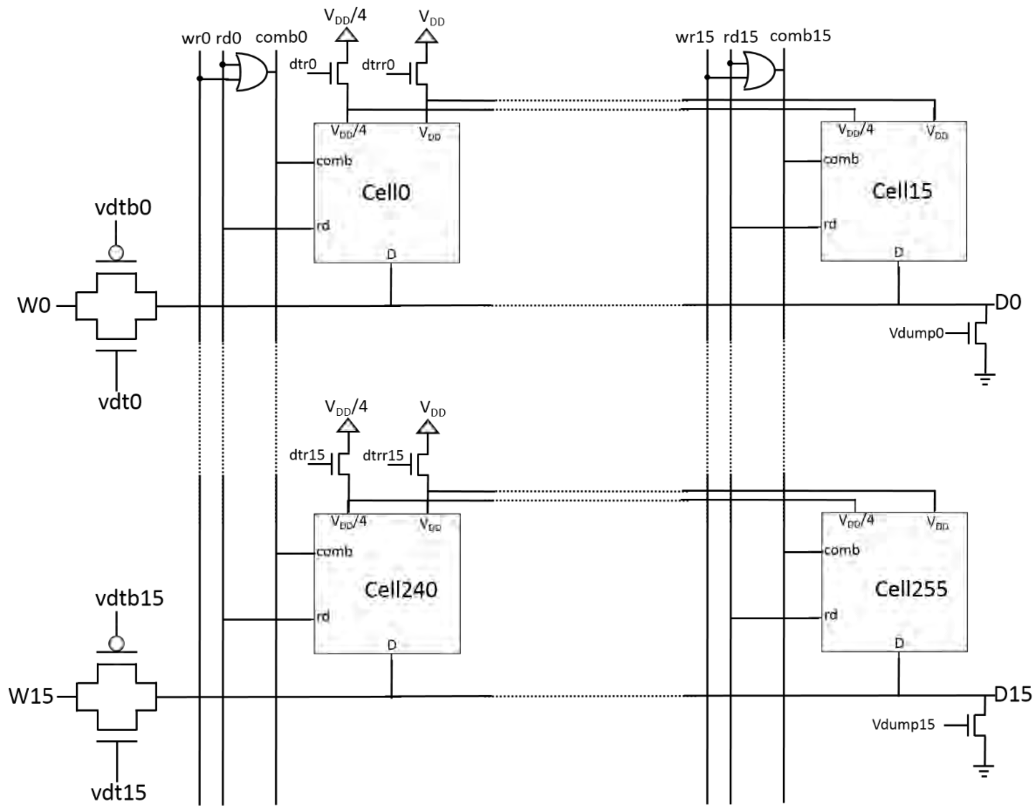


Figure 4.15: 16×16 Array Structure of the proposed memristor based SRAM

Column Selection: Rdx, Wrx signals ORed to get column selection signal Vcomb. One OR gate is required for each column.

Row Selection: Row selection is necessary to isolate the VDD and VDD/4 source from different rows. Each row requires two transistors and two control signals Vdtry, Vdtrry for this purpose.

Data Input/Output: Data is fed through wordlines/bitlines. Switching between i/p and o/p is done with the help of CMOS transmission gate controlled by Vdty & Vdtby signals which are complement of each other. In practical circuit this purpose is served through encoders.

4.5 Simulation and Analysis

Several simulations were done to test the validity of our proposed SRAM structure and compare it with the traditional SRAM structures. In the simulations data was written and read to calculate several important parameters such as write time, read time, power consumption etc.

From the figure of array structure we can see there are several inputs and outputs.

Input Pulses: In the 16×16 array 120 input pulses were required for simulation.

Vrd0-Vrd15 → read signals for column 0 and 15 respectively.

Vwr0-Vwr15 → write signals for column 0 and 15 respectively.

Vdtr0-Vdtr15 → row selection signals for row 0 and 15 respectively.

Vdtrr0-Vdtrr15 → row selection signals for row 0 and 15 respectively.

Vcomb0-Vcomb15 → column selection signals for column 0 and 15 respectively.

Vwd0-Vwd15 → Input data signals for row 0 and 15 respectively.

Vdt0-Vdt15 → Input/output switching control signals for row 0 and 15 respectively.

Vdtb0-Vdtb15 → Input/output switching control signals for row 0 and 15 respectively.

Output signals: 16 output lines were used to get data from 16 rows

Vd0-Vd15 → Output data signals for row 0 and 15 respectively.

Let the row number be x and the column number be y.

Write Operation:

For write operation the input signals which should be high are

Vwrx, Vcombx, Vdtry, Vdty

And the input signals which should be low are

Vrdx, Vdtrry, Vdtby.

Data to be written should be at Vwdy.

Read Operation:

For read operation the input signals which should be high are

Vrdx, Vcombx, Vdtry, Vdtrry, Vdtby.

And the input signals which should be low are

Vwrx, Vdty.

Read data will be at Vdy.

4.5.1 Functional Verification of 16×16 Array Structure

Usually memory blocks are used to construct a large memory to circumvent capacitive load effect of large memory circuit. So we constructed a 16×16 array memory block consisting 256 bit of memory.

For functional verification of the array, the structure was tested in two steps:

i) WRITE AND READ DIFFERENT CELLS AND OBSERVE THE EFFECT ON A SINGLE CELL

ii) WRITE AND READ DIFFERENT CELLS AND CHECK THE OUTPUT VALUES

4.5.1.1 WRITE AND READ DIFFERENT CELLS AND OBSERVE THE EFFECT ON A SINGLE CELL

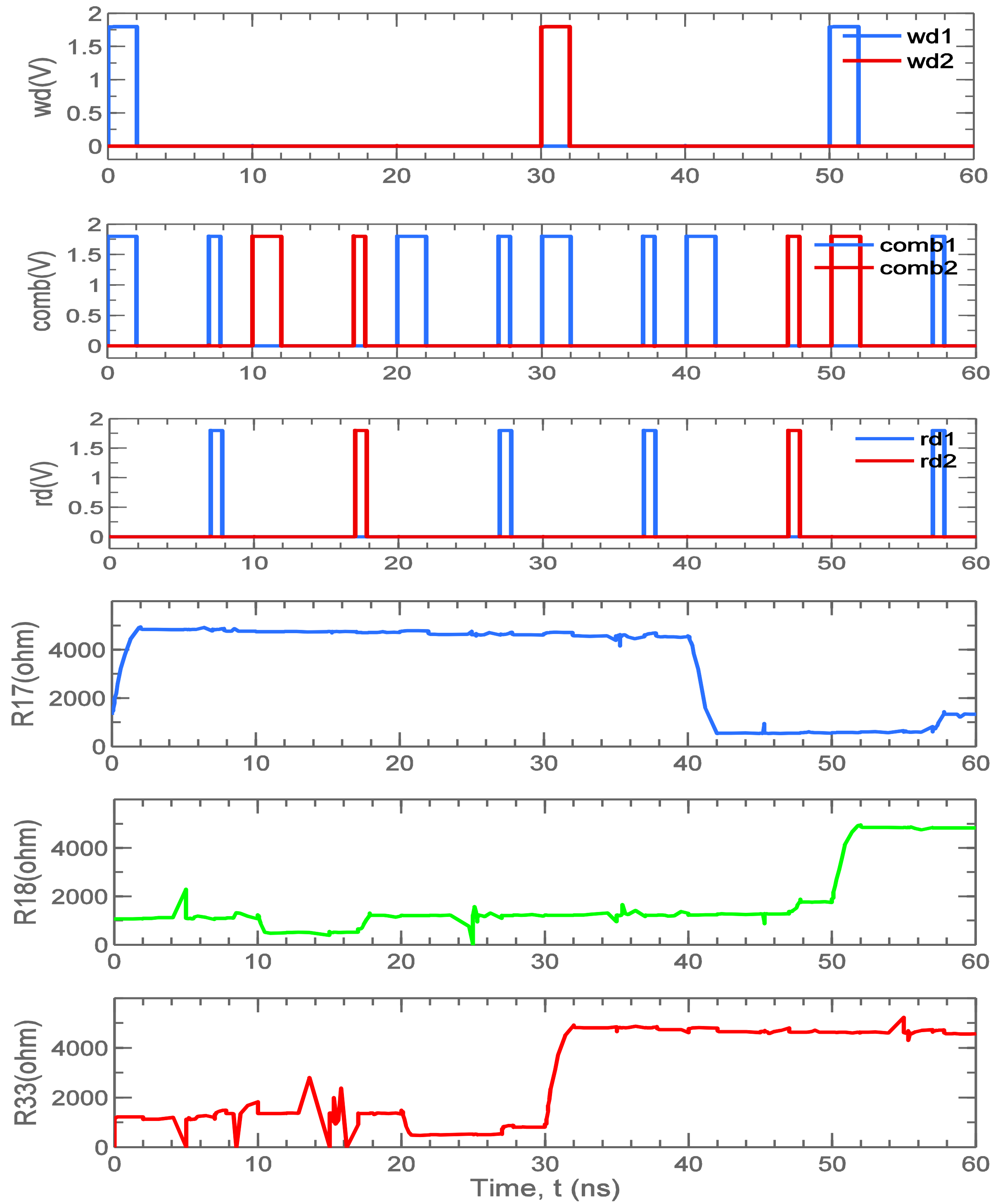
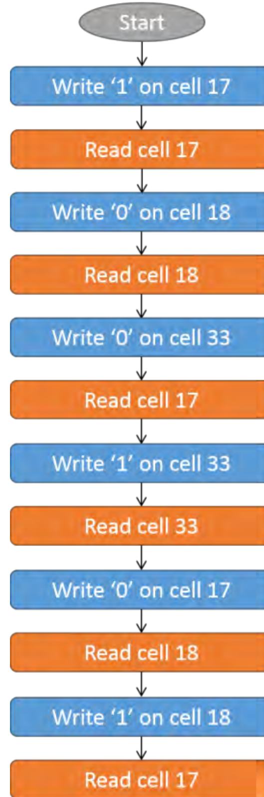


Figure 4.16: Write and read different cells and observe the effect on a single cell. Steps are described in following passage.

In the simulation the following operations were done serially:



R17, R18 and R33 are resistive values of the memristors of the particular cells: cell17, cell18 and cell33 respectively.

At first '1' was written on cell17 and value of R17 changed accordingly. After that cell17 was read. From the figure we can see the write operation ended at 2ns and during this time value of R18 and R33 was unchanged that is cell18 and cell33 were unaffected.

Again '0' was written on cell18 and value of R18 changed accordingly. After that cell18 was read. From the figure we can see the write operation ended at 12ns and during this time value of R17 and R33 was unchanged that is cell17 and cell33 was unaffected.

Next '0' was written on cell33 and value of R33 changed accordingly. From the figure we can see the write operation ended at 22ns. Cell17 was read at 27ns-27.8ns and also during this time cell33 and cell18 was unaffected.

Three more write-read cycles were carried out according to the flow diagram to test the functionality of the structure and found satisfactory results. So we came to a decision that our proposed structure is functional.

4.5.1.2 WRITE AND READ DIFFERENT CELLS AND CHECK THE OUTPUT VALUES

The same previous operations were carried out and output values were checked.

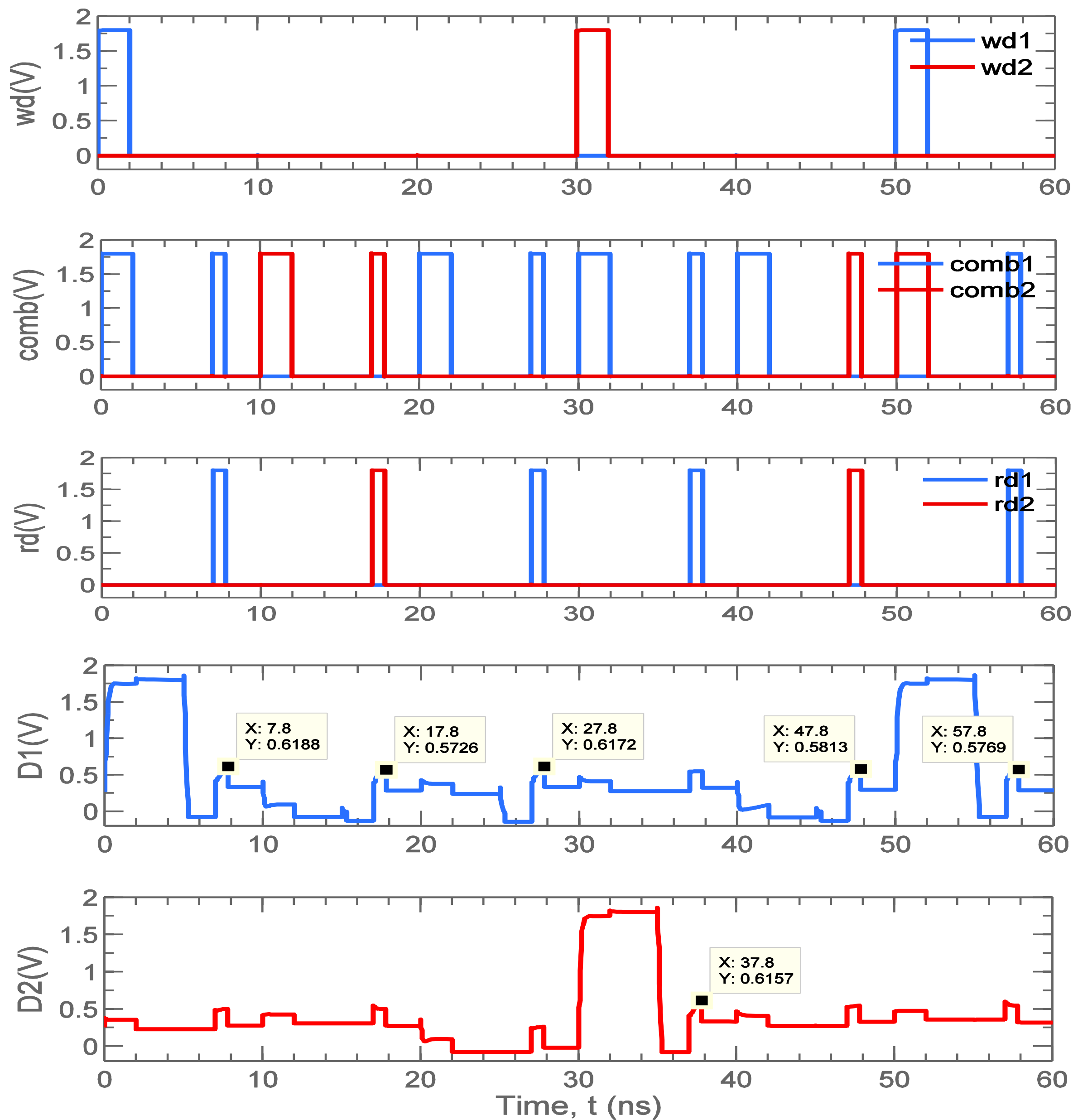


Figure 4.17: write and read different cells and check the output values

At the marked points,

at 7.8ns, d1=0.6188V → Cell17='1'. at 17.8ns, d1=0.5726V → Cell18='0'.

at 27.8ns, d1=0.6172V → Cell17='1'. at 37.8ns, d2=0.6157V → Cell33='1'.

at 47.8ns, d1=0.5813V → Cell18='0'. at 57.8ns, d1=0.5709V → Cell17='0'.

4.5.2 SRAM Array with Sense Amplifier

4.5.2.1 Sense Amplifier

A comparator is a device that compares two voltages or currents and switches its output to indicate which is larger. It compares the voltages at the + and – inputs. If the + input is at a higher voltage than the – input the comparator output will be high. If the – input is at a higher voltage than the + input the comparator output will be low.

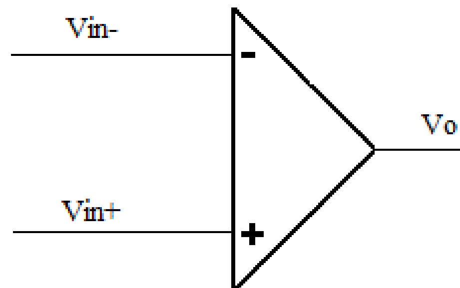


Figure 4.18: A simple voltage comparator

Comparator design specifications:

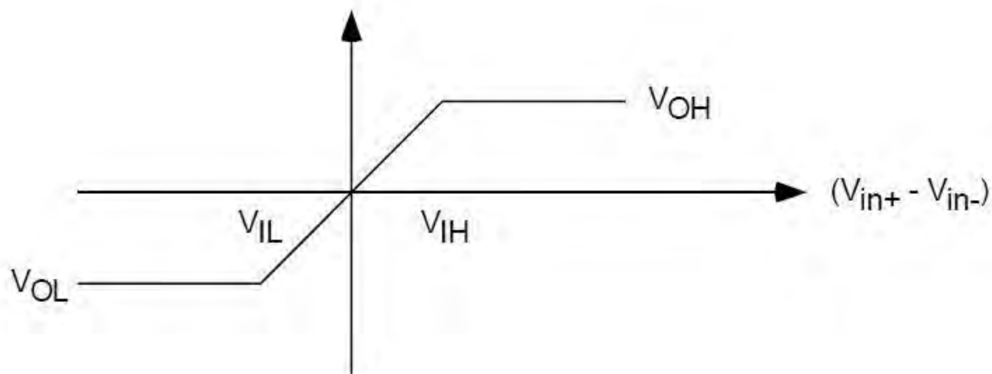


Figure 4.19: Comparator design specification

The output is defined as:

$$V_o = \begin{cases} V_{OH} & if\ (V_{in+} - V_{in-}) > V_{IH} \\ A_V(V_{in+} - V_{in-}) & if\ V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & if\ (V_{in+} - V_{in-}) < V_{IL} \end{cases}$$

The comparator used in our circuit was a two stage CMOS comparator with PMOS input drivers. A reference voltage was used at the negative terminal. The other terminal was

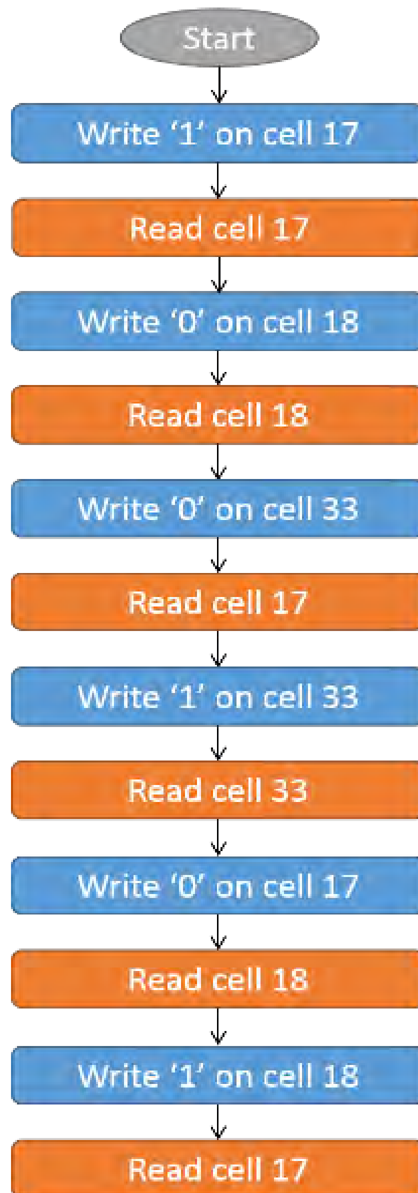
connected to the data line of the SRAM. The voltage was switched to ~1.4V if the voltage at the positive terminal was above the reference voltage and to ~0.3V if it was below. The comparator circuit is shown below:

Figure 4.20: CMOS comparator with PMOS input drivers.

4.5.2.2 ARRAY WITH SENSE AMPLIFIER

Figure 4.21: 16×16 Array Structure of the proposed memristor based SRAM with sense amplifier

The following operations were carried out and functionally of the sense amplifier was tested by checking the resulting output:



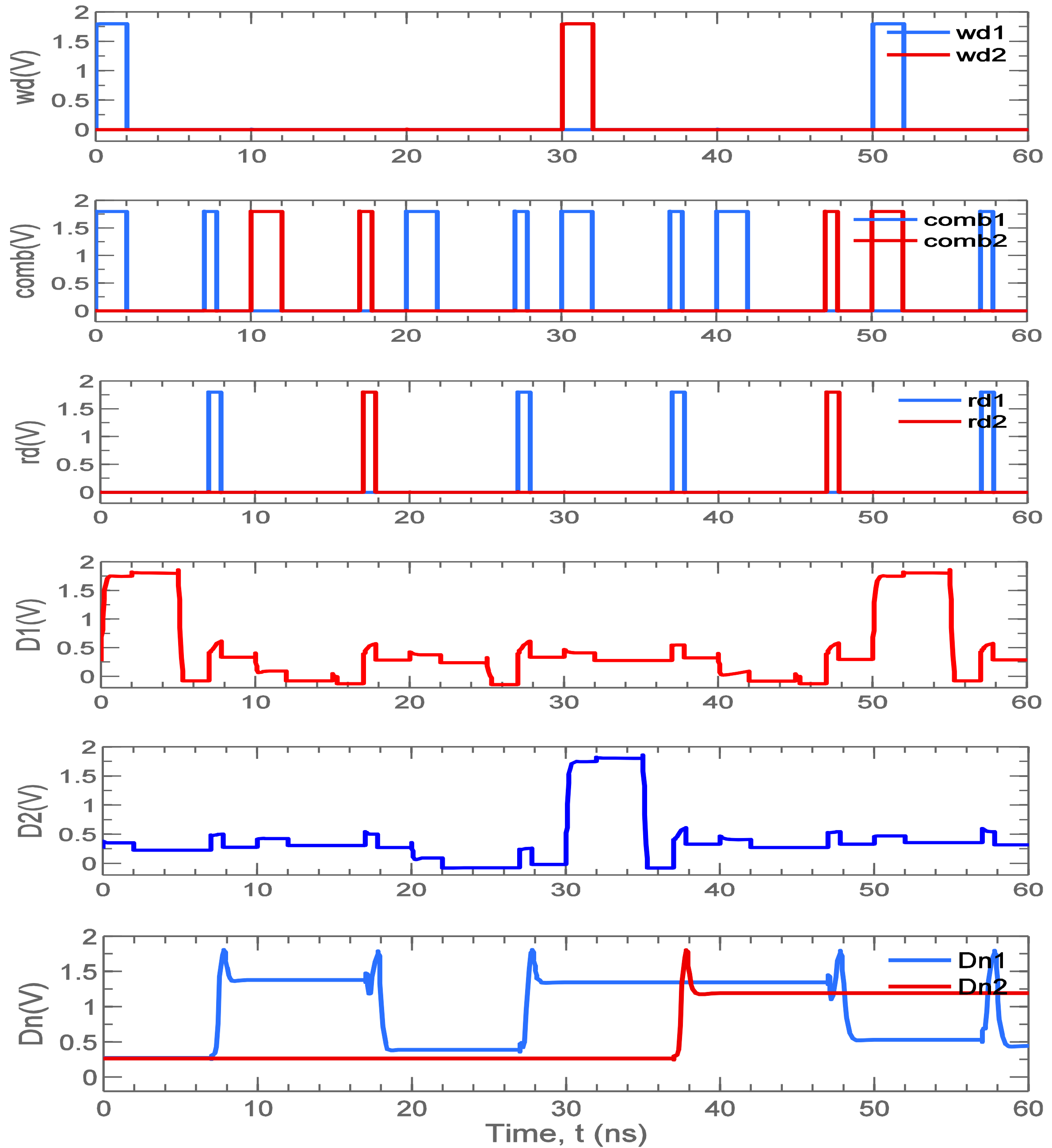


Figure 4.22: Functionality test of sense amplifier in the SRAM array circuit

At the marked points,

at 7.8ns, d1=0.6188V → Cell17='1', at 17.8ns, d1=0.5726V → Cell18='0'.

at 27.8ns, d1=0.6172V → Cell17='1', at 37.8ns, d2=0.6157V → Cell33='1'.

at 47.8ns, d1=0.5813V → Cell18='0', at 57.8ns, d1=0.5709V → Cell17='0'.

So the sense amplifier is perfectly functioning.

4.5.3 Non-volatility

Our proposed memristor based SRAM cell is nonvolatile in nature. To check its non-volatility the following operations were carried out:

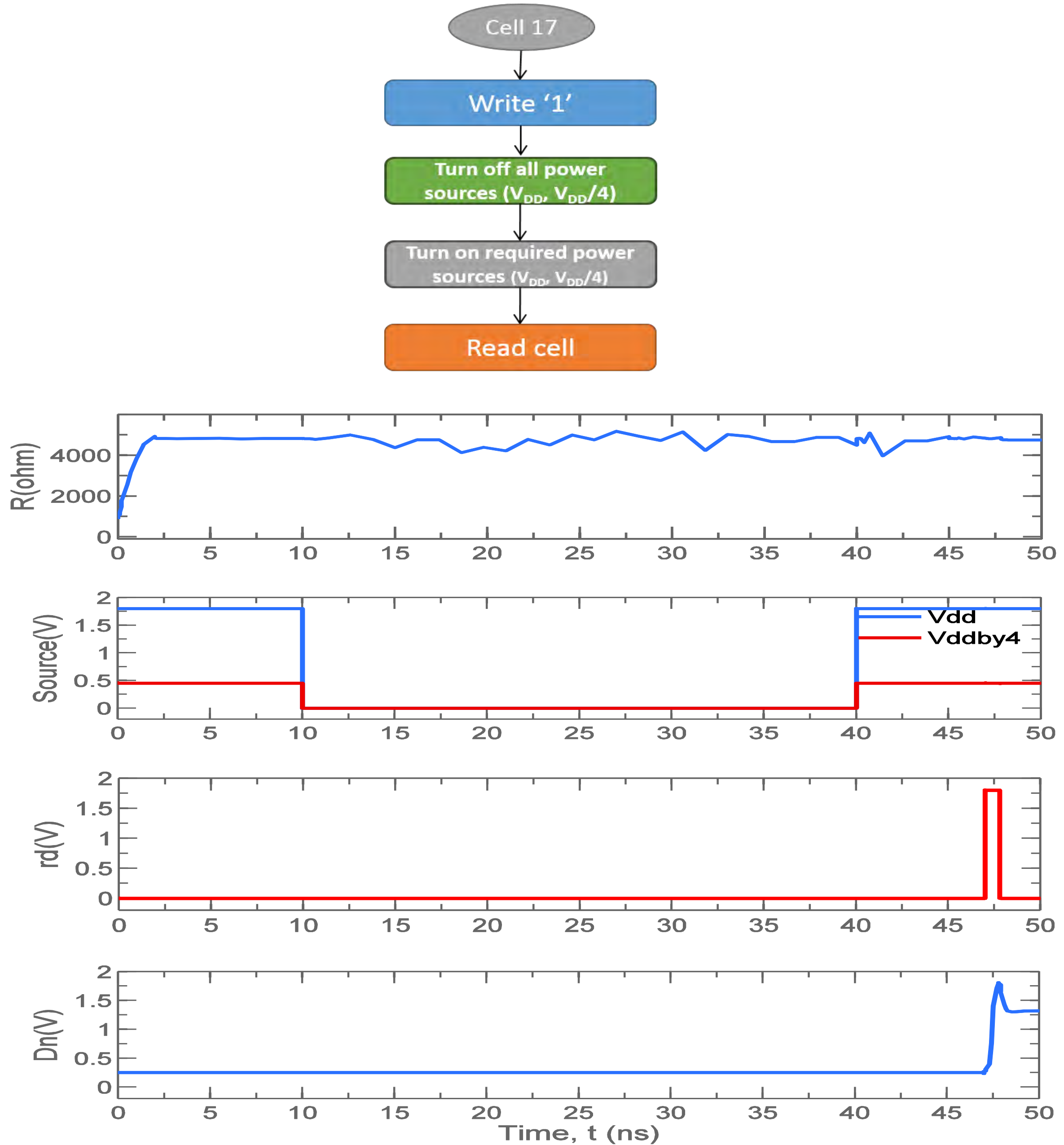


Figure 4.23: Evidence of non-volatility of the Memristor SRAM cell

All the power sources were turned off during the time interval 20ns-50ns. The output value of the sense amplifier was found correctly after the interval. This proves the nonvolatile nature of the circuit.

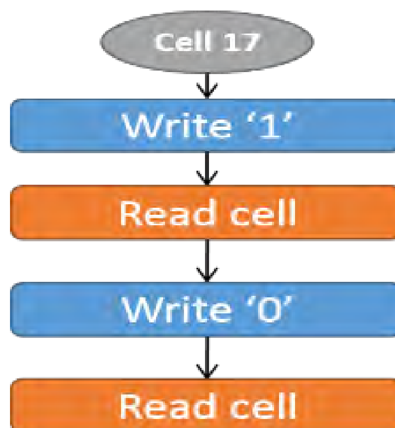
Chapter 5

Analysis and Comparison

This thesis work focuses on studying a novel circuit structure for Memristor-MOS hybrid architecture NVRAM to enhance the read/write speed, reduce power consumption and minimize area. In this chapter we analyzed and compared the performance of proposed NVRAM with existing and other promising memory circuits.

5.1 Timing Analysis

The following operations were carried out:



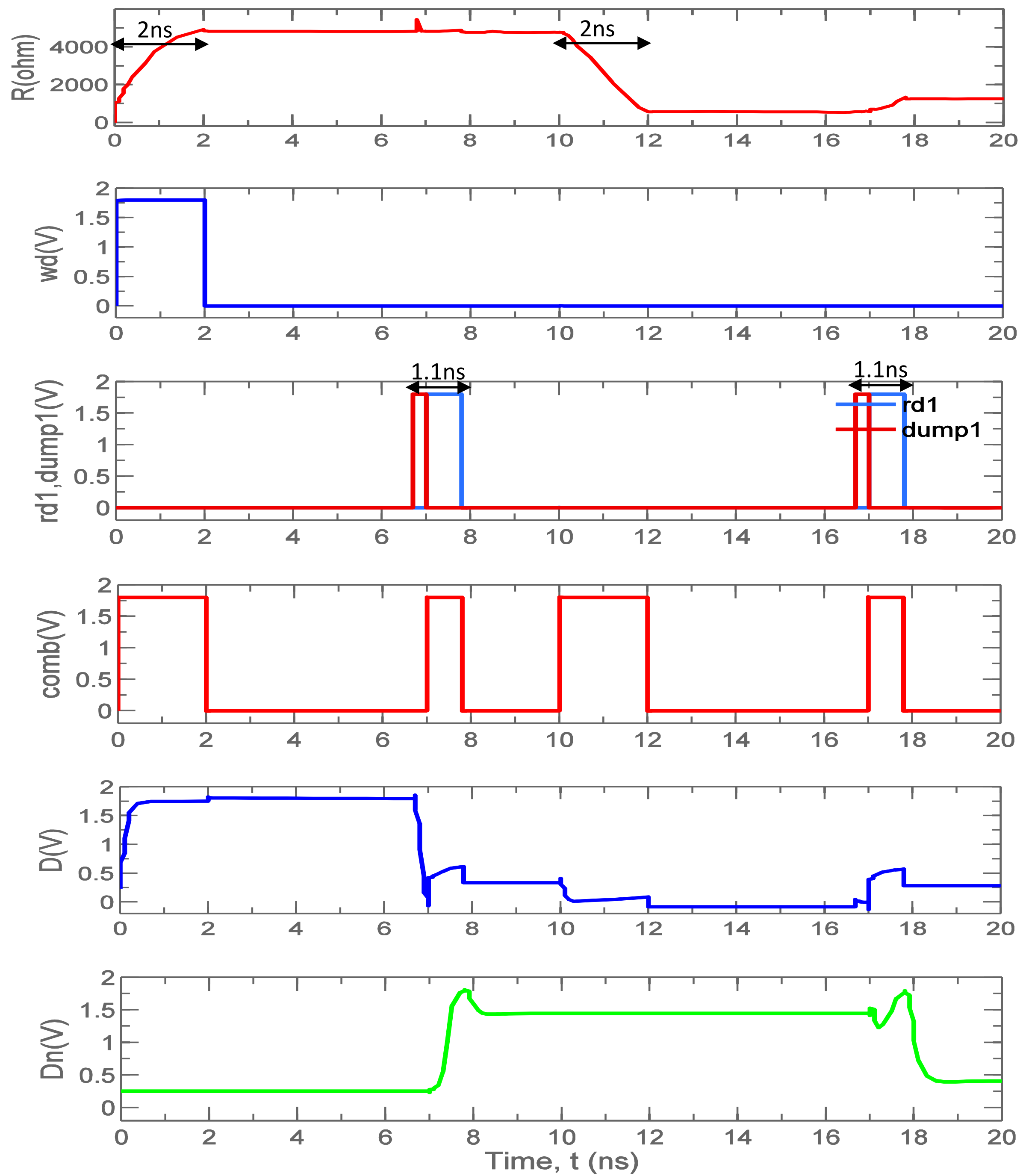


Figure 5.1: Timing Analysis

Write and read times were measured and compared:

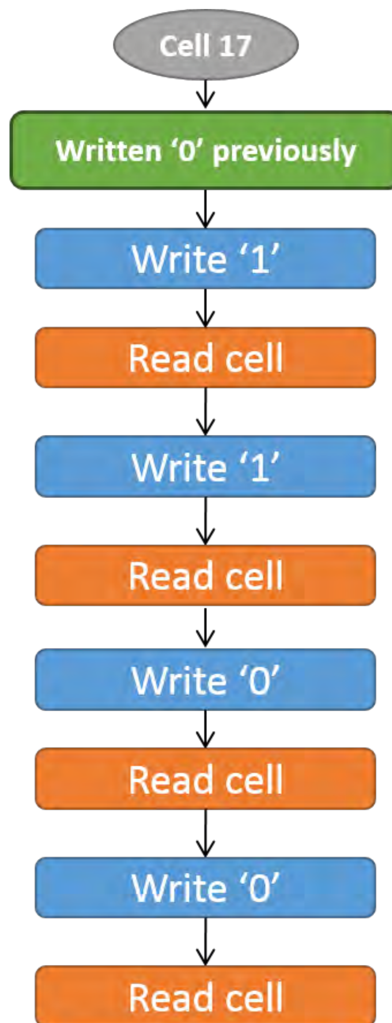
Operation	Proposed SRAM Cell	3T 2M Cell [19]	6T Cell [21]
Write	2ns	5.9ns	0.85ns
Read	1.1ns	0.2ns	1.23ns

Table 5.1: Write and read cycle time comparison

Our proposed SRAM cell requires significant amount of time for the write cycle compared to the conventional 6T SRAM [21], but requires much less time than 3T 2M cell [19]. By increasing the doping of the memristors, the write cycle time can be highly reduced. The read cycle time is depended on sensitivity and responsiveness of sense amplifier. It is less than the conventional 6T SRAM and it can be further reduced by implementing highly sensitive sense amplifiers.

5.2 Power Analysis

The following operations were carried out for the purpose of power analysis.



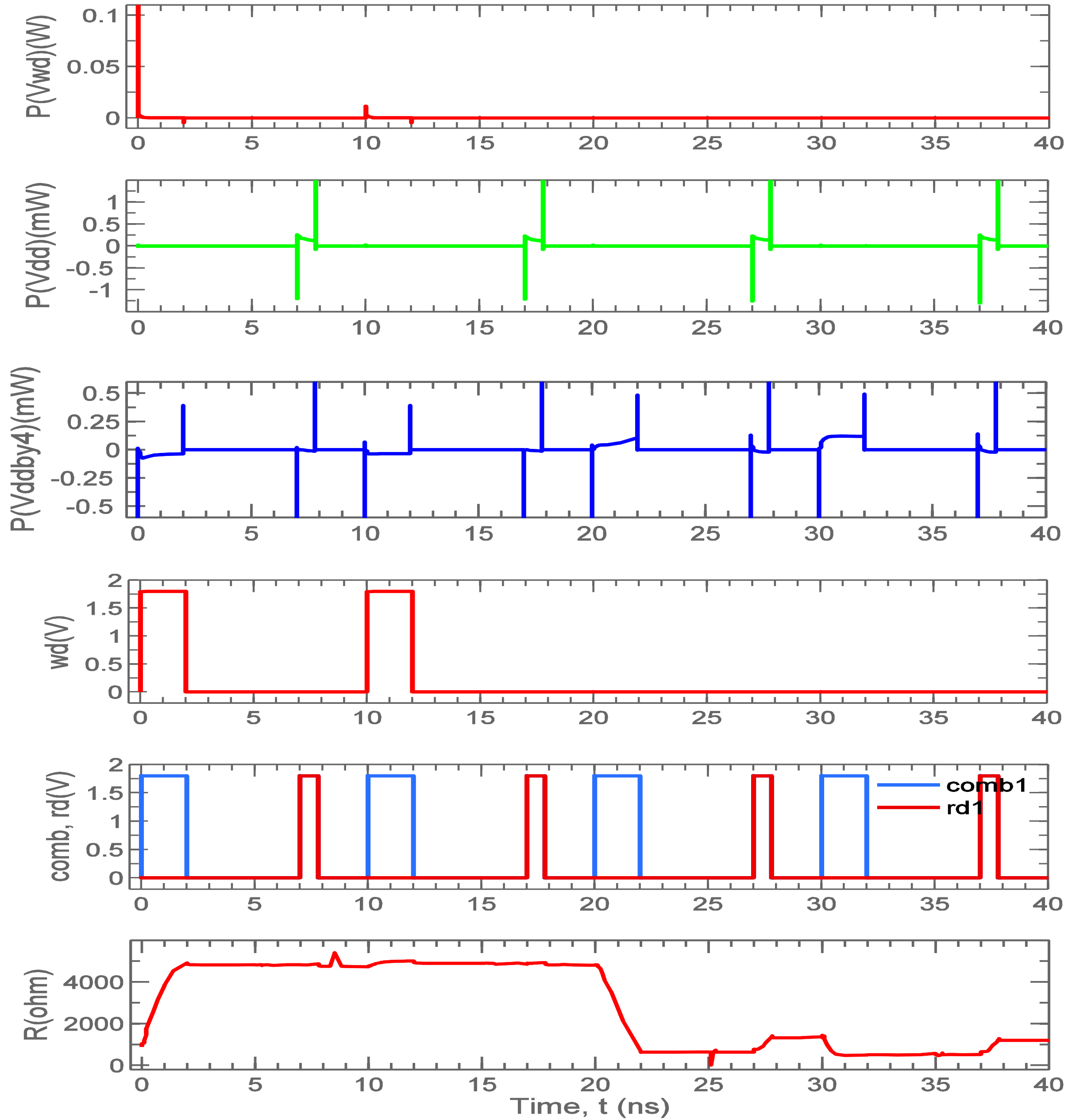


Figure 5.2: Simulation for Power Analysis

From simulation the power dissipation curve was found as showed in figure. Then integration was done to get the write and read energy per cycle. Four cases were considered.

a) 0→1 write and read 1
b) 1→1 write and read 1
c) 1→0 write and read 0
d) 0→0 write and read 0

The results are as follows:

Operation	0→1	1→1	1→0	0→0	Average Energy
Write (fJ/cycle)	731	613	115	220	419.75
Read (fJ/cycle)	125	117	126	131	125.75

Table 5.2: Write and read cycle average energy estimation

From average energy per cycle of write and read operation, average energy of one complete read-write cycle is calculated.

Average energy per cycle = (419.75+125.75) = 544.5 fJ/cycle.

Total cycle time = write cycle + read cycle = 2ns+1.1ns = 3.1ns [322MHz]

Dissipated average power was calculated by means of dividing average energy per cycle by total cycle time.

Comparison:

Operation	Proposed SRAM Cell	3T2M Cell [19]	6T Cell [21]
Average write-read power	0.175mW[322MHz]	0.407mW[165MHz]	10.373mW[500MHz]

Table 5.3: Write-read cycle average power comparison

Our proposed SRAM structure dissipates much less power than the conventional 6T SRAM cell and also the 3T2M SRAM cell. But since these circuits have different speeds, energy per cycle is more relevant to compare. Dissipated average power was multiplied by total cycle time to get total energy per cycle.

Operation	Proposed SRAM Cell	3T2M Cell [19]	6T Cell [21]
Average write-read energy	544.5 (fJ/cycle)	561.93 (fJ/cycle)	21575 (fJ/cycle)

Table 5.4: Write-read cycle average energy comparison

5.3 LAYOUT

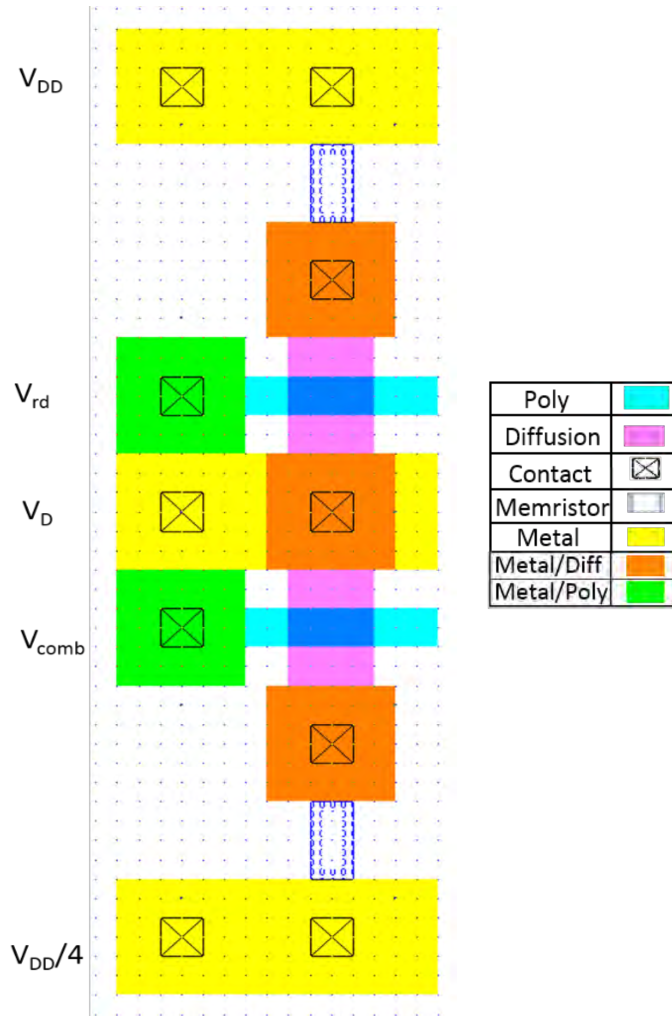


Figure 5.3: Layout of the SRAM cell

Area Estimation

To estimate the area a layout of the leaf cell of our proposed SRAM circuit was drawn using Microwind 2.0 layout design and simulation software. CMOS 0.18µm technology was used which has lambda based design rule with λ=0.09µm. By optimizing the layout we got width, x=15 λ and height, y=50 λ. This corresponds to an area of 15 λ × 50 λ= 6.075µm^2. We do not have proper model and design rules for memristor. Area of the memristor is 0.003µm×0.003µm= 0.000009 µm^2 which is so small compared to the cell area and does not affect the area calculations. We used minimum space required between two contacts for the memristor. For this reason we could not simulate and verify this layout. So this result is an approximation. We compared the cell area with a conventional 6 transistor SRAM cell fabricated in CMOS 0.18µm technology [21]. The results are in table 1.

Area	*Core Cell*	*8Kbit SRAM circuit*
conventional 6 transistor SRAM cell	122.07 μm^2	1×10^6 μm^2 [21]
3T 2M SRAM cell	9.6228μm^2	0.079 $\times10^6$ μm^2 [19]
Proposed 2T 2M SRAM cell	6.0750μm^2	0.049 $\times10^6$ μm^2

Table 5.5: Area estimation and comparison for 180nm process

The area of conventional 6 transistor SRAM cell fabricated in CMOS 0.18µm technology is approximately 20.5 times the area of our proposed SRAM cell. Also the 3T2M SRAM cell fabricated in CMOS 0.18µm technology is approximately 1.61 times the area of our proposed SRAM cell. The area can be more reduced if we can switch to more recent fabrication technologies such as 22nm technology [22].

Using lambda based calculation method we can approximately calculate proposed SRAM core cell area for 45nm process. In table 5 the approximate value is compared with fabricated SRAM of corresponding technology.

Area (45nm process approximation)	*Core Cell*
6T SRAM cell	0.4997 μm^2 [22]
Proposed 2T 2M SRAM cell	0.3797 μm^2

Table 5.6: Area estimation and comparison for 45nm process

From the table we can see that our proposed design can compete with the latest technology in terms of area consumption.

Chapter 6

CONCLUSION AND FUTURE WORK

In this chapter we will summarize the outcome of our proposed non-volatile SRAM cell and discusses the future improvements or works to be done on this circuit.

6.1 CONCLUSION

Till now, SRAMs have been mainly used as cache memories due to its cost and large area. Due to their complex structure and greater number of transistors needed per cell, the cost and the area of conventional SRAM cannot be reduced below a certain level. A few megabytes of SRAM can take up huge area which is simply unacceptable in modern computers. With the increase of varieties of operations performed by computer these days, there is a greater need for large cache memories. So the conventional structures have to make way. And that is where the proposed SRAM structure comes along. As it was shown, the area is reduced by 20.5 times. Along with that, the power consumption is also reduced significantly with not much increase in the reading or writing speed. Though the write cycle time is higher but is still comparable, and the read cycle time is slightly lower than the conventional 6T SRAM cell. As a result, larger memories can be made overcoming the area limitations and with less power consumption.

A vital feature of our proposed structure is its non-volatility. Conventional SRAMs continue their operation on presence of electricity. If electricity is interrupted all data is lost. But in our proposed memristor based SRAM structure, no data is lost in absence of power source which is shown in section *4.5.3*. So, data can be stored and the power can be turned off with the knowledge that the data will be retained after doing so.

So it has two great advantages:

1. It saves electricity: no need for hibernation or sleep mode in operating CPUs.
2. It saves time: rebooting is not required as memory is nonvolatile.

All these features combined can definitely lead to a more efficient SRAM structure which is suitable for both cache memory and storage memory. Having the non-volatile characteristic, the proposed memory cell could be a potential replacement of flash memory. Recent invention of 22nm floating gate transistor [23] makes it strong competitor against the proposed cell because it needs only 1 transistor which is as small as a MOSFET in latest CMOS technology. As our cell needs 2 transistors, cell area is obviously greater than the floating gate transistor cell area and also has lower packing density. But flash memory's main disadvantage is the speed as it takes longer to store data in flash memory. The RAM is the fastest memory available, providing very high read/write speeds and lowest access times. Compared to the access speeds of other storage mediums like hard disks (HDD) or flash memory, which are measured in milliseconds, the access times of RAM is measured in nanoseconds, making it thousands of times faster than any other storage solution. Flash memory also have very high voltage requirements for read-write purpose compared to RAM. So, the nonvolatile characteristics of the proposed memory cell makes it strong contender for flash memory market.

One disadvantage of the proposed structure is low noise margin. For the proposed memory structure noise margin is closely related to sensitivity of the sense amplifier and also the write-read speed. If we want to minimize the write-read time, then the sense amplifier gets less time to respond and gives less satisfactory output performance. More work is needed to improve the sensitivity and response of the sense amplifier which in turns will improve the noise margin. Another problem is the consecutive read operations. New techniques should be devised to read memristance value with following current through it.

6.2 Future Work

The proposed SRAM cell has a bit higher write time. It can be improved by increasing the memristor doping which will increase the mobility. So, there is a scope for improving the device characteristic working on device level. Another technique of achieving faster read cycle would be designing a more efficient and faster sense amplifier. The proposed memory

cell was simulated using TSMC 180nm technology library. But currently in the market more scaled technologies are available. Most of them have similar physical structure, hence are assumed to work satisfactorily if used in the proposed circuit and should also provide improved performance. But the latest 22nm technology has very different structure with 3-D Tri-Gate transistor. It will be a challenge to integrate memristor with this technology and exploit the advantages. New peripheral control circuitry may have to be introduced for this purpose. This can be another scope for research.

Memory architecture is very important for organizing cells in a memory array. We did not design the decoder logic for row-column selection and read-write encoder logic. We assumed the conventional logics are available. Our cell has slightly different data pin combination than conventional 6-T SRAM cell where both complementary forms of data are needed. But our cell only needs non-inverted data. It might be possible to build a different data-bus and selector circuitry which could be more efficient for this cell combination.

Also stability analysis such as read/write failure study, statistical analysis using Monte Carlo simulations to demonstrate variation tolerance can be done for confirming robustness of the scheme.

Chapter 7

REFERENCES

[1] Walker, J. “Fundamentals of Physics” (John Wiley & Sons Inc., New York), 8th ed.

[2] Young, H.D. and Freedman, R.A. “University Physics” (Addison Wesley, New York), 12th ed.

[3] Tipler, P.A. and Mosca, G. “Physics for Scientists and Engineers” (W.H. Freeman and Company, New York), 6th ed.

[4] Ohanian, H.C. and Markert, J.T. “Physics for Engineers and Scientists” (W.W. Norton and Company, New York), 3rd ed.

[5] Feynman, R.P., Leighton, R.B. and Sands, M. “The Feynman Lectures on Physics,” vol. II (Addison Wesley, New York).

[6] Chua, L.O. “Memristor - the missing circuit element,” Circuit Theory, IEEE Transactions on, vol.18, no.5, pp.507-519, Sep 1971.

[7] Chua, L.O. and Kang, S.M. “Memristive devices and systems,” Proceedings of the IEEE 64, no.2, pp. 209-223. 1976.

[8] L.O. Chua, “Device modeling via non-linear circuit elements,” Circuits and Systems, IEEE Transactions on, 27, pp. 1014-1044, 1980.

[9] Thakoor, S., Moopenn, A., Daud,T., and Thakoor, A.P. “Solid-state thin film memristor for electronic neural networks,” J. Appl. Phys. 67, pp. 3132-3135, 1990.

[10] Erokhin,V., Berzina, T.S. and Fontana, M.P., “Polymeric elements for adaptive networks,” Cryst. Report 52, pp. 159-166, 2007.

[11] Strukov, D. B., Snider, G. S., Stewart, D. R., and Williams, R. S. “The missing memristor found,” Nature, vol.453, no.7191, pp.80-83, May 2008

[12] Tour, J.M. and He, T. “The fourth element,” Nature 453, no. 7191: pp. 42-43, 2008.

[13] Vontobel, P. O., Robinett, W., Kuekes, P. J., Stewart, D. R., Straznicky, J., & Williams, R. S. “Writing to and reading from a nano-scale crossbar memory based on memristors” Nanotechnology 20, no. 42, 425204, 2009.

[14] Ebong, I.E.; Mazumder, P., “Self-Controlled Writing and Erasing in a Memristor Crossbar Memory”, Nanotechnology, IEEE Transactions on 10, no.6, pp. 1454-1463, 2011.

[15] Eshraghian, K., Kyoung-Rok C., Kavehei, O., Soon-Ku K., Abbott, D. and Sung-Mo S. K. “Memristor MOS Content Addressable Memory (MCAM): Hybrid Architecture for Future High Performance Search Engines,” Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol.19, no.8, pp.1407-1417, Aug 2011

[16] Biolek, Z., Biolek, D., and Biolkova, V. “SPICE model of memristor with nonlinear dopant drift.” Radio engineering, vol.18, no.2, pp. 210-214. June 2009.

[17] Joglekar, Y. N., and Wolf, S. J. “The elusive memristor: properties of basic electrical circuits.” European Journal of Physics, vol.30, no.4, pp.661-685, 2009.

[18] Seo, H. J., Song, D. K., Lee, J. H., Ahmed, M. G., & Cho, T. W. “A Study on the Memristor-based Non-Volatile 4T Static RAM Cell”. In proceeding of: The 26th International Technical Conference on Circuits/Systems, Computers and Communications. June 2011.

[19] Sarwar, S.S., Saqueb, S.A.N., Quaiyum, F. and Rashid, A.B.M.H.-U. “Memristor-Based Nonvolatile Random Access Memory: Hybrid Architecture for Low Power Compact Memory Design,” Access, IEEE, vol.1, no.1, pp.29-34, 2013.

[20] *Memristor - HP Touts 3nM Memristor Fabrication Milestones*. Available:
http://www.memristor.org/news/222/hp-touts-3nm-memristor-fabrication-milestones

[21] Reddy, G.M.S., and Reddy, P.C. "*Design and Implementation of 8K-bits Low Power SRAM in 180nm Technology*," In Proceedings of the International Multi Conference of Engineers and Compute Scientists, vol. 2, pp. 18-20, March 2009.

[22] Kawasumi, A., Yabe, T., Takeyama, Y., Hirabayashi, O., Kushida, K., Tohata, A., Sasaki, T. et al. “A Single-Power-Supply 0.7 V 1GHz 45nm SRAM with An Asymmetrical Unit-Ã-ratio Memory Cell.” In Solid-State Circuits Conference, ISSCC. Digest of Technical Papers. IEEE International, pp. 382-622. IEEE, 2008.

[23] Postel-Pellerin, J., F. Lalande, P. Canet, R. Bouchakour, F. Jeuland, B. Bertello, and B. Villard, “A full 2D and 3D TCAD simulation of ultimate 22nm NAND Flash memories,” In Non-Volatile Memory Technology Symposium (NVMTS), 10th Annual, pp. 80-82. IEEE, 2009.

APPENDIX A

SIMULATION CODES

PSPICE CODE FOR SECTION 4.5.1.1

Validity Test

```
xsram0rd0	comb0		d0	v2d0	Vdd0	sram
xsram1rd1	comb1		d0	v2d0	Vdd0	sram
xsram2rd2	comb2		d0	v2d0	Vdd0	sram
xsram3rd3	comb3		d0	v2d0	Vdd0	sram
xsram4rd4	comb4		d0	v2d0	Vdd0	sram
xsram5rd5	comb5		d0	v2d0	Vdd0	sram
xsram6rd6	comb6		d0	v2d0	Vdd0	sram
xsram7rd7	comb7		d0	v2d0	Vdd0	sram
xsram8rd8	comb8		d0	v2d0	Vdd0	sram
xsram9rd9	comb9		d0	v2d0	Vdd0	sram
xsram10		rd10	comb10	d0	v2d0	Vdd0	sram
xsram11		rd11	comb11	d0	v2d0	Vdd0	sram
xsram12		rd12	comb12	d0	v2d0	Vdd0	sram
xsram13		rd13	comb13	d0	v2d0	Vdd0	sram
xsram14		rd14	comb14	d0	v2d0	Vdd0	sram
xsram15		rd15	comb15	d0	v2d0	Vdd0	sram

xsram16		rd0	comb0	d1	v2d1	Vdd1	sram
xsram17		rd1	comb1	d1	v2d1	Vdd1	sram
xsram18		rd2	comb2	d1	v2d1	Vdd1	sram
xsram19		rd3	comb3	d1	v2d1	Vdd1	sram
xsram20		rd4	comb4	d1	v2d1	Vdd1	sram
xsram21		rd5	comb5	d1	v2d1	Vdd1	sram
xsram22		rd6	comb6	d1	v2d1	Vdd1	sram
xsram23		rd7	comb7	d1	v2d1	Vdd1	sram
xsram24		rd8	comb8	d1	v2d1	Vdd1	sram
xsram25		rd9	comb9	d1	v2d1	Vdd1	sram
xsram26		rd10	comb10	d1	v2d1	Vdd1	sram
xsram27		rd11	comb11	d1	v2d1	Vdd1	sram
xsram28		rd12	comb12	d1	v2d1	Vdd1	sram
xsram29		rd13	comb13	d1	v2d1	Vdd1	sram
xsram30		rd14	comb14	d1	v2d1	Vdd1	sram
xsram31		rd15	comb15	d1	v2d1	Vdd1	sram
```

```
xsram32    rd0    comb0     d2    v2d2    Vdd2    sram
xsram33    rd1    comb1     d2    v2d2    Vdd2    sram
xsram34    rd2    comb2     d2    v2d2    Vdd2    sram
xsram35    rd3    comb3     d2    v2d2    Vdd2    sram
xsram36    rd4    comb4     d2    v2d2    Vdd2    sram
xsram37    rd5    comb5     d2    v2d2    Vdd2    sram
xsram38    rd6    comb6     d2    v2d2    Vdd2    sram
xsram39    rd7    comb7     d2    v2d2    Vdd2    sram
xsram40    rd8    comb8     d2    v2d2    Vdd2    sram
xsram41    rd9    comb9     d2    v2d2    Vdd2    sram
xsram42    rd10   comb10    d2    v2d2    Vdd2    sram
xsram43    rd11   comb11    d2    v2d2    Vdd2    sram
xsram44    rd12   comb12    d2    v2d2    Vdd2    sram
xsram45    rd13   comb13    d2    v2d2    Vdd2    sram
xsram46    rd14   comb14    d2    v2d2    Vdd2    sram
xsram47    rd15   comb15    d2    v2d2    Vdd2    sram

xsram48    rd0    comb0     d3    v2d3    Vdd3    sram
xsram49    rd1    comb1     d3    v2d3    Vdd3    sram
xsram50    rd2    comb2     d3    v2d3    Vdd3    sram
xsram51    rd3    comb3     d3    v2d3    Vdd3    sram
xsram52    rd4    comb4     d3    v2d3    Vdd3    sram
xsram53    rd5    comb5     d3    v2d3    Vdd3    sram
xsram54    rd6    comb6     d3    v2d3    Vdd3    sram
xsram55    rd7    comb7     d3    v2d3    Vdd3    sram
xsram56    rd8    comb8     d3    v2d3    Vdd3    sram
xsram57    rd9    comb9     d3    v2d3    Vdd3    sram
xsram58    rd10   comb10    d3    v2d3    Vdd3    sram
xsram59    rd11   comb11    d3    v2d3    Vdd3    sram
xsram60    rd12   comb12    d3    v2d3    Vdd3    sram
xsram61    rd13   comb13    d3    v2d3    Vdd3    sram
xsram62    rd14   comb14    d3    v2d3    Vdd3    sram
xsram63    rd15   comb15    d3    v2d3    Vdd3    sram

xsram64    rd0    comb0     d4    v2d4    Vdd4    sram
xsram65    rd1    comb1     d4    v2d4    Vdd4    sram
xsram66    rd2    comb2     d4    v2d4    Vdd4    sram
xsram67    rd3    comb3     d4    v2d4    Vdd4    sram
xsram68    rd4    comb4     d4    v2d4    Vdd4    sram
xsram69    rd5    comb5     d4    v2d4    Vdd4    sram
xsram70    rd6    comb6     d4    v2d4    Vdd4    sram
xsram71    rd7    comb7     d4    v2d4    Vdd4    sram
xsram72    rd8    comb8     d4    v2d4    Vdd4    sram
```

```
xsram73   rd9    comb9    d4   v2d4   Vdd4   sram
xsram74   rd10   comb10   d4   v2d4   Vdd4   sram
xsram75   rd11   comb11   d4   v2d4   Vdd4   sram
xsram76   rd12   comb12   d4   v2d4   Vdd4   sram
xsram77   rd13   comb13   d4   v2d4   Vdd4   sram
xsram78   rd14   comb14   d4   v2d4   Vdd4   sram
xsram79   rd15   comb15   d4   v2d4   Vdd4   sram

xsram80   rd0    comb0    d5   v2d5   Vdd5   sram
xsram81   rd1    comb1    d5   v2d5   Vdd5   sram
xsram82   rd2    comb2    d5   v2d5   Vdd5   sram
xsram83   rd3    comb3    d5   v2d5   Vdd5   sram
xsram84   rd4    comb4    d5   v2d5   Vdd5   sram
xsram85   rd5    comb5    d5   v2d5   Vdd5   sram
xsram86   rd6    comb6    d5   v2d5   Vdd5   sram
xsram87   rd7    comb7    d5   v2d5   Vdd5   sram
xsram88   rd8    comb8    d5   v2d5   Vdd5   sram
xsram89   rd9    comb9    d5   v2d5   Vdd5   sram
xsram90   rd10   comb10   d5   v2d5   Vdd5   sram
xsram91   rd11   comb11   d5   v2d5   Vdd5   sram
xsram92   rd12   comb12   d5   v2d5   Vdd5   sram
xsram93   rd13   comb13   d5   v2d5   Vdd5   sram
xsram94   rd14   comb14   d5   v2d5   Vdd5   sram
xsram95   rd15   comb15   d5   v2d5   Vdd5   sram

xsram96   rd0    comb0    d6   v2d6   Vdd6   sram
xsram97   rd1    comb1    d6   v2d6   Vdd6   sram
xsram98   rd2    comb2    d6   v2d6   Vdd6   sram
xsram99   rd3    comb3    d6   v2d6   Vdd6   sram
xsram100  rd4    comb4    d6   v2d6   Vdd6   sram
xsram101  rd5    comb5    d6   v2d6   Vdd6   sram
xsram102  rd6    comb6    d6   v2d6   Vdd6   sram
xsram103  rd7    comb7    d6   v2d6   Vdd6   sram
xsram104  rd8    comb8    d6   v2d6   Vdd6   sram
xsram105  rd9    comb9    d6   v2d6   Vdd6   sram
xsram106  rd10   comb10   d6   v2d6   Vdd6   sram
xsram107  rd11   comb11   d6   v2d6   Vdd6   sram
xsram108  rd12   comb12   d6   v2d6   Vdd6   sram
xsram109  rd13   comb13   d6   v2d6   Vdd6   sram
xsram110  rd14   comb14   d6   v2d6   Vdd6   sram
xsram111  rd15   comb15   d6   v2d6   Vdd6   sram

xsram112  rd0    comb0    d7   v2d7   Vdd7   sram
xsram113  rd1    comb1    d7   v2d7   Vdd7   sram
```

```
xsram114   rd2    comb2     d7   v2d7   Vdd7   sram
xsram115   rd3    comb3     d7   v2d7   Vdd7   sram
xsram116   rd4    comb4     d7   v2d7   Vdd7   sram
xsram117   rd5    comb5     d7   v2d7   Vdd7   sram
xsram118   rd6    comb6     d7   v2d7   Vdd7   sram
xsram119   rd7    comb7     d7   v2d7   Vdd7   sram
xsram120   rd8    comb8     d7   v2d7   Vdd7   sram
xsram121   rd9    comb9     d7   v2d7   Vdd7   sram
xsram122   rd10   comb10    d7   v2d7   Vdd7   sram
xsram123   rd11   comb11    d7   v2d7   Vdd7   sram
xsram124   rd12   comb12    d7   v2d7   Vdd7   sram
xsram125   rd13   comb13    d7   v2d7   Vdd7   sram
xsram126   rd14   comb14    d7   v2d7   Vdd7   sram
xsram127   rd15   comb15    d7   v2d7   Vdd7   sram

xsram128   rd0    comb0     d8   v2d8   Vdd8   sram
xsram129   rd1    comb1     d8   v2d8   Vdd8   sram
xsram130   rd2    comb2     d8   v2d8   Vdd8   sram
xsram131   rd3    comb3     d8   v2d8   Vdd8   sram
xsram132   rd4    comb4     d8   v2d8   Vdd8   sram
xsram133   rd5    comb5     d8   v2d8   Vdd8   sram
xsram134   rd6    comb6     d8   v2d8   Vdd8   sram
xsram135   rd7    comb7     d8   v2d8   Vdd8   sram
xsram136   rd8    comb8     d8   v2d8   Vdd8   sram
xsram137   rd9    comb9     d8   v2d8   Vdd8   sram
xsram138   rd10   comb10    d8   v2d8   Vdd8   sram
xsram139   rd11   comb11    d8   v2d8   Vdd8   sram
xsram140   rd12   comb12    d8   v2d8   Vdd8   sram
xsram141   rd13   comb13    d8   v2d8   Vdd8   sram
xsram142   rd14   comb14    d8   v2d8   Vdd8   sram
xsram143   rd15   comb15    d8   v2d8   Vdd8   sram

xsram144   rd0    comb0     d9   v2d9   Vdd9   sram
xsram145   rd1    comb1     d9   v2d9   Vdd9   sram
xsram146   rd2    comb2     d9   v2d9   Vdd9   sram
xsram147   rd3    comb3     d9   v2d9   Vdd9   sram
xsram148   rd4    comb4     d9   v2d9   Vdd9   sram
xsram149   rd5    comb5     d9   v2d9   Vdd9   sram
xsram150   rd6    comb6     d9   v2d9   Vdd9   sram
xsram151   rd7    comb7     d9   v2d9   Vdd9   sram
xsram152   rd8    comb8     d9   v2d9   Vdd9   sram
xsram153   rd9    comb9     d9   v2d9   Vdd9   sram
xsram154   rd10   comb10    d9   v2d9   Vdd9   sram
xsram155   rd11   comb11    d9   v2d9   Vdd9   sram
```

```
xsram156   rd12   comb12   d9    v2d9   Vdd9   sram
xsram157   rd13   comb13   d9    v2d9   Vdd9   sram
xsram158   rd14   comb14   d9    v2d9   Vdd9   sram
xsram159   rd15   comb15   d9    v2d9   Vdd9   sram

xsram160   rd0    comb0    d10   v2d10  Vdd10  sram
xsram161   rd1    comb1    d10   v2d10  Vdd10  sram
xsram162   rd2    comb2    d10   v2d10  Vdd10  sram
xsram163   rd3    comb3    d10   v2d10  Vdd10  sram
xsram164   rd4    comb4    d10   v2d10  Vdd10  sram
xsram165   rd5    comb5    d10   v2d10  Vdd10  sram
xsram166   rd6    comb6    d10   v2d10  Vdd10  sram
xsram167   rd7    comb7    d10   v2d10  Vdd10  sram
xsram168   rd8    comb8    d10   v2d10  Vdd10  sram
xsram169   rd9    comb9    d10   v2d10  Vdd10  sram
xsram170   rd10   comb10   d10   v2d10  Vdd10  sram
xsram171   rd11   comb11   d10   v2d10  Vdd10  sram
xsram172   rd12   comb12   d10   v2d10  Vdd10  sram
xsram173   rd13   comb13   d10   v2d10  Vdd10  sram
xsram174   rd14   comb14   d10   v2d10  Vdd10  sram
xsram175   rd15   comb15   d10   v2d10  Vdd10  sram

xsram176   rd0    comb0    d11   v2d11  Vdd11  sram
xsram177   rd1    comb1    d11   v2d11  Vdd11  sram
xsram178   rd2    comb2    d11   v2d11  Vdd11  sram
xsram179   rd3    comb3    d11   v2d11  Vdd11  sram
xsram180   rd4    comb4    d11   v2d11  Vdd11  sram
xsram181   rd5    comb5    d11   v2d11  Vdd11  sram
xsram182   rd6    comb6    d11   v2d11  Vdd11  sram
xsram183   rd7    comb7    d11   v2d11  Vdd11  sram
xsram184   rd8    comb8    d11   v2d11  Vdd11  sram
xsram185   rd9    comb9    d11   v2d11  Vdd11  sram
xsram186   rd10   comb10   d11   v2d11  Vdd11  sram
xsram187   rd11   comb11   d11   v2d11  Vdd11  sram
xsram188   rd12   comb12   d11   v2d11  Vdd11  sram
xsram189   rd13   comb13   d11   v2d11  Vdd11  sram
xsram190   rd14   comb14   d11   v2d11  Vdd11  sram
xsram191   rd15   comb15   d11   v2d11  Vdd11  sram

xsram192   rd0    comb0    d12   v2d12  Vdd12  sram
xsram193   rd1    comb1    d12   v2d12  Vdd12  sram
xsram194   rd2    comb2    d12   v2d12  Vdd12  sram
xsram195   rd3    comb3    d12   v2d12  Vdd12  sram
xsram196   rd4    comb4    d12   v2d12  Vdd12  sram
```

```
xsram197   rd5    comb5    d12   v2d12  Vdd12  sram
xsram198   rd6    comb6    d12   v2d12  Vdd12  sram
xsram199   rd7    comb7    d12   v2d12  Vdd12  sram
xsram200   rd8    comb8    d12   v2d12  Vdd12  sram
xsram201   rd9    comb9    d12   v2d12  Vdd12  sram
xsram202   rd10   comb10   d12   v2d12  Vdd12  sram
xsram203   rd11   comb11   d12   v2d12  Vdd12  sram
xsram204   rd12   comb12   d12   v2d12  Vdd12  sram
xsram205   rd13   comb13   d12   v2d12  Vdd12  sram
xsram206   rd14   comb14   d12   v2d12  Vdd12  sram
xsram207   rd15   comb15   d12   v2d12  Vdd12  sram

xsram208   rd0    comb0    d13   v2d13  Vdd13  sram
xsram209   rd1    comb1    d13   v2d13  Vdd13  sram
xsram210   rd2    comb2    d13   v2d13  Vdd13  sram
xsram211   rd3    comb3    d13   v2d13  Vdd13  sram
xsram212   rd4    comb4    d13   v2d13  Vdd13  sram
xsram213   rd5    comb5    d13   v2d13  Vdd13  sram
xsram214   rd6    comb6    d13   v2d13  Vdd13  sram
xsram215   rd7    comb7    d13   v2d13  Vdd13  sram
xsram216   rd8    comb8    d13   v2d13  Vdd13  sram
xsram217   rd9    comb9    d13   v2d13  Vdd13  sram
xsram218   rd10   comb10   d13   v2d13  Vdd13  sram
xsram219   rd11   comb11   d13   v2d13  Vdd13  sram
xsram220   rd12   comb12   d13   v2d13  Vdd13  sram
xsram221   rd13   comb13   d13   v2d13  Vdd13  sram
xsram222   rd14   comb14   d13   v2d13  Vdd13  sram
xsram223   rd15   comb15   d13   v2d13  Vdd13  sram

xsram224   rd0    comb0    d14   v2d14  Vdd14  sram
xsram225   rd1    comb1    d14   v2d14  Vdd14  sram
xsram226   rd2    comb2    d14   v2d14  Vdd14  sram
xsram227   rd3    comb3    d14   v2d14  Vdd14  sram
xsram228   rd4    comb4    d14   v2d14  Vdd14  sram
xsram229   rd5    comb5    d14   v2d14  Vdd14  sram
xsram230   rd6    comb6    d14   v2d14  Vdd14  sram
xsram231   rd7    comb7    d14   v2d14  Vdd14  sram
xsram232   rd8    comb8    d14   v2d14  Vdd14  sram
xsram233   rd9    comb9    d14   v2d14  Vdd14  sram
xsram234   rd10   comb10   d14   v2d14  Vdd14  sram
xsram235   rd11   comb11   d14   v2d14  Vdd14  sram
xsram236   rd12   comb12   d14   v2d14  Vdd14  sram
xsram237   rd13   comb13   d14   v2d14  Vdd14  sram
xsram238   rd14   comb14   d14   v2d14  Vdd14  sram
```

```
xsram239      rd15    comb15        d14     v2d14  Vdd14  sram

xsram240      rd0     comb0         d15     v2d15  Vdd15  sram
xsram241      rd1     comb1         d15     v2d15  Vdd15  sram
xsram242      rd2     comb2         d15     v2d15  Vdd15  sram
xsram243      rd3     comb3         d15     v2d15  Vdd15  sram
xsram244      rd4     comb4         d15     v2d15  Vdd15  sram
xsram245      rd5     comb5         d15     v2d15  Vdd15  sram
xsram246      rd6     comb6         d15     v2d15  Vdd15  sram
xsram247      rd7     comb7         d15     v2d15  Vdd15  sram
xsram248      rd8     comb8         d15     v2d15  Vdd15  sram
xsram249      rd9     comb9         d15     v2d15  Vdd15  sram
xsram250      rd10    comb10        d15     v2d15  Vdd15  sram
xsram251      rd11    comb11        d15     v2d15  Vdd15  sram
xsram252      rd12    comb12        d15     v2d15  Vdd15  sram
xsram253      rd13    comb13        d15     v2d15  Vdd15  sram
xsram254      rd14    comb14        d15     v2d15  Vdd15  sram
xsram255      rd15    comb15        d15     v2d15  Vdd15  sram


vddby4 P2 0 dc 0.45v
vdd P1 0 dc 1.8v


vrd0 rds0 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd0 rds0 rd0 5

vrd1 rds1 0 PWL (
+   0.0 0.0

+       07e-9         0
+       07.01e-9      1.8
+       07.81e-9              1.8
+       07.82e-9      0.0

+       27e-9         0
+       27.01e-9      1.8
+       27.81e-9              1.8
+       27.82e-9      0.0
```

```
+        37e-9          0
+        37.01e-9       1.8
+        37.81e-9                 1.8
+        37.82e-9       0.0

+        57e-9          0
+        57.01e-9       1.8
+        57.81e-9                 1.8
+        57.82e-9       0.0

+        67e-9          0
+        67.01e-9       1.8
+        67.81e-9                 1.8
+        67.82e-9       0.0

+        87e-9          0
+        87.01e-9       1.8
+        87.81e-9                 1.8
+        87.82e-9       0.0

+   150.00e-9 0.0
  )
rsrd1 rds1 rd1 5

vrd2 rds2 0 PWL (
+   0.0 0.0

+        17e-9          0
+        17.01e-9       1.8
+        17.81e-9                 1.8
+        17.82e-9       0.0


+        47e-9          0
+        47.01e-9       1.8
+        47.81e-9                 1.8
+        47.82e-9       0.0

+        77e-9          0
+        77.01e-9       1.8
+        77.81e-9                 1.8
+        77.82e-9       0.0
```

```
+   150.00e-9 0.0
   )
rsrd2 rds2 rd2 5

vrd3 rds3 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd3 rds3 rd3 5

vrd4 rds4 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd4 rds4 rd4 5

vrd5 rds5 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd5 rds5 rd5 5

vrd6 rds6 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd6 rds6 rd6 5

vrd7 rds7 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd7 rds7 rd7 5

vrd8 rds8 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
```

```
rsrd8 rds8 rd8 5

vrd9 rds9 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd9 rds9 rd9 5

vrd10 rds10 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd10 rds10 rd10 5

vrd11 rds11 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd11 rds11 rd11 5

vrd12 rds12 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd12 rds12 rd12 5

vrd13 rds13 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd13 rds13 rd13 5

vrd14 rds14 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd14 rds14 rd14 5
```

```
vrd15 rds15 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rsrd15 rds15 rd15 5


vdt0 dts0 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt0 dts0 dt0 5

vdt1 dts1 0 PWL (
+   0.0 0.0
+       0.01e-9     1.8
+       02e-9       1.8
+       02.02e-9    0.0

+       10e-9       0
+       10.01e-9    1.8
+       12e-9       1.8
+       12.02e-9    0.0

+       30e-9       0
+       30.01e-9    1.8
+       32e-9       1.8
+       32.02e-9    0.0

+       40e-9       0
+       40.01e-9    1.8
+       42e-9       1.8
+       42.02e-9    0.0

+       70e-9       0
+       70.01e-9    1.8
+       72e-9       1.8
+       72.02e-9    0.0

+       80e-9       0
+       80.01e-9    1.8
+       82e-9       1.8
+       82.02e-9    0.0
```

```
+   150.00e-9 0.0
   )
rsdt1 dts1 dt1 5

vdt2 dts2 0 PWL (
+   0.0 0.0

+       20e-9       0
+       20.01e-9    1.8
+       22e-9       1.8
+       22.02e-9    0.0

+       50e-9       0
+       50.01e-9    1.8
+       52e-9       1.8
+       52.02e-9    0.0

+       60e-9       0
+       60.01e-9    1.8
+       62e-9       1.8
+       62.02e-9    0.0

+   150.00e-9 0.0
   )
rsdt2 dts2 dt2 5

vdt3 dts3 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt3 dts3 dt3 5

vdt4 dts4 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt4 dts4 dt4 5

vdt5 dts5 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
```

```
rsdt5 dts5 dt5 5

vdt6 dts6 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt6 dts6 dt6 5

vdt7 dts7 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt7 dts7 dt7 5

vdt8 dts8 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt8 dts8 dt8 5

vdt9 dts9 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt9 dts9 dt9 5

vdt10 dts10 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt10 dts10 dt10 5

vdt11 dts11 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt11 dts11 dt11 5

vdt12 dts12 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt12 dts12 dt12 5
```

```
vdt13 dts13 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt13 dts13 dt13 5

vdt14 dts14 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt14 dts14 dt14 5

vdt15 dts15 0 PWL (
+   0.0 0.0
+   150.00e-9 0.0
   )
rsdt15 dts15 dt15 5



vdtb0 dtbs0 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb0 dtbs0 dtb0 5

vdtb1 dtbs1 0 PWL (
+   0.0 1.8
+         0.01e-9          0
+         02e-9            0
+         02.02e-9         1.8

+         10e-9            1.8
+         10.01e-9         0
+         12e-9            0
+         12.02e-9         1.8

+         30e-9            1.8
+         30.01e-9         0
+         32e-9            0
+         32.02e-9         1.8

+         40e-9            1.8
```

```
+        40.01e-9        0
+        42e-9           0
+        42.02e-9        1.8

+        70e-9           1.8
+        70.01e-9        0
+        72e-9           0
+        72.02e-9        1.8

+        80e-9           1.8
+        80.01e-9        0
+        82e-9           0
+        82.02e-9        1.8

+   150.00e-9 1.8
   )
rsdtb1 dtbs1 dtb1 5

vdtb2 dtbs2 0 PWL (
+   0.0 1.8

+        20e-9           1.8
+        20.01e-9        0
+        22e-9           0
+        22.02e-9        1.8

+        50e-9           1.8
+        50.01e-9        0
+        52e-9           0
+        52.02e-9        1.8

+        60e-9           1.8
+        60.01e-9        0
+        62e-9           0
+        62.02e-9        1.8

+   150.00e-9 1.8
   )
rsdtb2 dtbs2 dtb2 5

vdtb3 dtbs3 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
```

```
   )
rsdtb3 dtbs3 dtb3 5

vdtb4 dtbs4 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb4 dtbs4 dtb4 5

vdtb5 dtbs5 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb5 dtbs5 dtb5 5

vdtb6 dtbs6 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb6 dtbs6 dtb6 5

vdtb7 dtbs7 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb7 dtbs7 dtb7 5

vdtb8 dtbs8 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb8 dtbs8 dtb8 5

vdtb9 dtbs9 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb9 dtbs9 dtb9 5
```

```
vdtb10 dtbs10 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb10 dtbs10 dtb10 5

vdtb11 dtbs11 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb11 dtbs11 dtb11 5

vdtb12 dtbs12 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb12 dtbs12 dtb12 5

vdtb13 dtbs13 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb13 dtbs13 dtb13 5

vdtb14 dtbs14 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb14 dtbs14 dtb14 5

vdtb15 dtbs15 0 PWL (
+   0.0 1.8

+   150.00e-9 1.8
   )
rsdtb15 dtbs15 dtb15 5
```

```
vwd0 wds0 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
   )
rswd0 wds0 wd0 5

vwd1 wds1 0 PWL (
+    0.0 0.0
+         0.01e-9        0
+         02e-9          0
+         02.02e-9       0.0

+         10e-9          0
+         10.01e-9       0
+         12e-9          0
+         12.02e-9       0.0

+         30e-9          0
+         30.01e-9       1.8
+         32e-9          1.8
+         32.02e-9       0.0

+         40e-9          0
+         40.01e-9       0
+         42e-9          0
+         42.02e-9       0.0

+         70e-9          0
+         70.01e-9       0
+         72e-9          0
+         72.02e-9       0.0

+         80e-9          0
+         80.01e-9       1.8
+         82e-9          1.8
+         82.02e-9       0.0

+    150.00e-9 0.0
   )
rswd1 wds1 wd1 5


vwd2 wds2 0 PWL (
```

```
+   0.0 0.0

+       20e-9           0
+       20.01e-9        0
+       22e-9           0
+       22.02e-9        0.0

+       50e-9           0
+       50.01e-9        0
+       52e-9           0
+       52.02e-9        0.0

+       60e-9           0
+       60.01e-9        1.8
+       62e-9           1.8
+       62.02e-9        0.0

+   150.00e-9 0.0
   )
rswd2 wds2 wd2 5

vwd3 wds3 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rswd3 wds3 wd3 5

vwd4 wds4 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rswd4 wds4 wd4 5

vwd5 wds5 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rswd5 wds5 wd5 5

vwd6 wds6 0 PWL (
+   0.0 0.0
```

```
+    150.00e-9 0.0
   )
rswd6 wds6 wd6 5

vwd7 wds7 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
   )
rswd7 wds7 wd7 5

vwd8 wds8 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
   )
rswd8 wds8 wd8 5

vwd9 wds9 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
   )
rswd9 wds9 wd9 5

vwd10 wds10 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
   )
rswd10 wds10 wd10 5

vwd11 wds11 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
   )
rswd11 wds11 wd11 5

vwd12 wds12 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
```

```
   )
rswd12 wds12 wd12 5

vwd13 wds13 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rswd13 wds13 wd13 5

vwd14 wds14 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rswd14 wds14 wd14 5

vwd15 wds15 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
   )
rswd15 wds15 wd15 5



vdtr0 dtrs0 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr0 dtrs0 dtr0 5

vdtr1 dtrs1 0 PWL (
+   0.0 0.0
+        0.01e-9         1.8
+        02e-9           1.8
+        02.02e-9        0.0

+        07e-9           0
+        07.01e-9        1.8
+        07.81e-9                  1.8
+        07.82e-9        0.0
```

```
+       10e-9       0
+       10.01e-9    1.8
+       12e-9       1.8
+       12.02e-9    0.0

+       17e-9       0
+       17.01e-9    1.8
+       17.81e-9            1.8
+       17.82e-9    0.0

+       30e-9       0
+       30.01e-9    1.8
+       32e-9       1.8
+       32.02e-9    0.0

+       37e-9       0
+       37.01e-9    1.8
+       37.81e-9            1.8
+       37.82e-9    0.0

+       40e-9       0
+       40.01e-9    1.8
+       42e-9       1.8
+       42.02e-9    0.0

+       47e-9       0
+       47.01e-9    1.8
+       47.81e-9            1.8
+       47.82e-9    0.0

+       57e-9       0
+       57.01e-9    1.8
+       57.81e-9            1.8
+       57.82e-9    0.0

+       70e-9       0
+       70.01e-9    1.8
+       72e-9       1.8
+       72.02e-9    0.0

+       77e-9       0
+       77.01e-9    1.8
+       77.81e-9            1.8
+       77.82e-9    0.0
```

```
+       80e-9           0
+       80.01e-9        1.8
+       82e-9           1.8
+       82.02e-9        0.0

+       87e-9           0
+       87.01e-9        1.8
+       87.81e-9                1.8
+       87.82e-9        0.0


+   150.00e-9 0.0
)
rsdtr1 dtrs1 dtr1 5

vdtr2 dtrs2 0 PWL (
+   0.0 0.0

+       20e-9           0
+       20.01e-9        1.8
+       22e-9           1.8
+       22.02e-9        0.0

+       27e-9           0
+       27.01e-9        1.8
+       27.81e-9                1.8
+       27.82e-9        0.0


+       50e-9           0
+       50.01e-9        1.8
+       52e-9           1.8
+       52.02e-9        0.0

+       60e-9           0
+       60.01e-9        1.8
+       62e-9           1.8
+       62.02e-9        0.0

+       67e-9           0
+       67.01e-9        1.8
+       67.81e-9                1.8
+       67.82e-9        0.0
```

```
+   150.00e-9 0.0
)
rsdtr2 dtrs2 dtr2 5

vdtr3 dtrs3 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr3 dtrs3 dtr3 5

vdtr4 dtrs4 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr4 dtrs4 dtr4 5

vdtr5 dtrs5 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr5 dtrs5 dtr5 5

vdtr6 dtrs6 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr6 dtrs6 dtr6 5

vdtr7 dtrs7 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr7 dtrs7 dtr7 5

vdtr8 dtrs8 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
```

```
)
rsdtr8 dtrs8 dtr8 5

vdtr9 dtrs9 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr9 dtrs9 dtr9 5

vdtr10 dtrs10 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr10 dtrs10 dtr10 5

vdtr11 dtrs11 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr11 dtrs11 dtr11 5

vdtr12 dtrs12 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr12 dtrs12 dtr12 5

vdtr13 dtrs13 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr13 dtrs13 dtr13 5

vdtr14 dtrs14 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr14 dtrs14 dtr14 5
```

```
vdtr15 dtrs15 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtr15 dtrs15 dtr15 5


vdtrr0 dtrrs0 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr0 dtrrs0 dtrr0 5

vdtrr1 dtrrs1 0 PWL (
+   0.0 0.0

+       07e-9       0
+       07.01e-9    1.8
+       07.81e-9            1.8
+       07.82e-9    0.0

+       17e-9       0
+       17.01e-9    1.8
+       17.81e-9            1.8
+       17.82e-9    0.0

+       37e-9       0
+       37.01e-9    1.8
+       37.81e-9            1.8
+       37.82e-9    0.0

+       47e-9       0
+       47.01e-9    1.8
+       47.81e-9            1.8
+       47.82e-9    0.0

+       57e-9       0
+       57.01e-9    1.8
+       57.81e-9            1.8
+       57.82e-9    0.0
```

```
+       77e-9           0
+       77.01e-9        1.8
+       77.81e-9                1.8
+       77.82e-9        0.0

+       87e-9           0
+       87.01e-9        1.8
+       87.81e-9                1.8
+       87.82e-9        0.0

+   150.00e-9 0.0
)
rsdtrr1 dtrrs1 dtrr1 5


vdtrr2 dtrrs2 0 PWL (
+   0.0 0.0

+       27e-9           0
+       27.01e-9        1.8
+       27.81e-9                1.8
+       27.82e-9        0.0

+       67e-9           0
+       67.01e-9        1.8
+       67.81e-9                1.8
+       67.82e-9        0.0

+   150.00e-9 0.0
)
rsdtrr2 dtrrs2 dtrr2 5

vdtrr3 dtrrs3 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr3 dtrrs3 dtrr3 5

vdtrr4 dtrrs4 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
```

```
rsdtrr4 dtrrs4 dtrr4 5

vdtrr5 dtrrs5 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr5 dtrrs5 dtrr5 5

vdtrr6 dtrrs6 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr6 dtrrs6 dtrr6 5

vdtrr7 dtrrs7 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr7 dtrrs7 dtrr7 5

vdtrr8 dtrrs8 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr8 dtrrs8 dtrr8 5

vdtrr9 dtrrs9 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr9 dtrrs9 dtrr9 5

vdtrr10 dtrrs10 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr10 dtrrs10 dtrr10 5
```

```
vdtrr11 dtrrs11 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr11 dtrrs11 dtrr11 5

vdtrr12 dtrrs12 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr12 dtrrs12 dtrr12 5

vdtrr13 dtrrs13 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr13 dtrrs13 dtrr13 5

vdtrr14 dtrrs14 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr14 dtrrs14 dtrr14 5

vdtrr15 dtrrs15 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rsdtrr15 dtrrs15 dtrr15 5


vcomb0 combs0 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rscomb0 combs0 comb0 5

vcomb1 combs1 0 PWL (
```

```
+   0.0 0.0
+       0.01e-9         1.8
+       02e-9           1.8
+       02.02e-9        0.0

+       07e-9           0
+       07.01e-9        1.8
+       07.81e-9                1.8
+       07.82e-9        0.0

+       20e-9           0
+       20.01e-9        1.8
+       22e-9           1.8
+       22.02e-9        0.0

+       27e-9           0
+       27.01e-9        1.8
+       27.81e-9                1.8
+       27.82e-9        0.0



+       30e-9           0
+       30.01e-9        1.8
+       32e-9           1.8
+       32.02e-9        0.0

+       37e-9           0
+       37.01e-9        1.8
+       37.81e-9                1.8
+       37.82e-9        0.0

+       50e-9           0
+       50.01e-9        1.8
+       52e-9           1.8
+       52.02e-9        0.0

+       57e-9           0
+       57.01e-9        1.8
+       57.81e-9                1.8
+       57.82e-9        0.0

+       60e-9           0
+       60.01e-9        1.8
```

```
+       62e-9           1.8
+       62.02e-9        0.0

+       67e-9           0
+       67.01e-9        1.8
+       67.81e-9                1.8
+       67.82e-9        0.0

+       70e-9           0
+       70.01e-9        1.8
+       72e-9           1.8
+       72.02e-9        0.0

+       87e-9           0
+       87.01e-9        1.8
+       87.81e-9                1.8
+       87.82e-9        0.0

+   150.00e-9 0.0
)
rscomb1 combs1 comb1 5

vcomb2 combs2 0 PWL (
+   0.0 0.0

+       10e-9           0
+       10.01e-9        1.8
+       12e-9           1.8
+       12.02e-9        0.0

+       17e-9           0
+       17.01e-9        1.8
+       17.81e-9                1.8
+       17.82e-9        0.0

+       40e-9           0
+       40.01e-9        1.8
+       42e-9           1.8
+       42.02e-9        0.0

+       47e-9           0
+       47.01e-9        1.8
+       47.81e-9                1.8
+       47.82e-9        0.0
```

```
+	77e-9		0
+	77.01e-9	1.8
+	77.81e-9			1.8
+	77.82e-9	0.0

+	80e-9		0
+	80.01e-9	1.8
+	82e-9		1.8
+	82.02e-9	0.0

+   150.00e-9 0.0
)
rscomb2 combs2 comb2 5

vcomb3 combs3 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rscomb3 combs3 comb3 5

vcomb4 combs4 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rscomb4 combs4 comb4 5

vcomb5 combs5 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rscomb5 combs5 comb5 5

vcomb6 combs6 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rscomb6 combs6 comb6 5
```

```
vcomb7 combs7 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
)
rscomb7 combs7 comb7 5

vcomb8 combs8 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
)
rscomb8 combs8 comb8 5

vcomb9 combs9 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
)
rscomb9 combs9 comb9 5

vcomb10 combs10 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
)
rscomb10 combs10 comb10 5

vcomb11 combs11 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
)
rscomb11 combs11 comb11 5

vcomb12 combs12 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
)
rscomb12 combs12 comb12 5

vcomb13 combs13 0 PWL (
+    0.0 0.0
```

```
+   150.00e-9 0.0
)
rscomb13 combs13 comb13 5

vcomb14 combs14 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rscomb14 combs14 comb14 5

vcomb15 combs15 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rscomb15 combs15 comb15 5


xsense00 sed0 vdn0 sense
xsense01 sed1 vdn1 sense
xsense02 sed2 vdn2 sense
xsense03 sed3 vdn3 sense
xsense04 sed4 vdn4 sense
xsense05 sed5 vdn5 sense
xsense06 sed6 vdn6 sense
xsense07 sed7 vdn7 sense
xsense08 sed8 vdn8 sense
xsense09 sed9 vdn9 sense
xsense10 sed10 vdn10 sense
xsense11 sed11 vdn11 sense
xsense12 sed12 vdn12 sense
xsense13 sed13 vdn13 sense
xsense14 sed14 vdn14 sense
xsense15 sed15 vdn15 sense


mnse0 d0 dtrr0 sed0 0 nenh w=4u l=.4u
mnse1 d1 dtrr1 sed1 0 nenh w=4u l=.4u
mnse2 d2 dtrr2 sed2 0 nenh w=4u l=.4u
mnse3 d3 dtrr3 sed3 0 nenh w=4u l=.4u
mnse4 d4 dtrr4 sed4 0 nenh w=4u l=.4u
mnse5 d5 dtrr5 sed5 0 nenh w=4u l=.4u
```

```
mnse6 d6 dtrr6 sed6 0 nenh w=4u l=.4u
mnse7 d7 dtrr7 sed7 0 nenh w=4u l=.4u
mnse8 d8 dtrr8 sed8 0 nenh w=4u l=.4u
mnse9 d9 dtrr9 sed9 0 nenh w=4u l=.4u
mnse10 d10 dtrr10 sed10 0 nenh w=4u l=.4u
mnse11 d11 dtrr11 sed11 0 nenh w=4u l=.4u
mnse12 d12 dtrr12 sed12 0 nenh w=4u l=.4u
mnse13 d13 dtrr13 sed13 0 nenh w=4u l=.4u
mnse14 d14 dtrr14 sed14 0 nenh w=4u l=.4u
mnse15 d15 dtrr15 sed15 0 nenh w=4u l=.4u


.SUBCKT sense 2 8
*************in*out
* Input Signals
*VIN 2 0 DC 0V

VOS 1 0 DC .48V

* Power Supplies
VDD 3 0 DC 1.8VOLT
VSS 4 0 DC 0VOLT

* Netlist for CMOS Comparator in Nwell
M1 5 1 7 7 penh W=15U L=.2U
M2 6 2 7 7 penh W=15U L=.2U
M3 5 5 4 4 nenh W=5.4U L=.2U
M4 6 5 4 4 nenh W=5.4U L=.2U
M5 7 9 3 3 penh W=30U L=.2U
M6 8 6 4 4 nenh W=21.6U L=.2U
M7 8 9 3 3 penh W=60U L=.2U
M8 9 9 3 3 penh W=60U L=.2U

* External Components
CL 8 0 .001fF
RB 9 0 0.20K
.ends sense


mndum0 d0 dum0 dumr0 0 nenh w=4u l=.4u
mndum1 d1 dum1 dumr1 0 nenh w=4u l=.4u
mndum2 d2 dum2 dumr2 0 nenh w=4u l=.4u
mndum3 d3 dum3 dumr3 0 nenh w=4u l=.4u
mndum4 d4 dum4 dumr4 0 nenh w=4u l=.4u
```

```
mndum5 d5 dum5 dumr5 0 nenh w=4u l=.4u
mndum6 d6 dum6 dumr6 0 nenh w=4u l=.4u
mndum7 d7 dum7 dumr7 0 nenh w=4u l=.4u
mndum8 d8 dum8 dumr8 0 nenh w=4u l=.4u
mndum9 d9 dum9 dumr9 0 nenh w=4u l=.4u
mndum10 d10 dum10 dumr10 0 nenh w=4u l=.4u
mndum11 d11 dum11 dumr11 0 nenh w=4u l=.4u
mndum12 d12 dum12 dumr12 0 nenh w=4u l=.4u
mndum13 d13 dum13 dumr13 0 nenh w=4u l=.4u
mndum14 d14 dum14 dumr14 0 nenh w=4u l=.4u
mndum15 d15 dum15 dumr15 0 nenh w=4u l=.4u

rdum0 dumr0 0 .10k
rdum1 dumr1 0 .10k
rdum2 dumr2 0 .10k
rdum3 dumr3 0 .10k
rdum4 dumr4 0 .10k
rdum5 dumr5 0 .10k
rdum6 dumr6 0 .10k
rdum7 dumr7 0 .10k
rdum8 dumr8 0 .10k
rdum9 dumr9 0 .10k
rdum10 dumr10 0 .10k
rdum11 dumr11 0 .10k
rdum12 dumr12 0 .10k
rdum13 dumr13 0 .10k
rdum14 dumr14 0 .10k
rdum15 dumr15 0 .10k


vdum0 dumrs0 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rdumrs0 dumrs0 dum0 5

vdum1 dumrs1 0 PWL (
+   0.0 0.0

+       05e-9       0
+       05.01e-9    1.8
+       05.3e-9             1.8
+       05.32e-9    0.0
```

```
+       15e-9           0
+       15.01e-9        1.8
+       15.3e-9                 1.8
+       15.32e-9        0.0

+       35e-9           0
+       35.01e-9        1.8
+       35.3e-9                 1.8
+       35.32e-9        0.0

+       45e-9           0
+       45.01e-9        1.8
+       45.3e-9                 1.8
+       45.32e-9        0.0

+       55e-9           0
+       55.01e-9        1.8
+       55.3e-9                 1.8
+       55.32e-9        0.0

+       75e-9           0
+       75.01e-9        1.8
+       75.3e-9                 1.8
+       75.32e-9        0.0

+       85e-9           0
+       85.01e-9        1.8
+       85.3e-9                 1.8
+       85.32e-9        0.0

+   150.00e-9 0.0
)
rdumrs1 dumrs1 dum1 5

vdum2 dumrs2 0 PWL (
+   0.0 0.0


+       25e-9           0
+       25.01e-9        1.8
+       25.3e-9                 1.8
+       25.32e-9        0.0
```

```
+	65e-9		0
+	65.01e-9	1.8
+	65.3e-9			1.8
+	65.32e-9	0.0


+	150.00e-9 0.0
)
rdumrs2 dumrs2 dum2 5

vdum3 dumrs3 0 PWL (
+	0.0 0.0

+	150.00e-9 0.0
)
rdumrs3 dumrs3 dum3 5

vdum4 dumrs4 0 PWL (
+	0.0 0.0

+	150.00e-9 0.0
)
rdumrs4 dumrs4 dum4 5

vdum5 dumrs5 0 PWL (
+	0.0 0.0

+	150.00e-9 0.0
)
rdumrs5 dumrs5 dum5 5

vdum6 dumrs6 0 PWL (
+	0.0 0.0

+	150.00e-9 0.0
)
rdumrs6 dumrs6 dum6 5

vdum7 dumrs7 0 PWL (
+	0.0 0.0

+	150.00e-9 0.0
)
```

```
rdumrs7 dumrs7 dum7 5

vdum8 dumrs8 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rdumrs8 dumrs8 dum8 5

vdum9 dumrs9 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rdumrs9 dumrs9 dum9 5

vdum10 dumrs10 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rdumrs10 dumrs10 dum10 5

vdum11 dumrs11 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rdumrs11 dumrs11 dum11 5

vdum12 dumrs12 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rdumrs12 dumrs12 dum12 5

vdum13 dumrs13 0 PWL (
+   0.0 0.0

+   150.00e-9 0.0
)
rdumrs13 dumrs13 dum13 5
```

```
vdum14 dumrs14 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
)
rdumrs14 dumrs14 dum14 5

vdum15 dumrs15 0 PWL (
+    0.0 0.0

+    150.00e-9 0.0
)
rdumrs15 dumrs15 dum15 5


rrd0p rd0 0 10000k
rrd1p rd1 0 10000k
rrd2p rd2 0 10000k
rrd3p rd3 0 10000k
rrd4p rd4 0 10000k
rrd5p rd5 0 10000k
rrd6p rd6 0 10000k
rrd7p rd7 0 10000k
rrd8p rd8 0 10000k
rrd9p rd9 0 10000k
rrd10p rd10 0 10000k
rrd11p rd11 0 10000k
rrd12p rd12 0 10000k
rrd13p rd13 0 10000k
rrd14p rd14 0 10000k
rrd15p rd15 0 10000k


rdt0p dt0 0 10000k
rdt1p dt1 0 10000k
rdt2p dt2 0 10000k
rdt3p dt3 0 10000k
rdt4p dt4 0 10000k
rdt5p dt5 0 10000k
rdt6p dt6 0 10000k
rdt7p dt7 0 10000k
rdt8p dt8 0 10000k
rdt9p dt9 0 10000k
rdt10p dt10 0 10000k
```

```
rdt11p dt11 0 10000k
rdt12p dt12 0 10000k
rdt13p dt13 0 10000k
rdt14p dt14 0 10000k
rdt15p dt15 0 10000k


rdtb0p dtb0 0 10000k
rdtb1p dtb1 0 10000k
rdtb2p dtb2 0 10000k
rdtb3p dtb3 0 10000k
rdtb4p dtb4 0 10000k
rdtb5p dtb5 0 10000k
rdtb6p dtb6 0 10000k
rdtb7p dtb7 0 10000k
rdtb8p dtb8 0 10000k
rdtb9p dtb9 0 10000k
rdtb10p dtb10 0 10000k
rdtb11p dtb12 0 10000k
rdtb12p dtb12 0 10000k
rdtb13p dtb13 0 10000k
rdtb14p dtb14 0 10000k
rdtb15p dtb15 0 10000k


rdtr0p dtr0 0 10000k
rdtr1p dtr1 0 10000k
rdtr2p dtr2 0 10000k
rdtr3p dtr3 0 10000k
rdtr4p dtr4 0 10000k
rdtr5p dtr5 0 10000k
rdtr6p dtr6 0 10000k
rdtr7p dtr7 0 10000k
rdtr8p dtr8 0 10000k
rdtr9p dtr9 0 10000k
rdtr10p dtr10 0 10000k
rdtr11p dtr11 0 10000k
rdtr12p dtr12 0 10000k
rdtr13p dtr13 0 10000k
rdtr14p dtr14 0 10000k
rdtr15p dtr15 0 10000k


rdtrr0p dtrr0 0 10000k
```

rdtrr1p dtrr1 0 10000k
rdtrr2p dtrr2 0 10000k
rdtrr3p dtrr3 0 10000k
rdtrr4p dtrr4 0 10000k
rdtrr5p dtrr5 0 10000k
rdtrr6p dtrr6 0 10000k
rdtrr7p dtrr7 0 10000k
rdtrr8p dtrr8 0 10000k
rdtrr9p dtrr9 0 10000k
rdtrr10p dtrr10 0 10000k
rdtrr11p dtrr11 0 10000k
rdtrr12p dtrr12 0 10000k
rdtrr13p dtrr13 0 10000k
rdtrr14p dtrr14 0 10000k
rdtrr15p dtrr15 0 10000k

rcomb0p comb0 0 10000k
rcomb1p comb1 0 10000k
rcomb2p comb2 0 10000k
rcomb3p comb3 0 10000k
rcomb4p comb4 0 10000k
rcomb5p comb5 0 10000k
rcomb6p comb6 0 10000k
rcomb7p comb7 0 10000k
rcomb8p comb8 0 10000k
rcomb9p comb9 0 10000k
rcomb10p comb10 0 10000k
rcomb11p comb11 0 10000k
rcomb12p comb12 0 10000k
rcomb13p comb13 0 10000k
rcomb14p comb14 0 10000k
rcomb15p comb15 0 10000k

rdum0p dum0 0 10000k
rdum1p dum1 0 10000k
rdum2p dum2 0 10000k
rdum3p dum3 0 10000k
rdum4p dum4 0 10000k
rdum5p dum5 0 10000k
rdum6p dum6 0 10000k
rdum7p dum7 0 10000k
rdum8p dum8 0 10000k

```
rdum9p dum9 0 10000k
rdum10p dum10 0 10000k
rdum11p dum11 0 10000k
rdum12p dum12 0 10000k
rdum13p dum13 0 10000k
rdum14p dum14 0 10000k
rdum15p dum15 0 10000k


mn0 wd0 dt0 d0 0 nenh w=4u l=.4u
mn1 wd1 dt1 d1 0 nenh w=4u l=.4u
mn2 wd2 dt2 d2 0 nenh w=4u l=.4u
mn3 wd3 dt3 d3 0 nenh w=4u l=.4u
mn4 wd4 dt4 d4 0 nenh w=4u l=.4u
mn5 wd5 dt5 d5 0 nenh w=4u l=.4u
mn6 wd6 dt6 d6 0 nenh w=4u l=.4u
mn7 wd7 dt7 d7 0 nenh w=4u l=.4u
mn8 wd8 dt8 d8 0 nenh w=4u l=.4u
mn9 wd9 dt9 d9 0 nenh w=4u l=.4u
mn10 wd10 dt10 d10 0 nenh w=4u l=.4u
mn11 wd11 dt11 d11 0 nenh w=4u l=.4u
mn12 wd12 dt12 d12 0 nenh w=4u l=.4u
mn13 wd13 dt13 d13 0 nenh w=4u l=.4u
mn14 wd14 dt14 d14 0 nenh w=4u l=.4u
mn15 wd15 dt15 d15 0 nenh w=4u l=.4u

mp0 d0 dtb0 wd0 3 penh w=8u l=.4u
mp1 d1 dtb1 wd1 3 penh w=8u l=.4u
mp2 d2 dtb2 wd2 3 penh w=8u l=.4u
mp3 d3 dtb3 wd3 3 penh w=8u l=.4u
mp4 d4 dtb4 wd4 3 penh w=8u l=.4u
mp5 d5 dtb5 wd5 3 penh w=8u l=.4u
mp6 d6 dtb6 wd6 3 penh w=8u l=.4u
mp7 d7 dtb7 wd7 3 penh w=8u l=.4u
mp8 d8 dtb8 wd8 3 penh w=8u l=.4u
mp9 d9 dtb9 wd9 3 penh w=8u l=.4u
mp10 d10 dtb10 wd10 3 penh w=8u l=.4u
mp11 d11 dtb11 wd11 3 penh w=8u l=.4u
mp12 d12 dtb12 wd12 3 penh w=8u l=.4u
mp13 d13 dtb13 wd13 3 penh w=8u l=.4u
mp14 d14 dtb14 wd14 3 penh w=8u l=.4u

mp15 d15 dtb15 wd15 3 penh w=8u l=.4u
```

```
mdtr0s P2 dtr0 v2d0 0 nenh w=4u l=.4u
mdtr1s P2 dtr1 v2d1 0 nenh w=4u l=.4u
mdtr2s P2 dtr2 v2d2 0 nenh w=4u l=.4u
mdtr3s P2 dtr3 v2d3 0 nenh w=4u l=.4u
mdtr4s P2 dtr4 v2d4 0 nenh w=4u l=.4u
mdtr5s P2 dtr5 v2d5 0 nenh w=4u l=.4u
mdtr6s P2 dtr6 v2d6 0 nenh w=4u l=.4u
mdtr7s P2 dtr7 v2d7 0 nenh w=4u l=.4u
mdtr8s P2 dtr8 v2d8 0 nenh w=4u l=.4u
mdtr9s P2 dtr9 v2d9 0 nenh w=4u l=.4u
mdtr10s P2 dtr10 v2d10 0 nenh w=4u l=.4u
mdtr11s P2 dtr11 v2d11 0 nenh w=4u l=.4u
mdtr12s P2 dtr12 v2d12 0 nenh w=4u l=.4u
mdtr13s P2 dtr13 v2d13 0 nenh w=4u l=.4u
mdtr14s P2 dtr14 v2d14 0 nenh w=4u l=.4u
mdtr15s P2 dtr15 v2d15 0 nenh w=4u l=.4u

mdtrr0s P1 dtrr0 Vdd0 0 nenh w=4u l=.4u
mdtrr1s P1 dtrr1 Vdd1 0 nenh w=4u l=.4u
mdtrr2s P1 dtrr2 Vdd2 0 nenh w=4u l=.4u
mdtrr3s P1 dtrr3 Vdd3 0 nenh w=4u l=.4u
mdtrr4s P1 dtrr4 Vdd4 0 nenh w=4u l=.4u
mdtrr5s P1 dtrr5 Vdd5 0 nenh w=4u l=.4u
mdtrr6s P1 dtrr6 Vdd6 0 nenh w=4u l=.4u
mdtrr7s P1 dtrr7 Vdd7 0 nenh w=4u l=.4u
mdtrr8s P1 dtrr8 Vdd8 0 nenh w=4u l=.4u
mdtrr9s P1 dtrr9 Vdd9 0 nenh w=4u l=.4u
mdtrr10s P1 dtrr10 Vdd10 0 nenh w=4u l=.4u
mdtrr11s P1 dtrr11 Vdd11 0 nenh w=4u l=.4u
mdtrr12s P1 dtrr12 Vdd12 0 nenh w=4u l=.4u
mdtrr13s P1 dtrr13 Vdd13 0 nenh w=4u l=.4u
mdtrr14s P1 dtrr14 Vdd14 0 nenh w=4u l=.4u
mdtrr15s P1 dtrr15 Vdd15 0 nenh w=4u l=.4u


.SUBCKT sram rd comb d v2d Vdd

mrd d rd 2 0 nenh w=4u l=.4u
mcomb 1 comb d 0 nenh w=4u l=.4u

xmem1 v2d 1 memristor
xmem2 Vdd 2 memristor2

.ENDS sram
```

```
.SUBCKT memristor Plus Minus PARAMS:
+ Ron=500 Roff=5K Rinit=1k D=3N uv=100n p=3
*********************************************
* DIFFERENTIAL EQUATION MODELING  *
********************************************
Gx 0 x value={ I(Emem)*uv*Ron/D^2*f(V(x),I(Emem),p)}
Cx x 0 1 IC={(Roff-Rinit)/(Roff-Ron)}
Raux x 0 1T
* RESISTIVE PORT OF THE MEMRISTOR *
******************************
Emem plus aux value={-I(Emem)*V(x)*(Roff-Ron)}
Roff aux minus {Roff}
*********************************************

* WINDOW FUNCTIONS
* FOR NONLINEAR DRIFT MODELING *
*********************************************
*window function, according to Joglekar
;.func f(x,p)={1-(2*x-1)^(2*p)}
*proposed window function
.func f(x,i,p)={1-(x-stp(-i))^(2*p)}
.ENDS memristor

.SUBCKT memristor2 Plus Minus PARAMS:
+ Ron=3.8k Roff=5K Rinit=4k D=3N uv=100n p=7
*********************************************
* DIFFERENTIAL EQUATION MODELING  *
********************************************
Gx 0 x value={ I(Emem)*uv*Ron/D^2*f(V(x),I(Emem),p)}
Cx x 0 1 IC={(Roff-Rinit)/(Roff-Ron)}
Raux x 0 1T
* RESISTIVE PORT OF THE MEMRISTOR *
******************************
Emem plus aux value={-I(Emem)*V(x)*(Roff-Ron)}
Roff aux minus {Roff}
*********************************************

* WINDOW FUNCTIONS
* FOR NONLINEAR DRIFT MODELING *
*********************************************
*window function, according to Joglekar
;.func f(x,p)={1-(2*x-1)^(2*p)}
*proposed window function
```

```
.func f(x,i,p)={1-(x-stp(-i))^(2*p)}
.ENDS memristor2


.MODEL nenh NMOS LEVEL=7 VERSION=3.1 TNOM=27 tox=4.1E-9 XJ=1E-7 NCH=2.3549E17
+VTH0=0.3662473 K1=0.5864999 K2=1.127266E-3 K3=1E-3
+K3B=0.0294061 W0=1E-7 NLX=1.630684E-7 DVT0W=0 DVT1W=0 DVT2W=0
DVT0=1.2064649
+DVT1=0.4215486 DVT2=0.0197749 U0=273.8094484 UA=-1.40499E-9
+UB=2.408323E-18 UC=6.504826E-11 VSAT=1.355009E5 A0=2 AGS=0.4449958
+B0=1.901075E-7 B1=4.99995E-6 KETA=-0.0164863 A1=3.868769E-4 A2=0.4640272
+RDSW=123.3376355 PRWG=0.5 PRWB=-0.197728 WR=1 WINT=0 LINT=1.690044E-8
+XL=0 XW=-1E-8 DWG=-4.728719E-9 DWB=-2.452411E-9 VOFF=-0.0948017
NFACTOR=2.1860065
+CIT=0 CDSC=2.4E-4 CDSCD=0 CDSCB=0 ETA0=2.230928E-3 ETAB=6.028975E-5
DSUB=0.0145467
+PCLM=1.3822069 PDIBLC1=0.1762787 PDIBLC2 = 1.66653E-3 PDIBLCB = -0.1
+DROUT=0.7694691 PSCBE1=8.91287E9 PSCBE2=7.349607E-9 PVAG=1.685917E-3
+DELTA=0.01 RSH=6.7 MOBMOD=1 PRT=0 UTE=-1.5 KT1=-0.11 KT1L=0 KT2=0.022
UA1=4.31E-9
+UB1=-7.61E-18 UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1 WWL=0 LL=0 LLN=1
LW=0
+LWN=1 LWL=0 CAPMOD=2 XPART=0.5 CGDO=8.23E-10 CGSO=8.23E-10 CGBO=1E-12

+CJ     = 9.466429E-4    PB     = 0.8          MJ     = 0.3820266

+CJSW    = 2.608154E-10   PBSW    = 0.8          MJSW    = 0.102322

+CJSWG   = 3.3E-10       PBSWG   = 0.8          MJSWG   = 0.102322

+CF      = 0             PVTH0   = -2.199373E-3   PRDSW   = -0.9368961

+PK2     = 1.593254E-3    WKETA   = -2.880976E-3   LKETA   = 7.165078E-3

+PU0     = 6.777519       PUA     = 5.505418E-12   PUB     = 8.84133E-25

+PVSAT   = 2.006286E3     PETA0   = 1.003159E-4    PKETA   = -6.759277E-3

+NOIMOD=2.0E+00               NOIA=1.3182567385564E+19

+NOIB=144543.977074592 NOIC=-1.24515784572817E-12 EF=0.92 EM=41000000
```

```
.MODEL penh PMOS LEVEL=7 VERSION = 3.1          TNOM    = 27            tox     = 4.1E-9
+XJ      = 1E-7          NCH     = 4.1589E17      VTH0    = -0.3906012
+K1      = 0.5341312      K2      = 0.0395326      K3      = 0
+K3B     = 7.4916211      W0      = 1E-6           NLX     = 1.194072E-7
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.5060555      DVT1    = 0.2423835      DVT2    = 0.1
+U0      = 115.6894042    UA      = 1.573746E-9    UB      = 1.874308E-21
+UC      = -1E-10         VSAT    = 1.130982E5     A0      = 1.9976555
+AGS     = 0.4186945      B0      = 1.949178E-7    B1      = 6.422908E-7
+KETA    = 0.0166345      A1      = 0.4749146      A2      = 0.300003
+RDSW    = 198.321294     PRWG    = 0.5           PRWB    = -0.4986647
+WR      = 1             WINT    = 0             LINT    = 2.94454E-8
+XL      = 0             XW      = -1E-8          DWG     = -2.798724E-8
+DWB     = -4.83797E-10   VOFF    = -0.095236      NFACTOR = 2
+CIT     = 0             CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0             ETA0    = 1.035504E-3    ETAB    = -4.358398E-4
+DSUB    = 1.816555E-3    PCLM    = 1.3299898      PDIBLC1 = 1.766563E-3
+PDIBLC2 = 7.728395E-7    PDIBLCB = -1E-3          DROUT   = 1.011891E-3
+PSCBE1  = 4.872184E10    PSCBE2  = 5E-10          PVAG    = 0.0209921
+DELTA   = 0.01           RSH     = 7.7            MOBMOD  = 1
+PRT     = 0             UTE     = -1.5           KT1     = -0.11
+KT1L    = 0             KT2     = 0.022          UA1     = 4.31E-9
```

```
+UB1    = -7.61E-18    UC1    = -5.6E-11     AT     = 3.3E4

+WL     = 0            WLN    = 1            WW     = 0

+WWN    = 1            WWL    = 0            LL     = 0

+LLN    = 1            LW     = 0            LWN    = 1

+LWL    = 0            CAPMOD  = 2           XPART   = 0.5

+CGDO   = 6.35E-10     CGSO   = 6.35E-10     CGBO   = 1E-12

+CJ     = 1.144521E-3  PB     = 0.8468686    MJ     = 0.4099522

+CJSW   = 2.490749E-10  PBSW   = 0.8769118   MJSW   = 0.3478565

+CJSWG  = 4.22E-10     PBSWG  = 0.8769118    MJSWG  = 0.3478565

+CF     = 0            PVTH0  = 2.302018E-3  PRDSW  = 9.0575312

+PK2    = 1.821914E-3  WKETA  = 0.0222457    LKETA  = -1.495872E-3

+PU0    = -1.5580645   PUA    = -6.36889E-11  PUB    = 1E-21

+PVSAT  = 49.8420442   PETA0  = 2.827793E-5  PKETA  = -2.536564E-3

+NOIMOD=2.0E+00        NOIA=3.57456993317604E+18        NOIB=2500

+NOIC=2.61260020285845E-11     EF=1.1388                EM=41000000

*(V(v2d0)- V(xsram0.1))/ I(xsram0.xmem1:1)

.options stepgmin
.tran .2n 90ns
.probe
.end
```

APPENDIX B

MEMRISTOR MODELING IN MATLAB

```
%linear drift model of memristor with sinwave

%it shows i-v characteristic of a memristor
clc;
clear all;
close all;

% params
Ron=100;
Roff=16000;
delR=Roff-Ron;
L=10e-9;
w0 =1e-9;
mu = 10e-14;
Q0=L^2/(mu*Ron);
eta = 1;

%% finding w(t)
f=5;
tval=0:1/(1000*f):1/f;
options=odeset('RelTol',1e-7,'AbsTol',1e-7);
[t,w]=ode45('memristor',tval,w0,options);
Mt=Roff-w'.*delR/L;
vt=sin(2*pi*f*t);
it=vt'./Mt;

plot(it,vt');
xlabel('i(Amp)');
ylabel('V(volt)');
-----------------------------------------------------------------------------------------------------------------------------------
function dwdt= memristor(t,w)

  Ron=100;
  Roff=16000;
  delR=Roff-Ron;
  L=10e-9;
  mu = 10e-14;
  f = 5;
  omega0 = 2*pi*f;
  dwdt=(mu*Ron/L)*(sin(omega0*t)/(Roff-delR*w/L));

end
```

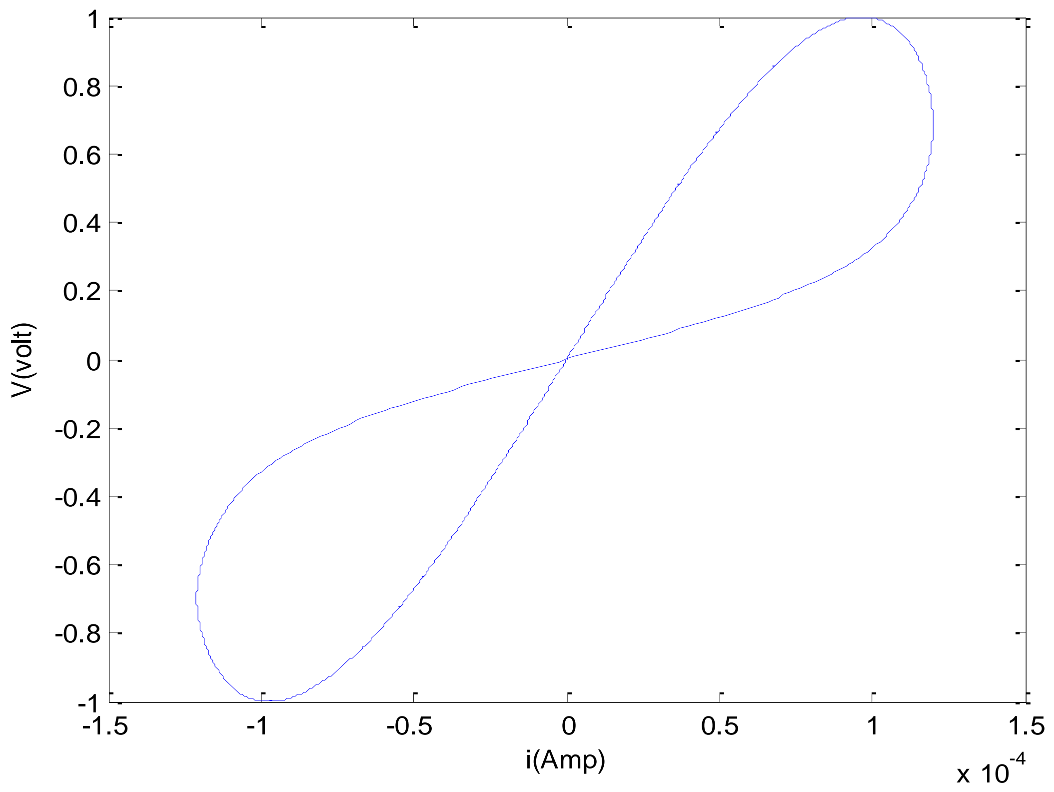


Figure B.1: i-V Characteristic of memristor

APPENDIX C

EXPORTING DATA FROM PSPICE TO MATLAB

1. Click on the plot window.
2. Go to Edit -> Select all.
3. Edit -> Copy.
4. Open Microsoft Excel.
5. Select row1, column 1.
6. Click paste or press Ctrl+V.
7. Value of independent and dependent variables are pasted in every column.
8. Select whole column without variable name and copy it.
9. Paste it to make a MATLAB variable.
10. These data can be plotted in MATLAB then.

1	Time	V(wr0)	V(rd0)
2	0	0	0
3	3.20E-11	4.68E-17	4.16E-17
4	6.40E-11	4.83E-17	4.27E-17
5	1.28E-10	3.86E-17	3.27E-17
6	2.56E-10	4.47E-17	3.78E-17
7	5.12E-10	4.47E-17	3.46E-17
8	1.02E-09	5.21E-17	3.70E-17
9	2.05E-09	6.21E-17	3.81E-17
10	4.10E-09	7.82E-17	4.13E-17
11	7.30E-09	9.60E-17	4.42E-17
12	9.00E-09	1.21E-16	4.77E-17

Figure C.1: Exporting data from pSPICE to matlab

APPENDIX D

SPICE CONVERGENCE PROBLEM ELIMINATION TECHNIQUES

SPICE is an important tool that is heavily used when designing analog electronic circuits. SPICE allows new designs to be evaluated quickly and at considerably less expense than the only other alternative, fabrication. However, even though SPICE has been heavily used for a long time now, getting it to converge and give an accurate answer is still considered an art. Considerable knowledge is needed to use SPICE successfully; however, much of it is based on particular situations or on tricks that are based largely on luck.

The answer to a nonlinear problem, such as those in the SPICE DC and Transient analyses, is found via an iterative solution. For example, SPICE makes an initial guess at the circuit's node voltages and then, using the circuit conductances, calculates the mesh currents. The currents are then used to recalculate the node voltages, and the cycle begins again. This continues until all the node voltages settle to values which are within specific tolerance limits. These limits can be altered using various *.Options* parameters such as Reltol, Vntol, and Abstol.

If the node voltages do not settle down within a certain number of iterations, the DC analysis will issue an error message such as "No convergence in DC analysis", "Singular Matrix", or "Gmin/Source Stepping Failed". SPICE will then terminate the run because both the AC and transient analyses require an initial stable operating point in order to proceed. During the transient analysis, this iterative process is repeated for each individual time step. If the node voltages do not settle down, the time step is reduced and SPICE tries again to determine the node voltages. If the time step is reduced beyond a specific fraction of the total analysis time, the transient analysis will issue the error message, "Time step too small," and the analysis will be halted.

Problems come in all shapes, sizes, and disguises, but convergence problems are usually related to one of the following:

- Circuit Topology
- Device Modeling
- Simulator Setup

The DC analysis may fail to converge because of incorrect initial voltage estimates, model discontinuities, unstable/bistable operation, or unrealistic circuit impedances. Transient analysis failures are usually due to model discontinuities or unrealistic circuit, source, or parasitic modeling. The various solutions to convergence problems fall under one of two types. Some are simply band-aids which merely attempt to fix the symptom by adjusting the simulator options. Other solutions actually affect the true cause of the convergence problems.

There are two strategies used to circumvent convergence problems in the transient analysis: reduce the effect of discontinuities in the nonlinear capacitors and eliminate discontinuous jumps in the solution. There steps can be followed to achieve that:

1. For each voltage source used, a small source resistance should be incorporated with it. Also, each MOSFET should have a shunt resistance and a capacitance to account for its gate impedance.

2. When specifying the nonlinear device model parameters, a complete capacitance model should be given. Simplified device models that do not have capacitances should not be used.

3. The source and drain areas for all MOSFETS should be given. This results in the junction capacitors being modeled. Also, all overlap capacitances should be given.

4. If, by a process of elimination, a nonlinear capacitance that seems to have a discontinuity can be identified, the nonlinear capacitor model should be simplified/modified. This can sometimes eliminate the discontinuity.

5. A small linear capacitor can be connected from every node to ground.

6. If all else fails, the RELTOL, ABSTOL, VNTOL parameters should be loosened and the transitions in the stimulus waveforms should be widened. This can sometimes cause the simulator to just jump past the convergence difficulties.

Received February 3, 2013, accepted April 14, 2013, published May 10, 2013.

Digital Object Identifier 10.1109/ACCESS.2013.2259891

Memristor-Based Nonvolatile Random Access Memory: Hybrid Architecture for Low Power Compact Memory Design

SYED SHAKIB SARWAR, SYED AN NAZMUS SAQUEB, FARHAN QUAIYUM (Student Member, IEEE), AND A. B. M. HARUN-UR RASHID (Senior Member, IEEE)

Department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, Dhaka 1000, Bangladesh.

Corresponding author: S. S. Sarwar (syed.shakib@ieee.org)

This work was supported by the Ministry of Science and Technology, Government of Bangladesh, under the Science and Technology Special Research Grant for 2012–2013.

ABSTRACT In this paper, a new approach toward the design of a memristor based nonvolatile static random-access memory (SRAM) cell using a combination of memristor and metal-oxide semiconductor devices is proposed. Memristor and MOSFETs of the Taiwan Semiconductor Manufacturing Company's 180-nm technology are used to form a single cell. The predicted area of this cell is significantly less and the average read–write power is ∼25 times less than a conventional 6-T SRAM cell of the same complementary metal-oxide semiconductor technology. Read time is much less than the 6-T SRAM cell. However, write time is a bit higher, and can be improved by increasing the mobility of the memristor. The nonvolatile characteristic of the cell makes it attractive for nonvolatile random access memory design.

INDEX TERMS CMOS, memory element, memristor (M), NVRAM, SPICE model.

I. INTRODUCTION

Chua [1] hypothesized the existence of a fourth passive two-terminal circuit element called the memristor in 1971 (the other three elements being the resistor, capacitor and inductor). In 2008, researchers at Hewlett Packard (HP) Labs reported that the memristor was realized physically using two-terminal titanium-di-oxide (TiO_2) nanoscale device [2]. HP Labs described the first experimental demonstration of a physical memristor, finally confirming Chua's theory and sparking much excitement in the electronics and business circles [3]. Basically the memristor is a resistance with memory; when a voltage is applied to this element, its resistance changes and remains on that particular value when the source is removed. The main difference between the memristor (M) and the three traditional circuit elements (R, L, C) is its nonlinear input-output characteristics.

The HP memristor exploits certain nanoscale properties of a titanium-di-oxide TiO_2 thin film. Other physical embodiments of memristors may also be possible and it has been recently proposed that coupling of current flow and spin transport at nanoscale dimensions can be used to realize memristance [4], [5]. Analog circuit applications incorporating the memristor are rapidly emerging in the literature. Witrisal considered Memristors in an ultra-wideband receiver to reduce signal processing power [6]. Memristors are also used as programmable resistive loads in a differential amplifier [7]. Varghese and Gandi used memristor as a source degeneration element in a complementary metal-oxide semiconductor (CMOS) differential pair [8]. Reference [9] shows a variety of programmable analog functional blocks based on analog memristor memory including an Op-Amp based variable gain amplifier (VGA). Pulse-programming methods for memristive analog memory in a differential pair amplifier are considered in [10].

Memristors have been studied intensively among many researchers because of their possibilities, especially as a strong candidate for future memories [11]. Non-volatile property and high packing density in a crossbar array particularly excites the researchers. The main feature of our proposed circuit is its non-volatility. The data is stored in the memory even when the power is turned off for an indefinite time. Another feature is its reduced size compared to the conventional 6T-SRAM. As only three transistors are used in each

 2169-3536/$31.00 © 2013 IEEE

cell of the proposed circuit, its area can be much less than the conventional SRAM cells. The power consumed by the proposed structure is significantly less than the conventional SRAM structure. All these features are discussed further later on in this paper.

The paper starts off with the introduction of memristors and its characteristics. After that some related works were discussed. Then it goes straight into the structure of our proposed circuit, its working principle and its functionality, then it discusses the perspectives, draws some comparisons, and finally it concludes with the possible future prospects of the circuit.

II. MEMRISTOR AS A MEMORY ELEMENT

Strukov *et al.* [2] presented a physical model of the memristor. They have shown that the memristor can be characterized by an equivalent time-dependent resistor whose value at a time t is linearly proportional to the quantity of charge q that has passed through it. They realized a proof-of-concept memristor, which consists of a thin nanolayer (2 nm) of TiO_2 and a second oxygen deficient nanolayer of TiO_{2-x} (8 nm) sandwiched between two Pt nanowires. Oxygen (O_2^-) vacancies are +2 mobile carriers and are positively charged. A change in distribution of O_2^- within the TiO_2 nanolayer changes the resistance. By applying a positive voltage, to the top platinum nanowire, oxygen vacancies drift from the TiO_{2-x} layer to the TiO_2 undoped layer, thus changing the boundary between the TiO_{2-x} and TiO_2 layers. As a consequence, the overall resistance of the layer is reduced corresponding to an "ON" state. When enough charge passes through the memristor that ions can no longer move, the device enters a hysteresis region and keeps q at an upper bound with fixed memristance, M (memristor resistance). By reversing the process, the

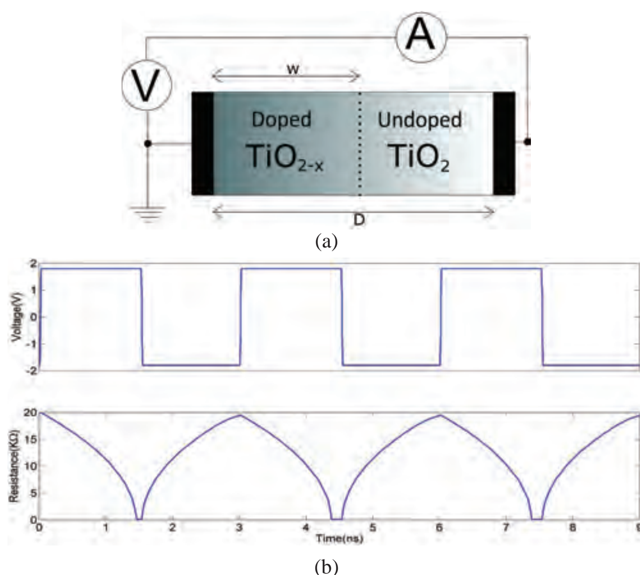


FIGURE 1. (a) Characterizing the memristor and (b) change of resistance when a 3.6 V p–p square wave is applied.

oxygen defects diffuse back into the TiO_{2-x} nanolayer. The resistance returns to its original state, which corresponds to an "OFF" state. The significant aspect to be noted here is that only ionic charges, namely oxygen vacancies (O_2^-) through the cell, change memristance. The resistance change is non-volatile hence the cell acts as a memory element. Fig. 1(a) shows the doped and undoped region of a memristor. If a voltage is applied across the memristor

$$v(t) = M(t)i(t) \text{ [2]} \tag{1}$$

$$M(t) = R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right) \tag{2}$$

where R_{ON} is the resistance of completely doped memristor and R_{OFF} is the resistance of completely undoped memristor, w(t) is given by

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{ON}}{D} i(t) \tag{3}$$

μ_v is the average dopant mobility and D is the length of the memrsitor. To consider the nonlinearity produced from the edge of the thin film, a window function [2], [12], [13] should be multiplied to the right side of (3).

$$f\left(\frac{w(t)}{D}\right) = 1 - \left(2\frac{w(t)}{D} - 1\right)^{2p}. \tag{4}$$

The spice model [13] which makes use of non-linear dopant drift in modelling is used for simulation. Change of resistance of a memristor applying 3.6 V p–p square wave across it is shown in Fig. 1(b). Following parameters were used for simulation: R_{ON} = 100 Ω, R_{OFF} = 20 kΩ, p = 10, D = 3 nm and $\mu_v = 350 \times 10^{-9}$ m²/s/V.

Resistance of the memristor changes from 20 kΩ to 100 Ω in positive cycle. This change occurs in reverse direction when the square pulse reverses its direction.

III. RELATED WORKS

SRAM is a form of semiconductor memory widely used in electronics, microprocessor and general computing applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion, and does not need to be dynamically updated as in the case of DRAM memory. While the data in the SRAM memory does not need to be refreshed dynamically, it is still volatile, meaning that when the power is removed from the memory device, the data is not held, and will disappear. The operation of the SRAM memory cell is relatively straightforward. When the cell is selected, the value to be written is stored in the cross-coupled flip-flops. The cells are arranged in a matrix, with each cell individually addressable. Most SRAM memories select an entire row of cells at a time, and read out the contents of all the cells in the row along the column lines. Access to the SRAM memory cell is enabled by the Word Line. This controls the two access control transistors which control whether the cell should be connected to the bit lines. These two lines are used to transfer data for both read

and write operations. The most commonly used SRAM type is the 6T SRAM which offers better electrical performances from all aspects (speed, noise immunity, standby current). The smallest 6T-SRAM cell that has been fabricated till today has an area of 0.08 μm^2 and it was fabricated in the 22 nm process using immersion and EUV lithography [15]. The main disadvantages of the 6T SRAM structure are its large size and high power consumption. To overcome these limitations, memristive-RAMs are being developed recently. According to HP, resistive random access memory (ReRAMs), which are memristor-based versions of both DRAM and SRAM, ought to speed up computers immensely. Along with HP, Samsung and many other companies are working on memristor technology.

There are several researches on memristor based memories. In [16], a complementary resistive switch was introduced. It consists of two anti-serial memristive elements which validates the construction of large passive crossbar arrays with a drastic reduction in power consumption. Junsangsri *et al.* [17] presented a novel memory cell consisting of a memristor and ambipolar transistors. Macroscopic models were utilized to characterize the operations of that memory cell. In [18], Kamran Eshraghian *et al.* provided a new approach towards the design and modeling of memristor based content addressable memory (MCAM) using a combination of memristor and MOS devices to form the core of a memory/compare logic cell. This cell forms the building block of the CAM architecture. The non-volatile characteristic and the minuteness together with compatibility of the memristor with CMOS processing technology increases the packing density, provides new approach towards power management through disabling CAM blocks without loss of stored data, which reduces power dissipation. This inspired us to design a SRAM cell using Memristor-MOS hybrid architecture exploiting the non-volatile characteristic and the nanoscale geometry of a memristor.

IV. PROPOSED SRAM CELL

Electrical scheme of the proposed SRAM cell is shown in Fig. 2(a). Two memristors are used as memory element. The arrangement is in such a way that during write cycle, they are connected in parallel but in opposite polarity [Fig. 2(b)] and during read cycle, they are connected in series [Fig. 2(c)]. These connections are established by two NMOS pass transistors T1 and T2. A third transistor T3 is used to isolate a cell from other cells of the memory array during read and write operations. The gate input of T3 is the Comb signal which is the OR of RD and WR signals. If a bit is to be written, RD is taken to the LOW state and WR and Comb are taken to the HIGH state. As a result, circuit of Fig. 2(b) is formed. The voltage across the memristors is $(V_D - VDD/4)$. Depending on the data, it can be positive (if $D = 1$ i.e. $V_D = VDD$) or negative (if $D = 0$ i.e. $V_D = 0$ V). As polarities of the memristors are opposite, change of memristances (or resistances) will also take place in the opposite direction. Now if the data is to be read, RD and Comb are

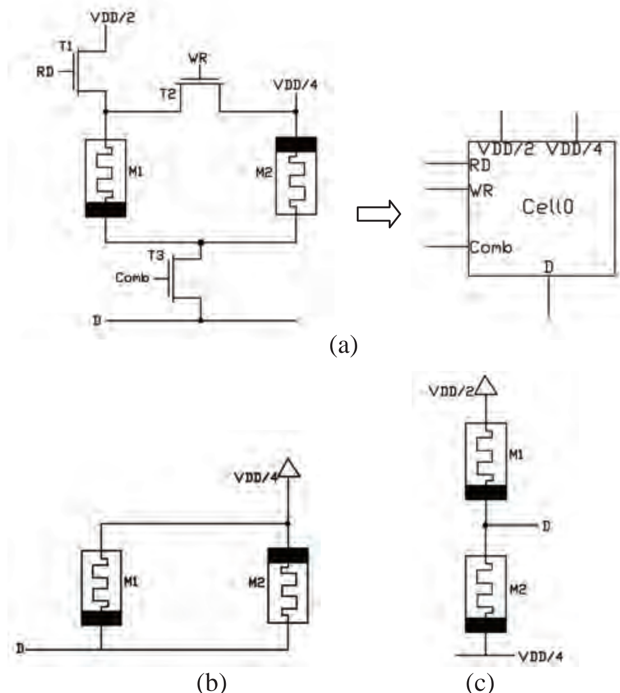


FIGURE 2. (a) Three transistor–two memristor SRAM cell (b) circuit when RD = 0, WR = 1, and Comb = 1. (c) Circuit when RD = 1, WR = 0, and Comb = 1.

taken to the HIGH state and this forms the circuit shown in Fig. 2(c). Voltage at D is now:

$$V_D = \left(\frac{V_{DD}}{2} - \frac{V_{DD}}{4}\right) \times \frac{R2}{(R1 + R2)} + \frac{V_{DD}}{4} \quad (5)$$

where, $R1$ and $R2$ are the resistances of $M1$ and $M2$ respectively. If "1" was written during write cycle, $R2$ becomes significantly greater than $R1$ and then V_D is greater than $VDD/4$. If "0" was written, $R1$ becomes significantly greater than $R2$ which makes V_D to be as close as $VDD/4$. A comparator can be used as a sense amplifier to interpret these voltages as HIGH or LOW correctly.

V. SIMULATIONS AND ANALYSIS

In Fig. 3, a 16 × 16 array is formed for the verification of array structure of our proposed NVRAM cell. Data is fed through wordlines/bitlines. Switching between i/p and o/p is done with the help of CMOS transmission gate controlled by Vdt and Vdtb signals which are complement of each other. In practical circuits, this purpose is served through encoders. Several simulations were done to test the validity of our proposed SRAM structure and compare it with the traditional SRAM structures. In the simulations data was written and read to calculate several important parameters such as write time, read time, power consumption etc. A comparator can be used as a sense amplifier to interpret these voltages as HIGH or LOW correctly. The reference of the comparator should be tied to 0.26 V. Simulations of the circuits are based on the following parameters: $R_{ON} = 100\ \Omega$, $R_{OFF} = 20\ k\Omega$, $p = 10$, $D = 3$ nm and $\mu_v = 350 \times 10^{-9}$ m^2/s/V. The NVRAM cell has been implemented using TSMC 180 nm technology.

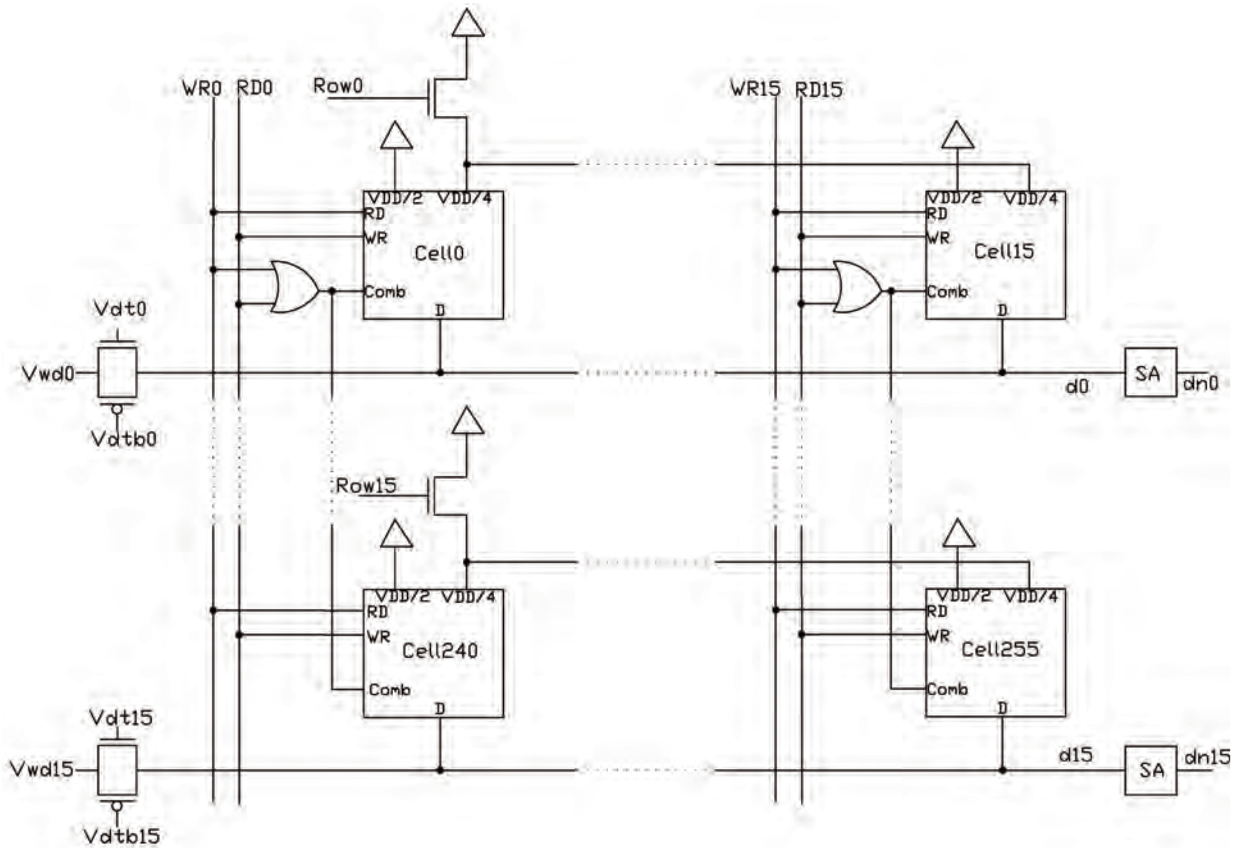


FIGURE 3. 16 × 16 array structure.

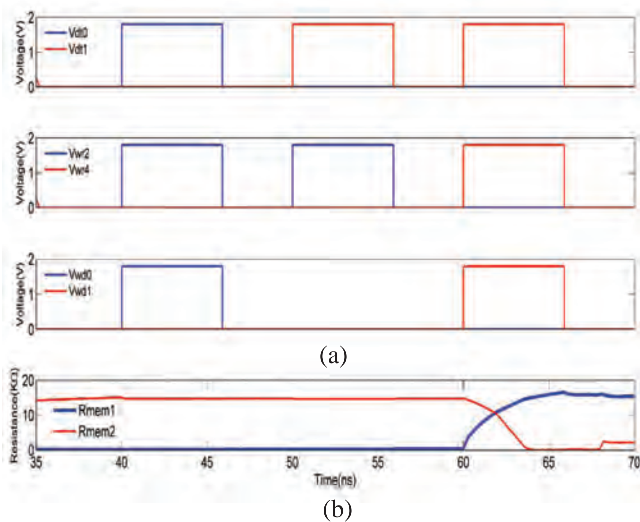


FIGURE 4. (a) Timing diagram of input pulses during write operation. (b) Change of resistance of the two memristors of cell20 during write operation.

A. WRITE OPERATION

In the first write cycle, "1" was written to cell2. Vwr2, Vrow0 and Vdt0 were set to HIGH state to select this cell. Timing diagram in Fig. 4(a) shows Vwr2, Vdt0 pulses and also shows the data in d0 which is Vwd0. This write cycle starts from 40 ns and during this cycle, Vwr2 = 1, Vdt0 = 1

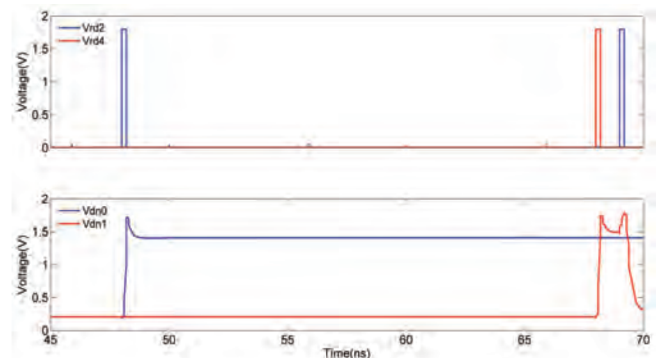


FIGURE 5. Timing diagram of read operation.

and Vwd0 = 1. In the next cycle, a "0" was written to cell18 (from 50 ns) and to do this, Vwr2, Vrow1, Vdt1 were set to HIGH state and Vwd1 was set to LOW state. Finally a "1" was written to cell20 (from 60 ns). For this, Vwr4, Vrow1, Vdt1 and Vwd1, all were set to HIGH state. In Fig. 4(b), plot of the resistance of two memristors in cell20 shows the alteration of resistance while writing "1" into it.

B. READ OPERATION

After writing "1" in cell 2, the stored data was read (from 48 ns). For this, Vrd2 was set to HIGH state and data at dn0 is checked. In Fig. 5, timing diagram of read cycles is shown.

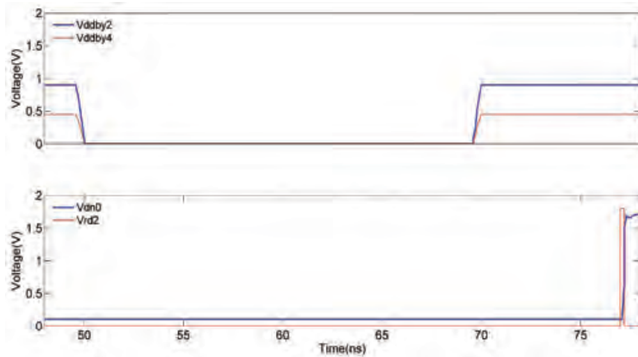


FIGURE 6. Evidence of non-volatility of the memristor SRAM cell. After writing "1" in cell 18, all the power sources are turned off during the time interval 50–69 ns. A read operation is done after turning on the power sources and found "1" in cell 18.

During read operation at cell2, dn0 was found HIGH. Then after two write cycles, cell20 was read (from 68 ns) and found HIGH at dn1. Finally, cell18 was read (from 69 ns) and found LOW at dn1. So after reading a cell, data was found to be exactly the same as it was written previously in that cell. Thus, the array structure shows proper functionality both in read and write operations.

VI. PERSPECTIVES

Our proposed memristor based memory cell is non-volatile in nature.

After writing "1" in cell 18, all the power sources were turned off during the time interval 50–69 ns (Fig. 6). A read operation is done after turning on the power sources and found "1" in cell 18. This proves the non-volatile nature of the cell.

The write and read times were measured and compared in Table 1:

TABLE 1. Write/read time comparison.

Operation	Proposed SRAM Cell (ns)	6-T Cell [19] (ns)
Write	5.9	0.85
Read	0.2	1.23

The proposed NVRAM cell requires a bit more time for the write cycle than the conventional SRAM cells. By further increasing the mobility of the memristors, the write cycle time can be considerably reduced. Fig. 7 shows the inverse relation between mobility of the memristor and the write cycle time. The read cycle time depends on the sensitivity and responsiveness of the sense amplifier.

From simulation the power dissipation curve was found and integration was done to get the energy dissipated for separate operations (writing and reading "1" & "0"). And then the energy values were divided by respective operation cycle times to get the corresponding power dissipations (Table 2).

The obtained values were then averaged to get the total power dissipation. This was compared with the value of the conventional SRAM cell in Table 3.

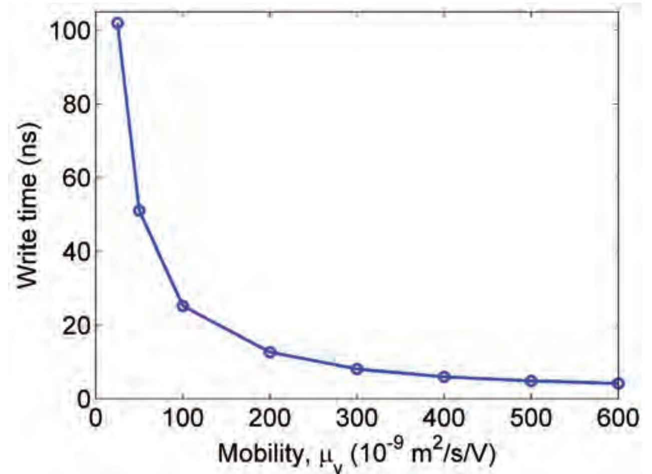


FIGURE 7. Inverse relation between mobility of the memristor and the write cycle time.

TABLE 2. Power dissipation during different operations.

Operation	Wr0	Wr1	Rd0	Rd1
Energy (fJ/cycle)	191.01	803.49	61.36	68
Power (μW)	32.37	136.18	306.85	340
Peak power (mW)	0.935	2.5	5.8	5.9

TABLE 3. Power comparison.

Operation	Proposed SRAM Cell (mW)	6-T Cell [19] (mW)
Power	0.407	10.373

Power consumption is much less than 6-T cell which can be reduced more by designing a faster comparator which would reduce the read time.

The area of the proposed memory cell can be predicted to be much less than the area of conventional 6-T SRAM cell, as only three transistors are used along with two memristors. As memristors can be as small as 3 nm, the area can be further reduced if we can switch to more recent fabrication technologies such as 22 nm technology.

VII. CONCLUSION

In this paper, we proposed a new idea of NVRAM cell using memristor. The read time is much faster compared to a conventional SRAM and the power consumption is also much smaller. However the writing speed is not satisfactory compared to existing SRAM cells due to the low mobility of the memristor in the SPICE model we used. Recent researches suggest that the write time can be significantly reduced [14], [20] using state-of-the-art fabrication techniques. The comparator used to read the data can be replaced by a more compact and efficient sense amplifier which in turn would further decrease the read time. There are further scopes to work on

power consumption as well. Overall, it can be said that our proposed NVRAM is a combination of new technology and innovative design which can open a new door in the field of memory design.

REFERENCES

[1] L. Chua, "Memristor-the missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep. 1971.

[2] D. Struckov, G. Snider, D. Stewart, and R. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[3] G. Chen, "Leon Chua's memristor," *IEEE Circuits Syst. Mag.*, vol. 8, no. 2, pp. 55–56, Apr. 2008.

[4] Y. V. Pershin and M. DiVentra, "Spin memristive systems: Spin memory effects in semiconductor spintronics," *Phys. Rev. B*, vol. 78, no. 11, pp. 113309-1–113309-4, 2008.

[5] X. Wang, Y. Chen, H. Xi, H. Li, and D. Dimitrov, "Spintronic memristor through spin-torque-induced magnetization motion," *IEEE Electron Device Lett.*, vol. 30, no. 3, pp. 294–297, Mar. 2009.

[6] K. Witrisal, "Memristor based stored reference receiver-the UWB solution," *Electron. Lett.*, vol. 45, no. 14, pp. 713–714, 2009.

[7] S. Shin, K. Kim, and S. M. Kang, "Memristor based fine resolution programmable resistance and its applications," in *Proc. IEEE Int. Conf. Commun., Circuits, Syst.*, Jul. 2009, pp. 948–951.

[8] D. Varghese and G. Gandi, "Memristor based highline arrange differential pair," in *Proc. IEEE Int. Conf. Commun., Circuits Syst.*, Jul. 2009, pp. 935–938.

[9] Y. V. Pershin and M. DiVentra, "Practical approach to programmable analog circuits with memristors," *IEEE Trans. Circuits Syst. I, Reg. Paper*, vol. 57, no. 8, pp. 1857–1864, Jan. 2010.

[10] S. Shin, K. Kim, and S. M. Kang, "Memristor applications for programmable analog ICs," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 266–274, Mar. 2011.

[11] D. Batas and H. Fiedler, "A memristor SPICE implementation and a new approach for magnetic flux controlled memristor modeling," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 250–255, Mar. 2011.

[12] D. B. Strukov and S. Williams, "Exponential ionic drift: Fast switching and low volatility of thin-film memristors," *Appl. Phys. A, Mater. Sci. Process.*, vol. 94, no. 3, pp. 515–519, 2009.

[13] Z. Biolek, D. Biolek, and V. Biolkov, "A SPICE model of memristor with nonlinear dopant drift," *Radio Eng. J.*, vol. 18, no. 2, p. 211, 2009.

[14] N. Y. Joglekar and S. J. Wolf, "The elusive memristor: Properties of basic electrical circuits," *Eur. J. Phys.*, vol. 30, no. 4, p. 661, 2009.

[15] O. Wood, C. Koay, K. Petrillo, H. Mizuno, S. Raghunathan, J. Arnold, D. Horak, M. Burkhardt, G. McIntyre, Y. Deng, B. La Fontaine, U. Okoroanyanwu, A. Tchikoulaeva, T. Wallow, H.-C. James, M. Colburn, S. S. C. Fan, Bala S. Haran, and Y. Yin, "Integration of EUV lithography in the fabrication of 22-nm node devices," *Proc. SPIE* vol. 7271, pp. 727104-1–727104-2, 2009.

[16] E. Linn, R. Rosezin, C. Kügeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," *Nature Mater.*, vol. 9, pp. 403–406, Apr. 2010.

[17] P. Junsangsri and F. Lombardi, "A memristor-based memory cell using ambipolar operation," in *Proc. IEEE 29th Int. Conf. Comput. Design*, Oct. 2011, pp. 148–153.

[18] K. Eshraghian, K.-R. Cho, O. Kavehei, S. KuKang, D. Abbott, and S. M. Steve Kang, "Memristor MOS content addressable memory (MCAM): Hybrid architecture for future high performance search engines," *IEEE Trans. Very Large scale Integr. (VLSI) Syst.*, vol. 19, no. 8, pp. 1407–1417, Aug. 2011.

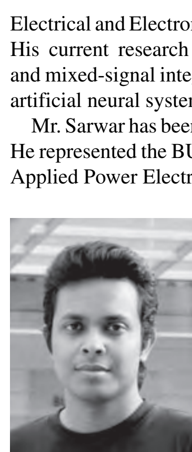
[19] G. M. Sreerama Reddy and P. C. Reddy, "Design and implementation of 8K-bits low power SRAM in 180nm technology," in *Proc. Int. Multi Conf. Eng. Comput. Sci.*, vol. 2. Mar. 2009, pp. 1–8.

[20] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, R. S. Williams, "'Memristive' switches enable 'stateful' logic operations via material implication," *Nature*, vol. 464, pp. 873–876, Apr. 2010.

SYED SHAKIB SARWAR (S'11) was born in Dhaka, Bangladesh, in 1989. He received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, in 2012. He is currently pursuing the M.Sc. degree in electrical and communication Engineering from the Department of Electrical and Electronic Engineering, BUET.

Since 2012, he has been a Faculty Member of Electrical and Electronic Engineering Department, BRAC University, Dhaka. His current research interests include high frequency, low power analog and mixed-signal integrated circuits, FPGA based digital circuit prototyping, artificial neural systems, and image processing.

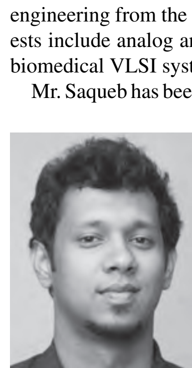
Mr. Sarwar has been with the IEEE Solid State Circuits Society since 2012. He represented the BUET team in the IFEC-2011 Workshop during the IEEE Applied Power Electronics Conference in Dallas, TX, USA.



SYED AN NAZMUS SAQUEB (S'11) was born in Natore, Bangladesh, in 1988. He received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, in 2012.

Since 2012, he has been a Faculty Member of the Electrical and Electronic Engineering Department, University of Asia Pacific, Dhaka. He is pursuing the M.Sc. degree in electrical and communication engineering from the Department of EEE, BUET. His current research interests include analog and mixed-signal circuit design, neuromorphic circuits, biomedical VLSI systems, and circuit design with novel devices.

Mr. Saqueb has been with the IEEE Solid State Circuits Society since 2012.



FARHAN QUAIYUM (S'11) was born in Dhaka, Bangladesh, in 1989. He received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 2012.

He has been an ASIC Design Engineer with Fastrack Anontex Ltd., since June 2012. He is pursuing the M.Sc. degree in electrical and communication engineering from the Department of EEE, BUET. His current research interests include high speed digital circuit design, ultra-low-power/low voltage circuits, and embedded systems.

A. B. M. HARUN-UR RASHID (M'89–SM'02) received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology (BUET) Dhaka, Bangladesh, in 1984, the M.Sc. degree in electronic engineering from Oita University, Japan, in 1988, and the Ph.D. degree in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1996.

He has been as a Faculty Member with the Department of Electrical and Electronic Engineering, BUET, where he is a Professor since 2006. He served as a Design Engineer with Texas Instruments Japan Ltd., from 1988 to 1993, where he worked on the research and development of 1.2μm Bi-CMOS process for mixed signal VLSI circuits. He was a Research Fellow with the Research Center for Nanodevices and Systems, Hiroshima University, Tokyo, Japan, from 2001 to 2003, where he worked in the design and demonstration of on-chip wireless interconnect. His current research interests include high speed and low power circuit design using novel nanodevices, very high frequency analog integrated circuit design, and on-chip wireless interconnect design.