INPUT SWITCHED HIGH PERFORMANCE SINGLE PHASE AC-DC CONVERTERS

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By

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Table of Contents

List of Figures	vi
List of Tables	xvi
List of Abbreviations of Technical Terms	xviii
Acknowledgement	xix
Abstract	XX
Chapter 1 Introduction	1
1.1 Background and present status of the problem	1
1.2 Objective of the thesis	6
1.3 Thesis Outline	7
Chapter 2 Single Phase Uncontrolled AC-DC Converters	8
2.1 Half Wave Rectifier	8
2.2 Full Wave Rectifier	9
Chapter 3 DC-DC Converters	14
3.1 Basics of DC-DC Converters	14
3.2 Types of DC-DC Converters	15
3.2.1 Buck Converter	16
3.2.2 Boost Converter	18
3.2.3 Buck-Boost Converter	19
3.2.4 Ćuk Converter	21
3.2.5 SEPIC Converter	23
3.2.6 Inverse SEPIC Converter	25
Chapter 4 Input Switched AC-DC Converters: Performance Analysis	27
4.1 Single Phase Input Switched Buck AC-DC Converter	27
4.2 Single Phase Input Switched Boost AC-DC Converter	36
4.2.1 Single Phase Input Switched Boost AC-DC Converter-Configuration 1	36
4.2.2 Single Phase Input Switched Boost AC-DC Converter-Configuration 2	45
4.3 Single Phase Input Switched Buck-Boost AC-DC Converter	51
4.3.1 Single Phase Input Switched Buck-Boost AC-DC Converter-	51
Configuration 1	

4.3.2 Single Phase Input Switched Buck-Boost AC-DC Converter-	59
Configuration 2	
4.3.3 Single Phase Input Switched Buck-Boost AC-DC Converter-	66
Configuration 3	
4.4 Single Phase Input Switched Ćuk AC-DC Converter	72
4.4.1 Single Phase Input Switched Ćuk AC-DC Converter-Configuration 1	72
4.4.2 Single Phase Input Switched Ćuk AC-DC Converter-Configuration 2	80
4.5 Single Phase Input Switched SEPIC AC-DC Converter	86
4.5.1 Single Phase Input Switched SEPIC AC-DC Converter-	86
Configuration 1	
4.5.2 Single Phase Input Switched SEPIC AC-DC Converter-	94
Configuration 2	
4.6 Single Phase Input Switched Inverse SEPIC AC-DC Converter	100
4.6.1 Single Phase Input Switched Inverse SEPIC AC-DC Converter-	100
Configuration 1	
4.6.2 Single Phase Input Switched Inverse SEPIC AC-DC Converter-	108
Configuration 2	
4.7 Example of a Closed Controlled Single Phase Input Switched Boost AC-DC	114
Converter	
4.7.1 Single Phase Output Regulated Boost AC-DC Converter with	114
Feedback Control	
4.7.2 Single Phase Input Regulated Boost AC-DC Converter	117
(Proposed Configuration 2) with Feedback Control	
Chapter 5 Conclusion	119
5.1 Summary of the thesis	119
5.2 Future Work	121
References	122

List of Figures

Fig 1.1:	Conventional rectifier circuit with inductive filter	4
Fig 1.2:	Rectifier circuit with input capacitance Cs	4
Fig 1.3:	Rectifier circuit with series resonant input filter	5
Fig 1.4:	Rectifier with parallel resonant filter	5
Fig 2.1:	Half wave rectifier	8
Fig 2.2:	Input and output voltage waves of half-wave rectifier	9
with resi	stive load	
Fig 2.3:	Full wave bridge rectifier	10
Fig 2.4:	Input and output waves of full-wave rectifier with resistive load	11
Fig 2.5:	Full wave rectifier with capacitor at the output	12
Fig 2.6:	Ripple voltage of full wave rectifier with capacitor at the output	12
Fig 2.7:	Input voltage and input current shapes of full wave rectifier	13
Fig 3.1:	A DC-DC converter	14
Fig 3.2:	PWM signal generated by microprocessor	15
Fig 3.3:	Buck DC-DC Converter	16
Fig 3.4:	Buck converter with switch ON	16
Fig 3.5:	Buck converter with switch OFF	17
Fig 3.6:	Buck converter gain vs. duty cycle	17
Fig 3.7:	Boost DC-DC Converter	18
Fig 3.8:	Boost converter with switch ON	18
Fig 3.9:	Boost converter with switch OFF	19
Fig 3.10:	Boost converter gain vs. duty cycle	19
Fig 3.11:	Buck-Boost DC-DC Converter	20
Fig 3.12:	Buck-Boost converter with switch ON	20
Fig 3.13:	Buck-Boost converter with switch OFF	20
Fig 3.14:	Buck-Boost converter gain vs. duty cycle	21
Fig 3.15:	Ćuk DC-DC Converter	21
Fig 3.16:	Ćuk converter with switch ON	22
Fig 3.17:	Ćuk converter with switch OFF	22

Fig 3.18:	Ćuk converter gain vs. duty cycle	22
Fig 3.19:	SEPIC DC-DC Converter	23
Fig 3.20:	SEPIC converter with switch ON	24
Fig 3.21:	SEPIC converter with switch OFF	24
Fig 3.22:	SEPIC converter gain vs. duty cycle	24
Fig 3.23:	Inverse SEPIC DC-DC Converter	25
Fig 3.24:	Inverse SEPIC converter with switch ON	26
Fig 3.25:	Inverse SEPIC converter with switch OFF	26
Fig 3.26:	Inverse SEPIC converter gain vs. duty cycle	26
Fig 4.1:	The conventional single phase bridge rectifier with	27
	output switching in Buck Configuration	
Fig 4.2:	The single phase input switched AC-DC converter	28
	(Buck Configuration)	
Fig 4.3:	Equivalent circuit of the circuit of Fig. 4.2 for	28
	positive cycle switch ON	
Fig 4.4:	Equivalent circuit of the circuit of Fig. 4.2 for	28
	positive cycle switch OFF	
Fig 4.5:	Equivalent circuit of the circuit of Fig. 4.2 for	29
	negative cycle switch ON	
Fig 4.6:	Equivalent circuit of the circuit of Fig. 4.2 for	29
	negative cycle switch OFF	
Fig 4.7:	Input current shape of the proposed input switched buck	30
	configuration circuit of Fig. 4.2, (without input filter)	

Fig 4.8:	Output voltage wave shape of the proposed input switched buck	30
	configuration circuit of Fig. 4.2, (without input filter)	
Fig 4.9:	Efficiency, Input PF and THD vs. duty cycle of input switched	32
	Buck AC-DC converter	
Fig 4.10:	Efficiency, Input PF and THD vs. Load Resistance of input	34
	switched Buck AC-DC converter	
Fig 4.11:	The conventional bridge rectifier with output switching in	35
	Boost configuration	
Fig 4.12:	The single phase input switched AC-DC converter	36
	(Boost Configuration 1)	
Fig 4.13:	Equivalent circuit of the circuit of Fig. 4.12	37
	for positive cycle switch ON	
Fig 4.14:	Equivalent circuit of the circuit of Fig. 4.12	37
	for positive cycle switch OFF	
Fig 4.15:	Equivalent circuit of the circuit of Fig. 4.12	38
	for negative cycle switch ON	
Fig 4.16:	Equivalent circuit of the circuit of Fig. 4.12	38
	for negative cycle switch OFF	
Fig 4.17:	Input current shape of the proposed input switched	39
	boost configuration 1 circuit of Fig. 4.12	
Fig 4.18:	Output voltage wave shape of the proposed input switched	39
	boost configuration 1 circuit of Fig. 4.12	
Fig 4.19:	Efficiency, Input PF and THD vs. Duty Cycle of input switched	41
	boost AC-DC converter-configuration 1	
Fig 4.20:	Efficiency, Input PF and THD vs. Load Resistance of	43
	input switched boost AC-DC converter-configuration 1	
Fig 4.21:	The single phase input switched AC-DC converter	44
	(Boost Configuration 2)	
Fig 4.22:	Equivalent circuit of the circuit of Fig.4.21	45
	for positive cycle switch ON	

Fig 4.23:	Equivalent circuit of the circuit of Fig.4.21	45
	for positive cycle switch OFF	
Fig 4.24:	Equivalent circuit of the circuit of Fig.4.21	46
	for negative cycle switch ON	
Fig 4.25:	Equivalent circuit of the circuit of Fig.4.21	46
	for negative cycle switch OFF	
Fig 4.26:	Input current shape of the proposed input switched	47
	boost configuration 2 circuit of Fig.4.21	
Fig 4.27:	Output voltage wave shape of the proposed input switched	47
	boost configuration 2 circuit of Fig.4.21	
Fig 4.28:	Efficiency, Input PF and THD vs. duty cycle of	49
	input switched Boost AC-DC converter-configuration 2	
Fig 4.29:	The conventional bridge rectifier with output switching in	50
	Buck-Boost configuration	
Fig 4.30:	The single phase input switched AC-DC converter	51
	(Buck-Boost Configuration 1)	
Fig 4.31:	Equivalent circuit of the circuit of Fig. 4.30	51
	for positive cycle switch ON	
Fig 4.32:	Equivalent circuit of the circuit of Fig. 4.30	52
	for positive cycle switch OFF	
Fig 4.33:	Equivalent circuit of the circuit of Fig. 4.30	52
	for negative cycle switch ON	
Fig 4.34:	Equivalent circuit of the circuit of Fig. 4.30	53
	for negative cycle switch OFF	
Fig 4.35:	Input current shape of the proposed input switched	53
	buck-boost configuration-1 circuit of Fig. 4.30	
Fig 4.36:	Output voltage wave shape of the proposed input switched	54
	buck-boost configuration-1 circuit of Fig. 4.30	
Fig 4.37:	Efficiency, Input PF and THD vs. duty cycle of	55
	input switched Buck-Boost AC-DC converter-configuration 1	

Fig 4.38:	Efficiency, Input PF and THD vs. Load Resistance of	57
	input switched Buck-Boost AC-DC converter-configuration 1	
Fig 4.39:	The single phase input switched AC-DC converter	58
	(Buck-Boost Configuration 2)	
Fig 4.40:	Equivalent circuit of the circuit of Fig.4.39	59
	for positive cycle switch ON	
Fig 4.41:	Equivalent circuit of the circuit of Fig.4.39	59
	for positive cycle switch OFF	
Fig 4.42:	Equivalent circuit of the circuit of Fig.4.39	60
	for negative cycle switch ON	
Fig 4.43:	Equivalent circuit of the circuit of Fig.4.39	60
	for negative cycle switch OFF	
Fig 4.44:	Input current shape of the proposed input switched	61
	buck-boost configuration-2 circuit of Fig. 4.39	
Fig 4.45:	Output voltage wave shape of the proposed	61
	input switched buck-boost configuration-2 circuit of Fig. 4.39	
Fig 4.46:	Efficiency, Input PF and THD vs. duty cycle of	63
	input switched Buck-Boost AC-DC converter-configuration 2	
Fig 4.47:	Efficiency, Input PF and THD vs. Load Resistance of	65
	input switched Buck-Boost AC-DC converter-configuration 2	
Fig 4.48:	The single phase input switched AC-DC converter	66
	(Buck-Boost Configuration 3)	
Fig 4.49:	Equivalent circuit of the circuit of Fig.4.48	67
	for positive cycle switch ON	
Fig 4.50:	Equivalent circuit of the circuit of Fig.4.48	67
	for positive cycle switch OFF	
Fig 4.51:	Equivalent circuit of the circuit of Fig.4.48	68
	for negative cycle switch ON	
Fig 4.52:	Equivalent circuit of the circuit of Fig.4.48	68
	for negative cycle switch OFF	

Fig 4.53:	Input current shape of the proposed input switched	69
	Buck-Boost configuration-3 circuit of Fig 4.48	
Fig 4.54:	Output voltage wave shape of the proposed input switched	69
	Buck-Boost configuration-3 circuit of Fig 4.48	
Fig 4.55:	Efficiency, Input PF and THD vs. duty cycle of	71
	input switched Buck-Boost AC-DC converter-configuration 3	
Fig 4.56:	The conventional bridge rectifier with output switching in	72
	Ćuk Configuration	
Fig 4.57:	The single phase input switched AC-DC converter	72
	(Ćuk Configuration 1)	
Fig 4.58:	Equivalent circuit of the circuit of Fig. 4.57	73
	for positive cycle switch ON	
Fig 4.59:	Equivalent circuit of the circuit of Fig. 4.57	73
	for positive cycle switch OFF	
Fig 4.60:	Equivalent circuit of the circuit of Fig. 4.57	74
	for negative cycle switch ON	
Fig 4.61:	Equivalent circuit of the circuit of Fig. 4.57	74
	for negative cycle switch OFF	
Fig 4.62:	Input current shape of the proposed input switched	75
	Ćuk configuration 1 circuit of Fig 4.57	
Fig 4.63:	Output voltage wave shape of the proposed input switched	75
	Ćuk configuration 1 circuit of Fig 4.57	
Fig 4.64:	Efficiency, Input PF and THD vs. duty cycle of	77
	input switched Ćuk AC-DC converter-configuration 1	
Fig 4.65:	Efficiency, Input PF and THD vs. Load Resistance of	79
	input switched Ćuk AC-DC converter-configuration 1	
Fig 4.66:	The single phase input switched AC-DC converter	80
	(Ćuk Configuration 2)	
Fig 4.67:	Equivalent circuit of the circuit of Fig.4.66	81
	for positive cycle switch ON	

Fig 4.68:	Equivalent circuit of the circuit of Fig.4.66	81
	for positive cycle switch OFF	
Fig 4.69:	Equivalent circuit of the circuit of Fig.4.66	82
	for negative cycle switch ON	
Fig 4.70:	Equivalent circuit of the circuit of Fig.4.66	82
	for negative cycle switch OFF	
Fig 4.71:	Input current shape of the proposed input switched	83
	Ćuk configuration 2 circuit	
Fig 4.72:	Output voltage wave shape of the proposed	83
	input switched Ćuk configuration 2 circuit	
Fig 4.73:	Efficiency, Input PF and THD vs. duty cycle of	85
	input switched Ćuk AC-DC converter-configuration 2	
Fig 4.74:	The conventional bridge rectifier with output switching in	86
	SEPIC configuration	
Fig 4.75:	The single phase input switched AC-DC converter	86
	(SEPIC Configuration 1)	
Fig 4.76:	Equivalent circuit of the circuit of Fig.4.75	87
	for positive cycle switch ON	
Fig 4.77:	Equivalent circuit of the circuit of Fig.4.75	87
	for positive cycle switch OFF	
Fig 4.78:	Equivalent circuit of the circuit of Fig.4.75	88
	for negative cycle switch ON	
Fig 4.79:	Equivalent circuit of the circuit of Fig.4.75	88
	for negative cycle switch OFF	
Fig 4.80:	Input current shape of the proposed input switched	89
	SEPIC configuration 1 circuit of Fig.4.75	
Fig 4.81:	Output voltage wave shape of the proposed input switched	89
	SEPIC configuration 1 circuit of Fig. 4.75	
Fig 4.82:	Efficiency, Input PF and THD vs. duty cycle of	91
	input switched SEPIC AC-DC converter-configuration 1	

Fig 4.83:	Efficiency, Input PF and THD vs. Load Resistance of	93
	input switched SEPIC AC-DC converter-configuration 1	
Fig 4.84:	The single phase input switched AC-DC converter	94
	(SEPIC Configuration 2)	
Fig 4.85:	Equivalent circuit of the circuit of Fig. 4.84	95
	for positive cycle switch ON	
Fig 4.86:	Equivalent circuit of the circuit of Fig. 4.84	95
	for positive cycle switch OFF	
Fig 4.87:	Equivalent circuit of the circuit of Fig. 4.84	96
	for negative cycle switch ON	
Fig 4.88:	Equivalent circuit of the circuit of Fig. 4.84	96
	for negative cycle switch OFF	
Fig 4.89:	Input current shape of the proposed input switched	97
	SEPIC configuration 2 circuit of Fig.4.84	
Fig 4.90:	Output voltage wave shape of the proposed input switched	98
	SEPIC configuration 2 circuit of Fig.4.84	
Fig 4.91:	Efficiency, Input PF and THD vs. duty cycle of	99
	input switched SEPIC AC-DC converter-configuration 2	
Fig 4.92:	The conventional bridge rectifier with output switching in	100
	Inverse SEPIC configuration	
Fig 4.93:	The single phase input switched AC-DC converter	100
	(Inverse SEPIC Configuration 1)	
Fig 4.94:	Equivalent circuit of the circuit of Fig.4.93	101
	for positive cycle switch ON	
Fig 4.95:	Equivalent circuit of the circuit of Fig.4.93	101
	for positive cycle switch OFF	
Fig 4.96:	Equivalent circuit of the circuit of Fig.4.93	102
	for negative cycle switch ON	
Fig 4.97:	Equivalent circuit of the circuit of Fig.4.93	102
	for negative cycle switch OFF	

Fig 4.98:	Input current shape of the proposed input switched Inverse SEPIC	103
	configuration 1 circuit of Fig.4.93	
Fig 4.99:	Output voltage wave shape of the proposed input switched	104
	Inverse SEPIC configuration 1 circuit of Fig.4.93	
Fig 4.100	: Efficiency, Input PF and THD vs. duty cycle of	105
	input switched Inverse SEPIC AC-DC converter-configuration 1	
Fig 4.101	: Efficiency, Input PF and THD vs. Load Resistance of	107
	input switched Inverse SEPIC AC-DC converter-configuration 1	
Fig 4.102	The single phase input switched AC-DC converter	108
	(Inverse SEPIC Configuration 2)	
Fig 4.103	Equivalent circuit of the circuit Fig. 4.102	109
	for positive cycle switch ON	
Fig 4.104	Equivalent circuit of the circuit Fig. 4.102	109
	for positive cycle switch OFF	
Fig 4.105	Equivalent circuit of the circuit Fig. 4.102	110
	for negative cycle switch ON	
Fig 4.106	Equivalent circuit of the circuit Fig. 4.102	110
	for negative cycle switch OFF	
Fig 4.107	: Input current shape of the proposed input switched Inverse SEPIC	111
	configuration 2 circuit of Fig. 4.102	
Fig 4.108	Output voltage wave shape of the proposed input switched	111
	Inverse SEPIC configuration 2 circuit of Fig. 4.102	
Fig 4.109	: Efficiency, Input PF and THD vs. duty cycle of input switched	113
	Inverse SEPIC AC-DC converter-configuration 2	
Fig 4.110	: Regulated DC power supply	114
Fig 4.111	The output regulated Boost AC-DC converter	114
Fig 4.112	: Feedback control loops for output regulated	115
	Boost AC-DC converter	
Fig 4.113	: Feed forward of the input voltage for output regulated Boost AC-	115
	DC converter with feedback control	

Fig 4.114: Feedback controlled output Boost converter regulated AC-DC	116
converter (power circuit with sensors)	
Fig 4.115: Feedback control circuit for Boost AC-DC converter	116
configuration-2	
Fig 4.116: Typical input current and output voltage waveforms of circuit of	117
Fig. 4.114 controlled by circuit of Fig. 4.115	
Fig 4.117: Input switched Boost AC-DC converter with feedback control	118
(proposed config. 2)	
Fig 4.118: Typical input current and output voltage waveforms of circuit of	118
Fig. 4.117 controlled by circuit of Fig. 4.115	

List of Tables

Table 4.1:	Performance Comparison of Proposed and Conventional Buck	31
	Topology Based Rectifier for Duty Cycle Variation	
Table 4.2:	Performance Comparison of Proposed and Conventional	33
	Buck Topology Based Rectifier for Load Variation	
Table 4.3:	Performance Comparison of Proposed and Conventional	40
	Boost Topology Based Rectifier Configuration 1	
	for Duty Cycle Variation	
Table 4.4:	Performance Comparison of Proposed and Conventional	42
	Boost Topology Based Rectifier Configuration 1	
	for Load Variation	
Table 4.5:	Performance Comparison of Proposed Input Regulated and	48
	Conventional Output Regulated Boost Topology Based	
	Rectifier Configuration 2 for Duty Cycle Variation	
Table 4.6:	Performance Comparison of Proposed and Conventional	54
	Buck-Boost Topology Based Rectifier Configuration 1	
	for Duty Cycle Variation	
Table 4.7:	Performance Comparison of Proposed and Conventional	56
	Buck-Boost Topology Based Rectifier Configuration 1	
	for Load Variation	
Table 4.8:	Performance Comparison of Proposed and Conventional	62
	Buck-Boost Topology Based Rectifier Configuration 2 for Duty	
	Cycle Variation	
Table 4.9:	Performance Comparison of Proposed and Conventional	64
	Buck-Boost Topology Based Rectifier Configuration 2 for Load	
	Variation	
Table 4.10:	: Performance Comparison of Proposed and Conventional	70
	Buck-Boost Topology Based Rectifier Configuration 3 for Duty	
	Cycle Variation	

Table 4.1	1: Performance Comparison of Proposed and Conventional Ćuk	76
	Topology Based Rectifier Configuration 1 for Duty Cycle	
	Variation	
Table 4.1	2: Performance Comparison of Proposed and Conventional Ćuk	78
	Topology Based Rectifier Configuration 1 for Load Variation	
Table 4.1	3: Performance Comparison of Proposed and Conventional Ćuk	84
	Topology Based Rectifier Configuration 2 for Duty Cycle	
	Variation	
Table 4.1	4: Performance Comparison of Proposed and Conventional SEPIC	
	Topology Based Rectifier Configuration 1 for Duty Cycle	90
	Variation	
Table 4.1	5: Performance Comparison of Proposed and Conventional SEPIC	92
	Topology Based Rectifier Configuration 1 for Load Variation	
Table 4.1	6: Performance Comparison of Proposed and Conventional SEPIC	98
	Topology Based Rectifier Configuration 2 for Duty Cycle	
	Variation	
Table 4.1	7: Performance Comparison of Proposed and Conventional Inverse	104
	SEPIC Topology Based Rectifier Configuration 1 for Duty Cycle	
	Variation	
Table 4.1	8: Performance Comparison of Proposed and Conventional	106
	SEPIC Topology Based Rectifier Configuration 1 u for Duty	
	Cycle Variation	
Table 4.1	9: Performance Comparison of Proposed and Conventional Inverse	112
	SEPIC Topology Based Rectifier Configuration 2 for Duty Cycle	
	Variation	

List of Abbreviations of Technical Terms

BJT Bipolar Junction Transistor

IEEE Institute of Electrical and Electronic Engineers

IEC International Electrotechnical Commission

IGBT Insulated Gate Bipolar Transistor

SCR Silicon Controlled Rectifier

MOSFET Metal Oxide Semiconductor Field Effect Transistor

PWM Pulse Width Modulation

THD Total Harmonic Distortion

CCM Continuous Current Conduction Mode

DCM Discontinuous Current Conduction Mode

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Abstract

Single phase diode rectifiers are widely used in industrial, commercial, utility and domestic applications. Many input wave shaping methods have been proposed to solve the problem of poor power factor which can be classified as active and passive methods. Six different DC-DC converter topologies have been studied to solve the low efficiency, poor input power factor and total harmonic distortion problems of single phase AC-DC converters. The proposed topologies showed superior performance over passive filtering techniques and output regulated single phase AC-DC converters. Some of the input switched topologies have been reported earlier, whereas, new input switched topologies with reduced component number are proposed in this thesis. Five reduced component input switched single phase AC-DC rectifier has been studied. The topologies used are Boost configuration-2, Buck-Boost configuration-3, Cuk configuration-2, SEPIC configuration-2 and Inverse SEPIC configuration-2. Results are compared with the reported ones. Proposed topologies show lower input current THD, higher PF compared to previously reported topologies. However efficiency remains almost the same for both previous and proposed topologies. All the newly reported topologies are easier to implement. Typical output voltage and input current waveforms are shown. It has been found that without feedback control, the input switched single phase rectifiers perform better than output regulated single phase AC-DC converters in terms of input current THD, input power factor and conversion efficiency. Input switched single phase AC-DC converters reported earlier and proposed in this thesis are expected to perform better with feedback control circuit as well. As an example an input switched Boost regulated single phase AC-DC converter is studied and its performance is briefly compared with output regulated Boost single phase AC-DC converter.

CHAPTER 1

INTRODUCTION

1.1 Background and present status of the problem

Single phase AC-DC converters (rectifiers) are common in power supplies that form interface between utility power supply and electronic equipment connected to them [1]. Uncontrolled single phase diode bridge rectifiers with output capacitive filter draw non-sinusoidal currents [2-7]. This causes high input current THD and low input power factor which is detrimental to utility power supply. In the past passive filters consisting of large L and C at the input was used to reduce current distortion (THD) at the cost of further power factor and efficiency reduction [1,4-5]. With the development of power electronics, active filtering techniques have been used to alleviate these problems [5-8]. These included harmonic current injection and use of DC-DC converter between rectifier and load. The DC-DC converter between rectifier and load has many possible configurations [8-9] including those of bridgeless configuration. Recently some configurations and techniques are being investigated for input current switching by providing switch between source and rectifier [8-9]. So far Boost, Buck, Buck-Boost and Ćuk configurations have been investigated for single phase rectifier input current switching.

The rectifier with output filter capacitor is called a conventional AC-DC utility interface. The filter capacitor reduces the ripples present in the output voltage. Although a filter capacitor significantly suppresses the ripple from the output voltage, it introduces distortions in the input current and draws current from the supply discontinuously in short pulses. This introduces problems including reduction of available power and increased loss.

Problems of conventional interface: The large harmonic content and the consequent poor power factor (PF) of operation of the conventional rectifier--capacitor type interface causes several problems to the utility supply. Some of them are listed below [1-4]

(i) Due to harmonic components - Because of the non-zero source impedance in the

utility supply, the harmonic currents flowing through the conventional AC-DC utility

interface will cause a distortion in the voltage waveform at the point of common

coupling. This may cause malfunction of power system protection, loads and

metering devices. Besides voltage waveform distortion, harmonic components may

also cause the problems of overheating of neutral line, distribution transformers and

distribution lines, interference with communication and control signals, over voltages

due to resonance conditions.

(ii) Due to poor PF - Poor power factor of operation implies ineffective use of the

volt-ampere ratings of the utility equipment such as transformers, distribution lines

and generators. Also, it places a restriction on the total equipment load that can be

connected to a typical home or office wall-plug with specified maximum r.m.s current

rating.

Desirable features of a power factor correction techniques

Input side features:

(1) Sinusoidal input current with close to unity PF operation.

(2) Reduced EMI.

(3) Insensitive to small signal perturbations in the load.

Output side features:

(1) Good line and load regulation.

(2) Low output voltage ripple.

(3) Fast output dynamics (i.e., high bandwidth).

(4) Multiple output voltage, levels if needed by the application.

Others: Mechanical and Electrical features

(1) Galvanic isolation between input and output.

- (2) High power conversion efficiency.
- (3) Hold-up time if required.
- (4) Universal input voltage operation (85 V- 270 V AC r.m.s)
- (5) Low part count.
- (6) Smaller size and weight.
- (7) Low cost.

Passive power factor correction

The power line disturbances caused by the proliferation of phase controlled and diode rectifier circuits were of concern even in late 70s [3] [11]. The definition of power factor for nonlinear circuits and passive techniques for improving it are presented in an early literature [11]. Passive techniques remained attractive for low power PFC applications [19]. It has been reported [30-34] that power factor as high as 0.98 can be achieved using passive PFC techniques. The following sub-sections discuss a few of the passive PFC circuits.

Inductive filter

Fig 1.1 shows a diode rectifier circuit with an inductor inserted between the output of the rectifier and the capacitor. The inclusion of the inductor results in larger conduction angle of the current pulse and reduced peak and r.m.s values. For low values of inductance the input current is discontinuous and pulsating. However, it is shown [36] that even for infinite value of the inductance; the PF cannot exceed 0.9 for this kind of arrangement.

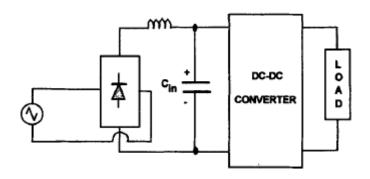


Fig 1.1: Conventional rectifier circuit with inductive filter [15]

In the scheme shown in Fig 1.2, a small filter capacitor Cs is connected across the input terminals of the circuit. The line inductance (not shown in Fig 1.2) and Cs forms the first stage LC filter. Therefore higher order harmonics of the line frequency will undergo greater attenuation (typically 80 dB) resulting in better harmonic performance. It is reported in [35] that for a relatively small value of the inductance; PF of 0.86 is attainable which is a considerable improvement over the no- capacitance case.

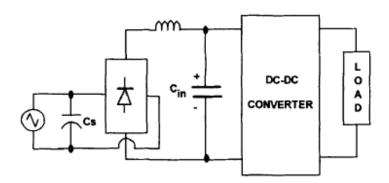


Fig 1.2: Rectifier circuit with input capacitance Cs [15]

Resonant input filter

Fig 1.3 shows the series filter arrangement for power factor correction [28-31], which results in good power factors as high as 0.94. Thus, harmonic performance is also good. This circuit arrangement is popularly used in applications where the supply frequency is high. The disadvantage with this type of arrangement is the use of large size of elements and large r.m.s currents in filter capacitors.

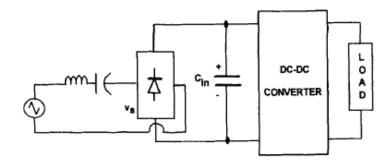


Fig 1.3: Rectifier circuit with series resonant input filter [15]

Some researchers [13] [6], suggest the use of parallel resonant filter (Fig 1.4) for PF improvement. With this arrangement power factor close to 0.95 is achievable. The filter is tuned to offer high impedance to the third harmonic component (the most predominant). The high value parallel resistor is added to damp out circuit oscillations.

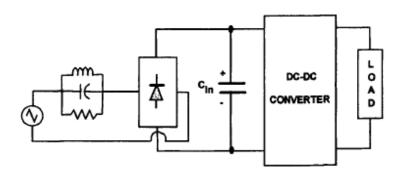


Fig 1.4: Rectifier with parallel resonant filter [15]

Active power factor correction

The active PFC technique, which involves the shaping of the line current using switching devices such as MOSFETs (metal oxide semiconductor field effect transistors) and IGBTs (insulated gate bipolar junction transistors), is a result of advances in power semiconductor devices and microelectronics.

For low and medium power ranges up to a few kilowatts (<5 kW), MOSFETs are the popular choice for PFC because of their switching speed, ease of driving and

ruggedness. BJTs and more recently IGBTs are used for high voltage medium power applications which MOSFETs are unable to contend with owing to their large on-state resistances.

For achieving good input current wave shaping using active techniques, typically the switching frequency should be at least an order of magnitude greater than 3 kHz (= $50 \times 60 \text{ Hz} = 50 \text{ th}$ harmonic of line frequency). With modern advances in MOSFETs and IGBTs, this is feasible.

One of the recent active power factor correction methods which is briefly discussed in the present work, is the single phase rectifier circuit with switch on AC side for high power factor and low total harmonic distortion proposed in [23]. The topology uses a MOSFET switch on the AC side to provide alternative path for the input current to flow and hence makes it continuous. The rectifier is connected to the ac mains through a combination of inductor and capacitor in series, which keeps the input current smooth and in-phase with the supply voltage. The input filter circuit constitutes a series resonant circuit in which the resonance condition is satisfied to calculate the inductance and capacitance values.

1.2 Objective of the thesis

The objective of the thesis with specific aims is as follows:

- a) To study conventional switch mode single phase AC-DC converter topologies at the input side of the rectifier including SEPIC, Inverse SEPIC and ZETA topologies for AC-DC conversion with high input PF, low input current THD and high efficiency,
- b) To improve the total harmonic distortion (THD) of single phase rectifiers using switch mode topologies of Buck, Boost, Buck-Boost, Ćuk, SEPIC, Inverse SEPIC and ZETA converters at the input side of the rectifiers,
- c) Power factor (PF) improvement of the rectifier circuits and
- d) High efficiency.

The possible outcomes may be as follows:

- a) Input current of controlled single phase rectifiers will be nearly sinusoidal and will be in phase with input voltage.
- b) Absolute front end bridge configuration will be replaced so that benefits will come in handy such as low conduction and switching losses and so on.
- c) High performance will be achieved i.e. high PF and efficiency as well as low THD.

1.3 Thesis outline

The new methodology of the single phase rectifiers is based on the fact that switching in the output section of the rectifier may be replaced by the input section switching. It is known that passive PFC techniques are not efficient and economic solution to single phase input current shaping and PF correction. To take advantage of the active PFC techniques, input current switching can offer good performance. Six different configurations have been studied and the results are compared to the conventional active PFC techniques in this thesis.

Chapter-2 contains introduction of single phase rectifiers and describes the necessity of the power factor correction schemes.

Chapter-3 contains introduction of DC-DC converters and describes their applications in various power factor correction schemes.

Chapter-4 deals with the work of this thesis. It presents the study and description of proposed input switched AC-DC converters at constant switching frequency. The analysis of six different converters with input filter and switching states are given. Simulated results, wave shapes and graphical representations are included in this chapter.

Chapter-5 concludes the thesis with conclusion, summary and suggestion on future works.

CHAPTER 2

SINGLE PHASE UNCONTROLLED AC-DC CONVERTERS

AC-DC converters are commonly known as rectifiers. A rectifier converts AC to DC. The purpose of a rectifier may be to produce an output that is DC, or the purpose may be to produce a voltage or current waveform that has a specific DC component. Single Phase Rectifiers are of two kinds:

- Half wave rectifier
- Full wave rectifier

Each of these rectifiers can either be uncontrolled or controlled by SCR, IGBT or by power semiconductor switches. In practice, the half-wave rectifier is used most often in low power applications because the average current in the supply will not be zero, and nonzero average current may cause problems in supply performance due to magnetic saturation.

2.1 Half Wave Rectifier

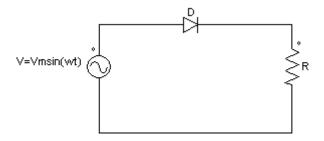


Fig 2.1: Half wave rectifier

A basic half-wave rectifier with a resistive load is shown in Fig. 2.1. The source is AC, and the objective is to create a load voltage which has a nonzero DC component [27]. The diode is a basic electronic switch that allows current in one direction. For the positive half cycle of the source in this circuit, the diode is on (forward biased). Considering the diode to be ideal, the voltage across a forward-biased diode is zero and the current is positive. For the negative half cycle of the source, the diode is

reverse-biased, making the current zero. The voltage across the reverse biased diode is the source voltage, which has a negative value.

Output Voltage,
$$V_o = V_m / \pi$$

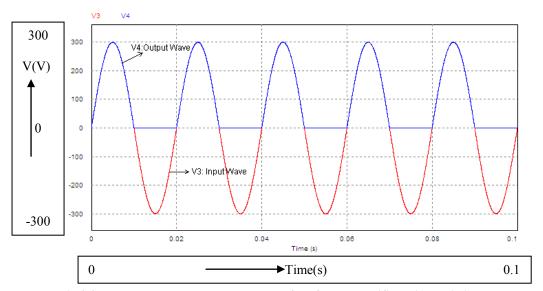


Fig 2.2: Input and output voltage wave of half-wave rectifier with resistive load

The dc component of the current for the purely resistive load is

$$I = V_o/R = V_m/\pi R$$

When the voltage and current are half-wave rectified sine waves then

$$V_{rms} = V_m/2$$

$$I_{rms} = V_m/2R$$

The voltage waveforms across the source and load are shown in Fig. 2.2

2.2 Full Wave Rectifier

The objective of a full-wave rectifier is to produce a voltage or current which is dc or has some specified dc component. While the purpose of the full-wave rectifier is basically the same as that of the half-wave rectifier, full wave rectifiers have some advantages. The average current in the AC source is zero in the full-wave rectifier, thus avoiding problems associated with nonzero average source current, particularly

in transformers. The output of the full-wave rectifier has inherently less ripple than the half-wave rectifier.

Full wave rectifiers may be of two configurations: [29]

- Bridge rectifier
- Center-tapped transformer rectifier

A basic full-wave bridge rectifier with a resistive load is shown in Fig. 2.3. The dc component of the output voltage is the average value, and the load current is simply the resistor voltage divided by resistance:

Output Voltage,
$$V_o = 2V_m/\pi$$

Load current,
$$I_0 = V_0/R = 2V_m/\pi R$$

RMS Source current=RMS Load current= I_{rms} = $I_m/\sqrt{2}$

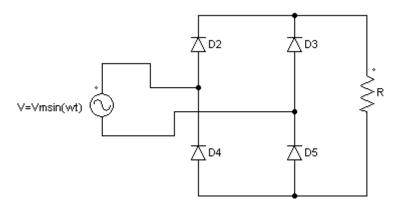


Fig 2.3: Full wave bridge rectifier

The source current for the full-wave rectifier with a resistive load is a sinusoid which is in phase with the voltage, so the power factor is 1. The average source current is zero. The fundamental frequency of the output voltage is 2ω , where ω is the frequency of the AC input, since two periods of the output occur for every period of the input. The Fourier series of the output consists of a DC term and the even harmonics of the source frequency. The voltage waveforms across the source and load are shown in Fig. 2.4.

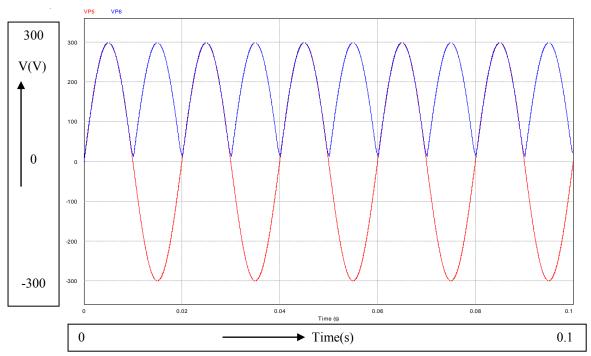


Fig 2.4: Input and output wave of full-wave rectifier with resistive load

Placing a large capacitor in parallel with a resistive load can produce an output voltage that is essentially DC (Fig. 2.5). In the full-wave rectifier circuit, the time that the capacitor discharges is smaller than for the half-wave circuit with a capacitor because of the rectified sine wave in the second half of each period. The output voltage ripple for the full wave rectifier is approximately one-half that of the half-wave rectifier. The peak output voltage will be less in the full wave circuit because there are two diode voltage drops rather than one.

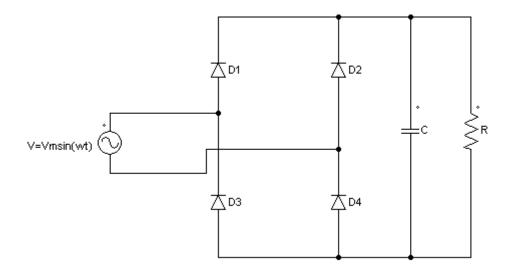


Figure 2.5: Full wave rectifier with capacitor at the output

The value of the capacitor can be calculated from the design constraints.

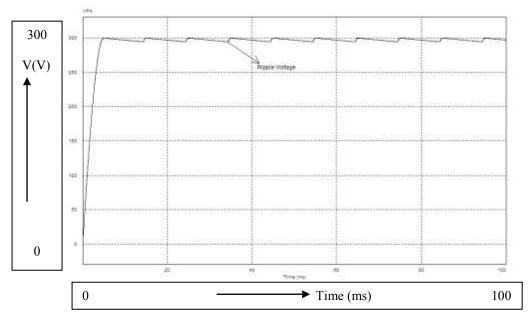


Fig 2.6: Ripple voltage of full wave rectifier with capacitor at the output

The ripple voltage is calculated as peak-to-peak ripple voltage, $\Delta V_o = V_m \pi/\omega RC$. An example of output ripple voltage is shown in Fig. 2.6.

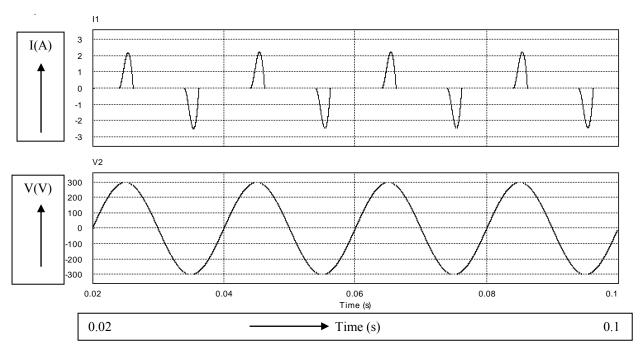


Fig 2.7: Input voltage and input current shapes of full wave rectifier

Input voltage (V2 in Fig. 2.7) and input current (I1 in Fig. 2.7) reveal the problem of supply interface due to discontinuous current pulses. Input Power Factor is found to be very poor (<0.6). Input current THD is also found to be very high (>140%). Efficiency is also very low (<60%). Therefore the power quality is very poor.

CHAPTER 3

DC-DC CONVERTERS

3.1 Basics of DC-DC Converters

The DC-DC converters are used in regulated switch-mode DC power supplies and in DC motor drive applications. As shown in Fig.3.1, the input to these is unregulated DC voltage, which is obtained by rectifying the line voltage, and therefore it will fluctuate due to changes in the line-voltage magnitude. Switch-mode DC-to-DC converters are used to convert the unregulated DC input into a controlled dc output at a desired voltage level.

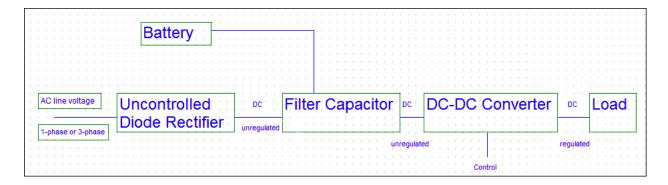


Fig 3.1: A DC-DC converter

The converters are analyzed in steady state. The switches are treated as being ideal, and the losses in the inductive and capacitive elements are neglected. The DC input voltage to the converters is assumed to have zero internal impedance. In DC-DC converters, the average DC output voltage must be controlled to a desired level despite fluctuation of the input voltage and output load. Switch-mode DC-DC converters utilize one or more switches to transform DC from one level to another. In a DC-DC converter with a given input voltage, the average output voltage is controlled by controlling the switch on and off (Ton and Toff) durations. In this method, called pulse-width modulation (PWM) switching, the switch duty ratio D, which is defined as the ratio of the on duration to the switching time period, is varied.

Duty Cycle,
$$D = T_{on}/T$$

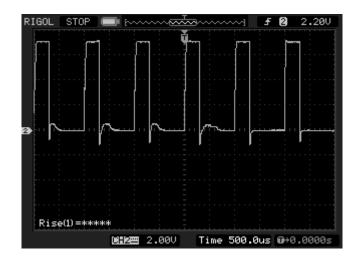


Fig 3.2: PWM signal generated by microprocessor

A typical PWM generated signal is shown in Fig.3.2. A constant switching frequency, f, in a PWM control is chosen to be in a few kHz to a few hundred kHz.

The dc-dc converters can have two distinct modes of operation:

- Continuous Current Mode(CCM)
- Discontinuous Current Mode(DCM)

In practice, a converter may operate in both modes, which have significantly different characteristics. Therefore, a converter and its control should be designed based on both modes of operation. We assume continuous current mode in all cases.

3.2 Types of DC-DC Converters

There are different types of DC-DC converters. Among these following are the common,

- 1. Buck Converter,
- 2. Boost Converter,
- 3. Buck-Boost Converter,
- 4. Ćuk Converter,
- 5. SEPIC Converter and
- 6. Inverse SEPIC Converter.

Of these six converters, only the buck (step-down) and the boost (step-up) are the basic converter topologies. Buck-Boost, Ćuk, SEPIC and Inverse SEPIC are different combination of these two basic topologies.

3.2.1 Buck Converter

As the name implies, a step-down converter produces a lower average output voltage, V_o than the dc input voltage V_{in} . The ideal input-output voltage and current relationships with the duty cycle are given by:

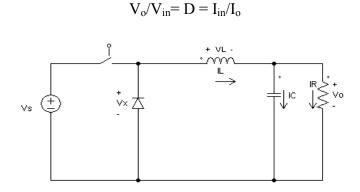


Fig 3.3: Buck DC-DC Converter

Equivalent for switch closed:

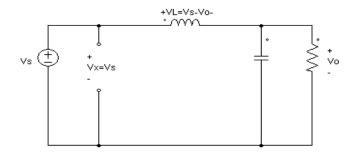


Fig 3.4: Buck converter of the circuit of Fig. 3.3 with switch ON

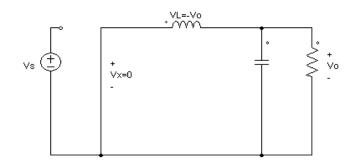


Fig 3.5: Buck converter of the circuit of Fig. 3.3 with switch OFF

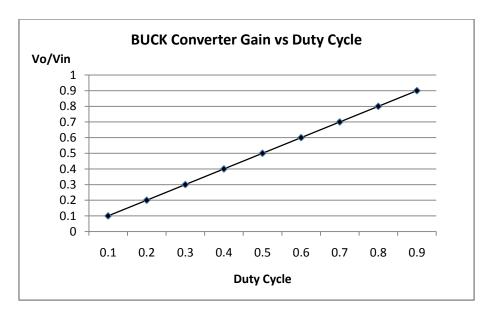


Fig 3.6: Buck converter gain vs duty cycle

3.2.2 Boost Converter

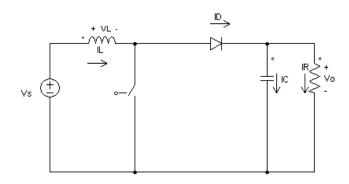


Fig 3.7: Boost DC-DC Converter

As the name implies, the output voltage is always greater than the input voltage. When the switch is on, the diode is reversed biased, thus isolating the output stage. The input supplies energy to the inductor. When the switch is off, the output stage receives energy from the inductor as well as from the input. In steady-state analysis, the output filter capacitor is assumed to be very large to ensure a constant output voltage, V_0 . The ideal input-output relation is given by:

$$V_o/V_{in} = 1/(1-D) = I_{in}/I_o$$

Boost converters are the most commonly used DC-DC converters in PFC techniques.

Equivalent for switch closed:

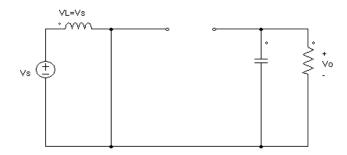


Fig 3.8: Boost converter of the circuit of Fig. 3.7 with switch ON

Equivalent for switch open:

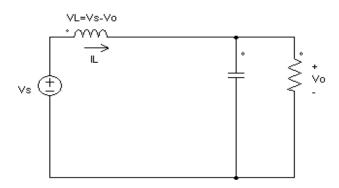


Fig 3.9: Boost converter of the circuit of Fig. 3.7 with switch OFF

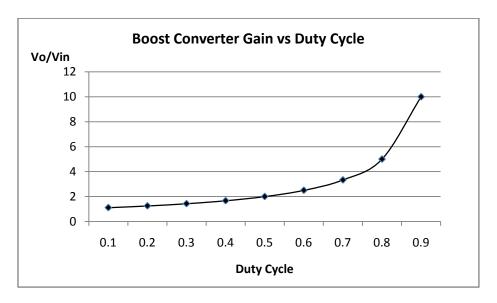


Fig 3.10: Boost converter gain vs. duty cycle

3.2.3 Buck-Boost Converter

A buck-boost converter can be obtained by the cascaded connection of the two basic converters: the step-down and the step-up converter. It inherits pulsating input current of buck and pulsating output current of boost. The ideal output-to-input voltage conversion ratio is given by:

$$V_o/V_{in} = D/(1-D) = I_{in}/I_o$$

This allows the output voltage to be higher or lower than the input voltage, based on the duty ratio, D. D<0.5 ensures buck operation and D>0.5 ensures boost operation.

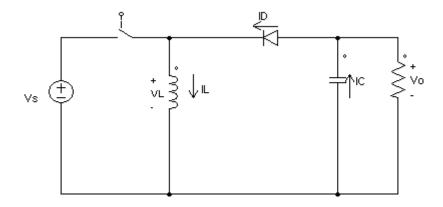


Fig 3.11: Buck-Boost DC-DC Converter

Equivalent for switch closed:

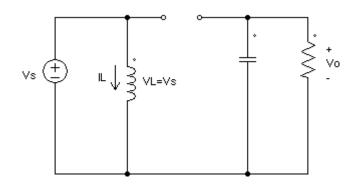


Fig 3.12: Buck-Boost converter of the circuit of Fig. 3.11 with switch ON

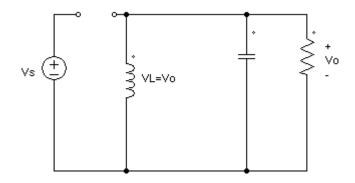


Fig 3.13: Buck-Boost converter of the circuit of Fig. 3.11 with switch OFF

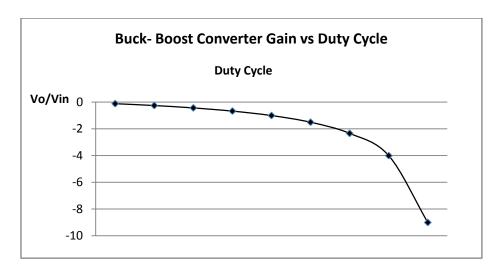


Fig 3.14: Buck-Boost converter gain vs. duty cycle

From Fig. 3.14 it is clear that the output voltage is inverted with respect to the input voltage.

3.2.4 Ćuk Converter

Named after its inventor, the Ćuk converter is shown in Fig.3.15. This converter is obtained by using the duality principle on the circuit of a buck-boost converter, discussed in the previous section. Like buck-boost converter, output voltage is inverted with respect to the input voltage. It has the same ideal voltage and current gain relationship as the Buck-Boost DC-DC converter.

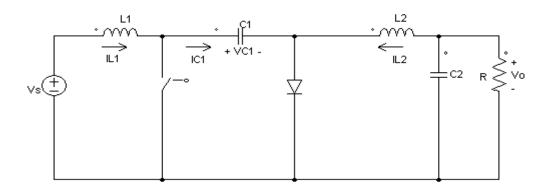


Fig 3.15: Ćuk DC-DC Converter

Equivalent for switch closed:

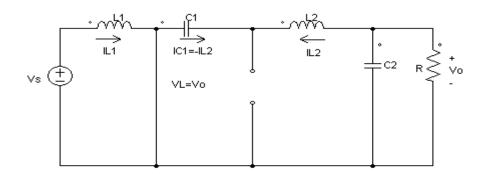


Fig 3.16: Ćuk converter of the circuit of Fig. 3.15 with switch ON

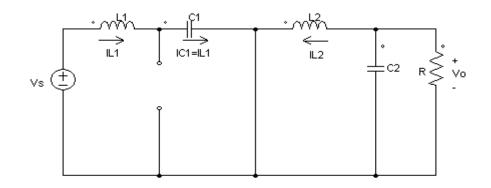


Fig 3.17: Ćuk converter of the circuit of Fig. 3.15 with switch OFF

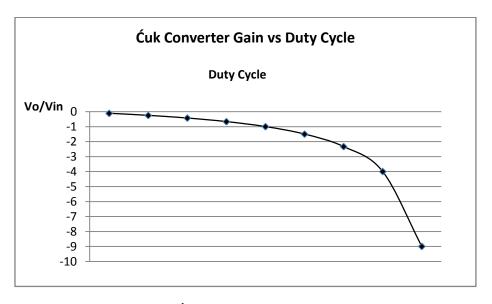


Fig 3.18: Ćuk converter gain vs. duty cycle

3.2.5 SEPIC Converter

Single-ended primary-inductor converter (SEPIC) is a type of DC-DC converter allowing the electrical potential (voltage) at its output to be greater than, less than, or equal to that at its input. The output of the SEPIC is controlled by the duty cycle of the control transistor. A SEPIC is similar to a traditional buck-boost converter, but has advantages of having non-inverted output (the output voltage is of the same polarity as the input voltage), the isolation between its input and output (provided by a capacitor in series). On the other hand, power factor correction converters are extensively used in the industrial life. These converters aim at increasing the power factor and decreasing the total harmonic distortion of the supply current.

Power factor correction and minimization of total harmonic distortion find great interest from researchers [19-21]. The international standards such IEC 61000-3-2 [10] restrict the maximum allowable total harmonic distortion for the current drained from the electric system. A typical SEPIC converter is shown in Fig.3.19. It is a boost incorporated dc-dc converter.

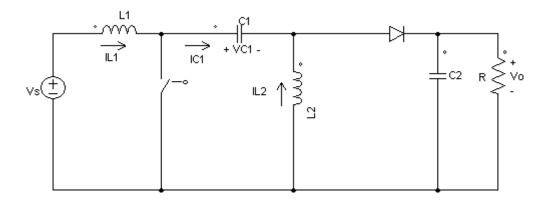


Fig 3.19: SEPIC DC-DC Converter

Equivalent for switch closed:

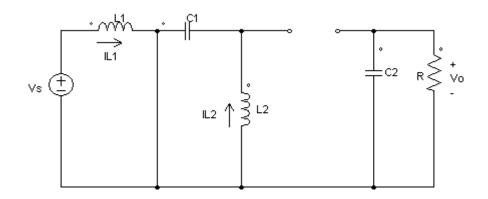


Fig 3.20: SEPIC converter of the circuit of Fig. 3.19 with switch ON

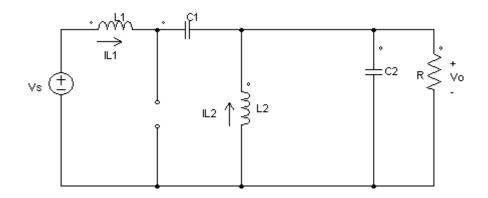


Fig 3.21: SEPIC converter of the circuit of Fig. 3.19 with switch OFF

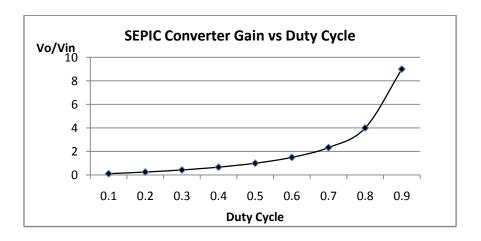


Fig 3.22: SEPIC converter gain vs. duty cycle

3.2.6 Inverse SEPIC Converter

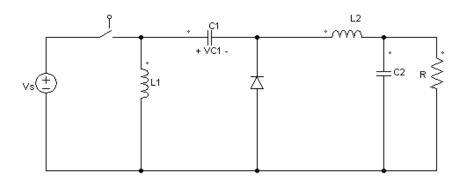


Fig 3.23: Inverse SEPIC DC-DC Converter

The ZETA converter (also known as the inverted SEPIC) offers certain advantages over the classical SEPIC. "Inverse" comes from the fact that if the SEPIC converter is rotated around Y-axis it transforms to this topology. This topology has the same buckboost functionality as the SEPIC, but the output current is continuous, providing a clean, low-ripple output voltage. This low-noise output converter can be used to power certain types of loads, such as LEDs, which are sensitive to the voltage ripple. The ZETA converter offers the same DC isolation between the input and output as the SEPIC converter, and can be used in high-reliability systems. This topology can offer high efficiency, especially if the synchronous rectification is used. The synchronous rectification can be easily implemented here, because this topology, unlike the SEPIC converter, uses a low-side rectifier. Besides, direct DC-DC converters briefly described, transformer coupled fly back and forward DC-DC converters, and other modified DC-DC converters to suit certain applications are also available in literature.

Equivalent for switch closed:

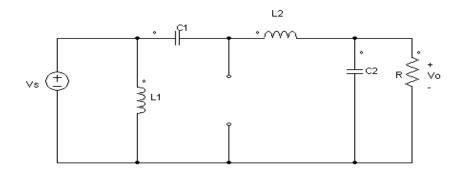


Fig 3.24: Inverse SEPIC converter of the circuit of Fig. 3.23 with switch ON

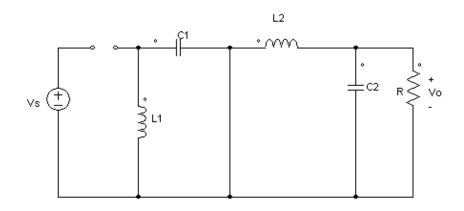


Fig 3.25: Inverse SEPIC converter of the circuit of Fig. 3.23 with switch OFF

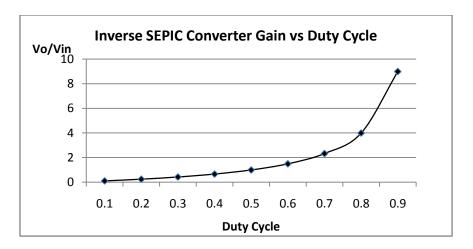


Fig 3.26: Inverse SEPIC converter gain vs. duty cycle

CHAPTER 4

INPUT SWITCHED AC-DC CONVERTERS: PERFORMANCE ANALYSIS

4.1 Single Phase Input Switched Buck AC-DC Converter

A conventional output regulated single phase AC-DC converter with buck topology is shown in Fig.4.1. In conventional PFC circuit, the DC-DC converter is placed between load and the rectifier as shown in Fig 4.1.

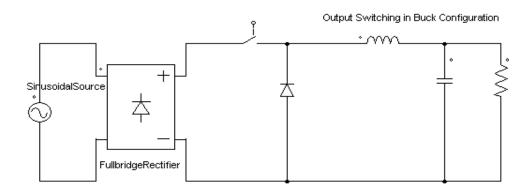


Fig 4.1: The conventional single phase bridge rectifier with output switching in Buck Configuration

The circuit of Fig. 4.2 illustrates the proposed input switched single phase AC-DC converter using Buck topology. The proposed circuit comprises of one inductor, one capacitor, five diodes and a switch Z1. Here L3 works as buck inductor. The circuit is shown without input filter section. The output capacitor (100μ) and load (200Ω) are shown in the output section.

Principle of Operation

Input AC chopping at high frequency provides switched AC current that requires small filter to make it nearly sinusoidal. As a result, the input current THD reduces and the power factor improves. The operating principle of the proposed Buck scheme is described below.

The proposed input switched buck rectifier topology has four operating states as shown in Fig.4.3 to Fig.4.6. Fig.4.3 and Fig.4.4 represent the positive half cycle operation with switch ON and OFF positions, whereas, Fig.4.5 and Fig.4.6 represent the negative half cycle with switch ON and OFF positions respectively.

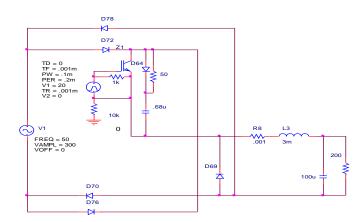


Fig 4.2: The single phase input switched AC-DC converter (Buck Configuration)

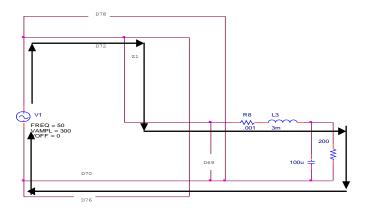


Fig 4.3: Equivalent circuit of the circuit of Fig. 4.2 for positive cycle switch ON

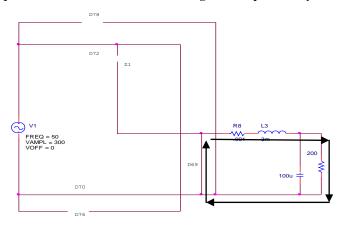


Fig 4.4: Equivalent circuit of the circuit of Fig. 4.2 for positive cycle switch OFF

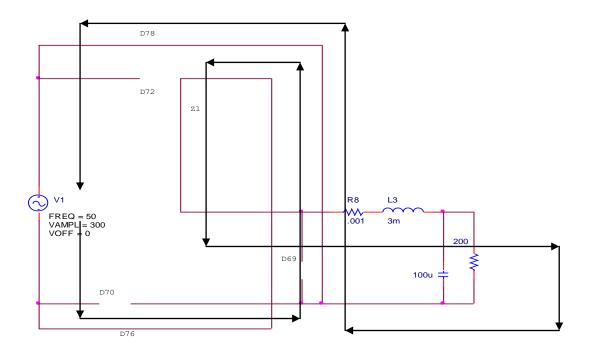


Fig 4.5: Equivalent circuit of the circuit of Fig. 4.2 for negative cycle switch ON

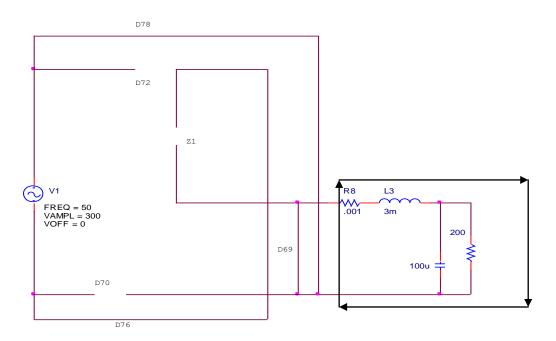


Fig 4.6: Equivalent circuit of the circuit of Fig. 4.2 for negative cycle switch OFF

Typical input current and the output voltage waveforms without any input filter are shown in Fig 4.7 and Fig.4.8 respectively. To maintain output voltage constant at low ripple with nearly sinusoidal input current feedbacks from output, input voltage and buck inductor current to a properly designed controller circuit is necessary. Also, in the case of input switched buck rectifier, proper input filter is also necessary. Table

4.1 and Fig 4.9 show the performance comparison of proposed input switched buck rectifier with conventional output switched buck rectifier in terms of efficiency, line current THD and input power factor with duty cycle variation (without any feedback and input filter). Also, the performance is investigated for load variation. In terms of input current THD and input power factor, the proposed circuit performs better, whereas; in terms of efficiency both have similar performance.

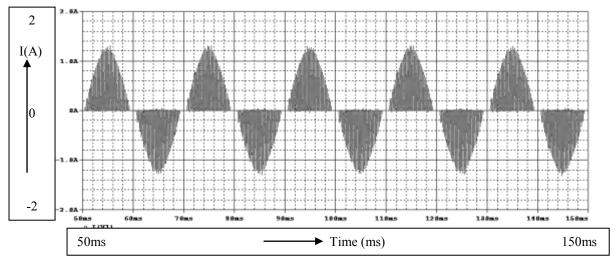


Fig 4.7: Input current shape of the proposed input switched buck configuration circuit of Fig. 4.2, (without input filter)

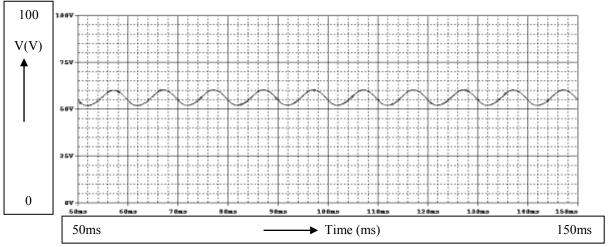
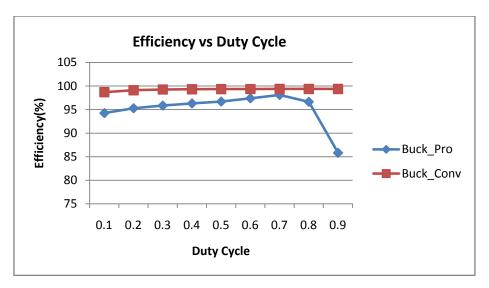
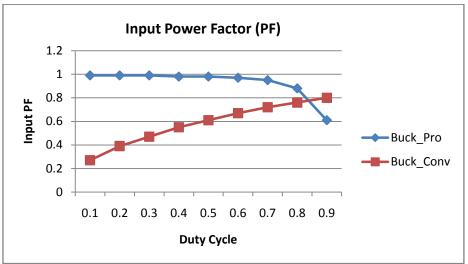


Fig 4.8: Output voltage wave shape of the proposed input switched buck configuration circuit of Fig. 4.2, (without input filter)

Table 4.1: Performance Comparison of Proposed and Conventional Buck Topology Based Rectifier for Duty Cycle Variation

Duty	Efficiency, n(%)		Input Power Factor (PF)		THD (%)	
Cycle	Proposed	Conventional	Proposed	Conventional	Proposed	Conventional
D	Buck	Buck	Buck	Buck	Buck	Buck
	Topology	Topology	Topology	Topology	Topology	Topology
0.1	94.25	98.68	0.99	0.27	7.78	351
0.2	95.28	99.10	0.99	0.39	7.42	237
0.3	95.85	99.24	0.99	0.47	7.34	184
0.4	96.31	99.30	0.98	0.55	7.43	151
0.5	96.70	99.33	0.98	0.61	7.47	127
0.6	97.39	99.35	0.97	0.67	7.51	109
0.7	98.10	99.36	0.95	0.72	7.41	95
0.8	96.65	99.37	0.88	0.76	6.67	83
0.9	85.81	99.37	0.61	0.80	14.18	74





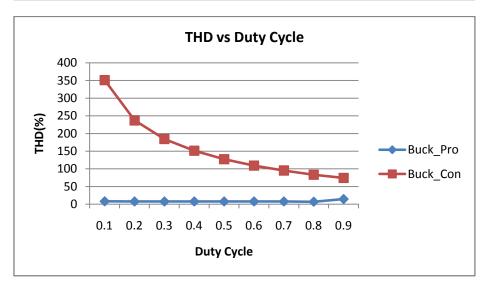
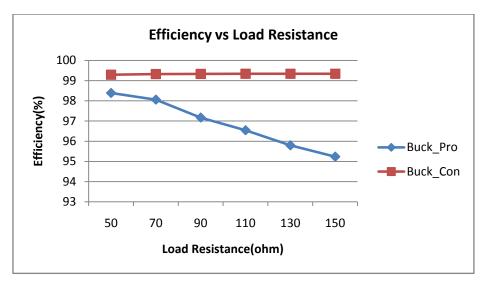
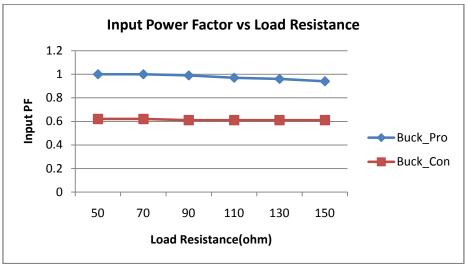


Fig 4.9: Efficiency, Input PF and THD vs. duty cycle of input switched Buck AC-DC converter

Table 4.2: Performance Comparison of Proposed and Conventional Buck Topology Based Rectifier for Load Variation

Load Resistance,	Efficiency, n(%)		Input Power Factor (PF)		THD (%)	
	Proposed	Conventional	Proposed	Conventional	Proposed	Conventional
	Buck	Buck	Buck	Buck	Buck	Buck
$RL(\Omega)$	Topology	Topology	Topology	Topology	Topology	Topology
50	98.39	99.29	1.00	0.62	5.20	128
70	98.06	99.32	1.00	0.62	5.95	127
90	97.17	99.33	0.99	0.61	6.79	127
110	96.54	99.34	0.97	0.61	8.06	127
130	95.79	99.34	0.96	0.61	8.28	127
150	95.23	99.34	0.94	0.61	8.78	127





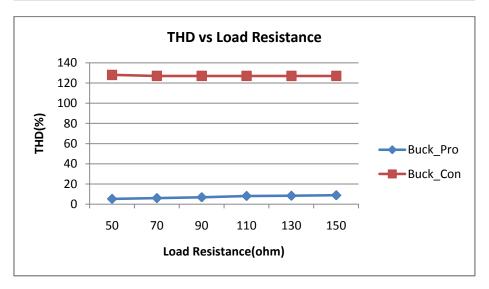


Fig 4.10: Efficiency, Input PF and THD vs. Load Resistance of input switched Buck AC-DC converter

4.2 Single Phase Input Switched Boost AC-DC Converter

A conventional output regulated single phase AC-DC converter with boost topology is shown in Fig.4.11:

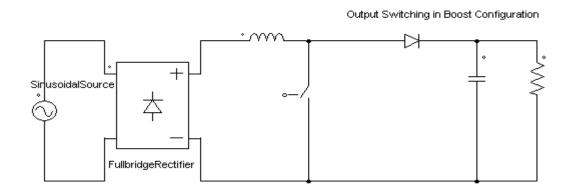


Fig 4.11: The conventional bridge rectifier with output switching in Boost configuration

In the boost-regulated AC-DC conversion, the boost rectifier should be operated in critical mode [4-6] where, the power switch should be turned ON at the instant of zero current in the boost diode. This needs variable switching frequency operation of the DC-DC converter as the load or the input voltage changes. Another approach for boost-regulated rectifier involves controlling to a constant level the average current of the boost diode [11-13]. In order to keep the average current constant through the boost diode, the duty cycle must be modulated over the line cycle. Bridge-less configurations [14-15] and two-diode, two-switch rectifiers [21-25] are also reported in literatures for AC-DC conversion having the above features of boost-regulated rectifier.

4.2.1 Input Switched Boost AC-DC Converter-Configuration 1

The boost circuit illustrated in Fig 4.12 differ from the mentioned output DC-DC converter regulated rectifiers or bridgeless rectifiers in two senses. Firstly, it uses a single bidirectional switch. Secondly, because of input current switching it ensures input AC current to be in phase with input voltage where there is no output filter. This would result shaping of input current to near sinusoid by use of small filter and will ensure good input power factor without having much impacts of output filter,

input voltage and change of load. The proposed boost AC- DC converter provides step-up output dc voltage with the duty cycle control of the switch. The efficiency is variable with the change in duty cycle.

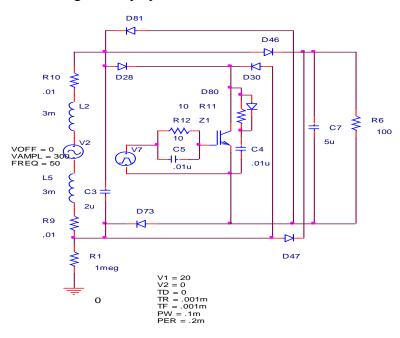


Fig 4.12: The single phase input switched AC-DC converter (Boost Configuration 1)

The boost topology has four operating states as shown in Fig.4.13 to Fig.4.16. Fig.4.13 and Fig.4.14 represent the positive half cycle operation with switch ON and OFF positions, whereas, Fig.4.15 and Fig.4.16 represent the negative half cycle with switch ON and OFF positions respectively.

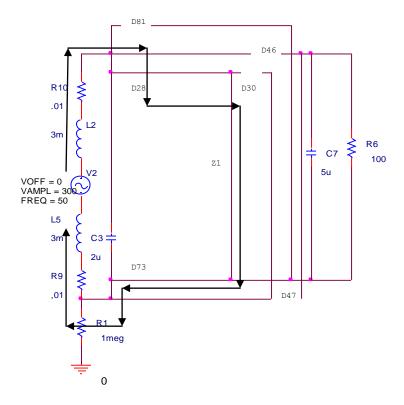


Fig 4.13: Equivalent circuit of the circuit of Fig. 4.12 for positive cycle switch ON

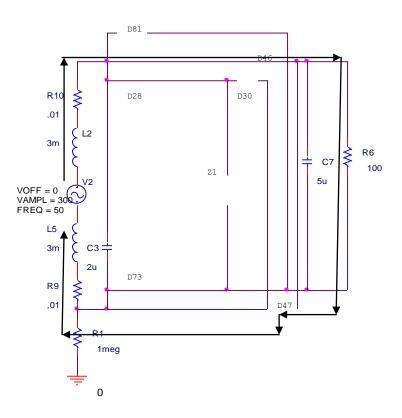


Fig 4.14: Equivalent circuit of the circuit of Fig. 4.12 for positive cycle switch OFF

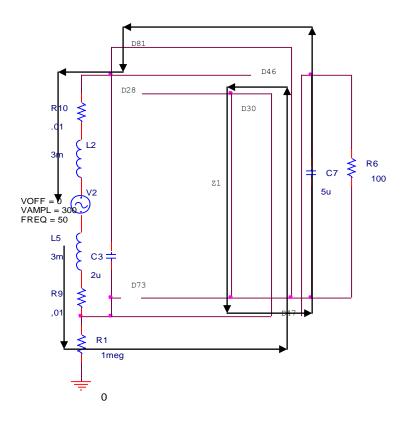


Fig 4.15: Equivalent circuit of the circuit of Fig. 4.12 for negative cycle switch ON

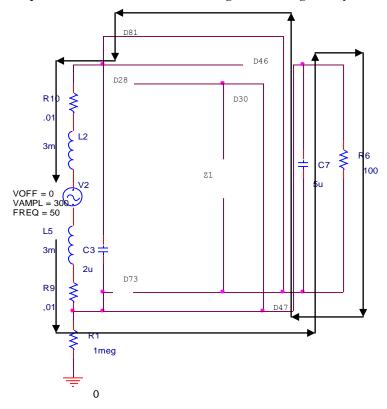


Fig 4.16: Equivalent circuit of the circuit of Fig. 4.12 for negative cycle switch OFF

Typical input current and the output voltage waveforms without any input filter are shown in Fig 4.17 and Fig.4.18 respectively. To maintain output voltage constant at low ripple with nearly sinusoidal input current feedbacks from output, input voltage and boost inductor current to a properly designed controller circuit is necessary. Also, in the case of input switched boost rectifier, proper input filter is also necessary. Table 4.3 and Fig 4.19 show the performance comparison of proposed input switched boost rectifier with conventional output switched boost rectifier in terms of efficiency, line current THD and input power factor with duty cycle variation (without any feedback and input filter). Also, the performance is investigated for load variation. In terms of input current THD and input power factor, the proposed circuit performs better, whereas; in terms of efficiency both have similar performance.

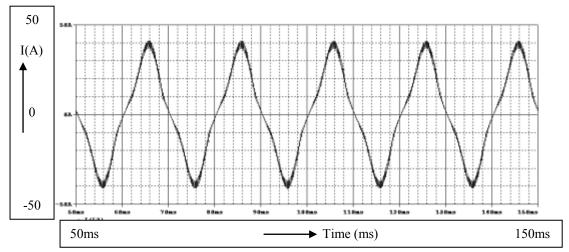


Fig 4.17: Input current shape of the proposed input switched boost configuration 1 circuit of Fig. 4.12

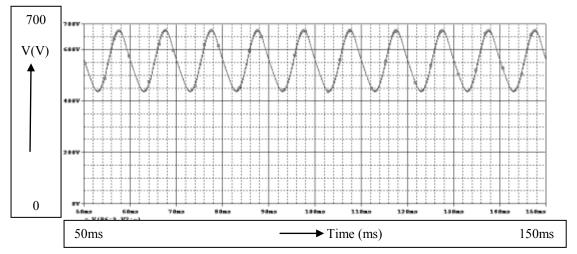
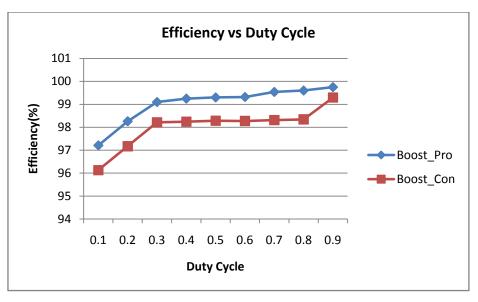
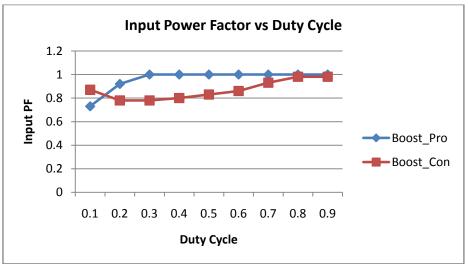


Fig 4.18: Output voltage wave shape of the proposed input switched boost configuration 1 circuit of Fig. 4.12

Table 4.3: Performance Comparison of Proposed and Conventional Boost Topology Based Rectifier Configuration 1 for Duty Cycle Variation

Dut	Efficiency, n (%)		Input Power Factor (PF)		THD (%)	
y						
Cyc	Proposed	Convention	Proposed	Convention	Proposed	Convention
le	Boost	al Boost	Boost	al Boost	Boost	al Boost
D	Topology	Topology	Topology	Topology	Topology	Topology
0.1	97.21	96.13	0.73	0.87	0.34	53.10
0.2	98.26	97.17	0.92	0.78	1.03	80.23
0.3	99.10	98.21	1.00	0.78	1.83	81.94
0.4	99.25	98.24	1.00	0.80	2.72	76.01
0.5	99.30	98.28	1.00	0.83	3.61	67.62
0.6	99.32	98.27	1.00	0.86	4.66	57.82
0.7	99.54	98.31	1.00	0.93	5.68	39.11
0.8	99.60	98.34	1.00	0.98	5.65	19.90
0.9	99.75	99.29	1.00	0.98	4.98	8.74





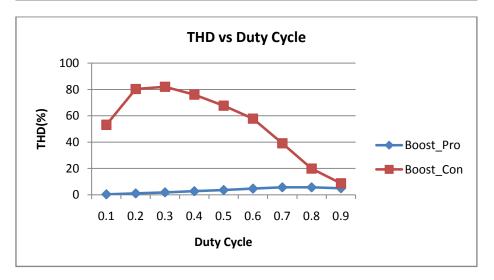
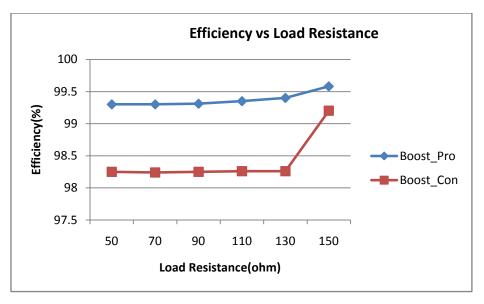
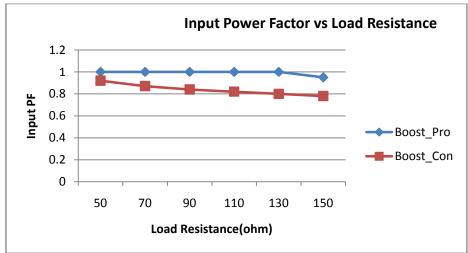


Fig 4.19: Efficiency, Input PF and THD vs. Duty Cycle of input switched boost AC-DC converter-configuration 1

Table 4.4: Performance Comparison of Proposed and Conventional Boost Topology Based Rectifier Configuration 1 for Load Variation

Load Resistance, RL (Ω)	Efficiency, n(%)		Input Power Factor (PF)		THD (%)	
	Proposed	Conventional	Proposed	Conventional	Proposed	Conventional
	Boost	Boost	Boost	Boost	Boost	Boost
KL (\$2)	Topology	Topology	Topology	Topology	Topology	Topology
50	99.30	98.25	1.00	0.92	2.50	40.88
70	99.30	98.24	1.00	0.87	3.04	55.79
90	99.31	98.25	1.00	0.84	3.46	64.52
110	99.35	98.26	1.00	0.82	3.73	70.26
130	99.40	98.26	1.00	0.80	4.06	74.54
150	99.58	99.20	0.95	0.78	4.37	77.93





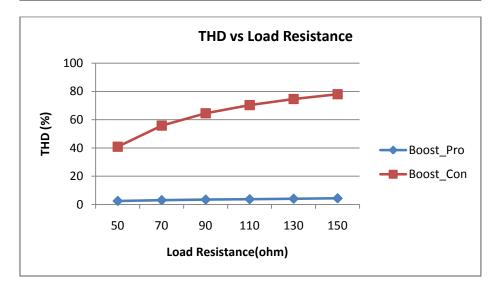


Fig 4.20: Efficiency, Input PF and THD vs. Load Resistance of input switched boost AC-DC converter-configuration 1

4.2.2 Single Phase Input Switched Boost AC-DC Converter-Configuration 2

A second possible input switched boost AC-DC converter consisting of an input bidirectional switch and an output rectifier is shown in Fig. 4.21.

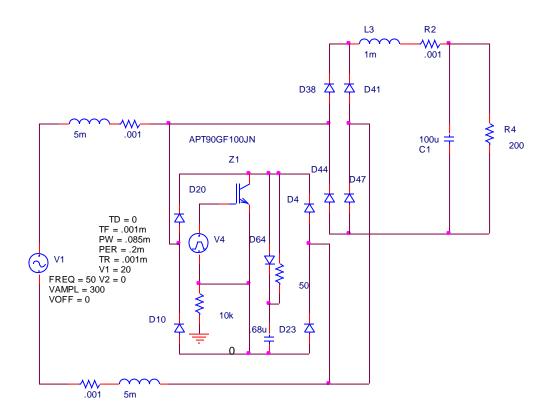


Fig 4.21: The single phase input switched AC-DC converter (Boost Configuration 2)

Four modes of operation of circuit of Fig. 4.21 are illustrated in Fig.4.22 to Fig.4.25. Fig 4.22 and Fig.4.23 are the circuit configurations for positive supply cycle for switch ON and OFF modes respectively. Fig. 4.24 and Fig.4.25 are the circuit configurations for negative supply cycle for switch ON and OFF modes respectively.

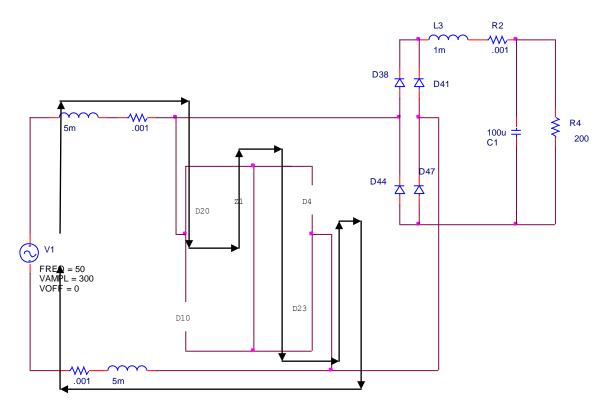


Fig 4.22: Equivalent circuit of the circuit of Fig.4.21 for positive cycle switch ON

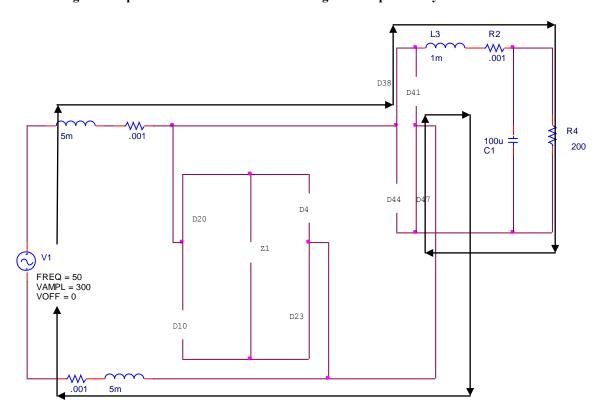


Fig 4.23: Equivalent circuit of the circuit of Fig.4.21 for positive cycle switch OFF

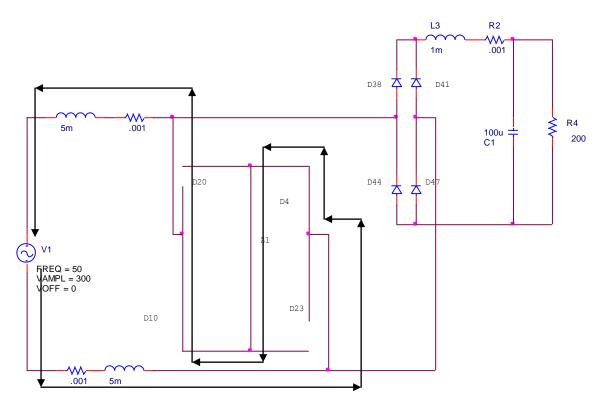


Fig 4.24: Equivalent circuit of the circuit of Fig.4.21 for negative cycle switch ON

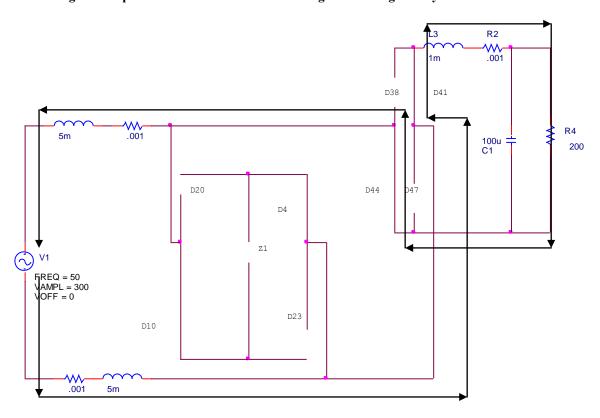


Fig 4.25: Equivalent circuit of the circuit of Fig.4.21 for negative cycle switch OFF

Typical input current and output voltage waveforms of the circuit of Fig.4.21 are shown in Fig.4.26 and Fig.4.27 respectively.

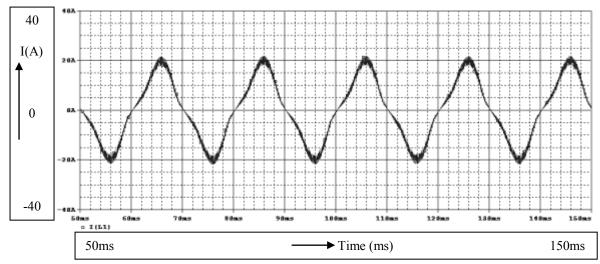


Fig 4.26: Input current shape of the proposed input switched boost configuration 2 circuit of Fig.4.21

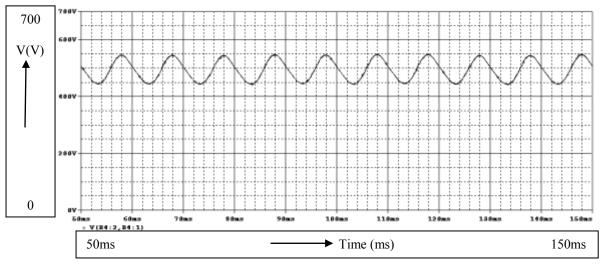
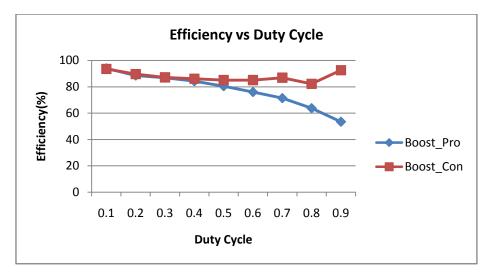


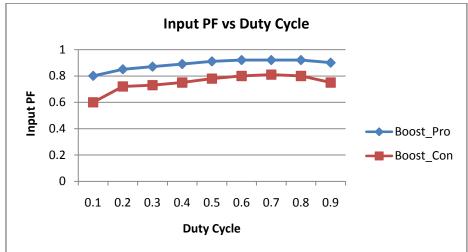
Fig 4.27: Output voltage wave shape of the proposed input switched boost configuration 2 circuit of Fig.4.21

Table 4.5: Performance Comparison of Proposed Input Regulated and Conventional Output Regulated Boost Topology Based Rectifier Configuration 2 for Duty Cycle Variation

Dut	Efficiency, n (%)		Input Power Factor (PF)		THD (%)	
y						
Cyc	Proposed	Convention	Proposed	Convention	Proposed	Convention
le	Boost	al Boost	Boost	al Boost	Boost	al Boost
D	Topology	Topology	Topology	Topology	Topology	Topology
0.1	93.96	93.47	0.80	0.60	73.20	115.00
0.2	88.50	89.60	0.85	0.72	60.83	90.76
0.3	86.78	87.12	0.87	0.73	54.18	90.00
0.4	84.21	86.11	0.89	0.75	47.62	83.12
0.5	80.41	85.06	0.91	0.78	41.00	73.96
0.6	76.00	85.07	0.92	0.80	33.63	63.95
0.7	71.38	86.87	0.92	0.81	25.65	59.34
0.8	63.72	82.23	0.92	0.80	16.15	59.05
0.9	53.47	92.52	0.90	0.75	7.03	41.29

Table 4.5 and Fig 4.28 show the performance comparison of proposed input switched boost rectifier-configuration 2 with conventional output switched boost rectifier in terms of efficiency, line current THD and input power factor with duty cycle variation (without any feedback and input filter). In terms of input current THD and input power factor, the proposed circuit performs better, whereas; in terms of efficiency both have similar performance. It is to be noted that for duty cycle 0.9, the conventional circuit efficiency is very high compared to proposed circuit in Fig. 4.21.





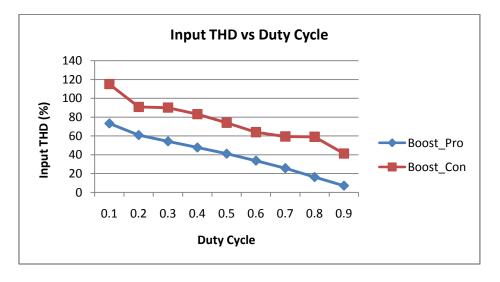


Fig 4.28: Efficiency, Input PF and THD vs. duty cycle of input switched Boost AC-DC converterconfiguration 2

4.3 Single Phase Input Switched Buck-Boost AC-DC Converter

A conventional output regulated AC-DC converter with buck-boost topology is shown in Fig.4.29:

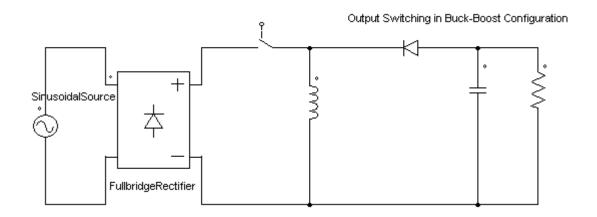


Fig 4.29: The conventional bridge rectifier with output switching in Buck-Boost configuration

4.3.1 Input Switched Buck-Boost AC-DC Converter-Configuration 1

Fig. 4.30 shows the proposed circuit diagram of a single phase switch mode AC-DC converter using the principle of Buck- Boost conversion. The circuit consists of four inductors, three capacitors, six diodes and a switch (Z1). As the given supply voltage is AC, Buck- Boost conversion on both positive and negative cycle of the input voltage is required. L1 and L3 are used as Buck-Boost inductors. The inductor L2 and capacitor C9 form the input filter. C3 and R3 are the output capacitor and load respectively. The buck-boost topology has four operating states as shown in Fig.4.31 to Fig.4.34. Fig.4.31 and Fig.4.32 represent the positive half cycle operation with switch ON and OFF positions, whereas, Fig.4.33 and Fig.4.34 represent the negative half cycle with switch ON and OFF positions respectively.

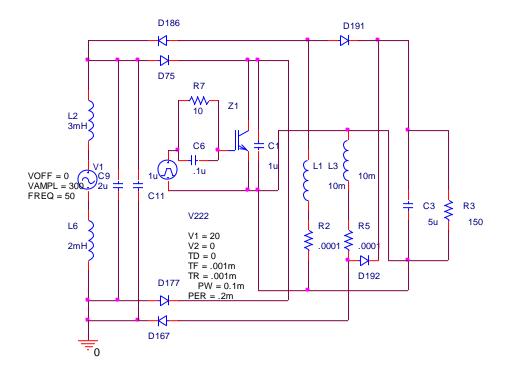


Fig 4.30: The single phase input switched AC-DC converter (Buck-Boost Configuration 1)

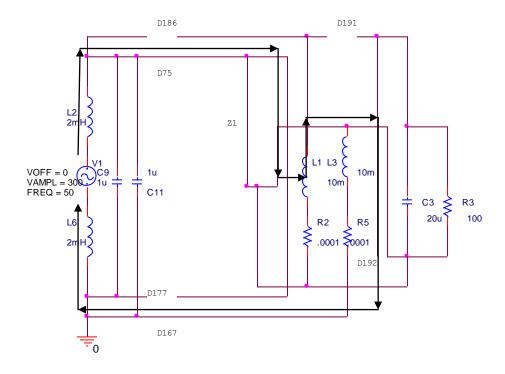


Fig 4.31: Equivalent circuit of the circuit of Fig. 4.30 for positive cycle switch ON

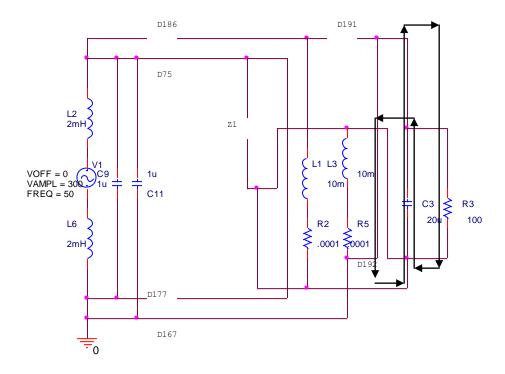


Fig 4.32: Equivalent circuit of the circuit of Fig. 4.30 for positive cycle switch OFF

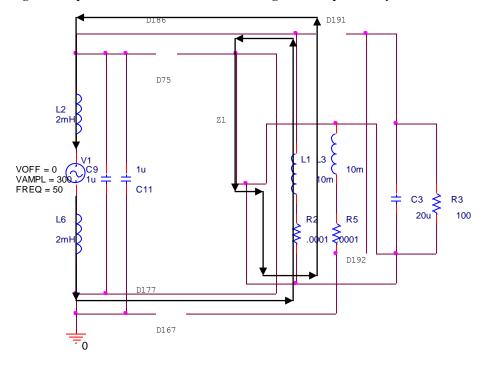


Fig 4.33: Equivalent circuit of the circuit of Fig. 4.30 for negative cycle switch ON

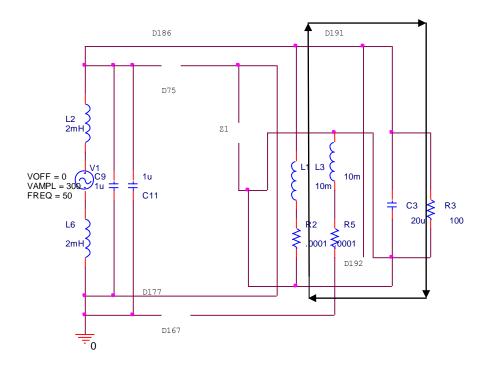


Fig 4.34: Equivalent circuit of the circuit of Fig. 4.30 for negative cycle switch OFF

Fig.4.35 and Fig.4.36 show typical input current and output voltage waveforms of input switched Buck-Boost AC-DC Converter of configuration 1(circuit of Fig.4.30). Table 4.6 and Table 4.7 with Fig. 4.37 present the configuration of output regulated Buck-Boost converter with input switched Buck-Boost AC-DC converter of configuration 1. The input current is in phase with the input voltage which results in lower input current THD.

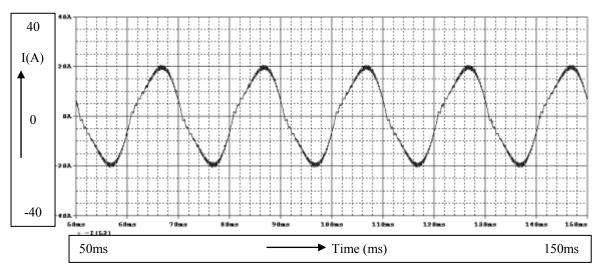


Fig 4.35: Input current shape of the proposed input switched buck-boost configuration-1 circuit of Fig. 4.30

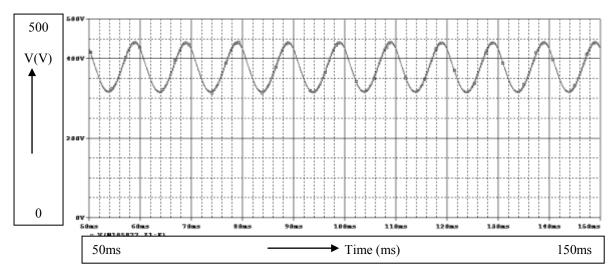
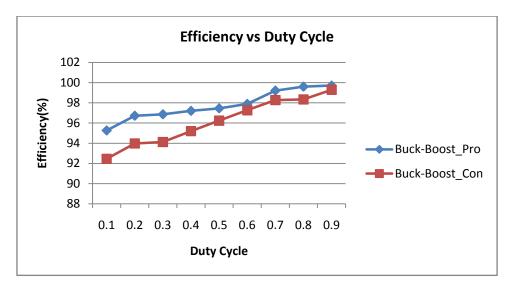
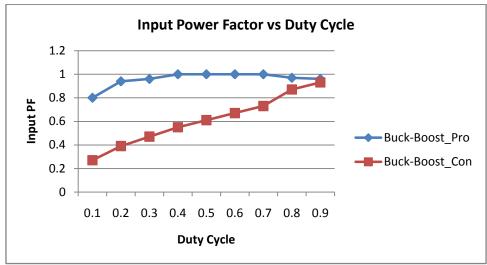


Fig 4.36: Output voltage wave shape of the proposed input switched buck-boost configuration-1 circuit of Fig. 4.30

Table 4.6: Performance Comparison of Proposed and Conventional Buck-Boost Topology Based Rectifier Configuration 1 for Duty Cycle Variation

Dut	Efficiency, n(%)		Input Power Factor (PF)		THD (%)	
y Cy cle D	Proposed Buck- Boost Topology	Convention al Buck- Boost Topology	Proposed Buck- Boost Topology	Convention al Buck- Boost Topology	Proposed Buck- Boost Topology	Convention al Buck- Boost Topology
0.1	95.26	92.45	0.80	0.27	11.54	351.1
0.2	96.72	93.97	0.94	0.39	11.84	238.1
0.3	96.86	94.11	0.96	0.47	8.53	185.6
0.4	97.20	95.19	1.00	0.55	5.05	152.8
0.5	97.45	96.23	1.00	0.61	3.79	129.1
0.6	97.89	97.26	1.00	0.67	3.09	110.6
0.7	99.21	98.27	1.00	0.73	3.15	92.7
0.8	99.60	98.33	0.97	0.87	3.43	57.1
0.9	99.71	99.28	0.96	0.93	5.45	34.7





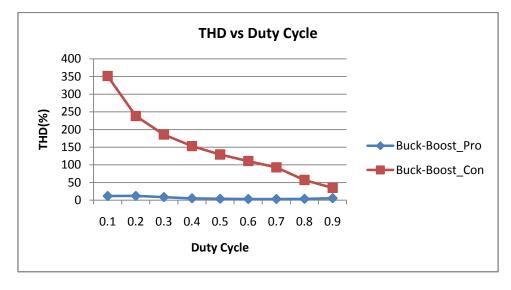
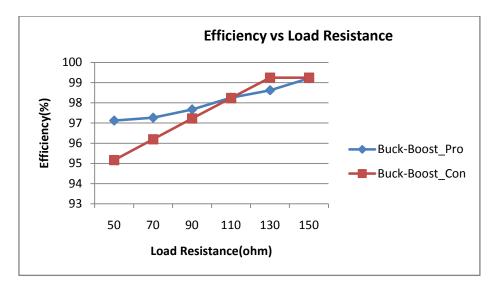
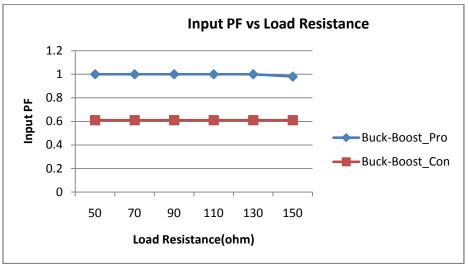


Fig 4.37: Efficiency, Input PF and THD vs. duty cycle of input switched Buck-Boost AC-DC converter-configuration 1

Table 4.7: Performance Comparison of Proposed and Conventional Buck-Boost Topology Based Rectifier Configuration 1 for Load Variation

	Efficiency, n(%)		Input Powe	er Factor (PF)	THD (%)	
Load Resistance, RL (Ω)	Proposed Buck- Boost Topology	Conventional Buck-Boost Topology	Proposed Buck- Boost Topology	Conventional Buck-Boost Topology	Proposed Buck- Boost Topology	Conventional Buck-Boost Topology
50	97.12	95.16	1.00	0.61	5.88	129.1
70	97.26	96.19	1.00	0.61	4.44	129.1
90	97.67	97.22	1.00	0.61	3.99	129.1
110	98.25	98.23	1.00	0.61	3.52	129.1
130	98.62	99.24	1.00	0.61	3.28	129.1
150	99.21	99.24	0.98	0.61	3.25	129.1





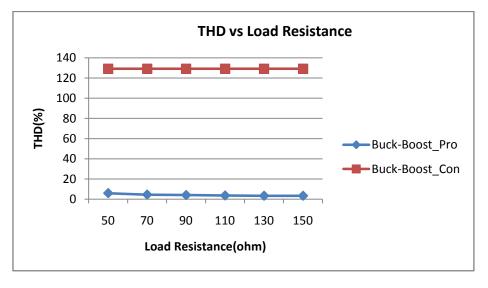


Fig 4.38: Efficiency, Input PF and THD vs. Load Resistance of input switched Buck-Boost AC-DC converter-configuration 1

4.3.2 Single Phase Input Switched Buck-Boost AC-DC Converter-Configuration

The topology has four operating states as shown in Fig.4.40 to Fig.4.43. Fig.4.40 and Fig.4.42 represent the positive half cycle operation with switch ON and OFF positions, whereas, Fig.4.42 and Fig.4.43 represent the negative half cycle with switch ON and OFF positions respectively.

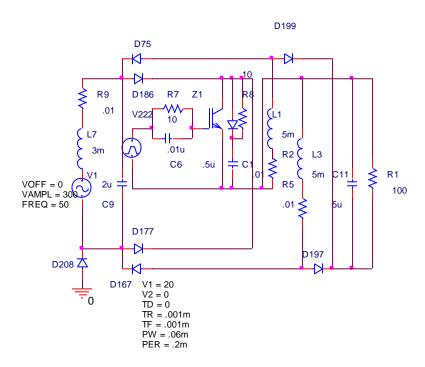


Fig 4.39: The single phase input switched AC-DC converter (Buck-Boost Configuration 2)

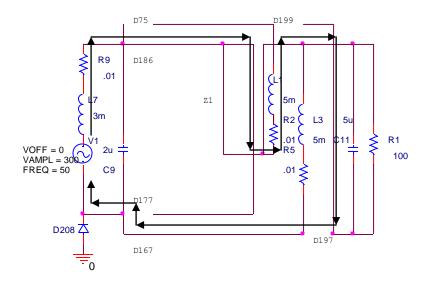


Fig 4.40: Equivalent circuit of the circuit of Fig.4.39 for positive cycle switch ON

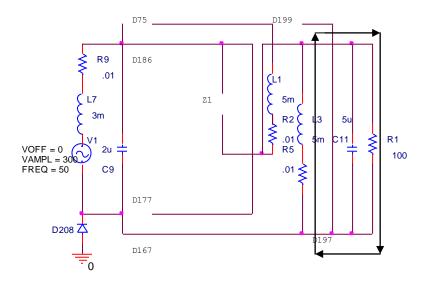


Fig 4.41: Equivalent circuit of the circuit of Fig.4.39 for positive cycle switch OFF

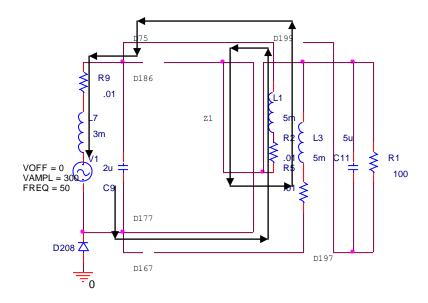


Fig 4.42: Equivalent circuit of the circuit of Fig.4.39 for negative cycle switch ON

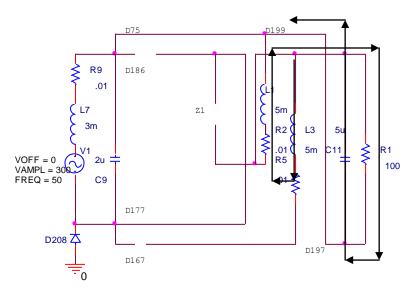


Fig 4.43: Equivalent circuit of the circuit of Fig.4.39 for negative cycle switch OFF

Typical input current and output voltage waveforms of circuit of Fig. 4.39 are shown in Fig. 4.44 and Fig. 4.45 respectively.

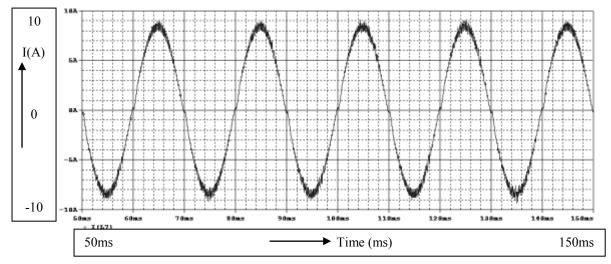


Fig 4.44: Input current shape of the proposed input switched Buck-Boost configuration-2 circuit of Fig. 4.39

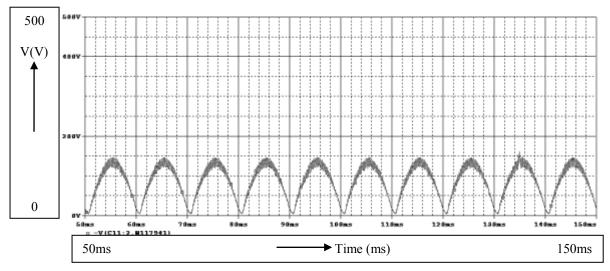
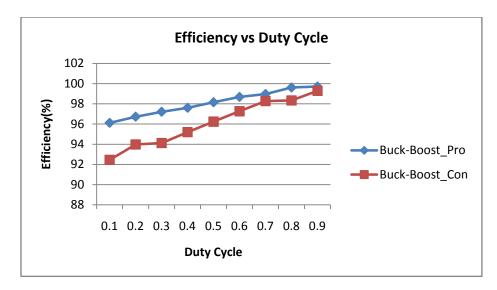
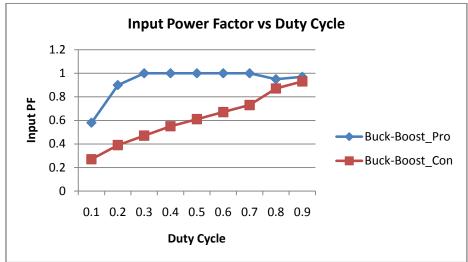


Fig 4.45: Output voltage wave shape of the proposed input switched Buck-Boost configuration-2 circuit of Fig. 4.39

Table 4.8: Performance Comparison of Proposed and Conventional Buck-Boost Topology Based Rectifier Configuration 2 for Duty Cycle Variation

Dut	Efficiency, n(%)		Input Power Factor (PF)		THD (%)	
у	Proposed	Convention	Proposed	Convention	Proposed	Convention
Су	Buck-	al Buck-	Buck-	al Buck-	Buck-	al Buck-
cle	Boost	Boost	Boost	Boost	Boost	Boost
D	Topology	Topology	Topology	Topology	Topology	Topology
0.1	96.11	92.45	0.58	0.27	10.64	351.1
0.2	96.72	93.97	0.90	0.39	9.77	238.1
0.3	97.21	94.11	1.00	0.47	7.80	185.6
0.4	97.60	95.19	1.00	0.55	5.12	152.8
0.5	98.15	96.23	1.00	0.61	3.51	129.1
0.6	98.68	97.26	1.00	0.67	2.51	110.6
0.7	98.97	98.27	1.00	0.73	2.46	92.7
0.8	99.61	98.33	0.95	0.87	3.21	57.1
0.9	99.71	99.28	0.97	0.93	6.74	34.7





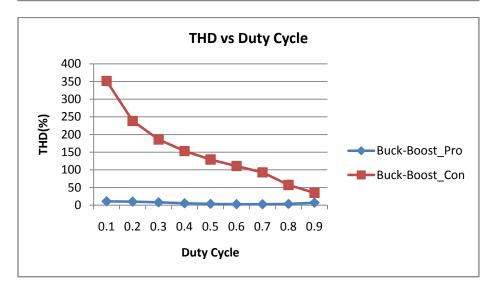
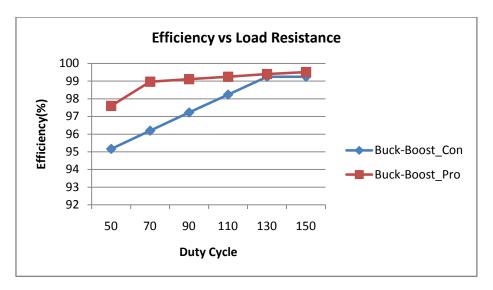
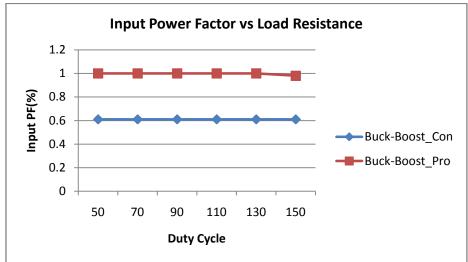


Fig 4.46: Efficiency, Input PF and THD vs. duty cycle of input switched Buck-Boost AC-DC converter-configuration 2

Table 4.9: Performance Comparison of Proposed and Conventional Buck-Boost Topology Based Rectifier Configuration 2 for Load Variation

	Efficiency, ŋ (%)		Input Powe	er Factor (PF)	THD (%)	
Load Resistance, RL (Ω)	Proposed Buck- Boost Topology	Conventional Buck-Boost Topology	Proposed Buck- Boost Topology	Conventional Buck-Boost Topology	Proposed Buck- Boost Topology	Conventional Buck-Boost Topology
50	97.60	95.16	1.00	0.61	4.60	129.1
70	98.97	96.19	1.00	0.61	4.03	129.1
90	99.11	97.22	1.00	0.61	3.66	129.1
110	99.25	98.23	1.00	0.61	3.42	129.1
130	99.40	99.24	1.00	0.61	3.15	129.1
150	99.51	99.24	0.98	0.61	2.94	129.1





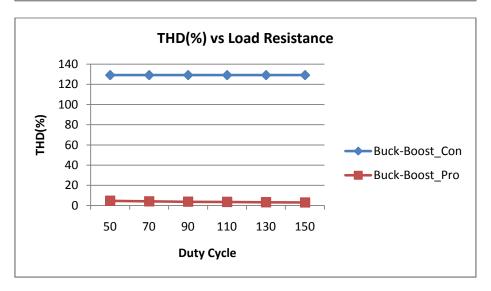


Fig 4.47: Efficiency, Input PF and THD vs. Load Resistance of input switched Buck-Boost AC-DC converter-configuration 2

4.3.3 Single Phase Input Switched Buck-Boost AC-DC Converter-Configuration 3

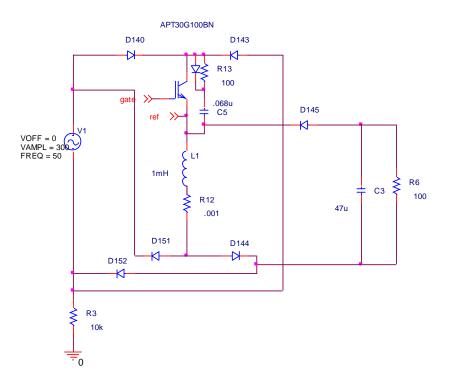


Fig 4.48: The single phase input switched AC-DC converter (Buck-Boost Configuration 3)

Fig. 4.48 shows the third topology of input switched single phase AC-DC Buck-Boost converter. This configuration has one buck-boost inductor, whereas, previous two input switched configuration discussed in 4.3.1 and 4.3.2 have two buck-boost inductors each in their respective circuits. The proposed topology-3 has four operating modes. Two modes are for positive supply cycle as shown in Fig. 4.49 and Fig. 4.50 for switch ON and switch OFF positions. The other two modes are for negative supply cycle as the switch of the circuit turns ON and OFF respectively (Fig. 4.51 and Fig 4.52 respectively).

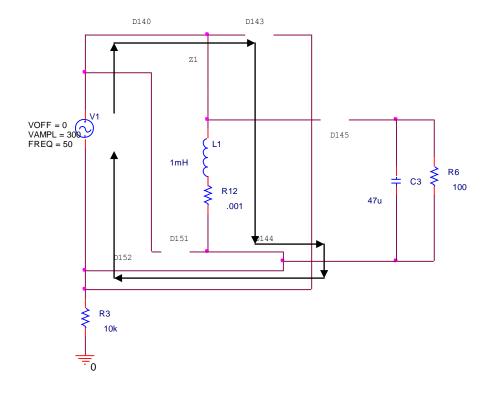


Fig 4.49: Equivalent circuit of the circuit of Fig.4.48 for positive cycle switch ON

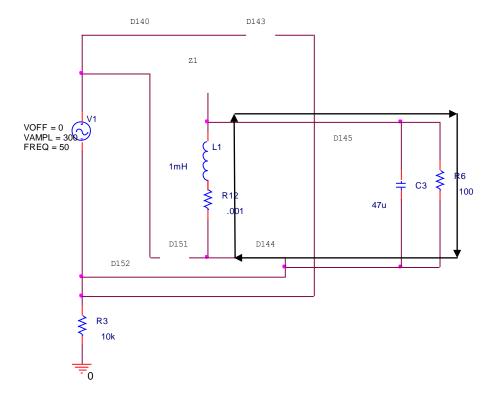


Fig 4.50: Equivalent circuit of the circuit of Fig.4.48 for positive cycle switch OFF

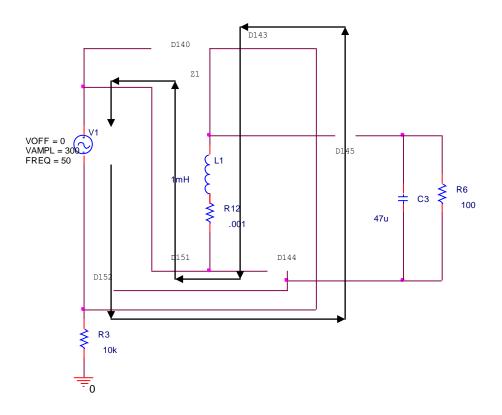


Fig 4.51: Equivalent circuit of the circuit of Fig.4.48 for negative cycle switch ON

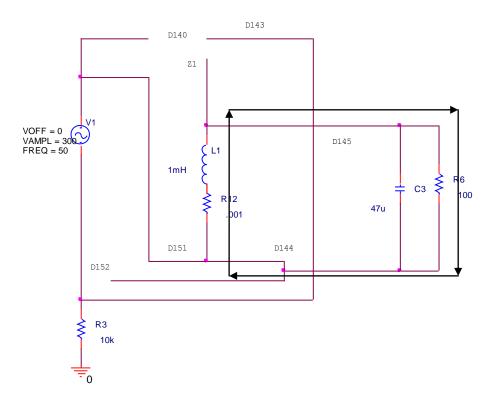


Fig 4.52: Equivalent circuit of the circuit of Fig.4.48 for negative cycle switch OFF

Typical input current and the output voltage of the circuit are shown in Fig. 4.53 and Fig. 4.54 respectively. The performance comparison with output regulated buck-boost AC-DC converter is depicted in Table 4.10 and Fig 4.55.

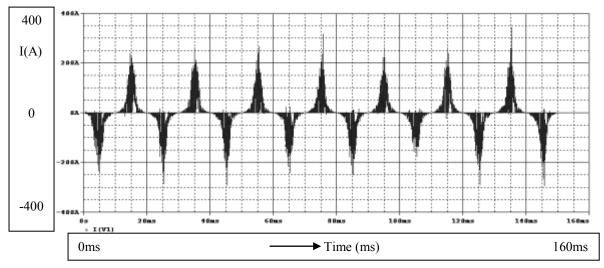


Fig 4.53: Input current shape of the proposed input switched Buck-Boost configuration-3 circuit of Fig 4.48

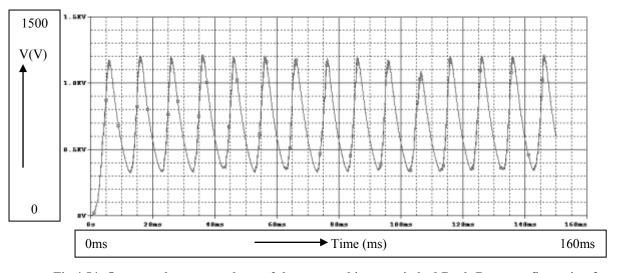
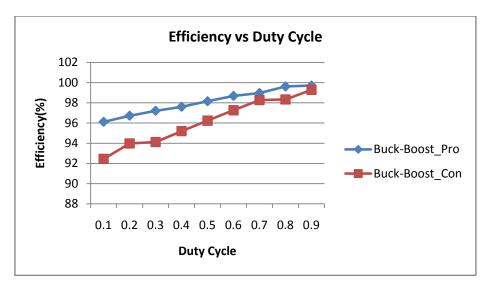
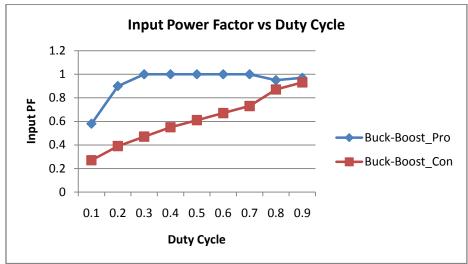


Fig 4.54: Output voltage wave shape of the proposed input switched Buck-Boost configuration-3 circuit of Fig 4.48

Table 4.10: Performance Comparison of Proposed and Conventional Buck-Boost Topology Based Rectifier Configuration 3 for Duty Cycle Variation

Dut	Efficiency, ŋ (%)		Input Powe	Input Power Factor (PF)		O (%)
y	Proposed	Convention	Proposed	Convention	Proposed	Convention
Су	Buck-	al Buck-	Buck-	al Buck-	Buck-	al Buck-
cle	Boost	Boost	Boost	Boost	Boost	Boost
D	Topology	Topology	Topology	Topology	Topology	Topology
0.1	96.11	92.45	0.58	0.27	10.64	351.1
0.2	96.72	93.97	0.90	0.39	9.77	238.1
0.3	97.21	94.11	1.00	0.47	7.80	185.6
0.4	97.60	95.19	1.00	0.55	5.12	152.8
0.5	98.15	96.23	1.00	0.61	3.51	129.1
0.6	98.68	97.26	1.00	0.67	2.51	110.6
0.7	98.97	98.27	1.00	0.73	2.46	92.7
0.8	99.61	98.33	0.95	0.87	3.21	57.1
0.9	99.71	99.28	0.97	0.93	6.74	34.7





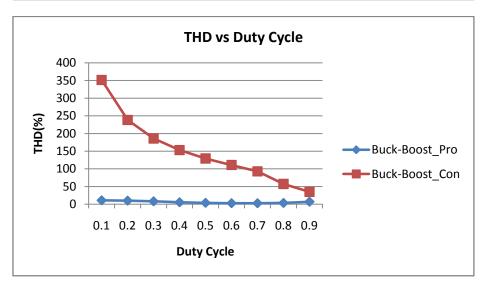


Fig 4.55: Efficiency, Input PF and THD vs. duty cycle of input switched Buck-Boost AC-DC converter-configuration 3

4.4 Single Phase Input Switched AC-DC Converter Ćuk Configuration

A conventional output regulated AC-DC converter with Ćuk topology is shown in Fig.4.56:

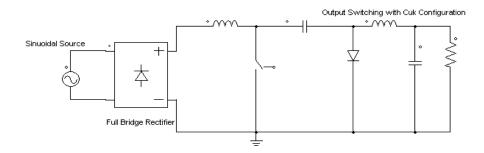


Fig 4.56: The conventional bridge rectifier with output switching in Ćuk Configuration

4.4.1 Input Switched Ćuk AC-DC Converter-Configuration 1

Fig. 4.57 shows a basic Ćuk topology based single phase AC-DC converter that can rectify both positive and negative half cycle of the input individually. A small input filter is designed in the input side to eliminate the ripple in the input side current and make the THD values within the range of different standards. The inductor L2, L3 and capacitor C3 work as input filter for both cycles of input signal.

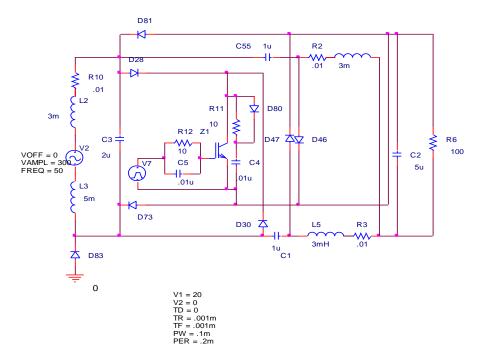


Fig 4.57: The single phase input switched AC-DC converter (Ćuk Configuration 1)

The Ćuk topology has four operating states as shown in Fig.4.58 to Fig.4.61. Fig.4.58 and Fig.4.59 represent the positive half cycle operation with switch ON and OFF positions, whereas, Fig.4.60 and Fig.4.61 represent the negative half cycle with switch ON and OFF positions respectively.

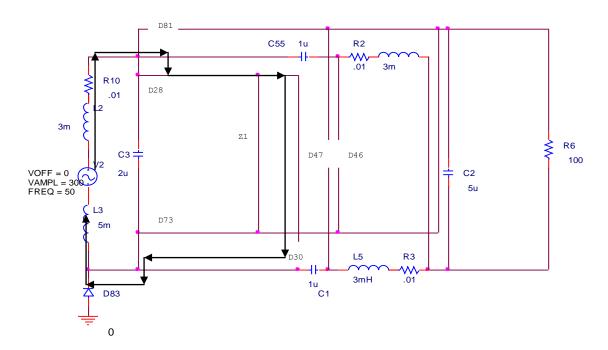


Fig 4.58: Equivalent circuit of the circuit of Fig. 4.57 for positive cycle switch ON

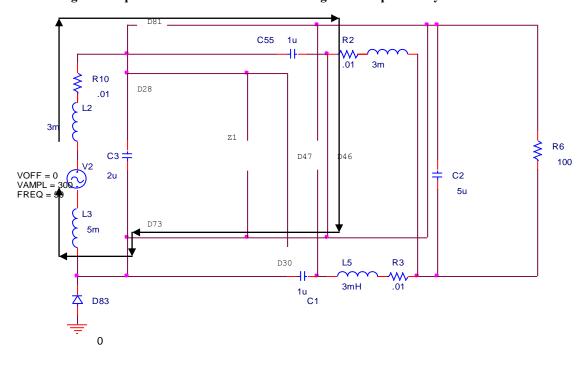


Fig 4.59: Equivalent circuit of the circuit of Fig. 4.57 for positive cycle switch OFF

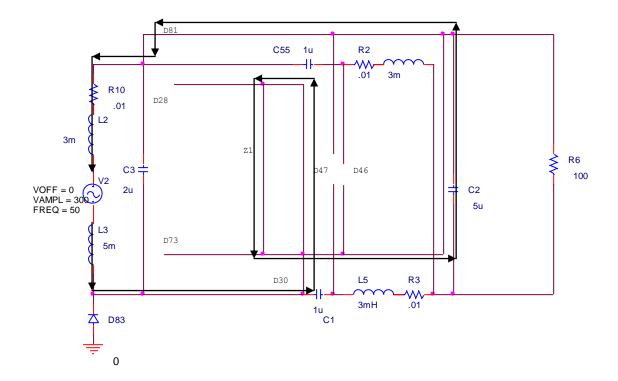


Fig 4.60: Equivalent circuit of the circuit of Fig. 4.57 for negative cycle switch ON

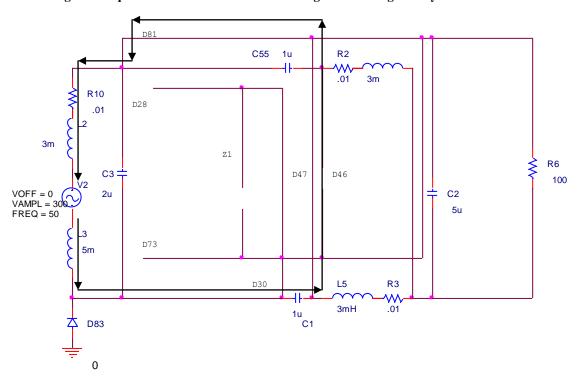


Fig 4.61: Equivalent circuit of the circuit of Fig. 4.57 for negative cycle switch OFF

Typical input current and the output voltage of the circuit are shown in Fig. 4.62 and Fig. 4.63 respectively. The performance comparison with output regulated buck-boost AC-DC converter is depicted in Table 4.11 and Fig 4.64.

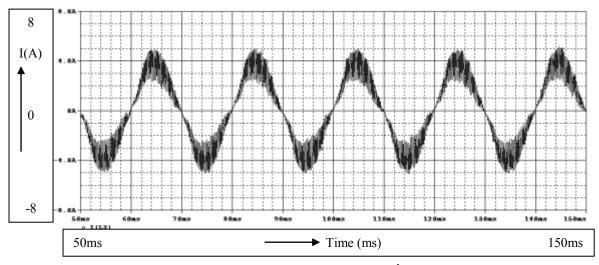


Fig 4.62: Input current shape of the proposed input switched Ćuk configuration 1 circuit of Fig 4.57

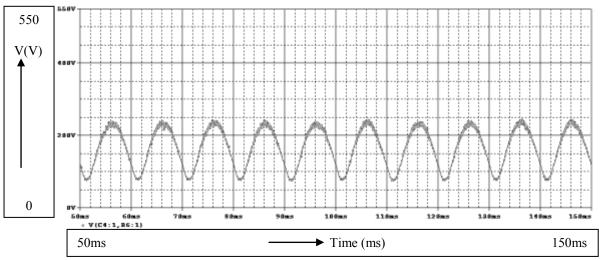
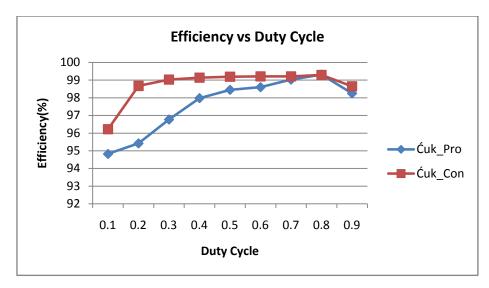
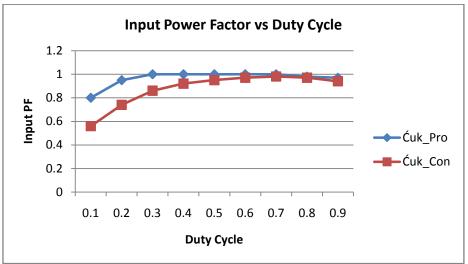


Fig 4.63: Output voltage wave shape of the proposed input switched Ćuk configuration 1 circuit of Fig 4.57

Table 4.11: Performance Comparison of Proposed and Conventional Ćuk Topology Based Rectifier Configuration 1 for Duty Cycle Variation

Dut	Efficiency, n(%)		Input Power Factor (PF)		THD (%)	
y Cycl e D	Proposed Ćuk Topology	Convention al Ćuk Topology	Proposed Ćuk Topology	Convention al Ćuk Topology	Proposed Ćuk Topology	Convention al Ćuk Topology
0.1	94.82	96.22	0.80	0.56	0.30	143.2
0.2	95.42	98.67	0.95	0.74	0.94	85.7
0.3	96.77	99.03	1.00	0.86	1.74	56.9
0.4	97.98	99.14	1.00	0.92	2.68	41.1
0.5	98.45	99.19	1.00	0.95	3.88	31.3
0.6	98.60	99.21	1.00	0.97	5.54	24.6
0.7	99.03	99.21	1.00	0.98	7.02	21.0
0.8	99.31	99.29	0.98	0.97	7.16	21.0
0.9	98.25	98.65	0.97	0.94	6.37	20.8





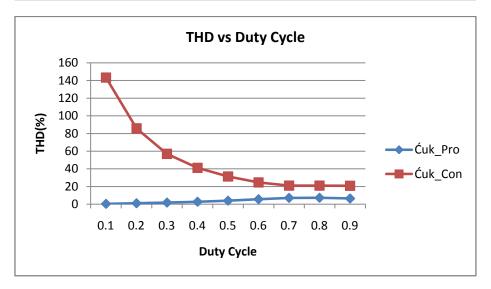
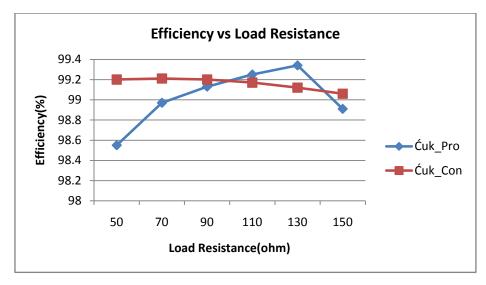
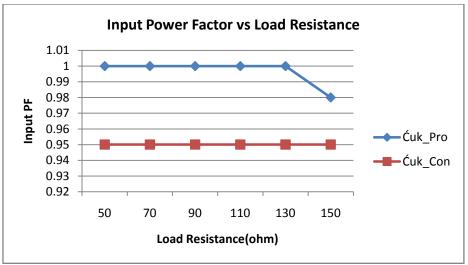


Fig 4.64: Efficiency, Input PF and THD vs. duty cycle of input switched Ćuk AC-DC converterconfiguration 1

Table 4.12: Performance Comparison of Proposed and Conventional Ćuk Topology Based Rectifier Configuration 1 for Load Variation

Load Resistance,	Efficiency, n(%)		Input Power Factor (PF)		THD (%)	
	Proposed	Conventional	Proposed	Conventional	Proposed	Conventional
$RL(\Omega)$	Ćuk	Ćuk	Ćuk	Ćuk	Ćuk	Ćuk
KL (32)	Topology	Topology	Topology	Topology	Topology	Topology
50	98.55	99.20	1.00	0.95	2.97	30.95
70	98.97	99.21	1.00	0.95	3.32	31.15
90	99.13	99.20	1.00	0.95	3.73	31.23
110	99.25	99.17	1.00	0.95	4.27	31.27
130	99.34	99.12	1.00	0.95	4.49	31.30
150	98.91	99.06	0.98	0.95	4.75	31.31





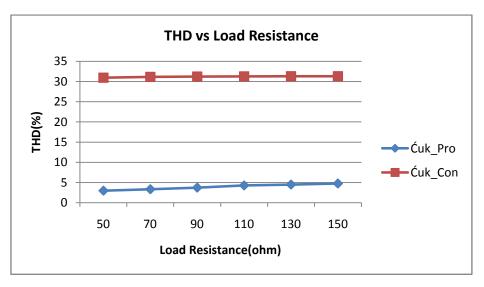


Fig 4.65: Efficiency, Input PF and THD vs. Load Resistance of input switched Ćuk AC-DC converter-configuration 1

4.4.2 Single Phase Input Switched Ćuk AC-DC Converter-Configuration 2

A second possible input switched Ćuk AC-DC converter consisting of an input bidirectional switch and an output rectifier is shown in Fig. 4.66.

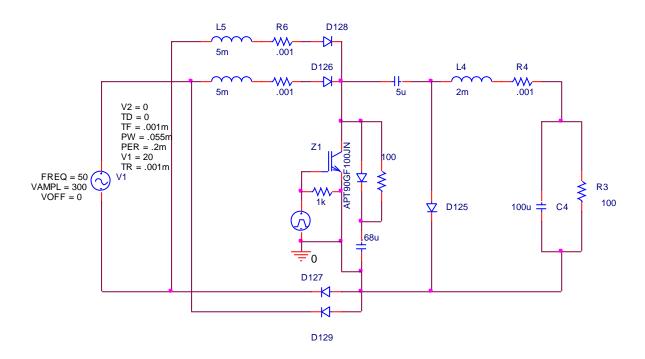


Fig 4.66: The single phase input switched AC-DC converter (Ćuk Configuration 2)

The topology has four operating states as shown in Fig.4.67 to Fig.4.70. Fig.4.67 and Fig.4.68 represent the positive half cycle operation with switch ON and OFF positions, whereas, Fig.4.69 and Fig.4.70 represent the negative half cycle with switch ON and OFF positions respectively.

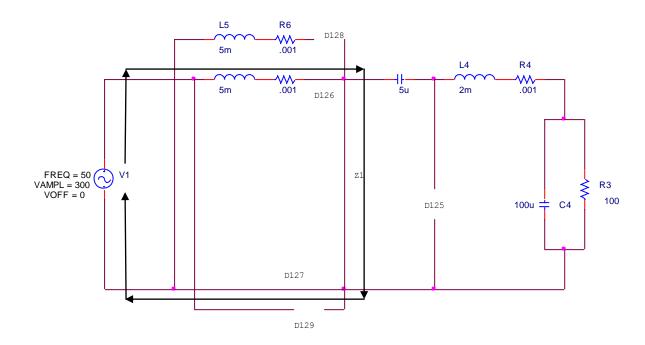


Fig 4.67: Equivalent circuit of the circuit of Fig.4.66 for positive cycle switch ON

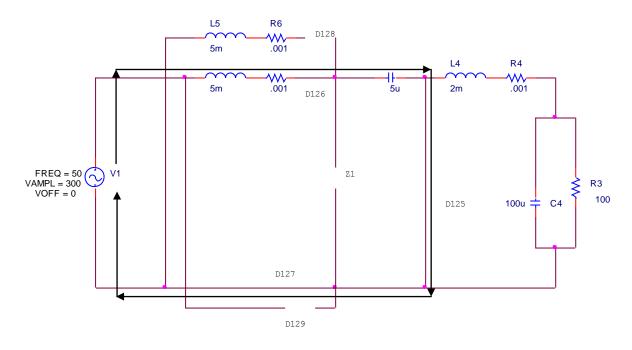


Fig4.68: Equivalent circuit of the circuit of Fig.4.66 for positive cycle switch OFF

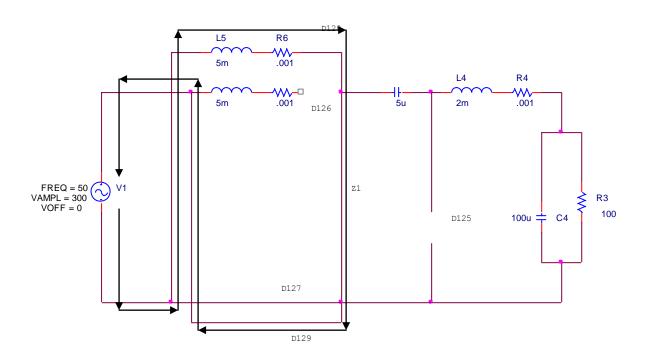


Fig 4.69: Equivalent circuit of the circuit of Fig.4.66 for negative cycle switch ON

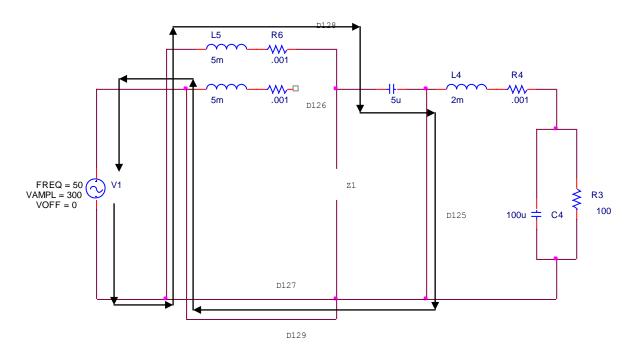


Fig 4.70: Equivalent circuit of the circuit of Fig.4.66 for negative cycle switch OFF

Typical input current and the output voltage waveforms without any input filter as shown in Fig 4.71 and Fig.4.72 respectively. Table 4.13 and Fig 4.73 show the performance comparison of proposed input switched Ćuk rectifier-configuration 2 with conventional output switched Ćuk rectifier in terms of efficiency, line current

THD and input power factor with duty cycle variation (without any feedback and input filter). In terms of input current THD and input power factor, the proposed circuit performs better, whereas; in terms of efficiency both have similar performance.

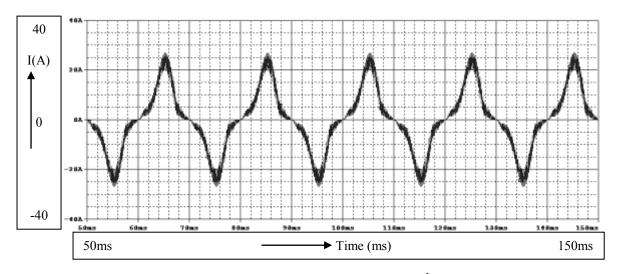


Fig 4.71: Input current shape of the proposed input switched Ćuk configuration 2 circuit

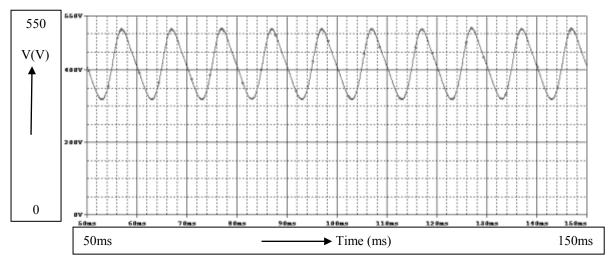
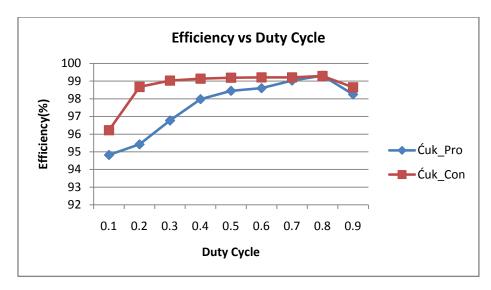
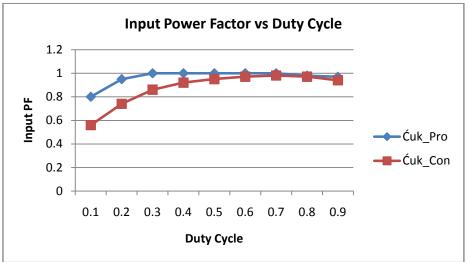


Fig 4.72: Output voltage wave shape of the proposed input switched Ćuk configuration 2 circuit

Table 4.13: Performance Comparison of Proposed and Conventional Ćuk Topology Based Rectifier Configuration 2 for Duty Cycle Variation

Dut	Efficier	Efficiency, n(%)		Input Power Factor (PF)		D (%)
y Cycl e D	Proposed Ćuk Topology	Convention al Ćuk Topology	Proposed Ćuk Topology	Convention al Ćuk Topology	Proposed Ćuk Topology	Convention al Ćuk Topology
0.1	95.82	96.22	0.80	0.56	0.30	143.2
0.2	96.42	98.67	0.95	0.74	0.94	85.7
0.3	97.77	99.03	1.00	0.86	1.74	56.9
0.4	98.98	99.14	1.00	0.92	2.68	41.1
0.5	98.45	99.19	0.99	0.95	3.89	31.3
0.6	98.60	99.21	0.99	0.97	5.58	24.6
0.7	99.03	99.21	0.99	0.98	7.06	21.0
0.8	99.31	99.29	0.98	0.97	7.15	21.0
0.9	98.25	98.65	0.97	0.94	6.31	20.8





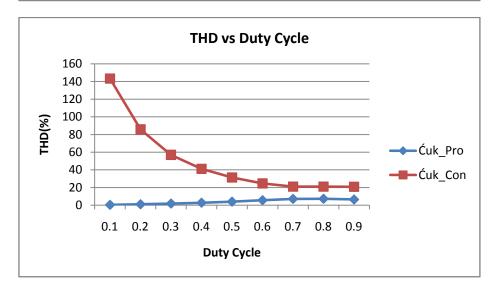


Fig 4.64: Efficiency, Input PF and THD vs. duty cycle of input switched Ćuk AC-DC converterconfiguration 2

4.5 Single Phase Input Switched SEPIC AC-DC Converter

A conventional output regulated AC-DC converter with SEPIC topology is shown in Fig.4.74:

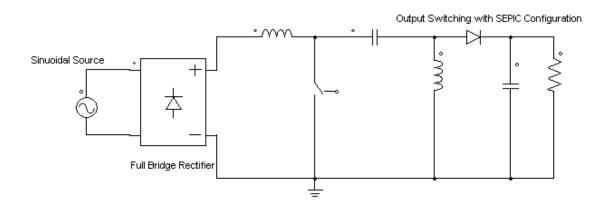


Fig 4.74: The conventional bridge rectifier with output switching in SEPIC configuration

4.5.1 Single Phase Input Switched SEPIC AC-DC Converter-Configuration 1

Fig. 4.75 shows the proposed circuit diagram of a single phase switch mode AC-DC converter using the principle of SEPIC conversion. The circuit consists of four inductors, four capacitors, six diodes and a switch (Z1). Supply voltage is AC; SEPIC conversion on both positive and negative cycle of the input voltage is required.

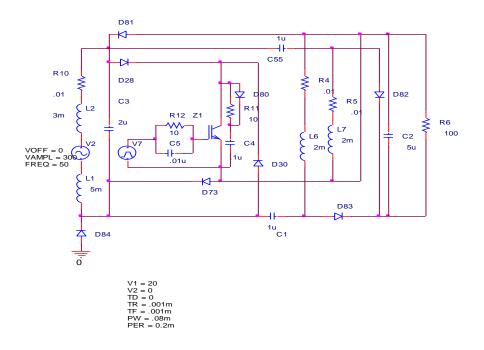


Fig 4.75: The single phase input switched AC-DC converter (SEPIC Configuration 1)

The SEPIC topology has four operating states as shown in Fig.4.76 to Fig.4.79. Fig.4.76 and Fig.4.77 represent the positive half cycle operation with switch ON and OFF positions, whereas, Fig.4.78 and Fig.4.79 represent the negative half cycle with switch ON and OFF positions respectively.

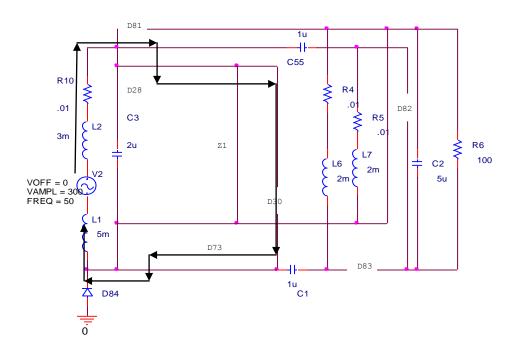


Fig 4.76: Equivalent circuit of the circuit of Fig.4.75 for positive cycle switch ON

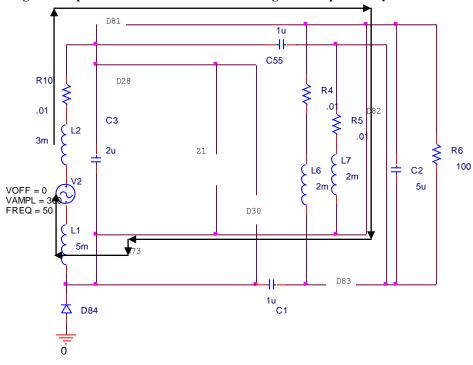


Fig 4.77: Equivalent circuit of the circuit of Fig.4.75 for positive cycle switch OFF

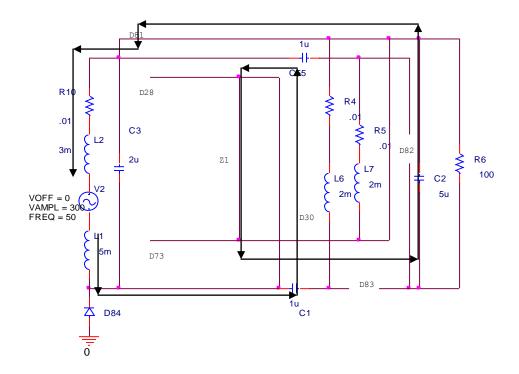


Fig 4.78: Equivalent circuit of the circuit of Fig.4.75 for negative cycle switch ON

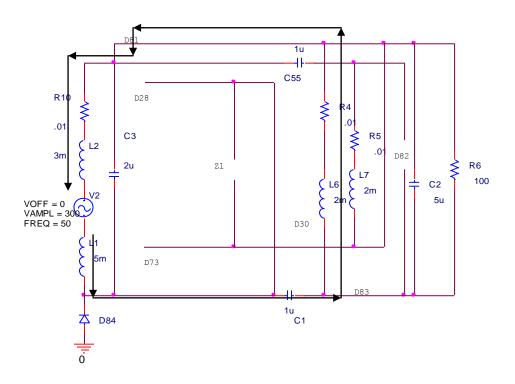


Fig 4.79: Equivalent circuit of the circuit of Fig.4.75 for negative cycle switch OFF

Typical input current and the output voltage waveforms without any input filter as shown in Fig 4.80 and Fig.4.81 respectively. Table 4.14 and Fig 4.82 show the performance comparison of proposed input switched SEPIC rectifier with conventional output switched SEPIC rectifier in terms of efficiency, line current THD and input power factor with duty cycle variation (without any feedback and input filter). Also, the performance is investigated for load variation (Table 4.15 and Fig. 4.83). In terms of input current THD and input power factor, the proposed circuit performs better, whereas; in terms of efficiency both have similar performance.

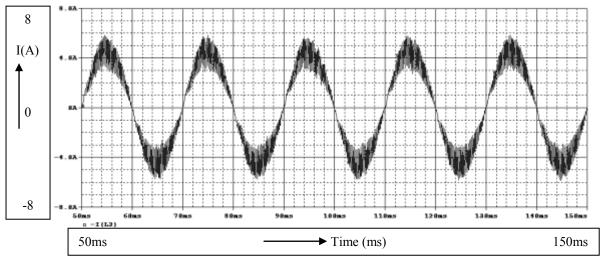


Fig 4.80: Input current shape of the proposed input switched SEPIC configuration 1 circuit of Fig.4.75

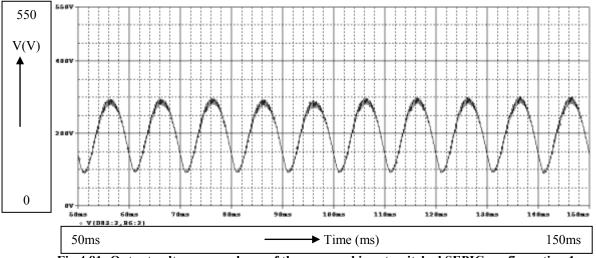
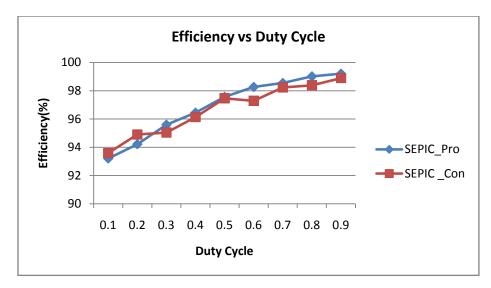


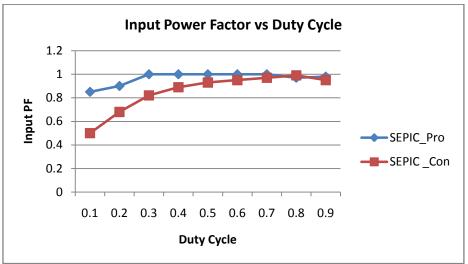
Fig 4.81: Output voltage wave shape of the proposed input switched SEPIC configuration 1 circuit of Fig. 4.75

Simulation of the proposed circuits is performed with PSIM professional version 9.0.3.400 and also with OrCAD Capture CIS 9.2 version. For simulation of SEPIC an input ac source of 300V amplitude with frequency of 50 Hz is employed. An IGBT is used for switching purpose. For the SEPIC scheme the inductors L6 and L7 have the values of 2mH and the capacitors C2 and C3 have the values of $5\mu F$ and $2\mu F$ respectively. A resistor of 100Ω is used as load. The proposed circuit topology has been compared with the respective conventional single phase AC-DC diode bridge rectifier configurations.

Table 4.14: Performance Comparison of Proposed and Conventional SEPIC Topology Based Rectifier Configuration 1 for Duty Cycle Variation

Dut	Efficiency, n(%)		Input Power Factor (PF)		THD (%)	
У						
Cyc	Proposed	Convention	Proposed	Convention	Proposed	Convention
le	SEPIC	al SEPIC	SEPIC	al SEPIC	SEPIC	al SEPIC
D	Topology	Topology	Topology	Topology	Topology	Topology
0.1	93.20	93.59	0.85	0.50	0.26	157.3
0.2	94.21	94.90	0.90	0.68	0.73	103.9
0.3	95.59	95.04	1.00	0.82	1.98	69.8
0.4	96.44	96.13	1.00	0.89	2.24	51.2
0.5	97.56	97.46	1.00	0.93	3.24	39.4
0.6	98.26	97.28	1.00	0.95	5.06	30.9
0.7	98.54	98.23	1.00	0.97	6.73	24.5
0.8	99.01	98.38	0.97	0.99	7.21	14.0
0.9	99.20	98.89	0.98	0.95	6.73	21.1





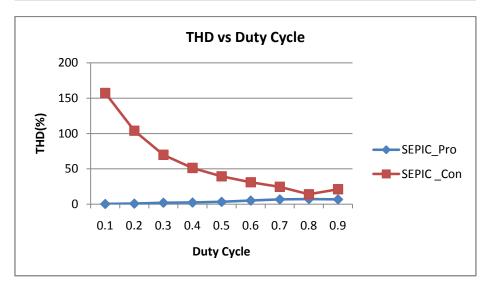
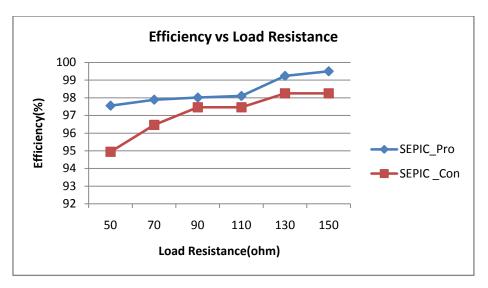
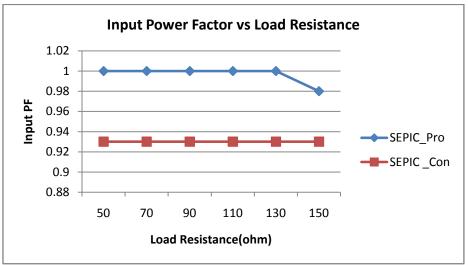


Fig 4.82: Efficiency, Input PF and THD vs. duty cycle of input switched SEPIC AC-DC converter-configuration 1

Table 4.15: Performance Comparison of Proposed and Conventional SEPIC Topology Based Rectifier Configuration 1 for Load Variation

Load	Efficiency, n(%)		Input Powe	er Factor (PF)	THD (%)	
Resistance,	Proposed	Conventional	Proposed	Conventional	Proposed	Conventional
$RL(\Omega)$	SEPIC	SEPIC	SEPIC	SEPIC	SEPIC	SEPIC
KL (32)	Topology	Topology	Topology	Topology	Topology	Topology
50	97.55	94.94	1.00	0.93	2.83	39.3
70	97.89	96.46	1.00	0.93	3.08	39.4
90	98.01	97.46	1.00	0.93	3.23	39.4
110	98.10	97.46	1.00	0.93	3.28	39.4
130	99.24	98.25	1.00	0.93	3.70	39.3
150	99.50	98.25	0.98	0.93	3.99	39.3





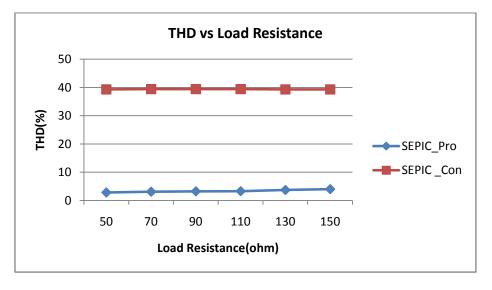


Fig 4.83: Efficiency, Input PF and THD vs. Load Resistance of input switched SEPIC AC-DC converter-configuration 1

4.5.2 Single Phase Input Switched SEPIC AC-DC Converter-Configuration 2

A second possible input switched SEPIC AC-DC converter consisting of an input bidirectional switch and an output rectifier is shown in Fig. 4.84.

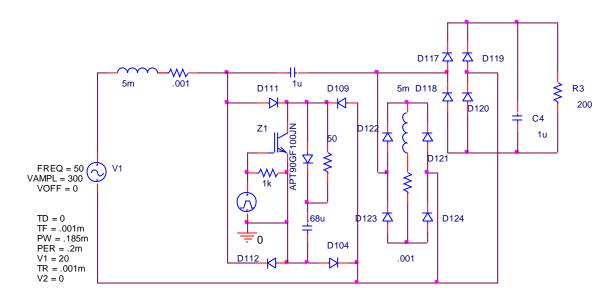


Fig 4.84: The single phase input switched AC-DC converter (SEPIC Configuration 2)

The SEPIC topology has four operating states as shown in Fig.4.85 to Fig.4.88. Fig.4.85 and Fig.4.86 represent the positive half cycle operation with switch ON and OFF positions, whereas, Fig.4.87 and Fig.4.88 represent the negative half cycle with switch ON and OFF positions respectively.

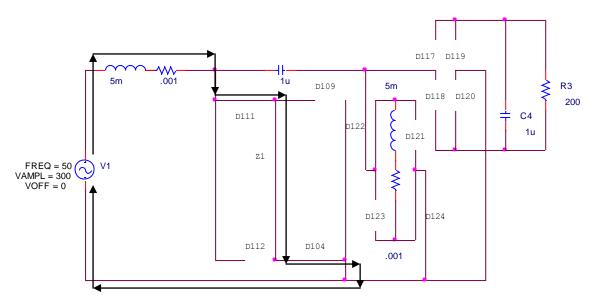


Fig 4.85: Equivalent circuit of the circuit of Fig. 4.84 for positive cycle switch ON

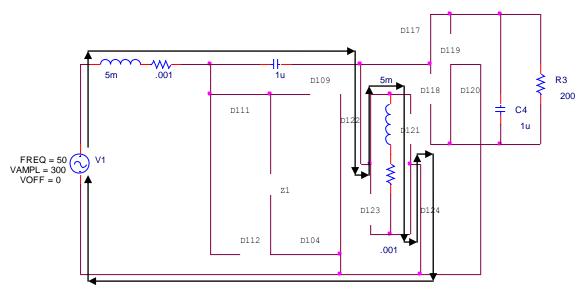


Fig 4.86: Equivalent circuit of the circuit of Fig. 4.84 for positive cycle switch OFF

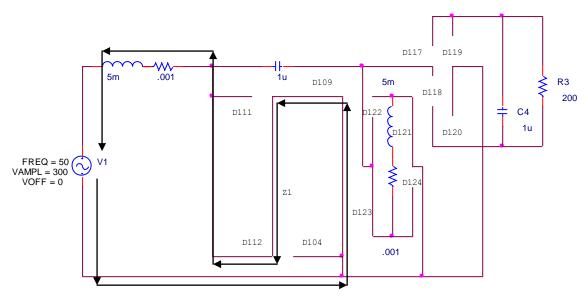


Fig 4.87: Equivalent circuit of the circuit of Fig. 4.84 for negative cycle switch ON

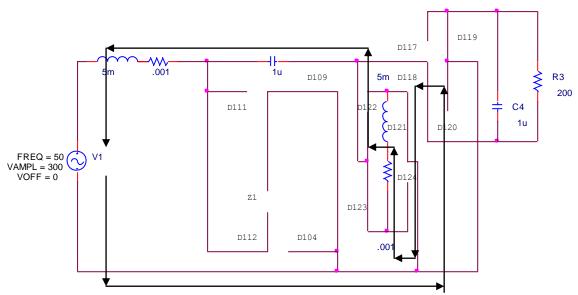


Fig 4.88: Equivalent circuit of the circuit of Fig. 4.84 for negative cycle switch OFF

Typical input current and the output voltage waveforms without any input filter are shown in Fig 4.89 and Fig.4.90 respectively. Table 4.16 and Fig 4.91 show the performance comparison of proposed input switched SEPIC rectifier with conventional output switched SEPIC rectifier in terms of efficiency, line current THD and input power factor with duty cycle variation of the switched (without any feedback and input filter). In terms of input current THD and input power factor, the

proposed circuit performs better, whereas; in terms of efficiency both have similar performance.

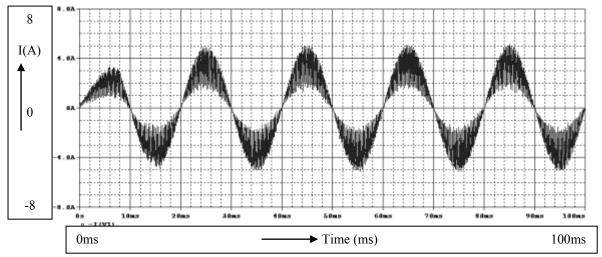


Fig 4.89: Input current shape of the proposed input switched SEPIC configuration 2 circuit of Fig.4.84

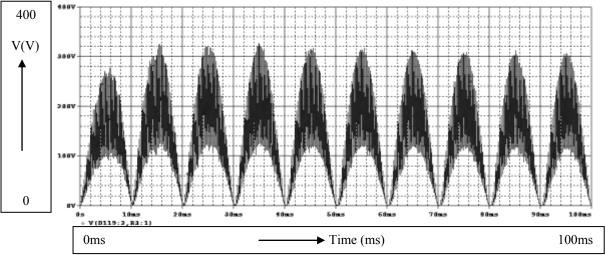
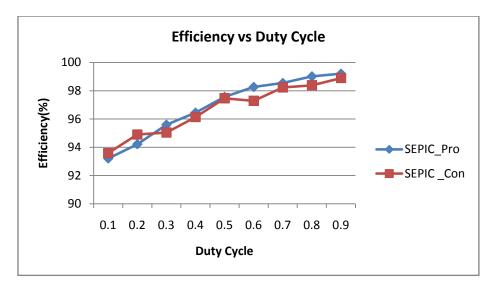
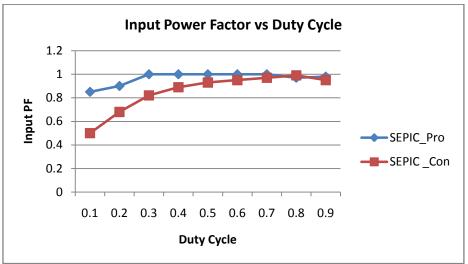


Fig 4.90: Output voltage wave shape of the proposed input switched SEPIC configuration 2 circuit of Fig.4.84

Table 4.16: Performance Comparison of Proposed and Conventional SEPIC Topology Based Rectifier-Configuration 2 for Duty Cycle Variation

Dut	Efficiency, n(%)		Input Power Factor (PF)		THD (%)	
y Cyc le D	Proposed SEPIC Topology	Convention al SEPIC Topology	Proposed SEPIC Topology	Convention al SEPIC Topology	Proposed SEPIC Topology	Convention al SEPIC Topology
0.1	93.25	93.59	0.85	0.50	0.26	157.3
0.2	94.61	94.90	0.90	0.68	0.73	103.9
0.3	95.61	95.04	1.00	0.82	1.98	69.8
0.4	96.48	96.13	1.00	0.89	2.24	51.2
0.5	97.55	97.46	0.99	0.93	3.26	39.4
0.6	98.29	97.28	0.99	0.95	5.16	30.9
0.7	98.55	98.23	0.99	0.97	6.61	24.5
0.8	99.05	98.38	0.98	0.99	7.23	14.0
0.9	99.21	98.89	0.98	0.95	6.72	21.1





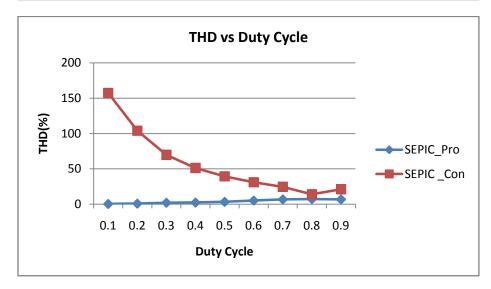


Fig 4.91: Efficiency, Input PF and THD vs. duty cycle of input switched SEPIC AC-DC converter-configuration 2

4.6 Single Phase Input Switched Inverse SEPIC AC-DC Converter

A conventional output regulated single phase AC-DC converter with SEPIC topology is shown in Fig.4.92:

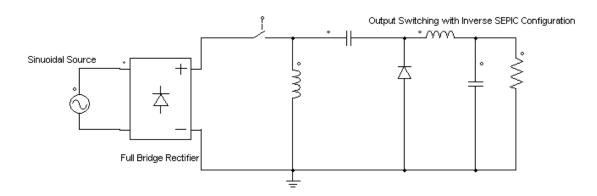


Fig 4.92: The conventional bridge rectifier with output switching in Inverse SEPIC configuration

4.6.1 Single Phase Input Switched Inverse SEPIC AC-DC Converter-Configuration 1

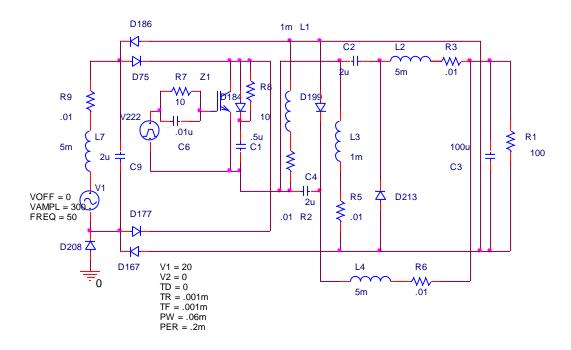


Fig 4.93: The single phase input switched AC-DC converter (Inverse SEPIC Configuration 1)

The Inverse SEPIC topology has four operating states as shown in Fig.4.94 to Fig.4.97. Fig.4.94 and Fig.4.95 represent the positive half cycle operation with switch

ON and OFF positions, whereas, Fig.4.96 and Fig.4.97 represent the negative half cycle with switch ON and OFF positions respectively.

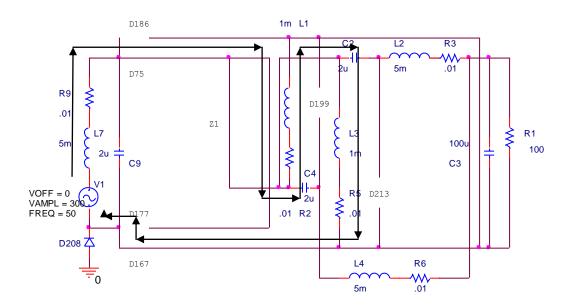


Fig 4.94: Equivalent circuit of the circuit of Fig.4.93 for positive cycle switch ON

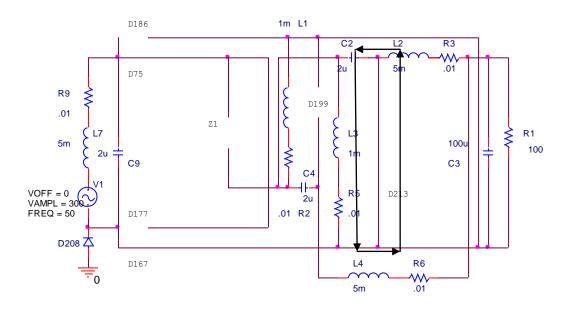


Fig 4.95: Equivalent circuit of the circuit of Fig.4.93 for positive cycle switch OFF

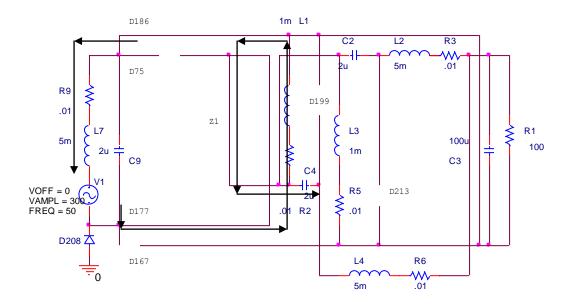


Fig 4.96: Equivalent circuit of the circuit of Fig.4.93 for negative cycle switch ON

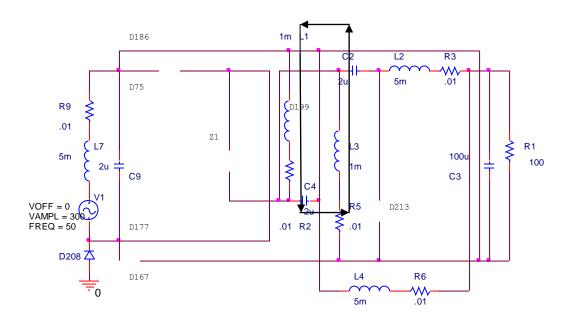


Fig 4.97: Equivalent circuit of the circuit of Fig.4.93 for negative cycle switch OFF

Typical input current and the output voltage waveforms without any input filter are shown in Fig 4.98 and Fig.4.99 respectively. Table 4.17 and Fig 4.100 show the performance comparison of proposed input switched SEPIC rectifier with conventional output switched SEPIC rectifier in terms of efficiency, line current THD and input power factor with duty cycle variation of the switched (without any

feedback and input filter). Table 4.18 and Fig.101 depict the load variation as well. In terms of input current THD and input power factor, the proposed circuit performs better, whereas; in terms of efficiency both have similar performance.

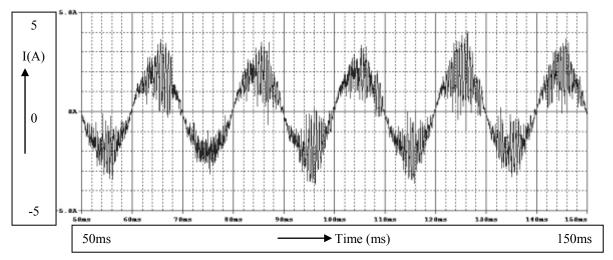


Fig 4.98: Input current shape of the proposed input switched Inverse SEPIC configuration 1 circuit of Fig.4.93

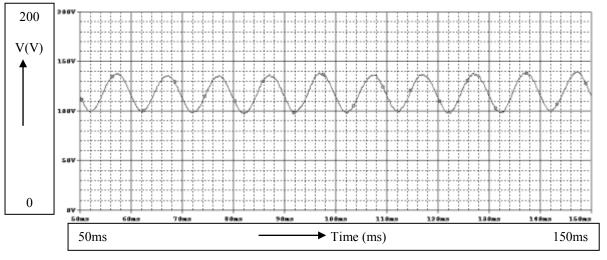
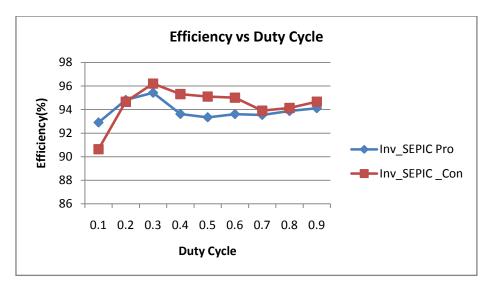
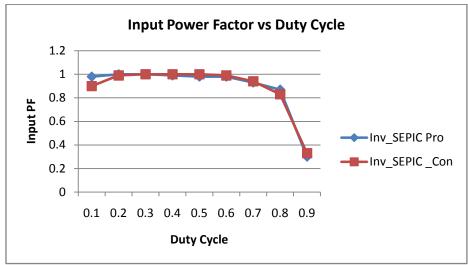


Fig 4.99: Output voltage wave shape of the proposed input switched Inverse SEPIC configuration 1 circuit of Fig.4.93

Table 4.17: Performance Comparison of Proposed and Conventional Inverse SEPIC Topology Based Rectifier Configuration 1 for Duty Cycle Variation

Du	Efficiency, n (%)		Input Power Factor (PF)		THD (%)	
ty Cy cle D	Proposed Inverse SEPIC Topology	Convention al Inverse SEPIC Topology	Proposed Inverse SEPIC Topology	Convention al Inverse SEPIC Topology	Proposed Inverse SEPIC Topology	Convention al Inverse SEPIC Topology
0.1	92.90	90.63	0.98	0.90	9.13	7.86
0.2	94.81	94.66	1.00	0.99	7.34	7.18
0.3	95.42	96.20	1.00	1.00	3.47	3.67
0.4	93.62	95.31	0.99	1.00	4.50	3.83
0.5	93.34	95.10	0.98	1.00	3.24	7.14
0.6	93.61	95.01	0.98	0.99	4.38	9.54
0.7	93.54	93.90	0.93	0.94	8.75	10.21
0.8	93.87	94.13	0.87	0.83	3.38	10.07
0.9	94.11	94.67	0.30	0.33	2.32	2.80





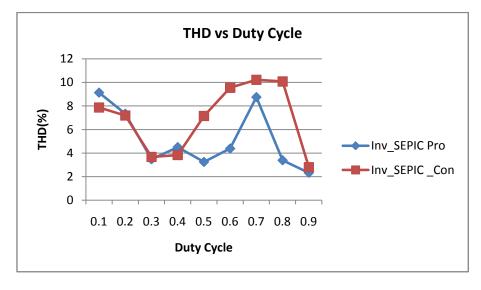
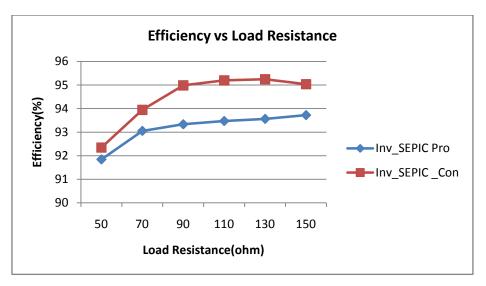
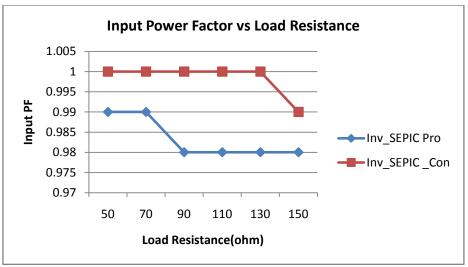


Fig 4.100: Efficiency, Input PF and THD vs. duty cycle of input switched Inverse SEPIC AC-DC converter-configuration 1

Table 4.18: Performance Comparison of Proposed and Conventional Inverse SEPIC Topology Based Rectifier Configuration 1 for Load Variation

Efficiency, n (%)		Input Power Factor (PF)		THD (%)		
Load	Proposed	Conventional	Proposed	Conventional	Proposed	Conventional
Resistance,	Inverse	Inverse	Inverse	Inverse	Inverse	Inverse
$RL(\Omega)$	SEPIC	SEPIC	SEPIC	SEPIC	SEPIC	SEPIC
	Topology	Topology	Topology	Topology	Topology	Topology
50	91.84	92.34	0.99	1.00	3.48	8.91
70	93.05	93.94	0.99	1.00	3.38	12.08
90	93.33	94.98	0.98	1.00	3.20	6.43
110	93.47	95.19	0.98	1.00	3.11	6.70
130	93.56	95.24	0.98	1.00	3.58	7.03
150	93.72	95.03	0.98	0.99	3.32	7.16





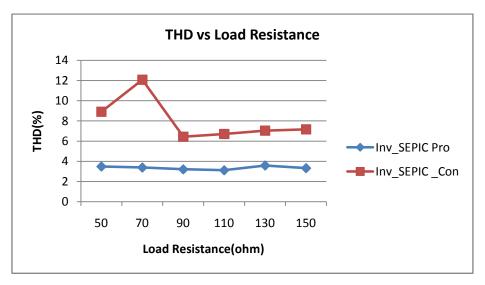


Fig 4.101: Efficiency, Input PF and THD vs. Load Resistance of input switched Inverse SEPIC AC-DC converter-configuration 1

4.6.2 Single Phase Input Switched Inverse SEPIC AC-DC Converter-Configuration 2

A second possible input switched Inverse SEPIC AC-DC converter consisting of an input bidirectional switch and an output rectifier is shown in Fig. 4.102.

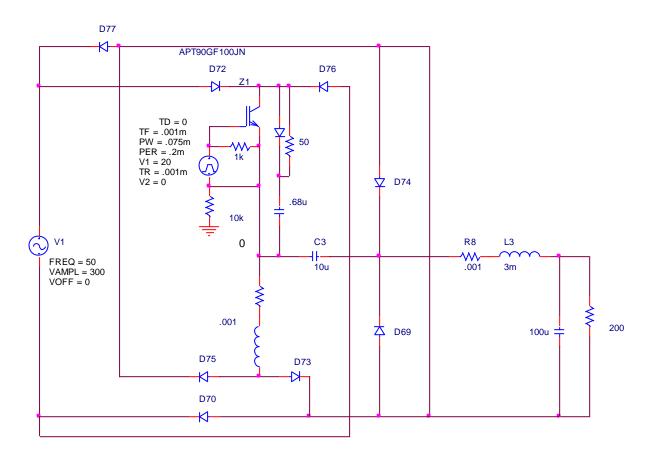


Fig 4.102: The single phase input switched AC-DC converter (Inverse SEPIC Configuration 2)

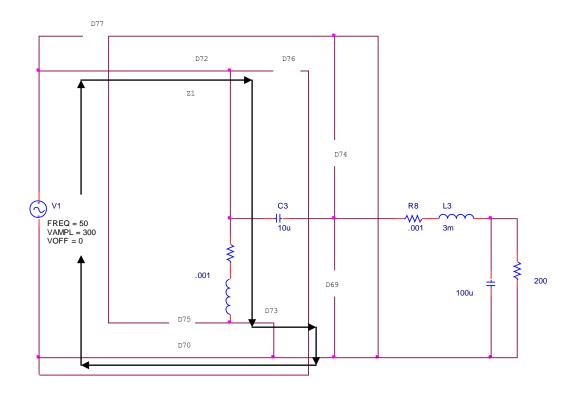


Fig 4.103: Equivalent circuit of the circuit Fig. 4.102 for positive cycle switch ON

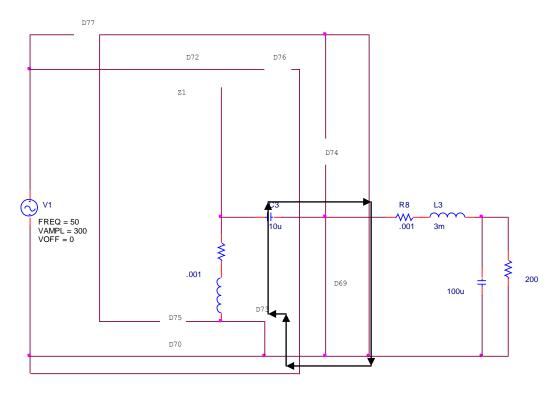


Fig 4.104: Equivalent circuit of the circuit Fig. 4.102 for positive cycle switch OFF

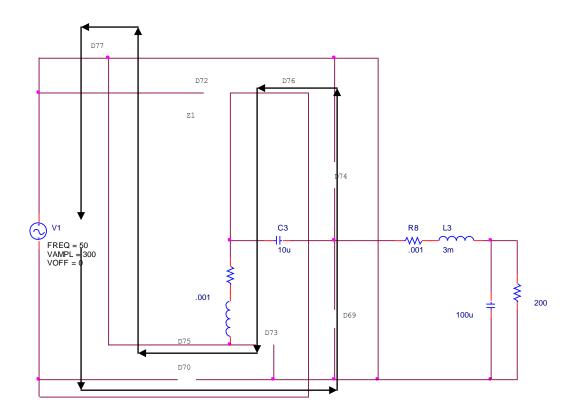


Fig 4.105: Equivalent circuit of the circuit Fig. 4.102 for negative cycle switch ON

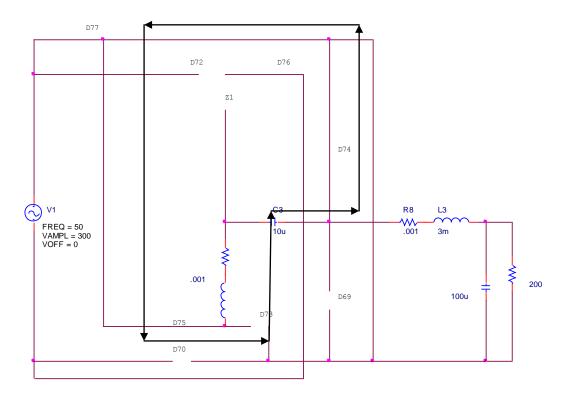


Fig 4.106: Equivalent circuit of the circuit Fig. 4.102 for negative cycle switch OFF

Like configuration 1, configuration 2 utilizes a common circuit path for all the operating states thus reducing the number of circuit elements in the input switched topology.

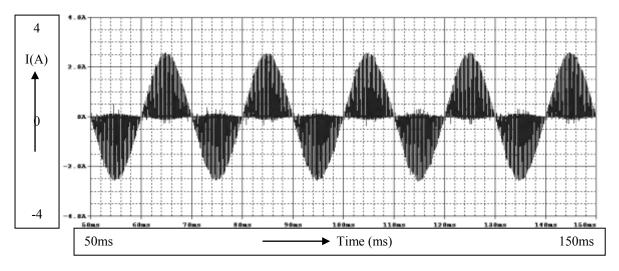


Fig 4.107: Input current shape of the proposed input switched Inverse SEPIC configuration 2 circuit of Fig. 4.102

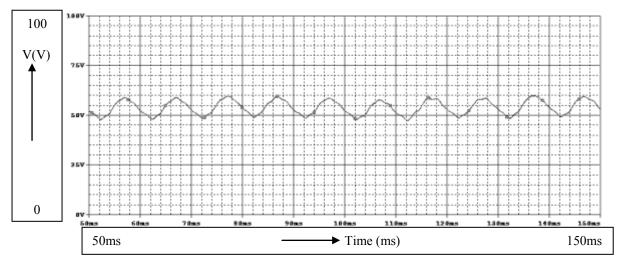
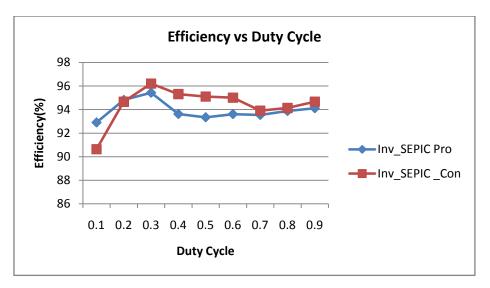
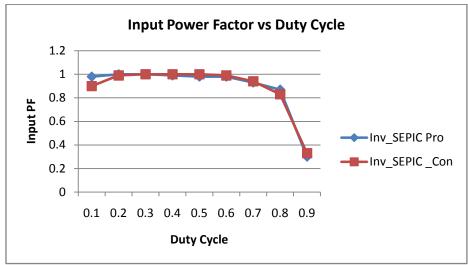


Fig 4.108: Output voltage wave shape of the proposed input switched Inverse SEPIC configuration 2 circuit of Fig. 4.102

Table 4.19: Performance Comparison of Proposed and Conventional Inverse SEPIC Topology Based Rectifier Configuration 2 for Duty Cycle Variation

Du	Efficiency, n(%)		Input Powe	r Factor (PF)	THD (%)	
ty Cy cle D	Proposed Inverse SEPIC Topology	Convention al Inverse SEPIC Topology	Proposed Inverse SEPIC Topology	Convention al Inverse SEPIC Topology	Proposed Inverse SEPIC Topology	Convention al Inverse SEPIC Topology
0.1	92.81	90.63	0.98	0.90	9.13	7.86
0.2	94.12	94.66	1.00	0.99	7.34	7.18
0.3	95.11	96.20	1.00	1.00	3.47	3.67
0.4	93.23	95.31	0.99	1.00	4.50	3.83
0.5	93.26	95.10	0.98	1.00	3.23	7.14
0.6	93.61	95.01	0.98	0.99	4.35	9.54
0.7	93.50	93.90	0.93	0.94	8.78	10.21
0.8	93.75	94.13	0.87	0.83	3.39	10.07
0.9	94.25	94.67	0.32	0.33	2.33	2.80





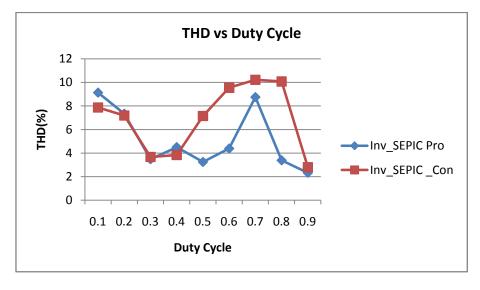


Fig 4.109: Efficiency, Input PF and THD vs. duty cycle of input switched Inverse SEPIC AC-DC converter-configuration 2

4.7 Example of a Closed Controlled Single Phase Input Switched Boost AC-DC Converter

Almost all DC-DC converters operate with their output voltage regulated to reference value as shown in Fig 4.110. This regulation is achieved by pulse-width-modulating of the duty ratio D of control signal of the switch.

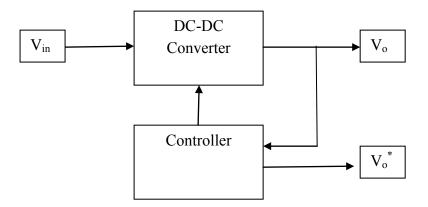


Fig 4.110: Regulated DC power supply [37]

The feedback controller to regulate the output voltage are usually designed with near zero steady state error, fast response to changes in the input voltage and the output load, low overshoot and low noise susceptibility. In switch mode regulated AC-DC converters, additional feedback are necessary to track the input current and emulate the load to be sensitive for low input current THD and high input power factor.

4.7.1 Single Phase Output Regulated Boost AC-DC Converter with Feedback Control

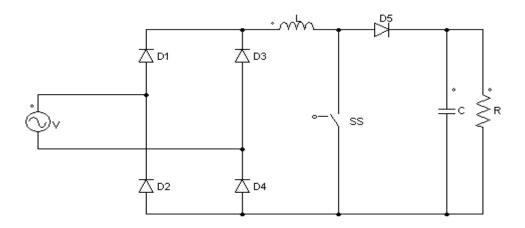


Fig 4.111: The output regulated Boost AC-DC converter

A typical output regulated Boost AC-DC converter is shown in Fig. 4.111. A Boost DC-DC converter is introduced between rectifier output and the DC output capacitor. In controlling an output regulated Boost AC-DC converter, the main objective is to draw a sinusoidal current, in phase with the input voltage. The Boost inductor current is of the full wave rectified form. The requirements on the form and the amplitude of the inductor current lead to two control loops- inner loop (dotted in Fig. 4.112) and outer loop [37].

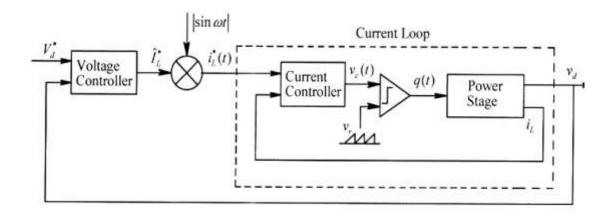


Fig 4.112: Feedback control loops for output regulated Boost AC-DC converter

In a system with PFC interface, the output is nearly constant, independent in the changes in the r.m.s value of the input voltage from the utility. To avoid propagating the input voltage disturbance through the PFC feedback loops, the input voltage peak is feed forward to determine the inductor current as shown in Fig. 4.113 [37].

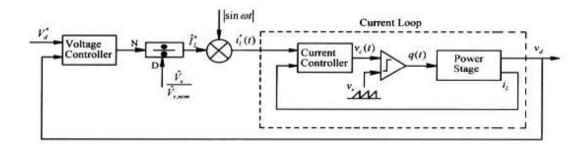


Fig 4.113: Feed forward of the input voltage for output regulated Boost AC-DC converter with feedback control [37]

The PSPICE simulation circuit of the power module with feedback sensors is shown in Fig. 4.114. The control circuit with two PI controllers and gate pulse generating circuit is shown in Fig. 4.115.

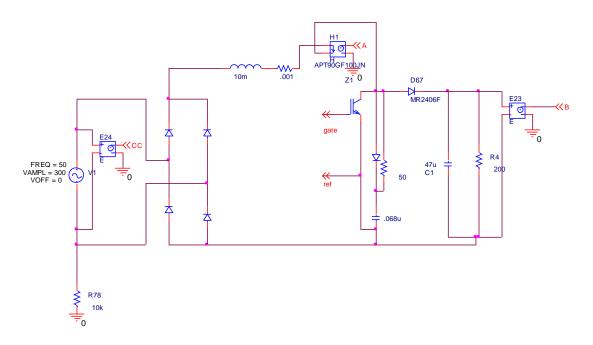


Fig 4.114: Feedback controlled output Boost converter regulated AC-DC converter (power circuit with sensors)

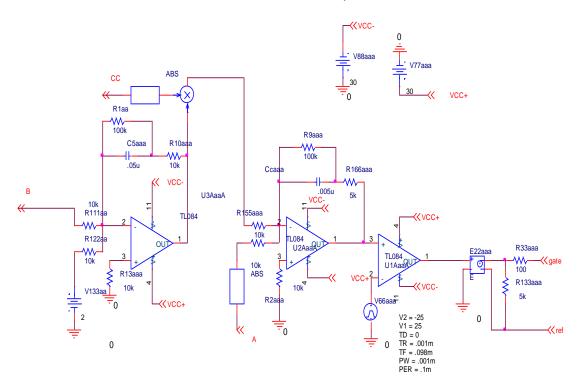


Fig 4.115: Feedback control circuit for Boost AC-DC converter configuration-2

The scaled output voltage is labeled as "B" and is fed into the voltage controller, where, it compared with a specified reference value. Scaled input voltage is marked as "CC" and is feed forwarded and multiplied by absolute sinusoidal signal. The scaled input inductor current "A" is fed to a current controller and with the help of the voltage controller it produces a control signal which is in turn compared to a reference signal that drives the gate of the bi-directional switch.

Typical output voltage of the rectifier and the input current is shown in Fig. 4.116. It is evident that the input current has low distortions (THD=17%) and it tracks the input voltage with near unity (0.98) power factor. The overall efficiency is near 84 percent.

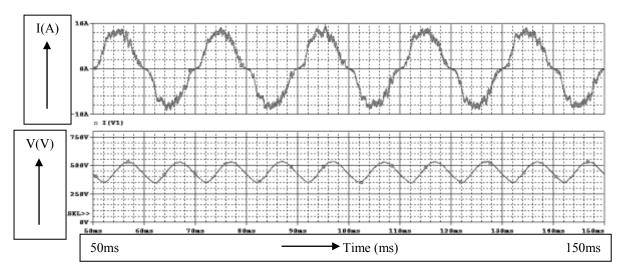


Fig 4.116: Typical input current and output voltage waveforms of circuit of Fig. 4.114 controlled by circuit of Fig. 4.115

4.7.2 Single Phase Input Regulated Boost AC-DC Converter (Proposed Configuration 2) with Feedback Control

Like output regulated Boost AC-DC converter with feedback control, input switched Boost AC-DC converter can also be designed with feedback control. The signals that need to be monitored and therefore feedback are the output voltage, inductor current and input voltage feed forward to maintain a certain reference value with a precise limit. Fig. 4.117 shows one example of the circuit. The control circuit is same as that of Fig. 4.115.

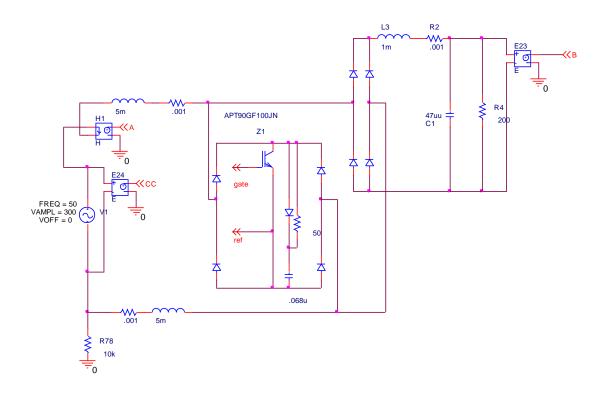


Fig 4.117: Input switched Boost AC-DC converter with feedback control (proposed config. 2)

Typical input current and output voltage wave shapes are given in Fig. 4.118 which shows similar performance as that of conventional output regulated Boost converter topology (input current THD=17%, PF=0.98, efficiency=84%).

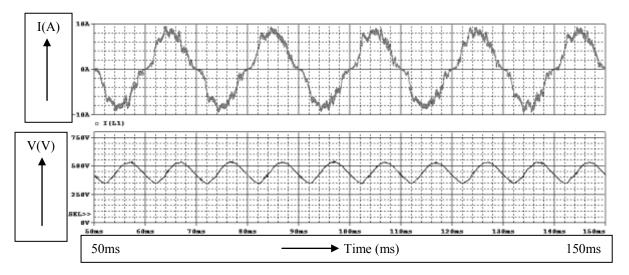


Fig 4.118: Typical input current and output voltage waveforms of circuit of Fig. 4.117 controlled by circuit of Fig. 4.115

CHAPTER 5

CONCLUSION

5.1 Summary of the thesis

A single phase full wave diode rectifier has been studied. The input current was found non sinusoidal pulsating and the THD was high. A passive output filter has been employed to make the input current sinusoidal. The THD and efficiency was found at the desired levels. But the filter was large. The output voltage was not controllable.

Output regulated DC-DC converters have been investigated by researchers with small input filter. It was observed that the input current had low THD and high efficiency. The output voltage was also controllable. The study was repeated in this thesis. The switching frequency was kept constant at 5 kHz. It was found from the analysis that the THD has improved wide range of duty cycles, but the overall efficiency of the regulator was not acceptable in the open loop control at all duty cycles. It was also observed that efficiency and THD cannot be kept at the desired level simultaneously with change in duty cycle.

In this thesis, input switched single phase AC-DC converter circuits have been studied and presented. The topologies used are Buck, Boost, Buck-Boost, Ćuk, SEPIC and Inverse SEPIC. Each type studied has multiple configurations, where, the last configuration in each type is the newly reported configuration (Buck, Boost Configuration-2, Buck-Boost Configuration-3, Ćuk Configuration-2, SEPIC configuration-2, and Inverse SEPIC configuration-2). Newly proposed Buck and Buck-Boost topologies have one Buck/Buck-Boost inductor, whereas, the previously reported circuits had two inductors. In Ćuk, SEPIC and Inverse SEPIC configuration also, the output stage have less number of inductors than previously reported circuits. All the newly proposed input switched single phase AC-DC converters are easier to implement than previously reported circuits. The circuits without any feedback exhibit improved performance than their counter part of output regulated single phase AC-DC converters.

Newly proposed Boost (configuration 2) based input switched rectifier have been studied as an example of feedback controlled rectifier. Some controller circuit has been used for input and output switched single phase Boost AC-DC converter and the result in the form of typical waveforms are presented in this thesis. This illustrates that input switched single phase AC-DC converter topologies can also be successfully used in input current shaping, input power factor improvement and efficiency improvement.

Input switched configurations have more diodes in the circuits than the output regulated circuits. However, the voltage stress across the switch of the input switched rectifiers is less than their output regulated counterparts. Further the study without feedback revealed that the input switched circuits have less input current THD than the output regulated circuits, hence it is expected that input regulated single phase AC-DC converters will require small input current filter for some input current ripple over sinusoidal shape. The same observation is applicable for output voltage filters of the two types of rectifiers.

5.2 Future Work

The contributions of this thesis indicate the opportunities of extending this work in future to meet other goals.

- Only simulation study is performed in this study. The proposed input switched AC-DC converter schemes may be implemented practically to investigate their actual potential. Such practical implementation would give further insight regarding the cost effectiveness of the proposed schemes compared to conventional PFC techniques of the similar types.
- Investigation can be made to improve quality of the gating signals at different duty cycle.
- Switching losses and EMI interference were not considered here. These can be investigated in future works.
- During the change of the output voltage by varying the duty cycle, it has been
 observed that the power factor also changes and becomes very low in some
 cases. To maintain the power factor unity at all duty cycle and output voltage,
 feedback control may be used as shown in the example of Boost PFC rectifier
 which will keep the power factor close to the unity and keep the THD and
 efficiency at acceptable levels.
- Concept of hybrid AC-DC converter technology may be studied using input switching technology to attain good performance at very low and at very high voltage attenuations/gains where component non-idealities play a major role.

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