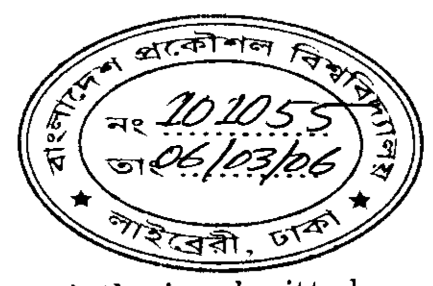
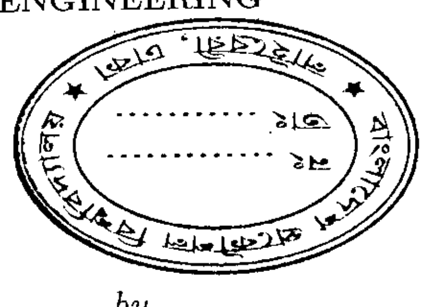
Modeling Electrostatic Properties of Strained-Si on SiGe MOS Devices



A thesis submitted

to the department of Electrical and Electronic Engineering of Bangladesh University of Engineering and Technology in partial fulfillment of the requirement for the degree of

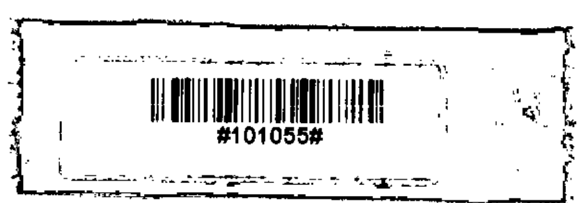
MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING



by

Abu Naser Md. Zainuddin

Department of Electrical and Electronic Engineering,
Bangladesh University of Engineering and Technology,
Dhaka-1000, Bangladesh,
December 2005.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The thesis titled **"Modeling Electrostatic Properties of Strained-Si on SiGe MOS Devices"** submitted by **Abu Naser Md. Zainuddin** Roll No.: 040406238P, Session: April, 2004 has been accepted as satisfactory in partial fulfillment of the requirements for the degree of **MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING** on December 13, 2005.

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Signature of the candidate

(Abu Naser Md. Zainuddin)

Dedication

To my parents and well wishers.

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Abstract

Electrostatic properties of deep submicron strained-Si (SS)/ $Si_{1-x}Ge_x$ (SiGe) n and p type MOS devices on (100) substrate have been studied under inversion gate voltage bias. Influence of strain on threshold voltage, gate capacitance and direct tunneling current has been modeled using a quantum mechanical (QM) approach. In addition, the threshold voltage is calculated with the help of a derived semiclassical model. In the QM model, potential profile has been calculated by solving the Schrödinger's and Poisson's equation self-consistently. During the self-consistent calculation wave function penetration int the gate dielectric has been considered. Schrödinger's equation has been solved by the method of Green's function formalism. The effect of dielectric constant change across SS/SiGe interface has been taken into account while solving the Poisson's equation numerically. Threshold voltage has been calculated based on the definition of equal current drive. It has been found that, in strained devices, threshold voltage reduces from that of unstrained devices. The reduction increases with increasing Ge-mole fraction (x), decreasing SS thickness (t_{Si}) and decreasing doping density. Moreover, consideration of SiGe dielectric constant further reduces the threshold voltage under strain. Inclusion of this effect has explained the mismatch between experiment and existing QM model. It has been also found that below a certain x and beyond a certain t_{Si}, the rather complex quantum mechanical model can be replaced by the derived simple semiclassical model in threshold voltage calculation. Results of C-V calculation has shown that for pMOS devices strained C-V characteristics differs from that of the unstrained one not only in threshold voltages but also in their shapes. The presence of a buried channel in SiGe near the SS/SiGe interface in pMOS is responsible for this difference. The degree of difference increases for higher strain, thinner SS layer and lower doping density. This difference is more prominent at moderate inversion than at high or low inversion level. Finally, tunneling current in SS-nMOS devices has been found to decrease with increasing x to increase in electron affinity. In SS-pMOS devices, due to nonmonotonic change in SS bandgap, tunneling current shows both an increasing and a decreasing trend depending on x.

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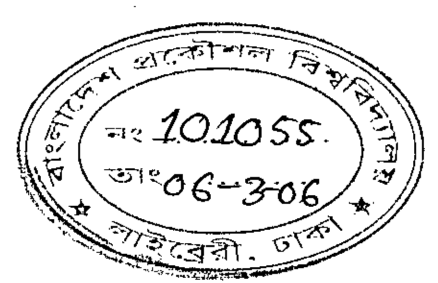
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Chapter 1

Introduction

Silicon CMOS technology has emerged over the last few decades as the predominant technology of the microelectronics industry. For almost four decades the rate of technological advances in Si MOS devices has followed Moore's Law anticipated by Gordon Moore in 1965 [1]. Since then, the geometric scaling of the MOS transistor has been the prime factor in integrated circuit design and fabrication. According to the recent forecast of International Technology Roadmap for Semiconductors (ITRS) 2004, relative chip static power dissipation with scaling for high performance logic will be 50 times higher in 2017 than the current value [2]. Consequently, to reduce chip static power as well as to increase transistor speed and simultaneously reduce the cost per function, state-of-the-art MOSFETs are now being fabricated with effective gate lengths of only a few tens of nanometers, pushing conventional Si-based technologies into the nanoelectronics regime [3]. For successful scaling of bulk-MOSFET to sub-100 nm feature sizes, several short channel effects, such as drain induced barrier lowering and inverse sub-threshold slope degradation, have to be minimized by a combination of increased channel doping, thinner gate oxide, reduced junction depths and lower power supply voltage [4]. Gate insulator thickness must decrease with the channel length to increase the drive current. But thinner gate oxides produce a higher degree of Si/SiO_2 interface roughness scattering. This, together with higher vertical field experienced by inversion layer channel carriers, due to higher substrate doping, leads to increased carrier scattering and ultimately lower channel mobility [5].

Moreover, below 2.5 nm oxide thicknesses, direct tunneling current (DT) increases rapidly, which is responsible for chip's standby power consumption and

thus limits the enhancement in oxide capacitance. The power supply voltage cannot be scaled down continuously without decreasing the threshold voltage, as this would reduce the drive current at saturation and again threshold voltage cannot be scaled down without resulting in an increased off-state leakage current.

Due to higher DT current and lower reliability, alternatives to SiO_2 as the gate insulator are under development, which achieve low effective oxide thickness by virtue of high permittivity. Unlike SiO_2, which is grown, these high-k dielectrics are usually deposited. This results in poor interface properties at the Si surface, leading to additional reductions in channel mobility.

By and large, the determining components of drive current- mobility of Si channel, oxide capacitance, channel length, power supply and threshold voltage are now in such status owing to aggressive scaling that further improvement in the performance of the bulk-Si devices entails serious complexities. Therefore new channel materials with advanced electronic properties are required in order for MOS devices to progress deeper into the Si nanoelectronics regime and maintain the rate of performance increases demanded by the ITRS [2]. Strained-Si channel on a relaxed SiGe buffer is one of the promising solutions to this problem.

1.1 Literature Review

Biaxially tensile strained-Si-SiGe (SS/SiGe) devices exhibit an improved electron and hole mobility and reduced threshold voltage characteristics, which ultimately enhances the drive current significantly. The SS/SiGe material system uses the 4.2% difference in the lattice constants of Si and Ge atoms to create nanoscale strain-engineered devices. Electron mobility is enhanced in strained Si compared with bulk Si due to tensile strain induced splitting of the six-fold degenerate conduction band valleys. This results in the two-fold bands with lower energy and reduced in-plane effective mass to be preferentially filled. Reduction of the in-plane effective mass of electrons enhance the electron mobility. Hole transport is improved in both tensile strained Si and compressively strained SiGe compared with bulk Si. The energy band offsets between strained and unstrained Si, Ge and SiGe alloys allow the confinement of carriers in high mobility epitaxial layers. Us-

ing the high mobility layers as the channel for MOSFET devices therefore leads to improved device performance without the need for expensive conventional scaling strategies. In the following paragraphs, the advent of SS/SiGe technology along with chronological research works are discussed in brief.

The built-in strain in the Si and SiGe two dimensional (2-D) layers has been first observed through Raman scattering experiments by Abstreiter *et al.* [6]. In spite of the large lattice mismatch of about 4% between Si and Ge, high-quality pseudomorphic growth of Si/SiGe multilayered structures were achieved by molecular beam epitaxy (MBE) in their work. Enhanced transport properties of (100) Si were studied by low temperature Hall measurements and Shubnikov-deHaas and cyclotron-resonance experiment. The results showed that splitting of 2-fold degenerate subbands into lower energy states increased the electron confinement, reduced in-plane carrier effective mass and carrier scattering due to tensile strain experienced in the Si layer. But the modeled band structure could not predict the mobility of Si channel and the valance band (VB) and conduction band (CB) offsets well.

A better approximation of valance band (ΔE_v) and conduction band (ΔE_c) discontinuities has been proposed for the first time by Van de Walle *et al.* [7] by self-consistent theory of atomic and electronic structure of pseudomorphic Si/Ge interfaces. They showed that these values were strongly dependent on strain. The shift and splitting of the bulk bands were expressed in terms of deformation potentials. Also the system types (I or II) were determined by properly lining up the strained layers as estimated from the value of ΔE_v. Both Abstreiter and Walle pointed that $\Delta E_c << \Delta E_v$. Tensile in-plane strain shifts down the 2-fold degenerate valleys which then become the energetically lowest CB states of the heterostructure. The smaller bandgap of the SiGe layers thus leads to a type-II band structure.

Since then, a lot of work has been done to identify the band structure and transport characteristics of SS/SiGe layers [8]-[11]. People studied the underlying physics of strain in Si/SiGe structures [8, 9]. On the other hand, Rieger and

Vogl proposed the band structure of biaxial tensile strained-SiGe on relaxed SiGe layer [10]. Both of them used multi-band **k.p** model. But the work of Fischetti and Laux [11] has been the most significant among these. They incorporated spin-orbit interaction into the multi-band **k.p** model making it more complete. In addition they theoretically predicted the mobility enhancement in SS channel.

From the fabrication point of view, Gibbons and his group for the first time in their Solid State Electronics Laboratory at Stanford University, fabricated both nMOS and pMOS transistors in various epitaxial layer structures containing SS active regions over relaxed SiGe substrate through CZ process [12, 13]. Later on, the same group for the first time fabricated and analyzed deep submicron SS n-MOSFETs to show the impact of strain on high field mobility due to shorter channel length [14, 15]. Recent studies on band structure and transport properties incorporates more complex features such as spin-orbit splitting [16], carrier scattering [16] and different substrate orientation [17] as well as quantum confinement modified by strain effects [18]. In all cases a full band Monte Carlo simulation have been performed to determine the device on-state current by improved modeling of mobility. Moreover, Takagi *et al.* [19] showed that (110)-surface strained-SOI n and pMOSFETs have much higher mobility over bulk-Si MOSFETs compared to other orientation.

Electrostatic behavior of SS MOS device has been partially studied by Oberhuber *et al.* [20] where inversion carrier distribution of SS PMOS is depicted. Through the 1-D self-consistent six-band **k.p** model they have analyzed the subband structure of SS layer and explained the effect of parasitic charge storage in SS-SiGe interface on the inversion layer densities in the potential profile. They also showed that the influence of the parasitic channel became negligible for high gate voltages (i.e. high inversion charge densities). Similar observations were reported by Yang and others [21] recently through similar procedure but for the scaled sub-100 nm regime SS/SiGe p channel MOSFETs. In this case the parasitic effect has been shown to be negligible for higher doping conditions also.

An important parameter for MOS devices is the threshold voltage (V_{TH}). V_{TH}

along with short channel effects were thoroughly studied under 1-D analytical and 2-D drift diffusion and hydrodynamic simulation by Sadek *et al.* [22]. Here SS layer appeared as a parasitic cap layer. Their electrostatic charge model revealed that V_{TH} in SS devices reduced with increasing SiGe spacer layer thicknesses and decreasing effective SiGe channel length. The reduction became insignificant for lower doping densities. They also studied electron and hole densities as a function of distance with the help of a 1-D self-consistent quantum mechanical model through which they predicted that these devices would show higher gate capacitance. But they have not actually calculated the gate capacitance and also their quantum mechanical model did not include wave function penetration effect and the effect of SiGe permittivity.

Reduction of V_{TH} and improvement of sub-threshold characteristics in SS MOS devices has been reported in Refs. [15, 23]. Goo *et al.* [23] suggested that reduction in threshold voltage is due to ΔE_v and subthreshold slope varies due to higher dielectric constants of SiGe layer along with shallower channel depletion depth (z_d). They also proposed that as $\Delta E_c << \Delta E_v$, pMOSFETs show smaller threshold voltage difference between SS and control-Si (ΔV_{TSS}) with negligible variation of subthreshold slope. Lower V_{TH} entails lower power supply voltage.

Models of V_{TH} in biaxially strained Si-SiGe devices have been proposed recently in the literatures [24, 25]. V_{TH} reduction has been attributed to both electron affinity and bandgap of the SS cap material and relaxed-SiGe substrate. Nayfeh *et al.* [24] proposed a semiclassically based model for SS nMOSFETs where extensive numerical simulation using MEDICI were performed for a wide range of channel doping density (N_a), oxide thickness (T_{OX}), Ge-fraction (x) and SS cap thickness t_{Si}. Their model suggests that ΔV_{TSS} increases with x and N_a. The increments are mainly due to the reduction of flat-band voltage (V_{FB}) in these devices. They also showed that, band offset between SS and SiGe layer created a charge dipole that resulted additional potential the gate must provide to achieve flat-band condition. As a consequence, V_{FB} reduces with increasing x and further exaggerated by increasing N_a.

On the other hand, Zhang and Fossum [25] proposed a quantum mechanical model to estimate ΔV_{TSS}. Analytical expressions for ΔV_{TSS} in both n type and p type MOSFETs have been derived based on the definition of equal current drive [44]. The expressions are indifferent for both $t_{Si} < z_d$ and $t_{Si} > z_d$ conditions where t_{Si} is the SS layer thickness. They proposed that, apart from the effect of increasing band offsets and narrowing bandgaps with increasing x in SS/SiGe devices, reduction in density-of-states (DOS) in SS layer with increasing x was also responsible for the increase in ΔV_{TSS}. Earlier, Lim *et al.* [26] in their work showed that uniaxial stress produced less threshold shift than biaxial stress in SS/SiGe devices due to greater reduction of DOS under biaxial stress than under uniaxial stress in the SS layer.

An essential topic of study for MOS devices is the gate capacitance-voltage (C-V) characteristics. Parameters like oxide thickness, substrate and poly-Si doping, band offset, mobility etc. are better estimated if the simulated C-V curve is in good agreement with the measured C-V curve. Though a significant amount of work has been done to model the transport characteristics, relatively less amount of work has been done on C-V modeling of SS MOSFETs. Sometimes in SS MOS devices C-V curves are used to facilitate the modeling of transport properties [27, 28]. The experimentally obtained C-V curves are also in general used to extract ΔE_v, Si-cap layer thickness, doping profile, threshold voltage, flat-band voltage and cross-over voltage in SS/SiGe MOS heterostructure for various Ge-concentrations [29]-[31]. In these cases, modeling is typically done with semi-classical commercial device simulators.

An interesting feature of the SS MOS C-V curve is the '*plateau*' phenomenon [29]-[32]. This is found under the accumulation bias of an SS nMOS device through a 1-D Poisson solver in [30]. Chottopadhyay *et al.* [31] found the plateau in both accumulation and inversion region of a SS/relaxed SiGe/SS/relaxed SiGe nMOS double quantum well structure. Armstrong *et al.* observed the kink in their experimentally obtained C-V curve of SS pMOS inversion layer and also obtained the same in semiclassically simulated C-V [29]. In all cases it has been believed that the hole confinement near SS/SiGe interface is responsible for these

plateaus. Also, no report has been found on the comparison of the kinks between accumulation and inversion region C-V curves.

Chandrashekhar *et al.* [32] recently proposed a semiclassical single-piece charge model over the entire accumulation/ depletion/ strong-inversion regions where flat-band voltages, surface potentials, bulk and inversion charges and capacitances are both physically derived and numerically validated through an unified regional charge based approach.

A quantum mechanical C-V model has been proposed by Cavassilas and Autran [33]. This is until now the only work that has discussed strained C-V characteristics through self-consistent quantum mechanical calculation. They calculated the band parameters through a multi-band **k.p** method and then introduced them into a 1-D Schrödinger-Poisson self-consistent solver to obtain the full C-V curve. They showed that strain linearly decreases the threshold voltage. The changes in the strained C-V curve from that of control-Si in the inversion region have been attributed to the reduction of bandgap with strain. A strong modification of hole effective mass in growth direction changes accumulation region characteristic. They also claimed that, this effective mass in the [100]-direction is not changed with strain. But they too did not consider wave function penetration effect and different dielectric constants in SS and SiGe regions.

Another important topic of study in deep submicron MOSFETs is the direct tunneling (DT) gate leakage current. Very few works have been done to study DT current of SS-pMOS and -nMOS devices. Takagi *et al.* [34] have found experimentally that gate tunneling current in nMOS device slightly decreases with an increase in strain and predicted that the increase in barrier height due to band splitting is responsible for it. Similar reasoning was used to explain the decrease in Fowler-Nordheim tunneling current in SS-nMOS devices [35].

1.2 Objective of the work

It is now established that SS MOS devices have emerged as a building-block for next generation CMOS devices. As a result, besides understanding the transport

behavior, study of electrostatic characteristics of SS MOS devices are necessary. Recent studies on V_{TH} [22]-[25], capacitance-voltage [27]-[33] and tunneling current [34, 35] are some evidences of such urgency. In most of the cases, analysis of SS MOS devices are based on semiclassical technique. These are performed by using numerical procedures with the help of commercial softwares. Consequently, many calculated parameters like surface potential (ϕ_S), voltage across oxide (V_{OX}), inversion carrier density (N_{INV}), total semiconductor charge (Q_{Sem}), flat-band voltage (V_{FB}) etc. do not include the essential physics of SS devices. While modeling V_{TH} either semiclassically [23, 24] or quantum mechanically [25], there are ambiguities in the attributes of reduction in V_{TH} which should be resolved. As MOS devices enter in to the deep submicron regime, quantum effects of inversion carriers become important. Also, ultrathin gate oxides have an adverse effect of high gate current due to the DT of inversion carriers. Therefore, modeling of nanoscale SS MOS devices should incorporate quantum mechanical corrections including wavefunction penetration effect into the gate oxide.

The objective of this study is to calculate the electrostatic properties of SS/SiGe n- and p-MOS devices for (100) orientation using an accurate, physically based, quantum-mechanical (QM) model as well as a simple semiclassically based, analytical model. The effect of the variation of the dielectric constant across SS/SiGe interface is explicitly taken into account in both models for the first time. The analytical model will be used for quick and reasonably correct estimation of SS MOS electrostatics, such as, for explaining the components in the reduction of V_{TH}. On the other hand, the self-consistent QM model will be used for quantitatively and accurately modeling SS MOS electrostatics. The model will be applied to explain a number of issues including mismatch between experimental and existing theoretical ΔV_{TSS}, C-V characteristics and direct tunneling current in SS MOS devices.

1.3 Organization of the Thesis

Chapter 2 reviews the strain induced changes in band structure and electrical properties of SS/SiGe. Chapter 3 reviews the theory of quantum mechanical analysis for MOS devices with modifications for SS/SiGe structures and also de-

scribes our derived semiclassical model for SS-nMOS devices. Chapter 4 presents the calculation of threshold voltage and the results and discussions of threshold voltage reduction in SS MOS devices based on both QM and semiclassical model. Chapter 5 narrates the gate capacitance calculation and the results and discussions for SS-pMOS device based on our QM model. Chapter 6 describes the QM calculation of DT current and the results and discussions for DT current in SS MOS devices. Summary of our work along with future directions have been presented in Chapter 7.

Chapter 2

Properties of Strained-Si on relaxed SiGe

2.1 Origin of strain in SS/SiGe structure

When a thin semiconductor epitaxial layer is grown pseudomorphically over a thick base layer (usually called the substrate) having different lattice constant from that of the epitaxial layer, the thin film experiences strain. Depending upon the lattice constant of the strained layer, two types of strain are introduced, namely, *tensile* and *compressive* strain. Fig. 2.1 shows an illustration of two different types of strain.

If the strained layer has a smaller native lattice constant than the bulk, we get biaxial tensile strain, whereas for the strained layer having a larger native lattice constant than the substrate gives compressive strain. When a film is grown on a substrate, the film is stressed and deformed to take the lattice constant of the bulk at the plane parallel to the interface. In the perpendicular direction the lattice constant of the strained film is different than that of the bulk.

Biaxial tension in the epitaxial layer is a case, where the unit cell of the strained layer is under tension in the in-plane direction (XY plane, perpendicular to the growth direction Z). To keep the volume the same as that of unstrained case, the cell undergoes compression in the out-of-plane direction (parallel to the growth direction Z). Similar situation is observed when Si is grown epitaxially in (100) plane on a relaxed SiGe buffer fabricated gradually on a (100) Si substrate (Fig. 2.2). The film stays strained upto a critical strain energy and critical

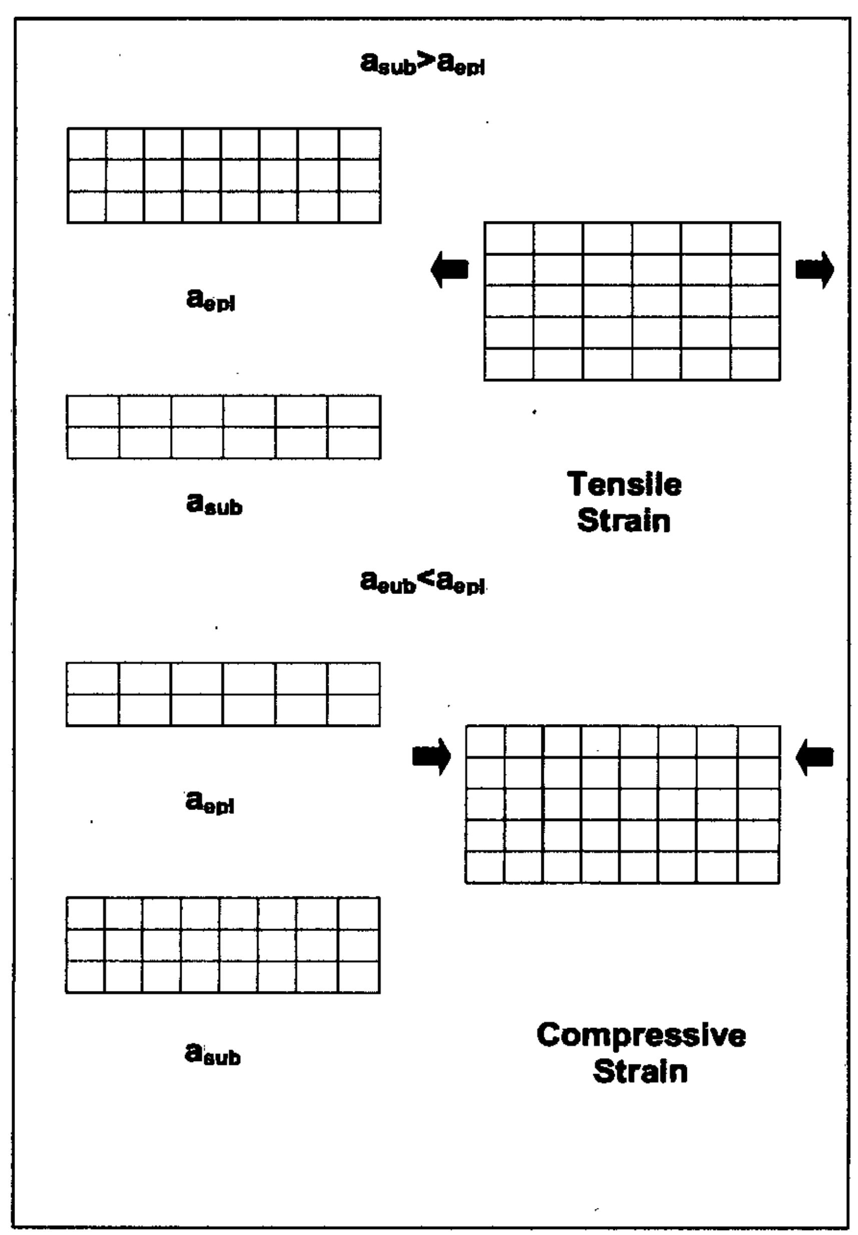


Figure 2.1: Origin of strain in thin epitaxial layer.

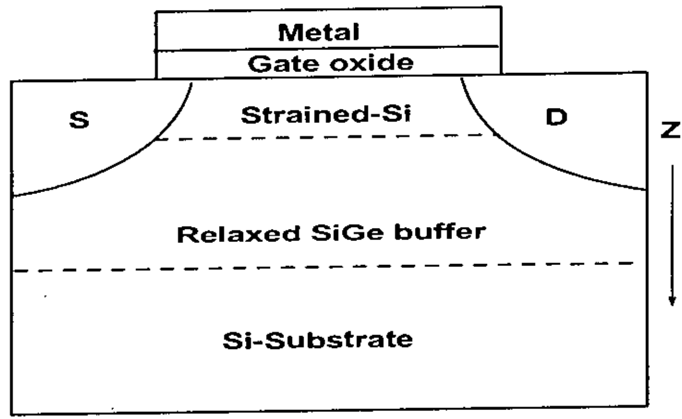


Figure 2.2: Schematic diagram of strained-Si MOSFET.

thickness. Above the energy and thickness limits it tends to relax forming crystal defects.

From Fig. 2.3(a) and (b) it is seen that the lattice constant of Si film conforms to that of the SiGe layer and the lattice mismatch between Si and SiGe leads to a biaxial tensile strain in the Si layer. If the SiGe is fully relaxed and the Si layer fully strained, the amount of strain in Si in the in-plane direction ($\epsilon_{\|}$) can be found from the following relation,

$$\epsilon_{\|} = \frac{a_{\mathrm{SiGe}} - a_{\mathrm{Si}}}{a_{\mathrm{Si}}} \tag{2.1}$$

then multiplying it with the Poisson's ratio (ρ) we obtain the amount of strain in the out-of-plane direction ($\epsilon_{\perp}$) from the following relation,

$$\epsilon_{\perp} = -\rho\epsilon_{\|}. \tag{2.2}$$

The lattice parameter of SiGe layer can be found from Vegard's law [10],

$$a_{\mathrm{SiGe}} = a_{\mathrm{Si}} + (a_{\mathrm{Ge}} - a_{\mathrm{Si}})x \tag{2.3}$$

where x is the Ge-mole fraction in the SiGe layer. So, the amount of strain in Si is approximately $4.2\times x\%$.

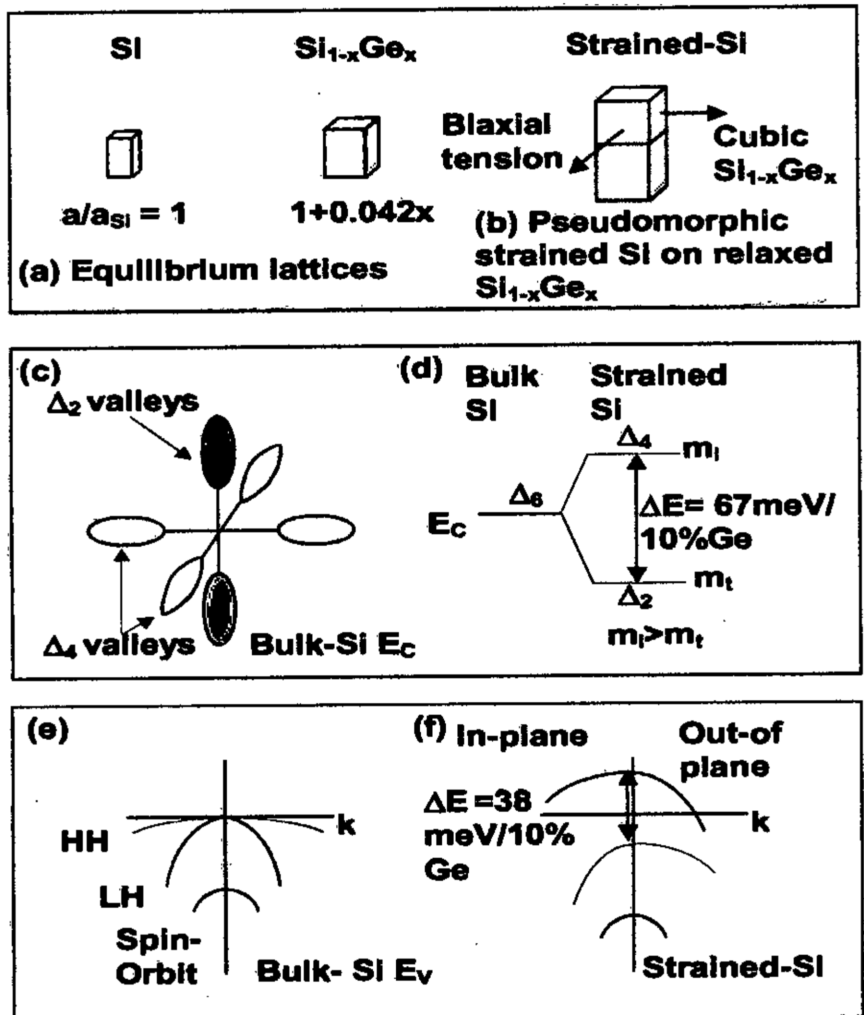


Figure 2.3: Strain is induced due to lattice mismatch (a),(b); splitting of conduction band valleys (c),(d); splitting of valance band edges (e),(f).

2.2 Band structure and transport properties

From now on the changes in band structure and electronic properties of Si/SiGe heterostructure under tensile strain will be concentrated. The noticeable differences between these two structures are the offsets of conduction and valence bands, ΔE_C and ΔE_V. For the tensile strained structure, large band offsets occur in both the valence and conduction bands. The band alignment is referred to as Type II. For large offsets in both the valence and conduction bands, this technology is attractive for both electron and hole confinement. So, both n-channel and p-channel high mobility MOSFETs can be achieved by tensile strained Si structures.

How the band offsets effect mobility and transport properties of electrons and holes needs clear understanding of the physics related to the valence and conduction bands of strained and unstrained materials. From device physics we know that lowering carrier effective mass and minimization of intervalley scattering are required for enhancement of carrier mobility.

Fig. 2.3(c) and (d) show the minimum energy conduction band valleys for strained Si. For unstrained bulk-Si, the minimum energy is six-fold degenerate. Electrons occupy the six-fold degenerate valleys with equal probability. Tensile strain splits the sixfold degeneracy of bulk-Si, and lowers the two fold degenerate perpendicular Δ-valleys (Δ_2) with respect to the four fold degenerate in-plane Δ-valleys (Δ_4). Such energy splitting causes preferential occupation of the Δ_2 valleys where the in-plane conduction mass is lower and suppresses inter-valley scattering between the Δ_2 and Δ_4 valleys. These two effects lead to increased electron mobility [11], [12], [14], [19].

Effective mass of an electron in a conduction band valley is directionally dependent. So, redistribution of electrons to different energy valleys because of strain causes the effective transport mass of those electrons to change. This can be understood through the concept of conductivity effective mass. The longitudinal mass m_l and transverse mass m_t of an electron in a conduction band energy

valley of Si are as follows,

$$m_l = 0.91m_0 \tag{2.4}$$

$$m_t = 0.19m_0 \tag{2.5}$$

Here, m_0 is the electron rest mass. The conductivity mass m_σ for unstrained Si is given by the equation,

$$\frac{1}{m_\sigma} = \frac{1}{3}\left(\frac{1}{m_l} + \frac{2}{m_t}\right) \tag{2.6}$$

According to this equation, we get the conductivity effective mass to be $0.26m_0$ for unstrained Si. This formula cannot be directly applied to strained Si cases. For, biaxial tensile strain, the effective in-plane mass will be the transverse effective mass in Si which is $m_t = 0.19m_0$. So, biaxial tensile strain helps to reduce the effective mass of electron and thus contribute to higher electron mobility. Splitting of six-fold degenerate conduction band valleys by strain also leads to reduction in allowable states to which carriers may scatter. This helps to reduce intervalley optical phonon scattering. Minimized scattering also helps to boost electron mobility.

Fig. 2.3(e) and (f) illustrates the E vs. k diagrams for Si valence band at unstrained and biaxially strained conditions. For the unstrained case, the valence band maxima has three bands, the degenerate heavy-hole (HH) and light-hole (LH) bands and the split-off (SO) band which is slightly lower in energy than the other two bands. Heavy-hole and light-hole refer to the effective masses of the holes in each band.

The relationship between effective mass (m^*) and E vs. k dispersion curve is given by,

$$m^* = \hbar^2 \left(\frac{\partial^2 E}{\partial k^2}\right)^{-1} \tag{2.7}$$

From Fig. 2.3(e) and Eq. (2.7) it can be seen that the HH band should have a higher effective mass than the LH band for unstrained case. Strain splits the valance band degeneracy at the zone center and shifts the spin-orbit (SO) band. The degenerated HH and LH bands split into higher LH and lower HH bands respectively. So interband phonon scattering between HH, LH and SO bands reduces. The higher LH band has a higher occupancy of holes in comparison

Table 2.1: Band parameters of SS and SiGe regions [8, 24].

Parameters	Values
χ_{SS} (eV)	$4.05+0.58x$
E_{gSS} (eV)	$1.084-x(0.31+0.53x)$
ϵ_{SS}	11.9
χ_{SiGe} (eV)	$4.05-0.05x$
ϵ_{SiGe}	$11.9+4.1x$
E_{gSiGe} (eV)	$1.084-0.420x$
ΔE_C (eV)	$0.63x$
ΔE_V (eV)	$x(0.74 - 0.53x)$

Table 2.2: Band splitting in SS region [38, 24].

Parameters	Values (eV)
Δ_2-Δ_4 split	$0.67x$
LH-HH split	$0.4x$
LH-SO split	$0.11x+0.044$

to HH band. Moreover, it has higher curvature in the in-plane direction than the bulk-Si case. Higher curvature entails lower effective mass in the in-plane direction. All these lead to an increase in hole mobility [11], [36].

2.3 Band diagram of SS/SiGe heterostructure

In Fig. 2.4 the band diagram of strained-Si-SiGe MOSFET has been shown under flat-band condition. Here ϕ_m, χ_{SS} and χ_{SiGe} are the metal work function and electron affinities of SS and SiGe layers respectively. E_{OX}, E_{gSS} and E_{gSiGe} are the bandgaps of oxide, SS and SiGe layers respectively. t_{OX} and t_{SS} are the oxide and strained-Si thicknesses correspondingly. The various band parameters and electron effective masses have been obtained from [8], [11], [24] and [33]. To find the hole effective masses of both SS and SiGe region, the well known Luttinger parameters γ_1, γ_2 and γ_3 have been used [37], [38].

Tables 2.1 and 2.2 list the band parameters of SS and SiGe layers. Bowing effect is considered in E_{gSS}. Different effective masses of electrons and holes of SS and SiGe regions are provided in Tables 2.3 and 2.4.

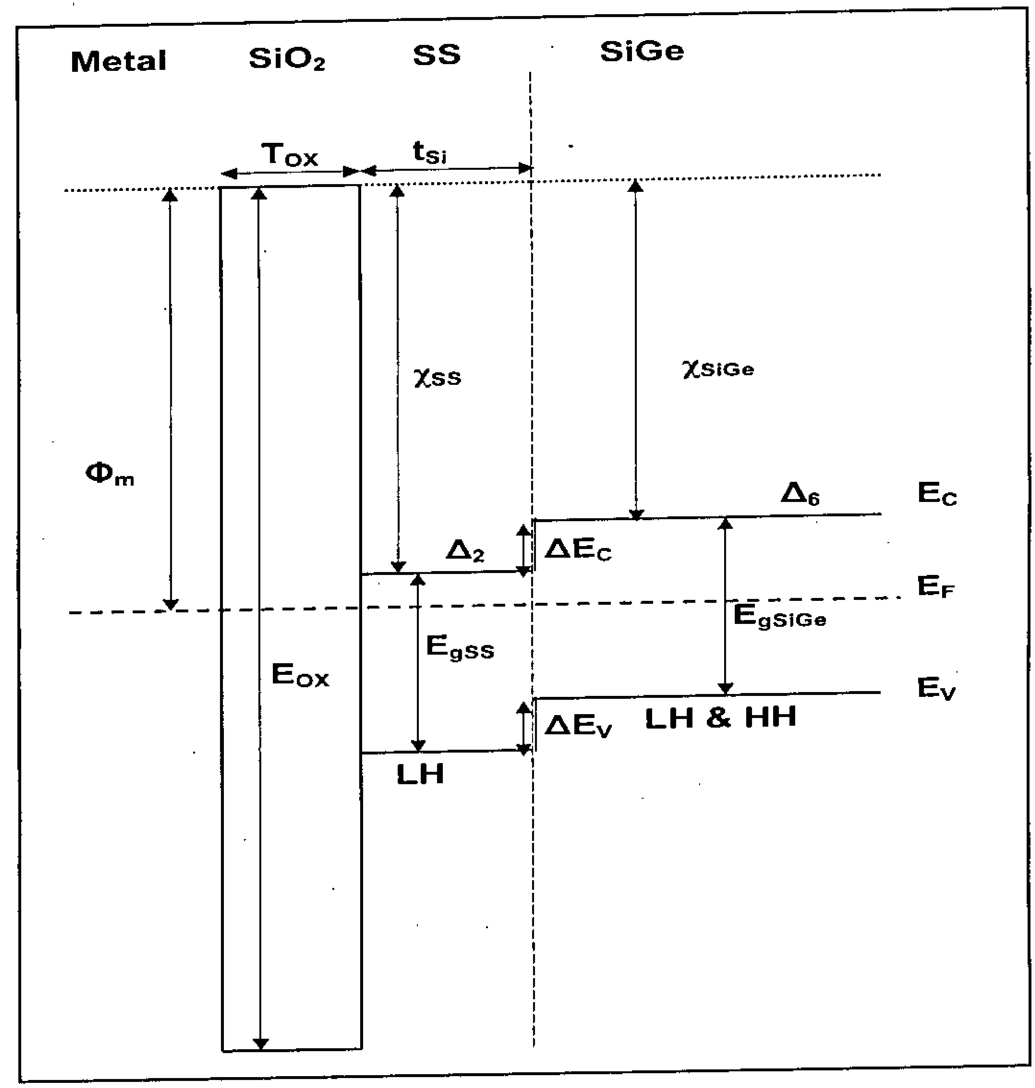


Figure 2.4: Band Diagram for Si-SiGe MOSFET under flat-band condition.

Table 2.3: Effective masses of electrons in different valleys [11, 33].

Valleys	Longitudinal		Transverse	
Degeneracy	2		4	
Normal mass (m_z/m_0)	0.916		0.190	
In-plane mass($/m_0$)	m_{2X}	m_{2Y}	m_{4X}	m_{4Y}
	0.190	0.190	(-0.012x+0.916)	(-0.005x+0.190)
DOS-mass (m_d/m_0)	$\sqrt{m_{2X}m_{2Y}}$		$\sqrt{m_{4X}m_{4Y}}$	

Table 2.4: Luttinger parameters for Si, Ge and SiGe [37, 38].

Symbols	Si value	Ge value	$Si_{1-x}Ge_x$ value
γ_1	4.22	13.35	4.22(1-x)+ 13.35x
γ_2	0.39	4.25	0.39(1-x)+ 4.25x
γ_3	1.44	5.69	1.44(1-x)+ 5.69x

Table 2.5: Hole effective masses in SS and SiGe regions [38].

	Normal mass(m_z/m_0)	DOS-mass (m_d/m_0)
HH (m_h/m_0)	$1/(\gamma_1 - 2\gamma_2)$	$1/(\gamma_1 + \gamma_2)$
LH (m_l/m_0)	$1/(\gamma_1 + 2\gamma_2)$	$1/(\gamma_1 - \gamma_2)$
SO (m_s/m_0)	$1/\gamma_3$	$1/(\gamma_1 + \gamma_2)$

Chapter 3

Theory

In this chapter the theory used to analyze SS/SiGe MOS devices has been presented. The methodologies include a quantum mechanical analysis and our derived semiclassical analysis.

3.1 Quantum Mechanical Analysis

The quantum effect in the MOS devices becomes important when the feature size is reduced below 100 nm. Higher doping density is required to avoid short channel effects in these devices which results in a higher surface electric field. The quantization of inversion layer carriers occurs due to the presence of high electric field at the surface of the semiconductor. In this section the quantum mechanical treatment for SS/SiGe MOS devices has been reviewed as developed in [39].

3.1.1 Schrödinger-Poisson self consistent solution

Stern [40] proposed the solution of coupled Schrödinger's and Poisson's equations for analysis of MOS inversion layer. The important assumptions made by him are,

a) The effective mass approximation is valid, so that periodic potential can be neglected.

b) The envelope function vanishes at the Si-SiO_2 interface.

The band bending of a SS/SiGe semiconductor heterostructure can be characterized by a potential $\phi(z)$. Fig. 3.1 shows a typical energy band diagram for an nMOS inversion layer.

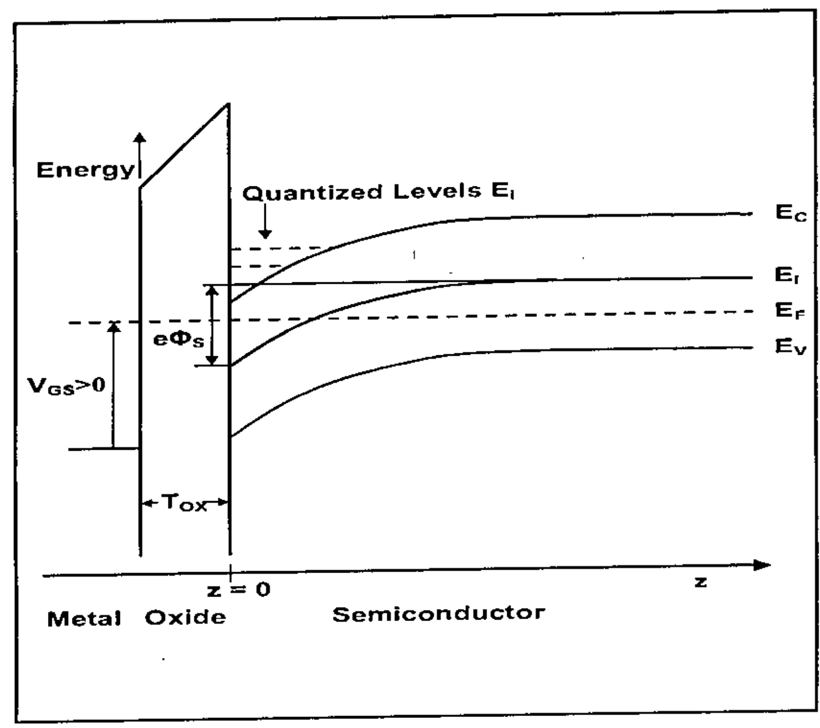


Figure 3.1: Typical band diagram for an nMOS inversion layer.

In the effective mass approximation, the electronic wavefunction for the ith subband is the product of the Bloch function at the bottom of the conduction band and the corresponding envelope function. Envelope function ψ(z) is the solution of,

$$\frac{d^2\psi(z)}{dz^2} + \frac{2m_z^*}{\hbar^2}[E_i + e\phi_{SS}(z)]\psi(z) = 0 \tag{3.1}$$

Here m_z^* is the effective mass in the direction perpendicular to the interface and E_i is the energy of the ith bound state in the state in the same direction. Closed boundary conditions commonly used for the solution of Eq. (3.1) are,

i) deep inside the bulk SiGe, $\psi(\infty) = 0$ and

ii) at the semiconductor-oxide interface, $\psi(0) = 0$.

Each solution of Eq. (3.1) gives the bottom of a continuum of levels called a subband. In the effective mass approximation of SS layer, the conduction band valleys are degenerate in pairs. Solution of Eq. (3.1) gives the eigenenergy E_i and the envelope function ψ(z). The potential ϕ(z) is found from the solution of

Poisson's equation, which is as follows,

$$\frac{d^2\phi(z)}{dz^2} = -\frac{[\rho_d(z) - e\sum_i N_i\psi^2(z)]}{\epsilon_{SS}\epsilon_0}, \quad 0 < z < t_{Si}$$
$$= -\frac{[\rho_d(z) - e\sum_i N_i\psi^2(z)]}{\epsilon_{SiGe}\epsilon_0}, \quad z > t_{Si} \tag{3.2}$$

here, ϵ_{SS} and ϵ_{SiGe} are the dielectric constants of SS and SiGe regions respectively and ϵ_0 is the absolute permittivity constant. N_i is the carrier concentration in the ith subband. N_i is given by the following equation,

$$N_i = \frac{n_{vi}m_{di}kT}{\pi\hbar^2}\ln\left[1 + \exp\left(\frac{E_F - E_i}{kT}\right)\right] \tag{3.3}$$

where n_{vi} is the valley degeneracy of the ith valley, m_{di} is the density of states effective mass per valley and E_F is the Fermi energy. ρ_d is the charge density in the depletion layer, which is taken to be,

$$\rho_d(z) = -e(N_A - N_D), 0 < z < z_d$$
$$= 0, \quad z > z_d \tag{3.4}$$

here, z_d is the depletion layer thickness. Neglecting the inversion charge density in Eq. (3.2) it can be shown that,

$$z_d = \sqrt{\frac{2\epsilon_{SS}\epsilon_0\phi_{dSS}}{e(N_A - N_D)}}, \quad \text{if } z_d < t_{Si}$$
$$= t_{Si} + \sqrt{\frac{2\epsilon_{SiGe}\epsilon_0\phi_{dSiGe}}{e(N_A - N_D)}}, \quad \text{if } z_d > t_{Si} \tag{3.5}$$

ϕ_{dSS} and the ϕ_{dSiGe} are the band bending due to depletion charge only in the SS and SiGe regions, respectively. ϕ_{dSiGe} and ϕ_{dSS} can be calculated from as,

$$\phi_{dSiGe} = \frac{eN_d}{2\epsilon_{SiGe}\epsilon_0}(z_d - t_{Si})^2,$$
$$\phi_{dSS} = \phi_{SS} - \left[\frac{eN_d}{2\epsilon_{SS}\epsilon_0}z_d^2 - \phi_{dSiGe}\right] - \frac{kT}{e} - \frac{eN_{INV}Z_{avg}}{\epsilon_{SS}\epsilon_0}, \tag{3.6}$$

where ϕ_{SS} is the total semiconductor band bending at the SS-SiO_2 interface, $N_{INV} = \sum_i N_i$ is the total number of charge per unit area in the inversion layer and Z_{avg} is the average penetration of inversion charge density into SS layer. The two boundary conditions conventionally used for solution of Eq. (3.2) are,

i) for large z (at $z \geq z_d$) $d\phi/dz = 0$ and

ii) at the surface, $d\phi/dz = F_S$.

Here, F_S is the electric field at the oxide-semiconductor interface and is given by,

$$F_S = \frac{e(N_{INV} + N_{dep})}{\epsilon_{SS}\epsilon_0} \tag{3.7}$$

$N_{dep} = z_d(N_A - N_D)$ is the number of charge per unit area in the depletion layer. In a self-consistent formulation, Eqs. (3.1) - (3.6) are solved iteratively for a given F_S until results converge.

3.1.2 Transmission Line Analogy

The general procedure to solve Schrödinger's equation involves rigorous matrix manipulation. Among various simple techniques, one approach considers transmission line concept of microwave engineering which is discussed here. In addition to this technique, later Green's function is introduced to calculate eigenenergies and wave functions.

Transmission line analogy to solve Schrödinger's equation is described briefly as follows [41]. The well known equations for voltage (V) and current (I) used in transmission line theory are,

$$\begin{aligned} I(z) &= I^+(e^{\gamma_t z} - \Gamma_t e^{-\gamma_t z}), \\ V(z) &= I^+ Z_0(e^{\gamma_t z} + \Gamma_t e^{-\gamma_t z}) \end{aligned} \tag{3.8}$$

where γ_t is the propagation constant and Γ_t is the wave amplitude reflection coefficient. Z_0 is the characteristics impedance of the transmission line.

If an electron with an energy E is incident on the potential barrier shown in Fig. 3.2, the corresponding wave function can be expressed as,

$$\psi(z) = A^+(e^{\gamma z} - \rho e^{\gamma z}) \tag{3.9}$$

where γ is the propagation constant and ρ is the wave amplitude reflection coefficient. If a function, $\zeta(z)$ is defined as

$$\zeta(z) = \frac{2\hbar}{im^*}\frac{d\psi}{dz} \tag{3.10}$$

then,

$$\zeta(z) = A^+ Z_0(e^{\gamma z} + \rho e^{-\gamma z}) \tag{3.11}$$

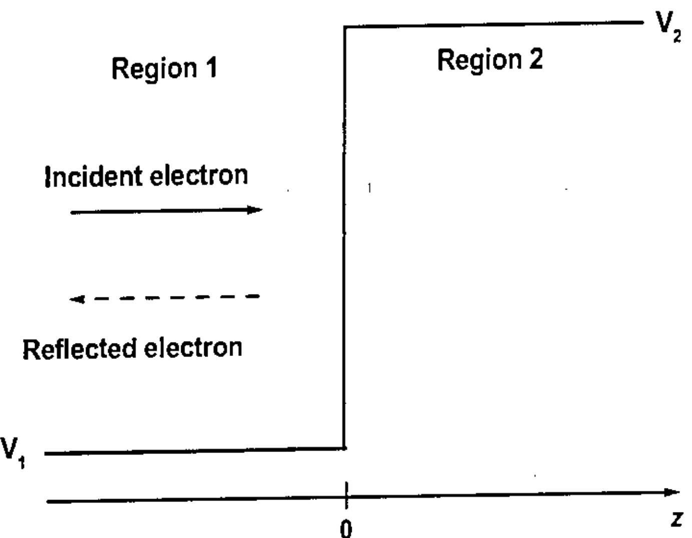


Figure 3.2: A potential barrier with an incident electron (solid line) and the reflected wave (dashed line).

where,

$$Z_0 = \frac{2\gamma\hbar}{im^*} \tag{3.12}$$

Now, an analogy is found between voltage and current expressed by Eqs. (3.8) with ζ and ψ expressed by Eqs. (3.11) and (3.9), respectively. Since, the transmission line impedance is the ratio of V and I, so the ratio of ζ and ψ is called as wave impedance by using this analogy. Moreover, ζ and ψ are continuous across the boundary between the two regions, which directly corresponds to transmission line boundary conditions. All these lead to a conclusion that a quantum mechanical wave impedance concept can be introduced analogous to transmission line impedance as given by at any plane z,

$$Z(z) = \frac{\zeta(z)}{\psi(z)} \tag{3.13}$$

Thus transmission line concept can be applied for quantum mechanical calculations. For example, the input impedance, Z_i at $z = -l$ may be expressed in terms of load impedance, Z_l at $z = 0$ as in transmission line,

$$Z_i = Z_0 \frac{Z_l \cosh(\gamma l) - Z_0 \sinh(\gamma l)}{Z_0 \cosh(\gamma l) - Z_l \sinh(\gamma l)}. \tag{3.14}$$

If at any energy the wave impedances looking to the right (positive direction) and to the left (negative direction), at any plane z are equal, i.e

$$Z_{iR} = Z_{iL} \tag{3.15}$$

the corresponding energy is the eigenenergy of the arbitrary quantum well.

3.1.3 Green's Function Formalism

Green's function formalism is used along with the transmission line analogy to calculate easily the normalized wave functions in arbitrary 1-D quantum well structures [42]. In this formalism the quantum mechanical wave impedance is redefined in terms of the logarithmic derivative of the retarded Green's function, G^R as,

$$Z(z,z';E) = \frac{2\hbar}{im_z^*}\left[\frac{\partial G^R(z,z';E)}{\partial z}/G^R(z,z';E)\right] \tag{3.16}$$

where G^R satisfies the equation,

$$\left[E + \frac{\hbar^2}{2m_z^*} - V(z) + i\epsilon\right] G^R(z,z';E) = \delta(z-z') \tag{3.17}$$

where ϵ is an infinitesimally small positive energy and m_z^* is the z- direction effective mass. $V(z)$ is the potential along z-direction. The Green's function in this context is discussed in detail in Ref. [43].

Wave impedance $Z(z,z';E)$ has a discontinuity at $z = z'$, and one needs two boundary conditions to determine $Z(z,z';E)$. To obtain these boundary conditions, the potential profile is assumed flat sufficiently far from $z = z'$ in both directions. If V_R is the constant potential at $z = \infty$ and if V_L is the constant potential at $z = -\infty$, the Green's function in these regions can be expressed as [42],

$$\begin{aligned} G^R(z\to\infty,z';E) &\approx e^{\gamma_R(z-z')} \\ G^R(z\to-\infty,z';E) &\approx e^{-\gamma_L(z-z')} \end{aligned} \tag{3.18}$$

where

$$\gamma_{R(L)} = i\sqrt{\frac{2m^*}{\hbar^2}(E - V_{R(L)})} \tag{3.19}$$

$\gamma_{R(L)}$ is imaginary if $E > V_{R(L)}$, else this is real. From the above relationships, the boundary conditions are found as

$$\begin{aligned} Z(z\to\infty,z';E) &= Z_0(\infty) \\ Z(z\to-\infty,z';E) &= -Z_0(-\infty) \end{aligned} \tag{3.20}$$

where

$$Z_0(\pm\infty) = \frac{2\hbar}{im_z^*}\gamma_{R(L)} \tag{3.21}$$

From the properties of the Green's functions it can be shown that [43],

$$\begin{aligned} Z(z, z'; E) &= Z_{iR}(z; E) \text{ for all } z' < z \\ Z(z, z'; E) &= Z_{iL}(z; E) \text{ for all } z' > z. \end{aligned} \tag{3.22}$$

It is noteworthy that $Z_{iR}(Z_{iL})$ does not depend on z' as long as $z > z'$ $(z < z')$ as $\delta(z - z') = 0$ for $z \neq z'$. Using transmission line analogy, $Z_{iR}(Z_{iL})$ can be calculated. The eigenenergies of an arbitrary quantum well can be determined using following condition,

$$Z_{iR}(z; E) = Z_{iL}(z; E) \tag{3.23}$$

From transmission line analogy, at any eigenenergy and for all values of z inside the quantum well the above equation must be satisfied. Once an eigenenergy is found, the corresponding normalized wavefunction can be calculated using the following relationship,

$$|\psi_n(z)|^2 = \frac{4\epsilon}{\hbar}\Im m\left[\frac{i}{Z_{iR}(z; E_n) - Z_{iL}(z; E_n)}\right] \tag{3.24}$$

The position dependent one dimensional (1-D) DOS $(N(z; E))$ is given by,

$$N(z; E) = \frac{4\epsilon}{\pi\hbar}\Im m\left[\frac{i}{Z_{iR}(z; E) - Z_{iL}(z; E)}\right] \tag{3.25}$$

Eqs. (3.23) and (3.24) are used to find the eigenenergies and wavefunctions in MOS inversion layers, respectively. Here the wavefunction is subject to open boundary conditions, assuming the potential barrier at SS-SiO_2 interface has a finite height and width. As a result the technique incorporates wavefunction penetration effects into the dielectric material. Through realistic boundary conditions instead of invoking some mathematical artifact. The effect of considering wave function penetration effect is shown in Fig. 3.3 for a typical MOS inversion layer. Here it can be seen that inversion charge distribution has a tail into the dielectric region indicating the effect of considering an open boundary condition while solving the Schrödinger's equation.

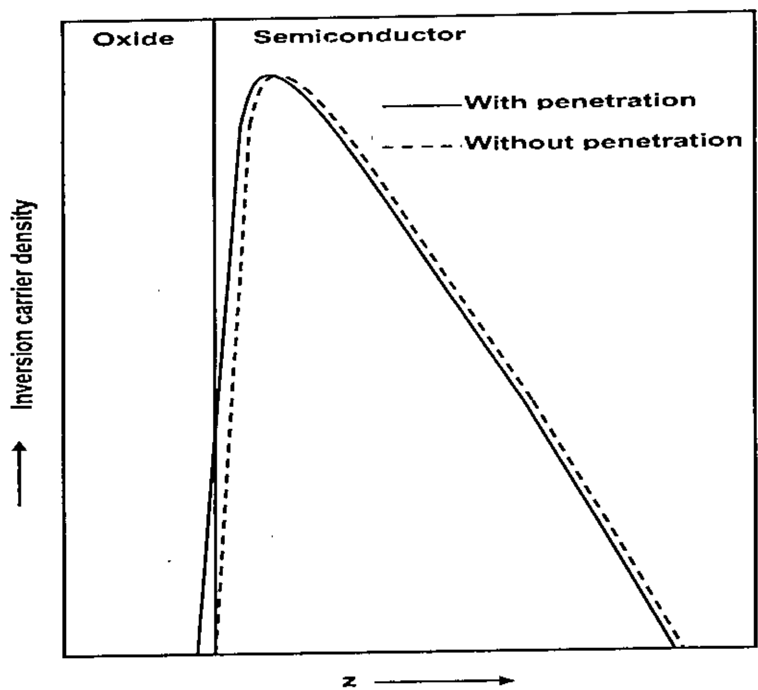


Figure 3.3: Inversion charge exists in the oxide region when the wave function penetration effect is considered in Schrödinger-Poisson self-consistent calculation.

3.2 Semiclassical Analysis

The analysis of MOS device is often done through semiclassical approach. In semiclassical analysis, the inversion layer charge is considered to be a sheet charge of negligible thickness located near the oxide-semiconductor interface. For relatively lower surface electric field or thicker dielectric material the quantization effects of electrons or holes are suppressed. Therefore, carrier concentration in the inversion layer can be estimated through semiclassical approach along with Fermi-Dirac statistics.

Although semiclassical analysis is less accurate than quantum mechanical analysis for modern submicron devices, this method has the advantages of simplicity and negligible computational time. Therefore, semiclassical approach is useful for making a quick, qualitative analysis. In this section a total semiconductor charge equation for SS/SiGe nMOS structure is derived.

3.2.1 Expression for total semiconductor charge

SS and SiGe layers differ in band gaps, electron affinities and also in dielectric constants. The intrinsic carrier concentrations n_{iSS} and n_{iSiGe} for the SS and SiGe regions respectively are,

$$\begin{aligned} n_{iSS} &= \sqrt{N_{vSS}N_{cSS}}\ e^{\left(\frac{-E_{gSS}}{2\phi_t}\right)} \\ n_{iSiGe} &= \sqrt{N_{vSiGe}N_{cSiGe}}\ e^{\left(\frac{-E_{gSiGe}}{2\phi_t}\right)}. \end{aligned} \quad (3.26)$$

where N_{cSSi}, N_{cSiGe} and N_{vSSi}, N_{vSiGe} are the effective density of states of electrons and holes, respectively and ϕ_t is the thermal potential. An average intrinsic carrier concentration n_{iS} would be,

$$n_{iS} = \sqrt{n_{iSS}n_{iSiGe}} \quad (3.27)$$

The Poisson's equation for an nMOS device along the confinement direction z can be represented as,

$$\begin{aligned} \frac{d^2\phi}{dz^2} &= \frac{eN_a}{\epsilon_{SS}\epsilon_0}\left[1 + \frac{n_{iS}}{N_a}\exp\left(\frac{\phi - \phi_b}{\phi_t}\right)\right], && 0 < z < t_{Si} \\ \frac{d^2\phi}{dz^2} &= \frac{eN_a}{\epsilon_{SiGe}\epsilon_0}, && t_{Si} < z < z_d \end{aligned} \quad (3.28)$$

where N_a is the doping density of semiconductor and the Fermi potential ϕ_b is given by,

$$\phi_b = \phi_t \ln\left(\frac{N_a}{n_{iS}}\right) \quad (3.29)$$

Eq. (3.28) is based on the following assumptions,

i) inversion layer band bending is due to only electrons and negatively charged ions; contribution of holes or positive ionic charge is insignificant,

ii) inversion carriers are confined mostly to SS regions.

Integrating Eq. (3.28) from $z = t_{Si}$ to $z = z_d$ we obtain,

$$\left[\frac{d\phi}{dz}\right]_{z_d} - \left[\frac{d\phi}{dz}\right]_{t_{Si}} = \left[\frac{eN_a z}{\epsilon_{SiGe}\epsilon_0}\right]_{t_{Si}}^{z_d}, \quad (3.30)$$

but at $z = z_d$, $[d\phi/dz] = 0$. So Eq. (3.30) is simply,

$$\left[\frac{d\phi}{dz}\right]_{t_{Si}} = -\frac{eN_a(z_d - t_{Si})}{\epsilon_{SiGe}\epsilon_0} = -\frac{eN_a z_{ds}}{\epsilon_{SiGe}\epsilon_0} \quad (3.31)$$

Putting appropriate boundary conditions, integration of Eq. (3.31) gives electrostatic potential at SS-SiGe interface, ϕ_{SiGe}, such that,

$$\phi_{SiGe} = \frac{eN_a z_{ds}^2}{2\epsilon_{SiGe}\epsilon_0} \tag{3.32}$$

or

$$z_{ds} = \sqrt{\frac{2\epsilon_{SiGe}\epsilon_0\phi_{SiGe}}{eN_a}}. \tag{3.33}$$

Here z_{ds} is the depletion width in the SiGe region.

Now, multiplying Eq. (3.31) by $\epsilon_{SiGe}\epsilon_0$ and putting the value of z_{ds}, it is found,

$$\left[\epsilon_{SiGe}\epsilon_0\frac{d\phi}{dz}\right]^2_{t_{Si}} = (2e\epsilon_{SiGe}\epsilon_0 N_a)\phi_{SiGe} \tag{3.34}$$

As we know that

$$\left(\frac{d\phi}{dz}\right)\frac{d^2\phi}{dz^2} = \frac{1}{2}\frac{d}{dz}\left(\frac{d\phi}{dz}\right)^2$$

, then Eq. (3.28) can be simplified

$$\begin{aligned}
\frac{1}{2}\frac{d}{dz}\left(\frac{d\phi}{dz}\right)^2 &= \frac{eN_a}{\epsilon_{SS}\epsilon_0}\left[1+\frac{n_{iS}}{N_a}\exp\left(\frac{\phi-\phi_b}{\phi_t}\right)\right]\left(\frac{d\phi}{dz}\right)\\
&= \frac{eN_a}{\epsilon_{SS}\epsilon_0}\left[1+\left(\frac{n_{iS}}{N_a}\right)^2\exp\left(\frac{\phi}{\phi_t}\right)\right]\left(\frac{d\phi}{dz}\right)
\end{aligned}$$

substituting ϕ_b

$$= \frac{eN_a}{\epsilon_{SS}\epsilon_0}\frac{d}{dz}\left[\phi+\phi_t\left(\frac{n_{iS}}{N_a}\right)^2\exp\left(\frac{\phi}{\phi_t}\right)\right]. \tag{3.35}$$

Again integrating Eq. (3.35) from $z=0$ to $z=t_{Si}$ we get,

$$\left(\frac{d\phi}{dz}\right)^2_{t_{Si}} - \left(\frac{d\phi}{dz}\right)^2_0 = \frac{2eN_a}{\epsilon_{SS}\epsilon_0}\left[\phi_{SS}+\phi_t\left(\frac{n_{iS}}{N_a}\right)^2\exp\left(\frac{\phi_{SS}}{\phi_t}\right)\right]_0^{t_{Si}} \tag{3.36}$$

Multiplying Eq. (3.36) by $(\epsilon_{SS}\epsilon_0)^2$ and putting the boundary values we have,

$$\left(\epsilon_{SS}\epsilon_0\frac{d\phi}{dz}\right)^2_{t_{si}} - \left(\epsilon_{SS}\epsilon_0\frac{d\phi}{dz}\right)^2_0$$
$$= -(2e\epsilon_{SS}\epsilon_0 N_a)\phi_{SiGe}\left[\phi_{SS}-\phi_{SiGe}+\phi_t\left(\frac{n_{iS}}{N_a}\right)^2\left(e^{\phi_{SS}/\phi_t}-e^{\phi_{SiGe}/\phi_t}\right)\right]. \tag{3.37}$$

As the flux density is continuous across the SS-SiGe interface we have,

$$\left(\epsilon_{SiGe}\epsilon_0\frac{d\phi}{dz}\right) = \left(\epsilon_{SS}\epsilon_0\frac{d\phi}{dz}\right) \tag{3.38}$$

From the Eqs. (3.34), (3.37) and (3.38) it is obtained,

$$\left(\epsilon_{SS}\epsilon_0\frac{d\phi}{dz}\right)_0^2 = (2e\epsilon_{SS}\epsilon_0 N_a)\left[\phi_{SS} - \phi_{SiGe}\left(1-\frac{\epsilon_{SiGe}}{\epsilon_{SS}}\right) + \phi_t\left(\frac{n_{iS}}{N_a}\right)^2\left(e^{\phi_{SS}/\phi_t} - e^{\phi_{SiGe}/\phi_t}\right)\right] \tag{3.39}$$

According to Gauss's law, $[\epsilon_{SS}\epsilon_0 d\psi/dz]_0$ is nothing but the total semiconductor charge Q_{Sem}. Hence,

$$Q_{Sem} = \sqrt{(2e\epsilon_{SS}\epsilon_0 N_a)\left[\phi_{SS} - \phi_{SiGe}\left(1-\frac{\epsilon_{SiGe}}{\epsilon_{SS}}\right) + \phi_t\left(\frac{n_{iS}}{N_a}\right)^2\left(e^{\phi_{SS}/\phi_t} - e^{\phi_{SiGe}/\phi_t}\right)\right]} \tag{3.40}$$

where ϕ_{SiGe} is given by Eq. (3.32) and ϕ_{SS} is given by,

$$\phi_{SS} = \frac{eN_a}{2\epsilon_{SS}\epsilon_0}\left[z_d^2 - z_{ds}^2\left(1-\frac{\epsilon_{SS}}{\epsilon_{SiGe}}\right)\right], \tag{3.41}$$

3.2.2 Determination of ϕ_{SS}, ϕ_{SiGe}

In this section the method of determining ϕ_{SiGe}, ϕ_{SS} from Eq, 3.40 for a particular N_{INV}, N_a, x and t_{Si} is provided. Depletion charge per unit area (Q_D) is given by,

$$Q_D = eN_a z_d. \tag{3.42}$$

Inversion charge per unit area (Q_I)can be given by,

$$Q_I = Q_{Sem} - Q_D. \tag{3.43}$$

For a given N_{INV}, a transcendental equation can be obtained,

$$\Delta = Q_I - eN_{INV}. \tag{3.44}$$

To find the solution for $\Delta = 0$, Eqs. (3.32), (3.41), (3.42) and (3.44) are simultaneously solved for z_d. Finally, using the value of z_d in Eqs. (3.32) and (3.41), ϕ_{SiGe} and ϕ_{SS} can be obtained.

Chapter 4

Modeling of Threshold Voltage

It is well known that, when MOS transistor gate length is scaled below submicron level, QM effects alter energy band structure such that subbands form, and the lowest subband is displaced upward (downward) in the electron (hole) inversion and accumulation layers. This has the effect of increasing the Si bandgap, and it results in a larger threshold voltage (V_{TH}) than that predicted by classical calculations which neglect these QM effects. Thus increase in doping though improves device turn-off characteristics, it adversely affects the V_{TH}.

In SS/SiGe devices, it has been observed that V_{TH} reduces with increasing Ge-mole fraction [22]-[25]. This has opened up an opportunity to circumvent the above stated problem. As a result, modeling of V_{TH} for SS/SiGe devices has become an important topic of interest. V_{TH} has three origins, namely, the SiO_2-semiconductor surface potential (ϕ_S), the oxide voltage (V_{OX}) and the flat-band voltage (V_{FB}). Reduction of V_{TH} means an overall reduction after these three components are combined. All three components are modulated by the changes in bandgaps, electron affinities and dielectric constants of SS and SiGe regions, density of states in SS region and band offsets between SS/SiGe interface, with the variation of Ge-mole fraction, x, in SiGe layer and the thickness of SS layer, t_{Si}.

Recent models of V_{TH} in SS/SiGe device (V_{TSS}) [23]-[25] have demonstrated the reduction of V_{TSS} in terms of all the components stated above except the contribution from a change in dielectric constant from ϵ_{SS} to ϵ_{SiGe} across the SS/SiGe interface. Though in [24] the change in permittivity has been included

through some kind of averaging while expressing V_{OX} for SS-nMOS devices, the effect is not clearly identified.

As a result, a more complete model for V_{TSS} has been developed in this work, through which different issues of V_{TSS} reduction phenomena have been explained in the following sections.

4.1 Theory of threshold voltage calculation

Once the self-consistent potential profile for any fixed inversion condition is obtained, gate voltage required to obtain the inversion condition can be calculated from the following equation,

$$V_{GS} = \phi_S + T_{OX}F_{OX} + V_{FB} \tag{4.1}$$

where ϕ_S is the total band bending or the Si surface potential and V_{FB} is the flat band voltage. Also T_{OX} and F_{OX} are oxide width and electric field in the oxide respectively.

Conventionally, V_{TH} is the gate voltage where the volume inversion carrier density at the channel surface is equal to the bulk doping density. However, this semiclassical definition is not suitable in deeply scaled devices due to quantum mechanical effect and non-linearity of scaling. Due to quantization effect, the inversion carrier density at the oxide-Si interface is always vanishingly small and the peak carrier concentration in the inversion layer is displaced from the gate dielectric-semiconductor surface. This creates an inversion capacitance (C_{INV}) in series with the oxide capacitance (C_{OX}). Since, V_{GS} is now shared by both of these capacitances, the amount of band bending under the influence of C_{INV} is larger than without any consideration of C_{INV} and, thus, a higher value of V_{GS} is required to induce the same amount of inversion charge density. This in turn, increases V_{TH} over the semiclassically predicted value.

Our model has considered a new definition of V_{TH} for SS/SiGe MOS devices which is based on the definition of equal current drive. This definition proposed by Takagi *et al.* [44] applied in both quantum mechanical and semiclassical analysis.

According to this definition, V_{TH} is the gate voltage necessary to induce an N_{INV} equal to 10^{11} cm^{-2} in the channel.

4.2 Results and discussions

4.2.1 Quantum mechanical analysis

In this section the simulation results based on our quantum mechanical analysis for both SS-nMOS and SS-pMOS devices have been discussed. As said earlier reduction in V_{TH} has three origins, these are explained below.

An energy band diagram at threshold for SS-nMOS and -pMOS device each for $x = 0.25$ has been shown in Fig. 4.1 that explains the effect of neglecting ϵ_{SiGe} in ϕ_{SS} while calculating V_{TSS}. Fig. 4.1(a) and (b) is for nMOS and pMOS, respectively. Curve (i) represents SS/SiGe system with different dielectric constants for SS and SiGe regions, curve (ii) is also for the SS/SiGe system, but with the dielectric constants of both SS and SiGe regions assumed to be equal to ϵ_{SS} and curve (iii) is for the control-Si device. From the difference between curve (i) and (ii) it can be seen that, ϕ_{SS} is overestimated by neglecting the effect of ϵ_{SiGe}.

Reduction in $\phi_{SSn(p)}$ can be explained in terms of the shift in conduction and valence band edges of SS layer, band offsets in SS/SiGe interface and higher value of ϵ_{SiGe}. Apart from an increase in intrinsic carrier concentration (n_{iSS}) due to the reduction in band gap with increase in x of SS region, reduction in ϕ_{SS} has another reason particularly for SS-nMOS device. For an SS-nMOS device, strain splits the Δ_4 and Δ_2 conduction band valleys and makes Δ_2 lower in energy level. As a result, the SiO_2-SS-SiGe quantum well becomes steeper than the unstrained bulk-Si quantum well for the same doping density. Therefore, less ϕ_{SS} is now required for the same inversion carriers to be confined within the well. For an SS-pMOS device, though SS/SiGe band offset cause parasitic charges to be stored at SS/SiGe interface which are supposed to increase ϕ_{SSp} required for inversion, ϕ_{SSp} reduces due to a reduction in density of states caused by an increase in n_{iSS} that subsides the effect of parasitic charges.

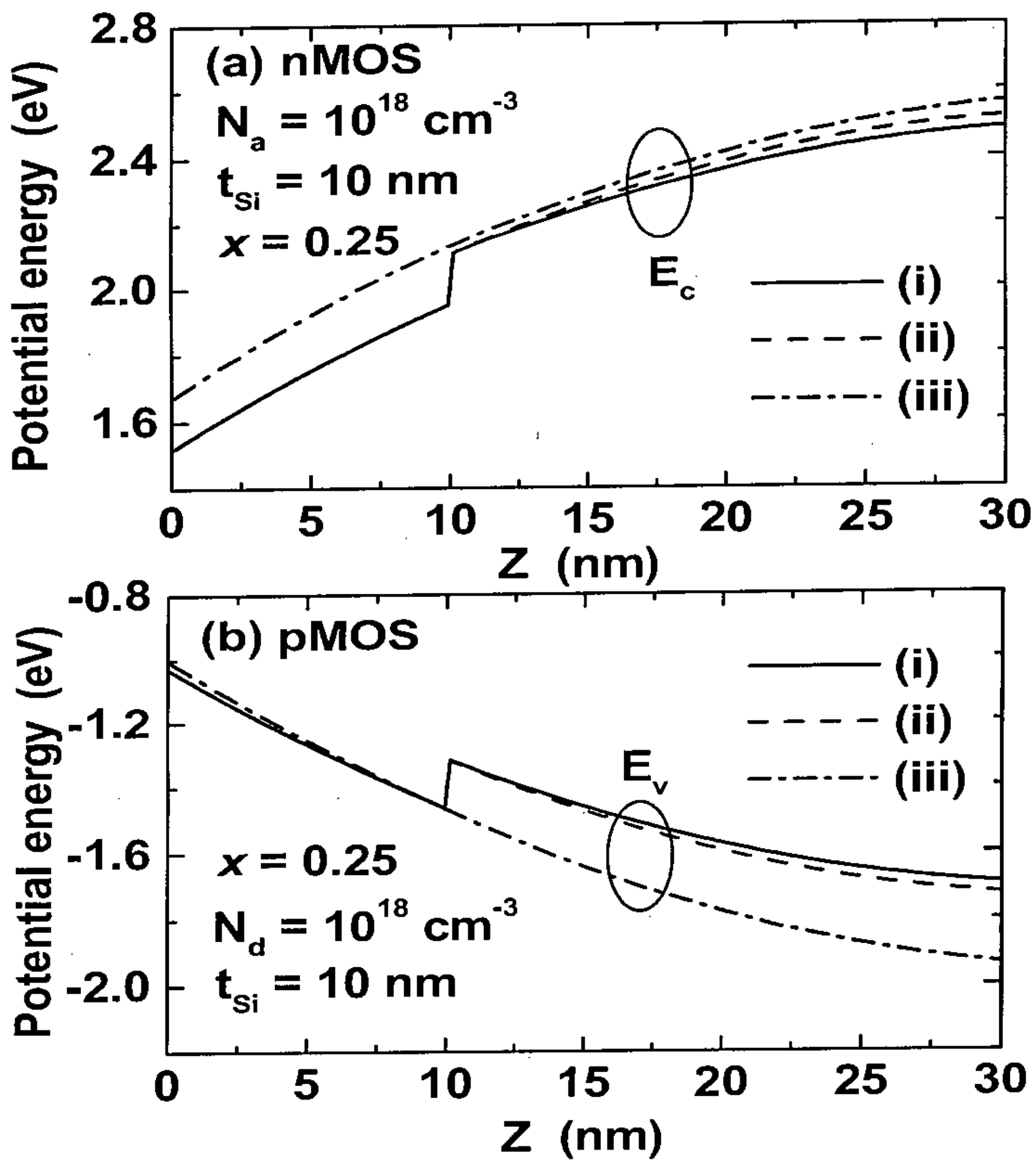


Figure 4.1: Energy band diagrams at threshold for SS-nMOS (a), and -pMOS (b) structures showing the effect of neglecting ϵ_{SiGe}. Curve (i) represents SS/SiGe system with different dielectric constants for Si and Ge regions, curve (ii) is for a SS/SiGe system with the dielectric constants of both SS and SiGe regions equal to ϵ_{SS}, and curve (iii) is for the control-Si device.

To understand the contribution of ϵ_{SiGe} in ϕ_{SS} reduction, Fig. 4.1(a) and (b) have to be looked back and probed again. Here, the relative positions of the conduction and valence band profiles for SS and control-Si devices are the results of increased electron affinity and reduced bandgap of SS and conduction and valence band offsets at the SS/SiGe interface. The difference in surface potentials between curves (i) and (iii) represents total $\Delta\phi_{SS}$ and this includes all different contributions. To identify the contribution in $\Delta\phi_{SS}$ arising from the difference in ϵ_{SS} and ϵ_{SiGe}, curves (i) and (ii) are compared. The difference in surface potential between these two curves ($\Delta\phi_{SS}(\epsilon)$) is due to only the change in the dielectric constant at SS/SiGe interface. Fig. 4.1 shows that the magnitude of ϕ_{SS} is smaller for curve (i) for both SS n- and p-MOSFETs. It is due to the fact that for the same depletion charge distribution, Electric field is lower in SiGe region (as $\epsilon_{SiGe} > \epsilon_{Si}$) in SS device compared to the electric field at the same depth in Si in the control-Si device. Consequently, there is a smaller potential drop across the SiGe region in the SS structure.

$\Delta\phi_{SS}(\epsilon)$ is shown in Fig. 4.2 as a function of x. Fig. 4.2 (a) is for nMOS and 4.2(b) is for pMOS device. $|\Delta\phi_{SS}(\epsilon)|$ is reduced by strain for both type of devices. The reduction is aggravated for smaller t_{Si} and lower substrate doping density $N_a(N_d)$. In [25] it is claimed that the silicon surface electric field should remain the same at threshold for both the control-Si and SS devices using a threshold voltage definition similar to that of [44]. For $t_{SS} < z_d$, this implies that z_d should be same for both the devices. Our calculations show that actually z_d is smaller in the SS device by around 5% in spite of the expected increase caused by a higher value of ϵ_{SiGe}. Similar observation has also been reported in [23]. This reduction in z_d is caused by a combination of bandgap narrowing in SS as well as SiGe regions and band offset. This additional factor will further reduce V_{TSS} in the SS device by reducing V_{OX} by a similar ratio.

Another important factor in V_{TSS} reduction is the reduction in V_{FB}. V_{FB} is the difference between the work function of gate material and semiconductor region. Though there are several expressions recently proposed in [24, 32], they

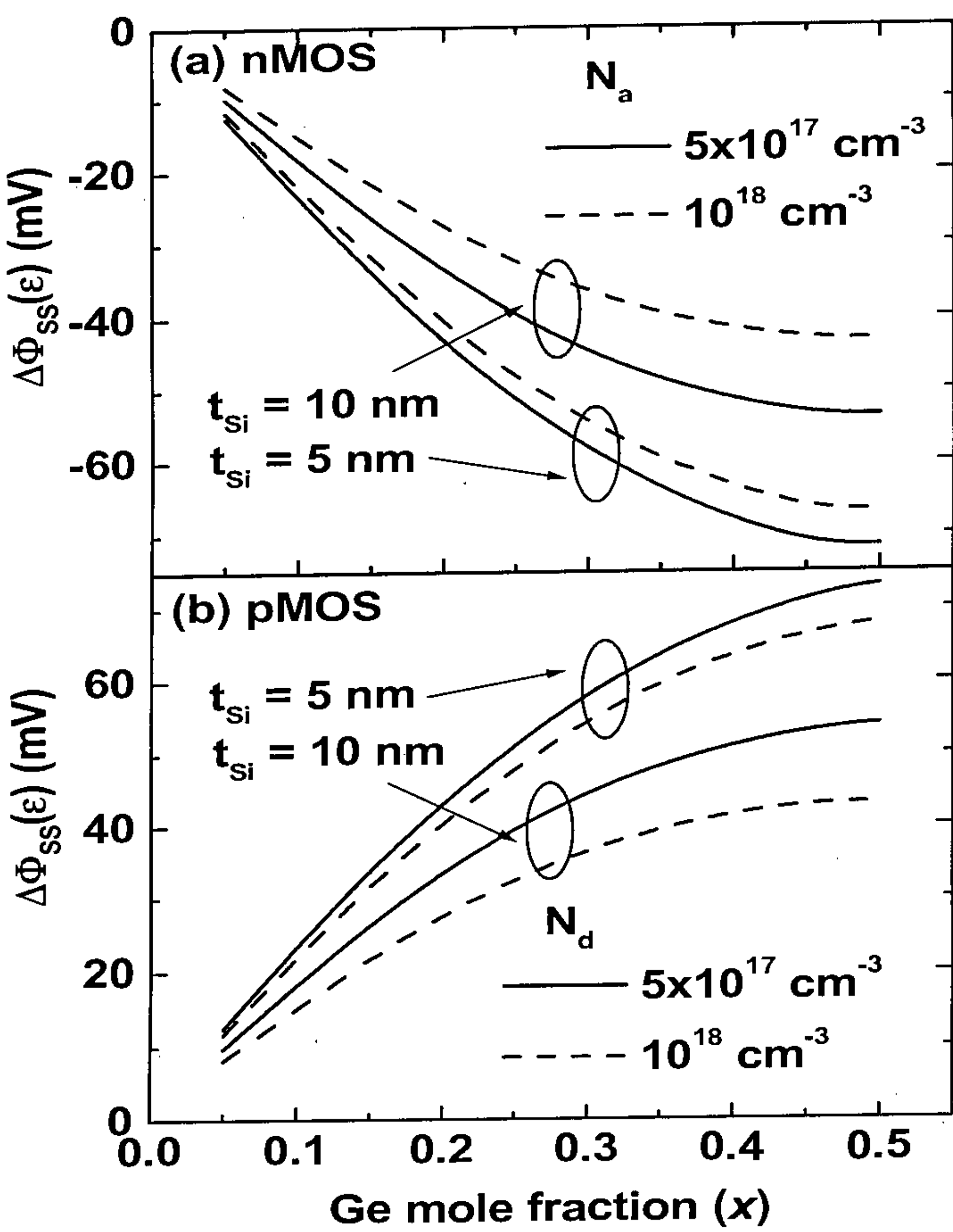


Figure 4.2: The contribution of the dielectric constant difference between SiGe and SS regions to the SS surface potential change in (a) SS-nMOS and (b)-pMOS structures.

are actually modification of the V_{FB} expression found in [46],

$$V_{FB} = \phi_M - (\chi_{SS} + \frac{E_{gSS}}{2e} \pm \phi_F). \quad (4.2)$$

Here, ϕ_M is the metal work function. χ_{SS}, E_{gSS} are the electron affinity, bandgap of SS layer and ϕ_F is the Fermi potential. '+' sign is for n and '-' is for p MOS devices. This simple expression is used in [25] and also in our model. In our simulation, Al gate of work function 4.1 eV has been considered and the reduction in V_{FB} is due to the decrease in bandgap and electron affinity of SS layer with increase in x.

In Fig. 4.3, changes in the components of V_{TH} are presented. It has been found that for both type of SS devices, V_{TH} shift is significant. The threshold voltage shift in SS n and p MOSFETs is defined as,

$$\Delta V_{TSSn(p)} = V_{TSSn(p)} - V_{TUSn(p)} \quad (4.3)$$

ΔV_{OX}, $\Delta\phi_{SS}$ and ΔV_{FB} are given by,

$$\begin{aligned} \Delta V_{OXn(p)} &= V_{OXSSn(p)} - V_{OXUSn(p)} \quad (4.4) \\ \Delta\phi_{SSn(p)} &= \phi_{SSn(p)} - \phi_{USn(p)} \\ \Delta V_{FB} &= V_{FBSSn(p)} - V_{FBUSn(p)} \end{aligned}$$

where V_{OXSS} and V_{OXUS} are the oxide voltages for strained and unstrained devices, respectively. Similar definitions are applicable to ϕ_{SS} and V_{FB} as well. Also, in all cases $x = 0$ corresponds to unstrained bulk-Si device. From Fig. 4.3(a) it is seen that, for nMOS device $\Delta\phi_{SSn}$ is the dominant term. But in Fig. 4.3(b) it can be seen that, $\Delta\phi_{SSp}$ has an opposite polarity to ΔV_{FB}. ΔV_{OX} is small for both cases.

$\Delta V_{TSSn(p)}$, calculated with and without considering variation of ϵ across SS/SiGe interface is demonstrated in Fig. 4.4. In both the Fig. 4.4 (a) and (b), $\epsilon_{SS} - \epsilon_{SS(SiGe)}$ indicates the value of dielectric constant in SS and SiGe regions, respectively. For SS-nMOS device as $V_{TSSn} > 0$, $\Delta V_{TSSn} < 0$ indicates a reduction in V_{TSSn}. V_{TSS} continues to reduce with increase in x. The reduction is mainly due to the reduction in ϕ_{SSn} as found from Fig. 4.3(a). In Fig. 4.4(b), $|\Delta V_{TSSp}|$ is

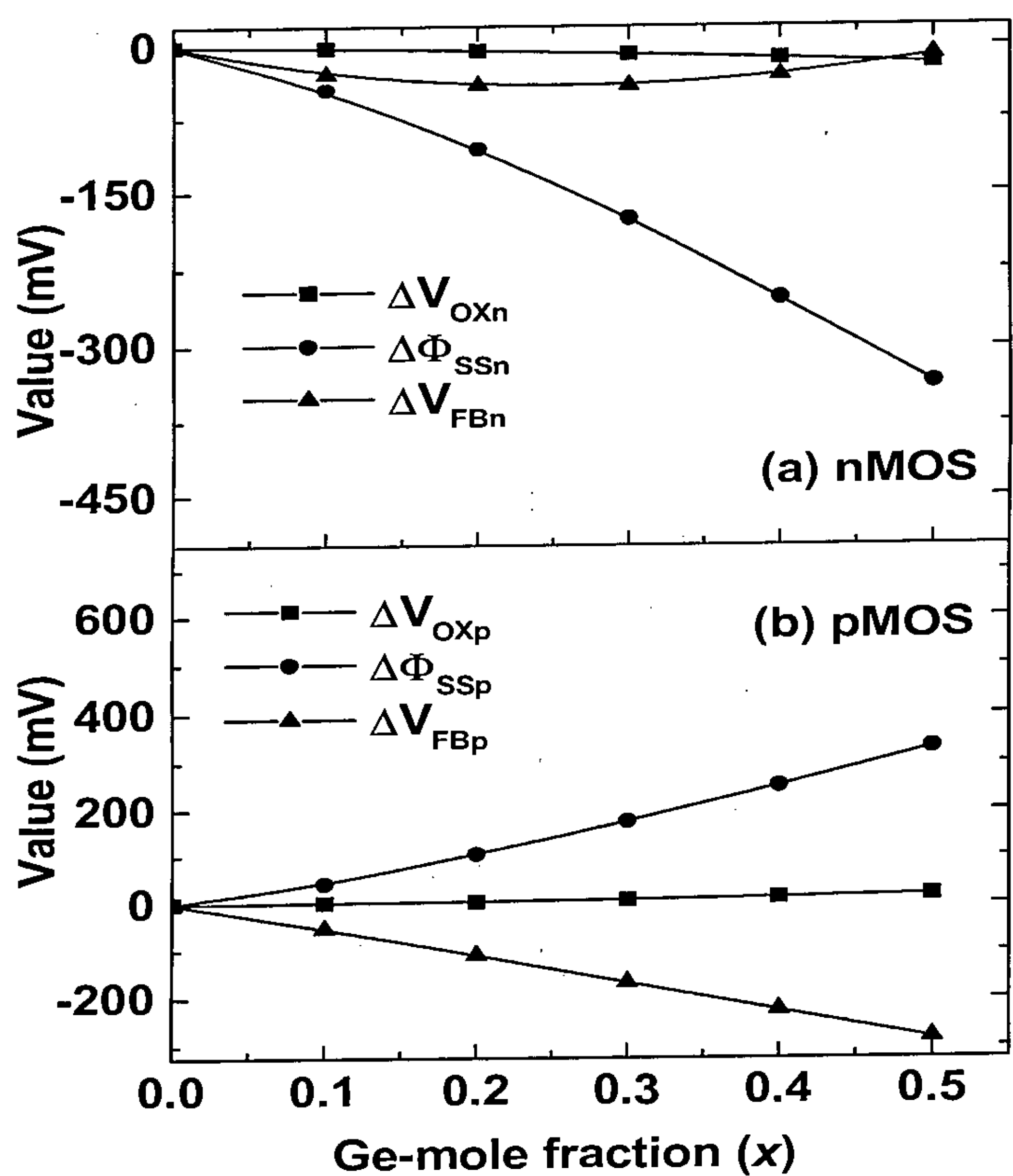


Figure 4.3: Various components of changes in V_{TH} (ΔV_{TSS}) in SS-nMOS (a) and -pMOS (b) devices with increasing x.

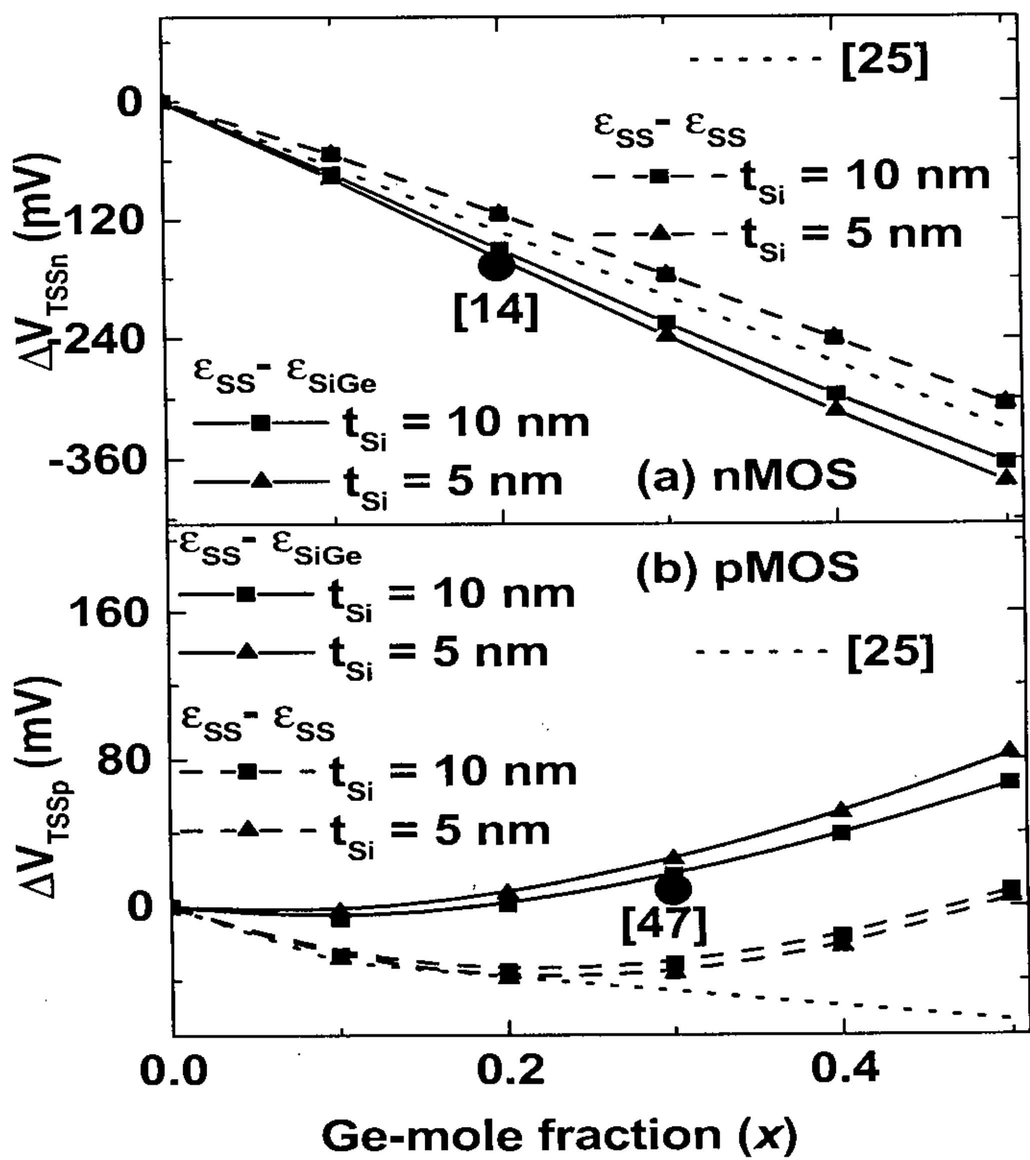


Figure 4.4: Reduction in threshold for SS-nMOS (a), and -pMOS (b) structures showing the effect of neglecting ϵ_{SiGe} for a doping density of 5×10^{17} cm^{-3}. Dotted lines are calculated values obtained from [25] and solid circles are experimental values reported in [14] and [47] for SS-n and -pMOSFETs, respectively.

underestimated when ϵ_{SiGe} is neglected. The main reason is the overestimation of ϕ_{SSn} as mentioned above.

In case of pMOS, the situation is more interesting. Here, it should be mentioned that $V_{TSSp} < 0$ and so, $\Delta V_{TSSp} > 0$ means a decrease in V_{TSSp}. Also it is clear from Fig. 4.3(b), that, ΔV_{TSSp} is determined by the competing effect of ΔV_{FBp} and $\Delta \phi_{SSp}$. ΔV_{TSSp} can become negative upto a certain x. This indicates an increase in $|V_{TSSp}|$ in SS-pMOS device. When, ϵ_{SiGe} not considered, a higher value of ϕ_{SSp} is assumed in $\epsilon_{SS} - \epsilon_{SS}$ case. So, $|\Delta \phi_{SSp}|$ becomes smaller and, thus, let the decreasing ΔV_{FBp} to dominate over increasing $\Delta \phi_{SSp}$ (Fig. 4.3) and cause ΔV_{TSSp} to become negative. For higher x when $|\Delta \phi_{SSp}|$ exceeds $|\Delta V_{FBp}|$, $|\Delta V_{TSSp}|$ again shows an increasing trend. On the other hand, when ϵ_{SiGe} is considered, $\Delta \phi_{SSp}$ cannot exceed ΔV_{FBp} and hence $|\Delta V_{TSSp}|$ always increases.

Zhang *et al.* [25] could not explicitly clarify the mismatch between their calculated value and experimentally obtained $\Delta V_{TSSn(p)}$ data from [14, 47]. Both their calculation and experimental values are also shown in Fig. 4.4. Model-predicted $|\Delta V_{TSS}|$ underestimates the measured data for both SS-nMOS and pMOS devices as can be seen from Fig. 4.4. Also, in SS-pMOS devices, $|V_{TSSp}|$ rather increases with x whereas the experimentally measured data suggests a decreasing trend. They also predicted that, the reasons for these apparent discrepancies are the uncertainties in the bandstructure parameters they have used and the overestimation of density-of-states in the strained devices.

We observe that the agreement between our calculated $|\Delta V_{TSS}|$ and experimental $|\Delta V_{TSS}|$ is excellent. Based on this, we suggest another possible reason to explain the observed mismatches, which is the overestimation of ϕ_{SS} owing to the negligence of ϵ_{SiGe}. Such a correction for SS-nMOS device can narrow the difference between their theoretically predicted and experimentally obtained data. This can be understood from Fig. 4.4(a). Moreover, in SS-pMOS device, the opposite trend between the measured and simulated data can also be explained upto $x = 0.25$ by making such correction. This is verified from Fig. 4.4(b) where we showed that, negligence of ϵ_{SiGe} can make $|V_{TSSp}|$ to increase.

4.2.2 Semiclassical analysis

This section discusses the results obtained through the semiclassical analysis described in Chapter 2. Fig. 4.5 shows z_d, ϕ_{SS} and Q_S for a SS-nMOS device. In Fig. 4.5(a) variation of z_d with increasing x is shown. For a particular N_a, increase in x results in decrease in z_d. This reduction is primarily due to an increase of n_{iSS} for reduction in bandgap of SS layer with increasing x. The decrease of ϕ_{SS} is due to the decrease in ϕ_{SiGe} owing to a larger value of ϵ_{SiGe} relative to ϵ_{SS}. Reduction of z_d also contributes to the reduction of ϕ_{SS} as seen in Fig. 4.5(b).

The effect of doping density on ϕ_{SS} can be seen from Fig. 4.5(b). At higher N_a the effect of strain is somewhat enhanced as seen from Fig. 4.5(a) and (b). For the same x, at higher N_a, ϕ_{SS} decreases slightly more from the unstrained case than at lower N_a. In this case, z_d is reduced and hence Q_S is more confined within the SS-region. As a result, ϕ_{SiGe} becomes smaller and the effect of SiGe layer is less prominent on ϕ_{SS} reduction, as estimated from Eq. (3.32).

Fig. 4.5(c) shows the reduction in Q_S with increasing x. This reduction is also the effect of shallower z_d as expected from Eq. (3.40). The reduction of Q_S causes a reduction of V_{OX} as dictated by Gauss's law. Also reduced Q_S entail smaller gate voltage required to induce the same inversion charge density. According to Takagi's definition of V_{TH}, this in turn reduces V_{TSS} further.

The effect of considering different dielectric constants for SS and SiGe layers on ϕ_{SSn} and V_{OXSSn} is shown in Fig. 4.6(a). It is seen from the figure that the effect of $\Delta\epsilon$ on $\Delta\phi_{SSn}$ is more pronounced than on ΔV_{OXn}. If ϵ_{SS} is considered for both SS and SiGe layers, both ϕ_{SSn} and V_{OXSSn} are overestimated.

Fig. 4.6(b) shows $\Delta\phi_{SSn}$ and ΔV_{OXn} for different t_{Si} for a particular N_a with increasing x. In Fig. 4.6(b) we see that a thinner t_{Si} causes greater reduction of ϕ_{SSn} from that of the unstrained bulk-Si device. Both $\Delta\phi_{SSn}$ and ΔV_{OXn} show larger deviation from the unstrained case for thinner t_{Si}. Probing into both Eqs. (3.41) and (3.32), the reasons for this trend can easily be inferred. For thinner t_{Si}, ϕ_{SiGe} increases further, causing its contribution towards the total

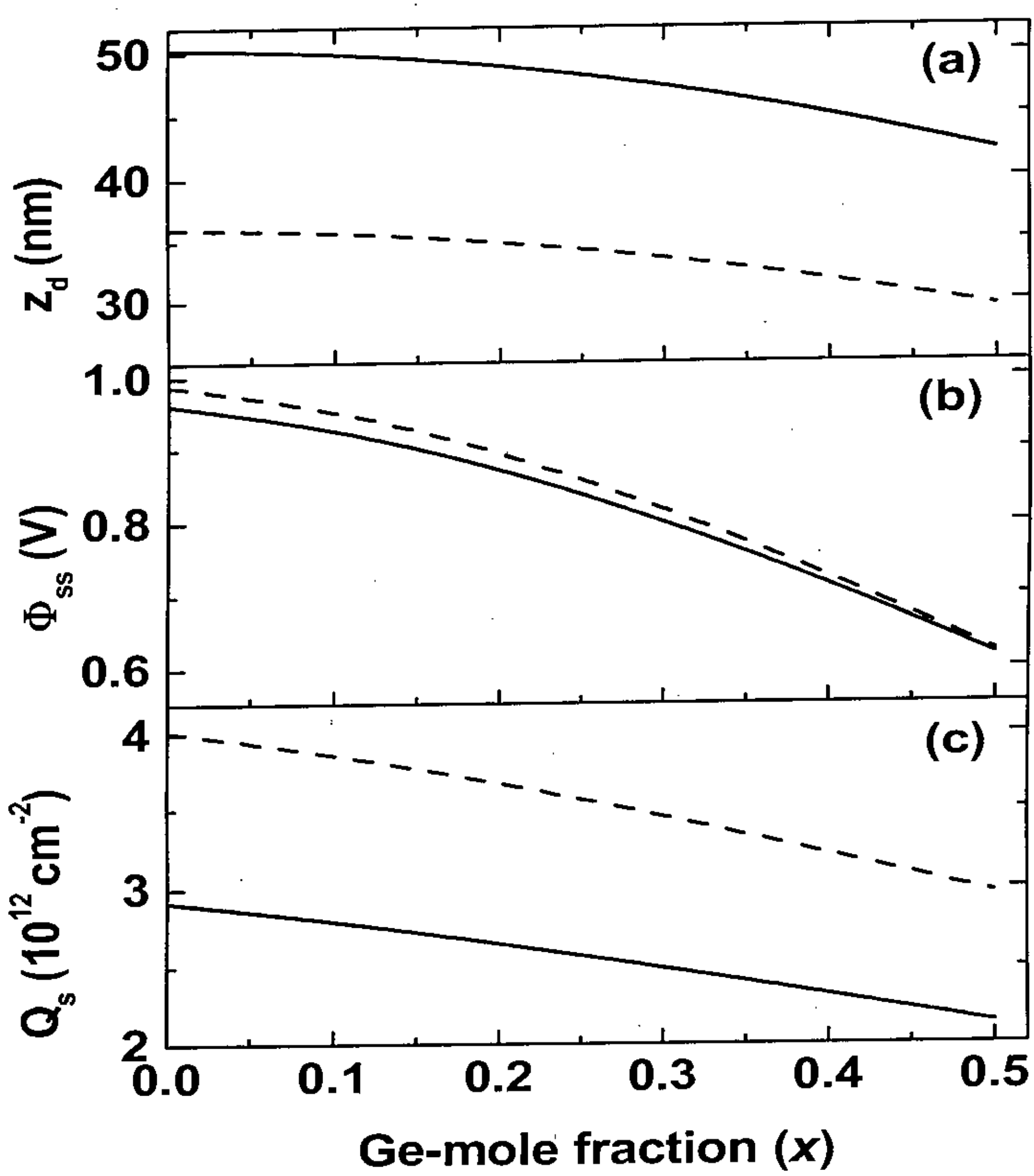


Figure 4.5: Variation of (a) z_d (b) ϕ_{SS} and (c) Q_S with increasing x for doping densities 5×10^{17} cm^{-3} (solid lines) and 10^{18} cm^{-3} (dashed lines). Here $N_{INV} = 10^{11}$ cm^{-2}.

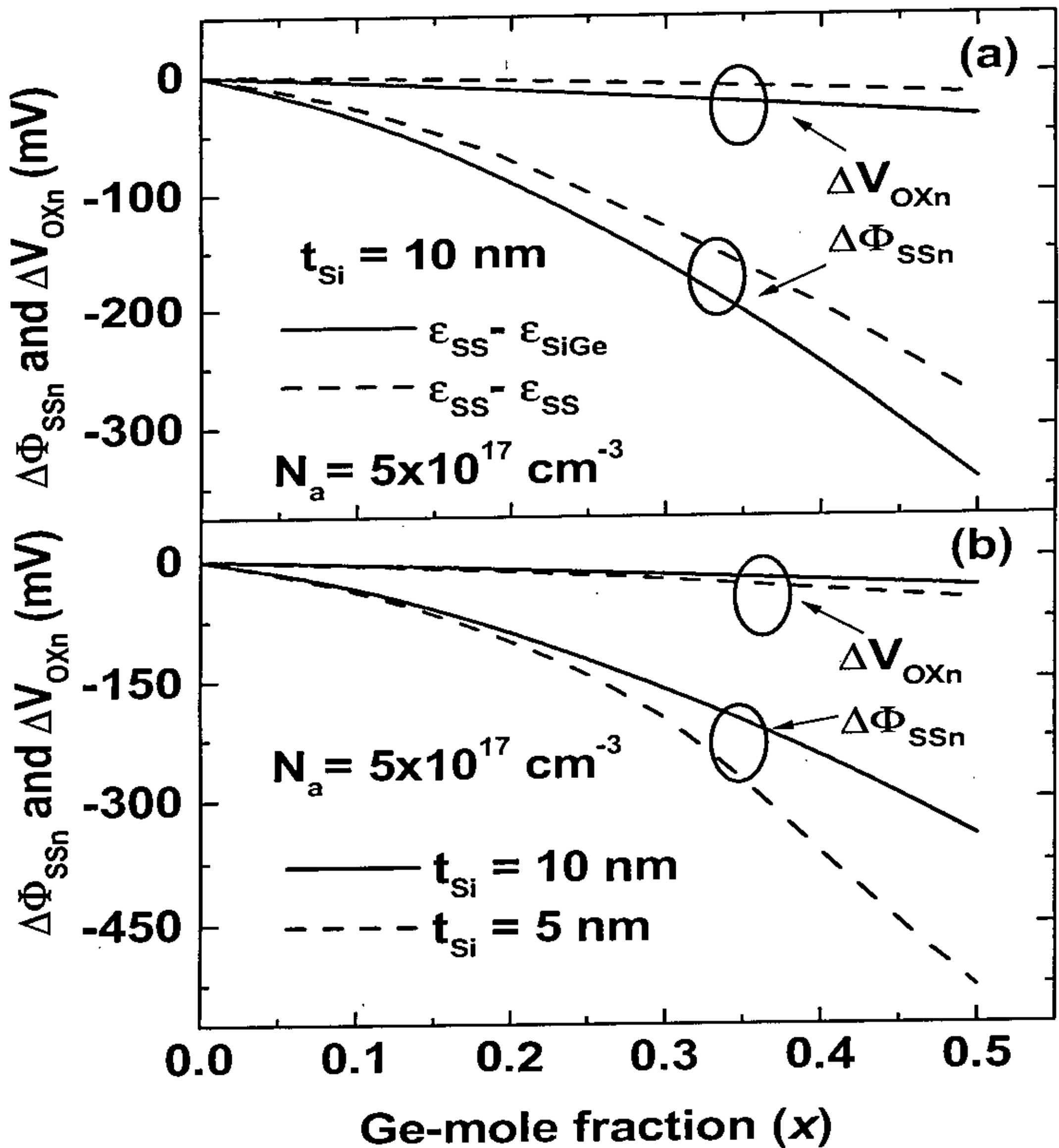


Figure 4.6: Influence of (a) different ϵ_{SiGe}, (b) thinner t_{Si} on $\Delta\phi_{SSn}$ and ΔV_{OXn} with increase in x, at N_a = 5x10^{17} cm^{-3}, N_{INV} = 10^{11} cm^{-2}.

both Eqs. (3.41) and (3.32), the reasons for this trend can easily be inferred. For thinner t_{Si}, ϕ_{SiGe} increases further, causing its contribution towards the total surface potential to increase. This implies that SiGe layer contains more regions of depletion area for a particular N_a and x conditions. But due to higher dielectric constant of SiGe, it results in smaller band bending in comparison to similar conditions under a thicker SS layer. So both $\Delta\phi_{SSn}$ and ΔV_{OXn} are further exaggerated in thinner SS layer with increasing x. Results in Fig. 4.6 show that the reduction in ϕ_{SS} and V_{OX} with increasing x predicted by semiclassical analysis can also explain the additional reduction of V_{TH} in SS device beyond the value predicted by conventional analysis [25].

4.2.3 Comparison between semiclassical and quantum mechanical analysis

As V_{TSS} has been modeled with two different techniques, a comparison between the two results will further clarify the physical behaviors of V_{TSS} under different conditions.

Fig. 4.7(a), (b) and (c) show, $\Delta\phi_{SSn}$ for three different SS thicknesses for an SS-nMOS device calculated with both semiclassical (SC) and quantum mechanical (QM) procedures. It is clear from Fig. 4.7(a), (b) and (c) that, the agreement between the two models improve with increasing t_{Si} at smaller x. For $t_{Si} = 15$ nm, the two models agree over the entire range of x considered. On the other hand, for $t_{Si} = 5$ nm, the difference is not negligible for $x > 0.25$.

In all cases of Fig. 4.7, $|\Delta\phi_{SS}|_{SC} > |\Delta\phi_{SS}|_{QM}$. This could be attributed to the negligence of conduction band offsets between SS and SiGe layer (ΔE_c) the semiclassical model. In QM analysis, the conduction band of the SS region becomes lower in energy from the conduction band edge of SiGe. This reduces the width of the well and also comparatively reduces the effect of ϵ_{SiGe} on $|\phi_{SS}|$ reduction. So $|\Delta\phi_{SS}|_{QM}$ is always smaller for a fixed t_{Si}, N_a and x.

Semiclassically, from Eq. (3.41), it can be understood that, thicker t_{Si} causes lesser reduction in ϕ_{SSn} compared to thinner t_{Si} under same x. The situation is

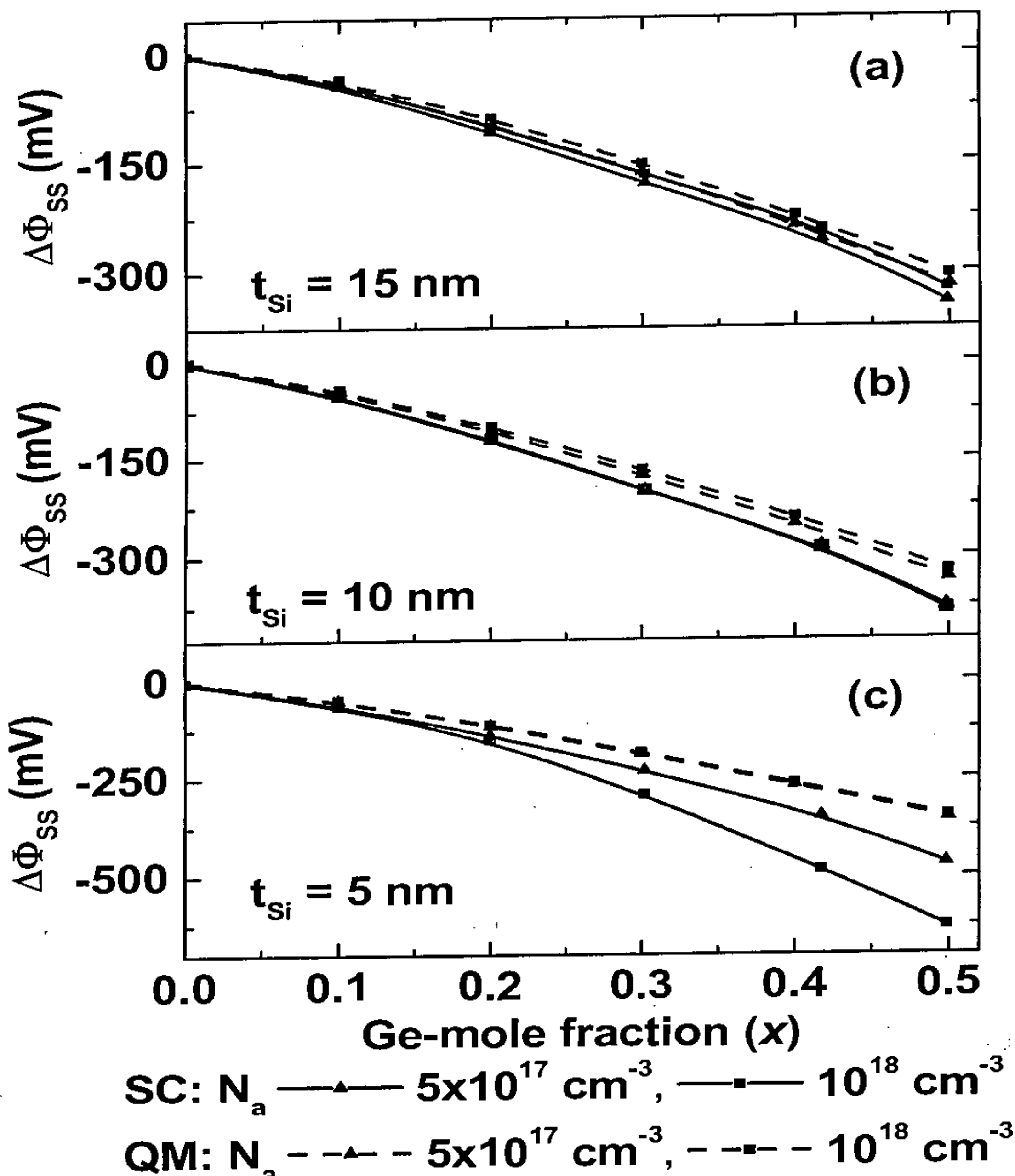


Figure 4.7: Comparison between semiclassically and quantum mechanically calculated $\Delta\phi_{SS}$ for SS/SiGe nMOS device.

similar in QM analysis.

An anomalous situation is observed in $\Delta\phi_{SS}$ shown in Fig. 4.7(b) and (c) as far as doping density is concerned. It is seen that, higher N_a shows smaller $\Delta\phi_{SS}$ compared to similar conditions at lower N_a, in QM analysis whereas the trend is found opposite in SC analysis. A plausible explanation has been provided below.

$|\Delta\phi_{SS}|$ increases with increasing n_{iSS}, ϵ_{SiGe}, ΔE_c and decreases with increasing t_{Si} . When ΔE_c increases, to induce same inversion charge, ϕ_{SS} decreases. It is already mentioned that QM analysis incorporate the effect of band offset in determining ϕ_{SS}. But at higher N_a, effect of ΔE_c does not suppress the difference in inversion charge induced band bending between strained and unstrained condition. Also, z_d is reduced. So $\Delta\phi_{SS}$ is less affected by both ΔE_c and ϵ_{SiGe} for a fixed t_{Si}. So at higher N_a, $|\Delta\phi_{SS}|$ is reduced in QM analysis.

In our SC analysis, $\Delta\phi_{SS}$ depends on n_{iSS}, ϵ_{SiGe} and t_{Si}. At higher N_a, z_d reduces. So, z_{ds}^2 in Eq. (3.41) is suppressed for a thicker t_{Si}. So, $|\Delta\phi_{SS}|$ follows QM result for thicker t_{Si}. But in case of sufficiently thinner t_{Si}, z_{ds}^2 severely reduces ϕ_{SS} and hence increases $|\Delta\phi_{SS}|$ for higher N_a.

A plot of ΔV_{TSSn} is provided finally to demonstrate the comparison of semiclassical and QM analysis on V_{TSSn} modeling in Fig. 4.8. Here, ΔV_{TSSn} follows similar trends as $\Delta\phi_{SSn}$ in Fig. 4.7 because from Fig. 4.3(a) it has been clarified that $\Delta\phi_{SSn}$ dictates ΔV_{TSSn}. Our semiclassical results are consistent with the results reported by Nayfeh *et al.* [24] such that $|\Delta V_{TSSn}|$ increases for higher N_a for a fixed t_{Si}. If it is assumed that, the two models agree when the difference in $(|\Delta\phi_{SS}|_{QM} - |\Delta\phi_{SS}|_{SC})$ falls below 10mV, then from the figure it can be inferred that, semiclassical analysis will give fairly accurate results for $x \leq 0.2$ when $t_{Si} \geq 10$ nm. This limit is important from the device analysis point of view as modeling experimental data is much easier through semiclassical techniques. Outside the range, the two methods differ significantly and QM analysis would be necessary.

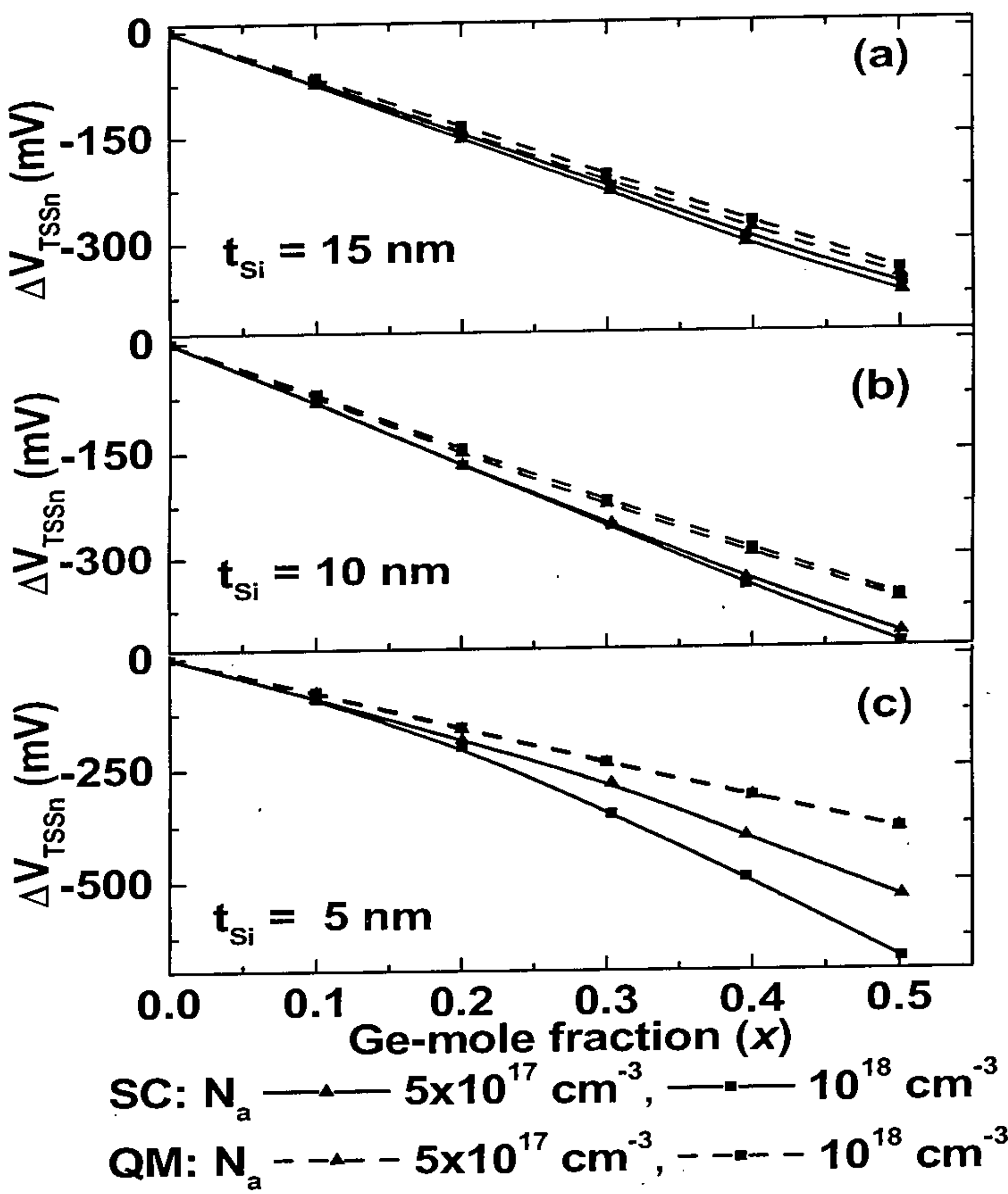


Figure 4.8: Comparison between semiclassical and quantum mechanical threshold voltage modeling for SS/SiGe nMOS device under different t_{Si} and N_a.

Chapter 5

Modeling of Gate Capacitance

Gate capcitances of strained-Si MOS devices is calculated in this chapter and compared with that of bulk-Si devices. Effects on capacitance in the context of thickness of strained layer, amount of Ge-mole fraction, dielectric constants of both SS and SiGe regions and substrate doping concentration considering wave function penetration effect are investigated.

5.1 Theory of gate capacitance calculation

MOS capacitor under inversion condition is represented by a series combination of oxide capacitance per unit area, C_{OX}, and the inversion layer capacitance per unit area, C_{INV}. Inversion layer capacitance has a significant influence on the performance of scaled MOSFET's with thin gate oxides. This is because the total gate capacitance, which determines the transconductance of MOSFET's is reduced by inversion layer capacitance [46]. C_{INV} is defined by,

$$C_{INV} = \frac{e\partial N_{INV}}{\partial \phi_S} \tag{5.1}$$

where N_{INV} is the surface carrier concentration and ϕ_S is the surface potential. The total gate capacitance per unit area, C_g, is defined by,

$$C_g = C_{OX}\frac{1}{1+\frac{C_{OX}}{C_{INV}}} \tag{5.2}$$

From Eq. (5.1), larger value of C_{INV} is favorable to obtain higher C_g. C_{INV} has two origins. One origin is the finite band bending associated with an increase in N_{INV} due to the finite density of states in the bands and the other is finite inversion layer thickness. C_{INV} due to inversion layer thickness is determined

is dominant in weak inversion and second one in strong inversion. Z_{avg} is significantly modified in SS/SiGe devices. After the self-consistent loop terminates, C_{INV} can be easily determined from Eqs. (5.1). For gate capacitance calculation, we used the following fundamental relation instead of Eq. (5.2),

$$C_g = \frac{e\partial(N_{INV} + N_{dep})}{\partial V_{GS}} \tag{5.3}$$

5.2 Results and discussions for pMOS devices

Self-consistent calculations for SS-pMOS devices are presented in this section. All the results are calculated at room temperature. In all cases, we have considered Aluminium for gate electrode having work function of 4.1 eV and SiO_2 having a thickness (T_{OX}) of 1 nm for gate dielectric. Effective mass for SiO_2 has been chosen as $0.5m_0$. Band structure parameters has been taken from Tables 2.1-2.4.

Fig. 5.1 shows inversion carrier density (ρ_{INV}(z)) as a function of z calculated using open boundary conditions. N_{INV} is 10^{11} cm^{-2}. The dashed line in the figure represents the potential profile of the device. There are two humps visible in ρ_{INV}(z) curve. Similar shape of ρ_{INV} has been reported in [20, 21]. The first hump is common where the usual quantum mechanical effects are present. Unlike the classical case, ρ_{INV} peak shifts away from the gate oxide into the bulk [39]. But the second hump is characteristic to SS-pMOS devices. It can be seen from the potential profile that, there is another quantum well produced at the SS/SiGe interface due to type-II nature of the SS/SiGe heterojunctions [23]. As a result a significant amount of holes are confined in the second well and are known as parasitic holes. The effect of such parasitic holes has been demonstrated in Fig. 5.2(a). The parasitic charge becomes negligible for higher inversion as also reported in [20].

In Fig. 5.2(a), z_{avg} is shown with increasing N_{INV} for two different x keeping N_d and t_{Si} constant. It is seen that z_{avg} is greater in SS device compared to control-Si device and it increases with increasing x. As the total N_{INV} charge is now shared by two wells, inversion charge centroid is shifted more into the semi-

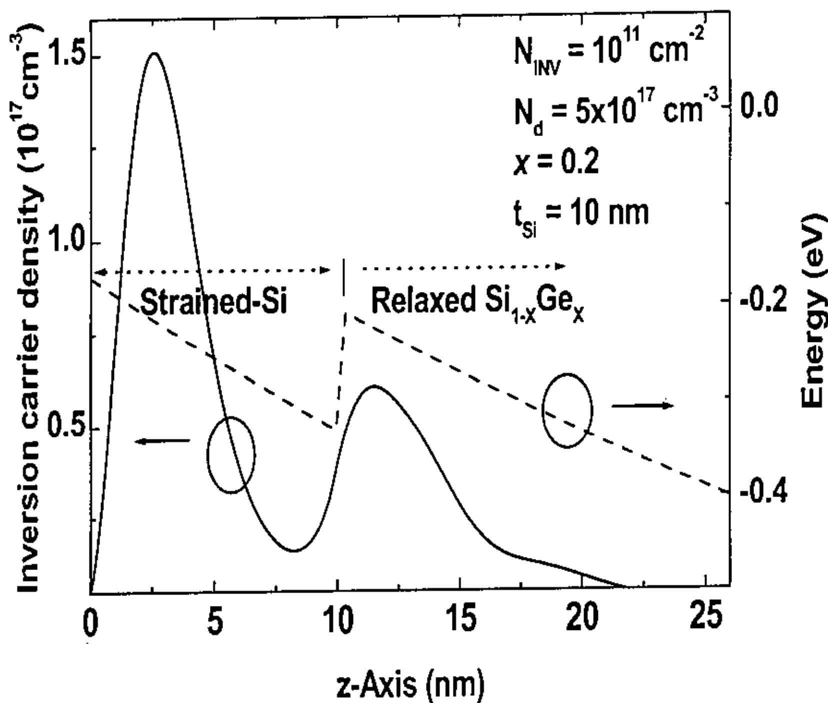


Figure 5.1: Inversion carrier density (solid line) as a function of z, in SS-pMOS device. The potential profile (dashed line) is for $N_d = 5 \times 10^{17}$ cm^{-3}, $N_{INV} = 10^{11}$ cm^{-2}, $x = 0.2$ and $t_{Si} = 10$ nm.

conductor region. At strong inversion the difference is reduced due to a strong SiO_2-SS electric field that makes the SiO_2-SS well much deeper than the parasitic one and hence z_{avg} is less affected by band offset. In Fig. 5.2(b), effect of strain on z_d has been shown. It is seen that, in SS-pMOS device z_d is lower than z_d in control-Si device and it decreases with increasing x. The reasons are already described in chapter 4 during the explanation of V_{TH} reduction in SS devices. The main reasons are increased n_{iSS} and higher dielectric constant of SiGe (ϵ_{SiGe}).

Expression for gate capacitances C_g can be rewritten as follows,

$$C_g = \frac{e\Delta N_t}{\Delta V_{GS}} \tag{5.4}$$

where $eN_t(= e(N_d z_d + N_{INV}))$ is the total semiconductor charge. For a fixed N_{INV},

$$e\Delta N_t = eN_d \Delta z_d \tag{5.5}$$

$$\text{also we know, } \Delta V_{GS} = \Delta V_{OX} + \Delta\phi_{dS} + \Delta\phi_{IN}$$

$$\text{and as } \Delta V_{OX} \text{ is negligible, } \Delta V_{GS} \approx \Delta\phi_{dS} + \Delta\phi_{IN} = \Delta\phi_S \tag{5.6}$$

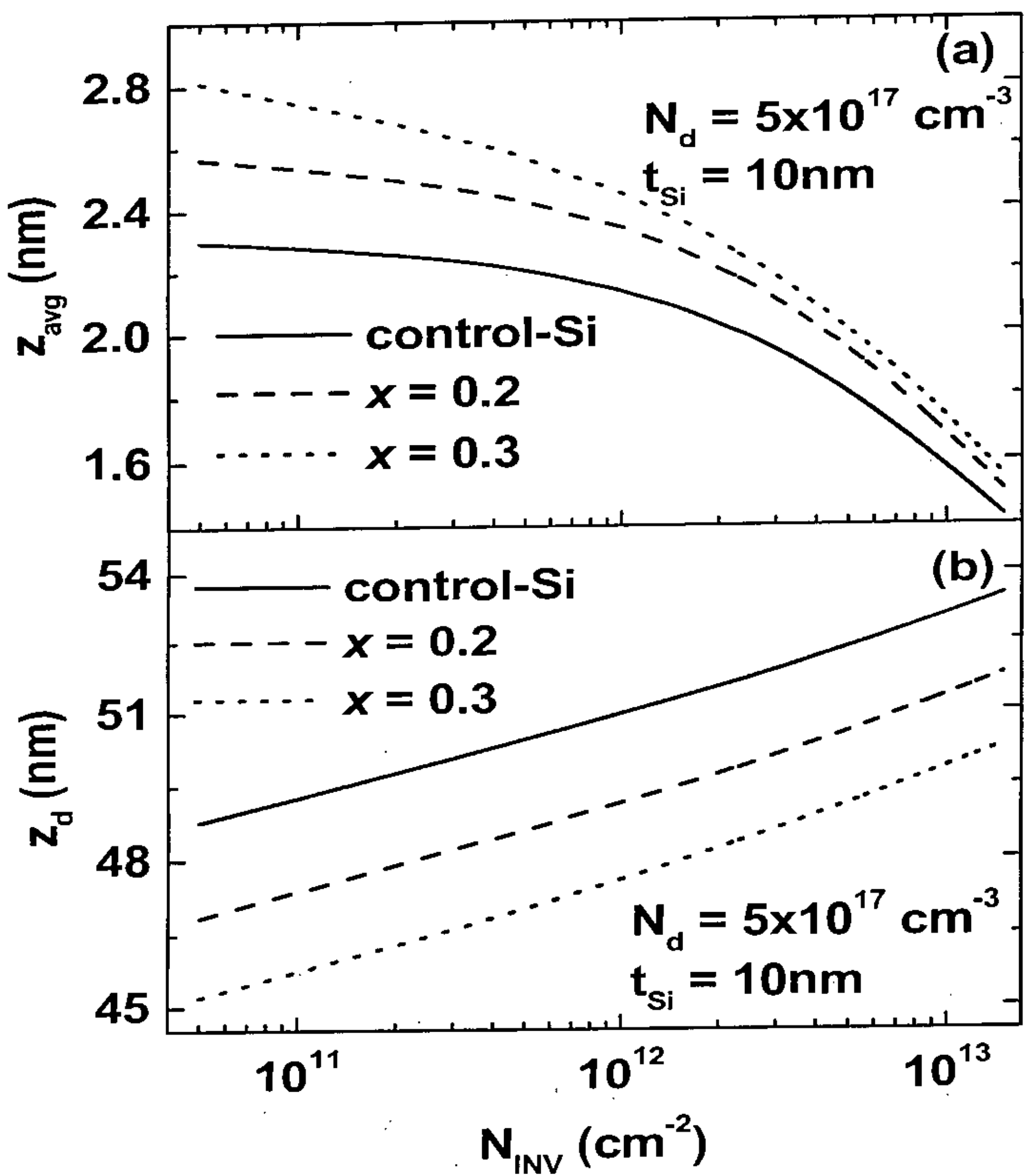


Figure 5.2: (a) average penetration of inversion charge (z_{avg}), (b) depletion depth (z_d) in SS-pMOS device with increasing x. Here, $N_d = 5 \times 10^{17}$ cm^{-3} and $t_{Si} =$ 10 nm.

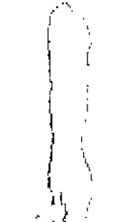
$$\text{also } \Delta\phi_{IN} = \frac{eN_{INV}\Delta z_{avg}}{\epsilon_{SS}} \tag{5.7}$$

Here, V_{OX} and ϕ_{IN} are oxide and inversion potential drop, respectively. ϕ_{dS} is the potential drop due to depletion charge and depends on z_d.

SiO_2-SS surface potential ϕ_{SS} and oxide electric field F_{OX}, are depicted in Fig. 5.3 and Fig. 5.4 under different inversion conditions. The effect of strain on both z_{avg} and z_d is reflected in Fig. 5.3(a) and (b). In Fig. 5.3(a), $|\phi_{SS}|$ decreases with increasing x. The difference is larger in lower inversion region than in the higher. At lower inversion, the effect of z_{avg} is less pronounced. Here, though z_{avg} is large, ϕ_{IN} is small due to lower value of N_{INV} (as can be seen from Eq. (5.7) if the differential operator is omitted). Hence, for the same inversion charge to induce, it requires lesser $|\phi_{SS}|$ compared to control-Si due to a larger decrease in z_d under strain. The decrease in z_d more than counters the effect of increase in $|\phi_{SS}|$ due to increase in z_{avg}. In moderate inversion level, $\Delta\phi_{IN}$ increases resulting in larger $\Delta\phi_S$. Finally, at strong inversion the rate of increase in $|\phi_{SS}|$ is sharper than that of control-Si. In high inversion, the effect of z_{avg} is strong. But since the difference in z_{avg} between SS and control-Si is rather small, decrease in z_d significantly reduces $|\phi_{SS}|$. In Fig. 5.3(b), though F_{OX} is reduced with strain, the reduction is very small and is therefore negligible under high inversion condition. Under low inversion condition, the change in F_{OX} is similar to the change in z_d.

Fig. 5.4(a) and (b) are arranged to show the effect of different t_{Si} on both ϕ_{SS} and F_{OX}. Here it can be found in Fig. 5.4(a) that, $|\phi_{SS}|$ decreases with decreasing t_{Si} under same x. In thinner t_{Si}, SiGe layer is closer to the surface than in the case of thicker one and the parasitic effect is pronounced. It causes an even larger z_{avg} for thinner t_{Si}. So at low inversion, in case of thinner t_{Si}, the effect of reduced z_d is compensated by the excessive increase in z_{avg} on $|\phi_{SS}|$ reduction. At strong inversion condition, the situation is reversed as again the effect of z_{avg} becomes less prominent due to small difference between z_{avg} of control-Si and SS devices. However from Fig. 5.4(b), it can be stated again that F_{OX} does not vary much with t_{Si}.

Using the concepts described above and with the help of Eq. (5.1), the inver-



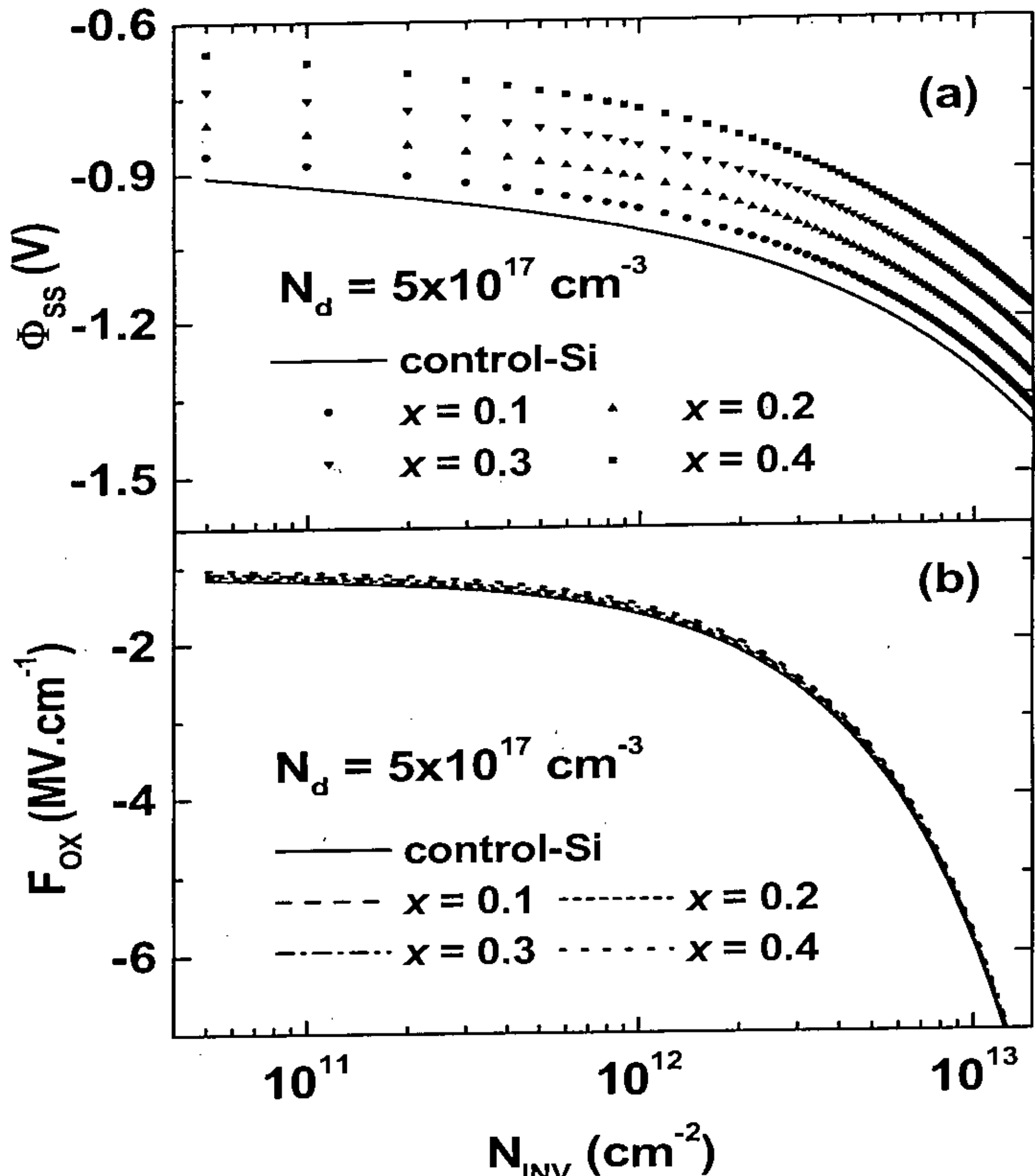


Figure 5.3: (a) SiO_2-SS surface potential ϕ_{SS}, and (b) oxide electric field F_{OX} for various x with increasing N_{INV} in SS-pMOS device where $N_d = 5 \times 10^{17}$ cm^{-3} and $t_{Si} = 10$ nm.

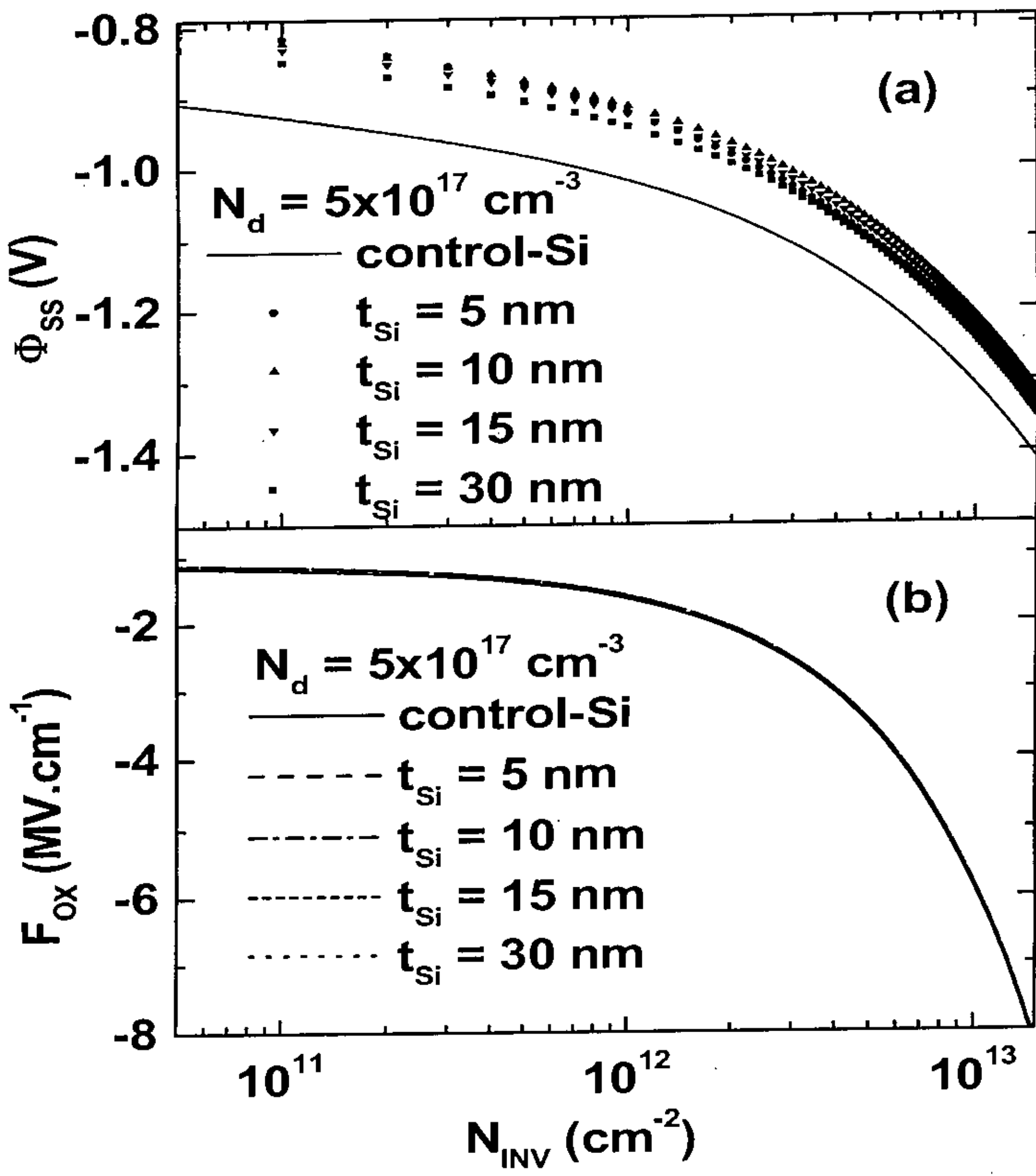


Figure 5.4: (a) SiO_2-SS surface potential ϕ_{SS}, and (b) oxide electric field F_{OX} for various t_{Si} in SS-pMOS device where $N_d = 5 \times 10^{17}$ cm^{-3} and $x = 0.2$.

sion capacitance of SS-pMOS (C_{ISS}) shown in Fig. 5.5 can now be explained. In Fig. 5.5(a), at low inversion, C_{ISS} increases with increasing x. At weak inversion, the change in ϕ_{SS} ($\Delta\phi_S$) is lower for higher x as discussed earlier. So, C_{INV} increases with increasing x at low inversion. At moderate inversion, C_{ISS} slightly decreases from that of control-Si. This is due the competing effect of z_{avg} and z_d in determining $\Delta\phi_S$. Here, larger $\Delta\phi_{IN}$ due to larger z_{avg} somewhat overcomes the smaller $\Delta\phi_{ds}$ and results in slightly larger $\Delta\phi_S$. At strong inversion, C_{ISS} becomes lower as a result of higher $|\Delta\phi_S|$ owing to higher rate of change in z_d and negligible effect of z_{avg} as explained before.

On the other hand, in Fig. 5.5(b), at lower and moderate inversion, thinner t_{Si} shows lower C_{ISS} even from the control-Si one. This is due to large $|\Delta\phi_S|$ originating from a large change in Δz_{avg}. At higher inversion when the effect of z_{avg} is minimized, the curves again overlap each other.

The effects of strain on the gate capacitance (C_g) are going to be discussed in detail in the following paragraphs. We have found that in SS devices $|V_{TSS}|$ decreases with the increase in strain, this effect can also be viewed in gate capacitance (C_g)-voltage (V_{GS}) curve shown in Fig. 5.6. Here it can be seen that, as the amount of strain is increased by increasing x, $|V_{TSS}|$ is reduced and C-V curves shift to the right accordingly. Moreover, in addition to V_{TSS} shift, a closer inspection reveals that the curves also differ in their shapes.

To explain the qualitative differences among the shapes of C-V curves in Fig. 5.6, V_{TSS} under different conditions is matched with that of the bulk-Si one. Then the curves take the form as shown in Fig. 5.7. From the figure it can be observed that, strained C-V curves have lower value in moderate inversion but higher value in strong inversion compared to those of control-Si device.

Fig. 5.7, can be explained with the help of Eqs. (5.4), (5.5), (5.6) and (5.7). At moderate level of inversion, both z_{avg} and z_d have nearly equal and opposite effects towards $|\Delta\phi_S|$ such that $|\Delta V_{GS}|$ remains nearly same as that of unstrained condition. But as the total charge is now decreased due to a lower z_d (Eq. (5.5)),

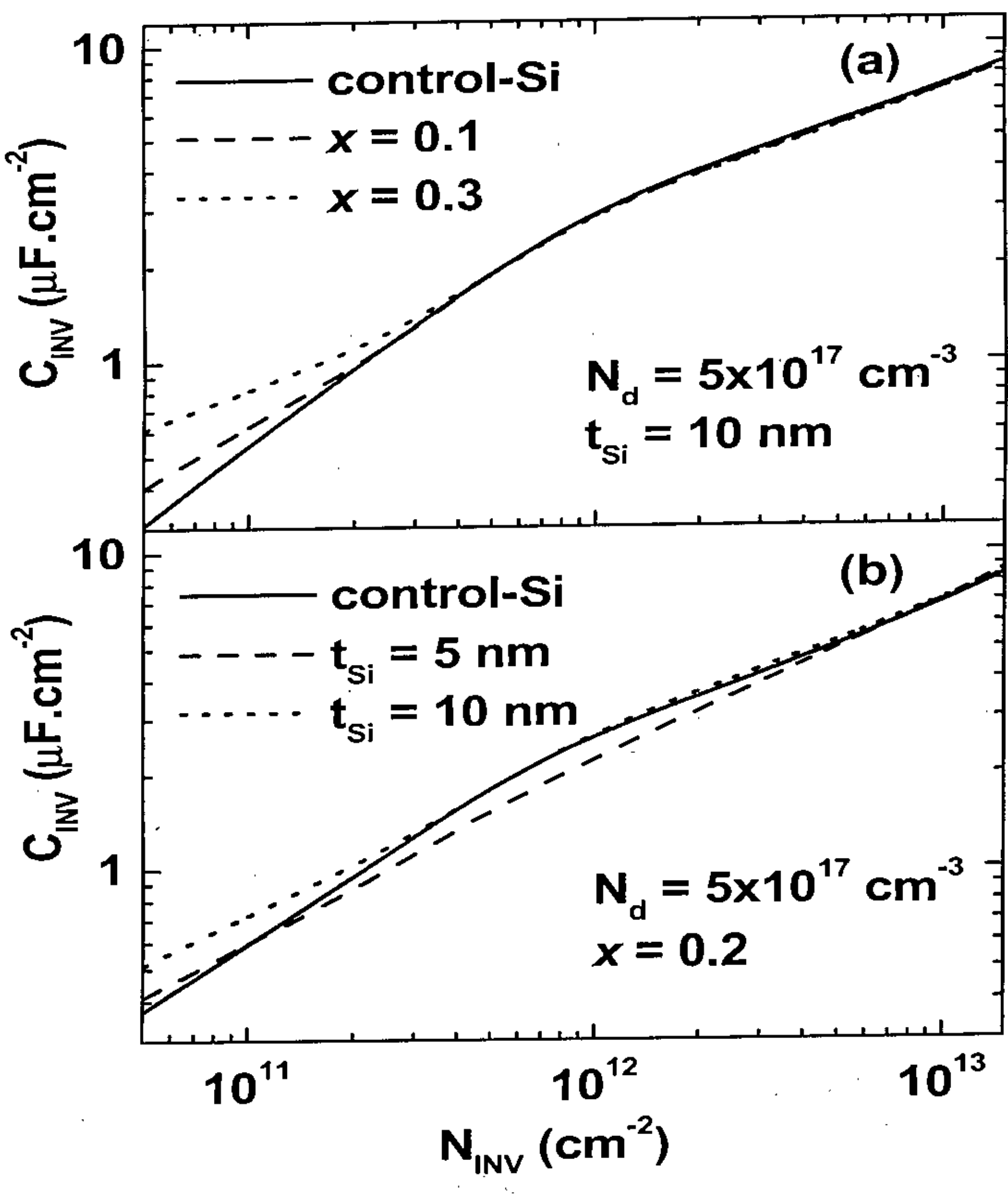


Figure 5.5: Inversion capacitance C_{INV} vs N_{INV} with (a) varying x, (b) varying t_{Si} where $N_d = 5 \times 10^{17}$ cm^{-3} and $x = 0.2$.

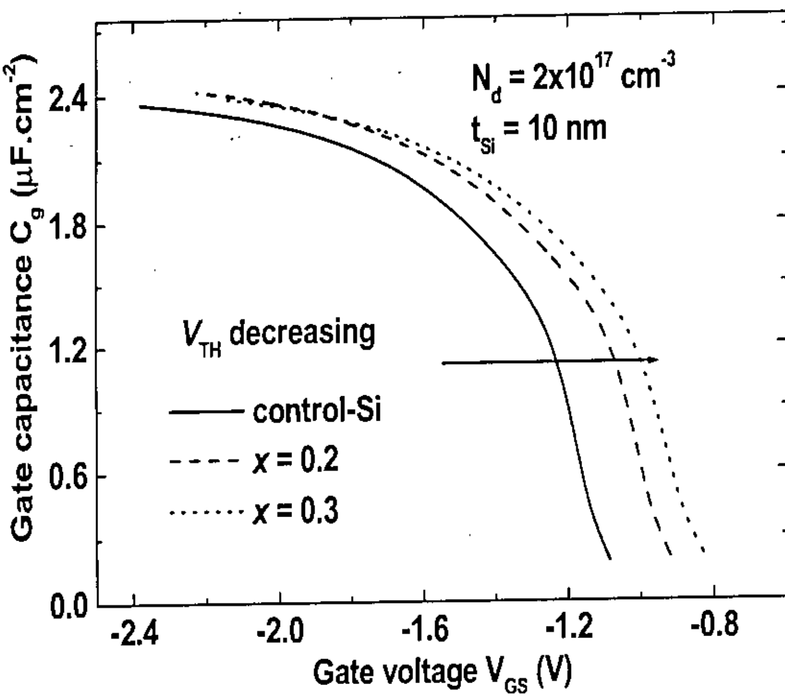


Figure 5.6: Gate capacitance C_g vs. gate voltage V_{GS} curve showing a decrease in V_{TH} in SS-pMOS device for higher x where $N_d = 2 \times 10^{17}$ cm^{-3} and $t_{Si} = 10$ nm.

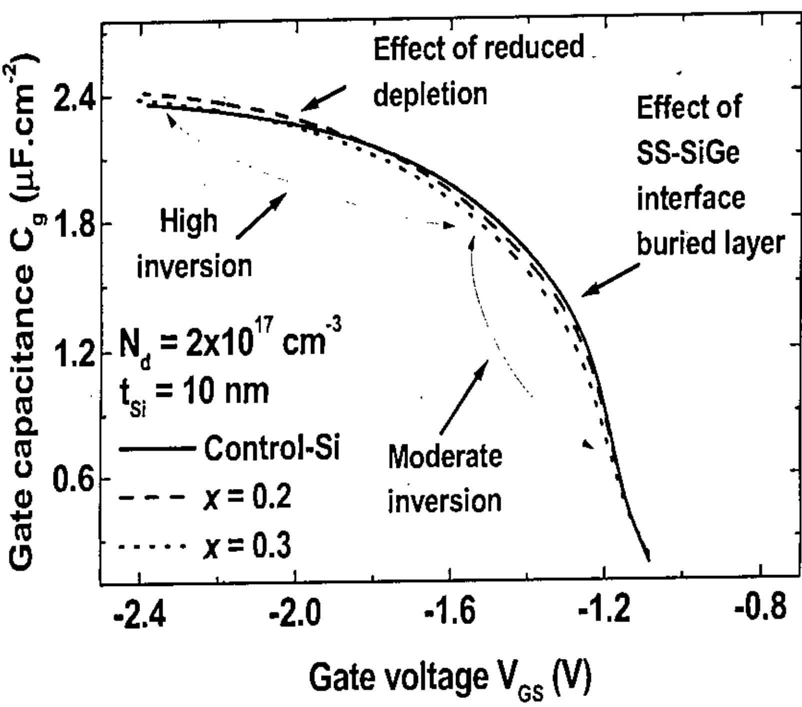
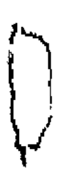


Figure 5.7: Gate capacitance C_g vs. gate voltage V_{GS} curve in matched V_{TH} condition where all the parameters are same as in Fig. 5.6.



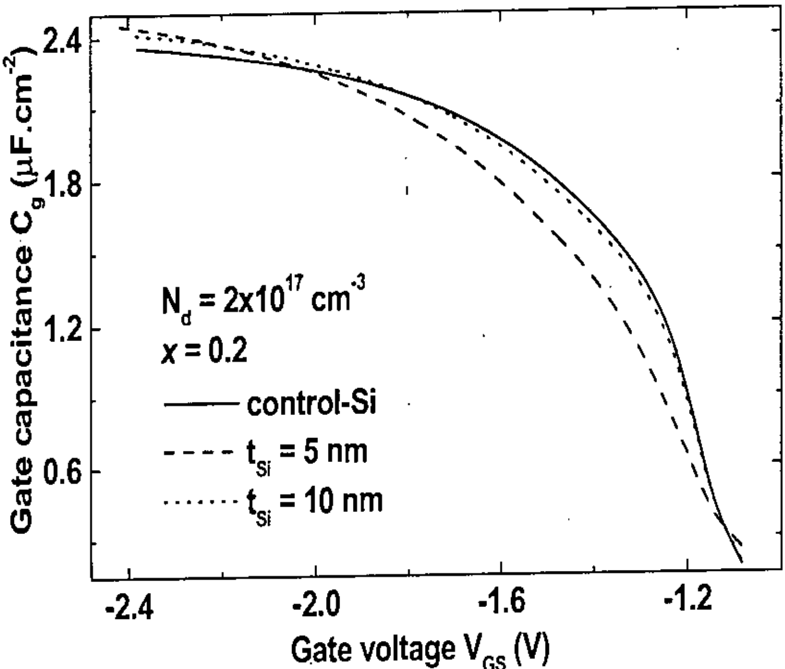


Figure 5.8: Effect of t_{Si} on gate capacitance C_g vs. gate voltage V_{GS} curve in matched V_{TH} condition for $N_d = 2 \times 10^{17}$ cm^{-3} and $x = 0.2$.

strained C_g now decreases. At strong inversion, as Δz_{avg} becomes smaller and hence $|\Delta V_{GS}|$ is also become smaller owing to smaller $\Delta\phi_{IN}$ (Eq. (5.6), (5.7)). This condition again causes the strained C-V curve to supersede at high inversion.

To compare the effect of t_{Si} on C-V characteristics, Fig. 5.8 is provided. At low inversion, thinner t_{Si} has lower C_g due to the increased effect of z_{avg} on $|\Delta V_{GS}|$ than in thicker t_{Si}. At moderate level, as z_d decreases more for thinner t_{Si}, C_g decreases further as well. At higher inversion the cross-over in C-V curves is for similar reasons explained above.

Effect of doping density on C-V characteristics is another important issue. To explain it, two different doping densities have been taken under consideration. For a higher and a lower range $N_d = 10^{18}$ cm^{-3} and 8×10^{16} cm^{-3} are taken, respectively. When a higher doping density is considered, the effect of strain is suppressed as shown in Fig. 5.10. In that case, the oxide-surface electric field is so high that the parasitic effect becomes negligible. So z_{avg} remains closer to the

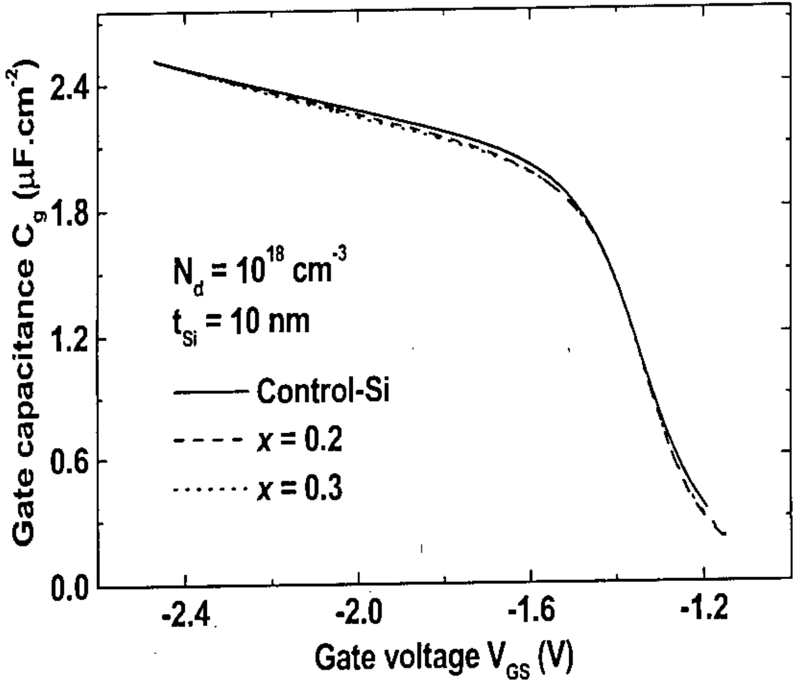


Figure 5.9: Effect of high doping density on gate capacitance C_g vs. gate voltage V_{GS} curve in matched V_{TH} condition where $N_d = 10^{18}$ cm^{-3} and t_{Si} = 10 nm.

oxide surface and Δz_{avg} in strained device remains same as in control-Si device. As a result, both the strained and unstrained C-V curves nearly overlap each other.

At lower N_d, C-V curve shows a notable characteristic. When the inversion concentration approaches from moderate to strong, a kink is observed in the strained C-V curve. Such a type of kink is also reported in [31, 30] in experimental SS-nMOS accumulation region capacitances. This is termed as a 'plateau' in the gate capacitance. For SS-nMOS devices, the kink in accumulation has been attributed to the charge confinement of holes in the SS/SiGe buried layer. Semiclassical models also show this 'plateau' in [31, 30]. Recently a semiclassical single-piece charge model has been proposed by Chandrasekaran *et al.* [32]. It is already mentioned that confinement in SS/SiGe interface buried layer is higher for higher x and lower t_{Si}. For higher x the second well is deeper and can contain sufficient charge even at flat band of SS/SiGe interface. So, at lower V_{GS}, accumulation starts at the SS/SiGe interface. When V_{GS} crosses the flat-band voltage of SiGe layer, hole accumulation ceases in SS/SiGe interface and starts

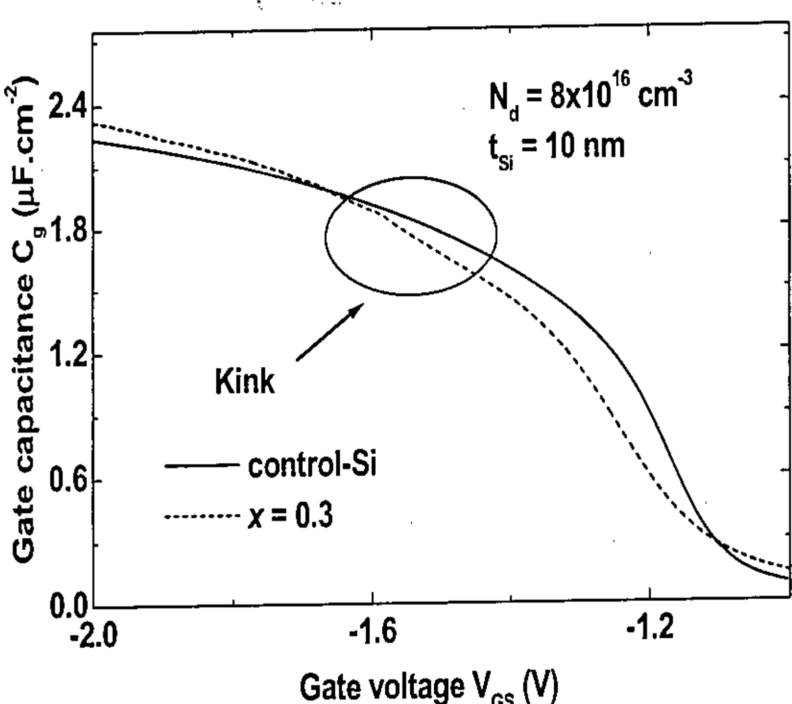


Figure 5.10: Effect of lower doping density on gate capacitance C_g vs. gate voltage V_{GS} curve in matched V_{TH} condition where $N_d = 8 \times 10^{16}$ cm^{-3}, $t_{Si} = 10$ nm and $x = 0.3$.

at SiO_2-SS interface. The kink is found in the C-V curve when there is a shift of accumulation charge from SS/SiGe interface to SiO_2-SS interface. During this transition, $|\Delta V_{GS}|$ is increased as the distance of the accumulation charge centroid (z_{avACC}) from the oxide surface decreases sharply. As a result, a dip in the C-V curve is observed.

Such kink has been identified by Armstrong *et al.* [29] also in SS-pMOS device inversion region, but the analysis was semiclassical and the reasons were not well identified. Such a kink in inversion region of SS-pMOS device has also been identified in our work and going to be analyzed with the QM model. Low doping density exaggerates the parasitic effect as the secondary well has nearly the same depth as the primary well at high x and thin t_{Si}, in fact SS/SiGe well can be on top for lower inversion charges.. So inversion carrier holes gather at SS/SiGe interface. After a certain V_{GS} value, holes move to SiO_2-SS interface. In this case the 'kink' is weaker due to the presence of depletion charges.

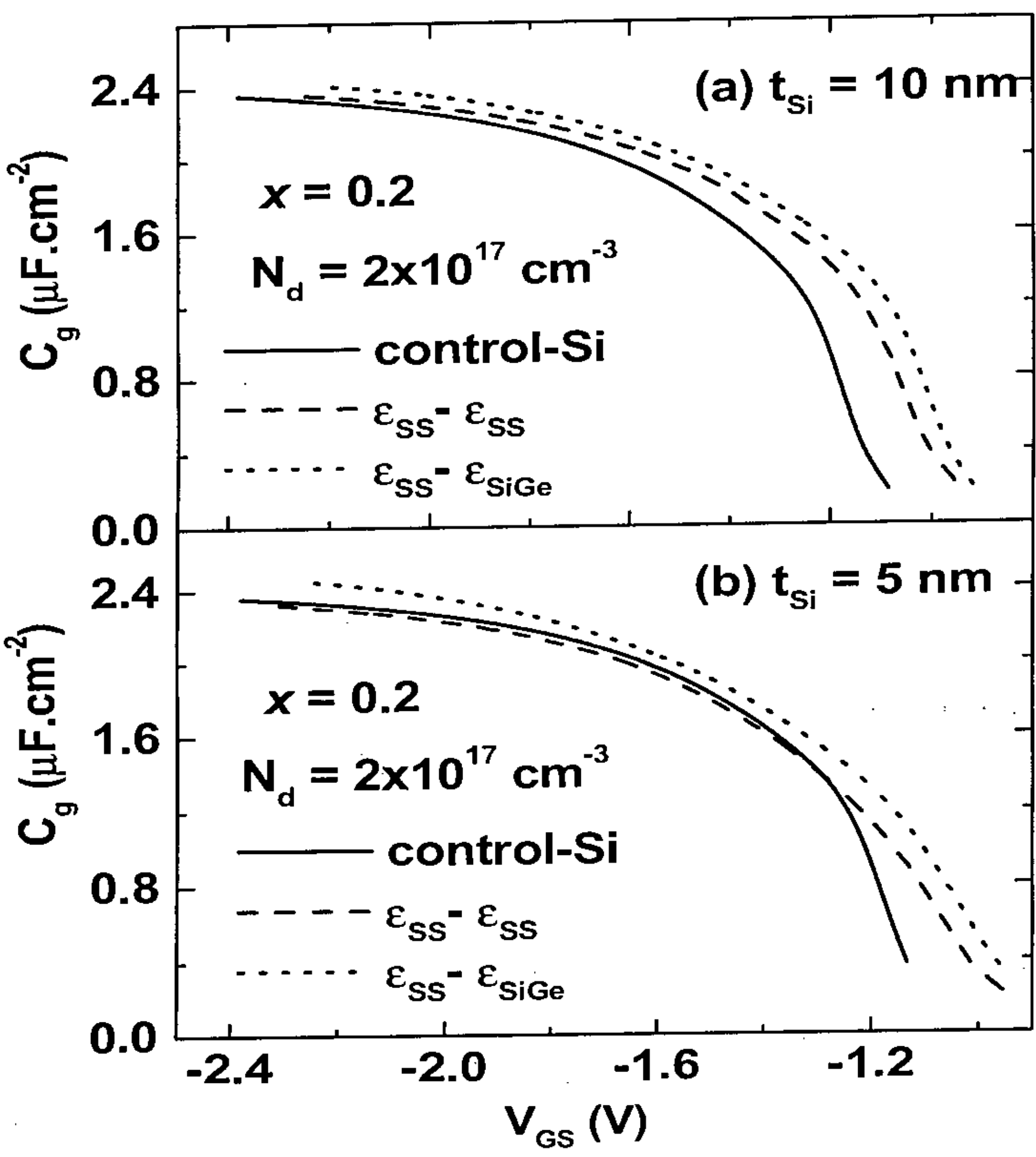


Figure 5.11: Effect of neglecting ϵ_{SiGe} on C-V characteristics for $N_d = 2 \times 10^{17}$ cm^{-3} for (a) $t_{Si} = 5$ nm , (b) t_{Si}= 10 nm. $\epsilon_{SS} - \epsilon_{SS(SiGe)}$ represents the values of dielectric constants used in SS and SiGe regions, respectively.

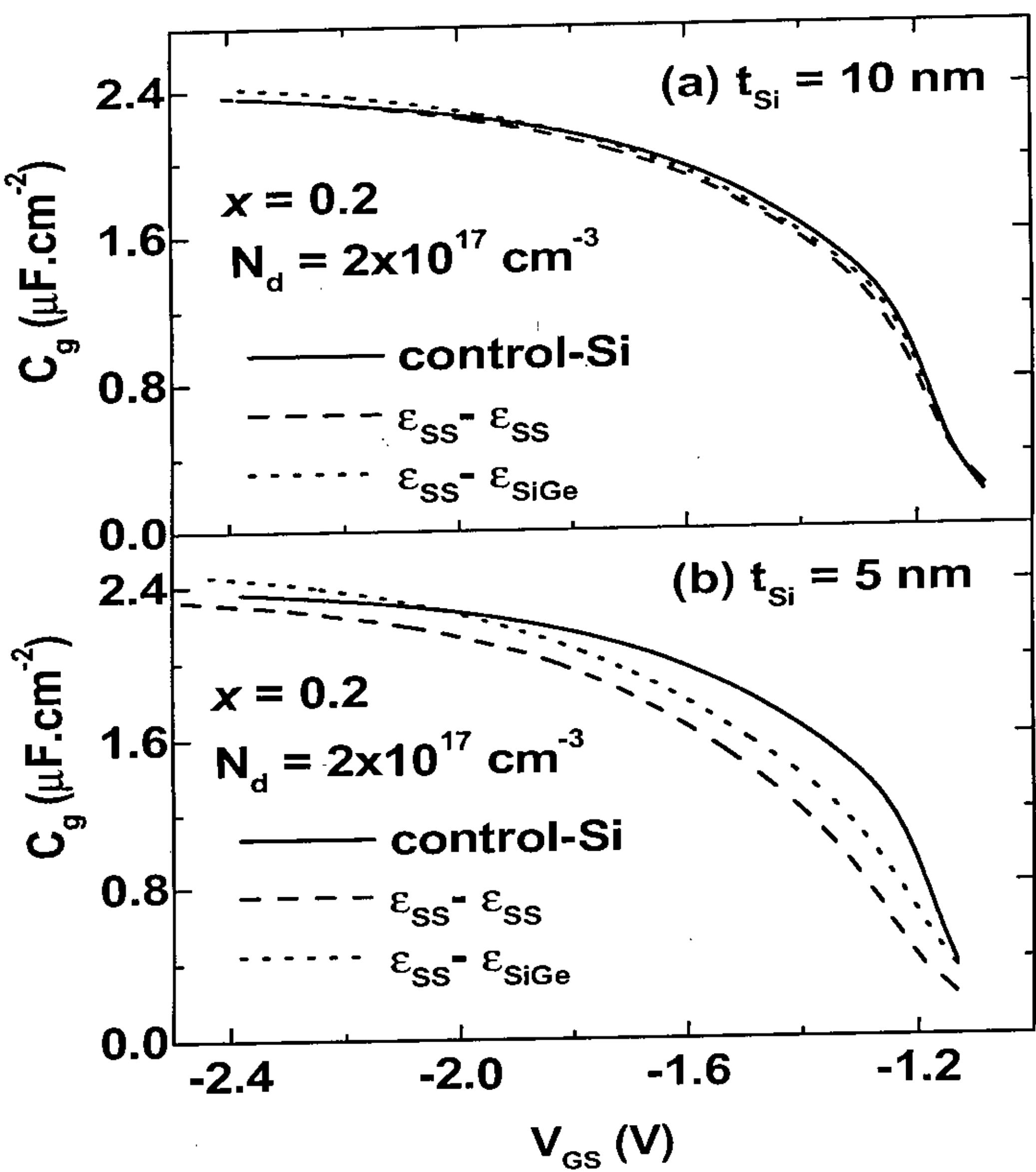


Figure 5.12: Effect of neglecting ϵ_{SiGe} in strained C-V characteristics under matched V_{TH} condition for similar parameters as in Fig. 5.11.

Fig. 5.11 shows the effect of neglecting ϵ_{SiGe} on C-V curves for two different t_{Si}. ϵ_{SS}-$\epsilon_{SS(SiGe)}$ in the figure corresponds to the value of the dielectric constants that have been considered for SS-SiGe regions. Comparatively a smaller shift in the strained C-V curves has been observed when the dielectric constant of the SiGe region is chosen to be the same as that of SS region (ϵ_{SS}). The amount of shift increases further for thinner t_{Si}. The reasons for V_{TH} shift under these conditions have already been discussed in details in chapter 4.

Fig. 5.12 presents the same curve as in Fig. 5.11 but under matched V_{TH} condition. From Fig. 5.12, it can be understood that, in addition to underestimation in V_{TSS} reduction, negligence of ϵ_{SiGe} also affects the shape of strained C-V characteristics. The difference in two strained C-V curves is prominent in the moderate inversion condition. When ϵ_{SS} is considered for SiGe layer, lower dielectric constant increases ϕ_{SiGe}. This makes SiO_2-SS surface quantum well deeper than parasitic well. As a result, z_{avg} is increased less compared to $\epsilon_{SS}-\epsilon_{SiGe}$ case. So z_{avg} under strain does not differ much from that of the unstrained case and hence ϕ_{IN} is underestimated. Moreover, overestimation of z_d also increases ϕ_{dS}. These two together, ultimately increase $|\Delta\phi_{SS}|$ in similar conditions when ϵ_{SiGe} is considered. In other words,, when ϵ_{SiGe} is not considered, for the same change in inversion carrier concentration at the SiO_2-SS surface, $|\Delta V_{GS}|$ increases relative to the case when ϵ_{SiGe} is considered. Hence, C_g decreases even more. The reduction is more significant when thinner t_{Si} is considered, shown in Fig. 5.12(b). For thinner t_{Si} at strong inversion Δz_{avg} becomes smaller again which causes the ΔV_{GS} to decrease due to lower z_d.

5.3 Results and discussions for nMOS devices

Self-consistent calculation has also been performed in SS-nMOS devices. Here SiO_2 has been used as the gate dielectric with $T_{OX} = 1$ nm and Al has been used as the gate electrode. Other material parameters are taken from Tables 2.1-2.4. To demonstrate the effect of strain on SS-nMOS C-V characteristics Fig. 5.13 is presented. Fig. 5.13 shows strained C-V curves for various x. The lateral shift in C-V curves is due to the reduction in V_{TH} with increasing x.

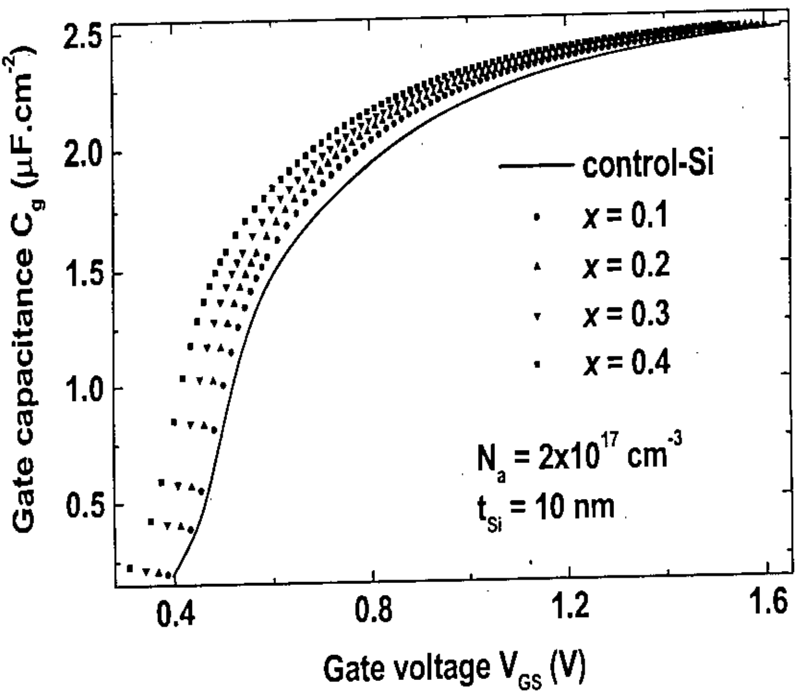


Figure 5.13: C-V curve for SS-nMOS device in different x where $N_a = 2 \times 10^{17}$ cm^{-3} and $t_{Si} = 10$ nm.

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To compare the shapes, Fig. 5.14 has been presented under matched V_{TH} condition. From Fig. 5.14 it can be seen that C_g increases with increase in strain in moderate inversion region. At low and high inversion region the curves do not differ much.

In SS-nMOS device the conduction band edge in the SS layer is lower than that of the SiGe layer. This increases electron confinement within the SS layer. In other words, z_{avg} is smaller compared to control-Si case. So Δz_{avg} (Eq. (5.7)) is even smaller. Effect of this reduction is not prominent in low inversion, as lower N_{INV} lowers the contribution of $\Delta\phi_{IN}$ in $\Delta\phi_S$. Similarly in strong inversion, when z_{avg} does not vary much with strain, lower Δz_{avg} diminishes $\Delta\phi_S$. But at moderate level, when both N_{INV} and Δz_{avg} has considerably higher value, $\Delta\phi_{IN}$ is significant. So decrease in Δz_{avg} under strained condition decreases ΔV_{GS} and makes the strained C_g greater. It can be also realized that thinner t_{Si} would have even greater C_g owing to higher confinement near the SiO_2-SS interface.

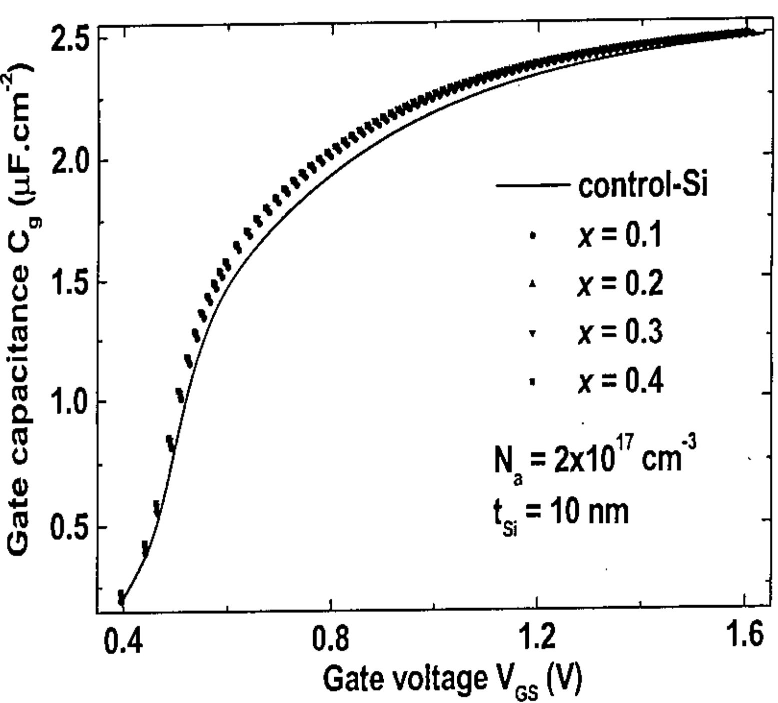

Figure 5.14: C-V curve of Fig. 5.13 under matched V_{TH} condition.

Chapter 6

Modeling of Direct Tunneling Gate Current

It is well-known that due to finite height and width of gate dielectric potential barrier, the inversion layer quantum well becomes leaky. In such case, inversion electrons can tunnel into the gate electrode from the inversion layer, resulting in a direct tunneling gate current. In this chapter, DT current in strained n and p type MOS devices are modeled.

6.1 DT current calculation procedure

The Hamiltonian for a finite system becomes non-Hermitian and the eigenenergies become complex when Schrödinger's equation is solved under open boundary conditions [45]. The real parts of the eigenvalues give the energies of the quasi-bound states and the imaginary parts are related to lifetimes. Most often, to avoid complexity, self-consistent solutions neglect tunneling effect. But through the technique described in Chapter 2, DT current can be calculated in a straight forward fashion incorporating wave function penetration effect with in the self-consistent loop.

The gate current due to quantum mechanical tunneling is calculated from carrier concentration and lifetimes of the carriers at all eigenstates using the following relationship,

$$J = \sum_i \frac{eN_i}{\tau_i}. \tag{6.1}$$

Here N_i is the concentration of the electrons in the ith eigenstate (Eq. (3.3)), τ_i is the lifetime of the electrons in the ith eigenstate and J is the total DT gate current density. The peaks of the energy broadened 1D DOS occur at the eigenenergies of the quasi-bound states and the lifetimes of the inversion layer electrons are related to the energy broadening of DOS according to,

$$\tau_i = \frac{\hbar}{2\Gamma_i} \ . \tag{6.2}$$

Here Γ_i is the Full-Width at Half-Maximum (FWHM) of the energy broadening around the ith eigenenergy [45]. The position dependant DOS as a function of energy around each eigenenergy is calculated using Eq. 3.25. Once self-consistent potential profile is obtained considering DT effect on potential profile, gate leakage current can easily be determined from Eq. (6.1) and Eq. (6.2) by searching FWHM broadening of DOS.

6.2 Results and discussions

We have calculated DT current for both n and p type SS/SiGe devices. Gate electrode and gate dielectric material are considered the same as in C-V analysis. DT current in SS/SiGe devices has been calculated to investigate the influence of strain on quantum tunneling under various t_{Si} and x conditions and compared with those of unstrained bulk-Si devices. To compare with the bulk-Si device, V_{TH} under strain is matched to the corresponding bulk-Si V_{TH} as was done in C-V analysis.

At first, the DT current in an SS-nMOS device is discussed. Fig. 6.1 shows the DT current in a SS-nMOS device for different x with a particular N_a and t_{Si}. From the figure it is seen that gate current reduces with strain. The reduction enhances with the increase in x. It is known that, DT current depends on both the gate dielectric thickness and the barrier height. When Si layer is under strain, electron affinity (χ_{SS}) becomes greater than in the unstrained condition as seen from Table 2.1. Increased χ_{SS} suppresses the tunneling of electrons into the dielectric material. Consequently, DT current is reduced in SS-nMOS device. An experimental verification of the trend predicted by our model can be found in [34]. Here the authors too have suggested that increase in barrier height due

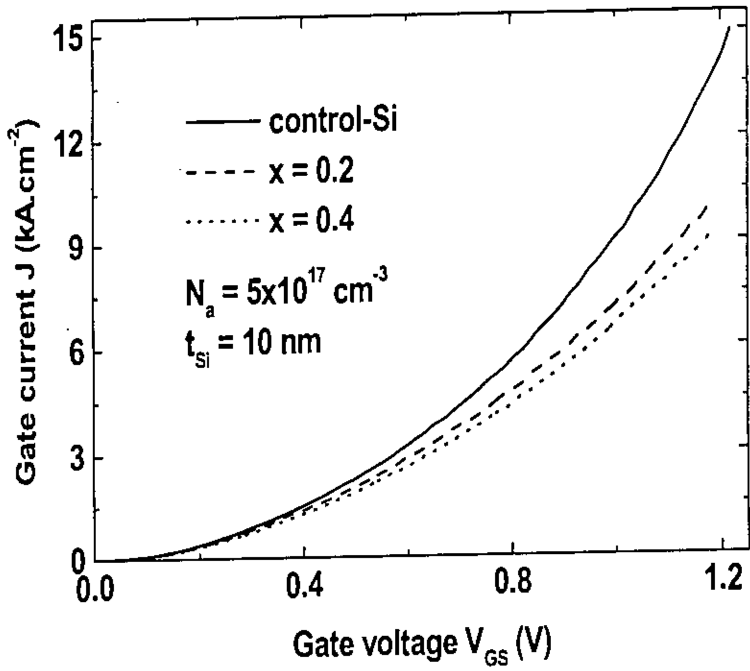

Figure 6.1: DT gate current J vs. gate voltage V_{GS} plot for a SS-nMOS device for different x in matched V_{TH} condition. Here $N_a = 5 \times 10^{17}$ cm^{-3}, $t_{Si} = 10$ nm, and $T_{OX} = 1$ nm.

to band splitting is responsible for this trend.

Fig. 6.2 shows the effect of t_{Si} on DT current. Though not much influence of t_{Si} variation over DT can be seen in the figure at low inversion, at moderate to high level of inversion, thinner t_{Si} shows slightly higher DT current. The reason is also understandable from the viewpoint of the effective barrier height. Effective barrier is the height of the barrier relative to the first eigenstate of the semiconductor quantum well. In case of thinner t_{Si}, first eigenstate has higher energy compared to the thicker t_{Si} case owing to higher depth and increase in narrowness of the well for the same inversion condition. As a result, probability of tunneling increases for thinner t_{Si}.

In SS-pMOS device, the DT current shows a rather interesting pattern. From Fig. 6.3 it can be seen that the gate current increases upto certain x and decreases afterwards although the change in J for pMOS is smaller than that in nMOS. This phenomenon can be explained with the help of the changes in barrier height

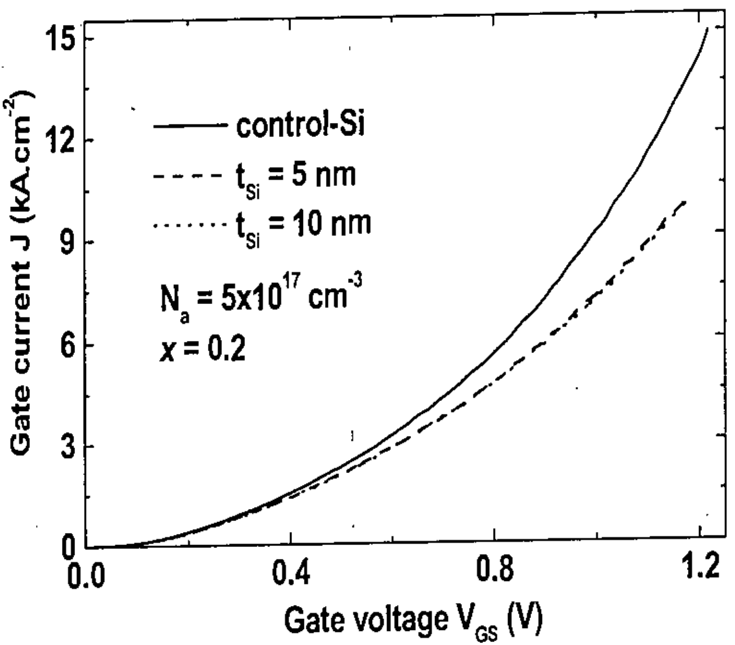

Figure 6.2: DT gate current J vs. gate voltage V_{GS} plot for a SS-nMOS device for different t_{Si} in matched V_{TH} condition. Here $N_a = 5 \times 10^{17}$ cm^{-3}, $x = 0.2$, and $T_{OX} = 1$ nm.

(ϕ_B) in the pMOS device. ϕ_B can be defined as,

$$\phi_B = E_{gSiO_2} - (\chi_{SS} + E_{gSS}) \tag{6.3}$$

where, E_{gSiO_2} and E_{gSS} are the bandgaps of SiO_2 and SS layers, respectively. From the plot of Eq. (6.3) shown in Fig. 6.4, it can be verified that ϕ_B decreases upto $x = 0.25$ and then it increases again. As long as, ϕ_B shows a decreasing pattern DT current increases with x and afterwards it reverses this trend. Moreover, the small change in ϕ_B is responsible for the small change in J.

To show the effect of t_{Si} on DT current behavior of SS-pMOS device, Fig. 6.5 has been presented. Form the figure, it is seen that, thinner t_{Si} shows lower DT current. This can be explained by the effect of buried layer in SS-pMOS device. Due to buried layer effect, z_{avg} increases and thus, it reduces tunneling probability.

The effect of increasing doping density on DT current in SS-pMOS device is non-trivial. It has been investigated that for higher doping density, other than

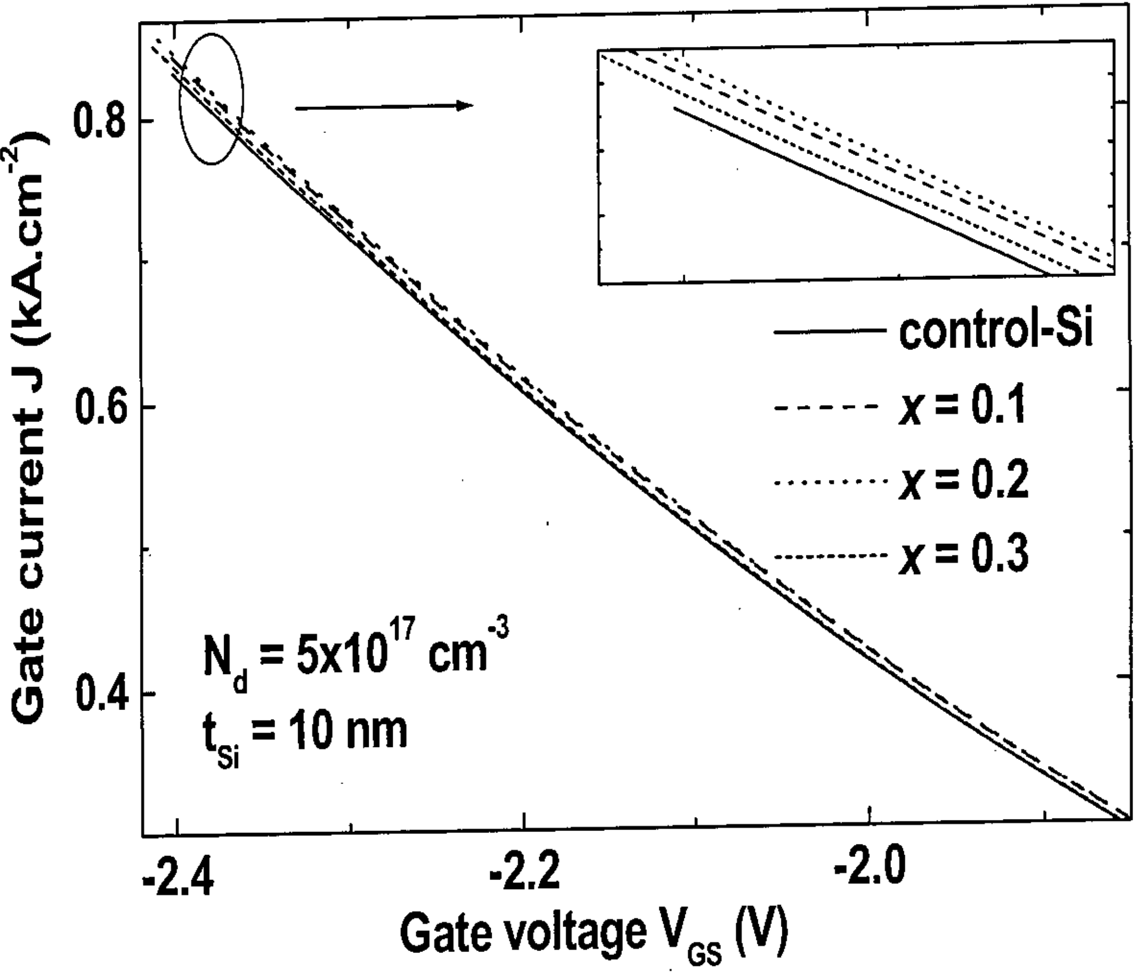

Figure 6.3: DT gate current J vs. gate voltage V_{GS} for a SS-pMOS device for different x in matched V_{TH} condition. Here, $N_d = 5 \times 10^{17}$ cm^{-3}, $t_{Si} = 10$ nm and $T_{OX} = 1$ nm. The inset shows the same plot in high inversion region to clarify the increase in DT current followed by a decreasing trend.

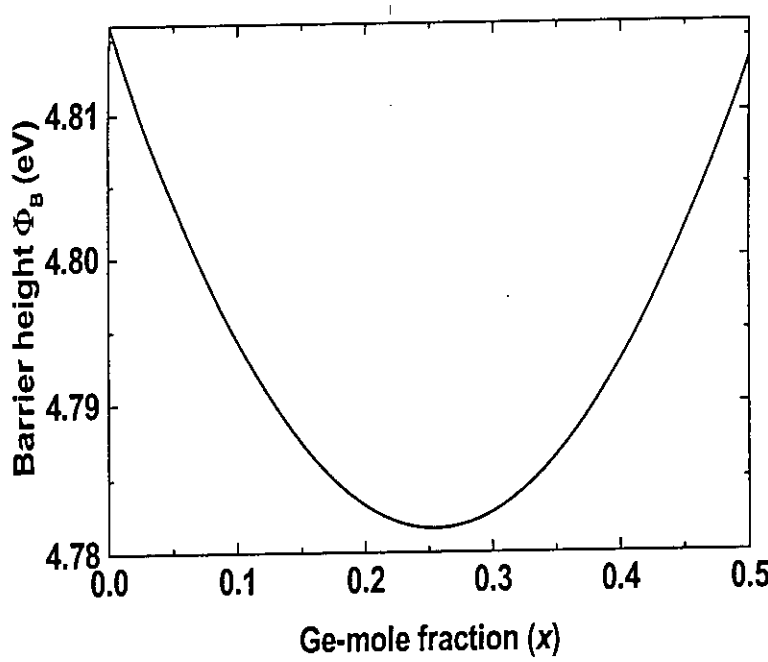

Figure 6.4: Variation in barrier height ϕ_B with the change in x for a pMOS.

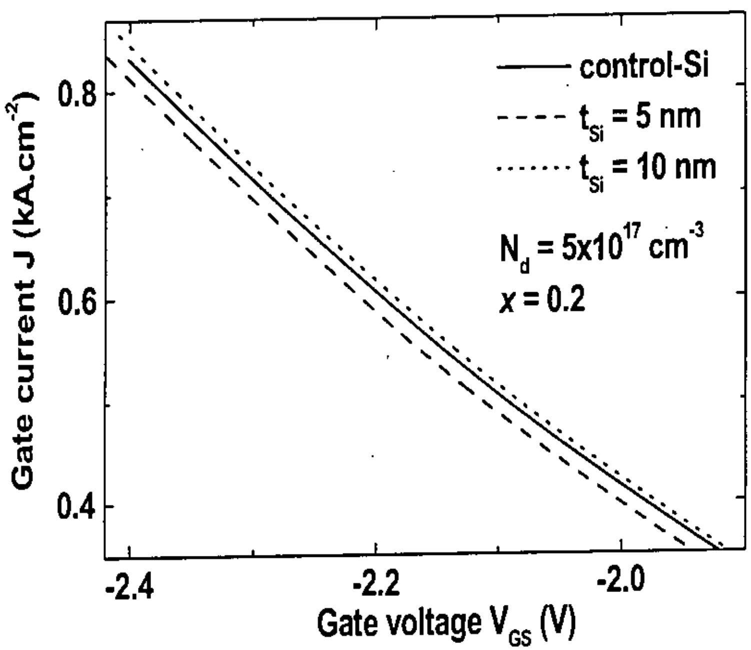

Figure 6.5: DT gate current J vs. gate voltage V_{GS} for a SS-pMOS device for different t_{Si} in matched V_{TH} condition. $N_d = 5 \times 10^{17}$ cm^{-3} , x = 0.2, and T_{OX} = 1 nm.

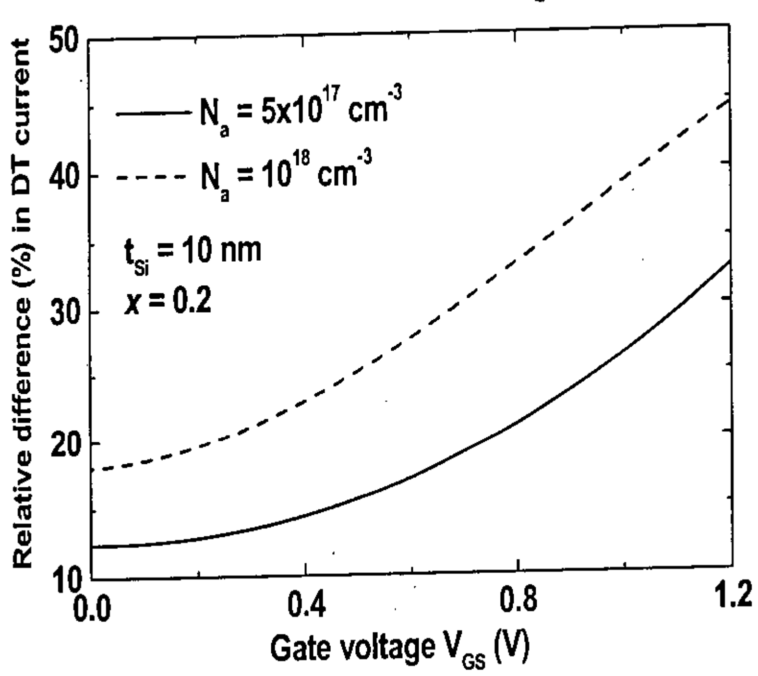

Figure 6.6: Effect of doping density on J in SS-nMOS device for different x in matched V_{TH} condition. Here $x = 0.2$ and $t_{Si} = 10$ nm.

increase in magnitude the relative difference in DT current between strained and unstrained devices $((J_{US} - J_{SS})/J_{US})$ shows similar patterns as in lower doping density (Fig. 6.3). However, in SS-nMOS device, higher doping density has an advantageous effect. Fig. 6.6 shows, the relative difference $(J_{US} - J_{SS})/J_{US}$ at two doping densities. From the figure it is clear that in case of higher N_a, strained device shows more reduction in DT current compared to lower N_a.

Chapter 7

Conclusion

7.1 Summary

Strained Si MOS devices on relaxed SiGe buffer layer has been analyzed in this study. The work focussed on the electrostatic behavior of SS/SiGe MOS devices. The analysis consists of a quantum mechanical and a semiclassical model. In the quantum mechanical model, the effect of wave function penetration into the gate oxide has been considered. Penetration effect are included within the self-consistent loop by solving Schroödinger's and Poisson's equations taking into account wave function penetration. Green's function formalism has been used for the solution of Schrödinger's equation. Poisson's equation has been solved numerically for the entire oxide and semiconductor regions taking into account both SS and SiGe layer dielectric constants. In our model, a new definition of threshold voltage, based on the principle of equal current density, has been used. Gate capacitance has been calculated from the fundamental relationship. To obtain DT current, the lifetimes of quasi-bound states are calculated from the broadening of the 1-D DOS around each eigenenergy. In the semiclassical model, a straight forward expression for total semiconductor charge has been derived based on charge sheet approximation. The total charge is dependent on SS and SiGe bandgaps, SS layer thickness and SiGe dielectric constant.

Results of V_{TH} calculation in both SS-n and -pMOS devices show that strain reduces V_{TH} in SS devices compared to bulk-Si devices. The cause of reduction is rooted in the splitting of both conduction and valance bands that modifies the bandgap, electron affinity, band offset and different effective mass parameters.

Also SS-thickness controls the degree of charge quantization in the well which in turn effects V_{TH}. The reduction of V_{TH} increases with increasing x, decreasing t_{Si} and decreasing doping densities. Moreover, if SiGe dielectric constant is considered, SS devices show further reduction in V_{TH}. This additional reduction in V_{TH} can explain the mismatch between experiment and existing QM theory. It has been found that, for SS-nMOS device, reduction in ϕ_{SS} is the key factor for V_{TH} reduction. On the other hand, in SS-pMOS device, competing effect of ϕ_{SS} and V_{FB} reduction determines overall reduction in V_{TH}. In all cases changes in V_{OX} is non-trivial. A comparison between semiclassically and quantum mechanically calculated V_{TH} reduction shows that upto a certain x and beyond a certain t_{Si} the two models are in reasonable agreement. The reduced threshold voltage in turn, can reduce the power supply requirement in MOS devices.

In the C-V calculation, it has been observed that in addition to V_{TH} reduction, SS devices, especially pMOS, show a notable qualitative differences to that of control-Si devices. In SS-pMOS devices, at moderate inversion levels gate capacitance decreases, but at strong inversion level it increases compared to unstrained gate capacitances. The difference is enhanced for lower doping densities and thinner t_{Si} conditions. On the contrary, qualitative changes in the SS-nMOS devices are not significant compared to that of SS-pMOS devices.

In the DT current analysis, SS-nMOS device shows a reduction in gate current with increase in strain. This is attributed to the increase in electron affinity in SS-nMOS device that increases the barrier height. But the SS-pMOS device shows rather an intersting behavior. DT current increases upto a certain x and then again decreases. This is due to the non-monotonic variation in barrier height with x.

7.2 Suggestion for the future work

In our work, calculation of threshold voltage through semiclassical analysis has been performed only for SS-nMOS devices. Similar expression can be obtained for the SS-pMOS devices following a procedure described in Chapter 2. Also, the model neglects the band offset between SS/SiGe interface. Including this term in

the surface potential calculation can improve the model.

We have studied the tensile strain effect on the Si layer in MOS devices. A compresive strain can be found when SiGe layer is grown on Si layer. Such compressive strain improves the hole mobility in pMOS devices and is expected to be more efficient when coupled with SS-nMOS devices in CMOS applications. Our model can be used to analyze strained SiGe-pMOS after necessary modifications of the band structure parameters.

For SS/SiGe devices, accumulation region capacitance has been much discussed in recent works as important properties like 'plateau' in the gate capacitance is found in the accumulation region of SS-nMOS devices. We have used the self-consistent QM model to study the inversion and depletion region properties of the SS/SiGe devices. Certain modifications of the model can be used to simulate the accumulation region characteristics.

In this work we concentrated fully on SS-MOSFET grown over (100) Si substrate. The model can also be modified to analyze the MOS properties when the channel surface is grown on (111) or (110) Si. It has been found that (110) surface channel pMOSFETs grown over (100) Si, doubles the hole mobility compared to the (100) surface channel pMOSFETs.

Few works on SS/SiGe tunneling characteristics has been done up to date. DT current behavior in high-K gate materials is yet to be investigated. For high-K gates, the effective oxide thickness and the effective mass of the dielectric material should be changed to determine tunneling current. Also, there are reports of fabrication difficulties in SS/SiGe device due to Ge outdiffusion in the channel from the SiGe layer in addition to SiO_2 from the dielectric. In that case, the model should include the effect of traps or other interfacial states.

We have essentially analyzed a MOS capacitor rather than a MOSFET itself because we did not account any drain-to-source voltage that can cause 2-D quantization of carrier. Then the Schrödinger's and Poisson's equations have to

be solved self-consistently in two dimensions. Such a model should be able to predict the transport behavior in ballistic SS/SiGe MOSFETs. When channel length is down to deep submicron range, the transport approaches to ballistic. In that case, carrier scattering can be neglected.

In the QM model, we have used effective mass approximation for both electron and holes. But we neglected anisotropy and valence band mixing and assumed the dispersion relation to be parabolic. So, whether the effective mass approximation is valid or not is another matter of importance. In SS/SiGe band structure, degeneracy splits and it reduces the band mixing effect. But on the other hand, it increases the anisotropy in the band structure. So a multiband self-consistent calculation is also worthy of interest.

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