Quantum Mechanical Analysis of Capacitance of Double Gate Ultrathin MOS Devices Incorporating the Effect of Interface States

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By

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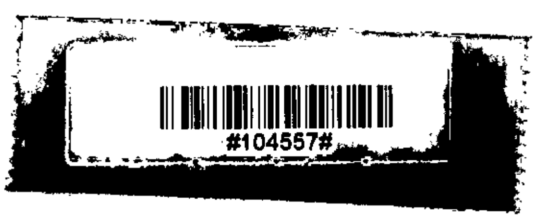

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To

My Loving Family

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Abstract

Modeling of charge quantization and Capacitance-Voltage (C-V) characteristic of ultra thin Double Gate (DG) MOSFET in deep submicron regime is studied in the presence of interface states. Self consistent modeling of double gate MOS inversion and accumulation layers have been performed by solving both Schrödinger's and Poisson's equations. A new solver based on Finite Element Method has been developed for the solution of both Schrödinger's and Poisson's equations that is much faster and more efficient than existing Schrödinger-Poisson solvers. It has the compatibility of analyzing both symmetric and asymmetric DG MOSFET structures. The developed numerical solver has been applied to fully depleted n-MOS and p-MOS DG MOSFETs to analyze electrostatics such as, inversion and accumulation layer charge density, surface potential, amount of interface trapped charges. Using these electrostatics, the C-V characteristics of the devices have been revealed which are found to be in accordance with reported data. Finally, the effect of interface states is incorporated in the C-V profile. It has been shown that the effect of interface states on C-V characteristic varies from low to high frequency operation. Interface trapped charges increase the device capacitance at low frequency and decrease it at high frequency. Also the degree to which interface trapped charges affect the capacitance, is also higher during low frequency operations. Simulation results show that increased oxide thickness amplifies the effect of interface trapped charges on device capacitance, but variation in silicon thickness or substrate surface orientation don't have any significant influence on the effect of interface states on C-V profile.

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CHAPTER 1

INTRODUCTION

1.1 Preface

Throughout the history of integrated circuit design, a general scaling methodology for MOSFET devices known as Moore's law [1] has been applied. Increase in the device density is made possible by shrinking the dimensions of each transistor. The ongoing reduction in transistor dimensions has resulted in an increment in packing density and operating frequencies of transistors. This has accelerated a tremendous technological progress and as a result, microprocessors with greater than 100 million transistors and memory chips with greater than 1Gb densities are now a reality. The key dimension that is reduced from one transistor generation to the next is the gate length (*LG*). This continued scaling is necessary for maintaining the evolutionary technological improvements that have been the foundation for integrated circuit development and design this far.

According to the 2006 International Technology Roadmap for Semiconductors (ITRS), the high performance logic limit of a device will correspond to a channel length of 13 nm with oxide thickness of less than 1 nm and a gate length of 13 nm [2]. Scaling devices to these dimensions is much more difficult and different when compared to current day scaling methodologies. This is because; metal-oxide-semiconductor (MOS) technology is approaching its limits at these dimensions. The most important issue to be addressed is how much further can aggressive device scaling be continued? Although very difficult to answer, it is clear that new and revolutionary technologies will be needed to replace conventional MOS transistors as the driver behind electronic products in the future. Development of nanoscale transistors at the limit poses numerous practical and

theoretical challenges that need to be surmounted if device scaling is to continue. Device simulation requires new modeling techniques that helps improve the understanding of device physics and design, for devices at the scaling limit.

1.2 Transistor Scaling

Basically, CMOS (complementary MOS) technology is implemented on either of two primary device structures. The first is the bulk structure, where a transistor is directly fabricated on the semiconductor substrate and the second, is called SOI (silicon-on-insulator), where a transistor is built on a thin silicon layer which is separated from the substrate by a layer of insulator. The bulk structure is relatively simple from a fabrication point of view and is still the standard structure in almost all CMOS based products.

It is crucial to maintain a balance between device functionality and device reliability in the course of device scaling. As the channel lengths are being scaled to smaller sizes, it is important to monitor these two key factors. To accomplish this, short channel effects (SCEs) have to be suppressed as much as possible. SCEs is characterized by threshold voltage (V_{TH}) variations versus channel length and drain induced barrier lowering (DIBL). Threshold voltage rolloff due to SCEs, results in a degraded subthreshold swing (S), which in turn renders it difficult to turn off a device, while DIBL results in a drain voltage dependent V_{TH}, which complicates CMOS design at a circuit level. As critical transistor dimensions are scaled, reliability concerns become more pronounced. Unwanted leakage currents due to gate tunneling and junction tunneling rapidly increase, resulting in high off-state power dissipation.

In these respect, partially and fully depleted single-gate SOI MOSFET structures have been investigated as candidates for device scaling below ~25nm because they offer improved electrical isolation between the substrate and the active device region. However, since these MOSFETs (single-gate) have a thick buried oxide which cannot terminate the electric field lines from the drain end, they exhibit severe SCE [3, 4].

Recent studies indicate that ultra-thin body dual (DG) SOI MOSFETs are better suited for ultimate scaling [5, 6, 7].

1.3 Modeling of Double-Gate (DG) MOSFET

Since CMOS scaling is approaching its limit to processing as well as fundamental considerations, Double gate (DG) MOSFETs are becoming an intense subject of VLSI design. Theoretically, DG MOSFETs can be scaled to the shortest channel length possible for a given oxide thickness [8]. Among the advantages of double-gate MOSFETs are: significant reduction of Short Channel Effects (SCE) as observed in single-gate SOI geometry, near-ideal subthreshold swing of 60 mV/decade, high transconductance, good electrostatic integrity which minimizes drain-induced barrier lowering and threshold variation with channel length [9, 10, 11].

As the gate length goes below deep submicron dimensions, the device design, as guided by scaling rules, can result in large nominal electric fields at the Si/SiO_2 interface, even near the threshold of inversion. This leads to a significant bending of the energy band at the Si/SiO_2 interface. It has long been known that with sufficient band bending, the potential well can become sufficiently narrow to quantize the motion of inversion layer carriers in the direction perpendicular to the interface [12].This gives rise a splitting of the energy levels into subbands (2-dimnsional density-of-states), such that, the lowest of the allowed energy levels for electrons in the well does not coincide with the bottom of the conduction band. Due to quantization, the electron density does not reach its maximum at the oxide-semiconductor interface as in the semi-classical profile [13, 14], instead some distance inside the semiconductor. Fig. 1.1 shows a typical conduction band profile for a double gate n-MOSFET device and Fig. 1.2 shows the electron density in silicon near Si/SiO_2 interface as obtained from Quantum Mechanical (QM) calculations.

Due to this extension of the electron density inside semiconductor, (i) the electric potential value at the interface is greater and (ii) the capacitance and the transconductance are reduced are reduced from those predicted by the semi-classical model.

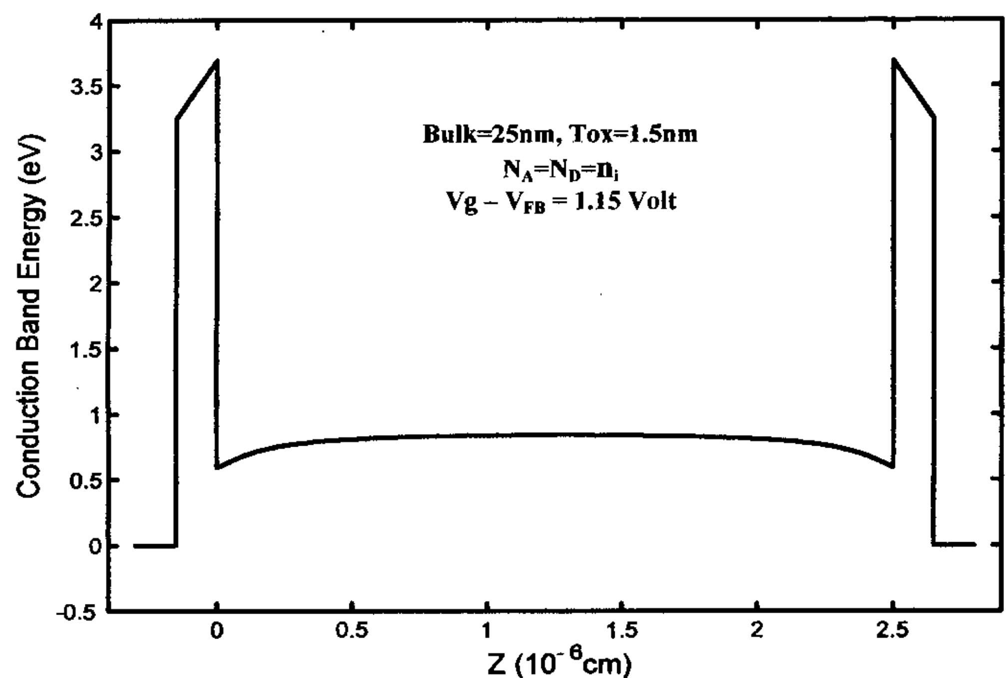


Fig. 1.1 A typical conduction band profile of a double gate n-MOSFET

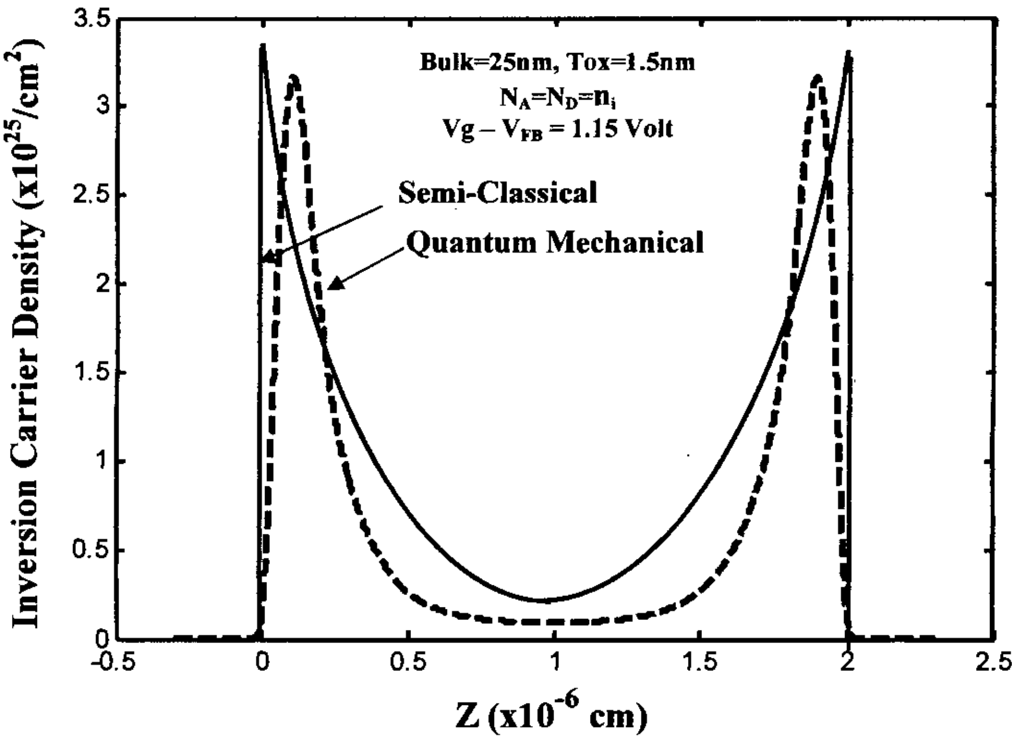


Fig. 1.2 Electron density in silicon near Si/SiO_2 interface as per Quantum Mechanical (QM) and Semi-Classical calculations

Thus it is important that the above mentioned inversion layer QM effects are incorporated in deep submicron device models. The use of traditional or semi-classical technique in device analysis and design, in which these effects are neglected, is inadequate at deep submicron dimensions and will lead to erroneous and misleading prediction of device structure and electrical behavior, such as physical oxide thickness, threshold voltage, drive current, gate capacitance and electrostatic potential. For this reason, the two-dimensional nature of electrons has to be considered in the inversion layer.

Also, since charges can move from source to drain by tunneling through the channel, the off-current value and the subthreshold swing may be dramatically degraded [15]. As a consequence of ultra-thin gate oxide requirements, electrons can tunnel to the gate, creating the gate-leakage current that is considered as one of the most severe challenge to take up for next complementary metal oxide-semiconductor (CMOS) generations, especially regarding the power consumption. So, the effect of the gate leakage current is studied extensively for a variety of MOS structures.

1.4 Literature Review

The first publication describing a double-gate SOI MOSFET dates back to 1984. The device received the acronym XMOS because of the resemblance of the structure with the Greek letter Ξ [16]. This initial paper predicted good short-channel characteristics of such a device. The first fabricated double-gate SOI MOSFET was the "fully Depleted Lean-channel Transistor (DELTA, 1989)", where the silicon film stands vertical on its side (Fig 1.3) [17]. Later vertical-channel, double-gate SOI MOSFETs (FinFET) [18] was implemented. Volume inversion was discovered in 1987 [19], and the superior transconductance brought about by this phenomenon were first experimentally observed in 1990 in the first practical implementation of a planar double-gate MOSFET called the "gate-all-around" (GAA) device [19] (Fig 1.4).

The structure that theoretically offers the best possible control of the channel region by

the gate is the surrounding-gate MOSFET. Such a device is usually fabricated using a pillar-like silicon island with a vertical-channel which include the cylindrical thin-pillar transistor (CYNTHIA) (Fig 1.5) [20] and the pillar surrounding-gate MOSFET [21].

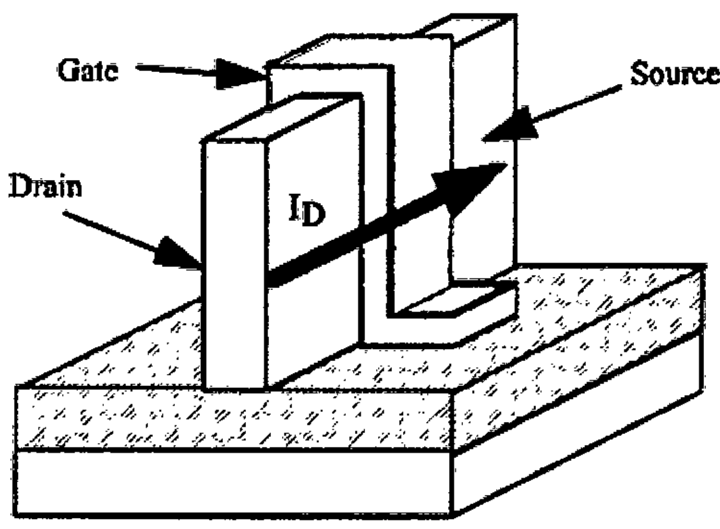


Fig 1.3. Delta/FinFET structure

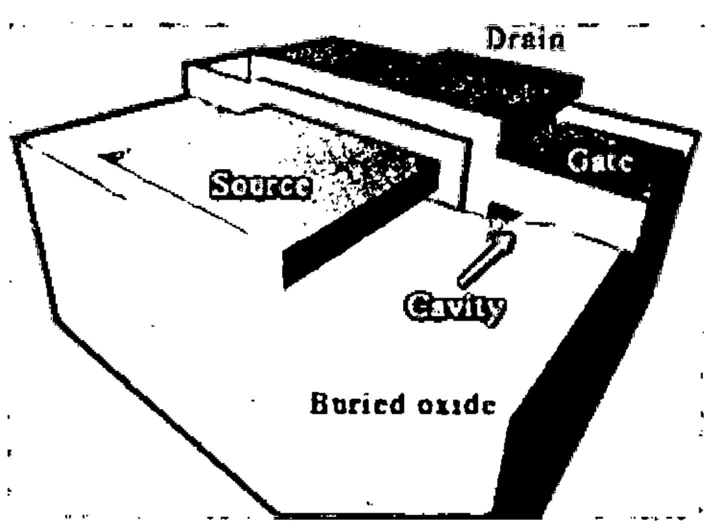


Fig 1.4. Gate-all-around (GAA) MOSFET

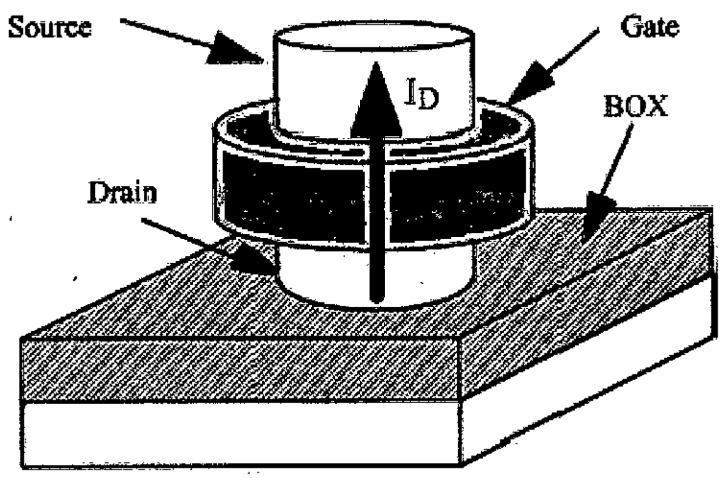


Fig 1.5. CYNTHIA / surrounding-gate MOSFET structure

The effects of volume inversion in thin-film short-channel SOI MOSFETs and the efficacy of dual-gate operation in enhancing their device performance have been analyzed by R. F. Pierret *et al.* [22] using two-dimensional device simulations and one - dimensional analytical computations. Their analyses have been restricted to the strong inversion regime, which is the practically useful region of operation of SOI MOSFETs. In this region, they suggested that when compared at constant $\mathbf{V_g}$ - $\mathbf{V_t}$ values, the dual - channel volume inverted devices do not offer significant current-enhancement advantages, other than that expected from the second channel, over the conventional single-channel devices for silicon thickness in the 0.1 μm range.

K. Suzuki *et al.* [23] established a scaling theory for double-gate SOI MOSFETs, which gives guidance for the device design. They calculated dependence of subthreshold slope S on device parameters. According to their theory, a device can be designed with a gate length of less than 0.1 μm while maintaining the ideal subthreshold factor, which is verified numerically with a two-dimensional device simulator. In a latest publication [24], they developed models for short channel n^+-p^+ double-gate SOl MOSFETs by solving a two-dimensional (2-D) Poisson's equation in the channel region, and showed how to design a device with a decreased gate length, suppressing short channel threshold voltage shift ΔV_{th} and subthreshold swing (S-swing) degradation.

G. Baccarani *et al.* [25] presented a compact model for the Double-Gate MOSFET (DG-MOSFET), which accounts for quantum mechanical effects, including motion quantization normal to the $Si-Si0_2$ interface, band splitting into subbands and non-static effects in the transport model. The model holds both in subthreshold and strong inversion, and ensures a smooth transition between the two regions.

J. M. Hergenrother *et al.* [26] showed that short-channel effects in fully-depleted double gate (DG) and cylindrical, surrounding-gate (Cyl) MOSFETs are governed by the electrostatic potential as confined by the gates, and thus by the device dimensions. For equivalent silicon and gate oxide thicknesses, evanescent-mode analysis indicates that Cyl-MOSFETs can be scaled to 35% shorter channel lengths than DG-MOSFETs.

S.-L. Jang *et* at. [27] have developed an analytical drain current model for symmetric double-gate SOI MOSFETs using a quasi-two-dimensional Poisson's equation. The model applicable for digital/analog circuit simulation contains the description of the subthreshold, near threshold and above-threshold regions of operation by one single expression. They considered effects of the source/drain resistance; on important short channel effects such as- velocity saturation, drain induced barrier lowering, channel length modulation, self-heating effect due to the low thermal conductivity of the buried oxide, impact-ionization of MOS devices, parasitic bipolar junction transistor associated with drain breakdown, etc.

B. Majkusiak *et* at. [28] have analyzed the influence of the semiconductor film thickness in the double-gate silicon-on-insulator (SOI) MOSFET on the electron concentration distribution, electron charge density, threshold voltage, electron effective mobility, and drain current. The consideration of the semiconductor region is based on two descriptions: the "classical" model based on a solution to the Poisson's equation and the "quantum" model based on a self-consistent solution to the Schrödinger's and Poisson's equation system. The electron effective mobility and the drain current are calculated with the use of the local mobility model.

Y. Taur [29] has derived a one-dimensional (I-D) analytical solution for an undoped (or lightly-doped) double-gate MOSFET by incorporating only the mobile charge term in Poisson's equation. The solution gives closed forms of band bending and volume inversion as a function of silicon thickness and gate voltage. A threshold criterion has been derived which serves to quantify the gate work function requirements for a double gate CMOS. Then in [30] the solution is applied to both symmetric and asymmetric DG MOSFETs to obtain closed forms of band bending and inversion charge as a function of gate voltage and silicon thickness. It is shown that for the symmetric DG device, "volume inversion" only occurs under subthreshold conditions, with a slightly negative impact on performance. Comparisons under the same off-state conditions show that the on-state inversion charge density of an asymmetric DG with one channel is only slightly less than that of a symmetric DG with two channels, if the silicon film is thin. From the analytic solutions, expressions for the various components of the equivalent capacitance circuit have been derived for symmetric and asymmetric DG devices.

J. O. Fossum *et al.* [31] have developed a compact physics-based quantum-effects model for symmetrical double-gate (DG) MOSFETs of arbitrary Si-film thickness. The model, based on the quantum-mechanical variational approach, not only accounts for the thin Si-film thickness dependence but also takes into account the gate-gate charge coupling and the electric field dependence; it can be used for FD/SOI MOSFETs as well. The analytical solutions, verified via results obtained from self-consistent numerical solutions of the Poisson and Schrödinger equations, provide good physical insight regarding quantization and volume inversion due to carrier confinement, which is governed by the Si-film thickness and/or the transverse electric field. A design criterion for achieving beneficial volume-inversion operation in DG devices has quantitatively defined for the first time. Further, the utility of the model for aiding optimal DG device design, including exploitation of the volume-inversion benefit to carrier mobility, is exemplified.

J. D. Meindl *et al.* [32] have developed an analytical subthreshold swing (S) model for symmetric DG MOSFETs using evanescent-mode analysis. Through a concept of effective conducting path, it explains a doping concentration (NA) dependence of S, providing a unified understanding of previous models and leading to a new model for

undoped DG MOSFETs. Expressions of a scale length have been derived, which expedite projections of scalability of DG MOSFETs and its requirement.

T. Ernst *et al.* [33] have analyzed the operation of 1-3 nm thick SOI MOSFETs, in double-gate (DG) mode and single-gate (SG) mode (for either front or back channel). They found some typical effects in these ultra-thin MOSFETs such as- threshold voltage variation, large influence of substrate depletion underneath the buried oxide, absence of drain current transients, and degradation in electron mobility. By comparing SG and DG configurations they have shown the superiority of DG-MOSFETs: ideal subthreshold swing and remarkably improved transconductance (consistently higher than twice the value in SG-MOSFETs). The experimental data and the difference between SG and DG modes have been explained by combining classical models with quantum calculations. They found that the key effect in ultimately thin DG-MOSFETs is volume inversion, which primarily leads to an improvement in mobility, whereas the total inversion charge is only marginally modified.

M. Wong *et al.* [34] have derived an analytical expression relating the potential and the electric field at the oxide-semiconductor interface of a symmetrical double-gate oxide intrinsic semiconductor-oxide system. The expression is applicable to all regimes of operation. The "turn-on" behavior of the system has been studied and an extrapolated threshold voltage has been defined. Opposite to the behavior of a conventional bulk metal-oxide-semiconductor capacitor realized on a doped substrate, this threshold voltage was shown to decrease with increasing oxide thickness.

M. Alessandrini *et at.* [35] have developed an analytical model for the electron mobility limited by surface optical phonons and applied to the simulation of ultra-thin SOI MOSFETs. The developed model reproduces the main features of experimental data recently reported in the literature and has been implemented in a conventional device simulator. An application to the analysis of technological options such as doping concentration and silicon thickness in SOl MOSFETs, have been reported.

M. J. Kumar *et at.* [36] have discussed how the short channel behavior in sub 100 nm channel range can be improved by inducing a step surface potential profile at the back gate of an asymmetrical double gate (DG) silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect-transistor (MOSFET) in which the front gate consists of two materials with different work functions.

1.4 Objective of the Work

A considerable amount of effort has been given in modeling and simulating the characteristics of double gate MOSFETs in recent works [11, 33, 37]. However there is still lack of numerical or experimental data that can reveal the quantum mechanical effects on Capacitance-Voltage characteristic of double gate MOSFET. Recently, the effect of interface states on MOS device capacitance has become of great interest. The alteration of device Capacitance-Voltage characteristics due to charges trapped in the interface states degrades the device reliability. So, in order to predict the Capacitance-Voltage characteristics efficiently, the effect of interface states should be taken into account. Present works on the effect of interface states [38, 39] cover only conventional single gate MOSFETs. So, a quantum mechanical analysis of double gate MOS capacitance incorporating the effect of interface states is in need.

The objective of this work is to develop a one dimensional (1D) self-consistent Schrödinger-Poisson solver with established accuracy and efficiency. The developed numerical solver will be applied to both n-MOS and p-MOS DG MOSFETs for analyzing electrostatics of the devices such as, inversion or accumulation layer charge, surface potential, charge contribution of interface states and hence the Capacitance-Voltage characteristic of the device will be modeled by taking the effect of interface states into account as well as neglecting it. Effect of device dimensions and substrate surface orientations will be investigated. Finally the results will be compared with reported data.

1.5 Organization of the Thesis

Chapter 2 is devoted to the theoretical study of Double Gate MOSFET. The advantages offered by a DG MOS in comparison with a SG MOSFET are also outlined in this chapter. Chapter 3 discusses the theory behind this work. In the first portion, the self-consistent modeling of double gate fully depleted MOS structure is described. A numerically efficient and faster technique is presented based on finite element method. The later portion describes how the device capacitance is modeled incorporating the effect of interface states as well as neglecting it. Chapter 4 deals with the results and discussions. In this chapter, various results obtained for n-MOS and p-MOS under different conditions are reported and discussed. Concluding remarks of this work along with suggestions for the future work are presented in Chapter 5.

CHAPTER 2

DOUBLE GATE (DG) MOSFET

In this chapter, a brief study of the Double Gate (DG) MOSFET is presented. Its advantages have been revealed with the help of a comparative study with conventional Single Gate MOSFET.

2.1 Introducing DG MOSFETs

Double-gate metal–oxide–semiconductor field-effect-transistors (DGMOSFETs) are currently considered a serious alternative to standard-bulk MOSFETs to increase the integration capacity of silicon technology in the near future. A dual-gate-silicon-on-insulator DGSOI Structure consists, basically, of a silicon slab sandwiched between two oxide layers (Fig. 2.1). A metal or a polysilicon film contacts each oxide. These films act as front and back gate, which can generate an inversion region near the Si–SiO2 interfaces, if an appropriate bias is applied. Thus we would have two MOSFETs sharing the substrate, source, and drain.

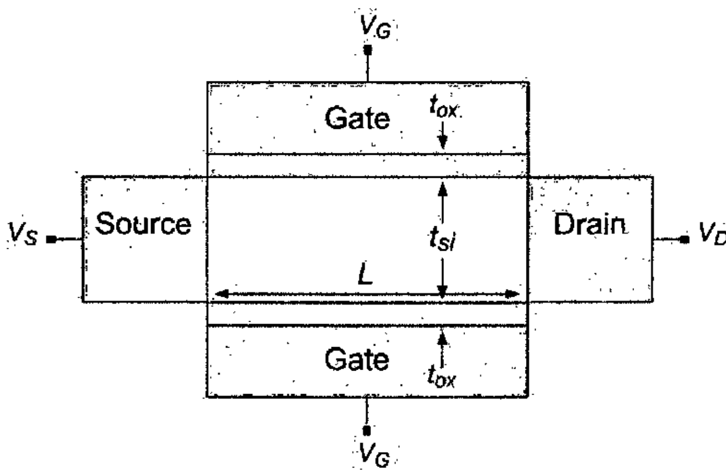


Fig.2.1. Double gate MOSFET

The salient features of the DG MOSFET [40] (Fig. 2.1) are control of short-channel effects by device geometry, as compared to bulk FET, where the short-channel effects are controlled by doping (channel doping and/or halo doping); and a thin silicon channel leading to tight coupling of the gate potential with the channel potential.

These features provide potential DG FET advantages that include 1) reduced 2D short channel effects leading to a shorter allowable channel length compared to bulk FET; 2) a sharper subthreshold slope (60 mV/dec compared to > 80 mV/dec for bulk FET) which allows for a larger gate overdrive for the same power supply and the same off-current; and 3) better carrier transport as the channel doping is reduced (in principle, the channel can be undoped). Reduction of channel doping also relieves a key scaling limitation due to the drain-to-body band-to-band tunneling leakage current. A further potential advantage is more current drive (or gate capacitance) per device area; however, this density improvement depends critically on the specific fabrication methods employed and is not intrinsic to the device structure.

The most common mode of operation of the DG FET is to switch the two gates simultaneously. Another use of the two gates is to switch only one gate and apply a bias to the second gate to dynamically alter the threshold voltage of the FET [41]. In this mode of operation, called "ground plane" (GP) or back gate (BG), the subthreshold slope is determined by the ratio of the switching gate capacitance and the series combination of the channel capacitance and the non-switching gate capacitance, and is generally worse than the DG FET. A thin gate dielectric at the non-switching gate reduces the voltage required to adjust the threshold voltage and preserves the drain-field-shielding advantage of the double-gate device structure. However, a thinner gate dielectric also means extra capacitance that does not contribute to channel charge for switching. Since the back-gate FET is very similar to a single-gated SOI FET with an adjustable threshold voltage [41].

DG-MOSFETs are claimed to be more immune to short channel effects (SCE) than bulk silicon MOSFETs and even more than single gate fully depleted SOI MOSFETs. This is due to the fact that the two gate electrodes jointly control the carriers, thus screening the

drain field from the channel. This latter feature would permit a much greater scaling down of these devices than ever imagined in conventional MOSFETs.

2.2 Advantages of DG MOSFET over SG MOSFET

2.2.1 Limitation of Scaled SG MOSFET

- **Drain Induced Barrier Lowering (DIBL) (Effect of Reduced Channel Length)**

In devices with long channel lengths, the gate is completely responsible for depleting the semiconductor. In very short channel devices, part of the depletion is accomplished by the drain and source bias. Since less gate voltage is required to deplete the semiconductor, the barrier for electron injection from source to drain decreases. This is known as drain induced barrier lowering (DIBL).

DIBL results in an increase in drain current at a given gate voltage, V_G. Therefore V_t decreases as channel length decreases. Similarly, as drain voltage V_D increases more semiconductor region is depleted by the drain bias, and hence I_d increases and V_t decreases.

- **Carrier Mobility : Velocity Saturation**

The mobility of the carrier reduces at higher electric fields normally encountered in small channel length devices due to velocity saturation effects. As the channel length, L is reduced while the supply voltage is not, the tangential electric field will increase, and the carrier velocity may saturate at $E_C \approx 10^4$ V/cm for electrons. Hence for n-MOSFET with $L < 1$ μm, velocity saturation causes the channel current to reach saturation before

$V_D = V_G - V_t$. $E_C \approx 5 \times 10^4$ V/cm for holes, hence velocity saturation for p-MOSFET will not become important until $L < 0.25$ μm.

- **Sub-threshold Conduction**

When the surface is in weak inversion ($V_G < Vt$), a conduction channel starts to form a low level of current flow between source and drain. As a result, drain leakage current and static power loss increases. Hence circuit stability decreases.

- **Hot Carrier Effect**

Hot carrier effects are among the main concerns when shrinking FET dimensions into the deep sub-micron regime. Reducing the channel length while retaining high power supply levels, known as constant voltage scaling, results in increased electric field strengths in the channel, causing acceleration and heating of the charge carriers. The free carriers passing through the high-field can gain sufficient energy to cause several hot-carrier effects. This can cause many serious problems for the device operation. Some of the manifestations of hot electrons on device operation are breakdown and substrate current caused by impact ionization, creation of interface states, gate current resulting from hot-electron emission across the interface barrier, oxide charges owing to tunneling of charge carriers into oxide states and photocurrents caused by electron-hole recombination with emission of photons. The substrate current resulting from electron-hole pair generation may overload substrate-bias generators, introduce snapback breakdown, cause CMOS latch-up and generate a significant increase in the sub-threshold drain current.

2.2.2 Short Channel Effects

Collectively, threshold voltage roll-off and subthreshold roll-up are commonly known as short-channel effects (SCEs). In consequence of SCEs, the ratio of the drive (ON) current to the leakage (OFF) current is substantially reduced, which imposes severe tradeoffs

between circuit speed and standby power. In addition, SCEs amplify the impact of process variations on CMOS circuits.

In conventional bulk MOSFETs, SCEs are caused by the lateral electric fields from the source to channel and drain to channel. As L decreases, the lateral fields terminate on further into the channel, which essentially steals the charge that would normally be terminated by the gate voltage in a long-channel device. This stealing of charge by the lateral fields effectively lowers the source-to-channel barrier, which controls the conduction of electrons from source to drain. To limit this charge stealing and thus mitigate SCEs, heavy channel doping is exploited in bulk MOSFETs. As the gate length is scaled to 50 nm and below, the required channel doping concentration is expected to be on the order of 10^{18} cm^{-3} and above. These extremely high doping levels, however lead to,

a) Severe degradation of the carrier mobility as the impurity scattering becomes dominant.
b) Severe threshold voltage variations due to random microscopic fluctuations of the dopant atoms.

The DG MOSFET does not require channel doping for SCE control. Instead, this novel device uses a second gate and a fully depleted silicon film as the channel to enhance the electrostatic control of the gates over the channel, which effectively suppresses the impact of the source/drain. The thin silicon film is undoped or lightly doped (typical doping concentration $N_A \langle$ 10^{18} cm^{-3}) to ensure the full depletion condition. For most effective SCE control, the two gate-oxide layers are equally thin. Use of an identical material for both gates results in a symmetric DG MOSFET.

2.2.3 Concept of Volume Inversion

The outstanding feature of these structures lies in the concept of volume inversion, introduced by Balestra *et al* [42]; if the Si film is thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers, and the operation of this device is similar to the operation of two conventional MOSFETs connected in parallel. However, if the Si thickness is reduced, the whole silicon film is depleted and an important interaction appears between the two potential wells. In such conditions the inversion layer is formed not only at the top and bottom of the silicon slab i.e., near the two silicon–oxide interfaces, but throughout the entire silicon film thickness. It is then said that the device operates in ''volume inversion'' i.e., carriers are no longer confined at one interface, but distributed throughout the entire silicon volume.

It has been reported [22, 29] that volume inversion presents some significant advantages, such as

i. Enhancement of the number of minority carriers.
ii. Increase in carrier mobility and velocity due to reduced influence of scattering associated with oxide and interface charges and surface roughness.
iii. As a consequence of the latter, an increase in drain current and transconductance.
iv. Decrease of low frequency noise.
v. A great reduction in hot-carrier effects.

CHAPTER 3

SIMULATION OF DG MOS STRUCTURES

In this chapter, the 1D simulation study of double gate MOS structure is presented. At first the self consistent system is studied. Then, the use of FEMLAB to solve Schrödinger's and Poisson's equations is discussed. Finally, the theory used for the calculation of device capacitance incorporating the effects of interface trapped charges is presented.

3.1 Self - Consistent Analysis

This self - consistent solution of coupled Schrödinger's and Poisson's equations is the most significant part of the study of a double gate MOS structures. These two equations and how they are solved using FEMLAB is presented in this section.

3.1.1 Schrödinger Equation

The Schrödinger equation is solved within the effective mass approximation. Within this approximation, Schrödinger's equation for a wave function ψ_{0ij} can be written as,

$$-[\frac{1}{2}\hbar^2\nabla m^{*-1}\nabla + qV(z)]\psi_{0ij} = \mathrm{E}'_{ij}\psi_{0ij} \qquad (3.1)$$

where, m^{*-1} represents the effective mass tensor, $V(z)$ the electrostatic potential, q the magnitude of the electron charge and E'_{ij} is the energy. z is reckoned positive into the semiconductor. Following [43], the electronic wavefunction ψ_{0ij} for the jth subband in

the ith valley can be expressed in terms of Bloch waves traveling parallel to the interface, constrained by an envelope function normal to it, thus.

$$\psi_{0ij}(x,y,z) = \psi_{ij}(z)e^{i\theta z}e^{ik_x x + ik_y y} \quad (3.2)$$

Here, k_x and k_y represent the transverse components of the wave vector k of the electron measured relative to the band edge. θ depends on k_x and k_y. Envelope function $\psi_{ij}(z)$ is the solution of,

$$[-\frac{\hbar^2}{2m_{zi}}\frac{d^2}{dz^2} + qV(z)]\ \psi_{ij}(z) = E_{ij}\psi_{ij}(z) \quad (3.3)$$

where, m_{zi} is the effective mass perpendicular to the interface and E_{ij} is the eigenenergies of the jth subband in the ith valley in the same direction. Each eigenvalue E_{ij} found from the solution of Eq. (3.3) is the bottom of a continuum of levels called a subband, with energy levels given by the relationship,

$$E'_{ij} = E_{ij} + \frac{\hbar^2 k_x^2}{2m_x} + \frac{\hbar^2 k_y^2}{2m_y} \quad (3.4)$$

here, m_x and m_y are the principle effective masses for motion parallel to the surface. There can be as many as three values of m_z depending on the surface orientation because the conduction band of silicon has six ellipsoidal valleys along the [100] direction of the Brillouin zone. In the effective mass approximation, the valleys are degenerate in pairs. Thus, solution of Eq. (3.3) gives the eigenenergy E_{ij} and the envelope function $\psi_{ij}(z)$.

Within the effective mass approximation, the 3D Schrödinger's equation in a MOS inversion layer may be decoupled into a 1D equation that describes the envelope function in the direction normal to the interface. In order to include the effect of wave function

penetration, an open boundary condition is required to be applied at the silicon – oxide interface of the two gates that should take into account the quasi – bound nature of the inversion layer states [43].

3.1.2 Poisson's Equation

The Poisson's equation that is used to find the potential profile V(z) can be written as,

$$\frac{d^2V(z)}{dz^2} = -\frac{\left[\rho_{depl}(z) - q\sum_{ij} N_{ij}\left|\psi_{ij}(z)\right|^2\right]}{\varepsilon_{si}\varepsilon_0} \tag{3.5}$$

where, ε_{si} is the dielectric constant of the semiconductor, N_{ij} is the carrier concentration in the j th subband in the i th valley.

$\rho_{depl}(z)$ is the charge density in the depletion layer, which can be defined as,

$$\begin{aligned} \rho_{depl}(z) &= -q(N_A - N_D), \qquad 0 < z < t_{si} \\ &= 0 \qquad , \qquad z \le 0 \text{ and } z \ge t_{si} \end{aligned} \tag{3.6}$$

here, t_{si} is the silicon body thickness. Since, the body thickness is less than 50 nm, the MOS structure can be considered to be fully depleted.

Since a fraction of inversion charge resides within the gate oxide due to wave function penetration, Poisson's equation should be solved for both the oxide and semiconductor regions. Considering wave function penetration, Poisson's equation can be represented as,

$$\frac{d^2V(z)}{dz^2} = -\frac{\rho_{inv}(z)}{\varepsilon_0\varepsilon_{ox}}, \qquad -T_{ox} < z < 0 \text{ and } t_{si} < z < (t_{si} + T_{ox})$$

$$= -\frac{[\rho_{depl}(z) + \rho_{inv}(z)]}{\varepsilon_0\varepsilon_{si}}, \qquad 0 < z < t_{si} \qquad (3.7)$$

where,

$$\rho_{inv}(z) = -q\sum_{ij} N_{ij}\left|\psi_{ij}(z)\right|^2 \qquad (3.8)$$

and $\rho_{depl}(z)$ is defined by Eq. (3.6). When $\left|\psi_{ij}(z)\right|^2$ is used to define $\rho_{inv}(z)$ in Eq. (3.8), effects of shift of inversion charges on the solution of Poisson's equation are also included.

The boundary conditions required to solve Eq. (3.7) are that, value of dV/dz at the gate metal – oxide interface (z = $-T_{ox}$ and z = $t_{si} + T_{ox}$) should be $-F_{ox}$, where

$$F_{ox} = \frac{q(N_{inv} + N_{depl})}{\varepsilon_0\varepsilon_{ox}} \qquad (3.9)$$

here,

$$N_{inv} = \sum_{ij} N_{ij} \quad \text{and}$$

$$N_{depl} = z_d(N_A - N_D) \qquad (3.10)$$

Where, N_{inv} and N_{depl} are the total inversion carrier concentration and depletion carrier concentration respectively.

Eq. (3.10) assumes that the wave function tail in the gate oxide region has decayed to an insignificant value at z = $-T_{ox}$ and z = $t_{si} + T_{ox}$. Another relationship necessary to relate oxide field F_{ox} to silicon field F_{si} is that at z = 0 and at z = t_{si}, $\varepsilon_{ox}F_{ox} = \varepsilon_{si}F_{si}$.

3.2 Self Consistent Solution using FEMLAB

With the advancement of semiconductor technology, device dimensions are entering into the nanoscale regime; quantum mechanical effects are playing a growing role in device operations and performance. So, semi-classical models are no longer valid and quantum mechanical modeling is inevitable. Although the quantum corrections improve the classical data, these approaches are unable to model or predict all quantum mechanical effects. As described in the previous section, in a fully quantum mechanical model the coupled Schrödinger's and Poisson's equations are solved self consistently. The Schrödinger's equation is solved under the effective mass approximation. The boundary condition for solving the Schrödinger's and Poisson's equations is also a critical issue. To calculate quantum mechanical charge distribution in MOS devices incorporating wave function penetration effects within the oxide layer of MOS devices, an open boundary condition is a must for the solution of Schrödinger's equation [43]. In the absence of suitable boundary conditions, zero penetration of wave function into gate oxide is assumed in the simulation of even deep submicron MOSFETs. While an open boundary condition can be neglected in devices with thick oxide layers, its negligence in deep submicron MOSFETs cannot be justified.

In this section, the solution procedure is portrayed for a dual gate n-MOS structure shown in Fig. 2.1 in the inversion region. FEMLAB with MATLAB has been used as the Partial Differential Equation (PDE) solver (suitable for linear or nearly linear problems), for the self consistent solution.

The classical PDEs coefficient form in multiphysics mode is used for the solution of Poisson's and Schrödinger's equation.

Poisson's equation in coefficient form is given in FEMLAB as.

$$-\nabla.(c\nabla u) = f \tag{3.11}$$

Where,

c = permittivity of the sub domain, $\varepsilon_0 \varepsilon$

u = Electrostatic potential, $v(z)$

f = Charge density termed as source term in FEMLAB, $q[p(z) - n(z) + N_D - N_A]$

z = the direction along the depth of the MOS structure

Using relevant parameters of MOS structures, Eq. (3.11) can be written as,

$$-\varepsilon_0 \varepsilon \frac{d^2 v(z)}{dz^2} = q[p(z) - n(z) + N_D - N_A] \tag{3.12}$$

Where, $n(z)$, $p(z)$ are the electron, hole concentration and N_D, N_A are the ionized donor, acceptor concentration respectively. ε is the relative dielectric constant of the material and ε_0 is the permittivity of free space.

The electron concentration $n(z)$ is obtained for n-MOS structure according to the following expression.

$$n(z) = \sum_{ij} N_{ij} |\psi_{ij}(z)|^2 \tag{3.13}$$

Where,

$$N_{ij} = \frac{n_{vi} m_{di} kT}{\pi \hbar^2} \ln\left[1 + \exp(\frac{E_F - E_{ij}}{kT})\right] \tag{3.14}$$

$$E_F = E_{Fbulk} + V_G \tag{3.15}$$

Where, n_{vi} is the valley degeneracy and m_{di} is the density–of–states effective mass of the ith valley, given by $m_{di} = \sqrt{m_{xi} m_{yi}}$. E_F is the Fermi energy. Where N_{ij} is the carrier concentration in the jth subband of the ith valley, n_{vi} is the ith valley degeneracy and

m_{di} is the density–of–states effective mass of the ith valley, given by $m_{di} = \sqrt{m_{xi}m_{yi}}$. E_F *is* the Fermi energy. E_{ij} and ψ_{ij} are the eigenvalue and the eigenfunction of an electron in the jth energy level of the ith valley, which are obtained as a solution of the one dimensional Schrödinger equation.

Schrödinger equation in coefficient form is defined in FEMLAB as.

$$-\nabla.(c\nabla u) + au = \lambda u \tag{3.16}$$

Where,

$c = \dfrac{\hbar^2}{2m^*}$, m^* = effective mass for the subdomain

a = Electrostatic potential, $v(z)$

λ = eigen energies, E_{ij}

u =eigenfunction, ψ_{ij}.

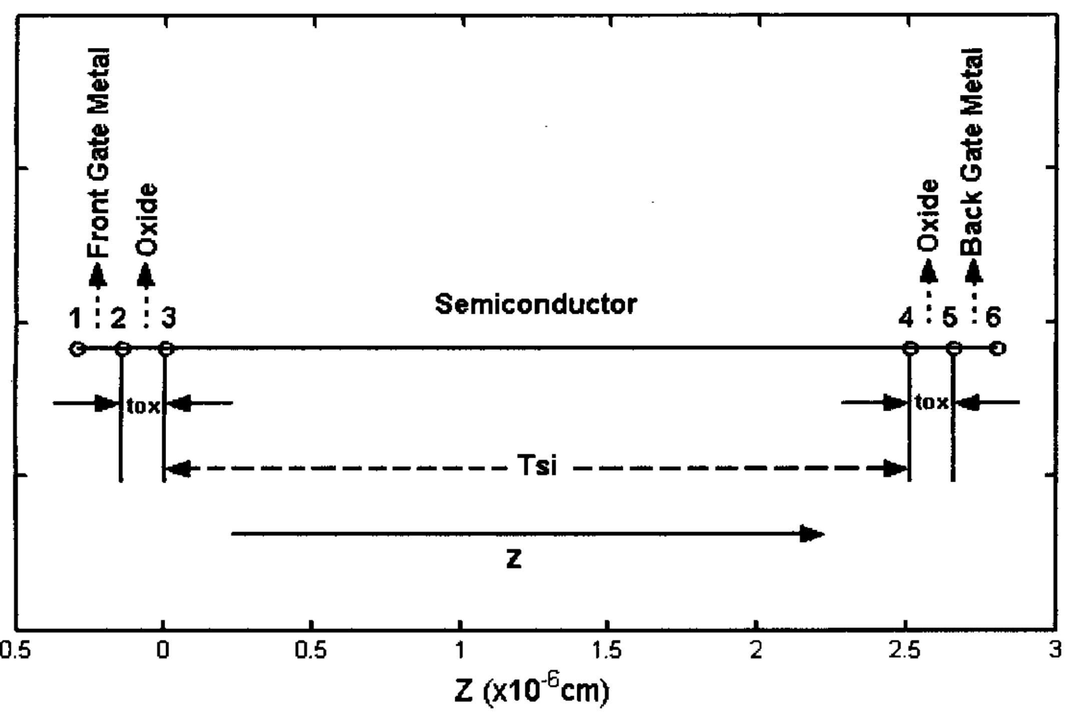


Fig.3.1. 1D geometry of Double Gate MOS structure

Using relevant parameters of effective mass Schrödinger's equation for one dimensional MOS structure quantum well Eq. (3.16) can be written as,

$$[-\frac{\hbar^2}{2m^*}\frac{d^2}{dz^2}+v(z)]\psi_{ij}(z)=E_{ij}\,\psi_{ij}(z) \tag{3.17}$$

At first, the device geometry (the fully depleted double gate structure) is defined as shown in Fig.3.1 in FEMLAB and the trial potential as presented in Fig.3.2 is obtained by solving Eq. (3.11) using the full depletion approximation assuming zero mobile charge density i.e. $n(z)=0$ in Eq. (3.12) with appropriate boundary condition at each interface through FEMLAB linear PDE solver.

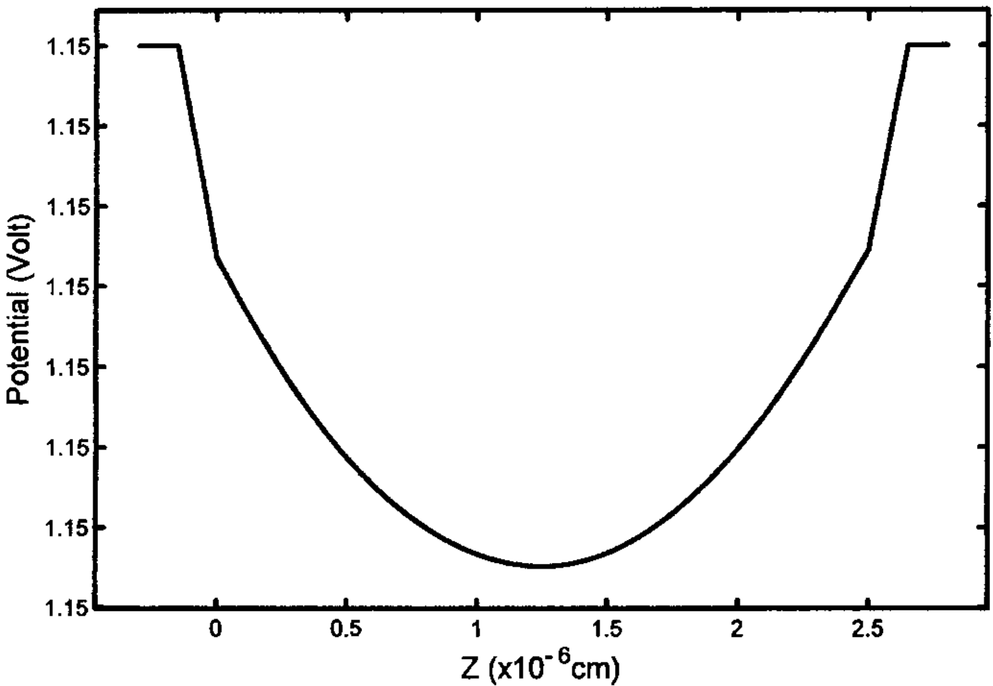


Fig.3.2. Trial Potential from full depletion approximation

For the solution of Poisson's equation, Dirichlet boundary condition (i.e. fixed value of voltage) is used at boundary points 1, 2, 5, 6 and Neumann boundary condition (i.e. continuous electric flux, εE) is used at interfaces 3 and 4.

For the solution of Poisson's equation, a discontinuous electric field boundary condition is required. For achieving this condition, Neumann boundary condition (needed for open boundary condition to consider penetration effect) is applied at all the points.

The charge density profile $n(z)$ is determined from Eq.(3.13) by solving Eq.(3.16) using FEMLAB eigen value solver with Neumann boundary condition, which is shown in Fig.3.3.

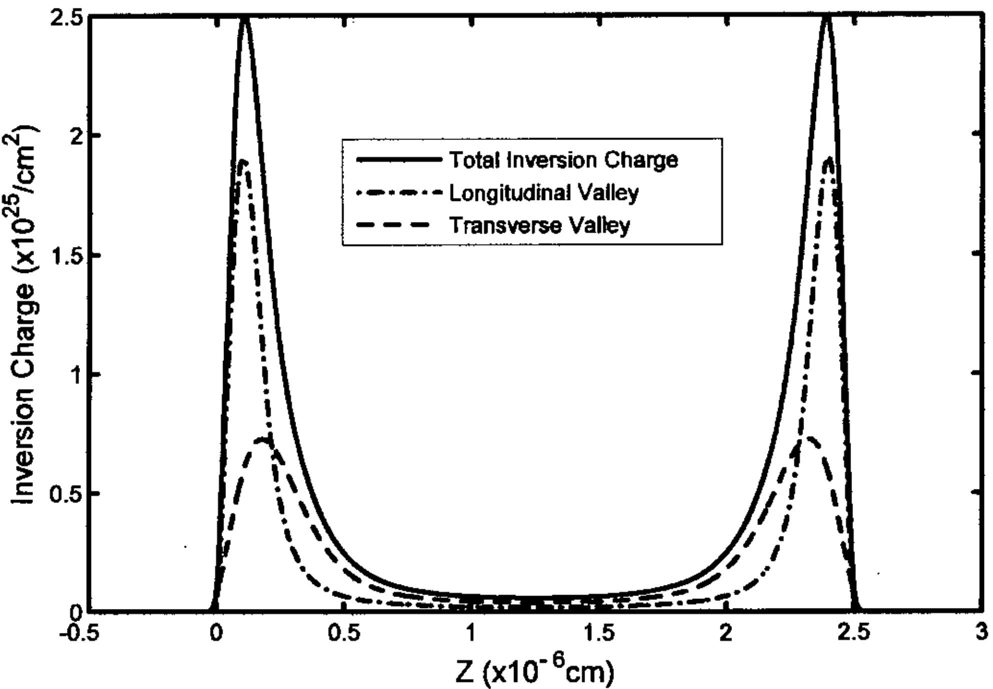


Fig.3.3. Inversion charge density as a function of depth, z

This charge density profile is added to the source term of Poisson's equation and then Eq.(3.11) and Eq.(3.16) are solved iteratively until the given convergence criteria [for successive iteration, change in electrostatic potential at any node point should be less than 10^{-7} volts] are fulfilled. Hence we get the actual band profile presented in Fig.3.4 and electrostatic potential incorporating wave function penetration as demonstrated in Fig.3.5. If the solution is to run without penetration effect, we just increase the barrier height in

the oxide region to a very large value (e.g. 100 eV) that can be considered as an infinite potential barrier.

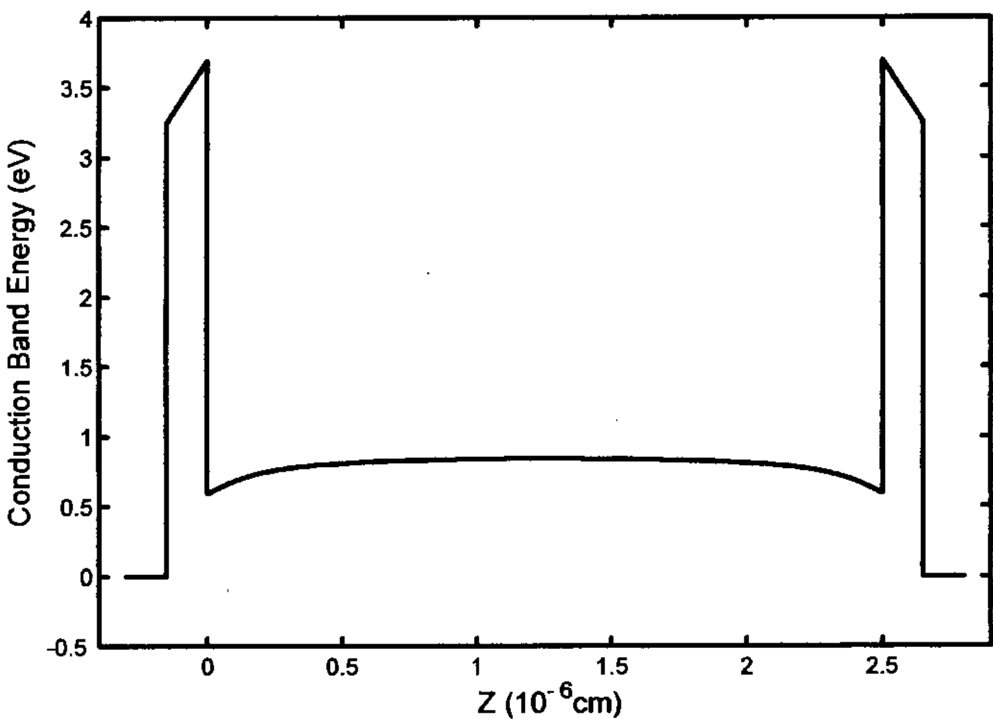


Fig.3.4. Actual Energy band diagram for the simulated structure

For the numerical convergence a weighing factor is used which is shown in Eq. 3.18. The weighting factor should be greater than 0.9. With the increase of weighting factor the assurance of convergence increases but the simulation becomes slower and more iteration is needed. Throughout this thesis, 0.95 is used as value of 'delta', which is the weighting factor, used in Eq. 3.18.

$$V_{prof} = V_{old} \times \text{delta} + V_{new} \times (1\text{-delta}) \quad (3.18)$$

Where, V_{prof} is the new interpolated profile

V_{old} is the previous profile

V_{new} is the new calculated profile

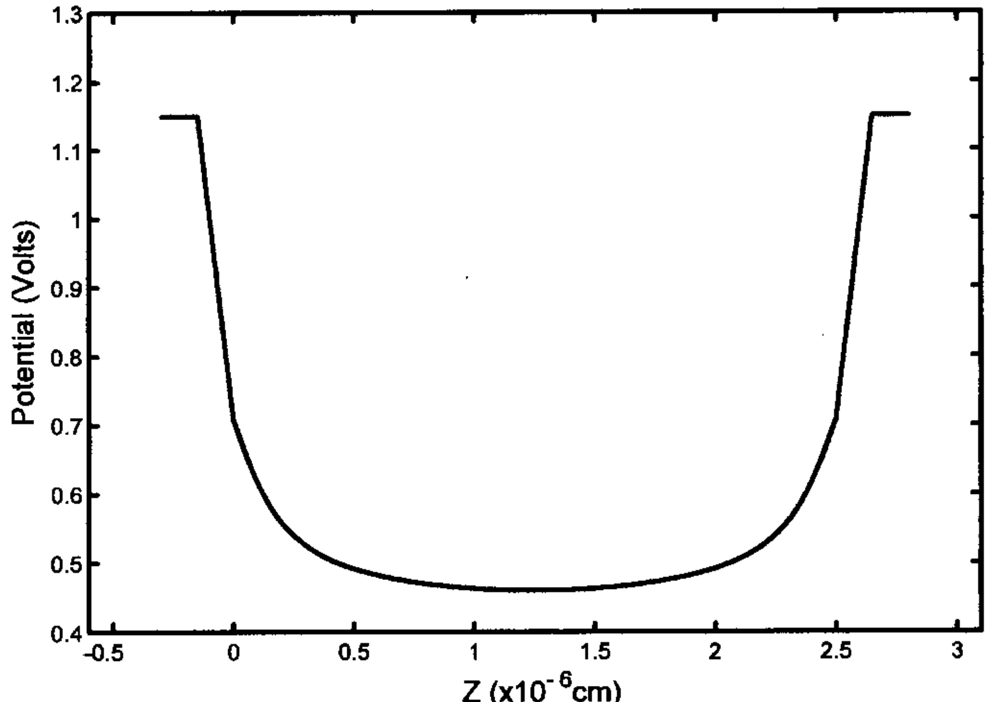


Fig.3.5. Actual Potential profile for the simulated structure

All the simulation results presented in this chapter has been generated for,

$N_A = N_D = n_i = 1.5 \times 10^{10}\ /cm^3$, $T_{ox}=1.5$ nm, $T_{si} = 20$ nm and $V_G = 1.15$ volts.

Detailed flowchart of the self-consistent solver is given in Appendix A.

3.3 Interface States

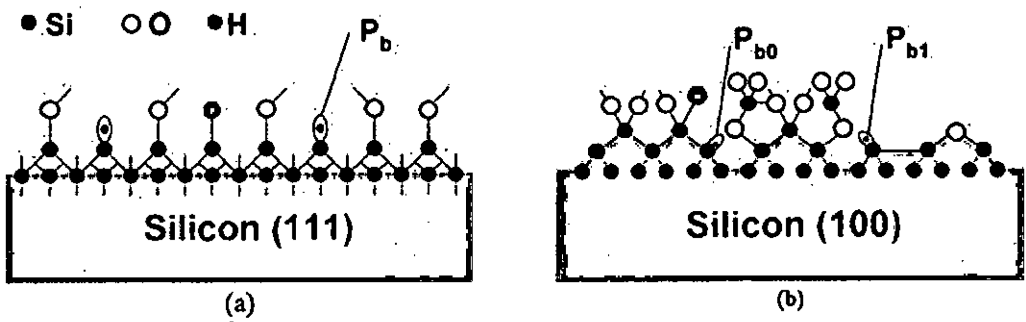


Fig.3.6. Structural model of the (a) (111) Si surface and (b) (100) Si surface

Silicon is tetrahedrally bonded with each Si atom bonded to four Si atoms in the wafer bulk. When the Si is oxidized, the bonding configuration at the surface is as shown in Fig.3.6 (a) and 3 (b) with most Si atoms bonded to oxygen at the surface. Some Si atoms bond to hydrogen. An interface trapped charge, often called interface trap, is an interface trivalent Si atom with an unsaturated (unpaired) valence electron at the SiO_2 /Si interface. It is usually denoted by

$Si_3 \equiv Si\bullet$

The ≡ represents three complete bonds to other Si atoms (the Si_3) and the • represents the fourth, unpaired electron in a dangling orbital (dangling bond). Interface traps are also known as P_b centers [44]. Interface traps are designated as D_{it} ($cm^{-2}\ eV^{-1}$), Q_{it} (C/cm^2), and N_{it} (cm^{-2}).

On (111)-oriented wafers, the P_b center is a $Si_3 \equiv Si\bullet$ center, situated at the Si/SiO_2 interface with its unbonded central-atom orbital perpendicular to the interface and aimed into a vacancy in the oxide immediately above it, as shown in Fig.3.6 (a). On (100) Si, the four tetrahedral Si-Si directions intersect the interface plane at the same angle. Two defects, named P_{b1} and P_{b0} , have been detected by electron spin resonance (ESR), shown in Fig.3.6 (b). The P_{b1} center was originally thought to be a Si atom backbonded to two substrate Si atoms, with the third saturated bond attached to an oxygen atom, designated as $Si_2O \equiv Si\bullet$,[44] This identification was found to be incorrect, as the calculated energy

levels for this defect do not agree with experiment [45]. A recent calculation suggests the P_{b1} center to be an asymmetrically oxidized dimer, with no first neighbor oxygen atoms. [46] By 1999, it was unambiguously established that both P_{b0} and P_{b1} are chemically identical to the P_b center. However, there is a charge state difference between these two centers indicating P_{b0} is electrically active, while some authors believe the P_{b1} to be electrically inactive.[47] The two different effects are the result of strain relief in (100) silicon. The defects result from the naturally occurring mismatch induced stress in the SiO_2 /Si layer during oxide growth.

3.3.1 Effects of Interface States

P_{b0} centers result when strain relaxation occurs with a defect residing at (111) microfacets at the Si/SiO_2 interface, while Pb1 centers result when strain relaxation occurs with a defect at (100) Si/SiO_2 transition regions. Based on these results and the fact that P_{b1} centers are believed to be electrically inactive, defects resulting from P_{b0} centers are considered the precursor in creating interface traps in (100) silicon. It is worth mentioning that recent work indicates P_{b1} centers to be electrically inactive at low temperatures (T=77K). However, at room temperature and higher these defects contribute to the electrical activity of total interface traps. Recent ESR measurements show the P_{b1} center to be electrically active with two distinct, narrow peaks close to midgap in the silicon band gap. However, P_{b1} centers are typically generated at densities considerably lower than P_{b0} centers, making them potentially less important. Interface traps are electrically active defects with an energy distribution throughout the Si band gap. They act as generation/recombination centers and contribute to leakage current, low-frequency noise, and reduced mobility, drain current, and transconductance. Since electrons or holes occupy interface traps, they also contribute to threshold voltage shifts, given by

$$\Delta V_T = -\frac{\Delta Q_{it}(\phi_S)}{C_{ox}}, \tag{3.19}$$

where Φ_s is the surface potential and Q_{it} is the interface trapped charge on any one surface. The surface potential dependence of the occupancy of interface traps is illustrated in Fig.3.7.

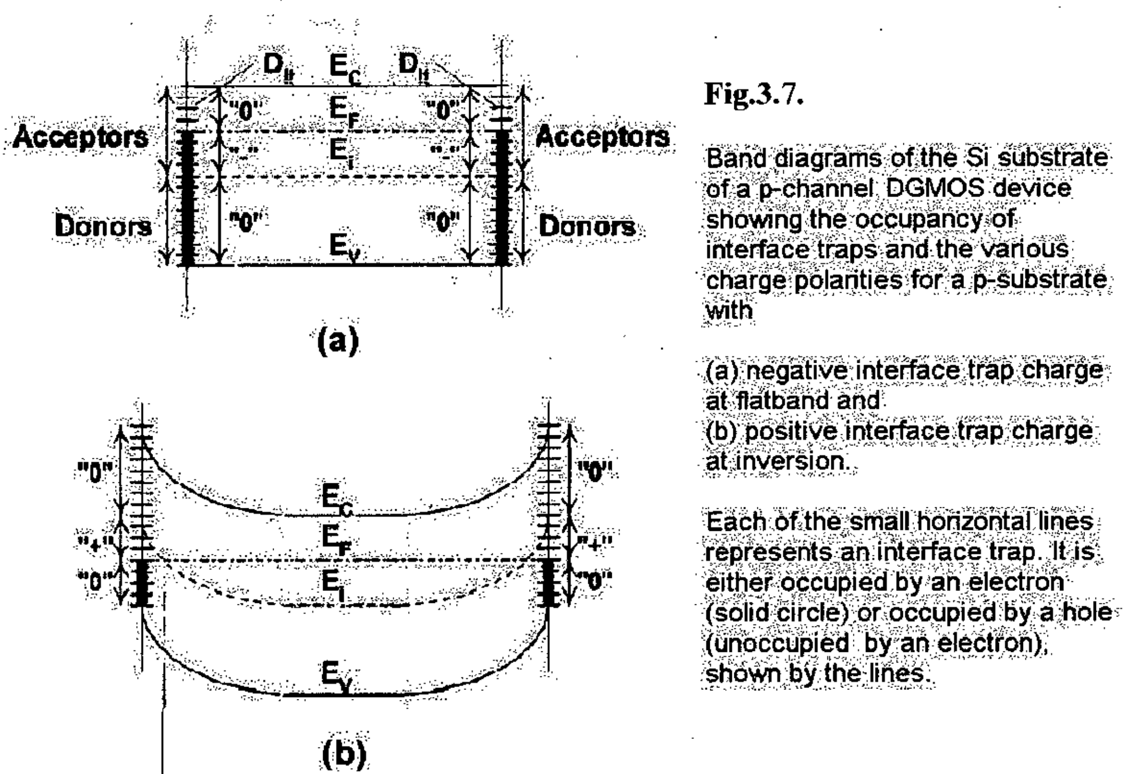


Fig.3.7.

Band diagrams of the Si substrate of a p-channel DGMOS device showing the occupancy of interface traps and the various charge polarities for a p-substrate with

(a) negative interface trap charge at flatband and
(b) positive interface trap charge at inversion.

Each of the small horizontal lines represents an interface trap. It is either occupied by an electron (solid circle) or occupied by a hole (unoccupied by an electron), shown by the lines.

Interface traps at the SiO_2 / Si interface are acceptor-like in the upper half and donor-like in the lower half of the band gap.[48] This is in contrast to doping atoms, which are donors in the upper half and acceptors in the lower half of the band gap. Hence, as shown in Fig.3.7 (a), at flatband, where electrons occupy states below the Fermi energy, the states in the lower half of the band gap are neutral (designated by "0"), being occupied donor states. Those between mid gap and the Fermi energy are negatively charged (designated by "–"), being occupied acceptor states and those above E_F are neutral (unoccupied acceptors). For an inverted p-channel DGMOSFET, shown in Fig.3.7 (b), the fraction of interface traps between mid gap and the Fermi level is now unoccupied donors, leading to positively charged interface traps (designated by "+"). Hence interface traps in p-channel devices in inversion are positively charged, leading to negative threshold voltage shifts. Interface traps, being acceptors in the upper half of the

band gap and donors in the lower half affect V_T shifts in n-channel and p-channel DGMOSFETs differently. Fig.3.8 and Fig.3.9 shows an n channel and a p channel DGMOSFET respectively.

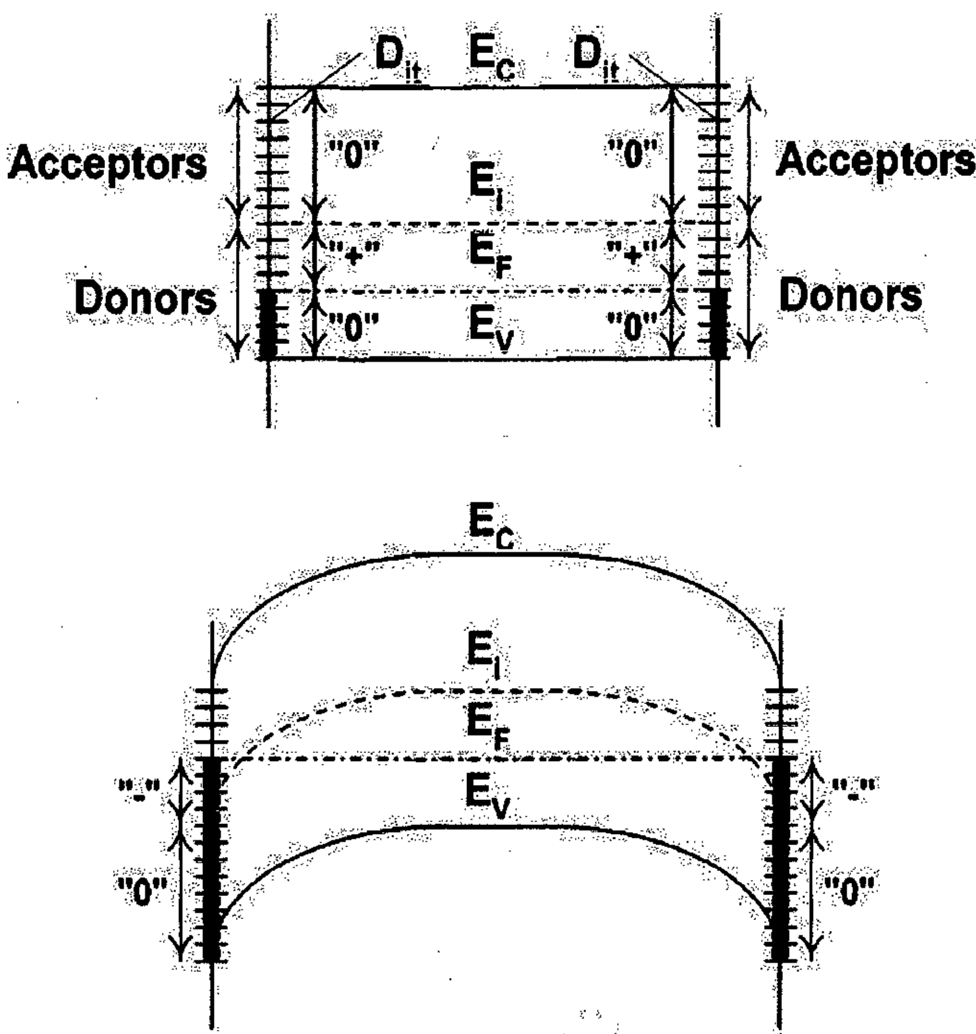
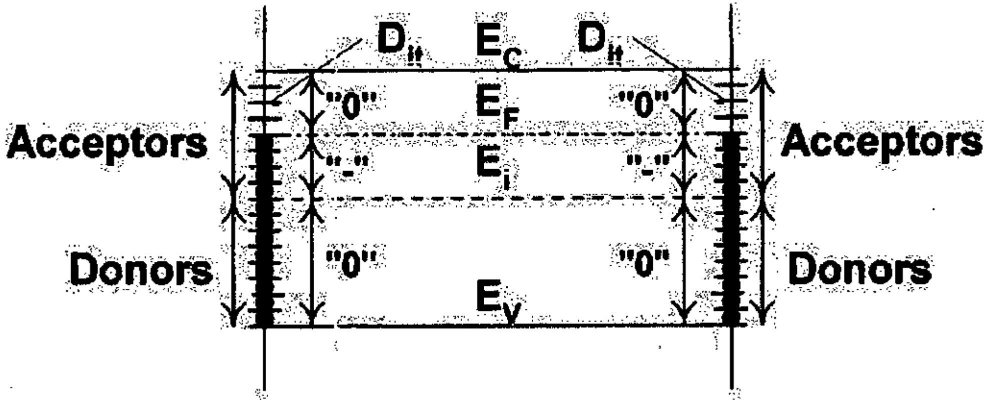


Fig.3.8. p substrate of DG nMOS with positive interface trap charge at flatband and negative interface trap charge at inversion

At flatband, the n channel has positive and the p channel has negative interface trap charge. At inversion, $\phi_S = |2\phi_F|$, the n channel has negative and the p channel has positive interface trap charge. Negative bias stress generates donor states in the lower half of the band gap.



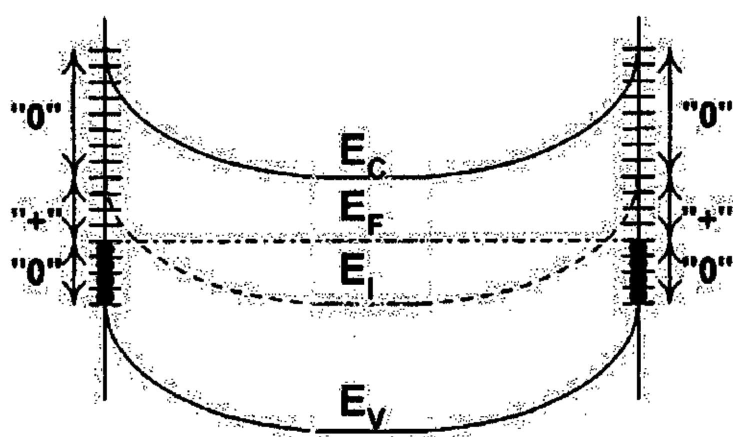


Fig.3.9. n substrate of DG pMOS with negative interface trap charge at flatband and positive interface trap charge at inversion

Interface trap charge densities of state-of-the-art devices are in the range of 10^{11} cm^{-2} or lower. For a DGMOSFET with a 0.1 μm x 1.0 μm gate, i.e., $A=10^{-9}$ cm^2, and $N_{it}=10^{11}$ cm^{-2}, there are only 100 interface traps at each SiO_2 / Si interface under the gate. 100 charges lead to a threshold voltage shift of –

$$\Delta V_T = -\frac{Q_{it}}{C_{ox}}$$

$$= -\frac{100q}{\epsilon_{ox}\epsilon_0 A} t_{ox}$$

$$= -\frac{100 \times 1.6 \times 10^{-19}}{3.45 \times 10^{-13} \times 10^{-9}} t_{ox}$$

$$= -4.6 \times 10^{4} t_{ox}$$

For t_{ox}=1.5 nm, this gives ΔV_T=–69 mV. Device failure is sometimes defined as ΔV_T = –49 mV [38].

CHAPTER 4

RESULTS AND DISCUSSION

In this chapter, the results from the self-consistent solution of Double Gate MOS structures considering wavefunction penetration effect are presented. The Capacitance-Voltage characteristics are investigated with and without incorporating the effect of interface states. Results are presented for both double gate n-MOSFET and p-MOSFETs considering different surface orientations and varying device dimensions and substrate doping concentrations.

In MOS structures, for the chosen interface that lies in the (100) crystal planes, the effective mass tensor becomes diagonal in the co-ordinate system which has its z-axis perpendicular to the surface pointing into the semiconductor. It is known that silicon has six ellipsoidal constant energy surfaces in the conduction band. The (111) surfaces have only one ladder of subbands with degeneracy 6 in the direction normal to the interface, since all the valleys have the same orientation with respect to the surface. For the (100) surfaces, m_z for electrons can take the value of longitudinal mass m_l, for the two bulk constant energy ellipsoid perpendicular to the surface giving rise to a two-fold degenerate subband ladder and the value of the transverse effective mass m_t, for the four other ellipsoids, giving rise to a fourfold degenerate ladder. The valleys which present the higher effective mass perpendicular to the surface have the lowest kinetic energy and lowest energy levels. Effective mass approximation has been found to be accurate in describing quantum effects of electrons in MOS structures [49]. The values of the different parameters used in the calculation are taken from Ref. [12] and are summarized in Table 4.1

Table 4.1: Effective masses of electrons in different valleys

Surface	**<111>**	**<100>**	
Valleys	m_l	m_l	m_t
Degeneracy, n_v	6	2	4
Normal mass, m_z/m_0	0.258	0.916	0.190
Density of state mass, m_d/m_0	0.358	0.190	0.417

It is known that the energy band structure for hole is non-parabolic. So it is disputed to represent the valence band structure within the effective mass approximation. A first principle formalism has been used to completely describe the valence band structure including the periodic lattice potential [49]. But this technique is very complicated and numerically inefficient. On the other hand, bulk effective mass approximation has been found to be accurate in describing the device capacitance for holes [50]. In this study we also used the bulk effective mass approximation of Refs. [12] [50].

The constant-energy surfaces of the light hole and the heavy hole bands are represented by,

$$E_h = \left(\frac{\hbar^2 k^2}{2m_0}\right)\left[A \mp \left(B^2 + C^2\left(\frac{k_x^2 k_y^2 + k_y^2 k_z^2 + k_z^2 k_x^2}{k^4}\right)\right)^{\frac{1}{2}}\right] \tag{4.1}$$

and is reckoned positive downwards into the valence band. Here + and – corresponds to the light hole and heavy hole bands, respectively. The parameters A, B, C are physical constants which has been determined experimentally in Ref. [51].

For the split-off band holes, the constant energy surfaces are isotropic and centered around Γ (zone center). With the three types of hole bands, we got three energy ladders. In the bulk, the light and heavy hole bands are degenerate at the Γ point (valence band edge), while the third one is separated from the other two by ΔE = 44 meV due to spin-orbit coupling.

The effective mass perpendicular to Si/SiO_2 interface, m_z and density of states effective mass , m_d, at the valence band edge on a (100) surface are reported in Refs. [50] [51]. The values of the effective masses for holes in (100) silicon used in this study are listed in Table 4.2.

Table 4.2: Effective masses of different types of holes

Holes	**m_z/m_0**	**m_d/m_0**
Heavy Hole	0.29	0.433
Light Hole	0.20	0.169
Split-off Hole	0.29	0.433

4.1 n-channel DG MOS Structures

Capacitance-Voltage characteristics of Double Gate MOSFETs are presented in this Sec.. All the results are calculated at room temperature. Values for different parameters of silicon are taken from [12] and Table 4.1. The potential barrier height at silicon-oxide interface is considered to be 3.1 eV. Electron effective mass in oxide is assumed to be $0.5m_0$ with a parabolic dispersion relationship. Aluminium is considered as the gate electrode with a work function equal to 4.1 eV.

4.1.1 n-MOS Device on (100) Silicon (Doped Substrate)

Same voltage is applied to a symmetric DG MOSFET at the two gates having the same work function. At zero gate voltage, the position of the silicon bands is largely determined by the gate work function, because as long as the thin silicon is lightly doped and the depletion charge is negligible, the bands remain essentially flat throughout the thickness of the film. Since there is no contact to the silicon body, the energy levels are referenced to the electron quasi-fermi level or the conduction band of the n+ source-drain.

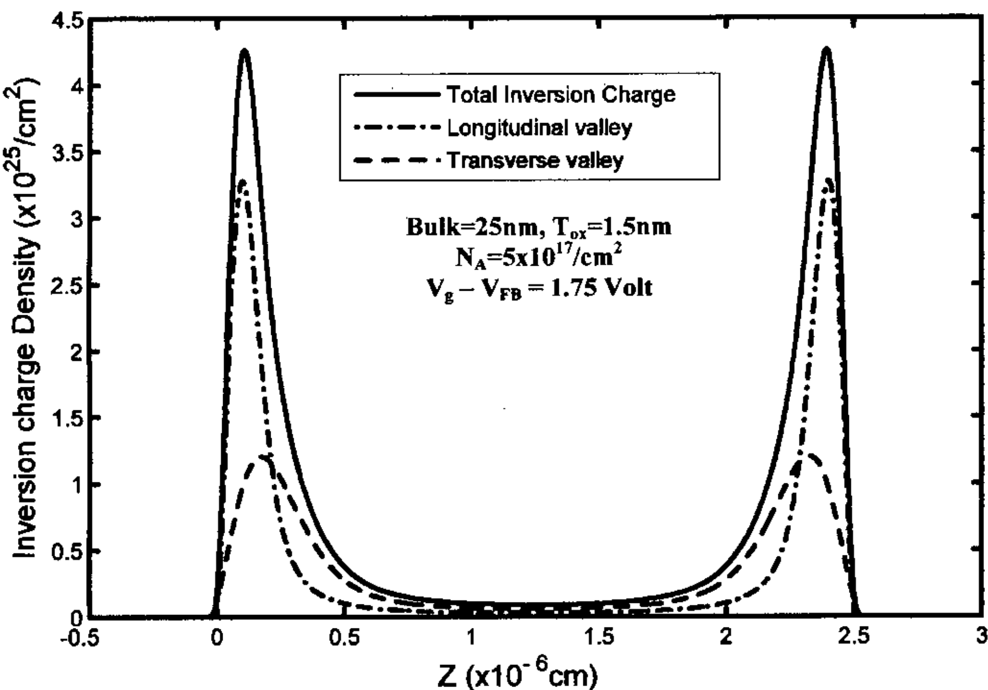


Fig.4.1. Inversion charge density as a function of depth Z

As the gate voltage increases toward the threshold voltage, mobile charge or electron density becomes appreciable when the conduction band of silicon approaches the conduction band of source-drain. Fig.4.1 shows the inversion charge density of an n-channel DGMOSFET with an undoped substrate found by using the 1-D self consistent solver discussed in Sec. 3.1. Such profiles generated for various applied voltages are used to generate the Charge-Voltage dependency profile depicted in Fig.4.2.

Since we know that-

$$C = \frac{\Delta Q}{\Delta V} \tag{4.2}$$

From the Charge-Voltage profile, we can determine the Capacitance-Voltage profile of the device as shown in Fig.4.3.

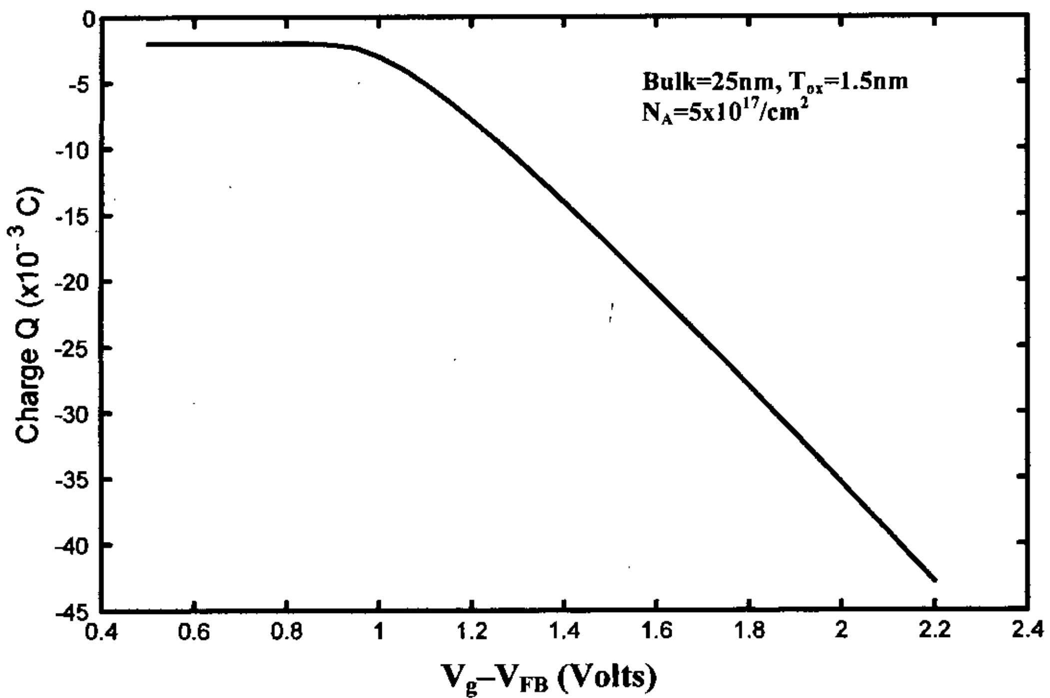


Fig.4.2. Variation of Charge with respect to applied voltage at inversion

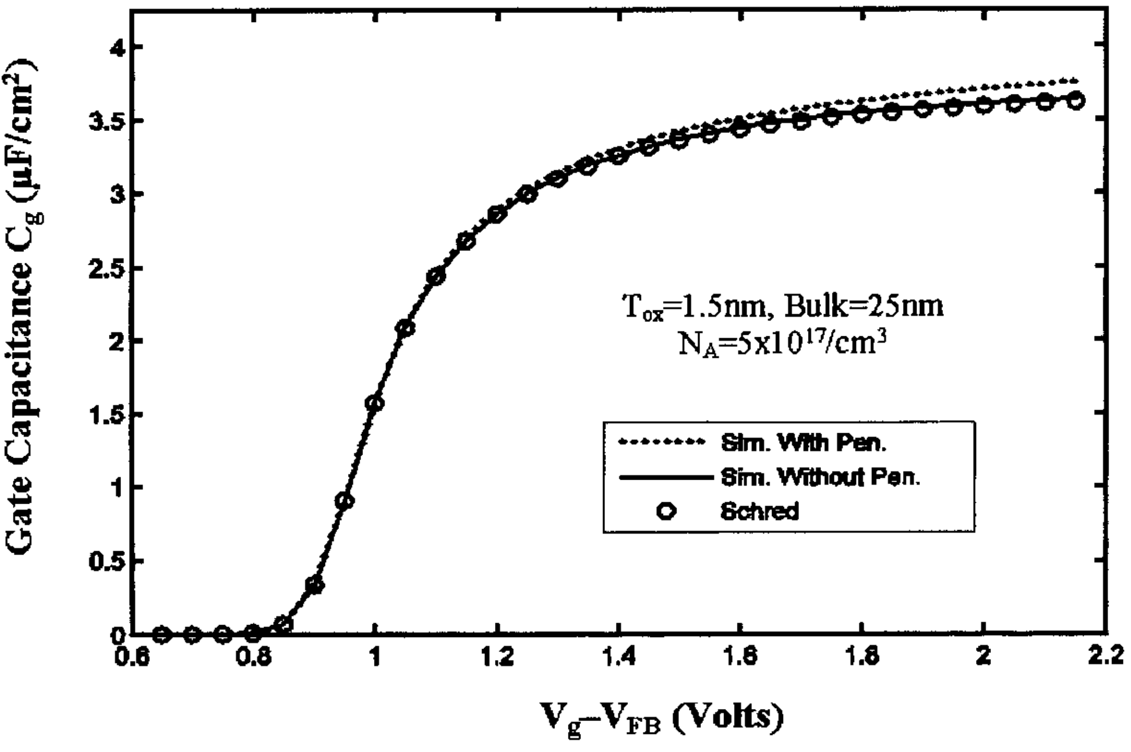


Fig.4.3. C-V Profile of an n-channel DG MOSFET during inversion

Figure 4.3 compares the simulated C-V profile with the simulated C-V profile generated by 'Schred' (A widely recognized numerical solver developed by 'Purdue University' that doesn't consider penetration effect, available at '*www.nanohub.org*'). As our simulated result considers wavefunction penetration, it gives a higher value of capacitance compared to 'Schred'. So, we simulated another C-V profile which doesn't take penetration effect into consideration and it completely matched with the profile found using 'Schred'. This clearly verifies the validity of the developed self-consistent solver. The complete C-V profile for the device is found as shown in Fig.4.4.

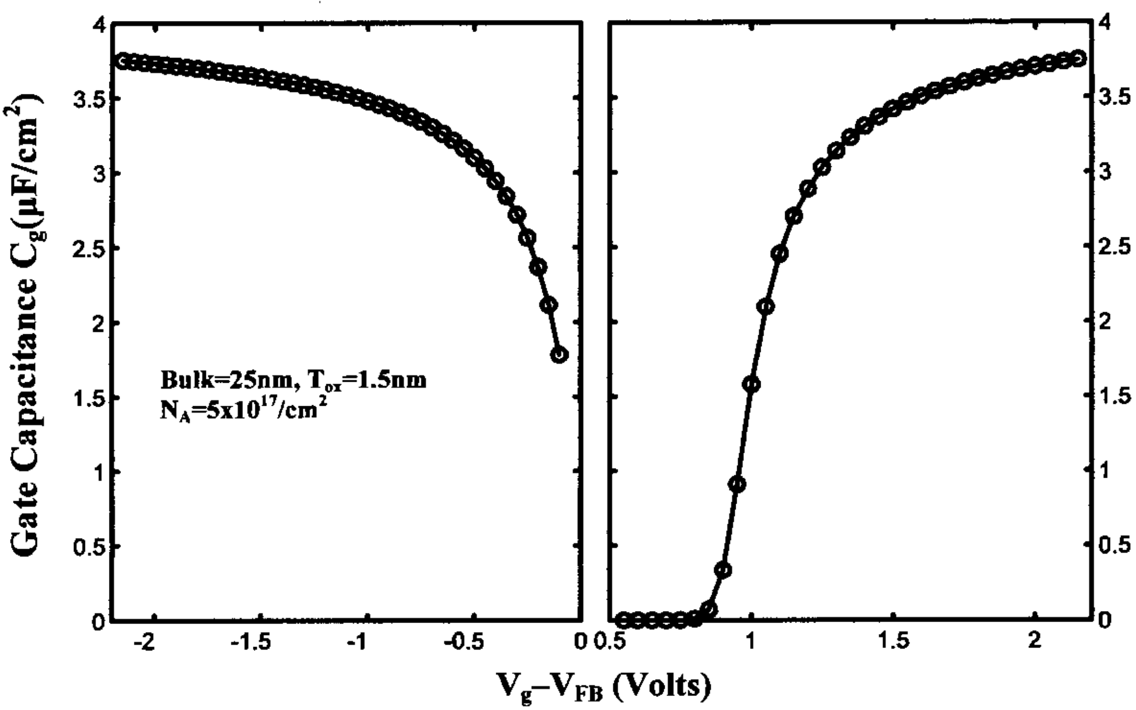


Fig.4.4. C-V Profile of an n-channel DG MOSFET

In order to include the effects of interface trapped charges in Fig.4.4, the variation of the surface potential V_S and (E_F–Ei) shown in Fig.4.5 and Fig.4.6 need to be investigated to calculate interface trapped charge Q_{it} for corresponding interface trap density D_{it}. Then eq. (3.20) can be used to model the effect as a change in device threshold voltage. Similar operation is done in accumulation region also to measure the amount of interface trapped charge Q_{it} for corresponding interface trap density D_{it}.

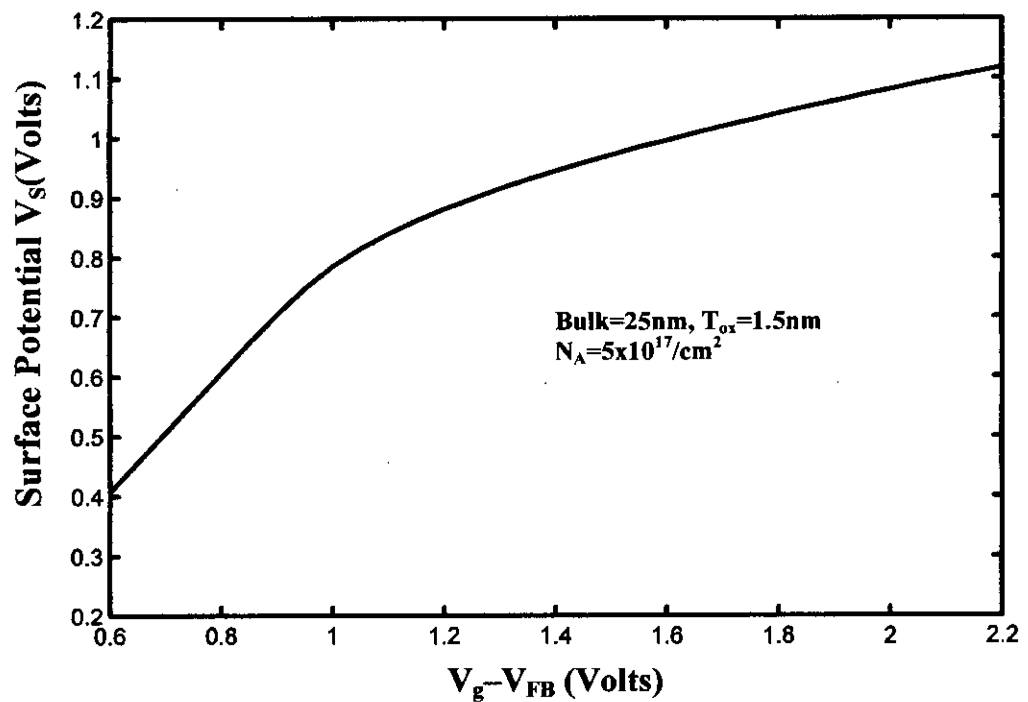


Fig.4.5. Surface Potential Vs Applied Voltage during inversion

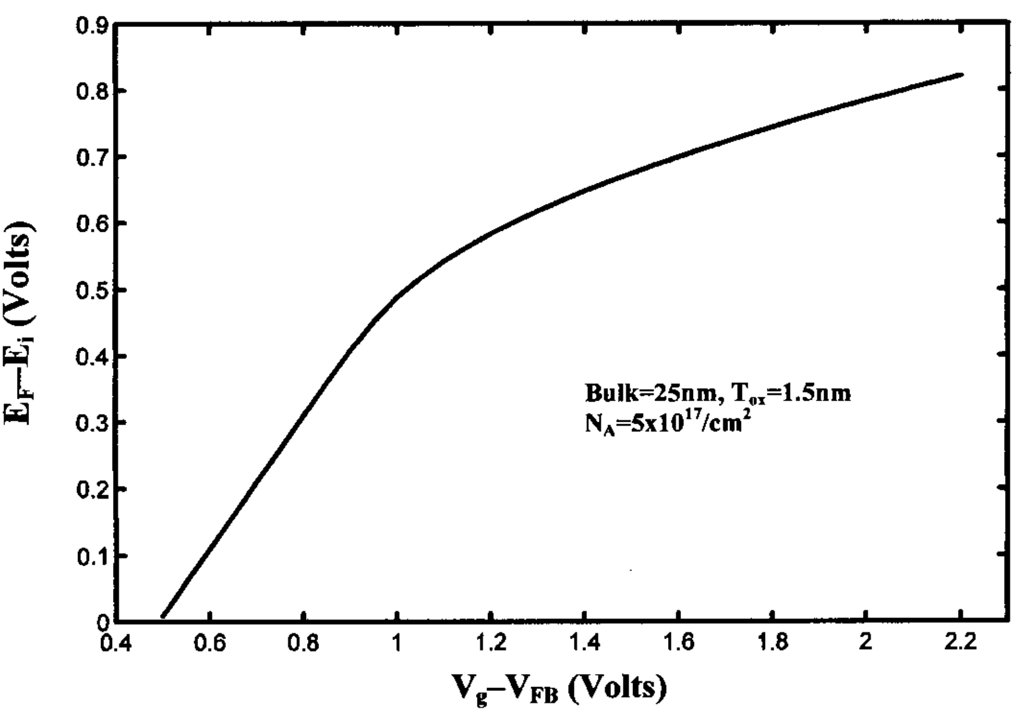


Fig.4.6. (E_F–E_i) Vs Voltage during inversion

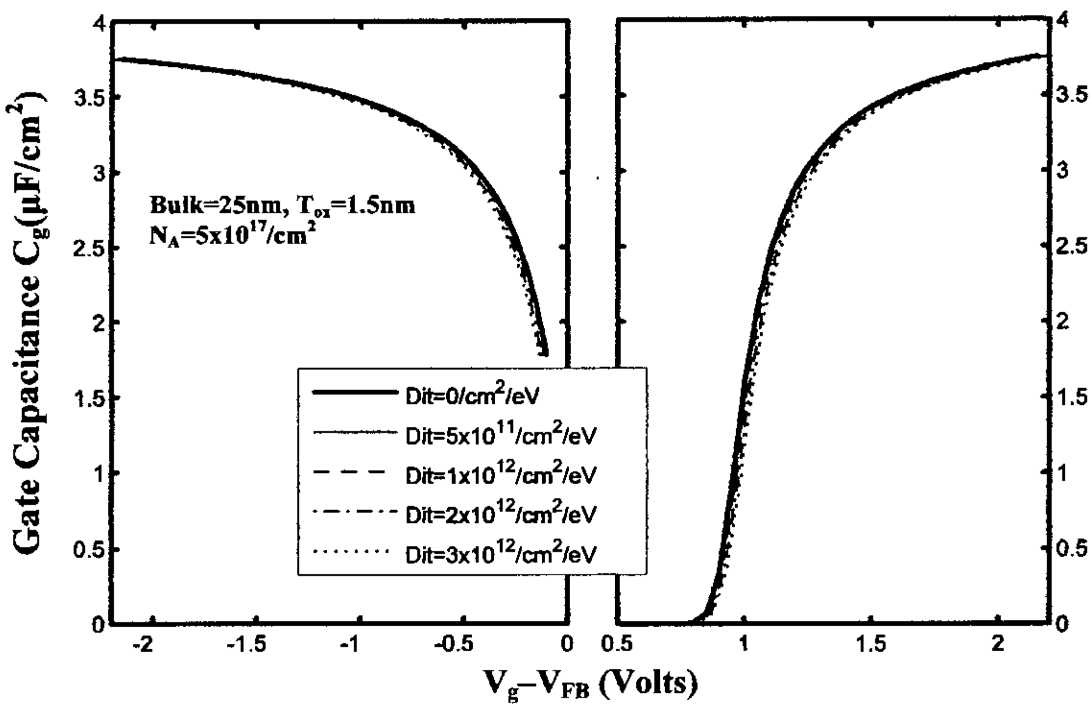


Fig.4.7. HFCV profile of an n-channel DGMOSFET for different Interface State densities

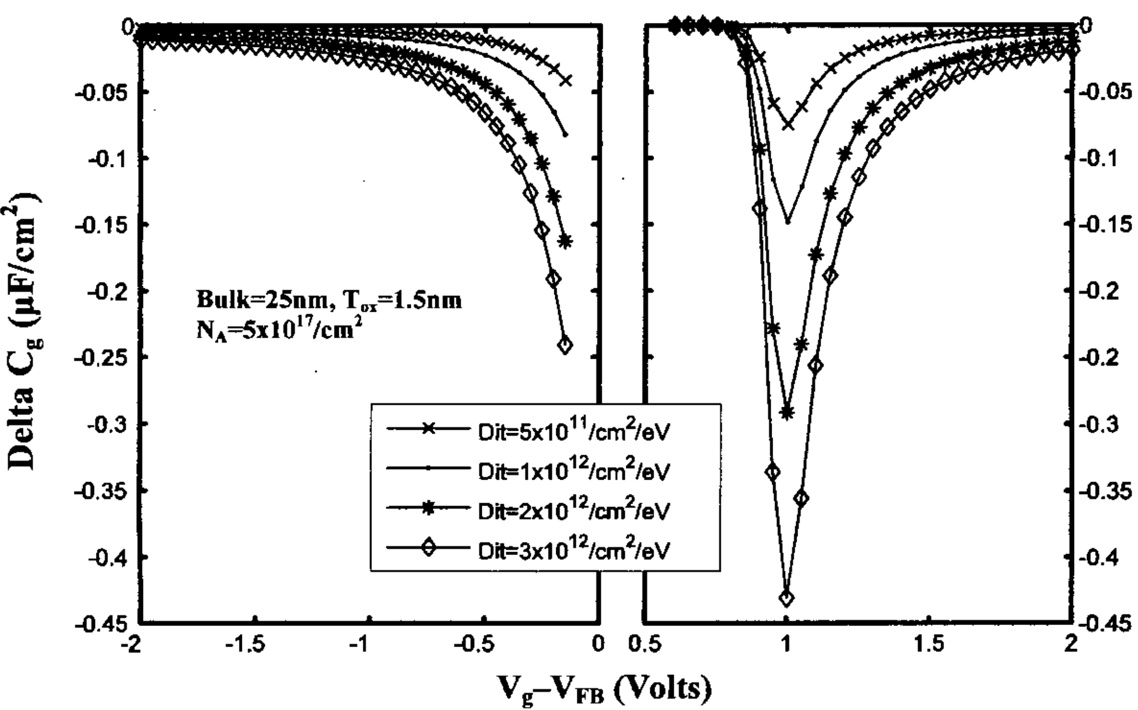


Fig.4.8. Change in HFCV Profile of an n-channel DGMOSFET for different Interface State densities

Fig.4.7 shows the C-V profile of an n-channel DGMOSFET taking the effect of interface states into consideration during High Frequency (HF) operation. During high frequency operation, the interface trapped charge cannot respond to the HF AC voltage superimposed on the DC bias and thus cannot affect the C-V profile significantly. But since it can respond to the DC bias, it affects the threshold voltage of the device as described by Eq. 3.20. It can be observed that the change in C-V profile is very small at high frequency of operation in Fig.4.7. This is even more clearly seen in Fig.4.8. But if we observe the percentage change in Cg as depicted in Fig.4.9, we can see that the alteration in the Capacitance is very significant during weak inversion. During depletion and strong inversion, the change in capacitance is negligible. This is because although the change in capacitance at weak inversion is very small, the device capacitance is also very small during that period. As a result, the percentage change in C-V profile becomes really significant.

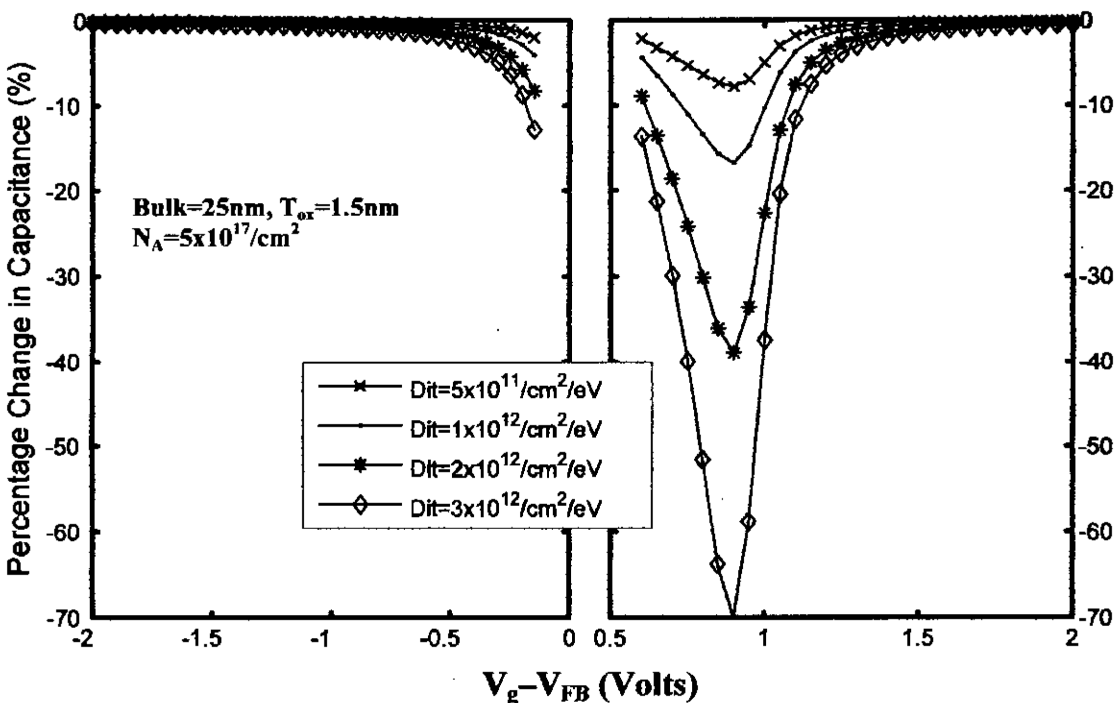


Fig.4.9. Percentage change in HFCV Profile of an n-channel DGMOSFET for different Interface State densities

$$\%Change = \frac{Capacitance(WithInterfaceStates) - Capacitance(WithoutInterfaceStates)}{Capacitance(WithInterfaceStates)} \times 100\% \tag{4.3}$$

At Low Frequency (LF) operations, the interface trapped charges can respond to the low frequency AC bias voltage. Therefore, the effect of interface states in LF operation on device C-V Profile is two-fold. It affects the threshold voltage in same way as it effects during HF operations. It also changes the capacitance of the device by contributing to the total charge of the device. Fig.4.10 shows the C-V profile of an n-channel MOSFET during LF operation. It can be seen that the capacitance is modified more prominently during low frequency operation. Also, the alteration in the value of capacitance is most significant during depletion since, the amount of charge in the device is the least during this period.

Fig.4.11 presents the change in device capacitance due to the effect of interface states at low frequency operation. It can be observed from Fig.4.11 also, that the change in device capacitance is grater during low frequency operation, especially during depletion mode.

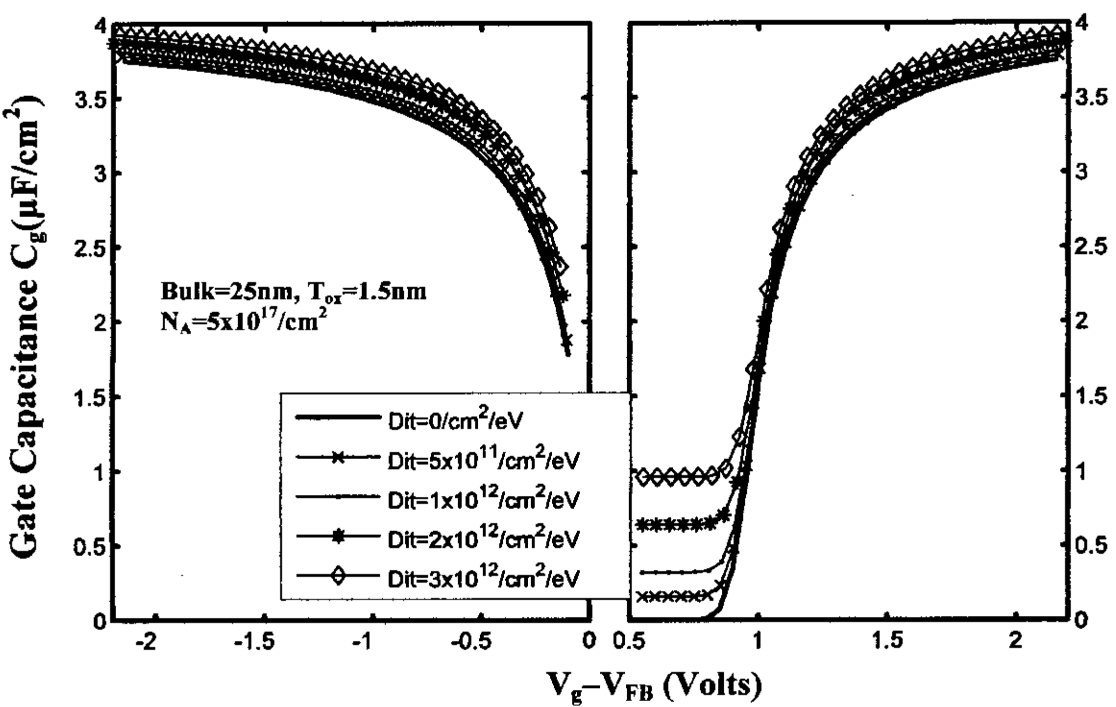


Fig.4.10. LFCV profile of an n-channel DGMOSFET for different Interface State densities

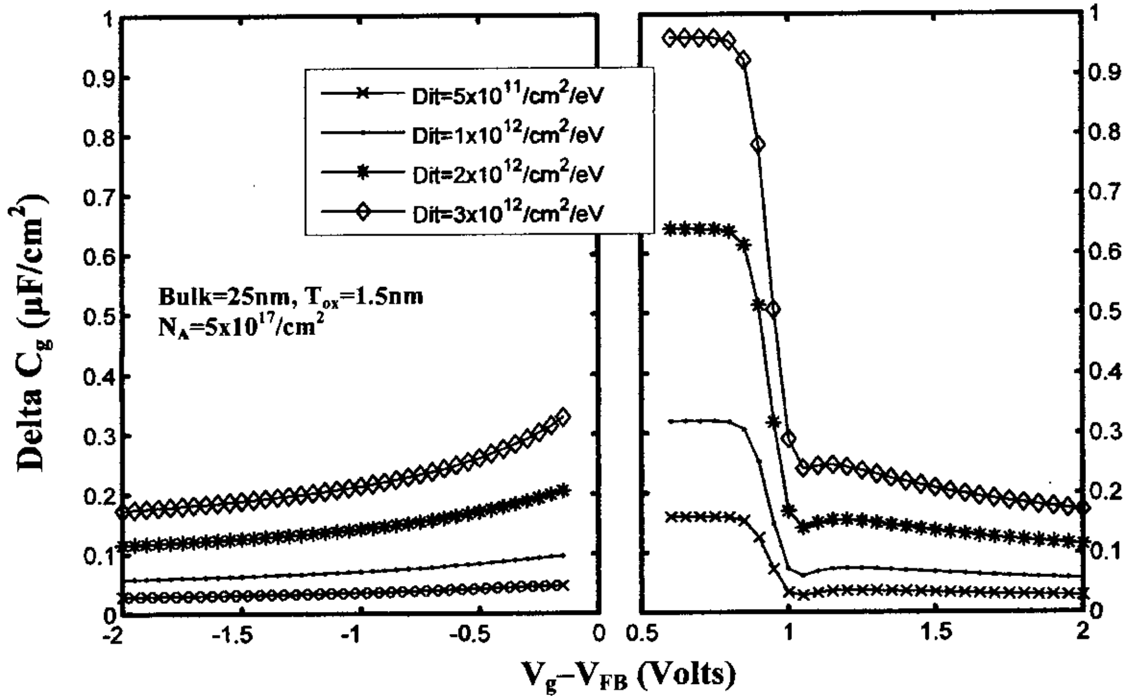


Fig.4.11. Change in LFCV Profile of an n-channel DGMOSFET for different Interface State densities

4.1.2 n-MOS Device on (100) Silicon (Undoped Substrate)

Similar calculations are performed on an n-channel DG MOS Structure with an undoped substrate. Due to the undoped substrate, the device goes to inversion at a very small applied voltage but accumulation takes place at much higher value of negative bias.

Fig.4.12 shows the C-V profile of an n-channel DGMOSFET with an undoped substrate. The effect of interface trapped charges are presented in Fig.4.13, 4.14 and 4.15 for High frequency (HF) of operation and Fig.4.16 and 4.17 shows the C-V profile of the device under Low Frequency (LF) operations.

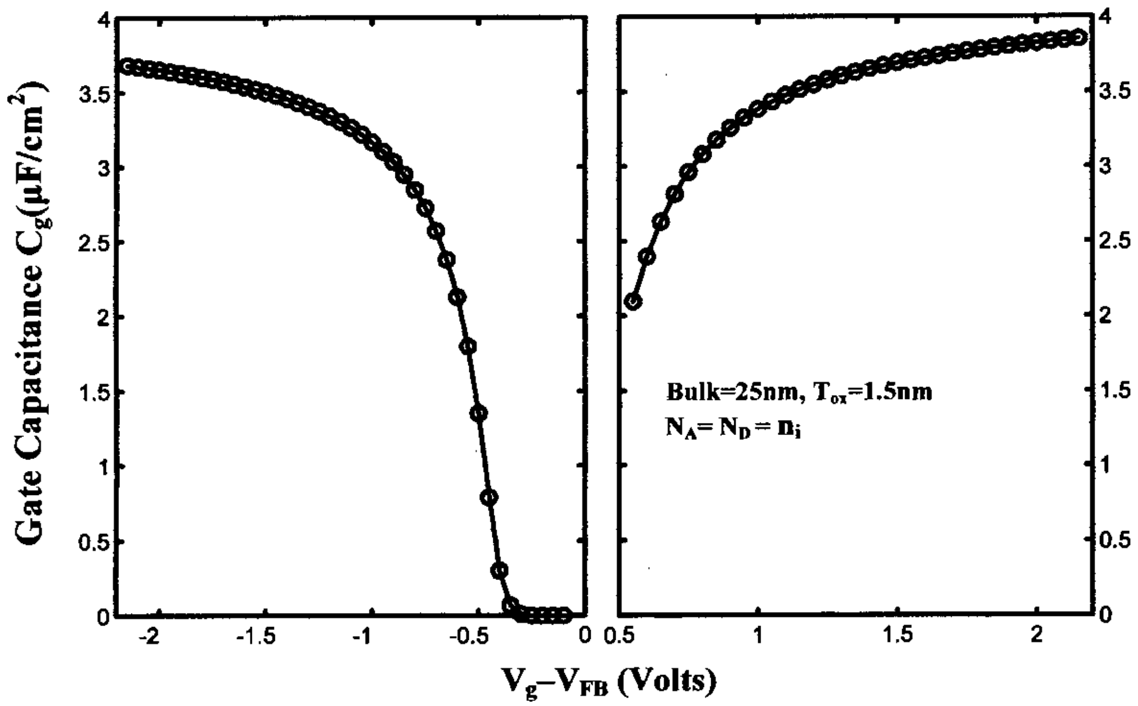


Fig.4.12. C-V Profile of an n-channel DG MOSFET

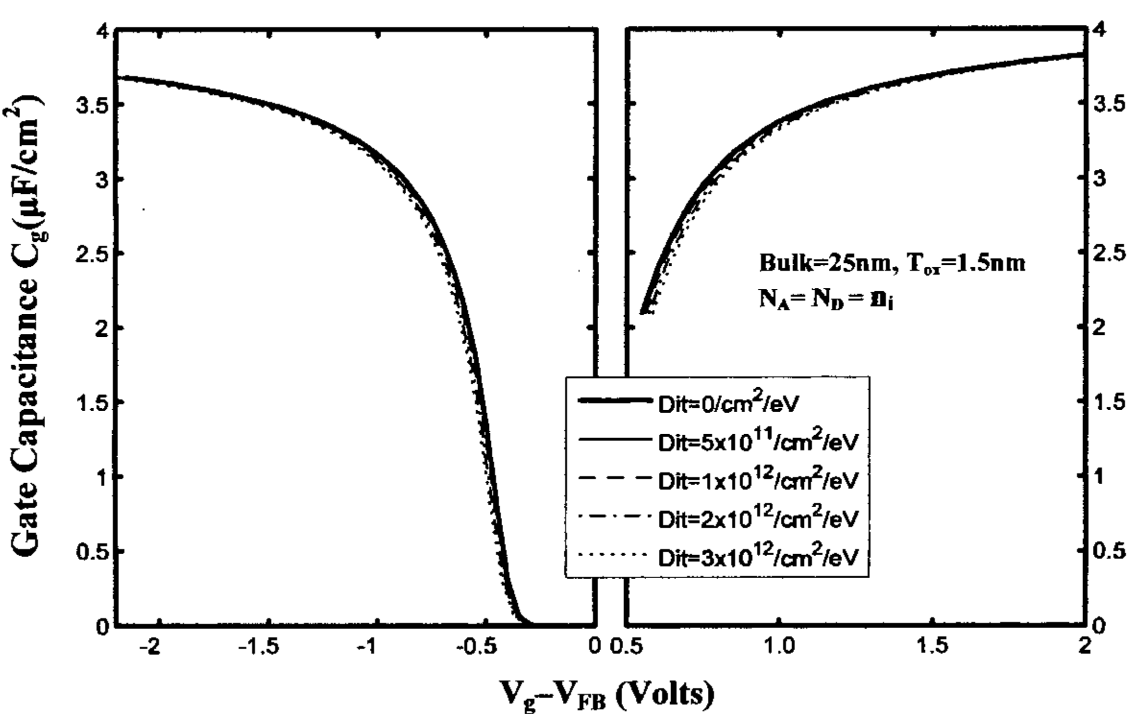


Fig.4.13. HFCV profile of an n-channel DGMOSFET for different Interface State densities

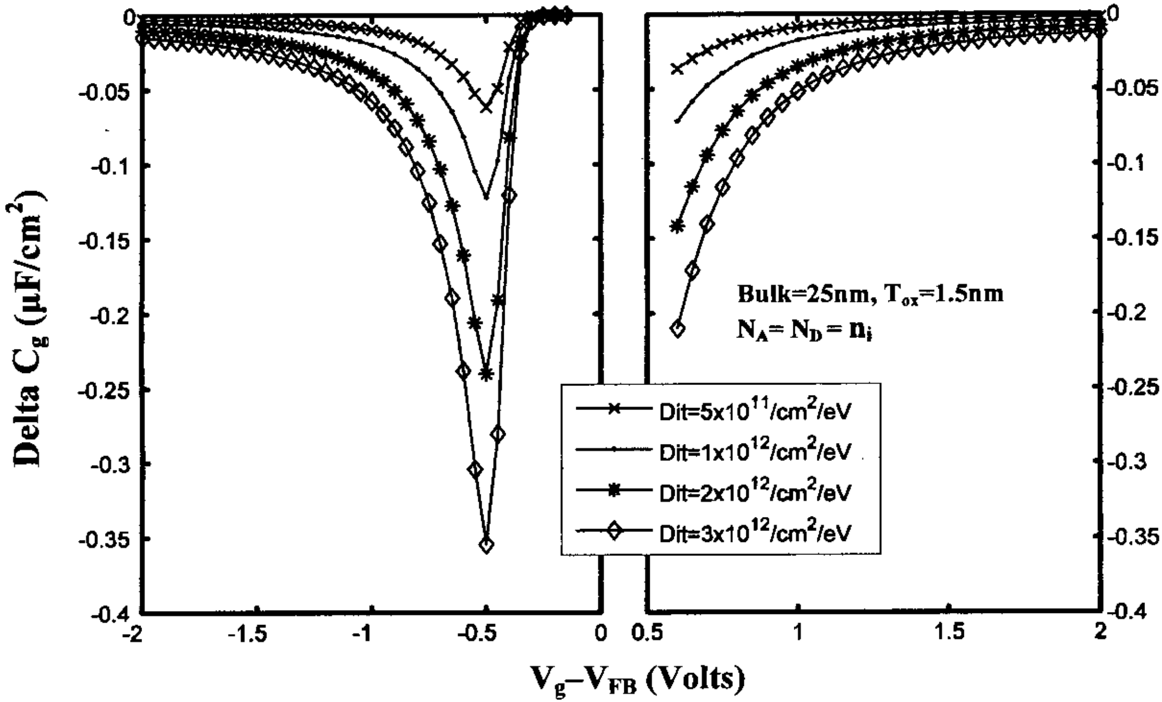


Fig.4.14. Change in HFCV Profile of an n-channel DGMOSFET for different Interface State densities

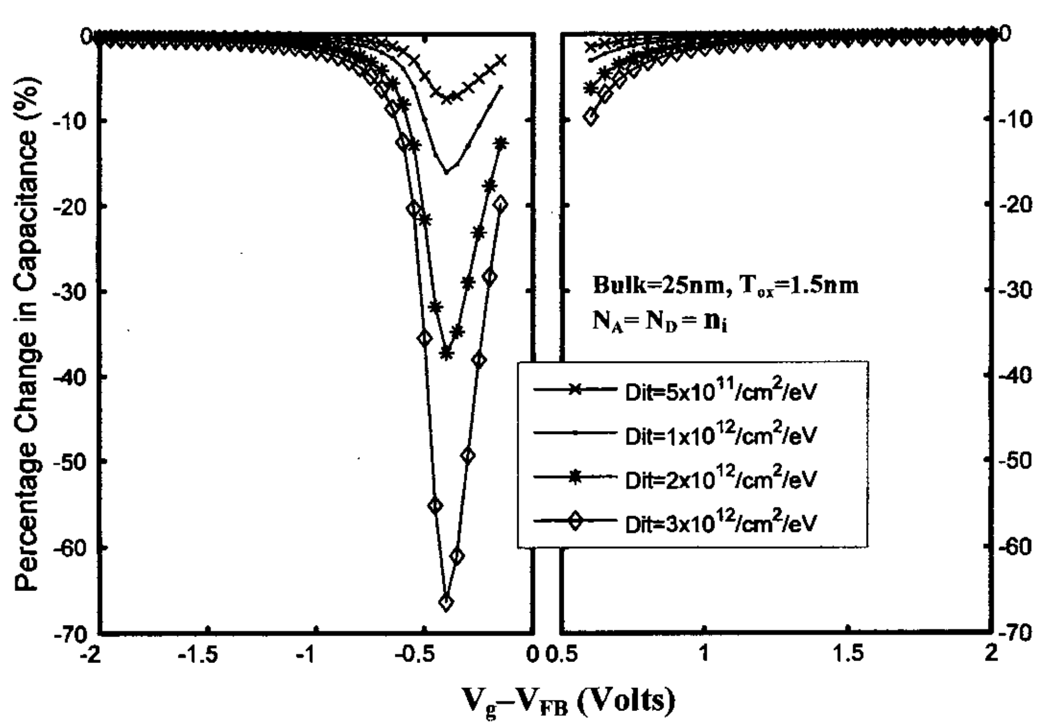


Fig.4.15. Percentage change in HFCV Profile of an n-channel DGMOSFET for different Interface State densities

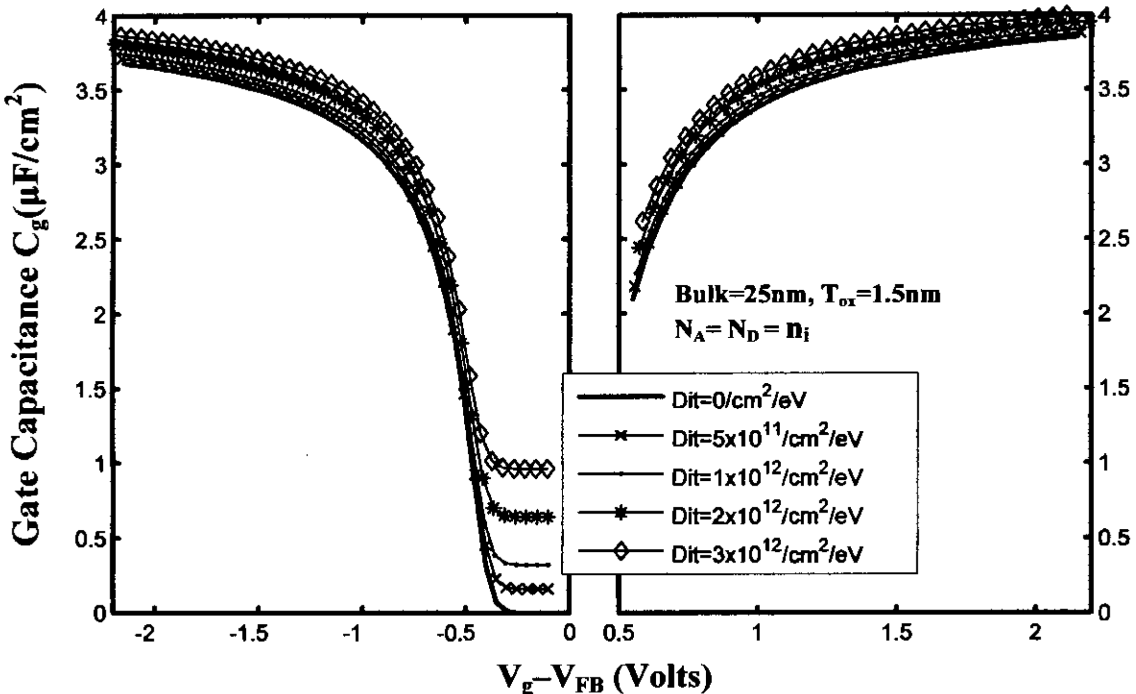


Fig.4.16. LFCV profile of an n-channel DGMOSFET for different Interface State densities

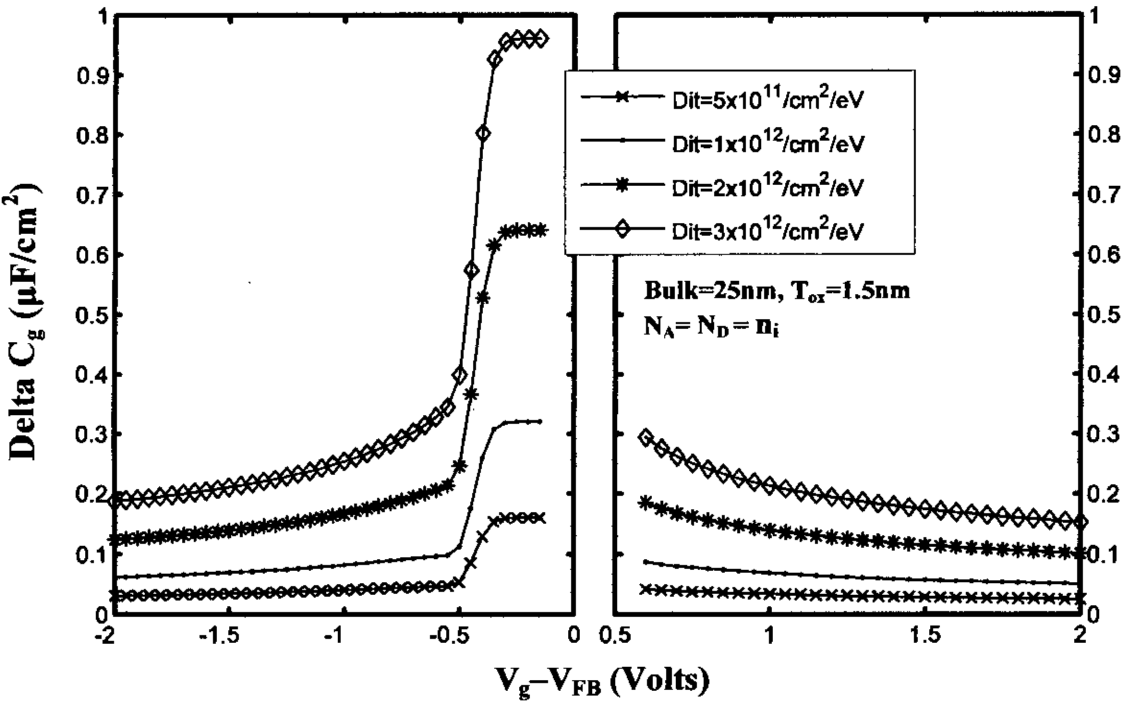


Fig.4.17. Change in LFCV Profile of an n-channel DGMOSFET for different Interface State densities

4.1.3 Effect of surface orientation

The C-V profile of an n-channel Double Gate (DG) MOSFET with substrate of (111) surface orientation silicon is also performed. The results are shown in Fig.4.18 and Fig.4.19 along with (100) surface orientated silicon substrate device of similar dimension. In Fig.4.18, we can see that the capacitance is almost same for both orientations with (100) surface resulting is slightly greater capacitance. The change in capacitance due to the effect of interface states are also presented for HF and LF operations in Fig.4.19 and 4.20 respectively for different surface orientations. It can be seen from the figures that surface orientation has no significant influence on the effect of interface trapped charges on device capacitance for identical interface state densities.

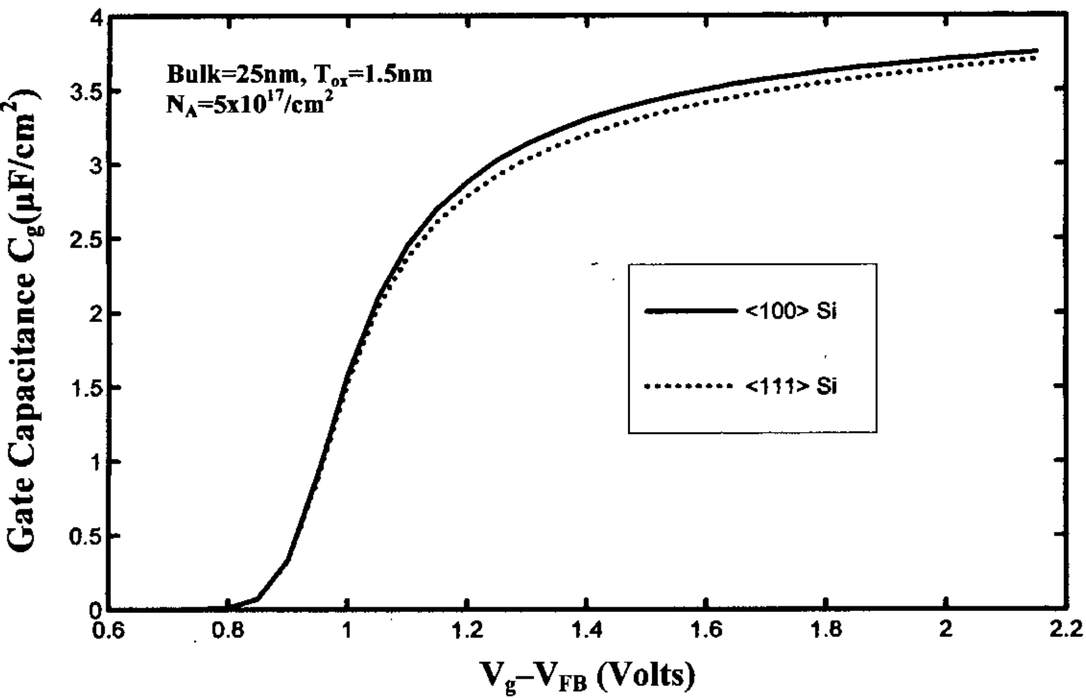


Fig.4.18. C-V Profile of n-channel DG MOS Structures at different surface orientations at inversion

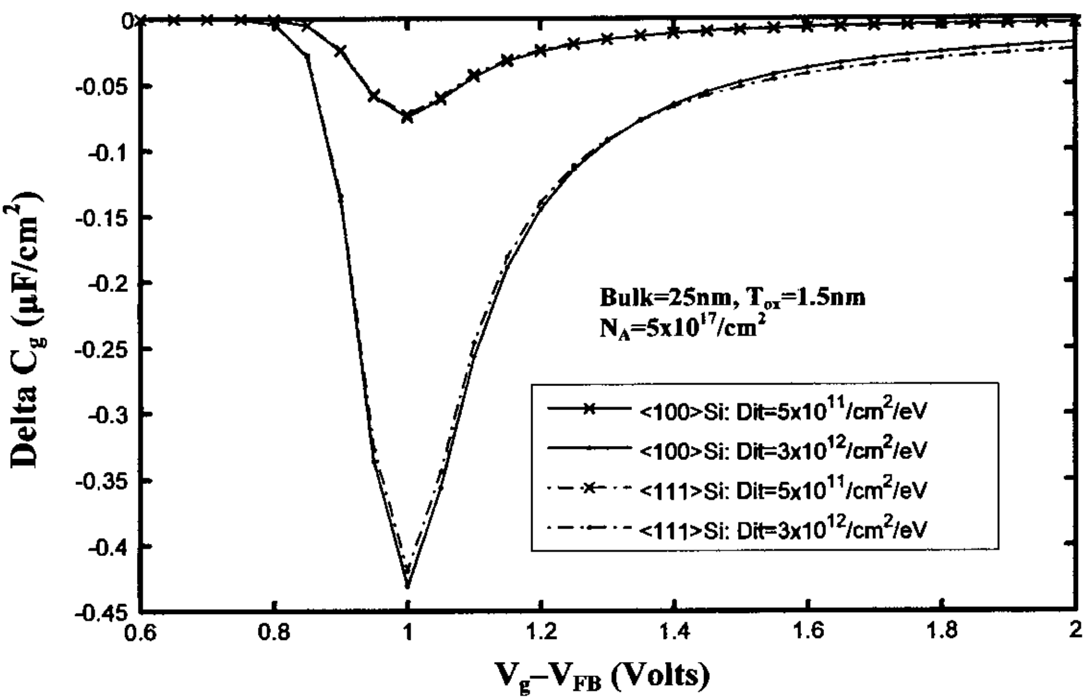


Fig.4.19. Change in HFCV Profile of n-channel DGMOSFETs at different surface orientations for different Interface State densities at inversion

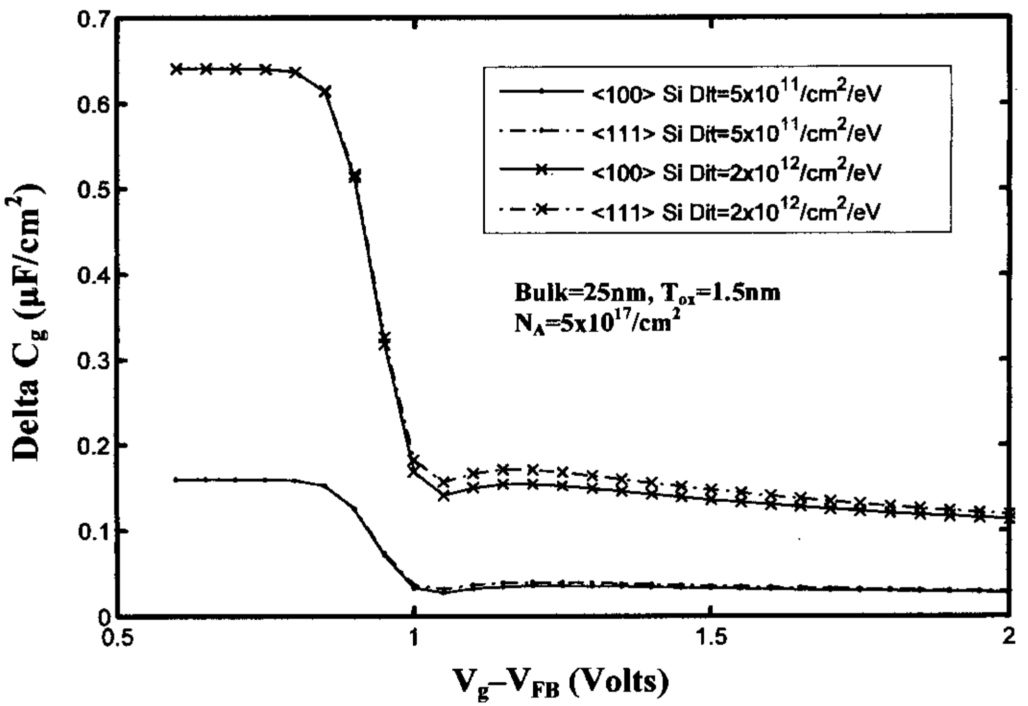


Fig.4.20. Change in LFCV Profile of n-channel DGMOSFETs at different surface orientations for different Interface State densities at inversion

4.1.4 Effect of Bulk Dimension

The effect of bulk dimension on the influence of interface trapped charge on CV Profile has been investigated. Fig.4.21 shows the C-V Profile of 3 n-channel DGMOSFETs with varying bulk dimensions. The devices have identical substrate surface orientation (100 Si), substrate doping density (Undoped) and Oxide thickness (1.5 nm). It can be seen from the Fig. that the effect of bulk dimension on C-V profile is very non-significant. The capacitance slightly decreases as the bulk size is increased but this decrement also becomes less significant as the bulk size is further increased.

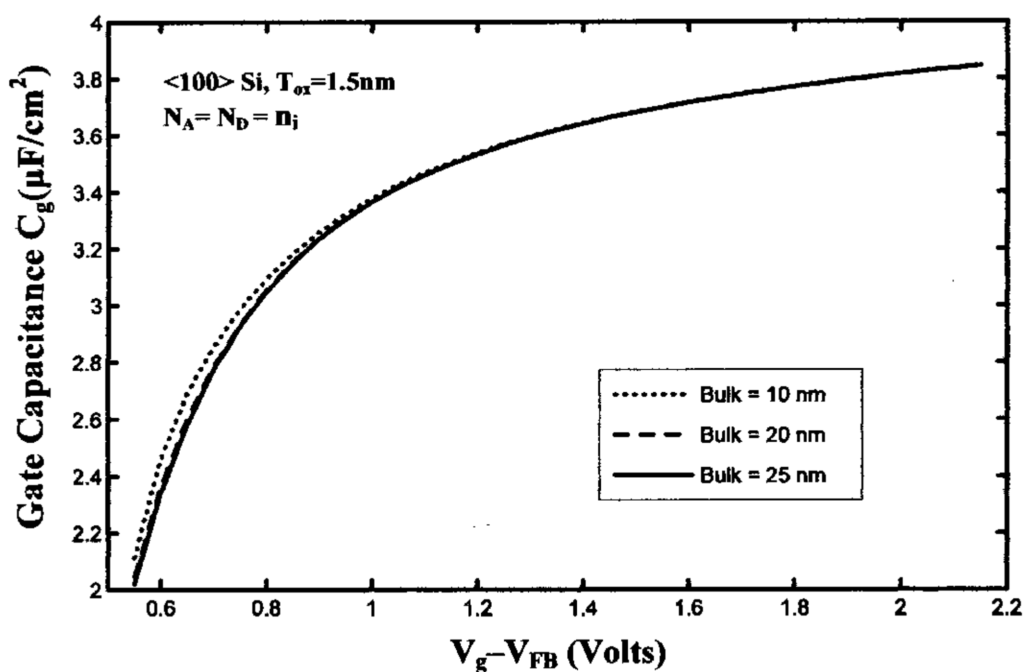


Fig.4.21. C-V Profile of n-channel DGMOSFETs of varying bulk size at inversion

Fig.4.22 and 4.23 shows the effect of bulk dimension on the influence of interface trapped charge on CV Profile under High Frequency (HF) and Low Frequency (LF) operations. During HF operation the change in C-V profile increases with increased bulk size and during LF operation the change in C-V profile decreases with increased bulk size. In both cases it can clearly be seen that the effect of bulk size is almost insignificant on C-V profile.

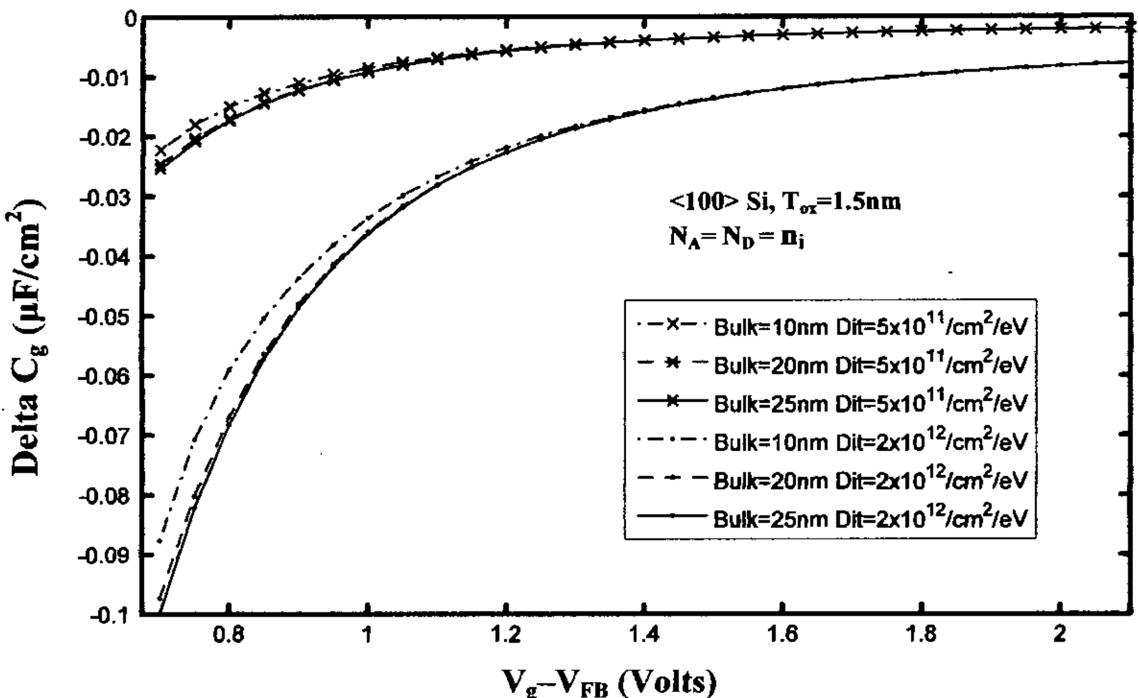


Fig.4.22. Change in HFCV Profile of n-channel DGMOSFETs of varying bulk size for different Interface State densities at inversion

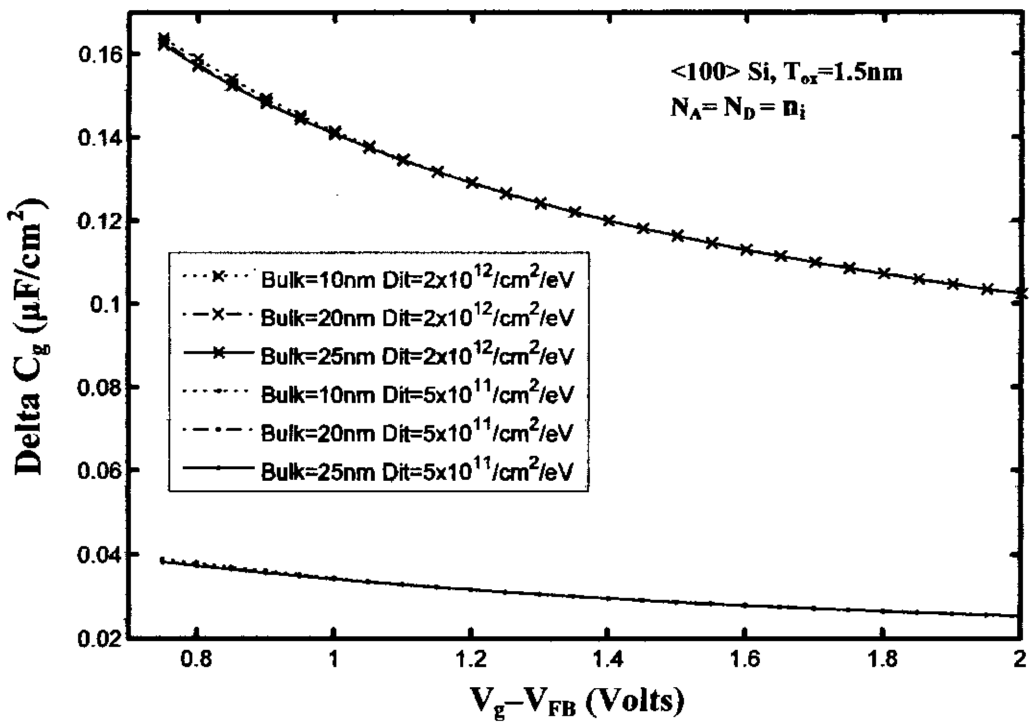


Fig.4.23. Change in LFCV Profile of n-channel DGMOSFETs of varying bulk size for different Interface State densities at inversion

4.1.5 Effect of Oxide Thickness

The effect of oxide thickness on the influence of interface trapped charge on CV Profile has been investigated. Fig.4.24 shows the C-V Profile of 3 n-channel DGMOSFETs with varying oxide thickness. The devices have identical substrate surface orientation (100 Si), substrate doping density (Undoped) and bulk thickness (25 nm). It can be seen from the Fig. that decreasing the device oxide thickness greatly reduces the capacitance of the devices.

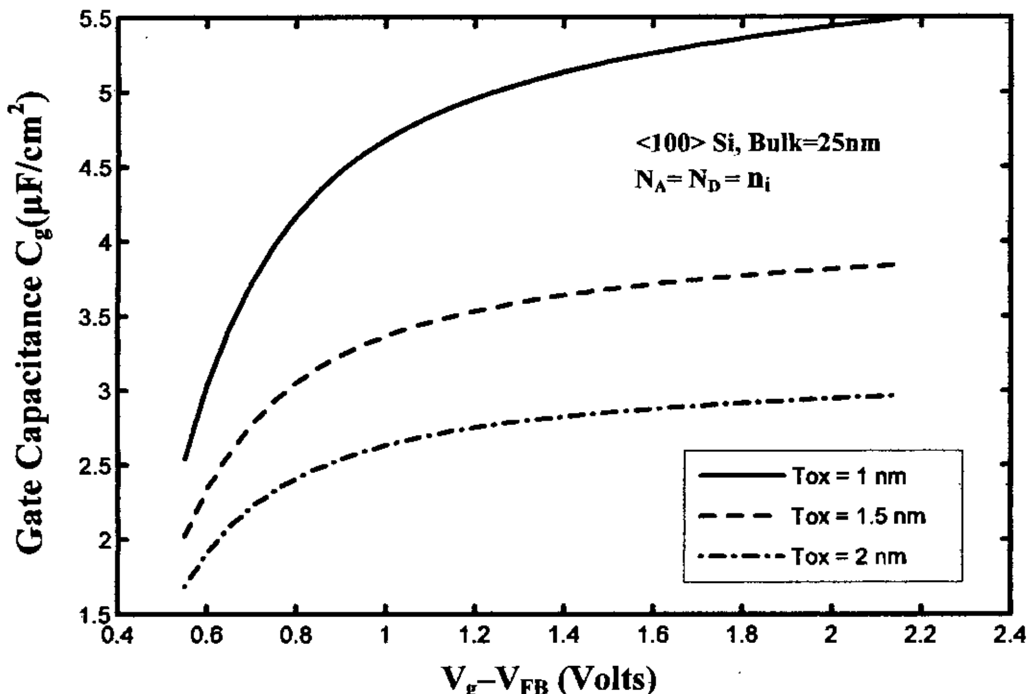


Fig.4.24. C-V Profile of n-channel DGMOSFETs of varying oxide thickness at inversion

Fig.4.25 and 4.26 shows the effect of oxide thickness on the influence of interface trapped charge on CV Profile under High Frequency (HF) operation. Fig.4.25 shows that an increased oxide thickness reduces the effect of interface states which is in contrast to the theory presented in Sec. 3.3 which illustrates that the increase of oxide thickness results in an increment in the change on threshold voltage due to interface trapped charges. The contradiction can be explained easily. The change in threshold voltage at

larger oxide thickness is more but since the original capacitance of the device is much less, even the greater change in threshold voltage fails to produce a more prominent change in device capacitance.

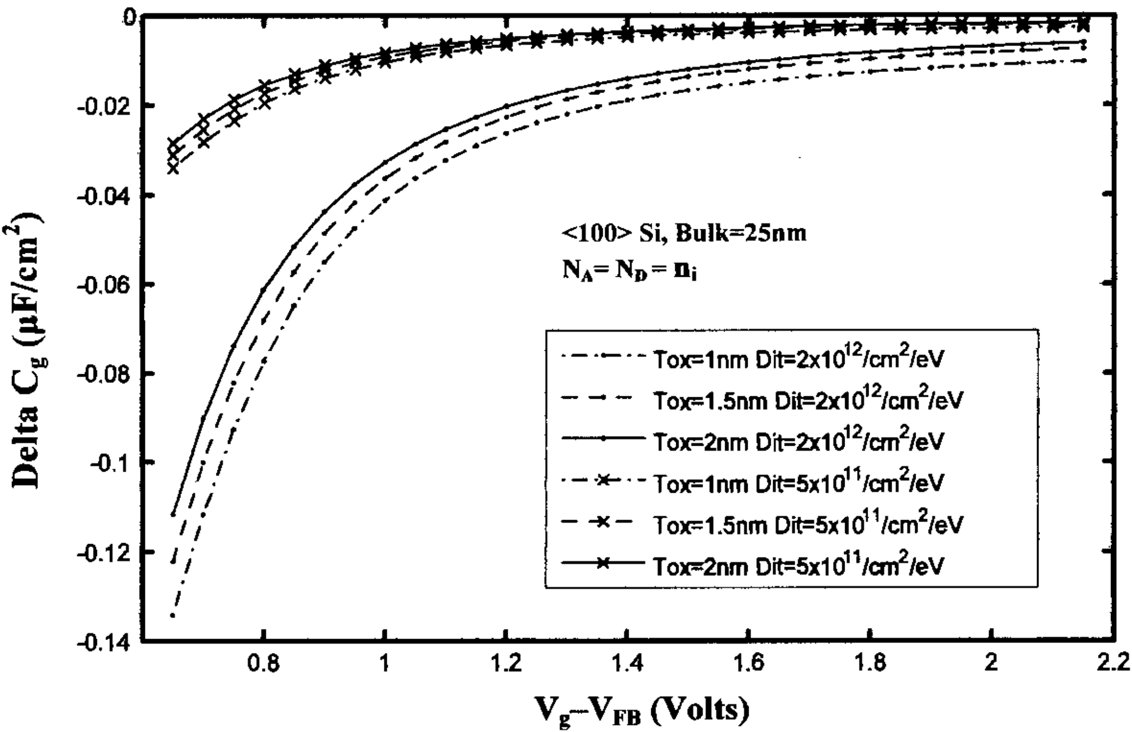


Fig.4.25. Change in HFCV Profile of n-channel DGMOSFETs of varying oxide thickness for different Interface State densities at inversion

This confusion is cleared if we observe the percentage change in device capacitance shown in Fig.4.26 instead of Fig.4.25. Fig.4.26 clearly shows that the percentage change in device capacitance due to interface trapped charges is much more prominent at increased oxide thickness. Thus the results are in complete accordance with eq. (3.20).

Fig.4.27 shows similar effect of oxide thickness on the influence of interface trapped charge on CV Profile under Low Frequency (LF) operation. The C-V Profiles are in accordance to the theory in Sec. 3.3.

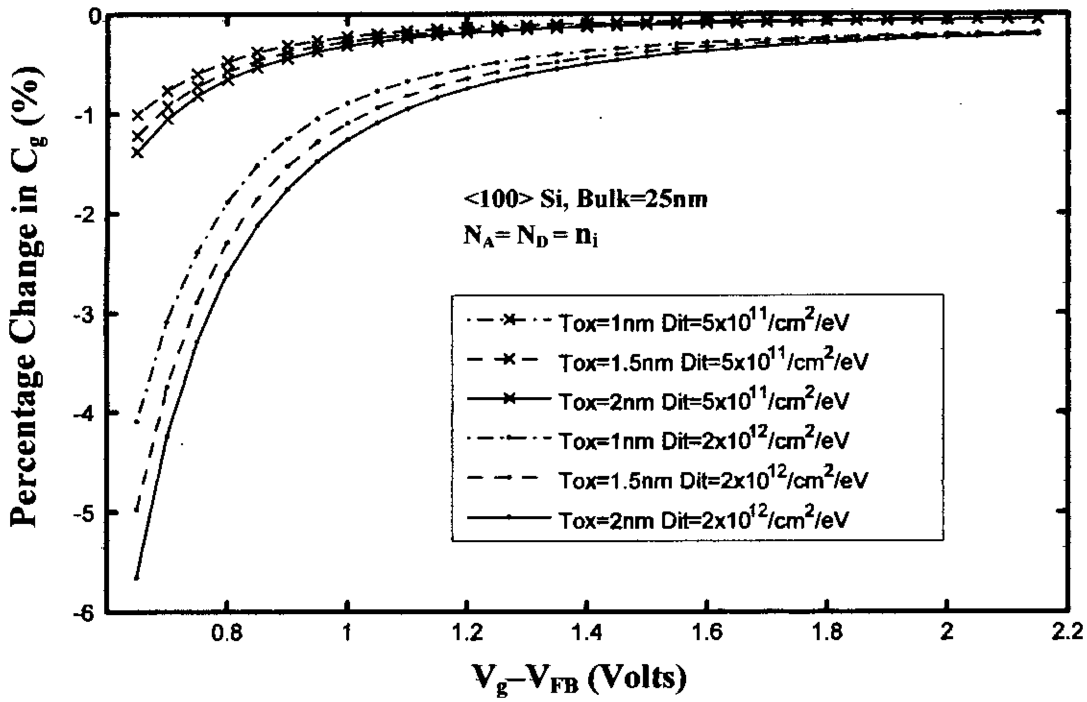


Fig.4.26. Percentage change in HFCV Profile of n-channel DGMOSFETs of varying oxide thickness for different Interface State densities at inversion

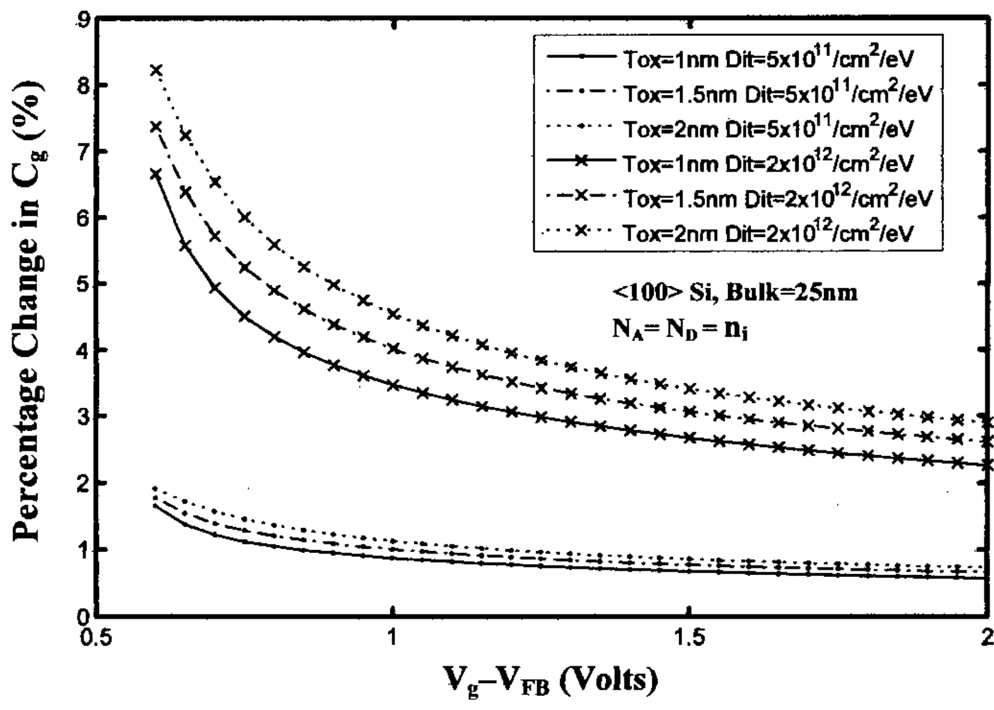


Fig.4.27. Percentage change in LFCV Profile of n-channel DGMOSFETs of varying oxide thickness for different Interface State densities at inversion

4.2 p-channel DG MOS Structures

Similar C-V profiles have been investigated for p-channel MOS structures. The results are shown in Fig.4.28 to 4.35. Both (111) and (100) surface orientations are considered. The substrate doping is also varied. The results are similar to those found for n-channel Double Gate MOS structures.

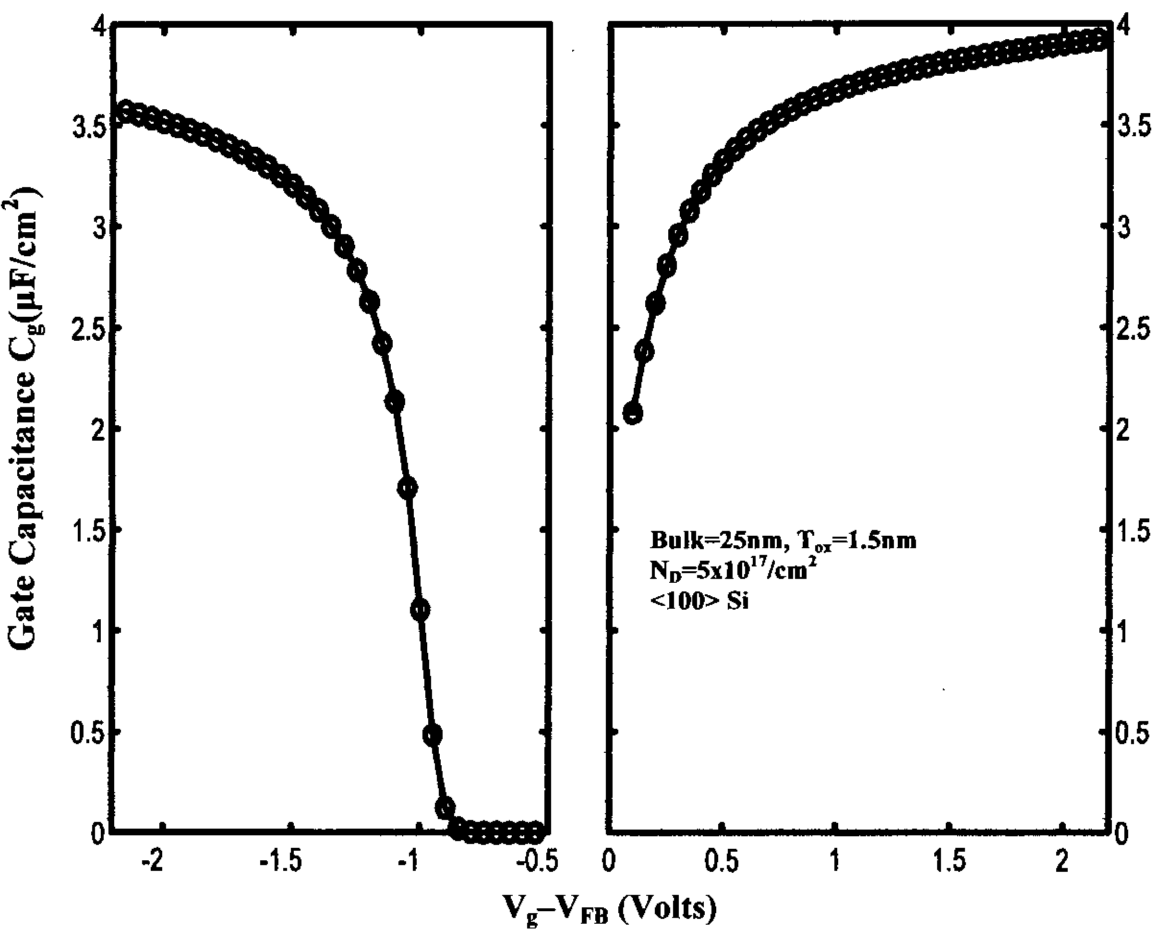


Fig.4.28. C-V Profile of an p-channel DG MOSFET

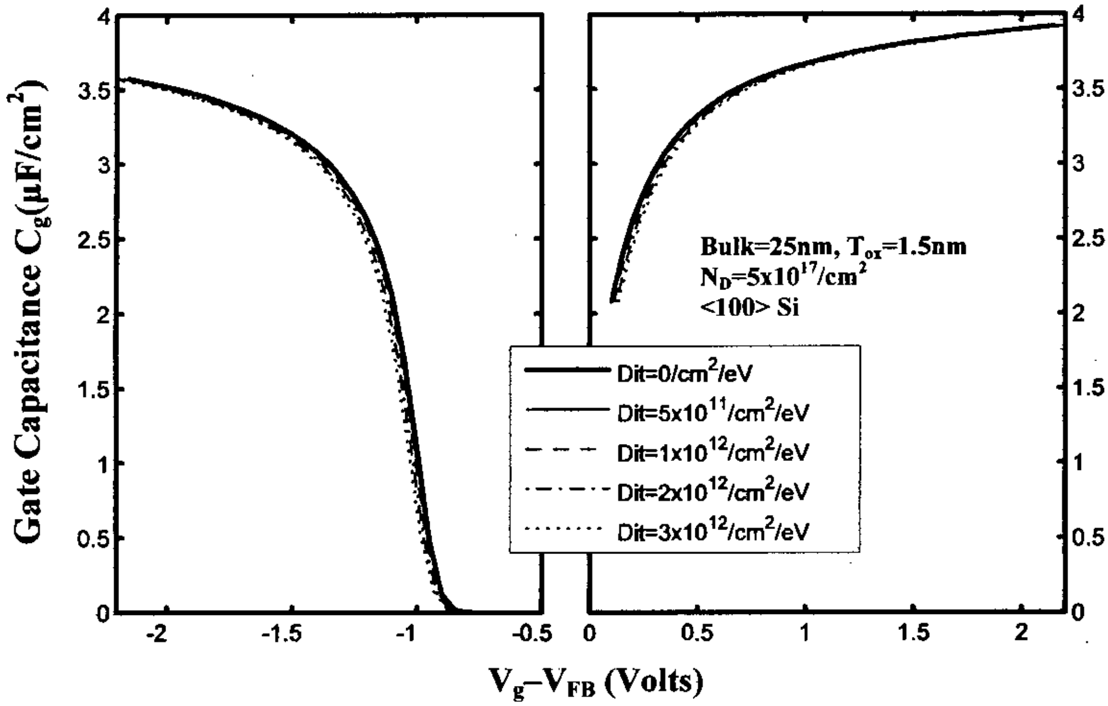


Fig.4.29. HFCV profile of a p-channel DGMOSFET for different Interface State densities

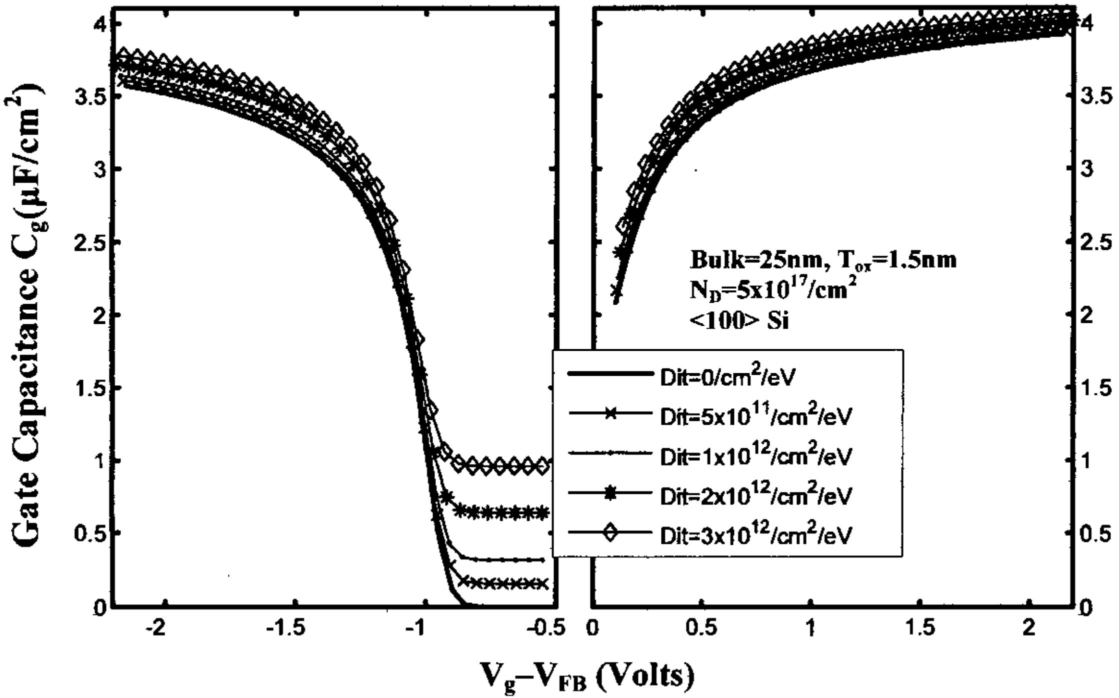


Fig.4.30. LFCV profile of a p-channel DGMOSFET for different Interface State densities

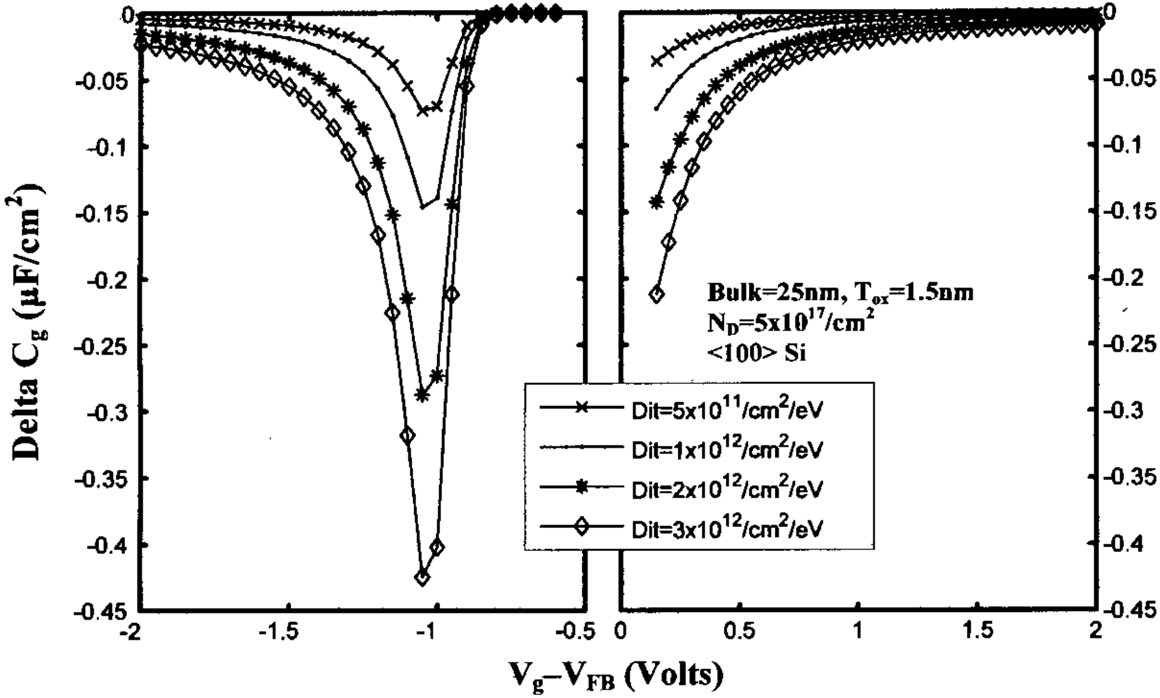


Fig.4.31. Change in HFCV Profile of a p-channel DGMOSFET for different Interface State densities

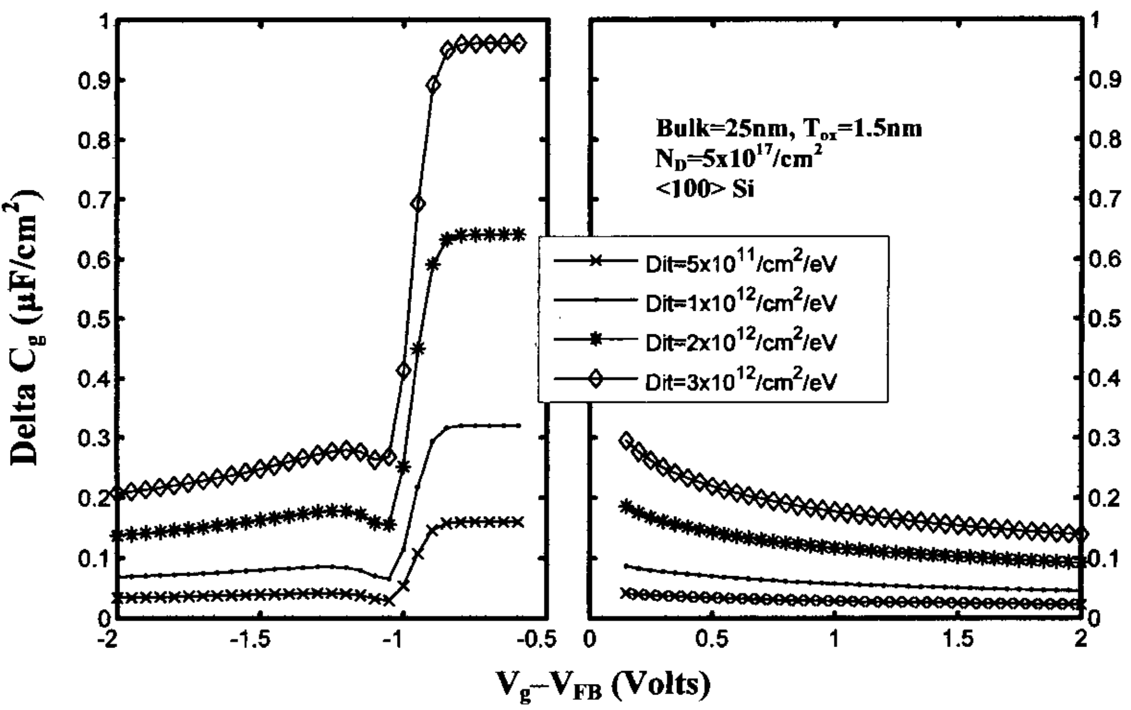


Fig.4.32. Change in LFCV Profile of a p-channel DGMOSFET for different Interface State densities

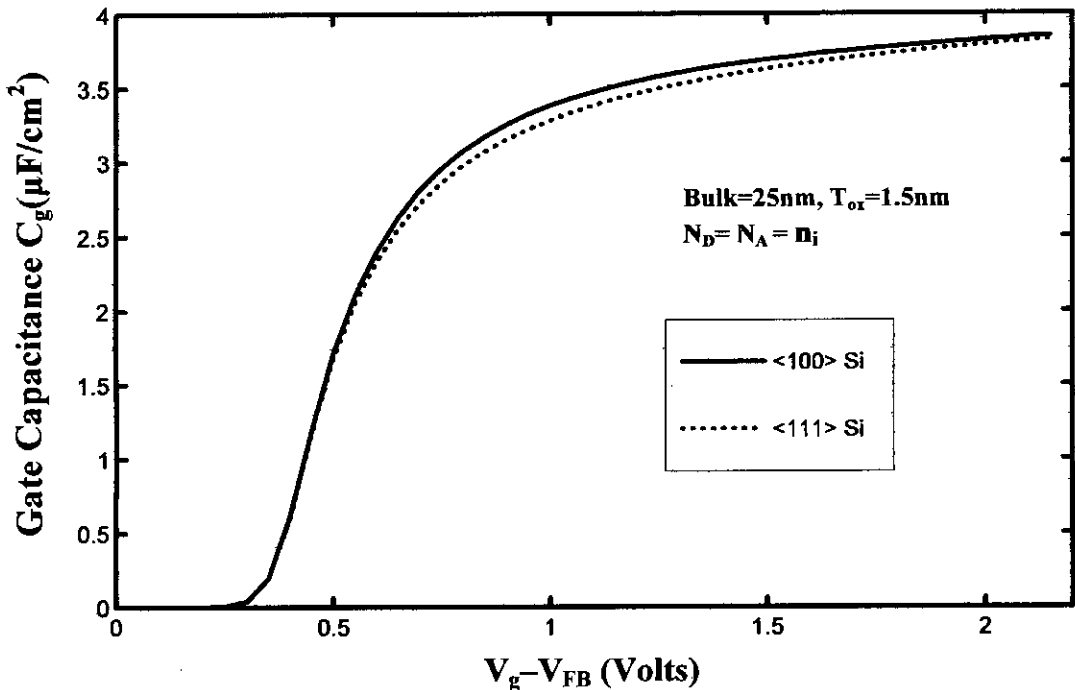


Fig.4.33. C-V Profile of p-channel DG MOS Structures for various surface orientations at accumulation

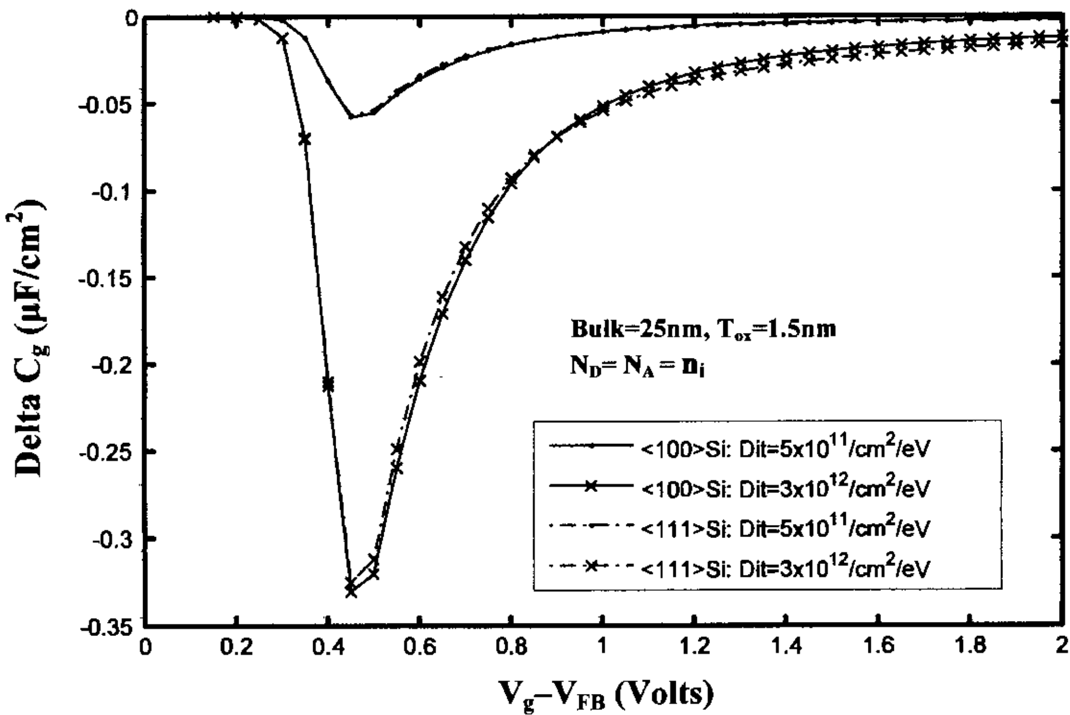


Fig.4.34. Change in HFCV Profile of p-channel DGMOSFETs at different surface orientations for different Interface State densities at inversion

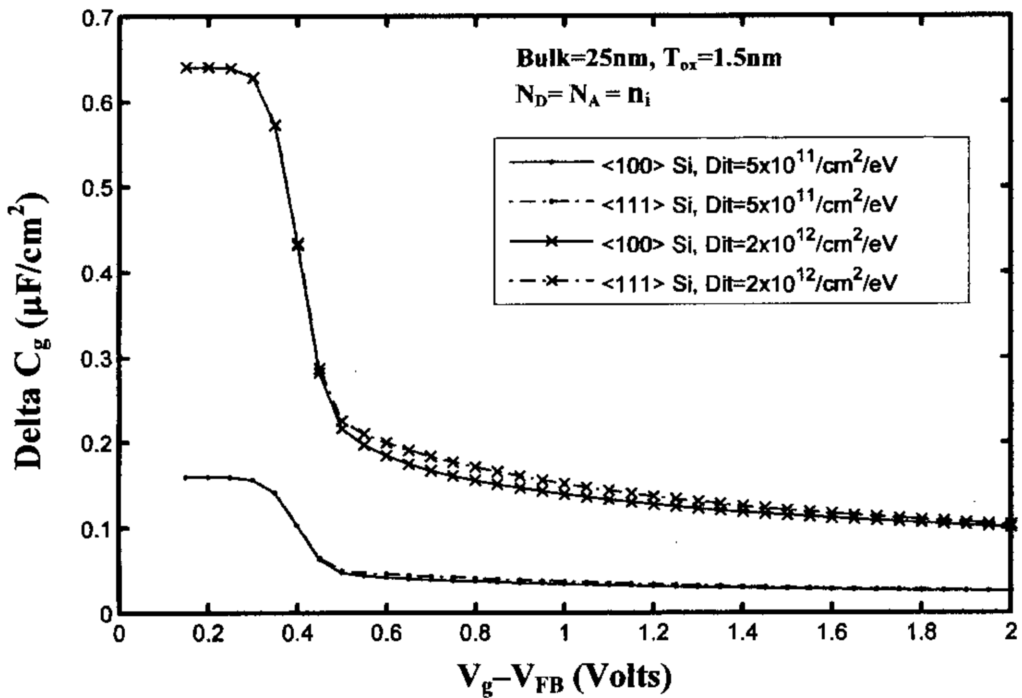


Fig.4.35. Change in LFCV Profile of p-channel DGMOSFETs at different surface orientations for different Interface State densities at inversion

CHAPTER 5

CONCLUSION

An improved and efficient self-consistent model has been developed for MOSFET simulation that incorporates the effect of wave function penetration into the oxide region. It can also be used for simulation without penetration effect. The developed model is used to investigate the Capacitance-Voltage characteristics of double gate n-channel and p-channel MOS structures. The effect of interface states on C-V characteristics are investigated by comparing the C-V profiles generated with and without incorporating the effect of interface states. It has been found that the effect of interface trapped charges on C-V characteristic is quite insignificant during high frequency operations but the effect becomes much more prominent during low frequency operations.

5.1 Summary

Effects of interface states on the Capacitance-Voltage characteristics of DG MOS structures are studied. Effect of wavefunction penetration into oxide layers has been taken into consideration while solving both Schrödinger's and Poisson's equation within the self-consistent loop. An accurate and fast formalism has been used for the solution of Schrödinger's equation using FEMLAB. Poisson's equation is solved for the combined oxide and semiconductor regions by applying an appropriate boundary condition at the gate metal-oxide interface.

The effects of interface trapped charges are incorporated in the C-V profile in two aspects. The shift in threshold voltage due to the interface trapped charges and the increase in inversion and accumulation layer charges are considered. Both high frequency

and low frequency operations are investigated. Varying device dimensions and surface orientations are considered.

Numerical results on n-channel DGMOS structures on (100) silicon show that during high frequency operation, interface trapped charges cause an almost insignificant amount of reduction in device capacitance during strong inversion and strong accumulation. But during weak inversion or accumulation, the percentage change in capacitance is quite significant. In low frequency operation however the change in device capacitance due to interface states is very prominent and it increases the capacitance unlike the case in high frequency operations. Also, the most significant change occurs during depletion mode of operation. Both doped and undoped substrates were considered and they produced similar results, with a slightly higher overall capacitance for devices with undoped substrates.

The effect of surface orientation has also been investigated. Results show that both (111) and (100) silicon DGMOSFETs are identically affected by the interface trapped charges. The capacitance is found to be slightly greater for (100) Si devices, when compared with (111) Si devices.

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Comparison between numerical results from devices with varying bulk size shows that the capacitance decreases slightly with increasing silicon thickness. During HF operation the change in C-V profile due to interface states increases with increased bulk size and during LF operation the change in C-V profile decreases with increased bulk size.

Investigation on the effect of oxide thickness on the influence of interface trapped charge on CV Profile shows that decrement in device oxide thickness greatly reduces the capacitance of the devices. Results show that percentage change in device capacitance due to interface trapped charges is much more prominent at increased oxide thickness for both high and low frequency operations.

5.2 Suggestion for Future Work

Self-consistent solution is an important tool for simulation of many devices where the QM effects become significant. Our self-consistent model may be used for simulating many systems such as single gate, double gate MOS structure, high electron mobility transistor, resonant tunneling diodes and quantum well lasers, where self-consistent calculations with open boundary conditions is necessary. A few suggestions for future work are given below-

We have applied 1-D analysis of the DGMOS capacitor. But when voltage is applied between the drain and the source, 2-D nature of QM arise in the channel. So, a 2-D simulation should be performed. A 2-D analysis can also be used to determine the transport behavior of DGMOSFETs. Device characteristics such as drain current, transconductance, channel mobility etc can be determined with the use of 2-D analysis. FEMLAB can be used to perform 2-D and 3-D simulations also. Hence, 2-D nature of device parameters can be determined.

As the gate length of CMOS devices are continued to be scaled down to sub 100 nm regime, scaling rule dictate that the gate oxide thickness be scaled down to well below 1 nm. It is know, with the decreasing dielectric thickness, tunneling gate current increases rapidly. In order to decrease this leakage current, high K materials should be used as gate dielectric. The modeling of such devices can be done easily with the proposed self-consistent model.

In our calculations, we have used effective mass approximation for both electrons and holes. However, due to anisotropy and mixing of valence bands, the use of effective mass approximation for holes has been a topic of debate. The present model for pMOS devices may be further improved by incorporating the non-parabolic valence band structure.

APPENDIX A

The modified self consistent model, which has been used in this study, has been described in section 3.2. Here, a details flow diagram of the solver is given for better understanding.

A.1 Flowcharts

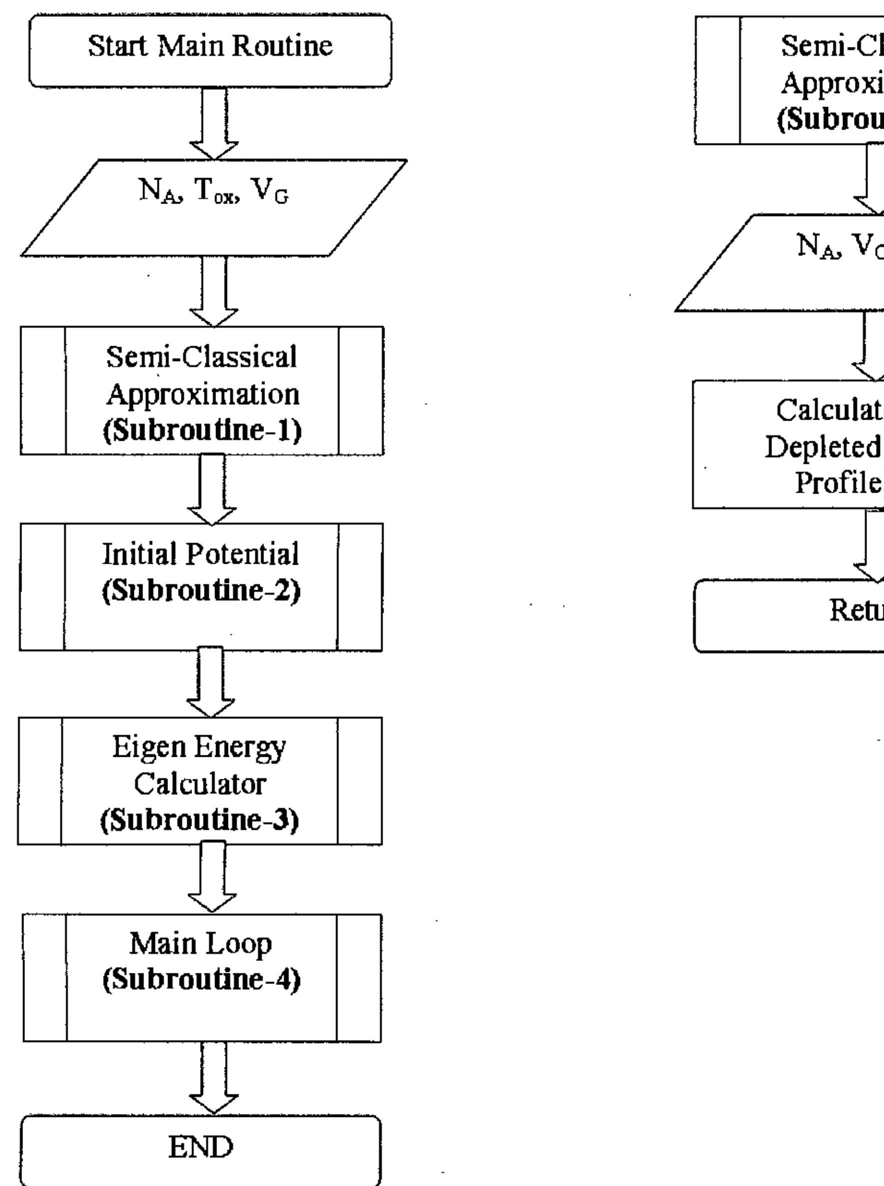
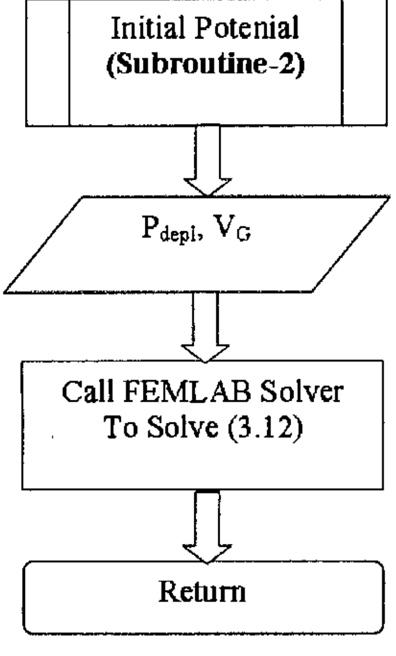


Fig.A1. Flowchart



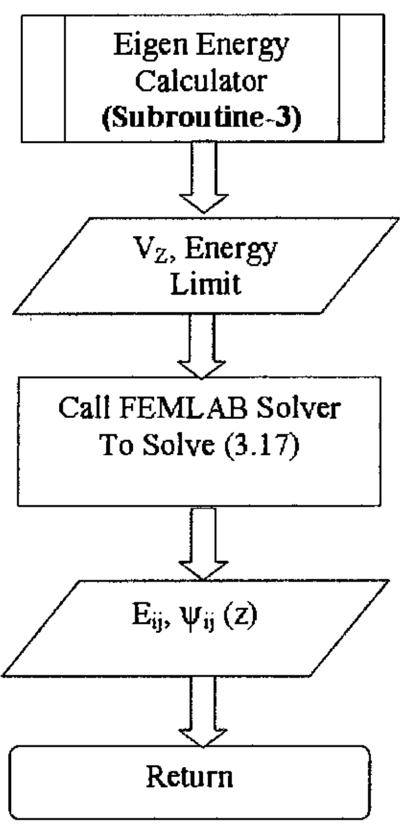


Fig.A2. Flowchart (contd.)

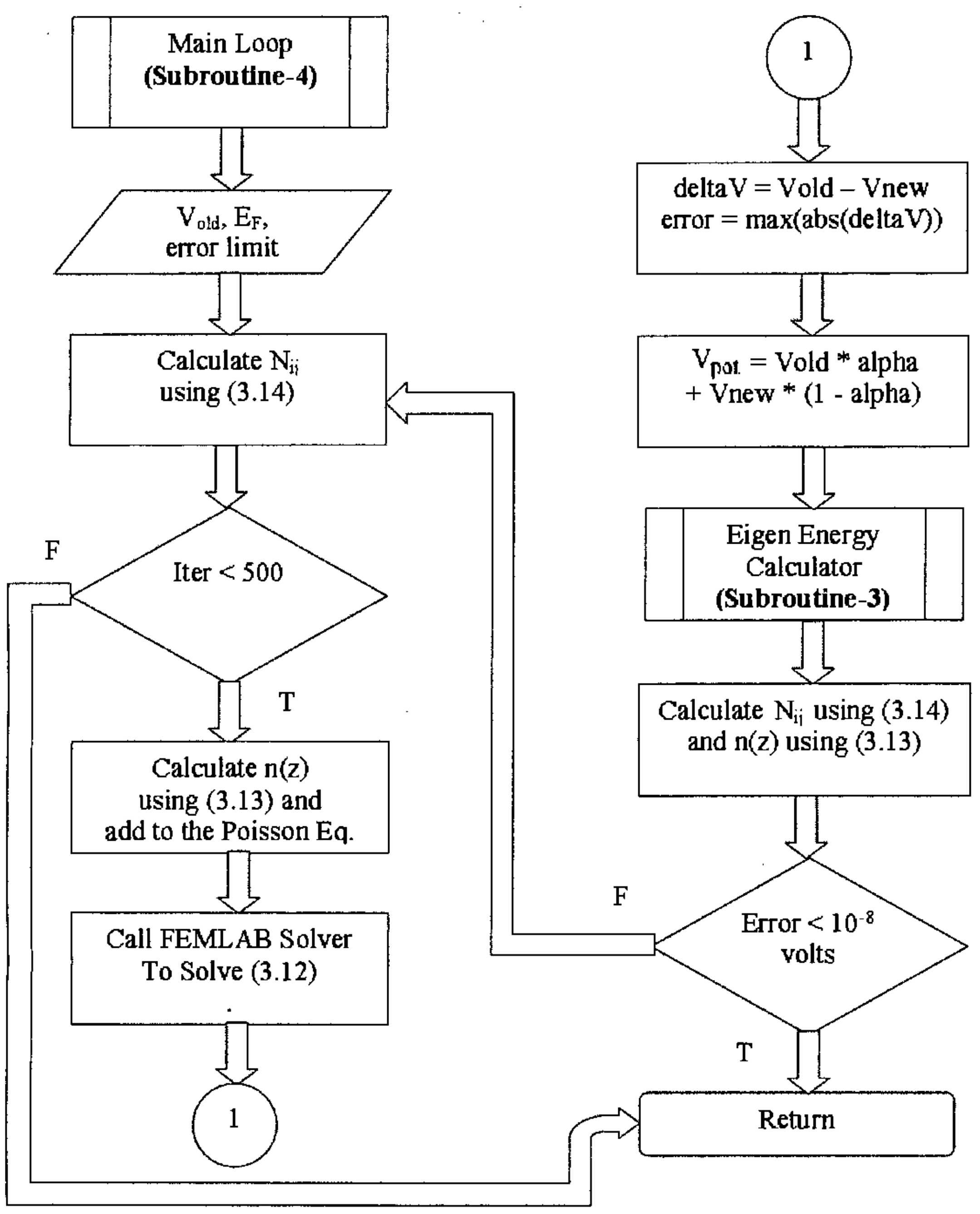


Fig.A3. Flowchart (contd.)

APPENDIX B

Publications based on this work is recorded below-

1. **Ahsan-Ul-Alam**, Sabbir Ahmed, Md. Kawsar Alam and Quazi D. M. Khosru, "A Quantum Mechanical Study Of C-V Characteristics Of Double Gate MOS Structures Incorporating The Effects Of Interface States" Accepted for publication at the 2008 International Conference on Nanoscience and Nanotechnology, Melbourne, Australia, to be held on February 25-29, 2008

2. **A. Alam**, S. Ahmed, M.K. Alam and Quazi D.M. Khosru , "Effect of Interface States on C-V Characteristics of Double Gate MOS Structures," Accepted for publication at the IEEE International Nanoelectronics Conference (INEC) 2008, Shanghai, China, to be held on March 24-27, 2008.

3. M. K. Alam, **A. Alam**, S. Ahmed and Q. D. M. Khosru, "On the Self-Consistent Calculation of Ultra Thin Body Double Gate MOSFET," Accepted for publication at the IEEE International Nanoelectronics Conference (INEC) 2008, Shanghai, China, to be held on March 24-27, 2008.

4. S. Ahmed, M.K. Alam, **A. Alam** and Quazi D.M. Khosru , "Calculation of Gate Leakage Current of a Double Gate MOS structure incorporating Wave Function Penetration Effects," Accepted for publication at the IEEE International Nanoelectronics Conference (INEC) 2008 , Shanghai, China, to be held on March 24-27, 2008.

5. M.K. Alam, **A. Alam**, S. Ahmed, M.G. Rabbani and Q.D.M. Khosru , "Wavefunction Penetration Effect on C-V Characteristic of Double gate MOSFET," In Press for publication at the International Semiconductor Device Research Symposium (ISDRS 2007), College Park, MD, USA, to be held on Dec. 12-14, 2007.

6. S. Ahmed, M.K. Alam, **A. Alam**, M.G. Rabbani and Q.D.M. Khosru , "Quantum Mechanical Study of Gate Leakage Current in Double Gate MOS structures," In Press for publication at the International Semiconductor Device Research Symposium (ISDRS 2007) , College Park, MD, USA, to be held on Dec. 12-14, 2007.

7. S. Ahmed, M.K. Alam, **A. Alam**, M.G. Rabbani and Q.D.M. Khosru , " Study of Gate Leakage Current incorporating Quantum Mechanical Effects," In Press to be included in the Proceeding of the IEEE ED Bangladesh Chapter Student Paper Contest 2007.

8. M.K. Alam, **A. Alam,** S. Ahmed, M.G. Rabbani, and Q.D.M. Khosru , "An Accurate and Fast Schrodinger-Poisson Solver using Finite Element Method ," Proceedings of the 18th IASTED International Conference on Modelling and Simulation ~MS 2007~ , Montreal, Canada, pp.246-249 , June, 2007.