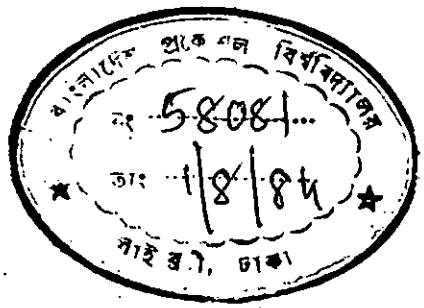
DEVELOPMENT OF A DIGITAL AC VOLTAGE REGULATOR



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A dissertation on the

Development of a Digital A.C. Voltage Regulator

Submitted to the
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and Electronic Engineering

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CERTIFICATE

This is to certify that this work has been done by me and it has not been submitted elsewhere for the award of any degree or diploma or for publication.

Arun Kanti Chowdhury

(Signature of the candidate)

COUNTERSIGNED:

(Supervisor)

Date: 26/6/78

ABSTRACT

The digital alternating voltage regulator using thyristors for synchronous tap-changing gives an output voltage which varies within a range. This range of variation is more when less number of taps are provided to the regulator transformer. Generalized form of an a.c. voltage regulator proposed in this dissertation is one in which N number of taps are provided to the regulator transformer. A salient feature of the control circuit is that the number of NAND-gates at the input terminals of the power module is equal to the number of taps of the regulator transformer. The design procedure is such that the number n of the D-flip flops, SR-flip flops or comparators used are determined by the formula, $n=N-1$, where N is the number of NAND-gates. The voltage regulator designed for maximum number of N provides an output voltage with a minimum percentage of regulation, that is the range of variation of the output voltage is a minimum. Practical circuitry are designed and initial construction as per design are provided for $N=5$.

CERTIFICATE OF ACCEPTANCE

Accepted as satisfactory for partial fulfilment of the requirements for the degree of Master of [redacted] Engineering in Electrical and Electronic Engineering.

Examiners:

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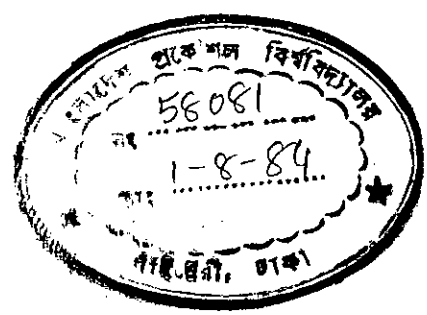

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1-3 FORMULATION OF THE PROBLEM

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1.1. INTRODUCTION:

An established method of using thyristors to regulate alternating voltage-supplies is to employ them as tap-changing switches on a transformer. High switching speeds are possible. The control of the switching pattern permits accurate regulation of output voltage. With loads having long time constants, the switching dutcycle may allow each tap to be connected continuously to the load for several cycles. In many cases, however, this is unacceptable and variation in output voltage must occur no more slowly than the nominal cycling of supply voltage. It is convenient to achieve this by moving through one complete tap-changing sequence every half cycle of supply voltage as it is then possible to utilize natural commutation of thyristor switches.

The inverse parallel connected thyristors operate as bilateral switches and at the start of each half cycle, one of the pair of thyristors conducts supplying voltage to the load. Sometimes, later, in the next half cycle, the other thyristor of the pair is fired. The circuit is simple and because only a fraction of the output power is handled directly by the SCR, component ratings are relatively low. The same control circuit can be used for the regulator of any rating. Only the power module and the regulator transformer are required to be changed to change the rating of the regulator.

The tap-switches of the regulator transformer will be selected in steps of discrete variation of voltage at the input side. If we consider the regulator using servomotor (in which the continuous input variation will operate the servomotor continuously) as an analog voltage regulator, we may call the discrete variation type voltage regulator as a digital voltage regulator.

1-2. HISTORICAL BACKGROUND:

A.C. voltage regulators are used to obtain steady voltage from a fluctuating supply voltage. Changes in supply voltage level above and below the nominally declared value, if exceeds a certain limit, may cause serious problems. The appliances and equipment connected to the system may get damaged, complicated production line may stop, the entire system may be required to be repeated again, readings of the indicating system may become erroneous, thus creating a lot of inconveniences and also may result in loss of revenue. For continuous and precision operation and protection of the system concerned, voltageregulators are essential.

The abbreviation AVR is used for Automatic Voltage Regulator. It is a device with the help of which line voltage can be regulated. In fact, AVRs are used in obtaining a predetermined fixed voltage from a varying or changing voltage source. However, AVR can provide with a constant output only for a certain range of variation of the input voltage. The maximum tolerable voltage variation for most AVR equipments are found to be around ±10% of the nominal voltage.

For equipments like computers and computing devices, televisions, control equipment for various industrial installations, telephone equipments and other communication equipments, small and medium size refrigerating units, stage lighting control dimming equipment, broadcasting equipments and several other equipment and installations, AVRs are needed for smooth operation and protection.

In an automatic voltage regulator there are a tap-changing transformer or Buck and Boost transformer and the automatic control part. In the automatic control portion there may be servo-motor controlled by electronic circuits or electronocally controlled switching circuits, for switching the transformer taps. If it is desired that the output from the voltage regulator be fixed to one value, in that case electrocally controlled servomotor is necessary for continuous variation at the input side.[1] But if it can be tolerated that the output from the AVR can remain within a range (say ± 5%), step variations may be done at the input side.

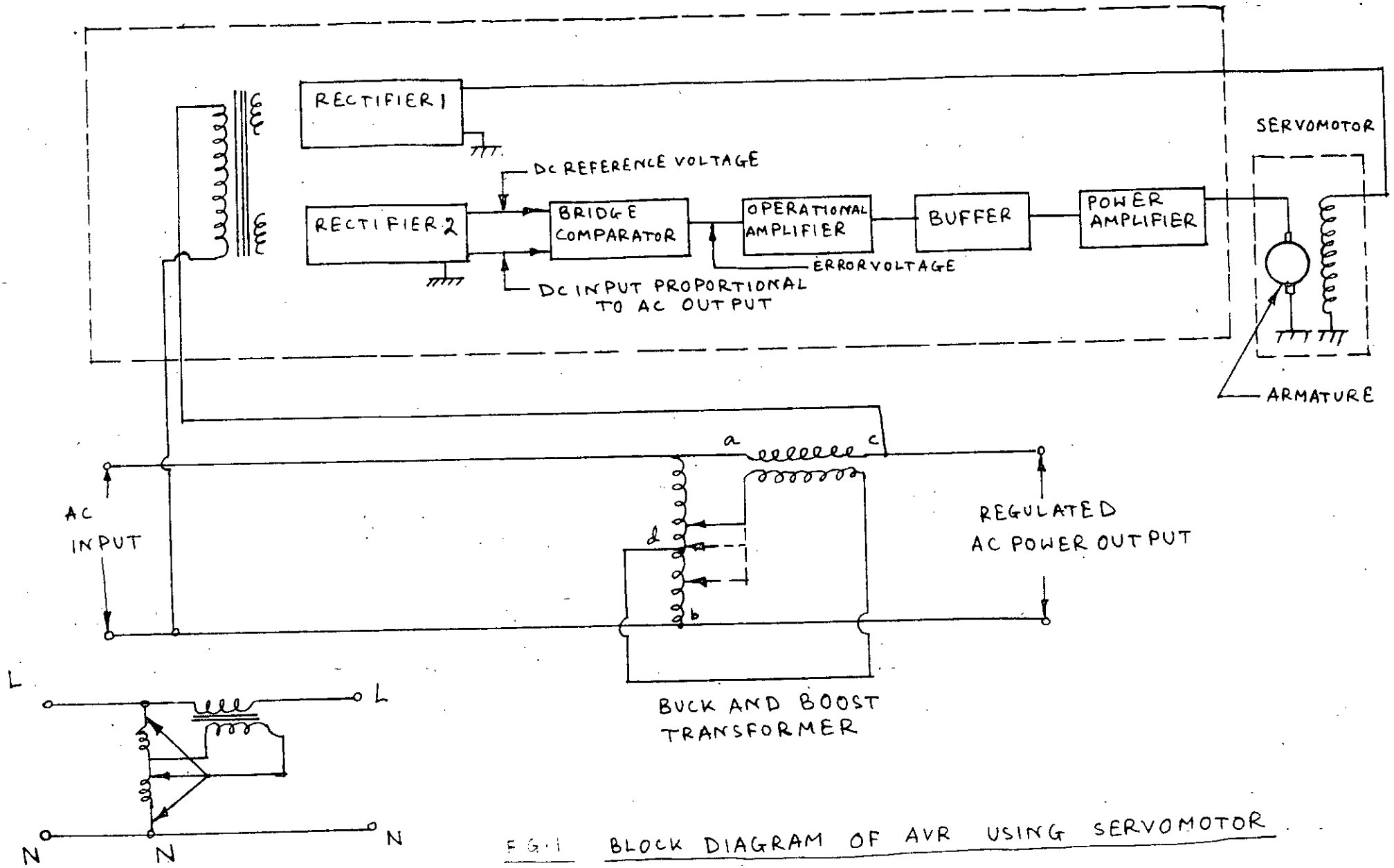
There are two types of AC AVR equipments :

(1) Continuous variation type using servomotor.

(2) Discrete variation type using tap-switches.

The AVR using buck and boost transformer and servomotor is shown in fig.-1.

AC input is supplied to the input terminals of the buck and boost transformer and the regulated AC output is taken from the output terminals of the same. The servomotor shaft is mechanically connected to the moving contact of the regulator transformer. When normal line voltage is present g is connected to the point d and the transformer secondary is shorted to short out the transformer primary (because the impedence of the transformer will be reduced). When high line voltage is present point g moves towards b to buckdown the input voltage. When low line voltage is present point g moves towards a to boost up the input voltage. Rectifier 1 supplies current to the field of the servomotor. From rectifier 2, the reference voltage and the input to the comparator are obtained. When the input is different from the reference voltage as the input ac line voltage is high or low, a current will flow through the armature of the servomotor. Then the servomotor will operate the contact g of the regulator transformer to make required correction to the line voltage.



FG·1 BLOCK DIAGRAM OF AVR USING SERVOMOTOR

1-3 FORMULATION OF THE PROBLEM

An A.C. voltage regulator, having the ability to boost up or buckdown the supply voltage to a predetermined value has been designed. We have taken the help of the original design by Topaz Electronics in which they used three transformer taps i.e. N = 3. Digital logic circuits have been used to control the output voltage of the regulator. The essential features of the system have been shown in the block diagram as in figure 2 and 3. The control circuit diagram is shown in figure -4.

In three phase circuits, one control circuit is used in each phase, separately. The voltage regulator consists of (1) a solid state control circuit (2) , a tapped transformer and (3) solid state tap switches.

The control circuit senses the line voltage and determines what correction must be made. The solid state tap switches are controlled by the control circuit. The selected taps of the transformer are operated by them. The required correction to the line voltage is then made by the transformer.

The regulator is designed in such a way that the output from the regulator will always remain at 220 ± 5% volts for a variation of input voltage from 200 V to 250 V. When any of the line voltage (to neutral) attains a value more than 250 V, over voltage protection circuit will operate and trip the line circuit breaker. When a fault occurs in the circuit of any phase, an unbalance occurs in the 3 phase supply mains, line loss circuit will operate and trip the line circuit breaker. When the line voltage drops to a value less than the rated minimum of 200 V to (neutral) the driver inhibit output will be at logic 0. This output is supplied to a relay which will operate and trip line circuit breaker. The inverter and the low input voltage sensor circuit constitute the driver inhibit.

CONTROL BLOCK DIAGRAM

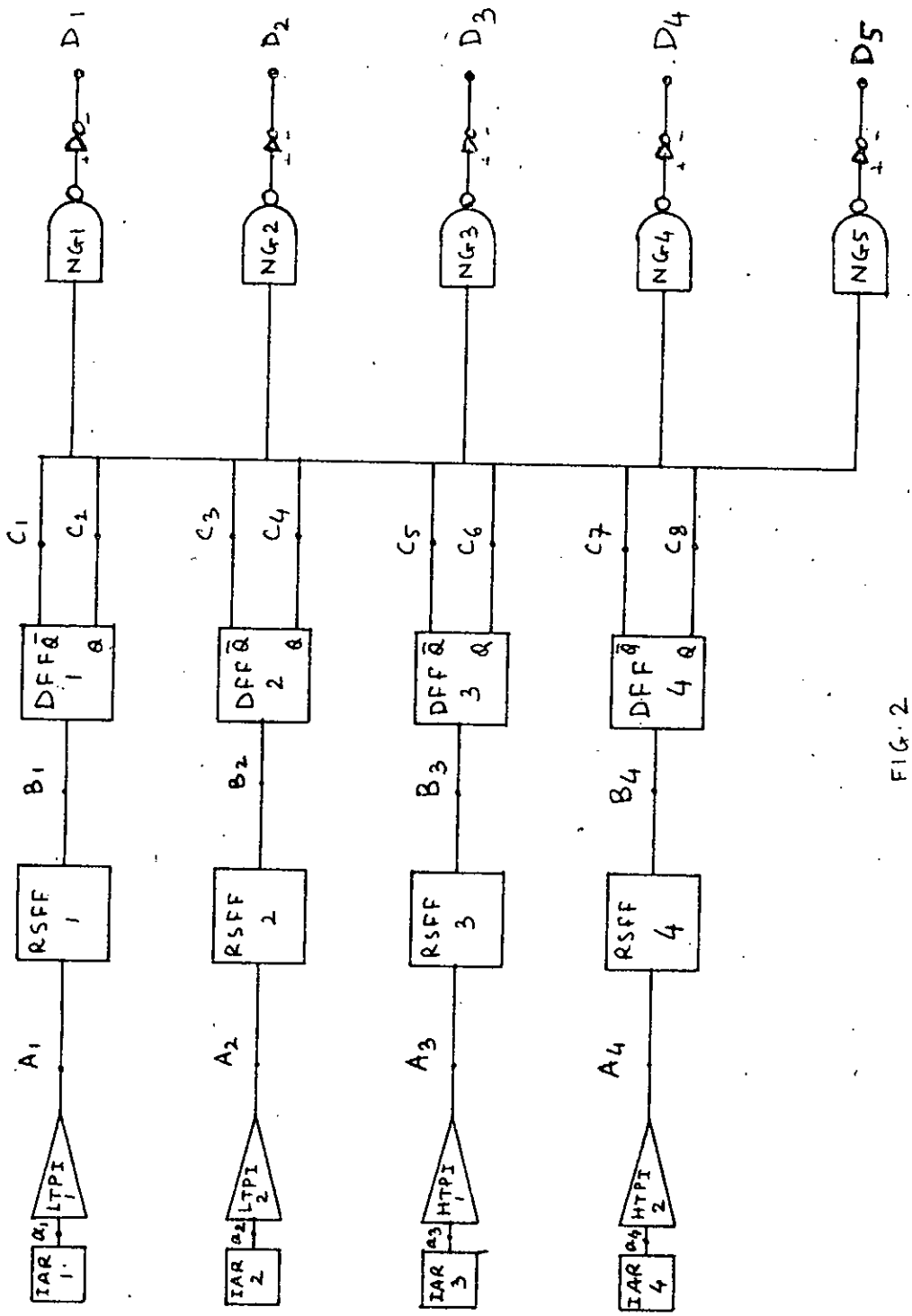
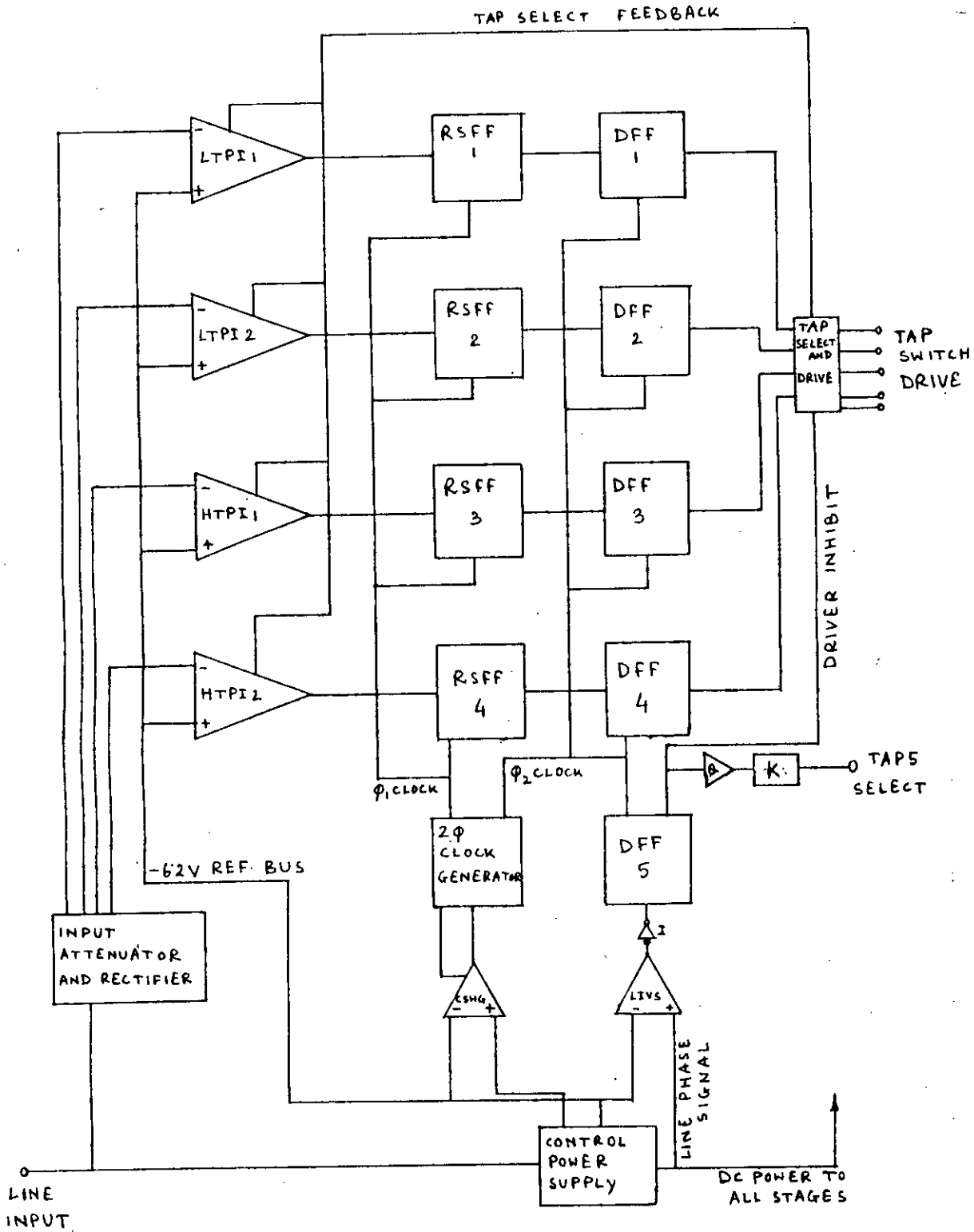


FIG. 2

CONTROL CIRCUIT BLOCK DIAGRAM



FIG·3

CONTROL CIRCUIT

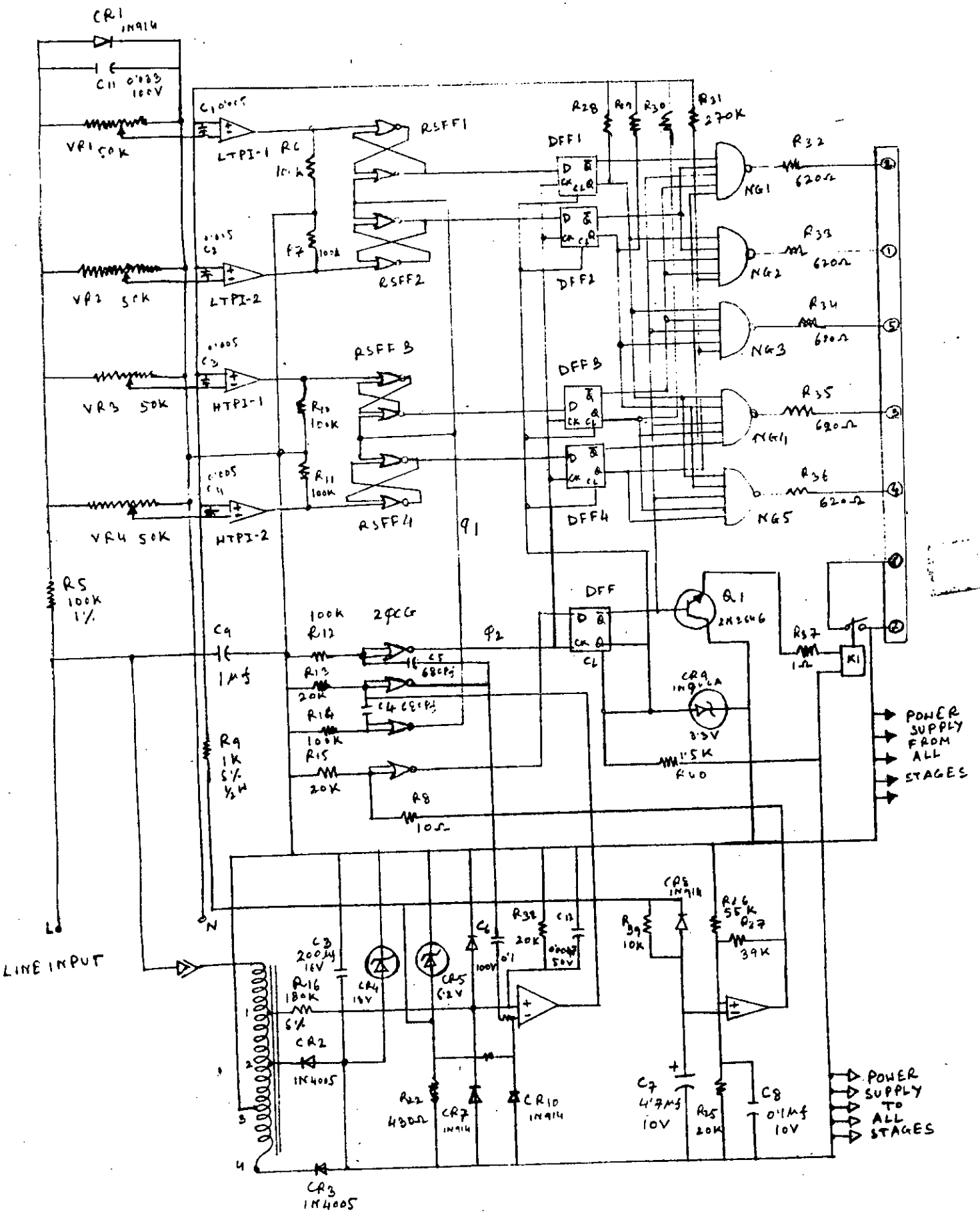


FIG. 4.

Another output is taken from the LIVS circuit and connected to one input of each NAND-gate. Thus the NAND-gates are also prohibited to operate under this condition.

The regulating trasformer is designed in such a way that it can step up the input voltage , leave it unchanged or step it down.

The input attenuator reduces the line voltage to a desired optimum value and feeds the input rectifier. The rectifier rectifies the negative half cycles of the line frequency and feeds 4(four) comparators. Among the comparators, two are low trip point input comparator (LTPI 1 and 2) and the other two are high tip point input comparators (HTPI 1 and 2). The output of the rectifier will be proportional to the input voltage. At the another input terminal of each comparator, a reference dc voltage is supplied. A voltage in the form of square waves will appear at the output of a comparator, when the rectified voltage exceeds a certain limit. When line voltage is below 200V, none of the comparators has got output. When the line voltage is above 210V, comparator 1 (LTPI 1) will have square waves at it's output . When line voltage is above 220V, comparator 2 (LTPI2) will have square waves at it's output together with comparator 1. When line voltage is above 230V, comparator 3 (HTPI 1), will have square waves at it's output, together with comparators 1 and 2, When line voltage is above 240V, comparator 4 (HTPI2) will have square waves at it's output, together with comparators 1, 2 and 3.

The outputs of these comparators will be fed to a set of four RS-flipsflops which constitutes first level of data storage. Clock pulses are supplied to the RS- flip-flops to x transfer data from the input to the output. Thus when a clock pulse comes, the input of the RS flip-flop will appear at the output.

The outputs of these RS-flip flops are fed to a set of four D-flip-flops which constitutes the second level of datastorage. Clock-pulses are supplied to D-flipflops to respond to any changes of state at their inputs from RS flipflops.

The outputs of D-flipflops are 8 (eight) in number in total. These outputs are connected to a set of five 5-input NAND gates. Another input is supplied to each of the NAND-gates from the driver inhibit line. So, in total 9 (nine) output terminals are distributed to 5(five) NAND gates. One NAND-gate will have output state logic 0, when and only when all the inputs connected to it are logic 1. The regulator is designed in such a way that when the line voltage is in the range of 200V to 250V, only one of the NAND-gates will have logic 0 at it's output. Outside this range, the circuit will remain off. The output from each NAND-gate is inverted, converted to negative logic and fed to the gates of triacs of the power module. Two triacs and two SCRs connected in inverse parallel comprises a solid state tape switch. The SCRs are connected in inverse parallel to pass current for both half cycles of the line voltage. The SCRs are connected to proper taps of the regulating transformer. The pair of SCRs which have got triggering voltages from the control circuit. the transformer tap connected to that pair will be selected. Then the output voltage will be determined by the regulating transformer. For low power regulators only triacs are used for tap switches. But for high power regulators, two SCRs are also added to the set of two triacs to make one tap switch.

The regulating transformer is a multitap auto-transformer with an auxiliary secondary winding. The auto-transformer part has got 6(six) of tap points. The auxiliary secondary winding has got a solid state tap switch which shorts the secondary side when normal line voltage appears at the mains. Then the transformer core becomes saturated to reduce it's impedence. The Automatic voltage regulator also has phase sensing circuits which controls the timing of tap-changes. The phase sensing circuits are comprised of clocksquarewave generator, two phase clock generator and a low input voltage sensor. The clock-square wave generator converts sinewaves of line voltage to square waves by a monostable multivibrator circuit. The square - waves

is then converted to two pulses, one is phase 1 clock pulse and the other is phase 2 clockpulse. Phase 1 clockpulse drives the SR flipflops and phase 2 clockpulse drives the D- flip-flops. The two phase clock-generator supplies another pulse to the clocksquare-wave generator.

The low input voltage sensor circuit output is logic 0, when and only when the line voltage is above 200V. Below 200V it is logic 1 . The output of LIVS is inverted, passed through a DFF and then supplied to one input of each NAND-gate.

The timing diagram has been shown in the figure 5. The timing diagram has been prepared with respect to the block diagram of fig. 2. AC input voltage at different phases is shown at the top of the diagram. Outputs of the rectifiers are shown at a1, a2, a3 and a4. D.C. reference voltage is shown below. When voltages at a1, a2, a3 and a4 are higher then the reference voltage, output of the comparators are logic 1(on) as shown at A1, A2, A3 and A4. Clock phase 1 and 2 are shown at Ø 1 and Ø2. Reset-set flipflops are set and reset as shown at B1, B2, B3 and B4. When any comparator output is at logic 1 (on), output of the SR flipflop connected to that comparator is also at logic 1(on). D flipflop output is at logic 1(on) or logic 0 (off) as shown at C1,C2,C3 C4, C5, C6, C7 and C8. When any SR flipflop output is at logic 1, the D- flipflop connected to SR flipflop has also logic 1 at its output. The final outputs of the control circuit are shown at D1, D2, D3, D4 and D5. Then clock square wave generator output, Low input voltage sensor output and the driver inhibit outputs are shown.

The truth table of the control logic circuit has also been shown in fig.-6. Conditions for the input voltage are marked as very low, low,normal, high and very high. For comparators and flipflops logic 1 is on and logic 0 is off. For NAND gates logic 1 is 10V and logic 0 is 0V. After the inverter logic 1 is -10V and logic 0 is 0V. When all the inputs to a NAND gate is logic 1 (10 V), it's output is logic 0 (0V). If the input to the inverters is logic 0(0V), its output is logic 1 (-10V) and if the input is logic 1 (-10V), it's output is logic 0 (0V). At the inverter positive logic is converted to negative logic.

TIMING DIAGRAM

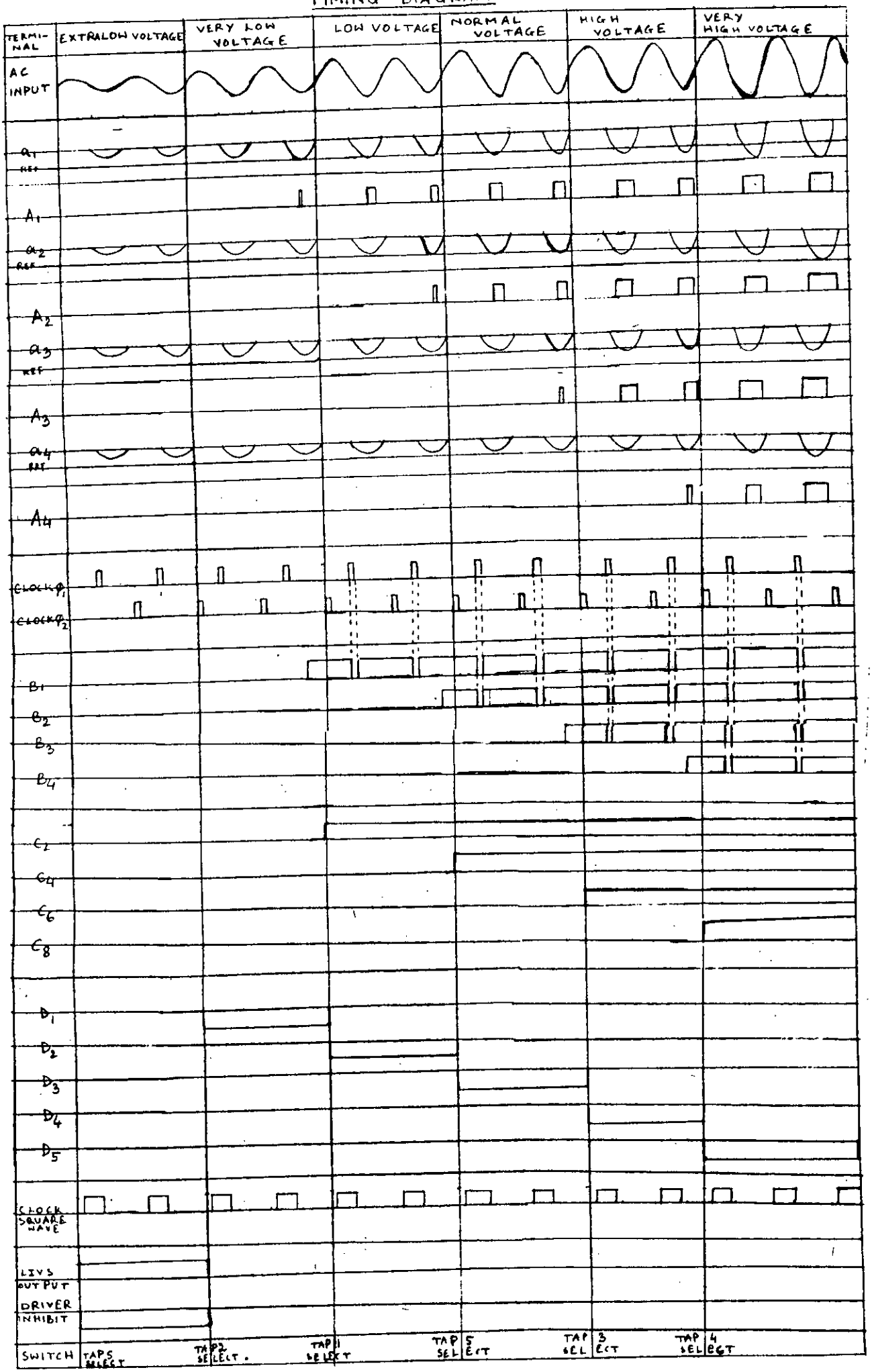


FIG. 6

TRUTH TABLE

TERMINAL / VOLTAGE CONDITION	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	D_1	D_2	D_3	D_4	D_5
VERY LOW	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	0	0
LOW	1	0	0	0	1	0	0	0	0	1	1	0	1	0	1	0	0	1	0	0	0
NORMAL	1	1	0	0	1	1	0	0	0	1	0	1	1	0	1	0	0	0	1	0	0
HIGH	1	1	1	0	1	1	1	0	0	1	0	1	0	1	1	0	0	0	0	1	0
VERY HIGH	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	0	0	0	1

FIG·6

1.4 CONSTRUCTION OF THE REGULATOR.

The regulator system is constituted with the following sections:

1) Input attenuator and rectifier.

2) Comparators.

3) R-S flipflops.

4) D-Flipflops.

5) NAND-gates.

6) Control power supply.

7) Clock-squarewave generator.

8) Two phase Clock generator.

9) Low input voltage sensor circuit.

10) Power module.

11) Lineloss and overvoltage protector circuit.

12) Tap changing transformer.

CHAPTER - II

2-1. OPERATION OF EACH SECTION OF THE SYSTEM

2-1. OPERATION OF EACH SECTION.:

2-1.1. Input attenuator and rectifier:

The input line voltage is attenuated by a single resistance attenuator which is used to reduce the amplitude of the input waveform. It is half wave rectified for negative half cycles of the input line voltage. It is then applied to the input comparators where it is compared with a dc reference voltage.

2-1.2 Comparators:

The input comparators generate a high (1) output if the negative peak of the input line voltage goes more negative than a preset value. There are four input comparators. Two are low-tripoint and the other two are high tripoint comparators. These are used to convert analog input signal to digital output signal.

2-1.3. R-S flip flops:

The signals from the input comparators are high (1) only for the time that the instantaneous value of the input voltage is more negative than a preset level. For this reason, data storage is provided by RS flip-flops which stores data from the comparators. The flipflop is set by a high signal from the comparator and reset by clock-phase 1 at the start of each negative half cycle of input line voltage. There are four RS flipflops.

2-1-4 D-flipflops:

D-flipflops store data from RS-flipflops. D-flipsflops provide a second level of data storage. The D-flipflops are clocked by Clock-phase 2 in such a way that they can only change state (1) when a new tap is to be selected and (2) then only the input line voltage reaches the proper value.

2-1-5 NAND-gates:

5-input NAND-gates are used because 5 transformer taps are to be provided. The output of any NAND-gate is low only when 5-inputs are high. Outputs of four D-flipflops are eight in number and distributed to 25(twenty five) input terminals of 5(five) NAND gates. The combination is in such a way that only one NAND gate will have low-output at a time and others will have high simultaneously.

2-1-6, Control Power Supply:

The control power supply (1) provides operating power to all stages, (2) generates a dc reference voltage that is used in various parts of the system and (3) provides a phase reference signal to the clock squarewave generator.

2-1-7. Clock-square wave generator:

The clock square wave generator is a comparator that compares the line phase signal with a dc reference voltage. It generate a rectangular wave that goes low shortly after the positive to negative zero crossing of the input line voltage. It's output goes high little time prior to the negative to positive

zero crossing of the input line voltage. The clock squarewave generator drives the two-phase clock generater.

2-1·8. Two-phase clock generater:

The phase 1 clockpulse is generated when the clock-square wave generater output goes low. The phase 2 clockpulse is generated when the clock square wave generaters output goes high.

2-1·9. Low input voltage sensor circuit:

The low input voltage sensor circuit senses the output voltage of the control power supply. It's output is high if the supply voltage is too low to run the control circuit. This signal is inverted and sent to D-flipflop. This data is clocked by clock-phase 2. It is then sent to NAND gates where it inhibits normal tap-switch drive. It also opens the contact K1 which forces selection of tap 5, shorting out the transformer.

2-1·10. Power Module:

SCRs are connected inverse parallel to switch the taps of the regulating transformer. The SCR power module consists of five solid state switches those correspond to five taps on the regulating transformer.

2-1·11. Line loss and overvoltage protector circuit:

Lineloss circuit operates when there occure an unbalancing due to short circuit or open circuit in the regulator or in the load system. When the unbalancing occure due to overvoltage in any phase, over voltage circuit will operate.

When the unbalancing is due to short-circuit, open circuit or low voltage in any phase of the system, only linalease-circuit will operate.

CHAPTER - III

3-1. DESIGN OF THE INPUT ATTENUATOR & RECTIFIER SECTION.

3-2. DESIGN OF THE COMPARATOR SECTION, LOGIC CIRCUITS AND THE DRIVER.

3-3. DESIGN OF THE POWER MODULE,

3-4. DESIGN OF THE REGULATOR TRANSFORMER AND THE POWER SUPPLY TRANSFORMER.

3-5. DESIGN OF THE CLOCK-SQUARE WAVE GENERATOR AND THE TWO-PHASE CLOCK GENERATOR.

3-6. DESIGN OF THE LOW INPUT VOLTAGE SENSOR CIRCUIT.

3-7. DESIGN OF THE POWER SUPPLY SECTION.

3-8. DESIGN OF THE LINELOSS AND THE OVER VOLTAGE PROTECTOR CIRCUIT.

3-1. DESIGN OF THE INPUT ATTENUATOR AND RECTIFIER SECTION:

The designed circuit for input attenuator and rectifier is shown in figure-7. In the first half cycle of the ac power supply, current will flow only through the diode CR and the resistor R. In the second half cycle, current will be opposed by the diode and will flow through the variable resistors VR1, VR2, VR3, VR4 and the fixed resitor R. We can get various outputs from these variable resistors for inputs to the comparators. Let us take 250V for design calculations which is the upper limit for regulation. Voltage at point B of the circuit is abritrarilly chosen to be 50V, power rating for resistors is 1W arbitrarilly chosen. ½W power dissipation is considered through the resistor for safety. P = VI (Power factor consideration is not important, here.) For the case when the diode is forward biased.

$\frac{1}{2} = 250 \times I$

$I = 2$ mA

$V = RI$

$250 = R \times 2 \times 10^{-3}$

$R = 125K.$

For the case when the diode is reverse biased, the current will be equally shared by 4 variable resistors. 20K variable resistors are chosen arbitrarily for the purpose. Total resistance = 20/4 = 5K, current = 250/130 = 1.9 mA. which will be equally shared by four variable resistors. Now, we can tap different voltages from the variable resistors.

INPUT ATTENUATOR AND RECTIFIER.

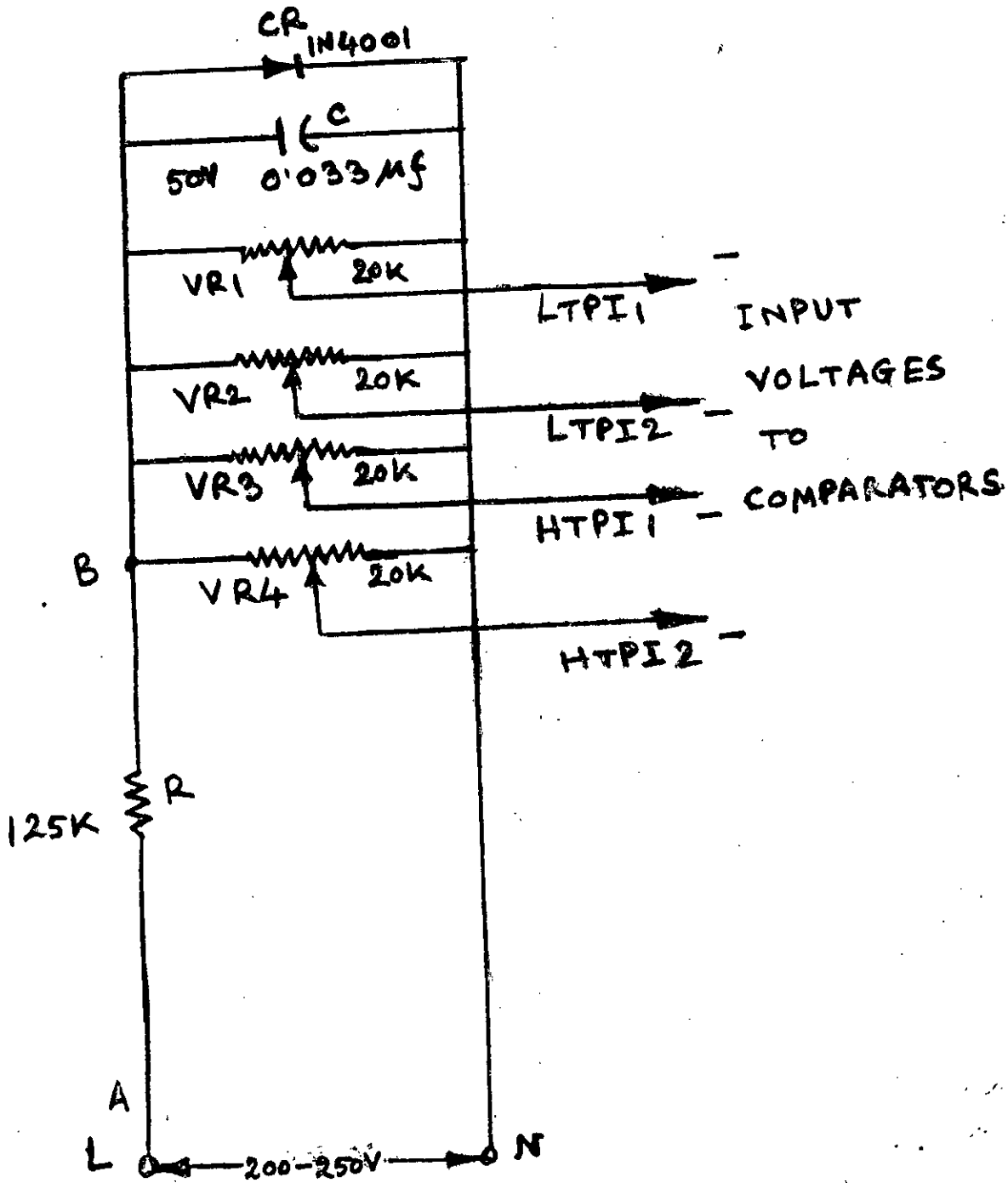


FIG. 7

3.2. DESIGN OF THE COMPARATORSECTION, LOGIC CIRCUITS AND THE DRIVER.

We take the reference voltage, VR = -6.2V.

So, Input voltage, Vi must be greater than -6.2V to get an output terminal change.

For our design, we can consider the relation.

$$Vi = VR. \quad [2]$$

As the reference voltage is negative, we must rectify negative halfcycle of the *Sinusoidal ac* input. Negative half cycle is rectified for the advantage of having a common earth line for both d.c. and ac. currents.

[3,4]

We can take the help of truth table to design the logic circuits.

Number of comparators= 4 (four), Number of RS- flipflops = 4 (four), Number D-flipflops = 4 (four).

Number of NAND-gates = 5 (five).

The truth tables are shown in fig. 8. The timing diagram is shown in fig. 9. 5 input NAND-gates are selected, because we shall regulate the voltage at 5-different phases i.e. 200-210-230-240-250V. The RS flipflops and the D-flipflops are shown in fig. 10. NAND-gate connections are shown in fig.11.

SET-RESET TRUTHTABLE

S	Clk	Q	$\overline{Q}$
0	0	Previous	Previous
0	1	1	0
1	0	0	1

DELAY TRUTHTABLE

Cr	$\overline{Q}$	U	D	Q	Ck	V
1^*	0	1	0^*	1_*	0^*	1
1^*	1	1	0^*	0	1^*	0
1^*	0	0	1^*	1_*	1^*	1
1^*	0	1	1^*	1_*	0^*	1

FIG. 8.

TIMING DIAGRAM

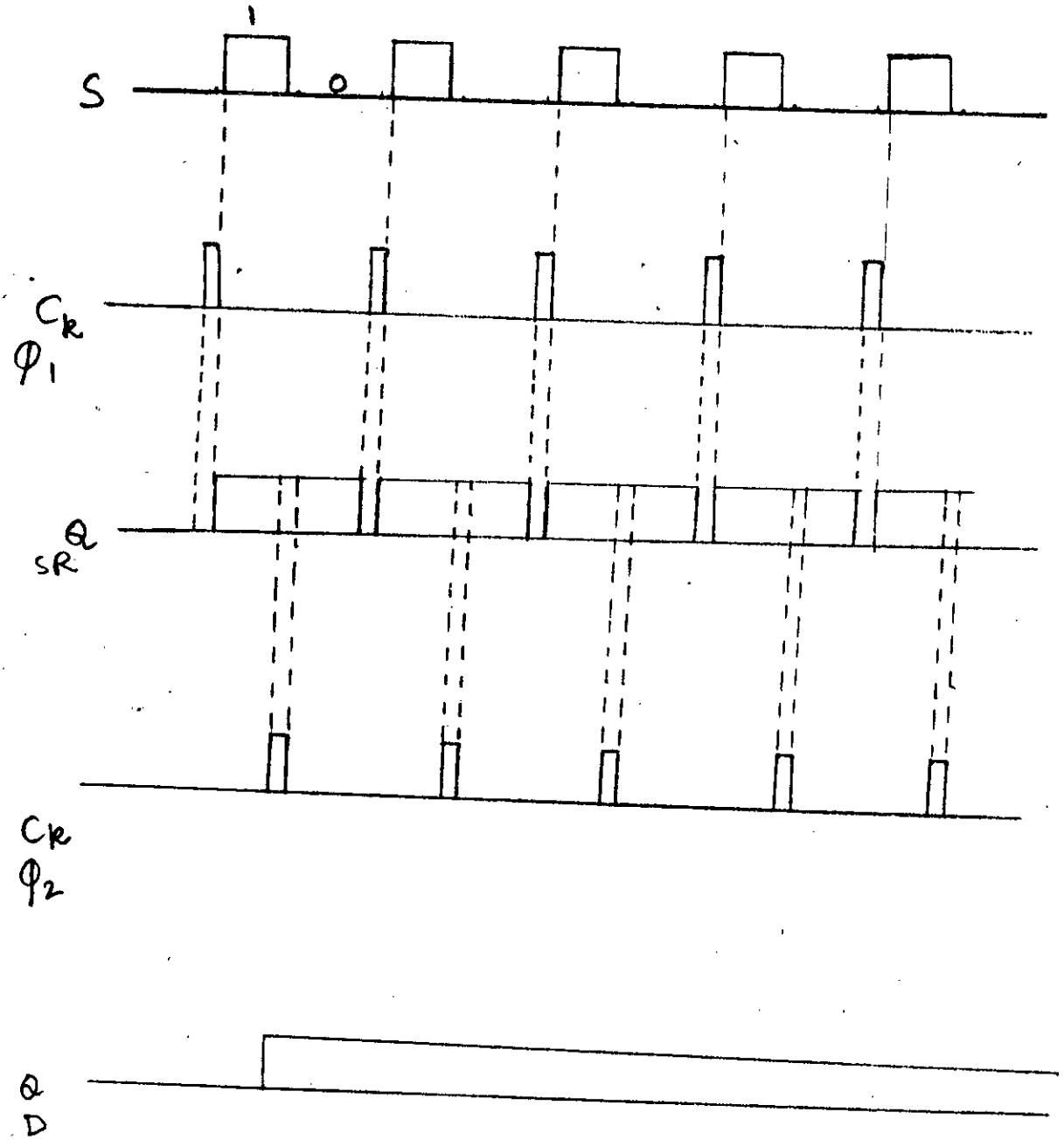
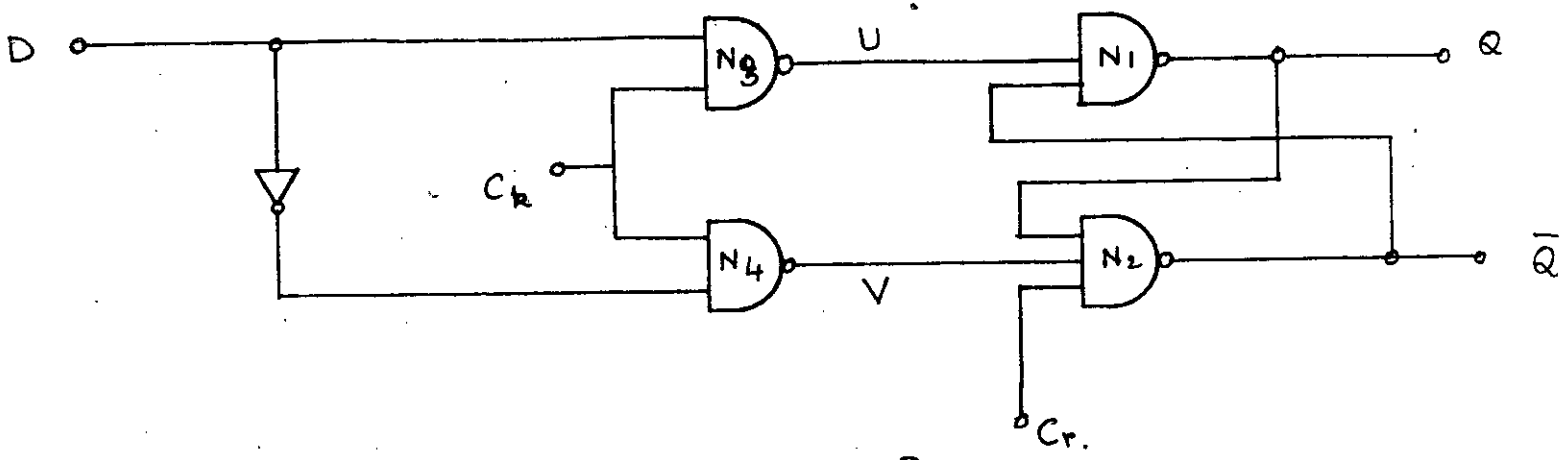
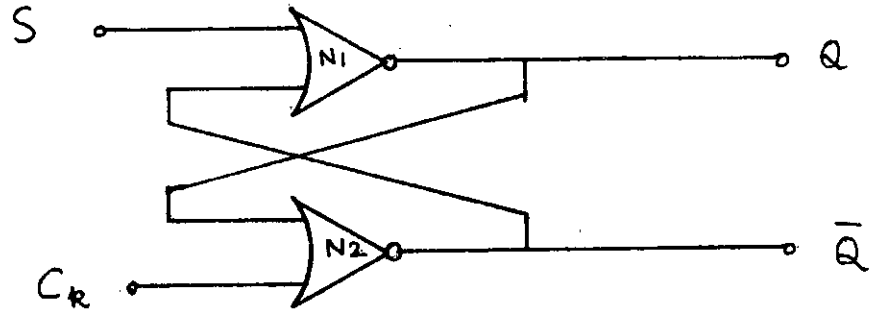


FIG. 9.

DELAY FLIPFLOP



RESET-SET FLIPFLOP



FIG·10

NAND GATE CONNECTIONS

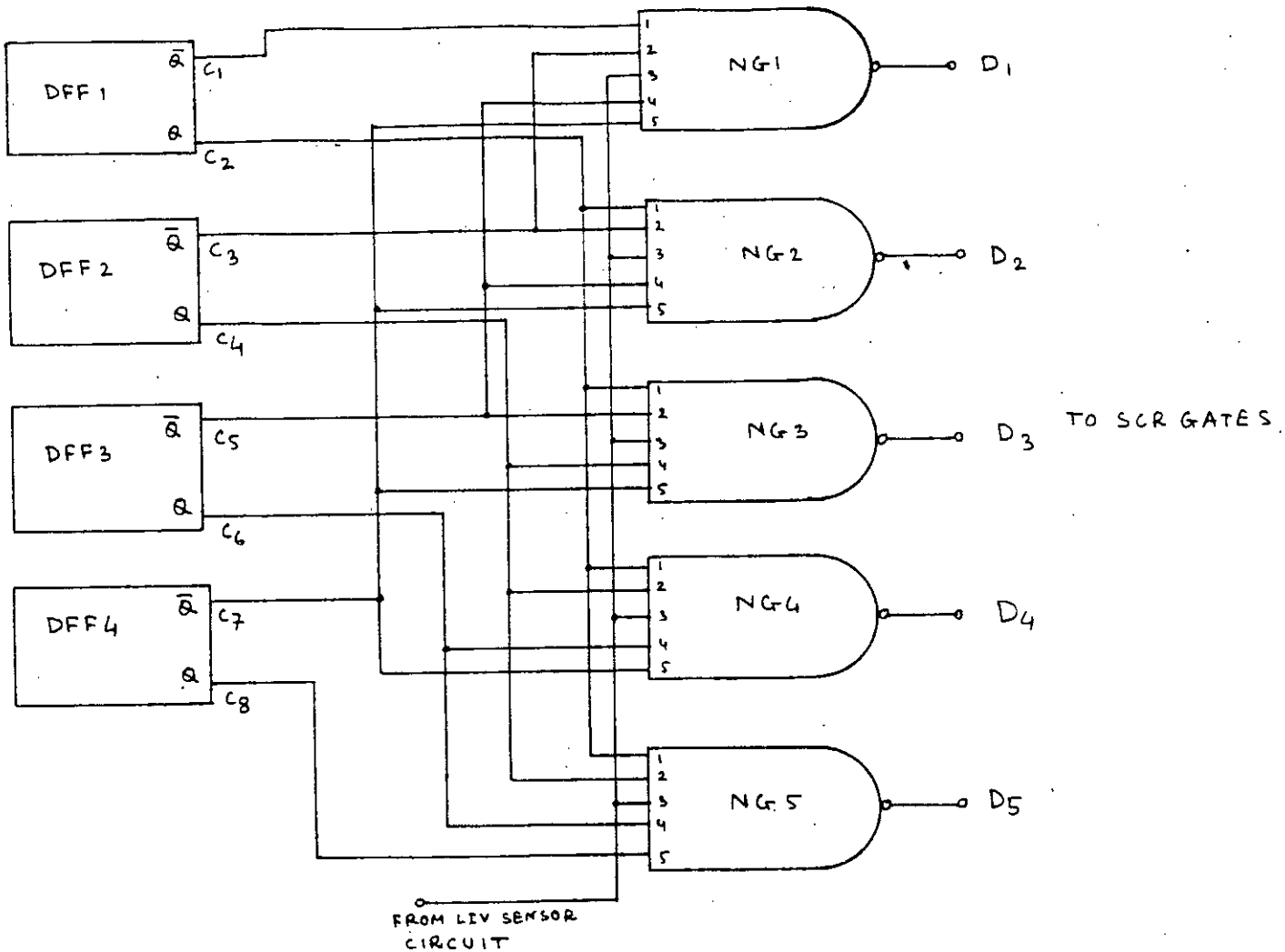


FIG.11

3.3 DESIGN OF THE POWER MODULE:

We designed the regulator as 1KVA rating. Maximum current to be drawn is $\frac{1000}{240}$ = 4.2A. So, we select the SCRs and Triacs of 9A rating.

Let us first design the circuit, then we shall calculate the component values. The circuit is first developed as shown in fig.12. [4]

When tap 1 is to be selected , the control assembly draws a negative current from the gate of Q_2. This turns Q_2 on and current flows from E_6 through Q_2 to the gate of Q_3. This turns Q_3 on. When Q_3 turns on, it provides a path for gate current for either Q_1 or Q_4, depending on the polarity of the voltage at E_1. If E_1 is positive, gate current flows from E_1 through CR1 and Q_3 to the gate of Q_4. If E_1 is negative, gate current flows from E_{16} (earth) through CR2 and Q_3 to the gate of Q1. C_1 and R_4 form a snubber that protect the circuit from high dv/dt. [5,6]

Taps 2, 3 and 4 operate in the same manner. But Tap 5 operate in a different manner. When normal line voltage is present, Tap 5 is to be selected. Tap 1 is selected to step up low voltage 210V to 220V. Tap 2 is selected to step up very low voltage (200V) to 220V. Tap 3 is selected to step down high voltage (230V) to 220V. Tap 4 is selected to stepdown very high voltage 240V to 220V. Tap 5 is selected , when normal line voltage (220V) is present.

Tap 5 which is connected to E5 must be turned on at all times when the control power supply voltage is too low for proper operation and when normal line voltage is present (220V). This tap is selected, when the control

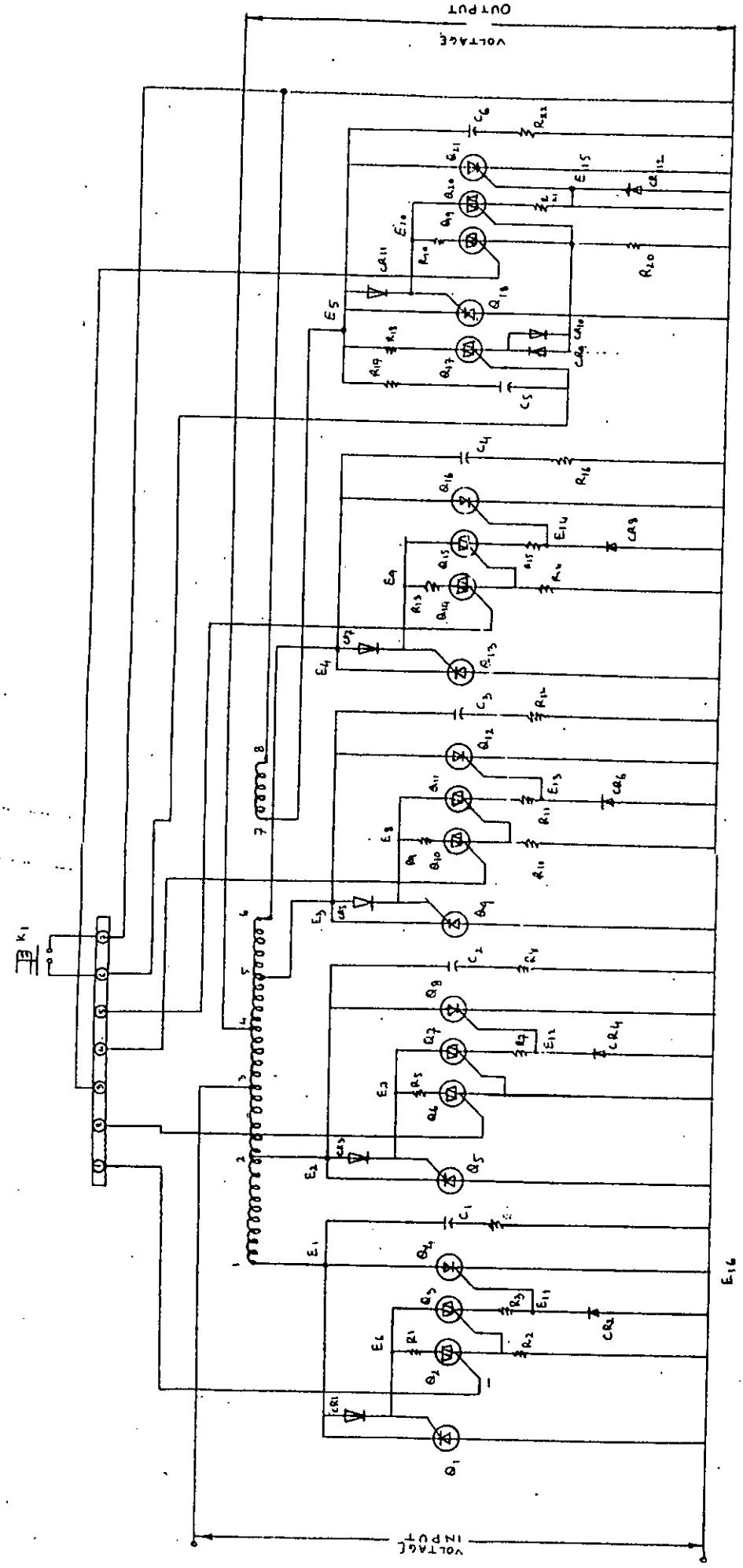


FIG. 12

E1 – SELECTED FOR VERY LOW VOLTAGE CONDITION
E2 – " " LOW " "
E3 – " " HIGH " "
E4 – " " VERY HIGH " "
E5 – " " NORMAL " "

power supply is coming up and when the input ac voltage is below rated minimum (below 200V). When normal line voltage is present the contact switch K1 shorts the gate of Q17 to ground. When the control power supply voltage is below rated minimum, K1 remains open. Gate current is then provided to Q17 from E5 through R17 and C5. This turns Q17 on which turns Q20 on which in turns Q18 and Q21 on, alternately.

We first consider the current limiting resistors, To limit the current through diodes and Triacs to 1mA, we should use the resistor value as $\frac{250}{10^{-3}} = 250$ kohms. Resistor of 250 kohms is available, So, 250 kohms 1/2 w resistors are used. Diodes CR1 and CR2 are designed for 1A 500V rating. For snubber circuit, let us take 1 μsec time constant. [1]

So $10^{-6} = RC$.

Let us consider a very low resistance e.g. 10 ohms.

So, $10^{-6} = 10C$

or, C = 0.1 uf.

Voltage rating should be approximately 500V.

So, 0.1 uf, 500V, which are available are used.

The circuits for taps 2, 3, 4 and 5 are to be of the same design as the circuit for tap 1.

3-4. DESIGN OF THE REGULATOR TRANSFORMER AND THE POWER SUPPLY TRANSFORMER.

3-4.1. The design sheet for the regulator transformer is given below:

DESIGN SHEET

W = KW output = KVA output = 1.

Primary voltage = 200V, Secondary voltage = 220V,	very low voltage condition (tap 2 select)
Primary voltage = 210V, Secondary voltage = 220V,	Low voltage condition (tap 1 select)
Primary voltage = 220 V, Secondary voltage = 220V,	Normal voltage condition (tap 5 select)
Primary voltage = 230 V, Secondary voltage = 220V,	High voltage condition (tap 3 select)
Primary voltage = 240 V Secondary voltage 220V,	Very high voltage condition (tap 4 select).

CALCULATIONS

Empirical formula [19]

Volts per turn, $E = \frac{W}{100(S+1)} = \frac{1000}{100(5+5)} = 1$

So, turn per volt = 1

Current density = 800A/Sq. in for copper.

Cross-section of the wire per ampere = $\frac{1}{800}$ = 0.00125 sq.in.

Ampere rating of the transformer = $\frac{1000}{200}$ = 5A.

Cross-section of the wire = 0.00125x5 = 0.00625 sq. in. or 13 SWG.

The cross-section of the core is shown in fig. 13.

$W^2 + L^2 = C^2$

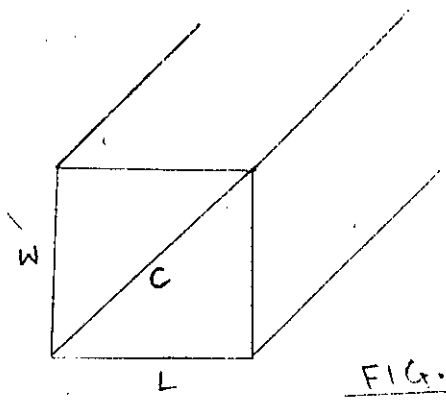


FIG. 13

When the cross-section is squre,

$W^2 + W^2 = C^2$ or, $2W^2 = C^2$ or $W = C/\sqrt{2}$. [12]

Cross sectional area is given by the formula,

$$A = \frac{E \times 10^8}{25.8fF\,B}$$

Where A = cross-section in sq.in.

E = volts per turn.

f = frequency in Hz.

B = Magnetic flux density in gauss

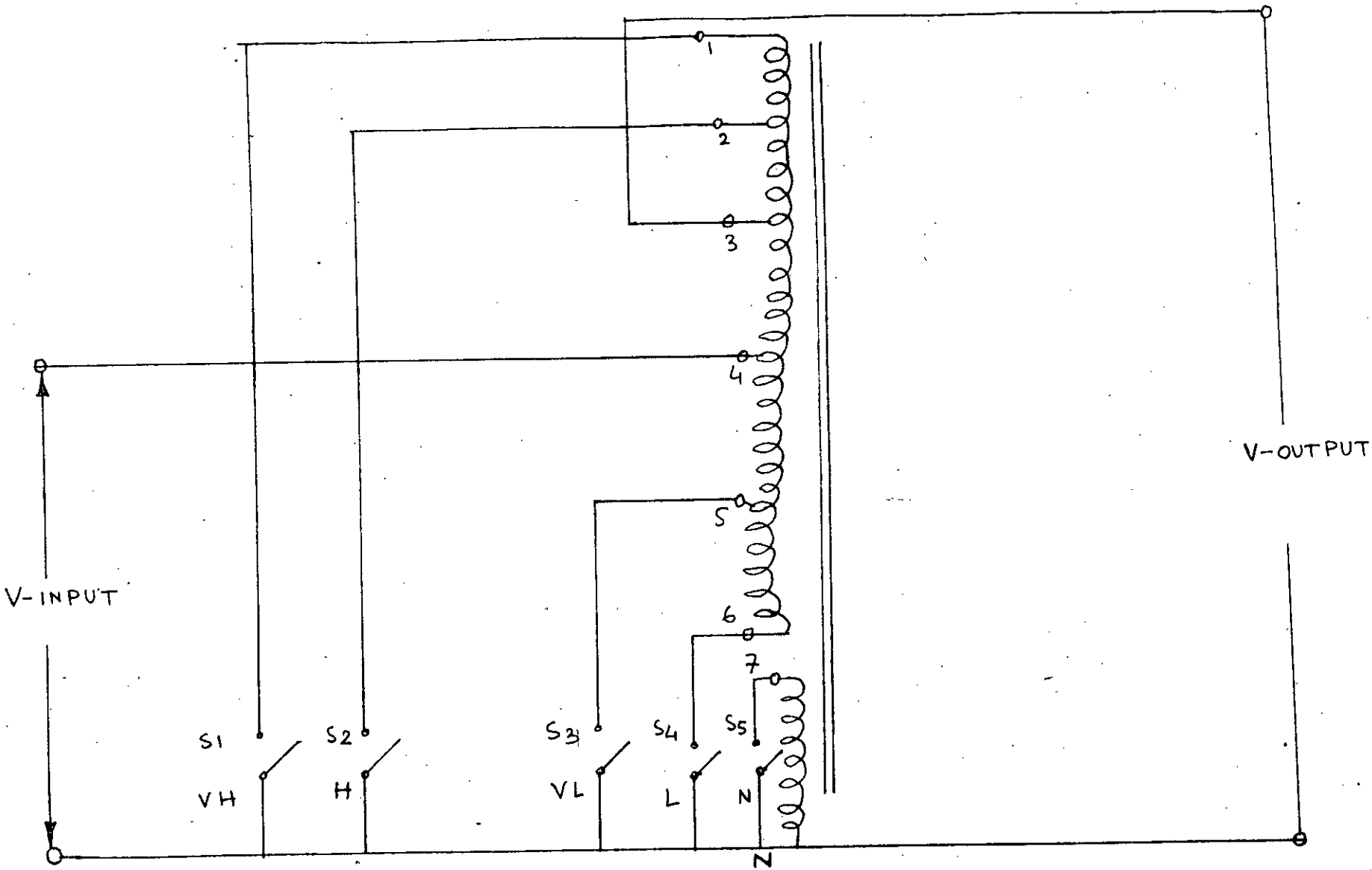
F = form factor = 1.11.

Here, B = 12000 gauss.

$$A = \frac{1 \times 10^8}{25.8 \times 1.11 \times 50 \times 12000} = 5.8 \text{ sq. inch.}$$

The labelled sketch and the regulating circuit of the regulator transformer is shown in fig. 14.

TRANSFORMER TAPPING



FIG·14

Sl. No.	Summary of Calculations

1 Volts per turn, V_t = IV

2

Tap points	1-2	2-3	3-4	4-5	5-6	7-8
Windings						
No. of turns	10	220	10	220	10	20

3 No. of coils = 2 (One is the multitap autotransformer and other is the auxiliary secondary winding). [11]

4 Turns per coils = The multitap autotransformer portion has been designed for 470 turns and the auxiliary secondary winding portion has been designed for 20 turns.

5 Current density, A/S qr. in. = 800

6 Cross section of Conductor = 0.00625 sq. in.

7 Dimension of the conductor = 13 SWG

8 Cross-section of the core = 5.8 sq.inch.

9 It is a transformer of approximately unity turns ratio, so HT and LT conductor sizes are the same.

3.4.2. The design sheet for the power supply transformer is given below.

DESIGN SHEET

VA output = 100.

Primay line voltage = 235 V

Secondary tap points = 15V, 30V, 125V.

The labelled sketch of the power supply transformer is shown in fig. 15.

Cross-sectional area, [2] $A = \frac{\mathcal{E} \times 10^8}{25.8\ f\ B}$ Sq. in.

Here, B = 12000 gauss.

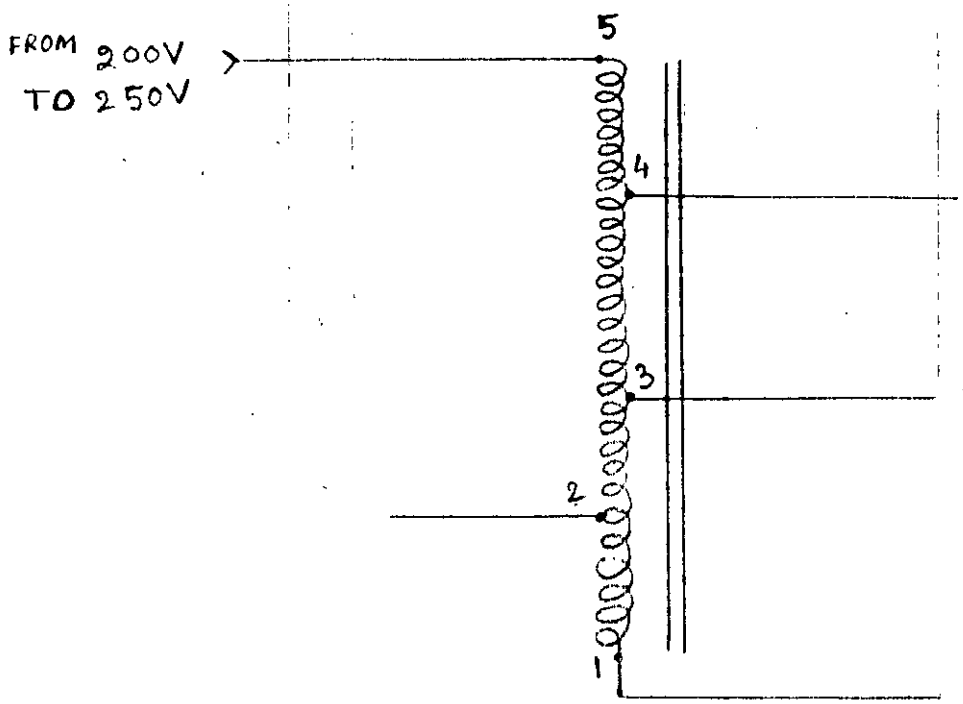
So, $A = \frac{0.2 \times 10^8}{25.8 \times 1.11 \times 50 \times 12000}$ = 1.2 sq.inch.

From current density for copper,

Cross-section of wire = 0.00125 x 0.5

= 0.000625 sq. in.

Size of the wire, SWG = 22.



FIG·15

Sl.No.	Summary of Calculations				
1	Volts per turn, V_t = 0.2				
2	Total no. of turns	1-2	1-3	1-4	1-5
		75	150	625	1175
3	Cross-section of the wire, Sq. in. = 0.000625 SWG = 22				
4	Cross section of the core = 1.2 sq. in.				
5	It is an autotransformer, so the conductor size is the same throughout. [9,10]				

Supply to 5(five) ICs require 500 mA or 0.5A, considering 100mA for 1 IC.
Power, W = 220V x 0.5 = 110W - 100W $\simeq$ 100VA. [1]

Empirical formulae, $E = \frac{W}{100\ (5+1)} = \frac{W}{100\ (5+0.5)} = \frac{W}{550}$

or, $\frac{W}{550}$ volts/turn = $\frac{100}{550}$ = 0.18 V/turn $\simeq$ 0.2 V /turn.

So, turns per volt = $\frac{1}{0.18}$ = 5.5 $\simeq$ 5T/Volt.

So, for 235V, No. of turns = 5 x 235 = 1175
for 125V, No. of turns = 5 x 125 = 625
for 30V, No. of turns = 5 x 30 = 150
for 15V, No. of turns = 5 x 15 = 75

3-5. DESIGN OF THE CLOCK-SQUARE WAVE GENERATOR AND THE TWO-PHASE CLOCK GENERATOR:

The circuit design is shown in figure -16

The clock squarewave generator is a monostable multivibrator. [2]

A comprator is used, where reference of 6.2V is applied to the inverting terminal. AC voltege of 10V rms i.e. 14.1V maximum value (≃ 15V) is applied at the non-inverting terminal. MC3302IC is used. C_6 is designed to

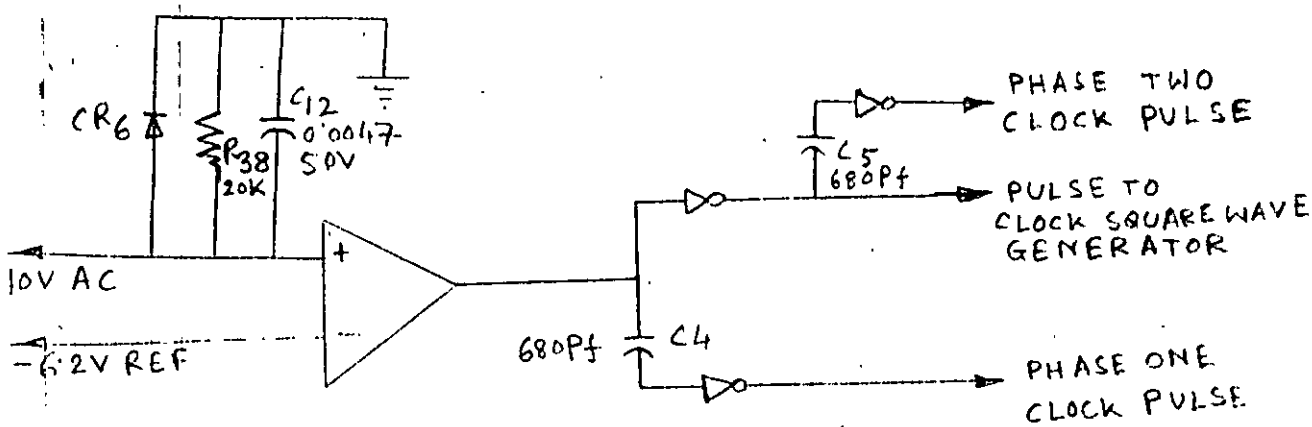


Fig.16

have the value 0.1 uf 600V and R_{32} = 1 ohm ½ W. Time constant $0.1 \times 10^{-6} \times 1$ = 0.1 u sec.

CR 7 is selected for 1, μf, 250V. It is used not to short (-10V) line to input signal. In the first half cycle current flows from the line through CR_5 to earth. In the Second half cycle, current from earth through C_6, charging the capacitor. Again in the next half cycle, the capacitor discharges. The capacitor C_6 will continue to be charged till the voltage reaches the reference voltage. Diode CR10 is provided not to short (-10V) line to inverting terminal. The trigger pulse $\phi 3$ is given to change state of the monostable multivibrator. [3]

The two phase clock generator is constructed by inverter and capacitors. [4] The capacitor will be charged and discharged only around rising time and falling time of the squarewave and pulses are produced. Very low time constant is designed

se, 680PF capacitors are selected, Resistors to earth are selected for low values. The pulses generated are shown in the timing diagram.

3.6. DESIGN OF THE LOW INPUT VOLTAGE SENSOR CIRCUIT:

The designed circuit is shown in fig. -17.

The low input voltage sensor circuit is also a comparator. Reference of 3.3V is applied to the inverting terminal and 10V d.c. is applied to non-inverting terminal of the comparator. Operation al amplifier of the comparator has got R_{25} the bias resistor of value 20K and by pass capacitor of 0.1 uf 50V. R27 is of value 39K is the short between output and the non-inverting terminal and is provided to make the gain of the comparator unity. R_{26} is also the bias resistor of 5K. Diode CR8 is for protection of the circuit, CR_{13} is of value 4.7/μf 10V, electrolytic capacitor to make the reference constant over very quick changes. [2, 3]

Capacitor C_3 1 uf 370V paper type is used to prevent ac to come to dc line, because both ac and dc supply have got the same earth. Resistors R_{16}, 17 and 18 are of value 100 k 1/2W and are provided for earthing the inverters. [4]

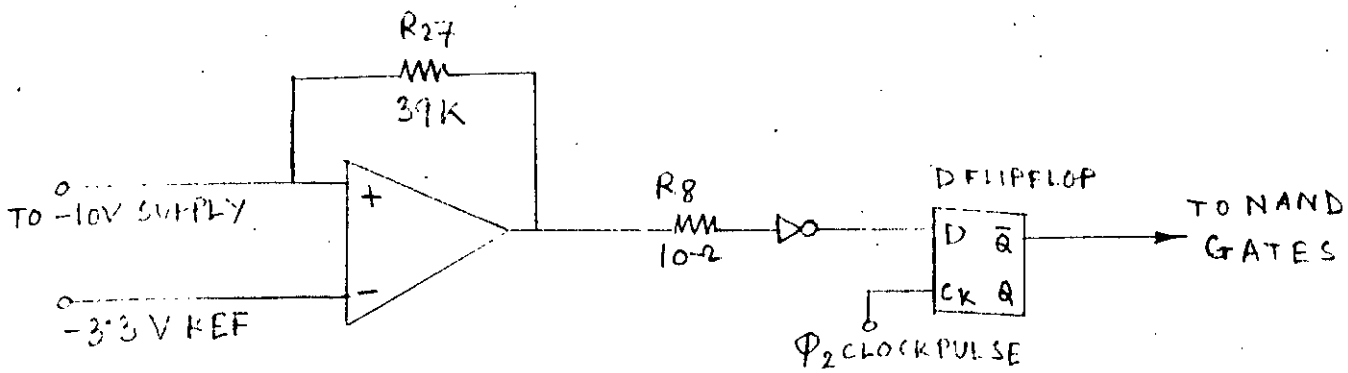


Fig.17

3-7. DESIGN OF THE POWER SUPPLY SECTION:

The designed circuit is shown in fig. 18.

This power supply circuit is designed for an output voltage of 10V. Diodes of 350V, 1A rating are selected. Diodes CR 10 and CR 11 from the fullwave rectifier. The rectified voltage is filtered by C_8 of value 200 uf 16V electrolytic. The voltage is regulated by the 10V zener diode CR_3. The Zener diode CR_4 is used for regulation of -6.2V which is applied as reference voltage to comparators and low input voltage sensor circuit. [15, 16] R_{22} is a 5K resistor is used to limit current through CR_4.

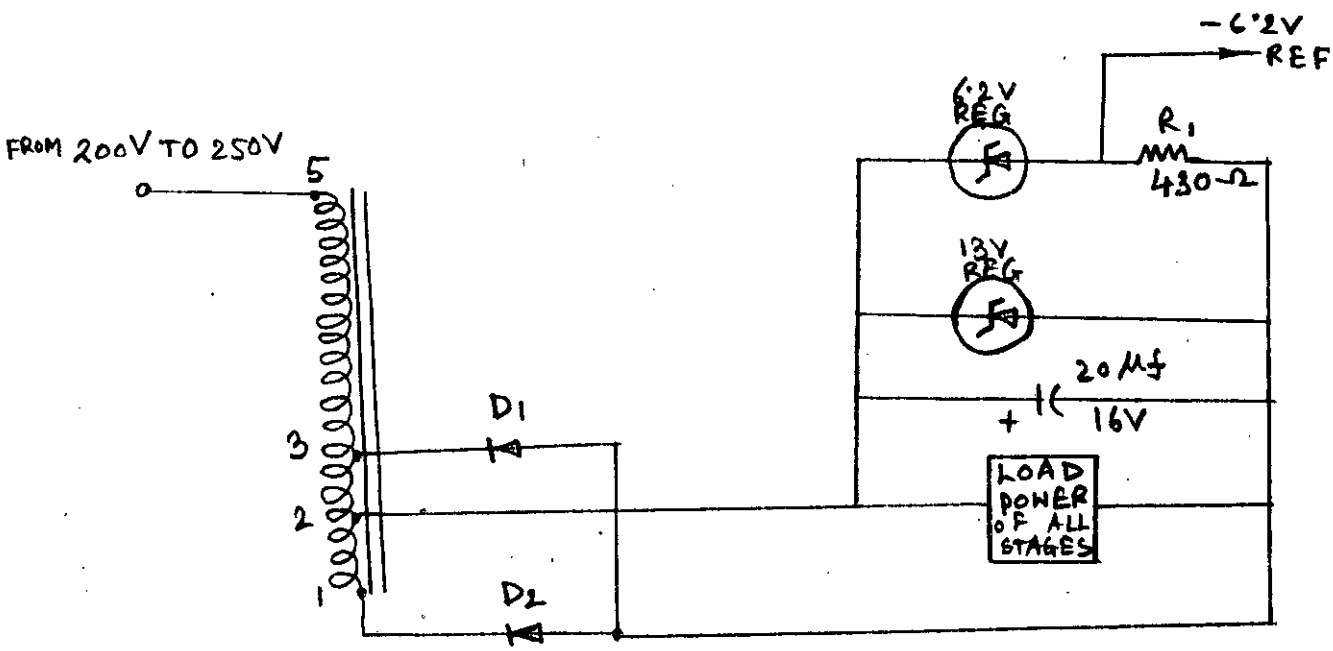


FIG. 18

3-8. DESIGN OF LINELOSS AND OVERVOLTAGE PROTECTOR CIRCUIT.

The complete lineloss and overvoltage protector circuit is shown in figure 19.

Lineloss circuit operates when there occurs an unbalancing due to short circuit or open circuit. When the unbalancing occurs due to overvoltage in any phase overvoltage circuit will operate. But when the unbalancing is due to short circuit, open circuit or low voltage in any phase, only lineloss circuit will operate.

3-8.1. DESIGN OF THE LINELOSS CIRCUIT:

A. Let us design the circuit for undervoltage, it will be sufficient. Because, the circuit, then, will surely operate for short circuit or open circuit. Let us design the circuit for say 5% under voltage in any phase.

So, phase voltage will be $220 \angle 0^\circ$ V $220 \angle 120^\circ$ V and $210 \angle 240^\circ$ V

The above figures have been taken by considering nominal phase voltage to be 220V (line voltage to be 380V) and only voltages impressed are unequal and voltages differ in equal phase angles.

For design purpose, let us consider R_1, R_2 and R_3 to be 100K, 1W. The figure is selected by trial and error method, taking into account the low reference (below 10V) of differential amplifier.[14]

$$I\,a'a = \frac{220 \angle 0^\circ}{100 \angle 0^\circ} = 2.2 \angle 0^\circ \text{ A.}$$

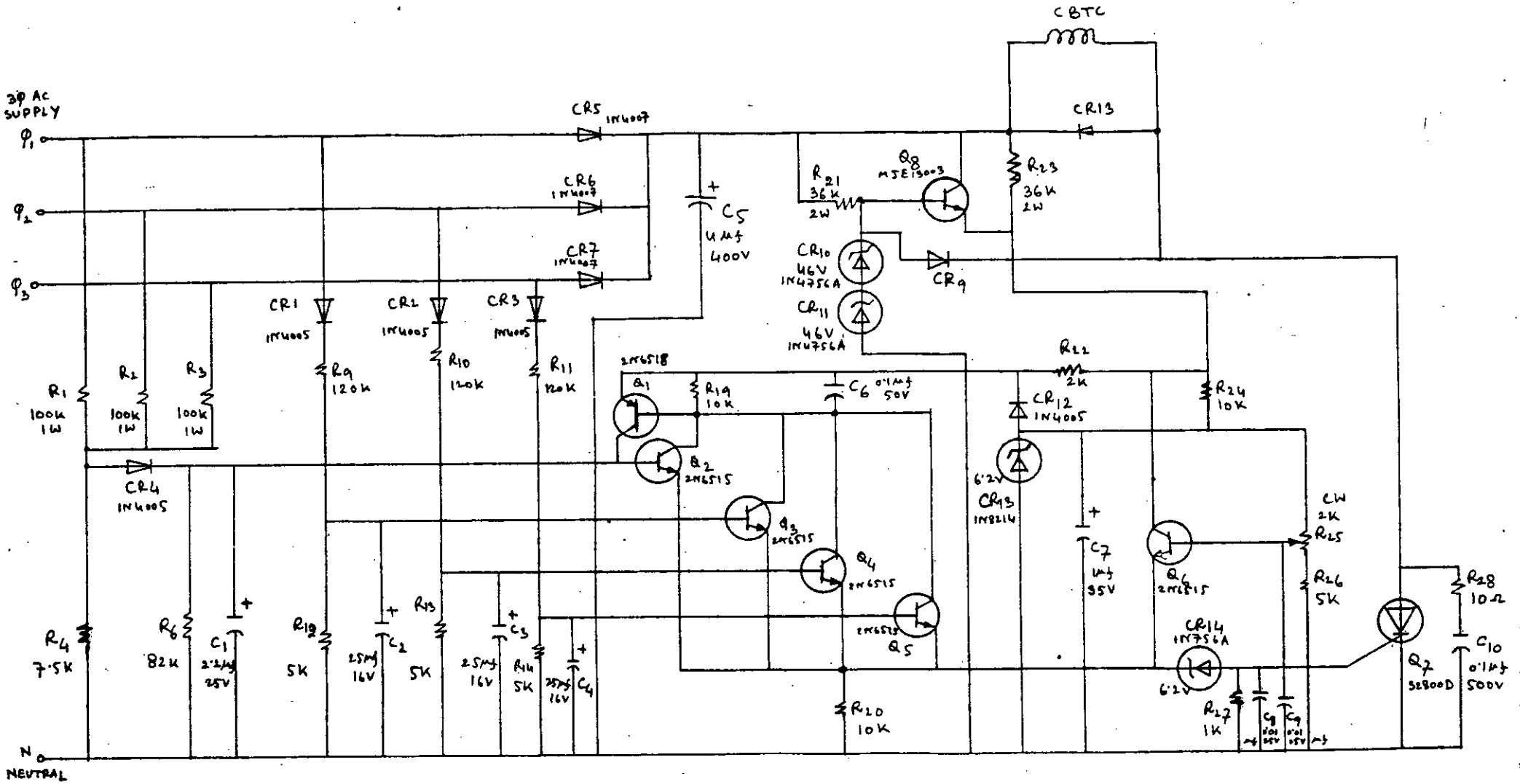
$$Ib'b = \frac{220 \angle 120^\circ}{100 \angle 0^\circ} = 2.2 \angle 120^\circ \text{A}$$

$$Ic'c = \frac{210 \angle 240^\circ}{100 \angle 0^\circ} = 2.1 \angle 240^\circ \text{A}$$

When voltages are balanced and consequently line currents are also balanced because of balanced three phase load,

$$Ia'a + Ib'b + Ic'c = 0$$

LINE LOSS AND OVER VOLTAGE PROTECTOR CIRCUIT



FIG·19

But when, the voltages are unbalanced and consequently currents are also unbalanced as calculated above, a current will flow through the path ng.

The circuit design is shown in fig. 20.

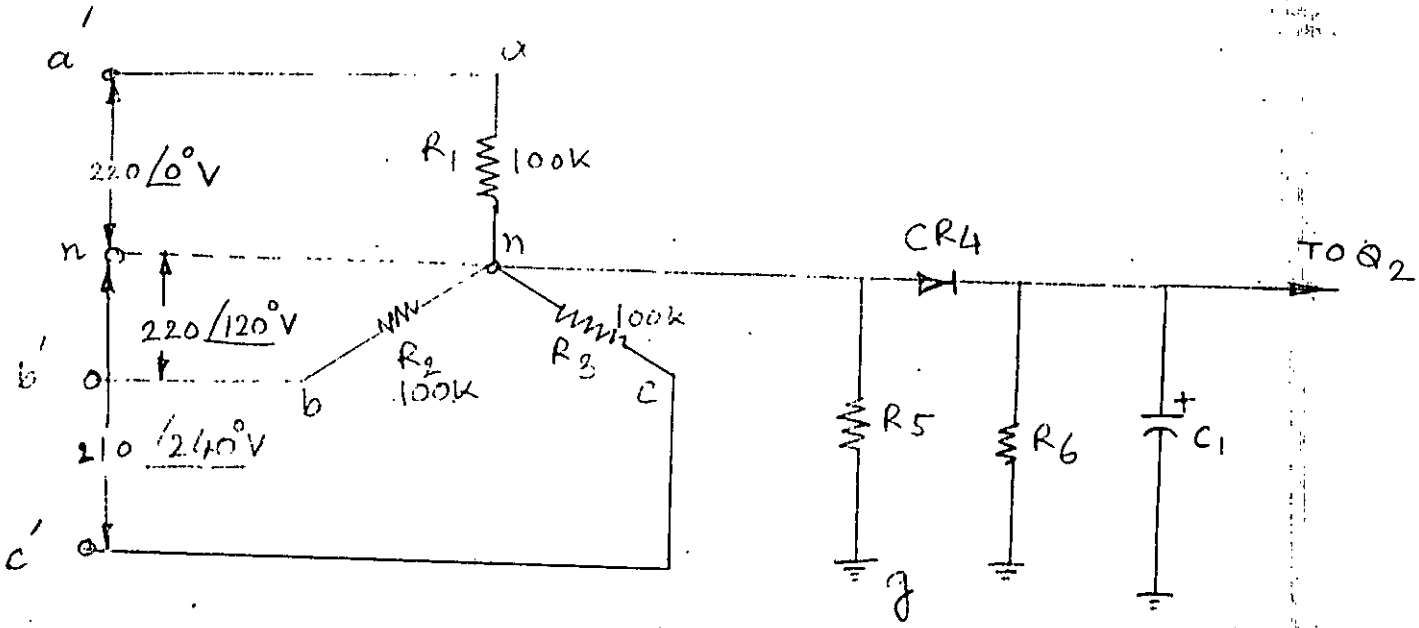


FIG. 20

The value of the current

$$I_{ng} = 2.2\angle 0^\circ + 2.2\angle 120^\circ + 2.1\angle 240^\circ$$

$$= 2.2 + j0 + 2.2(-0.5 + j0.866) + 2.1(-0.5 - j0.866)$$

$$= 2.2 - 1.1 + 1.91 - 1.05 - j\,1.82$$

$$= 0.05 + j0.09\ A$$

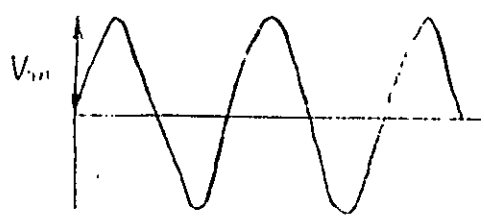
$$= \sqrt{0.05^2 + 0.09^2} \angle \tan^{-1} \frac{0.09}{0.05}$$

$$= \sqrt{0.0025 + 0.0081} \angle \tan^{-1} 1.8$$

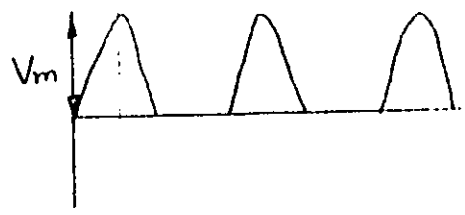
$$= \sqrt{0.0106} \angle \tan^{-1} 1.8$$

$= 0.103 \angle 60^\circ$ A, considering no resistance with the neutral.

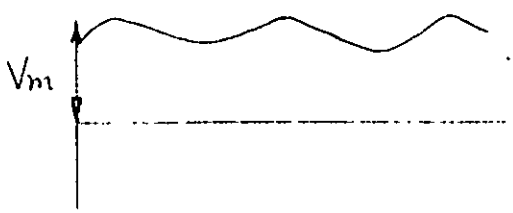
Let us consider, the reference voltage set for the differential amplifier to be 6.2V for design purposes. 6.2V Zener diodes are available. In order for the lineless circuit to operate, voltage after CR_4 must exceed 6.2V. Let us consider the voltage for our design purpose to be 6.2V, d.c. The ripple voltage is neglected for design purposes [15]. After rectification, the half-wave is maintained at maximum value by the filter capacitor C_1 as shown in figure 21.



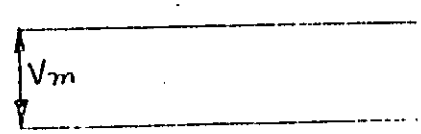
(a) VOLTAGE BEFORE CR4.



(b) VOLTAGE AFTER CR4 WITHOUT C1.



(c) VOLTAGE AFTER CR4 WITH C1 CONSIDERING RIPPLES.



(d) NEGLECTING RIPPLES.

FIG. 21

So, V_{max} = 6.2V and

Voltage before CR_4

$$V_{rms} = \frac{6.2}{2} = 4.4V$$

In order for the voltage to be developed at the node of R_1, R_2 and R_3 i.e. before CR_4, Resistance $R_5 = \frac{4.4}{0.103} = 43.1$ ohms $\simeq$ 45 ohms, 1/2W. To provide a path for negative half cycle, resistance R_6 is provided for the rectified value of R_6 is chosen so that 20% of current through R_5 will be drained. So, it will be 80% or 8 times the R_5 i.e. $R_6 = 45 \times 8 = 360$ ohms, 1/2W. In this case it is the load to the rectifier.

(a) CR_4 is selected of 250V rating which is available 1A capacity.

The formulae for filter capacitor is $C = \frac{796000}{3\ fR}$ uf

Where R = load resistance in ohms

f = frequency of ac supply.

c = capacitance in uf

$$f = \frac{796000}{3 \times 50 \times 360}$$

= 14.7 uf.

$\simeq$ 15 uf.

Since it is a filter capacitor , we selected it of electrolytic type and because the voltage is low, it of 25V rating.

(b) Taking 1mA current through the circuit, $\Delta v \simeq 10V$

$$C = \frac{I \Delta t}{\Delta v} = \frac{1 \times 10^{-3} \times 20 \times 10^{-3}}{10} = 2.0 \text{ uf.}$$

Design (b) is preferred.

(B) Now let us design the circuit for the situation when one phase is open circuited as shown in figure 22. For design we are required to assume some values, use some empirical formulae and some theoretically proved established formulae.

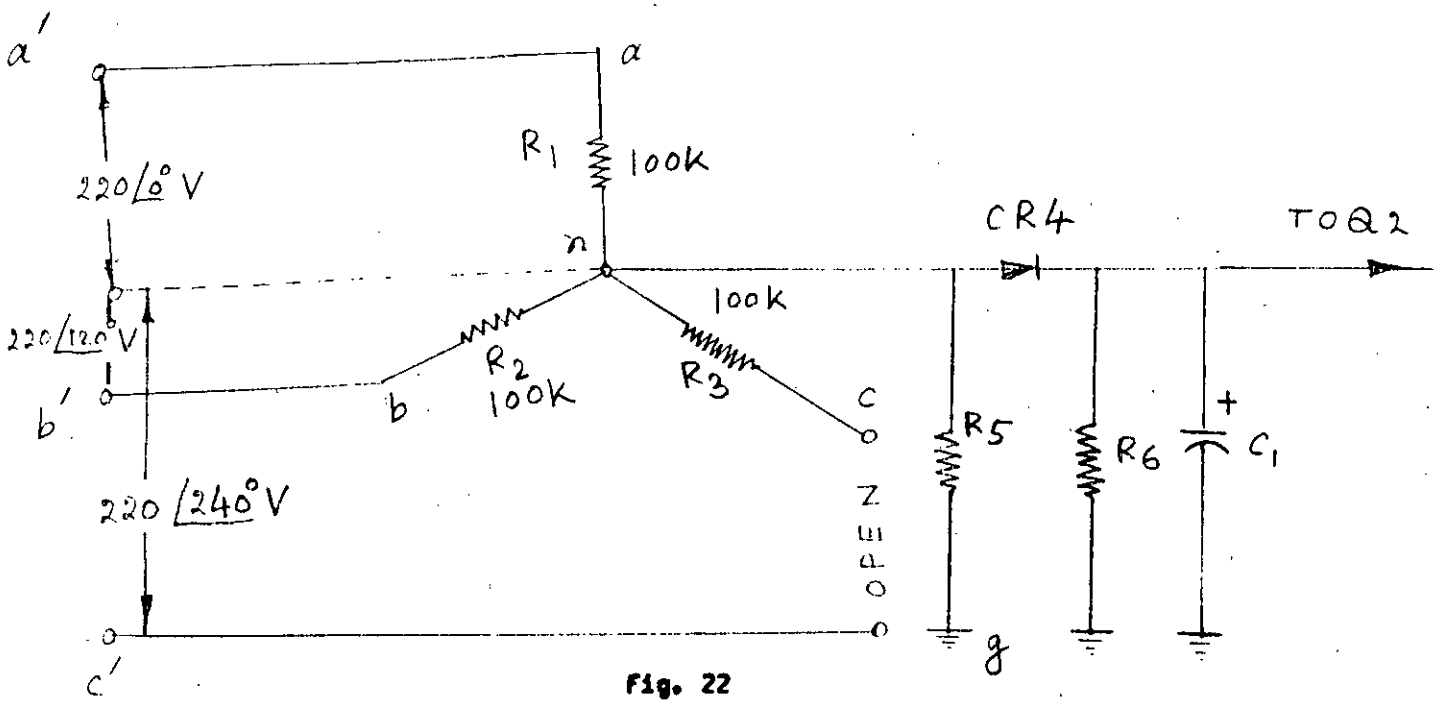


Fig. 22

$I_{a'a} = \frac{220/0^\circ}{100/0^\circ} = 2.2/0^\circ$ A

$I_{b'b} = \frac{220/120^\circ}{100/0^\circ} = 2.2/120^\circ$ A.

$I_{c'c} = 0$ A.

$I_{ng} = 2.2/0^\circ + 2.2/120^\circ = 2.2 - 1.1 + j1.91$ A

$= 1.1 + j1.91$

$I_{ng} = \sqrt{1.1^2 + 1.91^2} \tan^{-1} \frac{1.91}{1.1}$ A

$= \sqrt{1.21 + 3.65} \tan^{-1} 1.74$ A

$= \sqrt{4.86/60^\circ}$ A

$I_{ng} = 2.2/60^\circ$ A, considering no resistance with the neutral.

$R_5 = \frac{4.4}{2.2} = 2$ ohms, 1/2W

$R_6 = 16$ ohms, 1/2W

C = 330 uf, 25V.

(C) DESIGN OF LINELOSS CIRCUITS

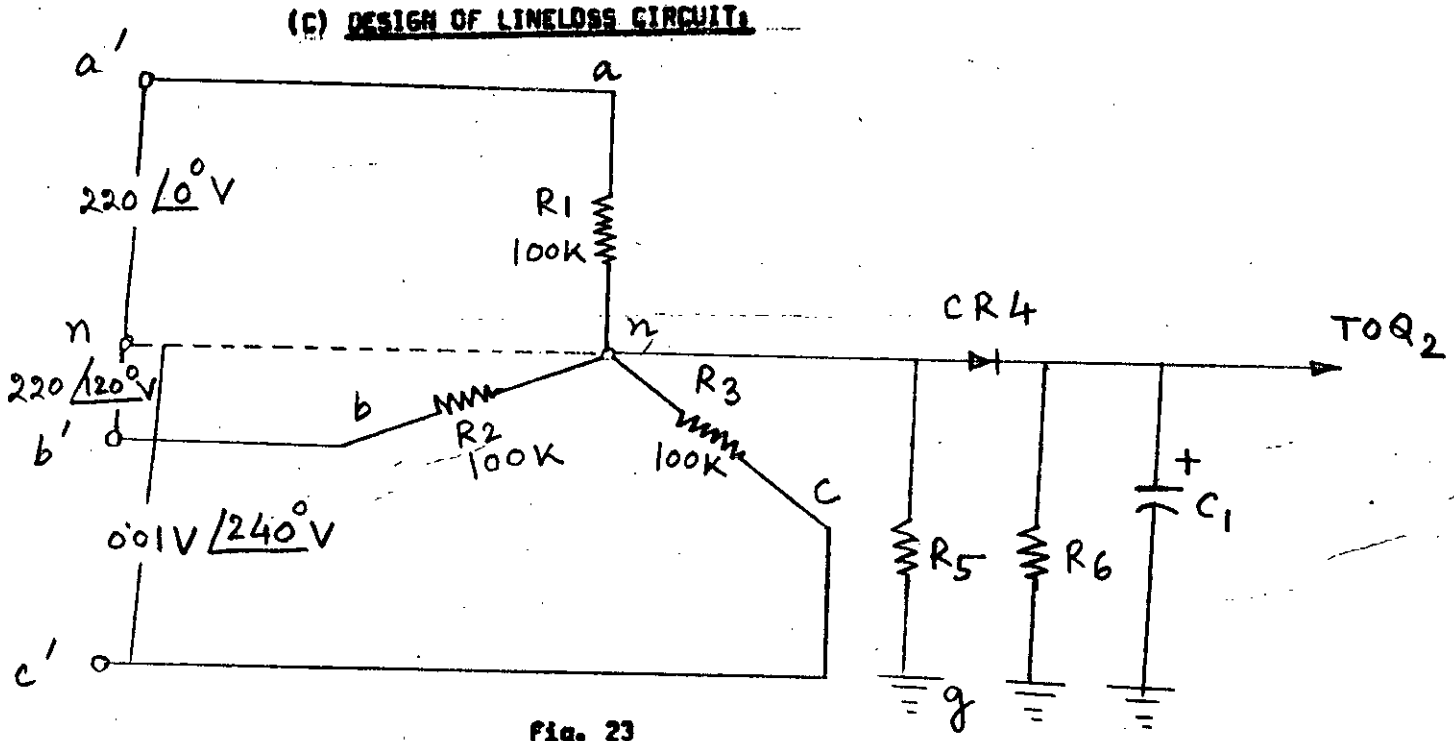


Fig. 23

$$Ia'a = \frac{220\angle 0^\circ}{100\angle 0^\circ} = 2.2\angle 0^\circ A$$

$$Ib'b = \frac{220\angle 120^\circ}{100\angle 0^\circ} = 2.2\angle 120^\circ A$$

$$Ic'c = \frac{V\angle 240^\circ}{100\angle 40^\circ} = 0.01V\angle 240^\circ A$$

Let us consider, for design purpose, voltage after CR_4 to be 5.2V dc.

RMS voltage before CR_4 is $\frac{6.2}{2} = 4.4V$.

By trial and error, let us fix the resistance R_5 to 10K, current through R_5 .

$$Ing = \frac{4.4}{10K} = 0.46 \text{ mA, rms.}$$

When balanced condition exists.

$$Ia'a + Ib'b + Ic'c = 0.$$

When unbalanced condition exists,

$I_{aa'} + I_{bb'} + I_{cc'} = 0.46 \angle 0^\circ \times 10^{-3}$ A.

Considering unity power factor.

$$2.2 \angle 0^\circ + 2.2 \angle 120^\circ + 0.01V \angle 240^\circ = 0.46\ 0 \times 10^{-3}$$

$$0.01V \angle 240^\circ = 0.00046 - 2.2 - 2.2 \angle 120^\circ$$

$$V \angle 240^\circ = 0.046 - 220 - 220 \angle 120^\circ$$

$$V = 0.046 \angle -240^\circ - 220 \angle -240^\circ - 220 \angle -120^\circ$$

$$= 0.046 (-0.5 + j0.866) - 220(-0.5 + j0.866)$$

$$= 220 (-0.5 - j0.866)$$

$$= -0.023 + j0.040 + 110 - j191$$

$$+ 110 + j191$$

$$= 220 + j0.040$$

$$= \sqrt{220^2 + 0.040^2} \qquad \tan^{-1} -\frac{0.04}{220}$$

$$\sim 220 \angle 0^\circ$$

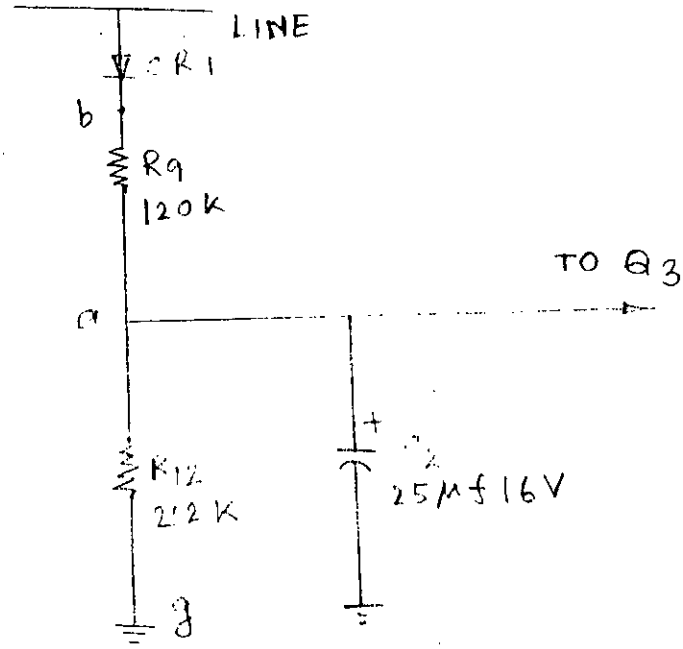
So, we cannot get the result, variation above 220V is negligible.

So, design (B) is more realistic

The overvoltage condition in any phase will cause unbalance to the 3(three) phase system mode. But this unbalance condition will not be sufficient to operate the lineless circuit. So, to operate the line less circuit, complete open or short circuit is necessary in any phase.

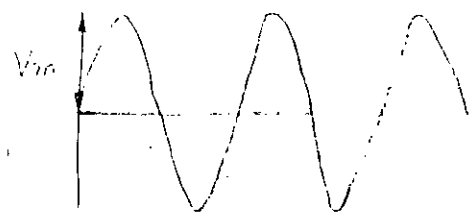
3-8.2. DESIGN OF THE OVERVOLTAGE CIRCUIT:

Overvoltage circuit for phase is shown in figure 24.

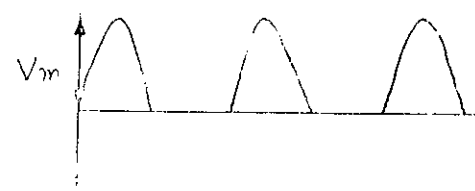


FIG·24

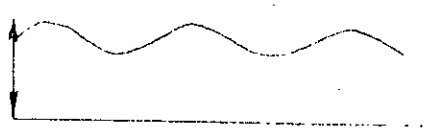
How a perfect dc voltage is obtained by the ac supply is shown in fig. 25.



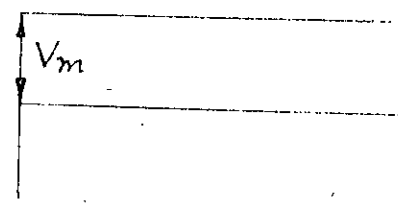
(a) VOLTAGE BEFORE CR1



(b) VOLTAGE AFTER CR1 WITHOUT C2.



(c) VOLTAGE AFTER CR1 WITH C2 CONSIDERING RIPPLES.



(d) NEGLECTING RIPPLES.

FIG·25

Current through CR_1

$$I = \frac{310}{R_9 + R_{12}}$$

Let us assume 6.2v, at point a, when at point b, voltage is 310V, for design purpose.[15]

$$(310-6) : 6 = R_{12} : R_9$$

$$304 : 6 = R_{12} : R_9$$

So, if R_{12} = 30 4K,

R_9 = 6k

Or, if R_{12} = 152K

R_9 = 3 k.

To be on safe side, by trial and error.

We select R_{12} = 120K

and R_9 = 2.2K.

Analysis shows that these should be of 1/2, W rating

CR_1 is selected for 500V rectifier and 3A capacity, because,

Current

$$I = \frac{310}{125} = 2.48A.$$

6.2Vreference is the maximum,It can be varied for 4V to 6.2V.

Design (a)

[11]

Capacitor, C_2 is

$$C_2 = \frac{796000}{150 \times 6 \times 10} = 0.88 \text{ uf}$$

voltage is selected to be 10V for the capacitor.

Similar circuits are constructed for the phases 2 and 3.

Design (b)

$$C_2 = \frac{1 \times 10^{-3} \times 20 \times 10^{-3}}{1} = 20 \text{ uf, } 10V.$$

Where $\Delta v = 1V$.

Design (b) is prefered.

The designed circuit is shown in figure 14.

[15]

Limit of overvoltage range:

$$V_1 : V_2 = 120 : 2.2.$$

When reference is 4V, the circuit breaker will trip when

$$V_2 = 4V.$$

So, $V_1 : 4 = 120 : 2.2.$

$$V_1 = 220V.$$

When reference in 6.2V, the circuit breaker will trip when $V_2 = 6.2V$.

$$V_1 : 6.2 = 120 : 2.2$$

$$V_1 = 340V.$$

So, overvoltage limit may be fixed to any value from 220V to 340V.

3-8.3. DESIGN OF THE POWER SUPPLY CIRCUIT:

The Power supply circuit is shown in figure -26.

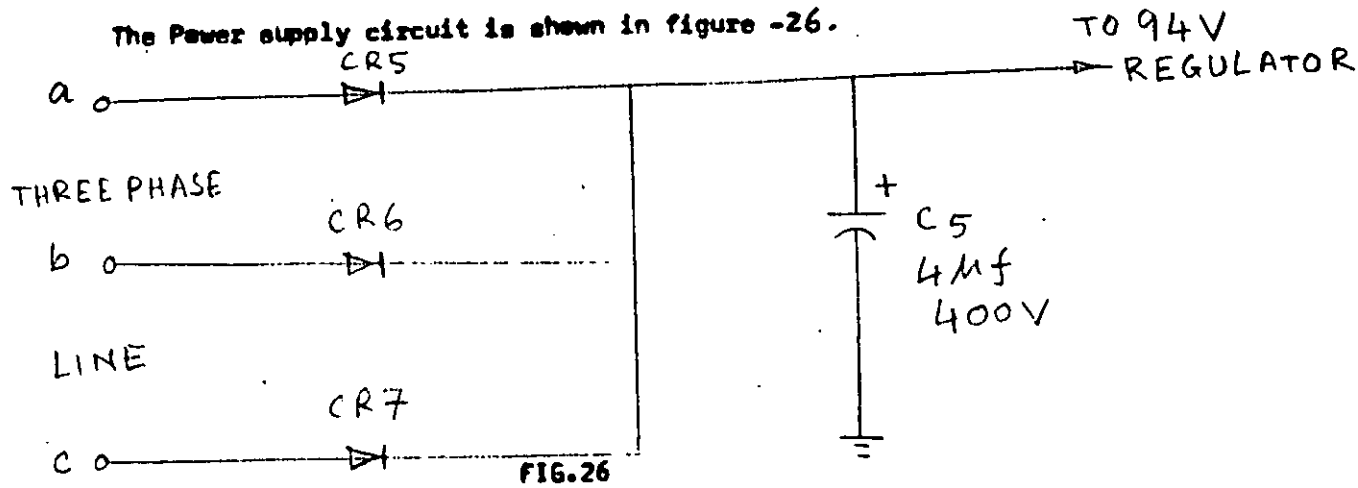


FIG.26

The simple three phase halfwave rectifier circuit is preferred against bridge rectifier circuit by consideration of the application. [15]

Diodes CR_5, CR_6, CR_7, from the Rectifier.

These diodes are selected for rating of 580V rms. Because of momentary short circuit in the circuit, infinite current will flow, through the diodes, so a resistance is used in series with the circuit breaker trip coil.

The rectified voltage, has the magnitude after filtered by C_5, $V_m = 400\sqrt{2} = 565V$.

So, the diodes are selected for 500V rms. i.e. 705V max. To limit the current through the diodes to 5A, a Resistance is required to be connected in series with the circuit breaker trip coil. So, R_{se} + RTC = Series Resistant+TC resistance.

$R = R_{se} + R_{TC}$ = 113 ohms ~ 115 ohms, 5W.

New, voltage rating of C_5 to be selected is 600 V.

$$C_5 = \frac{796000}{150 \times 1 \times 10} = 5.3 \sim 5 \text{ uf.}$$

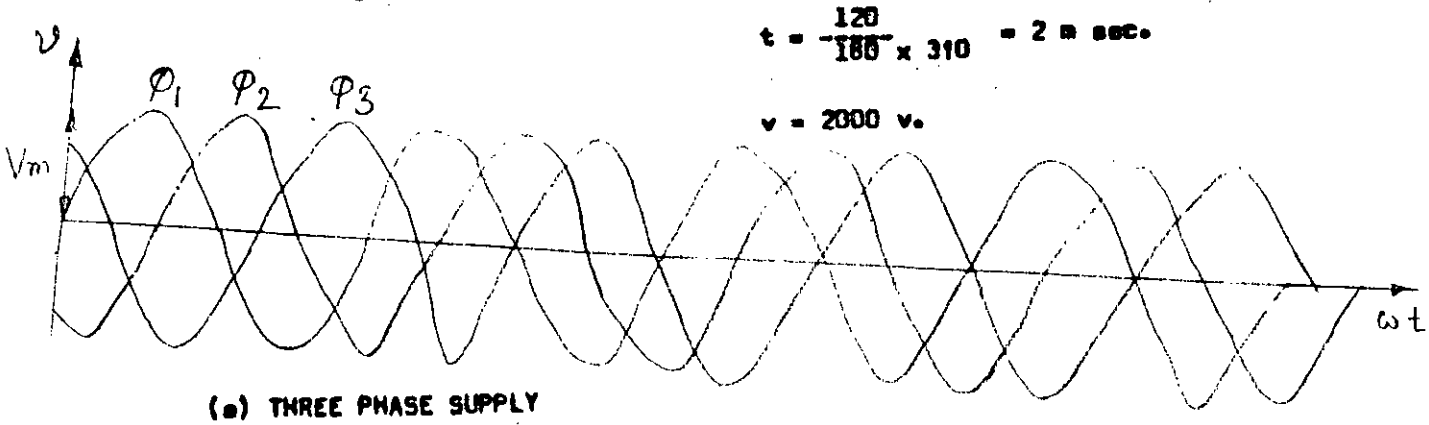
Supposing load to the power supply to be 1K, for design purpose.

Design (b)

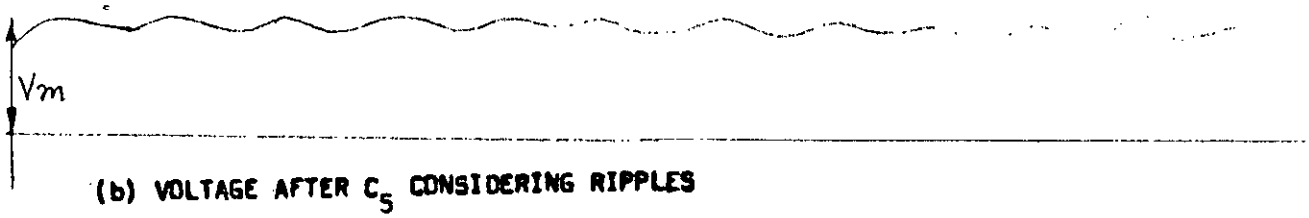
$$C_5 = \frac{5 \times 2 \times 10^{-3}}{2000} = 5 \text{ uf} \qquad 2 \text{ ft} = 120^{\circ}$$

$$t = \frac{120}{180} \times 310 = 2 \text{ m sec.}$$

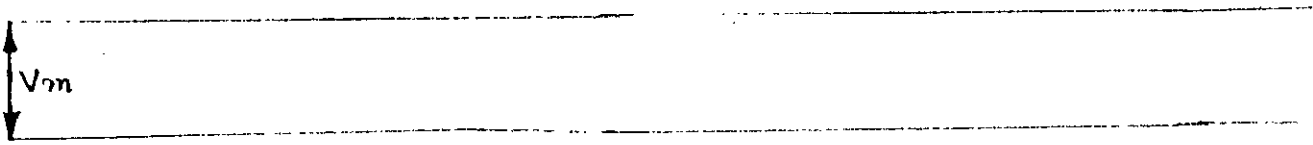
v = 2000 v.



(a) THREE PHASE SUPPLY



(b) VOLTAGE AFTER C_5 CONSIDERING RIPPLES



(c) NEGLECTING RIPPLES.

Fig.27.

500 V, charging of capaciter to be on safe side, 4 times, Δv = 2000V

Design (b) is preferred.

How a perfect dc voltage is obtained from three phase ac supply is shown in fig. 27.

3.8.4. DESIGN OF THE 94 V REGULATOR CIRCUIT

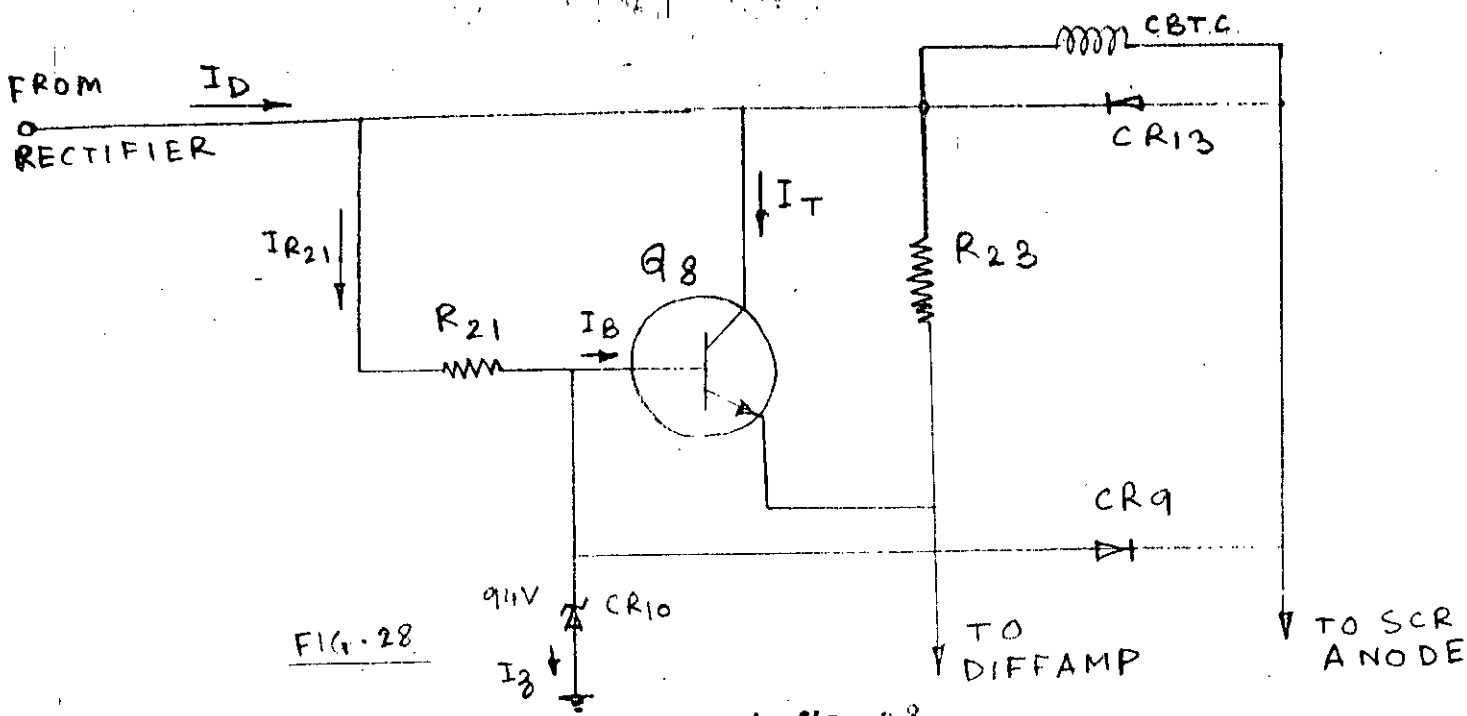


FIG. 28

The designed circuit is shown in fig - 2.8.

The simple shunt regulator by CR_{10}, will cause diode current significant and large changes in diode current produces significant changes in load voltage. The operation is improved by using the transistor Q_8, for current amplification. The combination of transistor Q_8, diode CR_{10} and Resistor R_{21} and R_{23} can be considered to be a composite shunt regulator device. [16]

The current of the composite device is [1]

$$I_D = I_T + I_{R21} = h_{fe} \; I_B + \frac{565}{R21} \; hfe.$$

$$= hfe \left(IB + \frac{565}{R21} \right)$$

Thus the diode current and diode current changes for the circuit as well as output voltage changes will be about 1/hfe smaller than similar quantities without the transistors Q_8.

V_{LO} = Operating (nominally constant) load voltage.

= 94V

I_L = 1 mA.

V_{ss} = Supply voltage = 565V

T = 25°C

RS = Source resistance = 0 ohms.

The series transistor must have a power rating of $P_T = 565 \times 10^{-3}$ W

$= 0.565$ W

The transistor, MJE13003 is suitable hfe = 100

$$R_{21} = \frac{565 - 94}{10 \times 10^{-3}} = \frac{471}{10 \times 10^{-3}} = 47.1K.$$

50K, 2W

Power. $P = 471 \times 10 \times 10^{-3} = 4.71$ W

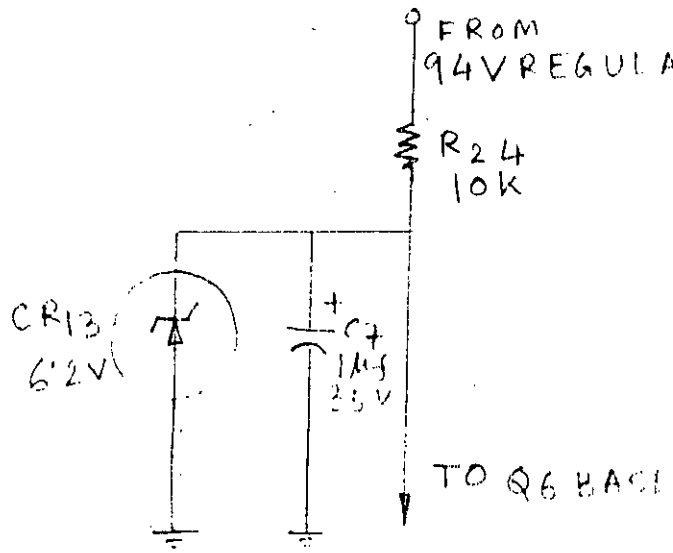
$$R_{23} = \frac{94}{2 \times 10^{-3}} = 46K \sim 50K, 2W.$$

$P = 94 \times 2 \times 10^{-3} = 0.2W.$

94V is selected as regulated voltage which is 1/6th of 565V.

Diode CR_8 and CR_9 are for over load protection.

3-8.5. DESIGN OF THE 6.2V REGULATOR CIRCUIT:



$$94 = 10\times10^{3}\times I + 6.2$$

$$I = \frac{88}{10 \times 10^{-3}} = 8.8 \text{ mA.}$$

$$\simeq 10 \text{ mA.}$$

FIG. 29

The designed circuit is shown in fig. 29. [16]

The reference is arbitrarily chosenas 6.2V. So, 6.2V zener diode is used.

Power is P=6.2x 10 mA = 62 mW.

In 821A, Zener has got these characteristics.

R_{24} is selected 10K, 1W arbitrarily which will drop some voltage before the regulator and limit current.

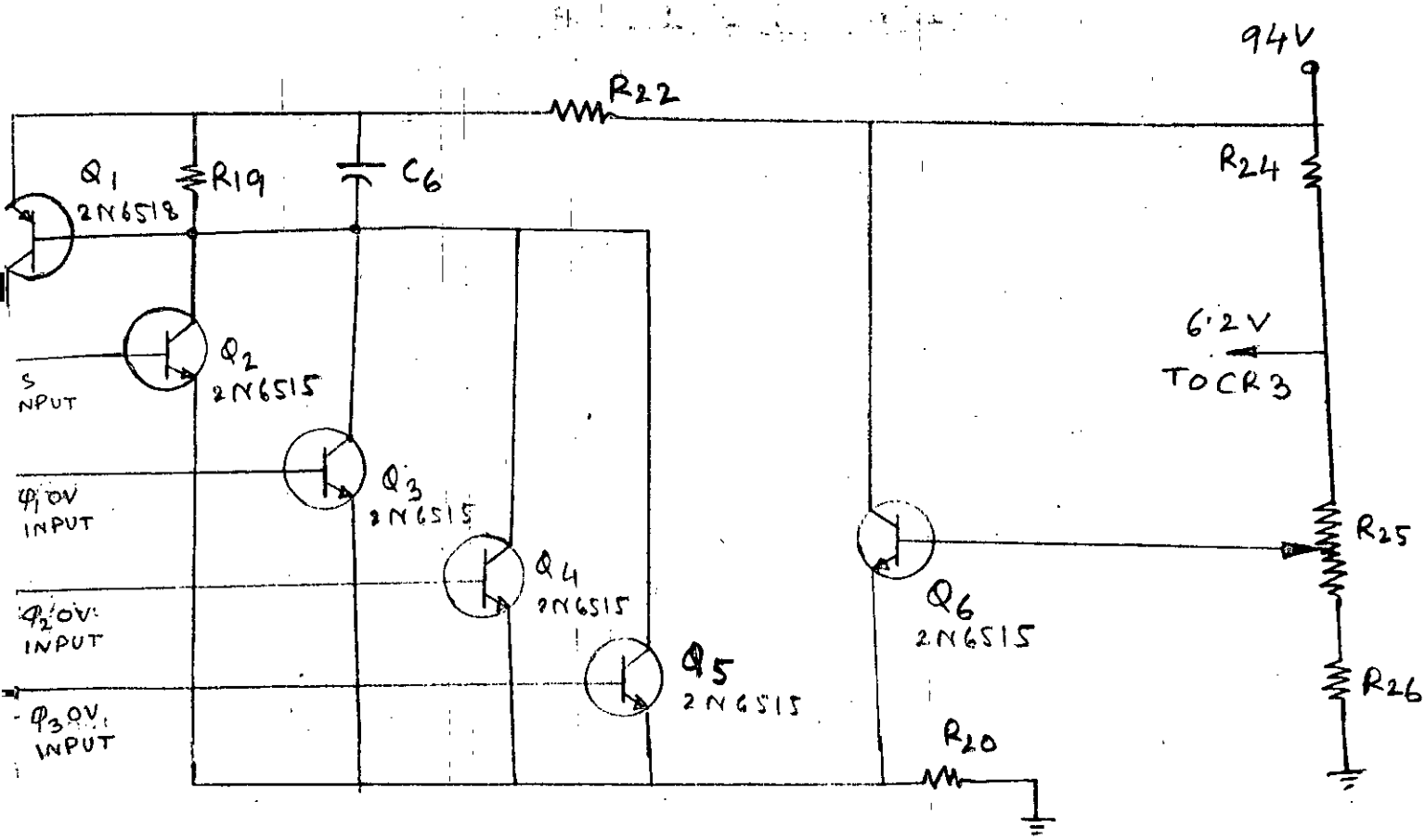
$$C_7 = \frac{I \ \Delta t}{\Delta V} = \frac{0.8 \times 10^{-3} \times 20 \times 10^{3}}{6}$$

$$= 1 \text{ uf}, \quad 10V$$

R_{22} = 2K, 1/32W arbitrarily chosen to limit current and to drop some voltage before the latch.

CR_{12} is for overvoltage protection 250V, 1A.

-8.6 : DESIGN OF THE DIFFERENTIAL AMPLIFIER:



FIX. 30

The designed circuit is shown in fig. 30 .

C_6 is bypass capaciter.

R_{19} is bias resister, 10K, 1/2W.

$C_6 = \frac{1\ \Delta t}{\Delta V}$ [1] . Here we can take it 0.1 uf.

The transisters will have to withstand the voltage of about 75V. So, approximately 3 times rating i.e. of 250V transisters are required 1W.

2N 6515 for NPN-Si transistor are used.

2N 6518 for PNP-Si transistor are used.

R_{20} = 10K, 1/2W.

The voltage to the base of transistor Q_6 can be varied from 4V to 6V by the variable resistor R_{25} and R_{26} is the current limiter, arbitrarily chosen as 5 K.

C_8 is the filter capacitor chosen as 0.01 uf, 25V.

Say, the base voltage to Q_6 is 5V. This 5V through the emitter appears across R_{20} with a drop of 0.7V.

i.e. $V_{R20} = 5 - 0.7 = 4.3V$.

But the voltage is required to reach 6.2V.

This reference voltage of 4.3v will prevent L.S, ϕ_1 0V, ϕ_2 0V and ϕ_3 0V to appear across R_{20}, and 4.3 V will not appear at the base of Q_2, Q_3 and Q_4. When L.S. or ϕ_1 0V or ϕ_2 0V or ϕ_3 0V will exceed (4.3 + 0.7 = 5V) the reference voltage of 5V, the full voltage across R_{28} will be from Q_2 or Q_3 or Q_4 or Q_5. This base current of Q_2, Q_3, Q_4 or Q_5, will cause collector current of the corresponding transistor to increase sharply. This sharp increase of collector current will flow through the base of Q_1 which will cause sharp increase of collector current of Q_1, which will have forward path through emitter of Q_2 and R_{20}, when a sharp increase of voltage will happen across R_{20}. [2]

$I_C = hfe\ IB$.

3-8.7 DESIGN OF THE SCR CIRCUIT:

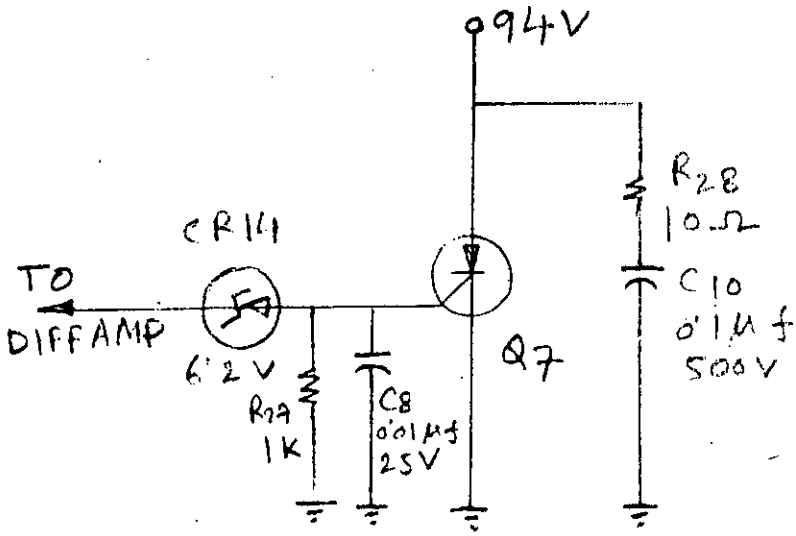


FIG.31

The designed circuit is shown in fig. 31.

From previous consideration, the SCR Q7 is selected for 10A rating. Because, we limited the current to 5A. So, double is taken for rating. Voltage rating is 1000V.

After the voltage of R_{20} exceeds 6.2V. CR_{14} will breakdown and current across R_{27} is 1k by trial and error method, C_9 0.01 uf 25V is a bypass capacitor, arbitrarily chosen.

High $\frac{dv}{dt}$ will short circuit the SCR, which is dangerous for it. So, the Snubber R_{28} and C_{10} are used to protect the SCR from high dv/dt. At the time of triggering of SCR and tripping of the circuit breaker, high dv/dt will appear across the SCR.[7]

During the high dv/dt condition a parallel circuit consisting of R_{28} and C_{10} is provided to share the current which would otherwise flow through the SCR.

$$\frac{dv}{dt} = \frac{1}{C} \quad \frac{dQ}{dt} = \frac{1}{C} \; 50 \times 10^{-3} = \frac{565}{1 \times 10^{-3}}$$

$$C = \frac{10^{-3} \times 5}{565} = 0.01 \times 10^{-3} \times 10^{-2}$$

$$= 0.1 \text{ uf}$$

A low resistance R_{28} = 10 ohms is selected to limit the current through the capacitor for the safety of the capacitor. [8]

CHAPTER - IV

4-1. DISCUSSION

4-1. DISCUSSION:

The need for a stable ac power supply needs no emphasis. Changes in the supply voltage levels above and below the nominally declared value, if it exceeds a certain limit may cause series problems. For continuous and precision operation and protection of the system concerned, voltage regulators are essential.

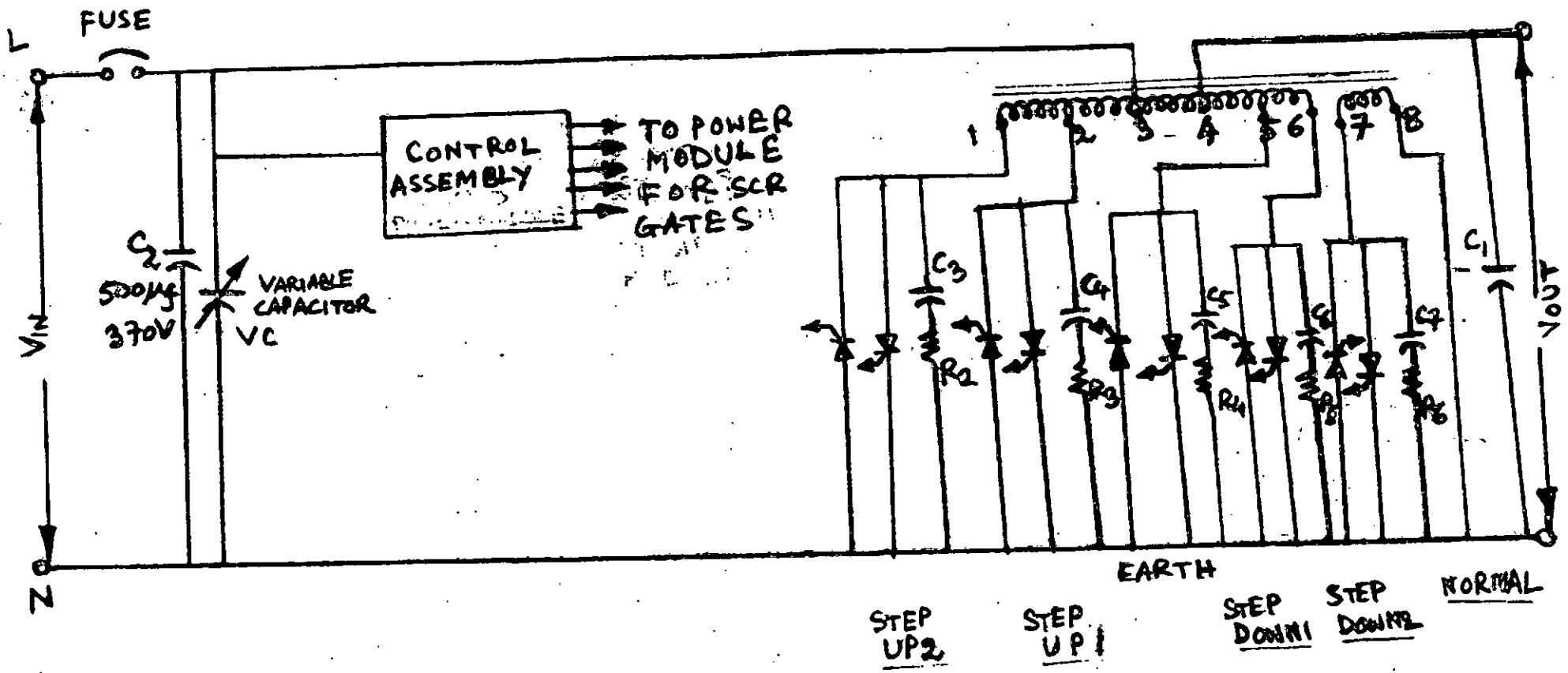
The single phase regulator circuits is shown in fig. 32.

The range of output variation is equal to steps of the input voltage to be regulated. i.e. if the nominally declared output value is 220V and the input variation is from 200 to 250V. The input voltage range may be divided in six or eleven equal steps. The steps may be 200V - 210V-230V-240V-250V or 200V-205V - 210V- 215V- 220V-225V-230V-235V-240V-245V-250V. In the former case output will vary from 210 to 230V i.e. percentage variation is $\frac{230 - 220}{220} \times 100\% = \pm 5\%$ and in the later case, the output will vary from 215V to 225V i.e. percentage variation is $\frac{225 - 220}{220} \times 100\% = \pm 2.5\%$. So, the more the steps, the closer the output value around the nominally declared value.

Voltage regulators are designed either to control continuously the output voltage by using buck and boost transformer or to control in steps the output voltage by using tap switches. In both cases electronic control circuits are employed either to adjust the position of the servos or to select the right tap.

The voltage regulator designed by us will provide an output which

REGULATOR-ONE PHASE



C1, C2 AND VC ARE FOR POWER FACTOR CORRECTION.

FIG. 32.

will remain with ± 5% the declared voltage even if the supply voltage varies from 200 V to 250V. The regulator will be useful for domestic use (i.e. for refrigerators, television etc.), Computers, control equipments in industrial units, scientific and communication equipment etc.

A major problem with this type of tap-changer is the fact that the time at which thethyristor ceases to conduct is affected by the load power factor.[6] This results in either preventing a tap change due to reverse bias on the thyristor to be triggered or causing a short circuit between taps via two thyristors. This is true for an inductive as well as capacitive loads. So, the input power factor must be improved before feeding the regulator.

Another problem which was mentioned earlier is that when only three taps are provided (which is the minimum number of N) the range of output variation is a maximum. So, to keep the output voltage very close to the normally declared value, the number of taps provided to the regulator-transformer must be maximum.

Another disadvantage of the tap changer is that it produces considerable distortion and this distortion is at a maximum at nominal input voltage. To alter this distortion characteristic, additional transformer taps must be used and this will increase the number of thyristors, Gates, Flipflops, Comparators etc.

The neccessity of AVR for different installations and equipments in our country is quite high. For lack of AVR, valuable equipments are getting damaged or cannot be operated usefully.

It is a fact that practical AC regulators using solid state devices are available in the market, but the supplier never gives the intricate design processes which is the heart of the operation of the system. Our investigation on this project will help us to explore the intricate design processes of the regulator.

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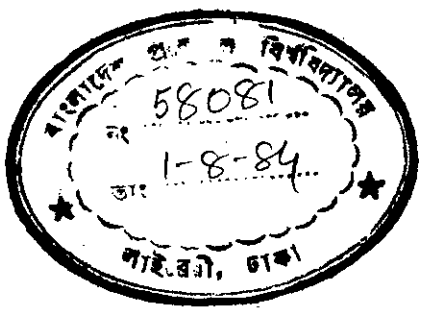

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